INTEGRATED CIRCUITS

Semiconductors for Wireless Communications



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Data Handbook IC17a
1998

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Short-form specification	The data in this specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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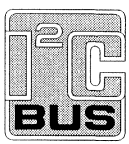

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

PREFACE

Semiconductors for Wireless Communications

Welcome to the latest edition of our Data Handbook "Semiconductors for Wireless Communications". Wireless communications is one of the fastest growing markets segments in the electronics business today. And no one has more to offer in this area than Philips Semiconductors. We supply semiconductor components for everything from cordless, cellular and paging products to exciting new applications, like wireless LAN, Personal Communications Systems (PCS), Global Positioning System (GPS), audio products, industrial control, security systems, and more.

What better place to start, therefore, with your search of wireless communication devices than with this Data Handbook. To make selections easier, we have split the book into two parts, parts a and b. In part a, you'll find IC selection charts, wireless system solutions and all our current wireless semiconductor data sheets. As a further aid, we can also supply all these data sheets on a separately available CD-ROM. To supplement this data, part b of the Data Handbook contains a selection of wireless application reports. These reports give detailed design examples, in-depth system information and practical advice on how to get the most from our wireless semiconductors.

For more information on how we can help with your wireless designs, or to speak to a local sales representative, in the U.S. call 1 800 447 1500, ext. 1253; in Europe fax +31 40 272 4825; in Asia/Pacific fax +852 319 7890, or in Japan fax +81 3 3740 5057. Or visit our worldwide web site at http://www.semiconductors.philips.com

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The following type numbers were included in the previous issue of this data handbook, but are not in the current edition.

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CGY2011G	Nearest replacement: CGY2013G
CGY2023G	Nearest replacement: CGY2021G
NE570	Replaced by SA570
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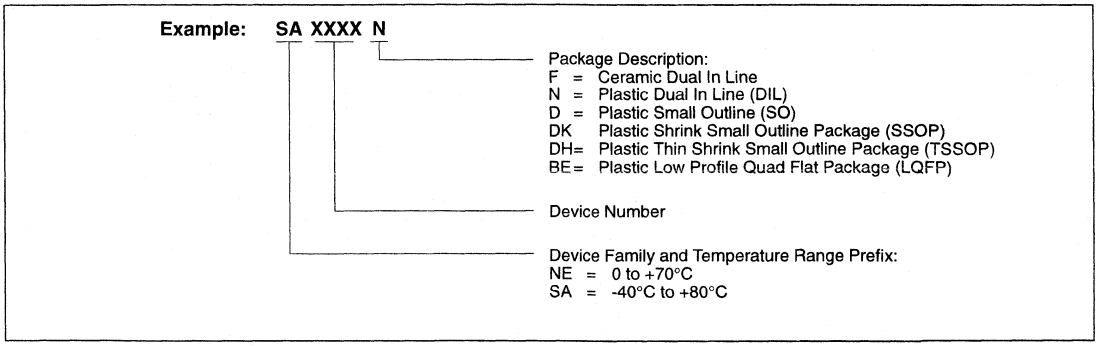
NE575	Replaced by SA575
NE576	Replaced by SA576
NE577	Replaced by SA577
NE578	Replaced by SA578
NE600	Replaced by SA600
NE602A	Replaced by SA602A
NE604A	Replaced by SA604A
NE605	Replaced by SA605
NE612A	Replaced by SA612A
NE614A	Replaced by SA614A
NE615	Discontinued
NE624	Replaced by SA624
NE625	Replaced by SA625
NE627	Replaced by SA627
NE630	Replaced by SA630
NE5200	Replaced by SA5200
NE5204A	Replaced by SA5204A
NE5205A	Replaced by SA5205A
NE5209	Replaced by SA5209
NE5219	Replaced by SA5219
NE/SA5750	Discontinued
NE/SA5751	Discontinued
PCA5097	Discontinued
PCD5032	Is not widely promoted
PCD5090	Discontinued
PCD5097	Is not widely promoted
PCF5075	Replaced by PCD5077
TDA8780M	Discontinued
UAA2072M	Replaced by UAA2043M

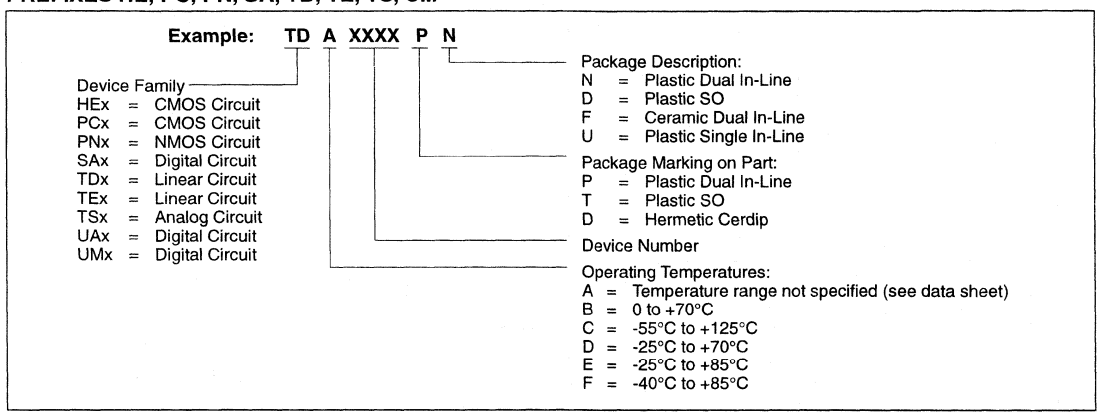
TYPE NUMBER	REASON FOR DELETION
UMA1005T	Not widely promoted
UMA1014	Not widely promoted. Nearest replacement: UMA1015AM
UMA1017M	Not widely promoted. Nearest replacement: UMA1020M
UMA1019AM	Discontinued. Nearest replacement: UMA1021M
UMA1019M	Discontinued. Nearest replacement: UMA1021M
UMA1020AM	Discontinued. Nearest replacement: UMA1021M

Ordering Information

COMMUNICATION PRODUCT GROUP RF PART NUMBERING SYSTEM



PHILIPS PRODUCTS PART NUMBERING SYSTEM
PREFIXES HE, PC, PN, SA, TD, TE, TS, UM



System Standard—Product Selector Guide

PRODUCTS			TARGET SYSTEMS															
			Cellular							Cordless					Wireless Data			
Function	Type	Description	(N)AMPS /(E) TACS	IS–54/–136 TDMA	IS–95 CDMA	GSM	DCS1800	PCS	PDC	CTO	CT1	SS	DECT	PHS	802.11	CDPD	PAGERS
RF Amplifiers											X	X					
	SA5200	Gain block–1 GHZ										X				X	
RF Front End																	
	SA611	1 GHz low volt LNA and mixer	X	X	X				X			●			●		
	SA2420	2.45GHz low voltage RF transceiver										●			●		
	SA621	1GHz low volt LNA, mixer and VCO	●	●	●				X			●					
	SA1620	Low voltage GSM RF transceiver				●											
	SA1921	Satellite/Cellular dual–band RF front–end				●											
	SA1920	PCS/Cellular dual–band RF front–end		●				●									
	UAA2073(A)M	Image reject GSM front–end				●											
	UAA2077AM	Image reject front–end for DECT											●				
	UAA2077BM	2GHz image reject front–end					●										
	UAA2077CM	2GHz image reject front–end						●									
	UAA2067G	Image reject 1.8GHz for DECT											●				
	UAA2080T	Advanced pager receiver															X
	UAA2082	Advanced pager receiver															●
Synthesizers/Prescalers																	
	UMA1015AM	Low–voltage, dual–1GHz	●								●					●	
	UMA1018M	Low–voltage, single loop–2 GHz	X		●	●											
	UMA1020M	Low–voltage, low noise–2.2 GHz						X					●	X	●		
	UMA1021M	Low–voltage, very low noise–2.2 GHz				●	●	●	●			●	●	●	●		
	UMA1022	Low voltage, very low noise–2.2 GHz				●	●	●	●			●	●	●	●		
	SA7025	Low–voltage, Fractional–N—1.04 GHz		●		X			●			●					
	SA8025A	Low–voltage, Fractional–N—1.8 GHz		●	●			●	●			●					
	SA7016	1.3GHz low voltage fractional–N synthesizer	●	●	●	●			●			●				●	
	SA8016	2.5GHz low voltage fractional–N synthesizer		●			●	●	●					●	●		
	SA7026	1.3GHz low voltage fractional–N dual frequency synthesizer	●	●	●	●			●			●				●	
	SA8026	2.5GHz low voltage fractional–N dual frequency synthesizer		●			●	●	●					●	●		

FSystem Standard—Product Selector Guide

PRODUCTS			TARGET SYSTEMS															
			Cellular							Cordless					Wireless Data			
Function	Type	Description	(N)AMPS /(E) TACS	IS–54/–136 TDMA	IS–95 CDMA	GSM	DCS1800	PCS	PDC	CTO	CT1	SS	DECT	PHS	802.11	CDPD	PAGERS	
Mixer/IF/Demod																		
	SA605	High perf/wide BW mixer FM/IF	X	X								X	X	X	X	X		
	SA606/7/8	Low–voltage, high perf mixer FM/IF	●	●						●	●					●		
	SA626	Low–voltage/Wide BW/fast RSSI										●		●				
	SA636	SA626 with Wideband data output											X		●	●		
	SA637	SA626 with Digital IF		●				●										
	SA639	Low–voltage mixer FM/IF w/switch										X	●		●			
	SA1630	Low voltage transceiver w/74 dB VGA							X			X			●			
	SA1638	Low–voltage GSM IF transceiver				●												
	SA647	IF Digital Receiver		●				●										
Power Amplifiers and Transmitters																		
	SA900	I/Q transmit modulator		●								X						
	SA910	Variable gain RF predriver amplifier	●									X						
	SA2410	2.45 GHz PA and T/R Switch													●			
	SA9025	Transmit modulator with 2.2 GHz fractional–N synthesizer integrated		●				●										
	CGY2013	GSM 4W power amplifier				●												
	CGY2021	DCS/PCS 2W power amplifier					●	●										
	CGY2030	DECT 0.5W power amplifier											●					
	CGY2032	DECT 0.5W power amplifier											●					

"●" = Recommended part–type/system solution

"X" = Alternate solution

Front-end, Integrated (high performance) Selection guide

FRONT-END, INTEGRATED CIRCUITSE

	DESCRIPTION[3]	V_{CC} (V)	I_{CC} (mA)	PINS	Pkg[2]	INPUT FREQUENCY
Image Reject Front-End Systems						
SA1920	Dual-band 800/1900 MHz LNA + IRM + IFamp.	3.6 – 3.9	HB Rx : 41.1 HB Tx : 21.3 @ 3.75 V	48	BE	869 – 960 MHz or 1.93-1.99 GHz
SA1921	Dual-band 900/1550 MHz LNA + IRM + IFamp.	3.6 – 3.9	HB Rx : 38.6 HB Tx : 18.8 @ 3.75 V	48	BE	935 – 960 MHz or 1.525 – 1.559 GHz
UAA2067G	LNA + IRM + Mod. + VCO	3 – 5.5	Rx : 24 Tx : 42 @ 3.6 V	32	BE	1.8 – 1.9 GHz
UAA2077AM	LNA + IRM	3.15 – 5.3	27 @ 4 V	20	DK	1.8 – 1.9 GHz
UAA2077BM	LNA + IRM + Tx down-convert mixer	3.6 – 5.3	Rx : 27 Tx : 14 @ 4 V	20	DK	1.8 – 2 GHz
UAA2077CM	LNA + IRM + Tx down-convert mixer	3.6 – 5.3	Rx : 36 Tx : 14 @ 3.75 V	20	DK	1.8 – 2 GHz
Image Reject Front-End Systems						
UAA2073M	LNA + IRM + Tx down-convert mixer	3.6 – 5.3	Rx : 26 Tx : 12 @ 3.75 V	20	DK	925 – 960 MHz
UAA2073AM	LNA + IRM + Tx down-convert mixer	3.6 – 5.3	Rx : 26 Tx : 12 @ 3.75 V	20	DK	925 – 960 MHz
Integrated Front-End Systems						
SA611	LNA + Mixer	2.7 – 5.5	7 mA @ 3 V @ 3 V	20	DK	LNA 1.2 GHz Mixer 1.2 GHz
SA621	LNA + Mixer + VCO	2.7 – 5.5	12/9.3[1] @ 3 V	20	DK	LNA 1.2 GHz Mixer 1.2 GHz
Mixer Systems						
SA602A	Mixer + Oscillator	4.5 – 8.0	2.4 @ 6 V	8	N, D	500 MHz
SA612A	Mixer + Oscillator	4.5 – 8.0	2.4 @ 6 V	8	N, D	500 MHz

Front-end, Integrated (high performance) — Selection guide

POWER GAIN (dB)	NOISE FIGURE (dB)	INPUT IP3 (dBm)	1 dB COMP. (dBm)	IMAGE REJECTION (dB)	INPUT IMPED.	OUTPUT IMPED.	FEATURE HIGHLIGHTS
F_{RF} = 2 GHz							
22	4.5	LB : 9 HB : 12	24 – 25	35	50 Ω	50 Ω	Dual-band 800 MHz & 1.9 GHz Tripple-mode AMPS/DAMPS/PCS
22	4.5	LB : 9 HB : 12	24 – 25	35	50 Ω	50 Ω	Dual-band 900 MHz & 1.5 GHz
30	5.8	–25	–33	34	190 Ω 0.8 pF diff.	50 Ω asym.	RF to IF DECT transceiver (DSH)
20	4.3	–17	–22	32	60 Ω 1 pF diff.	1 kΩ diff.	3.15 V, 4.3 dB DECT front-end (DSH)
20	4.3: DCS	–17	–23	32	60 Ω 1 pF diff.	1 kΩ diff.	DCS 1800 front-end
22	3.8: DCS 4.0: PCS	–17	–24	38	60 Ω 0.8 pF diff.	1 kΩ diff.	PCS1900/DCS1800 front-end
F_{RF} = 900 GHz							
23	3.25	–15	–23	37	150 Ω 1 pF diff.	1 kΩ diff.	3.6 V phase 2 GSM receiver
22	3.6	–15	–23	45	150 Ω 1 pF diff.	1 kΩ diff.	GSM high IF
F_{RF} = 900 GHz							
15/–20[1]	1.9	–5/+25[1]	–16		50 Ω	50 Ω	• Low voltage • Exellent Noise Figure • LNA Overload Mode
Mixer 1.2 GHz	7	9.5	+4	–9		50 Ω	
15/–20[1]	1.9	–5/+25[1]	–16		50 Ω	50 Ω	• Low Voltage • Excellent Noise Figure • LNA Overload Mode
7	9.5	+4	–9		50 Ω	High	• Low Phase-Noise • Internal VCO
Mixer F_{RF} = 45 MHz							
17	5.0	–13	–25		1.5 kΩ	1.5 kΩ	• Excellent Noise Figure • High Gain
17	5.0	–13	–25		1.5 kΩ	1.5 kΩ	• Excellent Noise Figure • High Gain

Front-end, Integrated (high performance) — Selection guide

	DESCRIPTION[3]	V_{CC} (V)	I_{CC} (mA)	PINS	Pkg[2]	INPUT FREQUENCY
RF Amplifiers						
SA5200	Dual Gain Stage	4.0 – 9.0	4.2/95 µA[1] @ 5 V (per) (amplif.)	8	D	DC – 1.2 GHz
SA5204A	Wideband Amp	5.0 – 8.0	25 @ 6 V	8	N, D	DC – 350 MHz
SA5205A	Wideband Amp	5.0 – 8.0	25 @ 6 V	8	N, D	DC – 550 MHz
SA5209	Variable Gain Amp	4.5 – 7.0	43 @ 5 V	16	N, D	DC – 850 MHz
SA5219	Variable Gain Amp	4.5 – 7.0	43 @ 5 V	16	N, D	DC – 700 MHz

Notes

1. Amplifier: Enabled/Disabled
2. Package Descriptions:
   a) D: = Small Outline (SO14/16/20)
   b) N: = Dual In-line (DIL)
   c) DK: = Shrink Small Outline Package (SSOP20)
   d) BE: = Low Quad Flat Package (LQFP)
3. IRM: Image Reject Mixer
   LNA: Low Noise Amplifier
   DSH: Double Superheterodyne
   diff.: differential
   asym.: asymmetrical

Front-end, Integrated (high performance) — Selection guide

POWER GAIN (dB)	NOISE FIGURE (dB)	INPUT IP3 (dBm)	1 dB COMP. (dBm)	IMAGE REJECTION (dB)	INPUT IMPED.	OUTPUT IMPED.	FEATURE HIGHLIGHTS
RF F_{RF} = 900 MHz (NE/SA 5200), 100 MHz (others)							
7.5/13.5[1] (per) (amplif.)	3.6	–1.8	+3.2		50 Ω	50 Ω	• DC to 1.2 GHz Operation • Power- Down Mode
19	6.0 (50 Ω) 4.8 (75 Ω)	–2	+4		50 Ω	50 Ω	• DC to 350 MHz Operation
19	6.0 (50 Ω) 4.8 (75 Ω)	–2	+4		50 Ω	50 Ω	• DC to 550 MHz Operation
25 (voltage)	9.3	+13 (output)	–3		1.2 Ω	60 Ω	• DC to 850 MHz Operaton • Gain Control Pin
25 (voltage)	9.3	+13 (output)	–3		1.2 Ω	60 Ω	• DC to 700 MHz Operation • Gain Control Pin

Notes

1. Amplifier: Enabled/Disabled
2. Package Descriptions:
   a) D: = Small Outline (SO14/16/20)
   b) N: = Dual In-line (DIL)
   c) DK: = Shrink Small Outline Package (SSOP20)
   d) BE: = Low Quad Flat Package (LQFP)
3. IRM: Image Reject Mixer
   LNA: Low Noise Amplifier
   DSH: Double Superheterodyne
   diff.: differential
   asym.: asymmetrical

FRONT-END, DISCRETE

SOCKET	SYSTEM FREQ. (MHz)	I_C (MA)	V_{CE} (V)	F_T (GHz)	GAIN (dB) @ 900 MHz	NOISE (dB) @ 900 MHz	GAIN (dB) @ 1.9 GHz	NOISE (dB) @ 1.9 GHz	PACKAGE				
									SOT23	SOT323	SOT343[1]	SOT353	SOT363
LNA	900	3	4.5	17	20	1	22	1.6			BFG403W		
	900 & 1900	2 – 5	3 – 12	9	17	1.2	10	1.9	BFR505	BFS505	BFG505W	BFC505	BFM505
	900 & 1900	3 – 30	3 – 12	9	17	1.2	10	1.9	BFR520	BFS520	BFG520W	BFC520	BFM520
	900 & 1900	1 – 10	2 – 4.5	22	21	1.2	29	0.9			BFG410W		
	900 & 1900	3 – 25	2 – 4.5	22	20	1.2	28	0.8			BFG425W		
Mixer	900	5 – 30	3 – 10	6	13	1.9			BFR93A	BFR93AW	BFG93AW		
	900 & 1900	2 – 5	3 – 12	9	17	1.2	10	1.9	BFR505	BFS505	BFG505W	BFE505	BFM505
	900 & 1900	3 – 30	3 – 12	9	17	1.2	10	1.9	BFR520	BFS520	BFG520W	BFE520	BFM520
	900 & 1900	1 - 10	2 – 4.5	22	21	1.2	29	0.9			BFG410W		
	900 & 1900	3 – 25	2 – 4.5	22	20	1.2	28	0.8			BFG425W		
Buffer & VCO	900	3 – 20	3 – 10	6	14	2.1			BFR92A	BFR92AW			
	900	5 – 30	3 – 10	6	13	1.9			BFR93A	BFR93AW			
	900 & 1900	2 – 5	3 – 12	9	17	1.2	10	1.9	BFR505	BFS505	BFG505W	BFC505	BFM505
	900 & 1900	3 – 30	3 – 12	8	17	1.2	10	1.9	BFR520	BFS520	BFG520W	BFC520	BFM520
	900 & 1900	1 – 10	2 – 4.5	22	21	1.2	29	0.9			BFG410W		
	900 & 1900	3 – 25	2 – 4.5	22	20	1.2	28	0.8			BFG425W		
IF	40 – 100	3 – 20	3 – 12	1.2	20 dB gain @ 100 MHz				BF547	BF547W			
	100 – 250	3 – 20	3 – 8	2.8	25 dB gain @ 250 MHz				BFS17A	BFS17W			
	>250	3 – 20	3 – 10	5	25 dB gain @ 500 MHz				BFR92A	BFR92AW			

Note

1. Typically the gain is 2 – 3 dB higher in SOT343 packages.

IF SYSTEMS

	V_{CC} (V)	I_{CC}	PINS	Pkg	INPUT FREQ. (MHz)	IF FREQ (MHz)	FRF = 45 MHz		
							INPUT SENSI-TIVITY	MIXER GAIN (dB)	INPUT IP_3 (dBm)
FM IF									
SA604A	4.5 – 8	3.3 mA @ 6 V	16	D,N	25	25	0.22(1)	-	-
SA614A	4.5 – 8	3.3 mA @ 6 V	16	D,N	25	25	0.22(1)	-	-
SA624	4.5 – 8	3.4 mA @ 6 V	16	D,N	25	25	0.22(1)	-	-
Mixer/FM IF									
SA605	4.5 – 8	5.7 mA @ 6 V	20	D,DK,N	500	25	0.22	13	–10
SA615	4.5 – 8	5.7 mA @ 6 V	20	D,DK,N	500	25	0.22	13	–10
SA625	4.5 – 8	5.8 mA @ 6 V	20	D,DK,N	500	25	0.22	13	–10
Low Voltage Mixer/FM IF									
SA606	2.7 – 7	3.5 mA @ 3 V	20	D,DK,N	150	2	0.31	17	–9
SA616	2.7 – 7	3.5 mA @ 3 V	20	D,DK,N	150	2	0.31	17	–9
SA676	2.7 – 5.5	3.5 mA @ 3 V	20	D,DK	100	2	0.45	17	–10
SA607	2.7 – 7	3.5 mA @ 3 V	20	D,DK,N	150	2	0.31	17	–9
SA608	2.7 – 7	3.5 mA @ 3 V	20	D,DK,N	150	2	0.31	17	–9
SA626	2.7 – 5.5	6.5 mA @ 3 V	20	D,DK	500	25	0.54(2)	11(2)	–16(2)
SA636	2.7 – 5.5	6.5mA @ 3V	20	D,DK	500	25	0.54(2)	11(2)	–16(2)
SA639	2.7 – 5.5	8.5 mA @ 3 V	24	DH	500	25	2.24(4)	12(4)	–12.5(4)
Low Voltage Mixer/Digital IF									
SA637	2.7 – 5.5	3.5 mA @ 3 V	20	D,DK	200	2	$\frac{-117\ dBm^3}{0.31\ \mu V}$	7	–17
SA647	2.7 – 5.5	5.9 @ 3 V	20	DK	200	2	–112 dBm	.	–28
SA1630	2.7 – 5.5	Tx: 26.5 Rx: 33.5 @3 V	48	BE	400				
SA1638	2.7 – 5.5	Tx: 22 Rx: 18 @3 V	48	BE	400				

RSSI RANGE (dB)	FAST RSSI	FREQ. CHECK PIN	IF FILTER MATCH (kHz)	OUTPUT OP AMPS	FEATURE HIGHLIGHTS
FM IF					
90	-	-	455	-	• High Sensitivity
80	-	-	455	-	• Wide IF BW
90	x	-	455	-	
Mixer/FM IF					
90	-	-	455	-	• High Sensitivity
80	-	-	455	-	• High Input Frequency
90	x	-	455	-	
Low Voltage Mixer/FM IF					
90	-	-	455	Audio Op Amp RSSI Op Amp	• High Sensitivity
80	-	-	455	Audio Op Amp RSSI Op Amp	• Low Power
70	-	-	455	Audio Op Amp RSSI Op Amp	• Audio Op Amp RSSI Buffered
90	-	x	455	Audio Op Amp RSSI Op Amp	• Audio/RSSI Output Op Amps
90	-	x	455	Audio Buffered RSSI Op Amp	• Power-Down Mode (SA626/636/633)
90	x	-	10.7 MHz	Audio Buffered RSSI Op Amp	
90	x	-	10.7 MHz	RSSI Op Amp	
90	x	-	10.7 MHz	Audio Buffered RSSI Op Amp Post-detect Amp Data Switch	
Low Voltage Mixer/Digital IF					
90	x	-	455 kHz	RSSI Op Amp	
90	x	-	455 kHz	RSSI Op Amp	• Improved mixer gain and sensetivity over SA637
					• Wireless LAN using DSSS modulation • Digital IF Gain Control of 70 dB in steps of 2 dB
					• GSM 900 Mhz • DCS 1.8 GHz • uadrature up & down mixer stage

Notes

1. Measured with a Philips MESA602A mixer prior to the IF input.
2. Measured at f_{RF} = 240 MHz.
3. Represents the –3 dB Input Limiting point (dBm). Also shown in μV units into a 50 Ω matching network.
4. Measured at f_{RF} = 110 MHz.

Temperature Ranges
SA: –40 to +85 °C.

Package DescriptionsIF Filter Match
D:
Small Outline - 16 DK: Shrink Small Outline Package (SSOP) - 20455 kHz = 1.5 kΩ
Small Outline - 20 N: Dual In-Line Plastic - 16, 2010.7 MHz = 330 Ω.

IF Filter Match
455 kHz = 1.5 kΩ
10.7 MHz = 330 Ω.

FREQUENCY SYNTHESIZERS

	V_{CC}	I_{CC}	PINS	Pkt	MAX RF/INPUT FREQ.	CHANNEL SPACING	FRACTIONAL -N DIVIDER	AUXILIARY SYNTHE-SIZER	APPLICA-TIONS
Fractional-N Frequency Synthesizers									
SA 7016DH	2.7 to 5.5 V	5 mA @ 3 V	16	TSSOP 16	1.3 GHz		x		IS-54/-136, IS-95, PDC, GSM digital cellular
SA 7025DK	2.7 to 5.5 V	7.5 mA @ 3 V	20	SSOP 20	1.0 GHz (main) 150 MHz (aux)		x	x	IS-54/-136, IS-95, PDC, GSM digital cellular
SA 7026DK	2.7 to 5.5 V	6.5 mA @ 3 V	20	SSOP 20	1.3 GHz (main) 550 MHz (aux)		x	x	IS-54/-136, IS-95, PDC, GSM digital cellular
SA 8016DH	2.7 to 5.5 V	6.5 mA @ 3 V	16	TSSOP 16	2.5 GHz		x		ISM band, IS-54/-136, IS-95, PDC, GSM digital cellular
SA 8025ADK	2.7 to 5.5 V	11 mA @ 3 V	20	SSOP 20	1.8 GHz (main) 150 MHz (aux)		x	x	PHS digital cordless, U.S. PCS, PDC digital cellular
SA 8026DK	2.7 to 5.5 V	8.5 mA @ 3 V	20	SSOP 20	2.5 GHz (main) 550 MHz (aux)		x	x	ISM band, IS-54/-136, IS-95, PDC, GSM digital cellular

Frequency synthesizers — Selection guide

	V_{CC}	I_{CC}	PINS	Pkt	MAX RF/INPUT FREQ.	CHANNEL SPACING	FRACTIONAL -N DIVIDER	AUXILIARY SYNTHE-SIZER	APPLICA-TIONS
Frequency Synthesizers									
UMA 1015M	2.6 to 5.5 V	9 mA @ 3 V	20	SSOP 20	1.1 GHz 1.1 GHz	5 – 1000 kHz		x (dual)	AMPS/TACS cellular CT1/CT2 cordless
UMA 1015AM	2.7 to 5.5 V	8.7 mA @ 3 V	20	SSOP 20	1.1 GHz	5 – 1000 kHz		x (dual)	AMPS/TACS cellular lower cost replacement of UMA 1015M
UMA 1018M	2.7 to 5.5 V	10 mA @ 5.5 V	20	SSOP 20	1250 MHz (main) 300 MHz (aux)	10 – 2000 kHz		x	GSM digital cellular
UMA 1020M	2.7 to 5.5 V	12 mA @ 5.5 V	20	SSOP 20	2400 MHz (main) 300 MHz (aux)	10 – 2000 kHz		x	DECT digital cordless, DCS 1800, PHS
UMA 1021M	2.7 to 5.5 V	10 mA @ 5.5 V	20	SSOP 20	2200 MHz	10 – 2000 kHz			GSM, WLAN, DECT digital cordless, DCS 1800, PHS
UMA 1022M	2.7 to 5.5 V	13 mA @ 3 V	20	SSOP 20	2200 MHz (main) 500 MHz (aux)	10 – 2000 kHz		x	900 MHz & 2 GHz applic-ations

	V_{CC}	I_{CC}	PINS	Pkt	MAX INPUT FREQ.	MAX COM-PARE FREQ.	INPUT SENSITIVITY	DIVIDE RATIO
Prescalers								
SA 701N,D	2.7 to 6 V	4.5 mA @ 3 V	8	DIP, S08	1.1 GHz	65 kHz/ 270 kHz	–35 dBm	128/129, 64/65
SA 702N,D	2.7 to 6 V	4.5 mA @ 3 V	8	DIP, S08	1.1 GHz	1000 kHz	–35 dBm	64/66/72

TRANSMITTERS ICs

TYPE NUMBER	FREQUENCY RANGE (OUTPUT) (MHz)	FREQUENCY RANGE (SYNTHESIZER) (MHz)	SUPPLY VOLTAGE (V)	I_{CC} (FULL POWER) (mA)	DIFFERENTIAL OUTPUT (dBm)	TRANSMIT OFFSET FREQUENCY (MHz)	PACKAGE	FEATURE HIGHLIGHTS
CELLULAR								
SA900	820 – 860 (AMPS) 820 – 920 (Dual)	N/A	4.5 – 5.1	42 (AMPS) 68 (Dual)	2	90 – 140	LQFP48	BiCMOS I/Q transmit RF modulator with on-chip crystal osc. and VCO
SA9025	820 – 920 (Dual) *1.840 – 1.920 (PCS) with ext. up-conv.*	800 – 2.200	3.6 – 3.9	95 (AMPS) 52(Dual)	11	90 – 180	LQFP48	Higly integrated I/Q transmit RF- modulator with 2.2 GHz dual synth. for 800 & 1900 Tripple mode TDMA

MMICs AMPLIFIERS

TYPE NUMBER	FREQUENCY BAND	SUPPLY VOLTAGE (V)	LOAD POWER (W)	OUTPUT POWER (dBm)	POWER GAIN (dB) MIN.	EFFICIENCY (%)	PACKAGE	FEATURE HIGHLIGHTS
CELLULAR								
CGY2021G	1.71 – 1.785 or 1.85 – 1.91 GHz	4.8	3.2	34	34	55	LQFP48	GaAs MMIC 2 W DCS/PCS Power Amplifier
CGY2013G	880 – 915 MHz	3.6	4	35.5	35.5	45	LQFP48	GaAs MMIC 4 W GSM Power Amplifier
SA910	820 – 905 MHz	2.7 – 5.5	0.5	24	32	35	SSOP20	BiCMOS Low-voltage 900 MHz variable gain pre-amplifier
CORDLESS								
CGY2030M	1.88 – 1.90 GHz	3.6	0.5	27	27	40	SSOP16	GaAs MMIC 500 mW amplifier
CGY2032TS	1.88 – 1.90 GHz	3.6	0.5	27	27	50	SSOP16	GaAs MMIC 500 mW amplifier
WLAN (ISM band)								
SA2410	2.4 – 2.5 GHz	3.0 – 5.5		18.5	29	25	TQFP32	2.5 GHz power amplifier and T/R switch for WLAN (ISM-band)

MODULE AMPLIFIERS

TYPE	FREQUENCY BAND (MHz)	SUPPLY VOLTAGE (V)	MIN. LOAD POWER (W)	DRIVE POWER (mW)	MIN. POWER GAIN (dB)	MIN./TYP. EFFICIENCY (%)	PACKAGE	PACKAGE THICKNESS (mm)
ANALOG CELLULAR - AMPS								
BGY115A	824 – 849	6	1.2	2	27.8	45/50	SOT321	4
BGY118A	824 – 849	4.8	1.2	2	27.8	50/55	SOT321	4
BGY119A	824 – 849	4.8	1.2	2	27.8	50/55	SOT359	3
BGY122A	824 – 849	4.8	1.2	2	27.8	50/55	SOT388	2
BGY120A[1]	824 – 849	3.6	1.2	1	30.8	50/55	NO388	2
ANALOG CELLULAR - (E)TACS								
BGY115B	872 – 905	6	1.2	2	27.8	45/50	SOT321	4
BGY118B	872 – 905	4.8	1.2	2	27.8	50/55	SOT321	4
BGY119B	872 – 905	4.8	1.2	2	27.8	50/55	SOT359	3
BGY122B	872 – 905	4.8	1.2	2	27.8	50/55	SOT388	2
BGY120B[1]	872 – 905	3.6	1.2	1	30.8	50/55	NO388	2
ANALOG CELLULAR - SPREAD SPECTRUM								
BGY115D	902 – 928	6	1.2	2	27.8	45/50	SOT321	4
BGY118D	898 – 928	4.8	1.2	2	27.8	50/55	SOT321	4
BGY119D	898 – 928	4.8	1.2	2	27.8	50/55	SOT359	3
BGY122D[1]	898 – 928	4.8	1.2	2	27.8	50/55	SOT388	2
DIGITAL CELLULAR - GSM								
BGY205	880 – 915	6	3.5	2	32.5	45 (typ.)	SOT321B	3
BGY204	880 – 915	4.8	3.2	2	32.5	45 (typ.)	SOT321B	3
BGY206	880 – 915	4.8	3	3	30	45 (typ.)	SOT388	3
BGY240[1]	880 – 915	3.5	3	1	35	45	SOT388	2

Note

1. Objective specification

DISCRETE AMPLIFIERS

TYPE NUMBER	FREQUENCY (MHz)	SUPPLY VOLTAGE (V)	LOAD POWER (W)	POWER GAIN (dB) MIN.	EFFICIENCY (%)		THERMAL RESISTANCE[3] (K/W)	PACKAGE
					MIN.	TYP.		
ANALOG CELLULAR								
BLT80	900	7.5	0.8	6	60	67	22[4]	SOT223
BLT81	900	7.5	1.2	6	60	70	32[5]	SOT223
BLT80	900	6.0	0.8	7 (typ.)		70	22[4]	SOT223
BLT81	900	6.0	1.2	6.5 (typ.)		70	32[5]	SOT223
BLT70	900	4.8	0.6	6	60		39[6]	SOT223
BLT71	900	4.8	1.2	6	60		24[7]	SOT223
BLT71/8	900	4.8	1.2	11	55	63	50	SOT96
BLT61[2]	900	3.6	1.2	10	50	63	35[8]	SOT96 (SO8pl)
DIGITAL CELLULAR/CORDLESS								
BFG540W	900	6	18 dBm	18				SOT343
BFG540W	1900	3.6	14 dBm	11				SOT343
BFG10W/x	900	6	28 dBm	10				SOT343
BFG10W/x	1900	3.6	20 dBm	6				SOT343
BFG11W/x	1900	3.6	26 dBm	6				SOT343
BFG21W	1900	3.6	0.4	11	50			SOT343
BLT82	900	6.0	3.5	8	50	65	32[9]	SOT96 (SO8pl)

APPLICATION	SUPPLY VOLTAGE (V)	LOAD POWER (W)	1st STAGE	2nd STAGE	3rd STAGE
Analog	6.0	1.2	BFG540W/x	BLT80	BLT81*
	4.8	1.2	BFG540W/x	BLT70	BLT71
	3.6	1.2	BFG520W/x	BFG10W/x	BLT61
	4.8	1.2	BFG10W/x	BLT71/8	
GSM	6.0	3.5	BFG520W/x	BFG10W/x	BLT82
DECT, PHS	3.6	0.4	BFG540/x BFG540W/x BFG425W	BFG10/x BFG10W/x BFG21W	BFG11/x BFG11W/x

Notes

1. Objective specification
2. Preliminary specification
3. Junction to soldering joint
4. P_{tot} = 2 W, T_g = 131 °C
5. P_{tot} = 2 W, T_g = 110 °C
6. P_{tot} = 2 W, T_g = 95 °C
7. P_{tot} = 3.5 W, T_g = 90 °C
8. P_{tot} = 2 W, T_g = 115 °C
9. P_{tot} = 1.9 W, T_g = 115 °C
10. P_{tot} = 1.9 W, T_g = 115 °C
11. P_{tot} = 1 W, T_g = 130 °C.

BASEBAND PROCESSORS

	PART TYPE	APPLICATION	V_{DD}	I_{DD}	PACKAGE
PCD5041	BMC (Burst Mode Controller)	DECT	2.7 – 6.0	15 mA Typ. Active	64-Pin QFP
PCD5042	BMC (Burst Mode Controller)	DECT	2.7 – 6.0	15 mA Typ. Active	64-Pin QFP
PCD5043	BMC (Burst Mode Controller)	DECT	2.7 – 6.0	15 mA Typ. Active	64-Pin QFP
PCD5091/2/3/4/5	Baseband Processor	DECT	2.7 – 3.6	--	QFP 100 LQFP 100
PCD5096	Universal Codec	DECT ISDN	2.7 – 3.6	--	QFP 44
PCF5083	Signal Processor	GSM/DCS/PCS	2.7 – 3.6	--	128-Pin LQFP
PCF507X	Baseband & Audio Interface	GSM/DCS/PCS	2.7 – 3.6	--	80-Pin LQFP
P90CL301	16-bit Low Voltage Micro Controller	GSM/DCS/PCS	2.7 – 3.6	--	
PCF5077	Power Amplifier Controllers	GSM/DCS/PCS	2.7 – 5.5	--	SSOP16
SA5752	Audio Companding VOX and Amplifier	AMPS TACS	2.7 – 5.5	3.1 mA Typ. 125 µA Stdby	20-Pin SOL 20-Pin SSOP
SA5753	Audio Filter and Control	AMPS TACS	3.0 – 5.5	1.7 mA Typ. 600 µA Stdby	20-Pin SOL 20-Pin SSOP
UMA1002	Data processor for cellular radio	AMPS TACS	2.7 – 5.5	0.8 mA Typ.	28-Pin SOL 32-Pin LQFP
PCF5001	POCSAG decoder	PAGERS	1.5 – 6.0	60 µA Typ.	28-Pin Mini-Pack 32-Pin QFP
PCD5002	APOC1/POCSAG decoder	PAGERS	1.5	50 µA Typ.	32-Pin LQFP
PCD5003	Advanced POCSAG paging decoder	PAGERS	1.5 – 6.0	50 µA Typ. (ON) 25 µA Typ. (OFF)	32-Pin LQFP
PCD5008	FLEX decoder	PAGERS	1.8 – 3.3	6.8 µA Typ.	32-Pin LQFP

COMPANDORS

	V_{CC}	I_{CC}	PINS	PACKAGES	ALC	REFERENCE VOLTAGE	UNITY GAIN	POWER DOWN	KEY FEATURES	APPLICATIONS
SA570	6 – 24 V	3.2 mA	16	D, F, N	Both channels	Fixed 1.8 V	775 mVms	No	-Excellent unity gain tracking error -Excellent THD	High Performance Audio Circuits "Hi-Fi Commercial Quality"
SA571	6 – 18 V	3.2 mA	16	D, F, N	Both channels	Fixed 1.8 V	775 mVms	No	-Excellent unity gain tracking error -Excellent THD	High Performance Audio Circuits "Hi-Fi Commercial Quality"
SA572	6 – 22 V	6 mA	16	D, F, N	Both channels	Fixed 2.5 V	100 MVms	No	-Independent attack & release time -Good THD -Needs an ext summing op amp	High Performance Audio Circuits "Hi-Fi Studio Quality"
SA575	3 – 7 V	3 – 5.5 mA(1)	20	D, DK, N	Right channels	$V_{CC}/2$	100 mVms	No	-2 Uncommitted on-chip op amps available -Low voltage	Consumer Audio Audio Circuits "Commercial Quality"
SA576	2 – 7 V	1 – 3 mA(1)	14	D, N	Right channels	$V_{CC}/2$	100 mVms	No	-Low power -Low external component count	Battery Powered Systems "Commercial Quality"
SA577	2 – 7 V	1 – 2 mA(1)	14	D, N	Right channels	$V_{CC}/2$	10 mV to 1 V(rms)	No	-Low power -Programmable unity gain	Battery Powered Systems "Commercial Quality"

SA578	2 – 7 V	1 – 2 mA[1]	16	D, N	Right channels	$V_{CC}/2$	10 mV to 1 V(ms)	Yes (170 µA)	-Low power -Programmable unity gain -Power down -Mute function summing capability (DTMF) -600 Ω Drive Capability	Battery Powered Systems "Commercial Quality"

Note

1. SA5752/5753 are also Excellent Audio Processor Components fro High Performance Cordless and Cellular Applications that include the Companding Function.
   ICC varies with VCC.
   Packages include: SA –40 to +80 °C; N: Plastic DIP; D: Plastic SO; F: Cer DIP; DK: SSOP (Shrink Small Outline Package).
   Applications include: Cordless Phones, Cellular Phones, Wireless Mics, Modems, Consumer Audio and Two-way Communications.

FIRST GENERATION NPN WIDEBAND TRANSISTORS (f_T up to 3.5 GHz)

f_T / I_C CURVE (see Fig.1)	PACKAGE					
	LEADED	SURFACE-MOUNT				
	SOT54	SOT23	SOT89	SOT143	SOT223	SOT323
(1)		BFT25				
(2)		BF747 BF547				BF547W
(3)	BF689K BF763	BFS17				BFS17W
(4)		BFS17A		BFG17A		
(5)		BFR53				
(6)			BFQ17		BFG16A	

SECOND GENERATION WIDEBAND TRANSISTORS (f_T up to 6 GHz)

f_T / I_C CURVE (see Fig.1)	POLARITY	PACKAGE					
		CERAMIC	SURFACE-MOUNT				
		SOT122	SOT23	SOT89	SOT143 (note 1)	SOT223	SOT323
(7)	NPN		BFR92(A)		BFG92A (/X)(/XR)		BFR92AW
	PNP		BFT92				BFT92W
(8)	NPN		BFR93(A)		BFG93A (/X)(/XR)	BFG94	BFR93AW
(9)	PNP		BFT93				BFT93W
(10)	NPN		BFR106	BFQ19		BFG97	
	PNP			BFQ149		BFG31	
(11)	NPN	BFQ34		BFQ18A		BFG35	
(12)	NPN	BFQ68					
(13)	NPN	BFQ136					

Note

1. SOT143 package is available with alternative pinning.
   European pinning - no type number suffix; USA pinning - suffix /X; Japanese pinning - suffix /XR.
   Brackets around the suffixes (/X) and (/XR) denote pinning options. No brackets means no options,
   (e.g. BFG10W/X: only available with USA pinning).

THIRD GENERATION NPN WIDEBAND TRANSISTORS (f_T up to 8 GHz)

f_T / I_C CURVE (see Fig.1)	PACKAGE				
	CERAMIC	SURFACE-MOUNT			
	SOT172	SOT23	SOT143 (note 1)	SOT223	SOT323
(14)		BFQ67	BFG67 (/X)(/XR)		BFQ67W
(15)			BFG197 (/X)(/XR)	BFG198	
(16)	BFQ135			BFG135	
(17)	BFQ270				

Note

1. SOT143 package is available with alternative pinning.
   European pinning - no type number suffix; USA pinning - suffix /X; Japanese pinning - suffix /XR.
   Brackets around the suffixes (/X) and (/XR) denote pinning options. No brackets means no options,
   (e.g. BFG10W/X: only available with USA pinning).

FOURTH GENERATION NPN WIDEBAND TRANSISTORS (f_T up to 10 GHz)

f_T / I_C CURVE (see Fig.1)	PACKAGE							
	CERAMIC	SURFACE-MOUNT						
	SOT172	SOT23	SOT143 (note 1)	SOT223	SOT323	SOT343 (note 1)	SOT353	SOT363
(18)		BFT25A	BFG25A/X		BFS25A	BFG25AW (/X)(/XR)		
(19)		BFR505	BFG505 (/X)(/XR)		BFS505	BFG505W (/X)(/XR)	BFC505 BFE505	BFM505
(20)		BFR520	BFG520 (/X)(/XR)		BFS520	BFG520W (/X)(/XR)	BFC520 BFE520	BFM520
(21)		BFR540	BFG540 (/X)(/XR)	BFG541	BFS540	BFG540W (/X)(/XR)		
(22)			BFG590 (/X)(/XR)	BFG591		BFG590W (/X)(/XR)		
(23)	BFQ621		BFG10(/X)			BFG10W/X		
(24)			BFG11(/X)			BFG11W/X		

Note

1. SOT143 and SOT343 packages are available with alternative pinning.
   European pinning - no type number suffix; USA pinning - suffix /X; Japanese pinning - suffix /XR.
   Brackets around the suffixes (/X) and (/XR) denote pinning options. No brackets means no options,
   (e.g. BFG10W/X: only available with USA pinning).

FIFTH GENERATION NPN WIDEBAND TRANSISTORS (f_T up to 25 GHz)

f_T / I_C CURVE (see Fig.1)	PACKAGE
	SURFACE-MOUNT
	SOT343
(25)	BFG403W
(26)	BFG410W
(27)	BFG425W
(28)	BFG21W

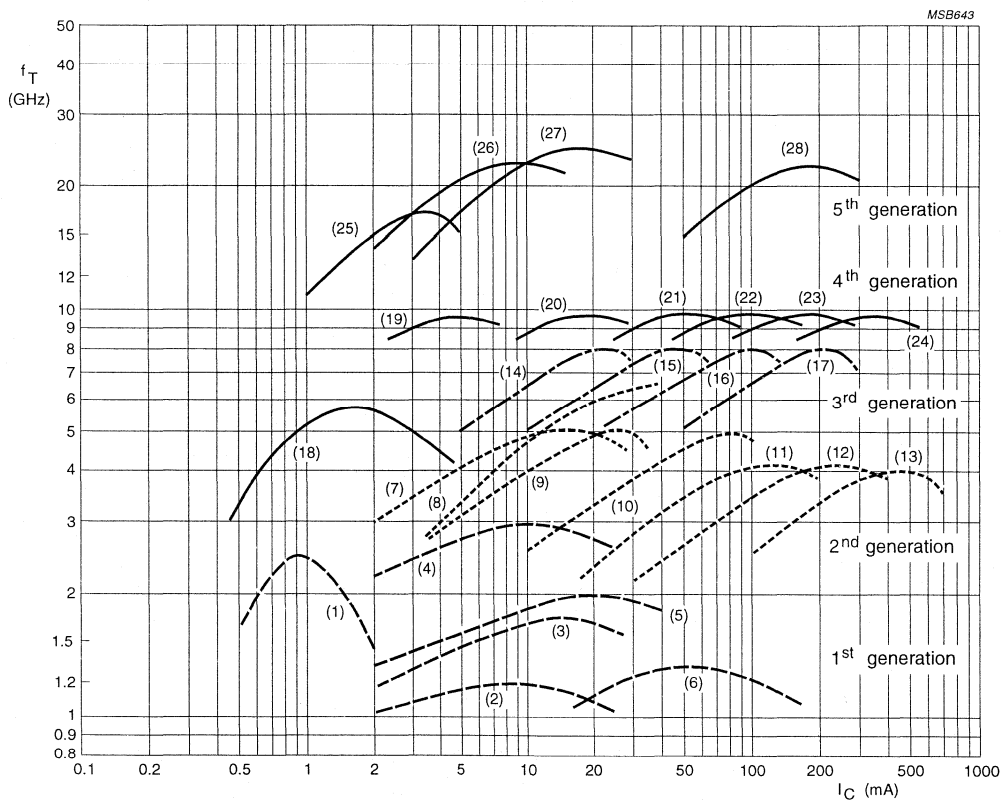


Fig.1 Transition frequency as a function of collector current for the five generations of RF bipolar wideband transistors.

PRODUCT DATA

TYPE NUMBER	f_T / I_C CURVE (see Fig.1)	POLARITY	PACKAGE	RATINGS		
				V_{CEO} (V)	I_C (mA)	P_{tot} (mW)
BF547	(2)	NPN	SOT23	20	50	300
BF547W	(2)	NPN	SOT323	20	50	300
BF689K	(3)	NPN	SOT54	15	25	360
BF747	(2)	NPN	SOT23	20	50	300
BF763	(3)	NPN	SOT54	25	25	360
BFC505	(19)	NPN	SOT353	8	18	500
BFC520	(20)	NPN	SOT353	8	70	1000
BFE505	(19)	NPN	SOT353	8	18	500
BFE520	(20)	NPN	SOT353	8	70	1000
BFG10(/X)	(23)	NPN	SOT143	8	250	250
BFG10W/X	(23)	NPN	SOT343	10	250	400
BFG11(/X)	(24)	NPN	SOT143	8	500	400
BFG11W/X	(24)	NPN	SOT343	8	500	760
BFG16A	(6)	NPN	SOT223	25	150	1000
BFG17A	(4)	NPN	SOT143	15	50	300
BFG25A/X	(18)	NPN	SOT143	5	6.5	32
BFG25AW(/X)(/XR)	(18)	NPN	SOT343	5	6.5	500
BFG31	(10)	PNP	SOT223	15	100	1000
BFG35	(11)	NPN	SOT223	18	150	1000
BFG67(/X)(/XR)	(14)	NPN	SOT143	10	50	380
BFG92A(/X)(/XR)	(7)	NPN	SOT143	15	25	400
BFG93A(/X)(/XR)	(8)	NPN	SOT143	12	35	300
BFG94	(8)	NPN	SOT223	12	60	700
BFG97	(10)	NPN	SOT223	15	100	1000
BFG135	(16)	NPN	SOT223	15	150	1000
BFG197(/X)(/XR)	(15)	NPN	SOT143	10	100	350
BFG198	(15)	NPN	SOT223	10	100	1000
BFG403W	(25)	NPN	SOT343	4.5	3.6	16
BFG410W	(26)	NPN	SOT343	4.5	12	54
BFG425W	(27)	NPN	SOT343	4.5	30	135
BFG505(/X)(/XR)	(19)	NPN	SOT143	15[1]	18	150
BFG505W(/X)(/XR)	(19)	NPN	SOT343	15[1]	18	500
BFG520(/X)(/XR)	(20)	NPN	SOT143	15[1]	70	300

Note

1. V_{CES}.

PRODUCT DATA

TYPE NUMBER	CHARACTERISTICS, typical values											
	f_T (GHz)	F (dB)	G_{UM} (dB)	@ f (MHz)	F (dB)	G_{UM} (dB)	@ f (MHz)	V_o[1] (mV)	P_L (dBm)	ITO (dBm)	@ I_C (mA)	& V_{CE} (V)
BF547	1.2		20	100								
BF547W	1.2		20	100								
BF689K	1.8	4		100	3	16[3]	200					
BF747	1.2		20	100								
BF763	1.8	5		800								
BFC505	7.3	1.8		900	3.5		2000					
BFC520	7	1.3		900								
BFE505	9	1.2		900	1.9		2000					
BFE520	9	1.1		900	1.9		2000					
BFG10(/X)			7[3]	1900								
BFG10W/X			10[2][3]	900		7[3]	1900					
BFG11(/X)			5[3]	1900								
BFG11W/X						6[2][3]	1900					
BFG16A	1.5		10	500								
BFG17A	2.8	2.5	15	800								
BFG25A/X	5	1.8	18	1000								
BFG25AW(/X)(/XR)	5	2	16	1000								
BFG31	5		16	500		12	800	550			70	10
BFG35	4		15	500		11	800	750			100	10
BFG67(/X)(/XR)	8	1.7	17	1000	2.5	10	2000					
BFG92A(/X)(/XR)	5	2	16	1000	3	11	2000					
BFG93A(/X)(/XR)	6	1.7	16	1000	2.3	10	2000					
BFG94	6	2.7		500	3	13.5	1000	500	21.5	34	45	10
BFG97	5.5	2	16	500		12	800	700			70	10
BFG135	7		16	500		12	800	850			100	10
BFG197(/X)(/XR)	7.5	2.3	16	1000		10	2000					
BFG198	8		18	500		15	800	700			70	8
BFG403W	17	1		900	1.6		2000			6	1	1
BFG410W	22	0.9		900	1.2		2000			15	10	2
BFG425W	25	0.8		900	1.2		2000			22	25	2
BFG505(/X)(/XR)	9	1.6	20	900	1.9	13	2000		4	10	5	6
BFG505W(/X)(/XR)	9	1.6	19	900	1.9	12	2000		4	10	5	6
BFG520(/X)(/XR)	9	1.6	19	900	1.9	13	2000	275	17	26	20	6

Notes

1. At $d_{im} = -60$ dB, measured according to DIN45004B, par. 6.3: 3-tone test.
2. Minimum value.
3. Power gain G_p.

PRODUCT DATA

TYPE NUMBER	f_T / I_C CURVE (see Fig.1)	POLARITY	PACKAGE	RATINGS		
				V_{CEO} (V)	I_C (mA)	P_{tot} (mW)
BFG520W(/X)(/XR)	(20)	NPN	SOT343	15[1]	70	500
BFG540(/X)(/XR)	(21)	NPN	SOT143	15[1]	120	500
BFG540W(/X)(/XR)	(21)	NPN	SOT343	15[1]	120	500
BFG541	(21)	NPN	SOT223	15[1]	120	650
BFG590(/X)(/XR)	(22)	NPN	SOT143	15	200	400
BFG590W(/X)(/XR)	(22)	NPN	SOT343	15	200	500
BFG591	(22)	NPN	SOT223	15	200	2000
BFM505	(19)	NPN	SOT363	8	18	500
BFM520	(20)	NPN	SOT363	8	70	1000

Note

1. V_{CES}.

PRODUCT DATA

TYPE NUMBER	CHARACTERISTICS, typical values											
	f_T (GHz)	F (dB)	G_{UM} (dB)	@ f (MHz)	F (dB)	G_{UM} (dB)	@ f (MHz)	V_o[1] (mV)	P_L (dBm)	ITO (dBm)	@ I_C (mA)	& V_{CE} (V)
BFG520W(/X)(/XR)	9	1.6	17	900	1.85	11	2000	275	17	26	20	6
BFG540(/X)(/XR)	9	1.9	18	900	2.1	11	2000	500	21	34	40	8
BFG540W(/X)(/XR)	9	1.9	16	900	2.1	10	2000	500	21	34	40	8
BFG541	9	1.9	15	900	2.1	9	2000	500	21	34	40	8
BFG590(/X)(/XR)	5		13	900		7.5	2000					
BFG590W(/X)(/XR)	5		13	900		7.5	2000		21		80	5
BFG591	7		13	900		7.5	2000					
BFM505	9	1.4	17	900	1.9	10	2000					
BFM520	9	1.7	15	900	1.9	9	2000					

Note

1. At $d_{im} = -60$ dB, measured according to DIN45004B, par. 6.3: 3-tone test.

PRODUCT DATA

TYPE NUMBER	f_T / I_C CURVE (see Fig.1)	POLARITY	PACKAGE	RATINGS		
				V_{CEO} (V)	I_C (mA)	P_{tot} (mW)
BFQ17	(6)	NPN	SOT89	25	150	1000
BFQ18A	(11)	NPN	SOT89	18	150	1000
BFQ19	(10)	NPN	SOT89	15	100	1000
BFQ34	(11)	NPN	SOT122	18	150	2700
BFQ67	(14)	NPN	SOT23	10	50	300
BFQ67W	(14)	NPN	SOT323	10	50	300
BFQ68	(12)	NPN	SOT122	18	300	4500
BFQ135	(16)	NPN	SOT172	19	150	2700
BFQ136	(13)	NPN	SOT122	18	600	9000
BFQ149	(10)	PNP	SOT89	15	100	1000
BFQ270	(17)	NPN	SOT172	19	500	10000
BFQ540	(21)	NPN	SOT89	12	120	1200
BFQ621	(23)	NPN	SOT172	16	150	800
BFR53	(5)	NPN	SOT23	10	50	250
BFR92	(7)	NPN	SOT23	15	25	300
BFR92A	(7)	NPN	SOT23	15	25	300
BFR92AW	(7)	NPN	SOT323	15	25	300
BFR93	(8)	NPN	SOT23	12	35	300
BFR93A	(8)	NPN	SOT23	12	35	300
BFR93AW	(8)	NPN	SOT323	12	35	300
BFR94A	(8)	NPN	SOT122	25	150	3500
BFR106	(10)	NPN	SOT23	15	100	500
BFR505	(19)	NPN	SOT23	15[1]	18	150
BFR520	(20)	NPN	SOT23	15[1]	70	300
BFR540	(21)	NPN	SOT23	15[1]	120	480
BFS17	(3)	NPN	SOT23	15	25	300
BFS17A	(4)	NPN	SOT23	15	25	300
BFS17W	(3)	NPN	SOT323	15	50	300
BFS25A	(18)	NPN	SOT323	5	6.5	32
BFS505	(19)	NPN	SOT323	15[1]	18	150
BFS520	(20)	NPN	SOT323	15[1]	70	300
BFS540	(21)	NPN	SOT323	15[1]	120	500
BFT25	(1)	NPN	SOT23	5	6.5	30
BFT25A	(18)	NPN	SOT23	5	6.5	32
BFT92	(7)	PNP	SOT23	15	25	300
BFT92W	(7)	PNP	SOT323	15	35	300
BFT93	(9)	PNP	SOT23	12	35	300

Note

1. V_{CES}.

PRODUCT DATA

TYPE NUMBER	CHARACTERISTICS, typical values											
	f_T (GHz)	F (dB)	G_{UM} (dB)	@ f (MHz)	F (dB)	G_{UM} (dB)	@ f (MHz)	V_o[1] (mV)	P_L (dBm)	ITO (dBm)	@ I_C (mA)	& V_{CE} (V)
BFQ17	1.5		16	200		6.5	800					
BFQ18A	4											
BFQ19	5.5	3.3	11.5	500		7.5	800					
BFQ34	4	8	16.3	500				1200	26	45	120	15
BFQ67	8	1.7	14	1000	2.7	8	2000					
BFQ67W	8	2	13	1000	2.7	8	2000					
BFQ68	4		13	800				1600	28	47	240	15
BFQ135	6.5		17	500		13.5	800	1200			120	18
BFQ136	4		12.5	800				2500			500	15
BFQ149	5	3.75	12	500								
BFQ270	6		16	500		10	1000	1600			240	18
BFQ540	9	1.9		900				500			40	8
BFQ621	7		18.5	500				1200			120	18
BFR53	2	5[2]		500		10.5	800					
BFR92	5	2.4	18	500				150			14	10
BFR92A	5	2.1	14	1000	3	8	2000	150			14	10
BFR92AW	5	2	14	1000	3	8	2000					
BFR93	5	1.9	16.5	500								
BFR93A	6	1.9	13	1000	3	7	2000	425			30	8
BFR93AW	5	1.5	13	1000	2.1	8	2000					
BFR94A	3.5	8		200	5	13.5	500					
BFR106	5	3.5	11.5	800				350			50	9
BFR505	9	1.6	17	900	1.9	10	2000		4	10	5	6
BFR520	9	1.6	15	900	1.9	9	2000		17	26	20	6
BFR540	9	1.9	14	900	2.1	7	2000	550	21	34	40	8
BFS17	1	4.5		500								
BFS17A	2.8	2.5	13.5	800				150			14	10
BFS17W	1.6	4.5		500								
BFS25A	5	1.8	13	1000								
BFS505	9	1.6	17	900	1.9	10	2000		4	10	5	6
BFS520	9	1.6	15	900	1.9	9	2000		17	26	20	6
BFS540	9	1.9	14	900	2.1	8	2000		21	34	40	8
BFT25	2.3	3.8	18	500		12	800					
BFT25A	5	1.8	15	1000								
BFT92	5	2.5	18	500				150			14	10
BFT92W	5	2.5	17	500	3	11	1000					
BFT93	5	2.4	16.5	500				300			30	5

Notes

1. At d_{im} = −60 dB, measured according to DIN45004B, par. 6.3: 3-tone test.
2. Maximum value.

PRODUCT DATA

TYPE NUMBER	f_T / I_C CURVE (see Fig.1)	POLARITY	PACKAGE	RATINGS		
				V_{CEO} (V)	I_C (mA)	P_{tot} (mW)
BFT93W	(9)	PNP	SOT323	12	50	300
MPSH10		NPN	SOT54	25	40	1000
PMBT3640		PNP	SOT23	12	80	350
PMBTH10		NPN	SOT23	25	40	400
PMBTH81		PNP	SOT23	20	40	400

DEVELOPMENT TYPES

TYPE NUMBER	f_T / I_C CURVE (see Fig.1)	POLARITY	PACKAGE	RATINGS		
				V_{CEO} (V)	I_C (mA)	P_{tot} (mW)
BFG21W	(28)	NPN	SOT343	4.5	200[1]	600

Note

1. Typical value.

PRODUCT DATA

TYPE NUMBER	CHARACTERISTICS, typical values											
	f_T (GHz)	F (dB)	G_{UM} (dB)	@ f (MHz)	F (dB)	G_{UM} (dB)	@ f (MHz)	V_o[1] (mV)	P_L (dBm)	ITO (dBm)	@ I_C (mA)	& V_{CE} (V)
BFT93W	5	2.4	15.5	500	3	10	1000					
MPSH10	0.65[2]											
PMBT3640	0.5[2]											
PMBTH10	0.65[2]											
PMBTH81	0.6[2]											

Notes

1. At d_{im} = –60 dB, measured according to DIN45004B, par. 6.3: 3-tone test.
2. Minimum value.

DEVELOPMENT TYPES

TYPE NUMBER	CHARACTERISTICS, typical values											
	f_T (GHz)	F (dB)	G_{UM} (dB)	@ f (MHz)	F (dB)	G_{UM} (dB)	@ f (MHz)	V_o[1] (mV)	P_L (dBm)	ITO (dBm)	@ I_C (mA)	& V_{CE} (V)
BFG21W	18[2]		10[2][3]	1900								

Notes

1. At d_{im} = –60 dB, measured according to DIN45004B, par. 6.3: 3-tone test.
2. Minimum value.
3. Power gain G_p.

LINE-UPS

Analog cellular (AMPS, (E)TACS, NMT) 900 MHz

INPUT POWER (mW)	1st STAGE	2nd STAGE	3rd STAGE	P_L (W)	SUPPLY VOLTAGE (V)
Bipolar					
1	BFG540/X	BLT80	BLT81	1.2	6
1	BFG540/X	BLT70	BLT71	1.2	4.8
1	BFG10W/X	BLT71/8	–	1.2	4.8

Digital cellular (GSM) 900 MHz

INPUT POWER (mW)	1st STAGE	2nd STAGE	3rd STAGE	P_L (W)	SUPPLY VOLTAGE (V)
Bipolar					
1	BFG540W/X	BFG10W/X	BLT82	3.5 pulsed	6

Portable transmitters (860 MHz to 960 MHz)

INPUT POWER (mW)	1st STAGE	2nd STAGE	3rd STAGE	P_L (W)	SUPPLY VOLTAGE (V)
Bipolar					
1	BFG540	BLT80	BLT81	1.2	6
15	BFG93A	BLT80	BLT92/SL	3	7.5

RF wideband transmitters for pager front-end (see Fig.2)

FUNCTION	TYPE NUMBER	REMARKS
RF amplifier	BFC505	higher gain, lower noise, high isolation (0.3 mA)
	BFG403W	high performance, low voltage, low current
	BFR505	higher gain, lower noise (1 mA)
	BFT25A	lowest current (0.2 mA)
Oscillator, mixer or buffer	BFQ67	choice of the transistor is determined by the available current and the required performance
	BFR92A	
	BFR505	
	BFT25A	

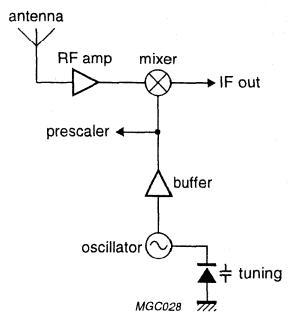


Fig.2 Typical front-end section for pagers.

RF wideband transistors for the receiver section in cordless/cellular phones (see Fig.3)

FUNCTION	TYPE NUMBER	SYSTEM FREQUENCY (MHz)	FEATURES
LNA	BFC505	1900	high isolation gain, low noise current
	BFG410W	900; 1900; 2500	very low noise
	BFG425W	900; 1900; 2500	very low noise
	BFR505	900; 1900	good performance at low current (1 mA)
	BFR520	900; 1900	higher gain, lower noise (10 mA)
Mixer	BFE505	900; 1900	balanced mixer in a single SOT353 package
	BFG505	900; 1900	good performance, low current
	BFG410W	900; 1900; 2500	low noise, high isolation
	BFG520	900; 1900	higher power to IF (10 mA)
	BFR93A	900	low cost, acceptable performance
Buffer and VCO	BFG410W	900; 1900; 2500	excellent isolation
	BFG505	1900	buffer and VCO in a single SOT353 package
	BFQ67	900	third generation, good performance
	BFR92A	900	excellent VCO, good buffer, low-cost
	BFR93A	900	excellent VCO, good buffer, low-cost
	BFR505	900; 1900	good VCO, high-gain buffer, low current
	BFR520	900; 1900	good VCO, higher output power
IF	BFS17A	40 to 100	any first or second generation transistor

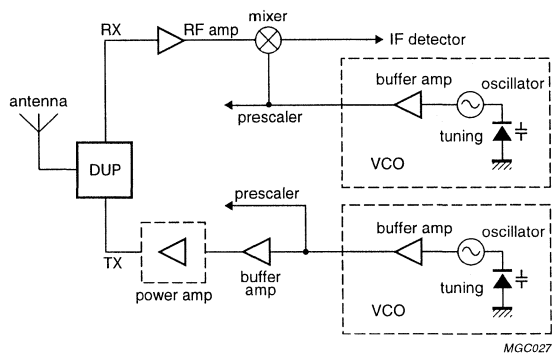


Fig.3 Typical RF section for cordless and cellular phones.

RF wideband transistors for the receiver section in cordless/cellular phones (see Fig.3)

FUNCTION	SYSTEM FREQUENCY (MHz)	SOT23	SOT323	SOT143 (1)	SOT343 (1)	SOT353	SOT363
LNA	900; 1900	BFR505	BFS505	BFG505	BFG505W	BFC505	BFM505
	900; 1900	BFR 520	BFS520	BFG520	BFG520W	BFC520	BFM520
Mixer	900	BFR93A	BFR93AW	BFG93A			
	900; 1900	BFR505	BFS505	BFG505	BFG505W	BFE505	BFM505
	900; 1900	BFR520	BFS520	BFG520	BFG520W	BFE520	BFM520
Buffer and VCO	900	BFR92A	BFR92AW	BFG92A			
	900	BFR93A	BFR93AW	BFG93A			
	900	BFQ67	BFQ67W	BFG67			
	900; 1900	BFR505	BFS505	BFG505	BFG505W	BFC505	BFM505
	900; 1900	BFR520	BFS520	BFG520	BFG520W	BFC520	BFM520
IF	40 to 100	BF547	BF547W				
		BFS17	BFS17W	BFG17A			
		BFR92A	BFR92AW	BFG92A			

Note

1. Also available in /X and /XR versions.

RF wideband transistors for the power amplifier section in cordless/cellular phones (see Fig.4)

SYSTEM	SUPPLY VOLTAGE (V)	P_{out} (mW)	SOT143	SOT343
CT1, CT1+, CT2, CT2+, CT3	3.3	driver for PA2	BFG67	
			BFG505	BFG505W
			BFG520	BFG520W
		15	BFG67	
		20	BFG520	BFG520W
		40	BFG540	BFG540W
DECT, PHP	3.3	400	BFG540/X	BFG540W/X
			BFG10/X	BFG10W/X
			BFG11/X	BFG11W/X

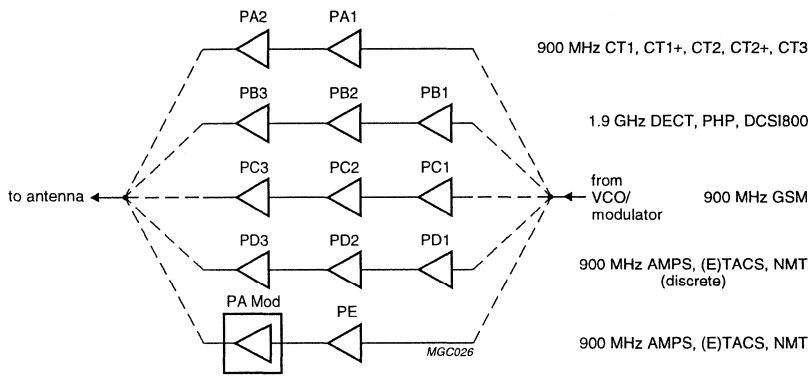


Fig.4 Typical power amplifier section for cordless and cellular phones.

MOSFETs for power/battery management and DC-DC convertor

Selection guide

MOSFETS FOR POWER/BATTERY MGT AND DC-DC CONVERTOR SELECTOR GUIDE

TYPE	DESCRIPTION	PACKAGE	V_{DS} (V)	RDS (ON)	@ V_{GS} (V)	P_{max} (W)
BSH103	N-channel enhancement mode MOS transistor	SOT23	30	520mΩ	2.5	0.5
BSH104	N-channel enhancement mode MOS transistor	SOT23	12	270mΩ	2.5	0.5
BSH105	N-channel enhancement mode MOS transistor	SOT23	12	180mΩ	2.5	0.5
BSH106	N-channel enhancement mode MOS transistor	SOT363	12	180mΩ	2.5	0.7
BSH107	N-channel enhancement mode MOS transistor	TSOP-6	12	70mΩ	2.5	0.8
BSH203	P-channel enhancement mode MOS transistor	SOT23	30	1300mΩ	2.5	0.5
BSH204	P-channel enhancement mode MOS transistor	SOT23	12	680mΩ	2.5	0.5
BSH205	P-channel enhancement mode MOS transistor	SOT23	12	450mΩ	2.5	0.5
BSH206	P-channel enhancement mode MOS transistor	SOT363	12	450mΩ	2.5	0.7
BSH207	P-channel enhancement mode MOS transistor	TSOP-6	12	180mΩ	2.5	0.8
BSN20W	N-channel enhancement mode vertical DMOS transistor	SOT323	50	15 Ω	10	0.2
BSP030	N-channel enhancement mode vertical DMOS transistor	SOT223	30	30mΩ	10	2
BSP090	P-channel enhancement mode vertical DMOS transistor	SOT223	30	90mΩ	10	2
BSP130	N-channel enhancement mode MOS transistor	SOT223	300	8 Ω	10	2
BSP255	P-channel enhancement mode MOS transistor	SOT223	300	17 Ω	10	2
PHC20512	Complementary enhancement mode MOS transistors	SO8	30	50+125 mΩ	10	2
PHC21025	Complementary enhancement mode MOS transistors	SO8	30	100+250 mΩ	10	2
PHC2300	Complementary enhancement mode MOS transistors	SO8	300	8+17 W	10	2
PHN1013	N-channel enhancement mode MOS transistor	SO8	30	13mΩ	10	2
PHN205	Dual N-channel enhancement mode MOS transistors	SO8	30	50+50m Ω	10	2
PHN210	Dual N-channel enhancement mode MOS transistors	SO8	30	100+100 mΩ	10	2
PHP212	Dual P-channel enhancement mode MOS transistors	SO8	30	125+125 mΩ	10	2
PHP212L	Dual P-channel enhancement mode MOS transistors	SO8	30	125+125 mΩ	4.5	2
PHP225	Dual P-channel enhancement mode MOS transistors	SO8	30	250+250 mΩ	10	2

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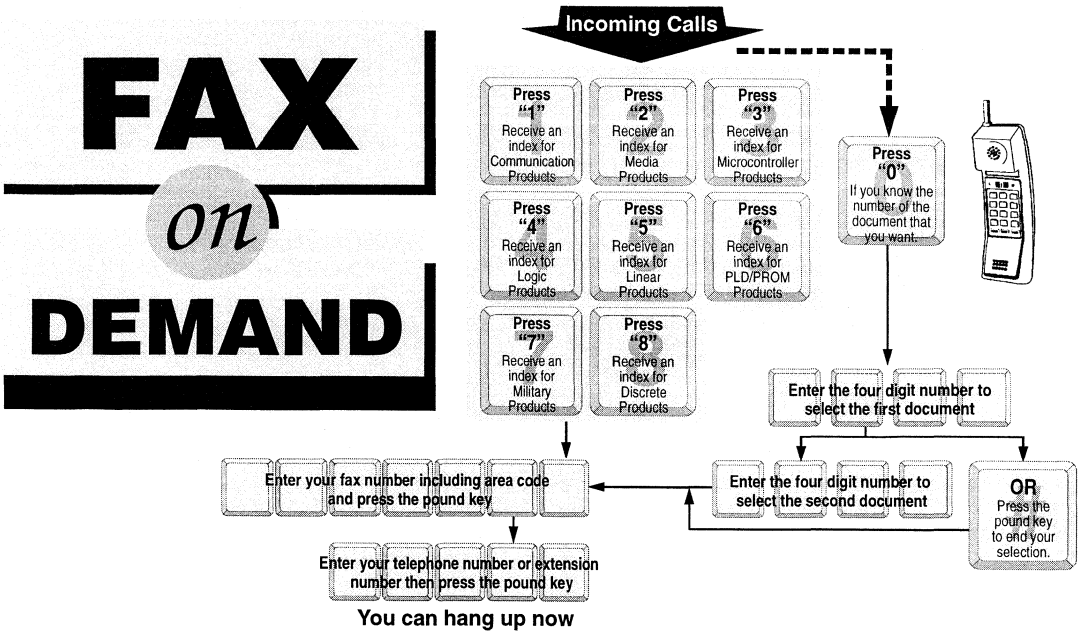

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GSM (GLOBAL SYSTEM FOR MOBILE COMMUNICATIONS) DIGITAL CELLULAR ICs

In 1992 Philips produced the first single-chip baseband signal processor for GSM. Today our low voltage GSM ICs cover all functions–from antenna to microphone.

GSM digital cellular ICs

Three highly integrated ICs are available for the RF section: the SA1620 RF transceiver, the SA1638 IF transceiver and the UMA1021M RF synthesizer. The ICs support high IF frequencies to allow simple, low-cost filters to be used for image-rejection.

The BGY204 Power Amplifier Module provides an off-the-shelf solution for 2-Watt GSM transmitters. CGY2011G is an alternative MMIC solution.

The PCF5077 Power Amplifier Controller ensures that PA on/off and output characteristics meet GSM/DCS1800 requirements, Phase II.

The baseband and audio interface is now a single-chip interface between the RF transceiver, the microphone and ear piece and the baseband processor. It integrates an audio Codec and auxiliary AD/DA converter for AGC, AFC and power management.

The baseband DSP includes the TDMA timer. An on-chip ROM contains firmware program modules to perform all necessary processing algorithms. Special attention has now been given to equalization in order to improve performance in hilly areas and fast-moving vehicles.

Philips Semiconductors' GSM ICs include:

SA1620 - Low voltage GSM RF transceiver

SA1638 - Low voltage GSM IF transceiver

UMA1021M - Low voltage frequency synthesizer for radio telephones

BGY204 - Power amplifier module

CGY2013G - MMIC power amplifier

UBA1710 - Modulator for GaAs PAs

PCF5077 - Power amplifier controller for GSM systems

TDA8002/TDA8005 - SIM interface

P90CL301 - Low voltage microcontroller

PCF507X - GSM baseband interface

PCF5083 - GSM baseband processor

TEA1095 - Handsfree IC

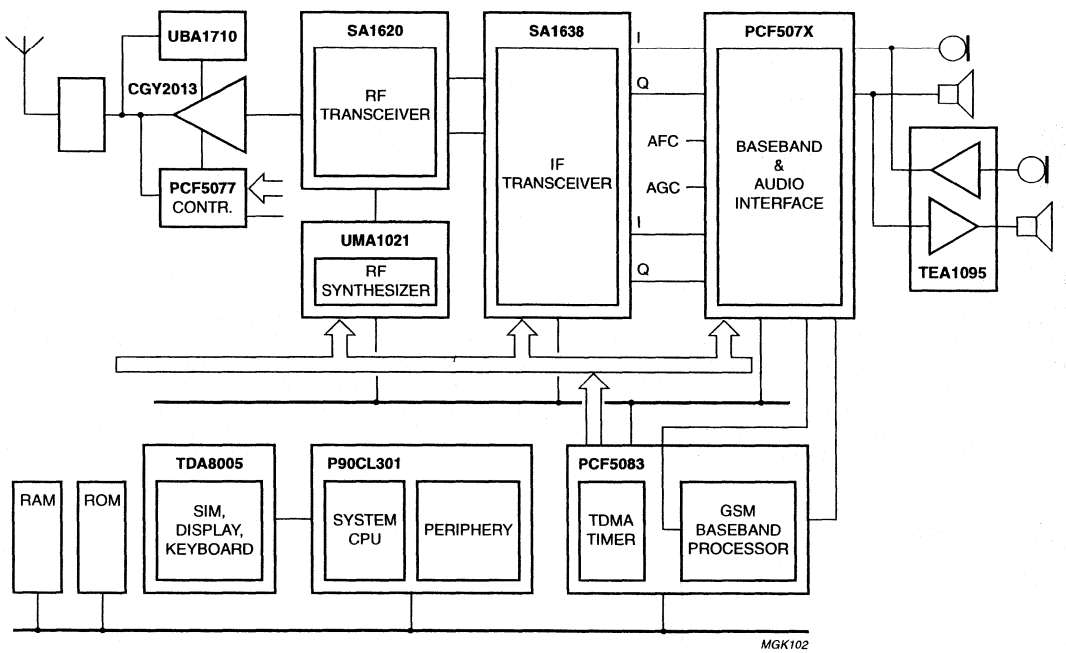


Fig.1 GSM digital cellular ICs.

American Digital Cellular RF transceiver chip–sets (TDMA)

North American Digital Cellular (NADC) IS-54/-136 PCS TDMA RF Transceiver Chipsets

1st generation TDMA RF transceiver chip–set (Single–band 800MHz, Dual–mode AMPS/DAMPS)
The chip–set combines all of the necessary RF and IF functions into **four integrated devices**: the SA621 RF front end, the SA7025 dual frequency synthesizer, the SA900 I/Q transmit modulator and the SA637 digital IF receiver or SA606 FM IF receiver + external I/Q demodulator. These devices were designed as a system and therefore have interface levels which are matched, eliminating the need for additional buffers and interface devices. There is also a common high speed serial interface bus, making addressing the devices simpler. Additionally the frequency plan was designed to eliminate the need for an additional synthesizer and VCO loop. All of these features dramatically reduces the cost and size while improving the performance of the overall system.

Although this is our first IS–54/–136 solution, our 4–chip configuration is one of the most integrated and easy to use chip–set available. For example, the SA900 provides I/Q modulators, the phase shifter, the VGA, a filter, control logic, clock distribution and more in a single IC. The need for two RF synthesizers was eliminated by closely coupling the SA7025 and the SA900 so it is possible to use the main synthesizer to simultaneously generate receive and transmit signals. The integration and connectivity of the chip–set promote significant cost reduction. In addition this integrated solution reduces the time to a final product by simplifying the design effort.

Philips 1st generation TDMA RF transceiver chipset consists of the following ICs:

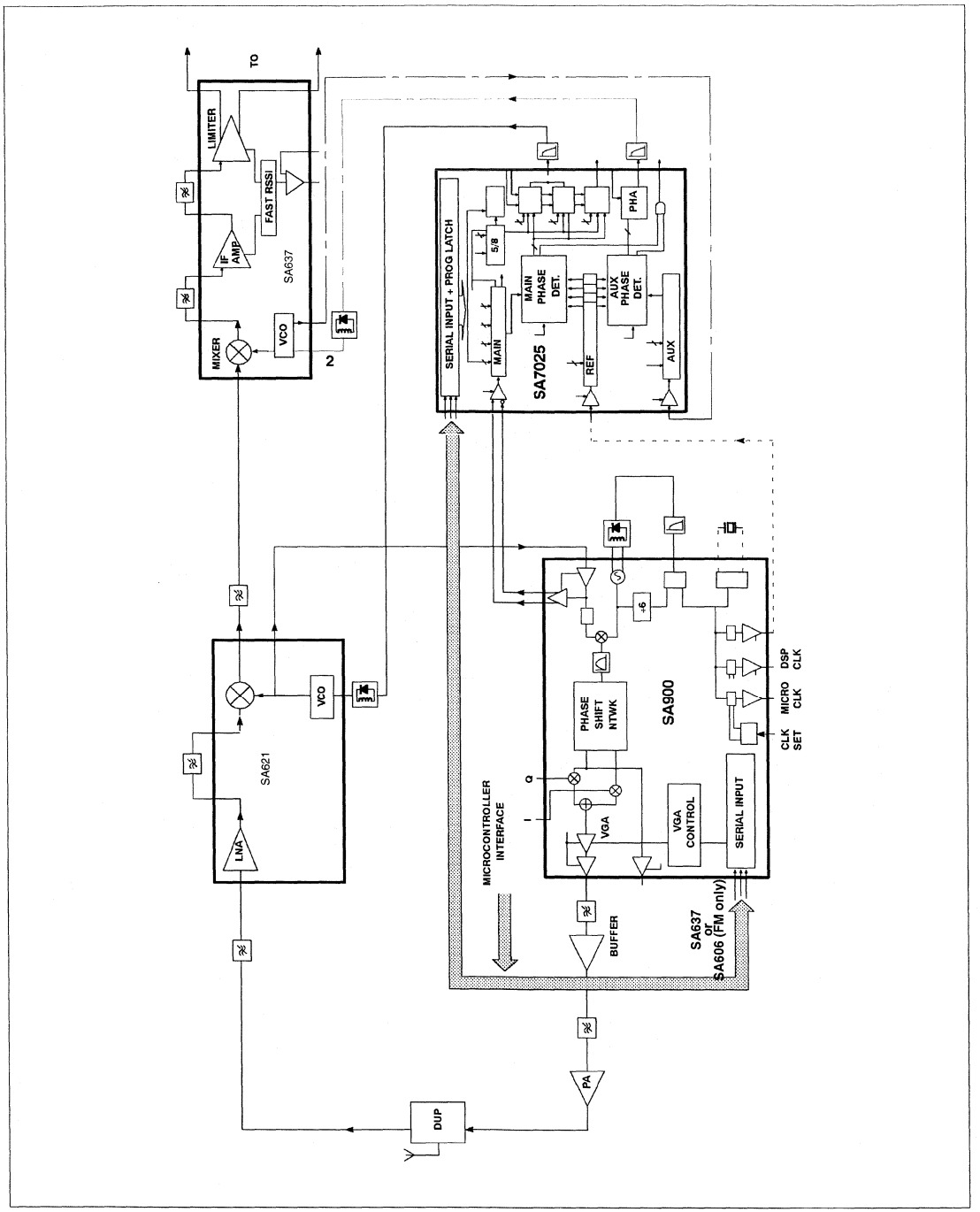
SA621	1GHz low voltage LNA, mixer and VCO
SA606	Low voltage high performance mixer FM/IF system
SA637	Low-voltage digital IF receiver
SA7025	Low-voltage 1GHz fractional-N synthesizer
SA900	I/Q transmit modulator

2nd generation TDMA RF transceiver chip–set (Dual–band 800/1900MHz, Triple–mode AMPS/DAMPS/PCS)
This chip–set combines all the necessary RF and IF functions into **three integrated devices**: the SA1920 RF dual–band front end, the SA647 Low power digital IF system receiver and the SA9025 I/Q transmit modulator with integrated dual fractional–N frequency synthesizer. This is the most highly integrated dual–band, triple–mode PCS chip–set available on the market. These devices were designed as a system and therefore have interface levels which are matched, eliminating the need for additional buffers and interface devices. Additionally the frequency plan was designed to eliminate the need for any additional synthesizer and VCO loop. The result is a smaller, cost effective, low–power phone that is ultimately more attractive to the end users.

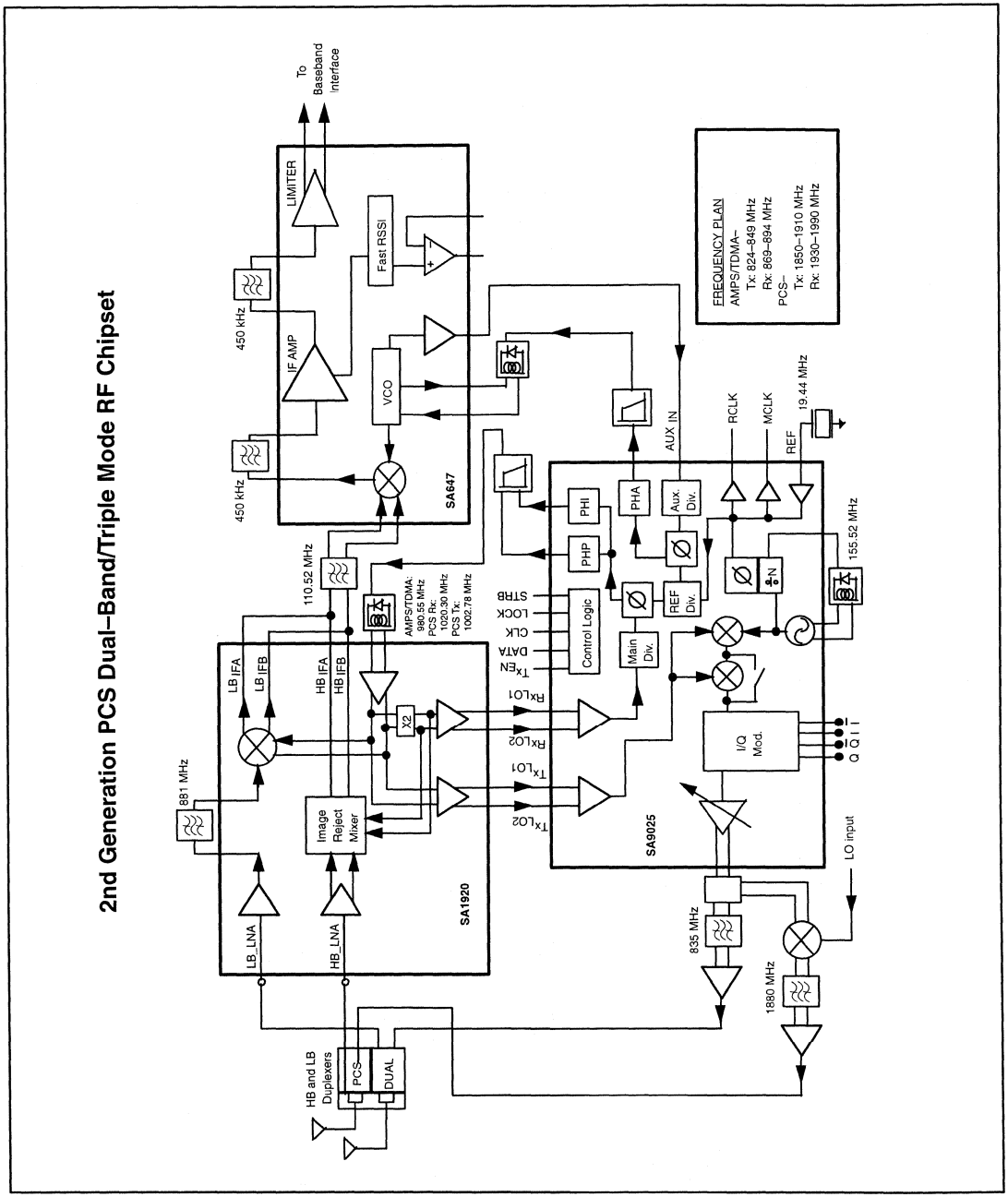
Philips 2nd generation TDMA (PCS) RF transceiver chipset consists of the following ICs:

SA1920	Dual–band 800/1900MHz RF Front–End
SA647	Low–Power FM IF System
SA9025	Transmit Modulator with integrated Dual Fractional–N synthesizer

1st generation TDMA RF transceiver chip–set (AMPS/DAMPS)



2nd generation TDMA RF transceiver chip–set (AMPS/DAMP/PCS)



DECT (DIGITAL ENHANCED CORDLESS TELECOMMUNICATIONS)

Set to become a world standard for cordless, DECT has been renamed to abbreviate "Digital Enhanced Cordless Telecommunications". Philips Semiconductors offers very competitive complete DECT solutions including hardware, software and support for applications ranging from residential to 2-line business systems. Both off-the-shelf and customized solutions are available.

Residential and 2-line business systems

- The RF transceiver incorporates a double superheterodyne receiver that is composed of the UMA1022M 2 GHz dual frequency synthesizer, SA639 FM IF and UAA2067 front end.
- The PCD509x (ABC) family is a range of versatile low-power GAP-compliant single chip baseband processor ICs designed to allow flexibility in the design of residential and small PBX systems and data applications and enables a high degree of customization of the MMI e.g. speaker phone and conference calling.
- The PCD5096 (Universal Codec) integrates two audio codecs, a DSP (performs echo cancellation, conference call, DTMF, dial tone generation) and two PSTN interfaces onto one chip. Together with the ABC family the universal codec meets all the requirements to create two-line PSTN low-cost digital cordless systems and add functionality to high-end corded phones. In addition, the IOM-2 interface can provide analog extensions for ISDN.
- Philips Semiconductors also provides GAP-compatible and approved DECT software tested in compliance with TBR22; both standard catalogue and customized MMIs.

Philips Semiconductors' DECT ICs include:

UAA2067G - Low voltage RF transceiver–2 GHz

SA639 - Low voltage mixer FM IF system with filter amplifier and data switch

UMA1022M - Low voltage frequency synthesizer for radio telephones

CGY2030/CGY2032 - Low voltage MMIC power amplifiers

PCD5091/2/3/4/5 - DECT baseband processor–ADPCM, burst-mode controller and microcontroller

PCD5096 - Universal CODEC

PCA1070/TEA1118A - Line Interface (Basestation)

PCD3316 - Caller ID/Call Waiting (CIDCW)

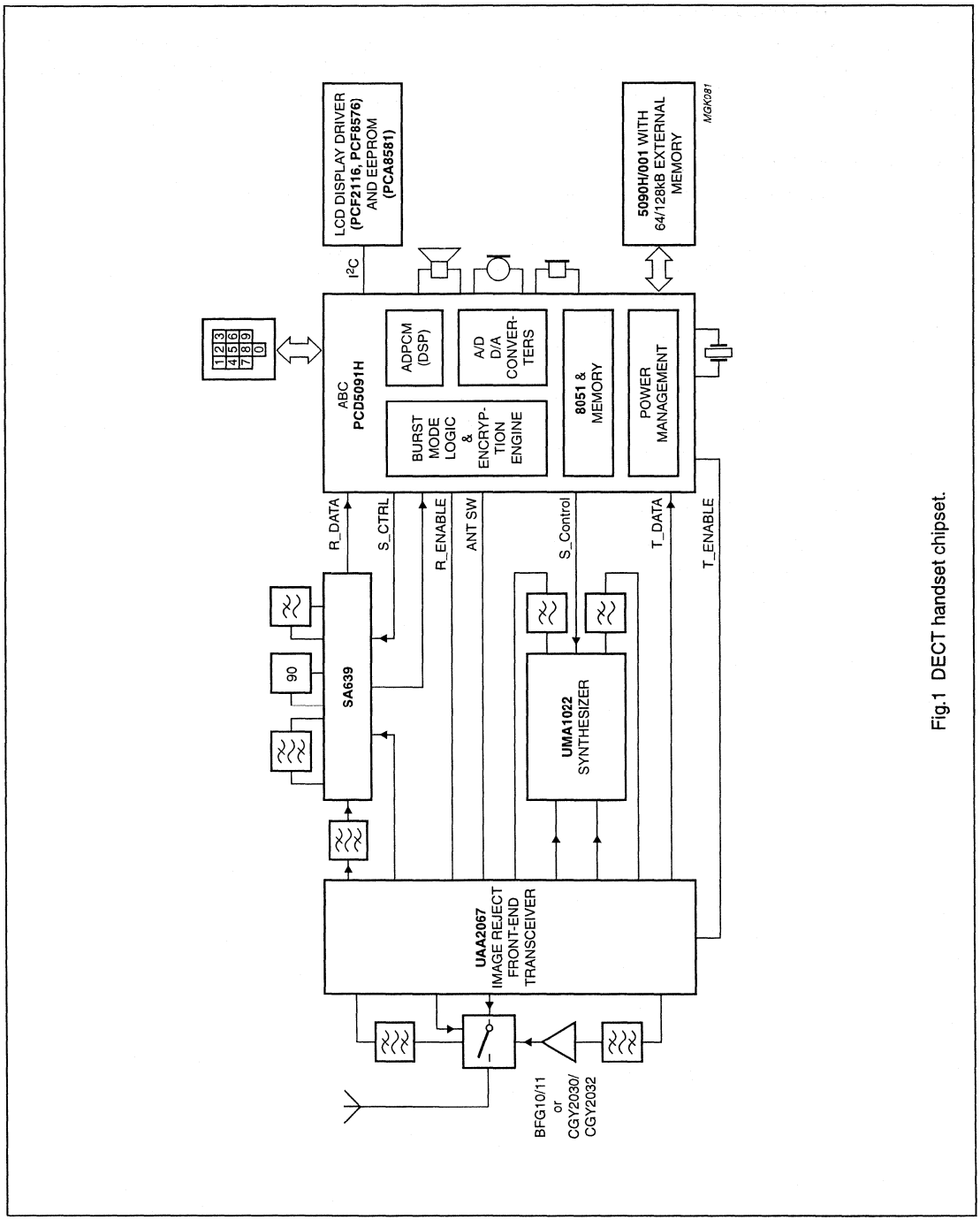


Fig.1 DECT handset chipset.

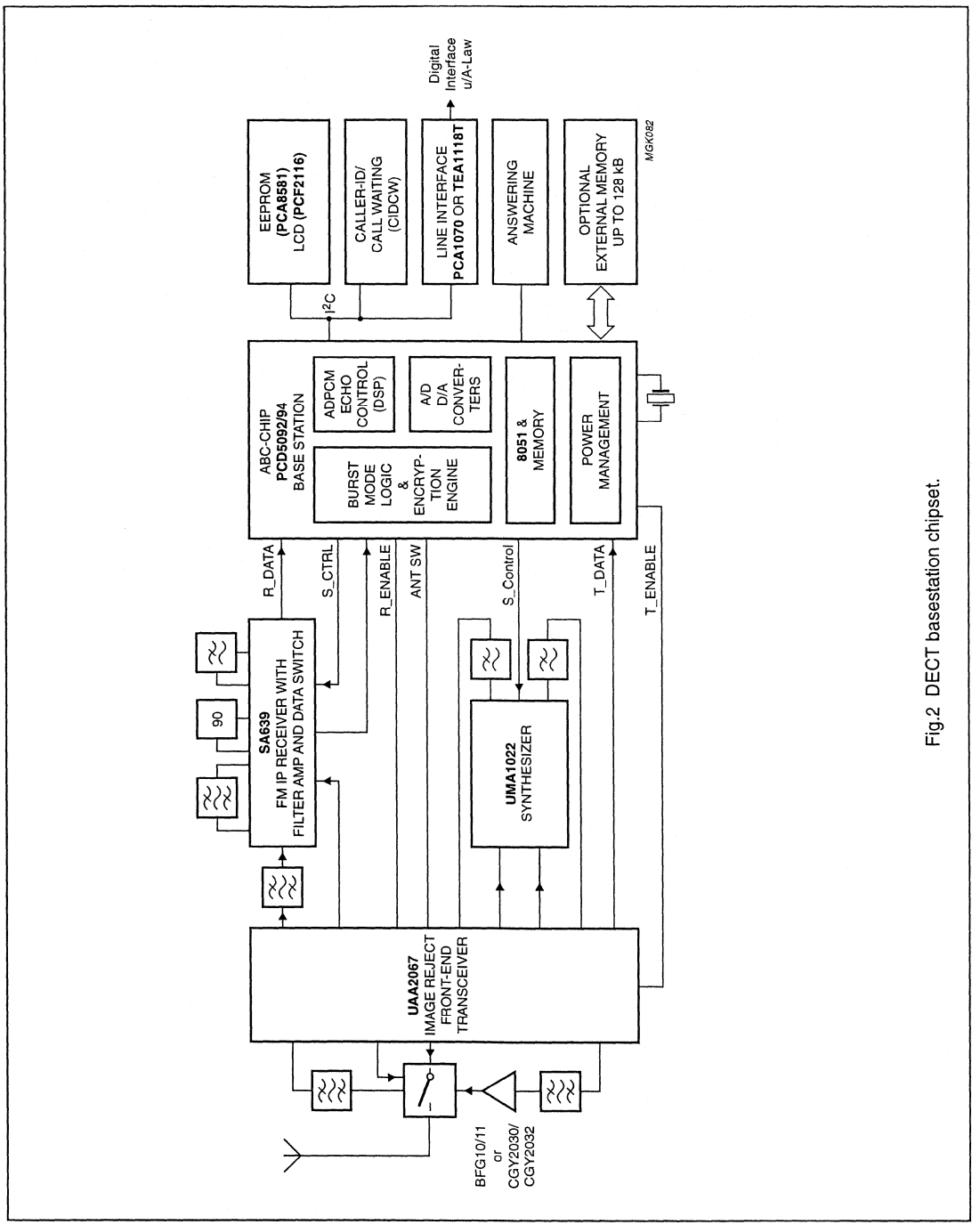


Fig.2 DECT basestation chipset.

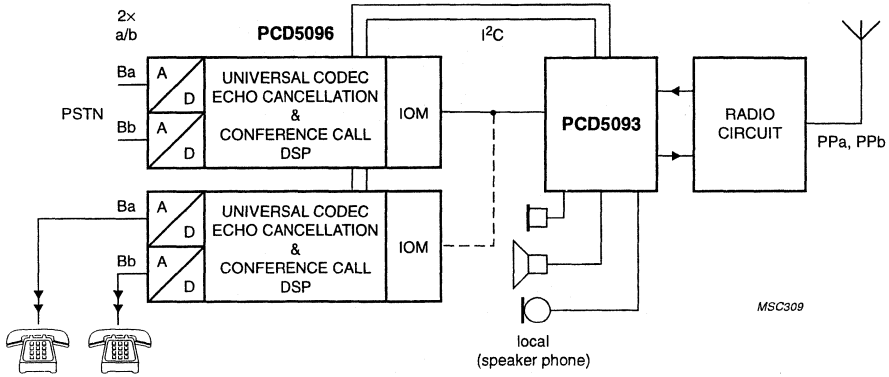


Fig.3 A typical DECT small business system with the PCD5096 universal codec, the single-chip baseband processor (ABC chip) and an RF interface.

AMPS/(E)TACS/CDPD Analog Cellular

Analog Cellular Chipset
AMPS (Advanced Mobile Phone Service)
TACS (Total Access Communication System)
CDPD (Cellular Digital Packet Data)

AMPS/ETACS

The analog cellular market is a consumer market with heavy price pressures on handsets and components. Analog cellular is still the worlds largest cellular system. Development in analog cellular handsets still continues at a faster pace, offering more features, lowering prices and more models.

Manufacturers of handsets face shorter product life cycles, faster Time–to–Market (TtM) and rapidly decreasing market prices. With Philips' long–time experience in analog cellular, our chipset presents a proven solution.

New ICs in the chipset are developed in order to meet market demand for lower cost and faster TtM.

Current AMPS/ETACS

Our chipset uses proven 3V technology to improve power–consumption of a hand–held phone, thus improving talk–time and standby–time.

The chipset is supported by a software package (source–code), consisting of protocol stack and examples for Man–Machine–Interface (MMI) and device drivers.

RF Transceiver

The transceiver section consists of 4 low–voltage, low–power ICs: For the Front–End, either the SA611 or SA621 can be used. Both have high–performance LNA and mixer on–chip. In addition, the SA621 contains an oscillator. With only an external resonator circuit, the SA621 can be configured as a VCO.

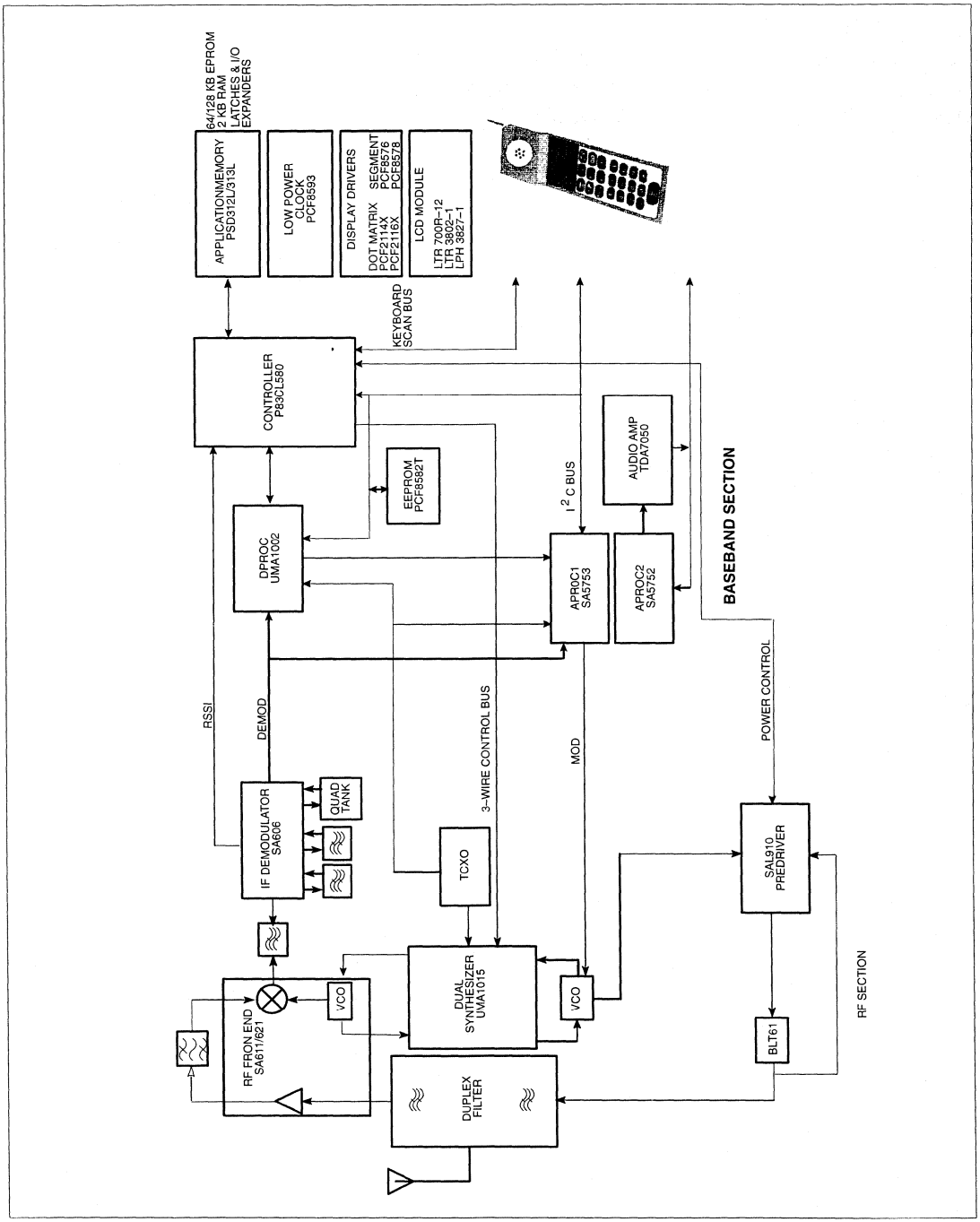
For the FM–IF, either the SA606 or the SA616 can be used. Both down–convert the 1st IF signal to provide the audio/data RSSI signals. The UMA1015 dual frequency synthesizer locks the receive and transmit VCOs. In the PA section, the SA910 is the low–voltage, high efficiency, pre–driver IC for the output power transistor (eg. BLT61).

Baseband Section

The AMPS/(E)TACS baseband solution handles all audio and data processing, control and memory functions. The SA5752, SA5753 audio processors and TDA7050 audio amplifier provide companding, VOX, filtering, amplification and control functions needed to meet AMPS and (E)TACS system requirements. The UMA1002 low voltage data processor incorporates all of the necessary data transceiving, processing and SAT functions. The P83CL580 8-bit microcontroller, PCF8582T EEPROM and PSD312L EPROM provide the control and memory for the entire handset.

The Philips Semiconductors AMPS/(E)TACS/CDPD chipset consists of:		IC17 Page
SA611/621	Low voltage LNA and mixer - 1GHz	
SA606	Low-voltage high performance mixer FM IF system	
UMA1015M	Low-power dual frequency synthesizer for radio communications	
SA5752	Audio processor - companding, VOX and amplifier section	
SA5753	Audio processor - filter and control section	
UMA1002	Data processor for cellular radio (DPROC2)	
P83CL580	8-Bit Microcontroller	
TDA7050	Audio amplifier	
SA910	Variabe gain RF predriver amplifier	

AMPS/(E)TACS/CDPD Analog Cellular



COMPLETE CT0 ANALOG CORDLESS CHIPSET

Philips fully supports all analog cordless standards with chipsets, discrete and module solutions, together with software/firmware, demo boards and comprehensive design-in/application support. Because our baseband modules/chipsets include some commonality in components and software, our CT0 solutions offer a low-risk investment for OEMs wishing to enter the analog cordless market. Demo/evaluation boards are available to cover all CT0 frequencies.

The low-frequency CT0 analog cordless standard is established in many countries at various frequencies around 50 MHz, including:

- France (26/41 MHz)
- Australia (30/39 MHz)
- The Netherlands and Spain (31/40 MHz)
- China, S. Korea, Taiwan, USA, Latin America (46/49 MHz)
- China (48/74 MHz).

As this market continues to grow (in terms of countries and increasing user density), our complete CT0 module/chipset system approach offers a low-cost solution with several competitive advantages. Our CT0-V3A chipset, for example, offers the following functionality:

- Auto-scan multiple-channel access (MCA) system automatically detects and selects a free channel for incoming and outgoing calls
- 1200 bps minimum shift keying (MSK) data transmission for high spectral efficiency and low-energy harmonics
- Supports up to seven handsets
- Call transfer between base unit and each handsets
- 20-bit digital security code, user programmable
- Advanced, patented power-saving scheme
- 10 days of stand-by with 270 mAh battery
- Two-way paging and intercom
- Speakerphone on base unit
- EEPROM for non-volatile storage of repertory memory and security code
- Independent repertory memory for base unit and each handset
- Tone/pulse mix-mode dialing
- Channel display in base unit
- Built-in 'test modes' to facilitate test alignment
- Jumper selectable country options (need to modify RF circuit accordingly).

Other recent additions to our range include the TEA1118 and TEA118A, which are derivatives of our TEA1112 speech/transmission ICs. These new ICs have transmit inputs which handle signals up to 1 Vrms with less than 2% THD, and have low transmit gain (typically 11 dB). The TEA1118A incorporates DTMF, Mute and transmit Mute inputs, and is therefore particularly suitable for CT0.

Philips Semiconductors' CT0 chipset consists of the following ICs:

TDA7052A/AT - 1 Watt low voltage audio power amp with DC volume control

SA676 - Low voltage mixer FM IF system

SA576 - Low power compandor

74V373D - Port extender

PCD3353 or **PCD3755** - DTMF dialler, EEPROM, RAM, microcontroller (handset)

PCD3354A - DTMF dialler, EEPROM, RAM, microcontroller (base station)

TEA1094 - Speaker phone amplifier (base station)

TEA1062A or **TEA1118/A** - Speech and line interfaces (base station)

LC7152M - Dual PLL synthesizer

HEF4511 - Seven-segment driver

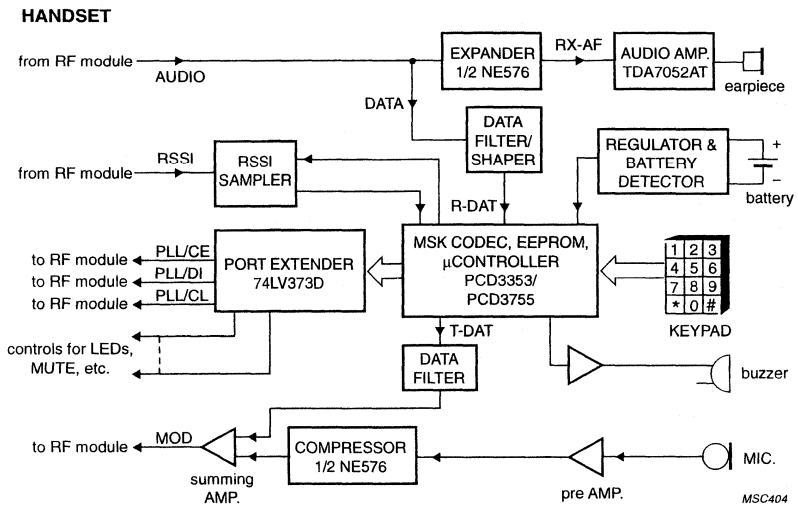


Fig.1 CT0-V3A handset chipset.

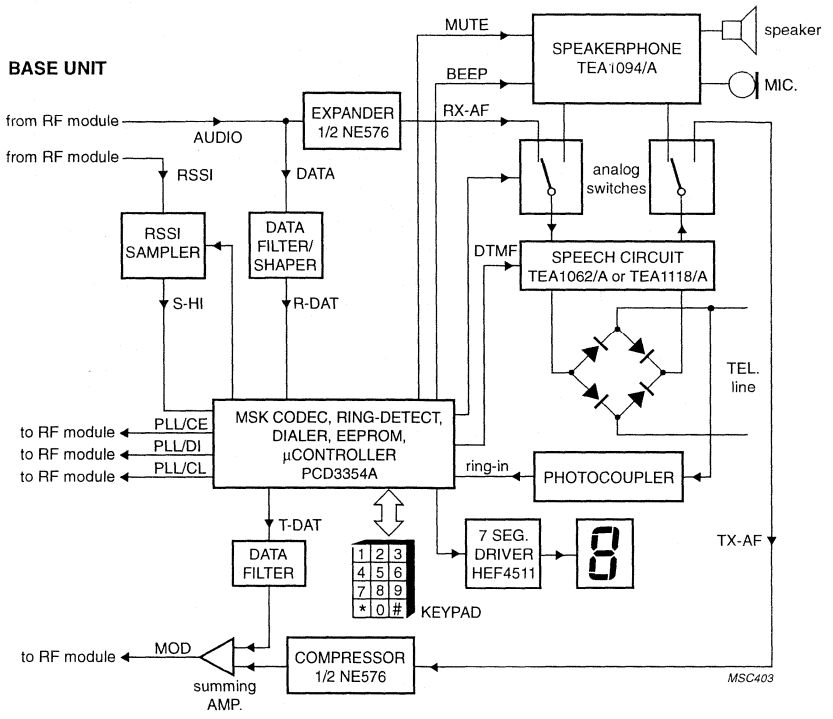


Fig.2 CT0-V3A base unit chipset.

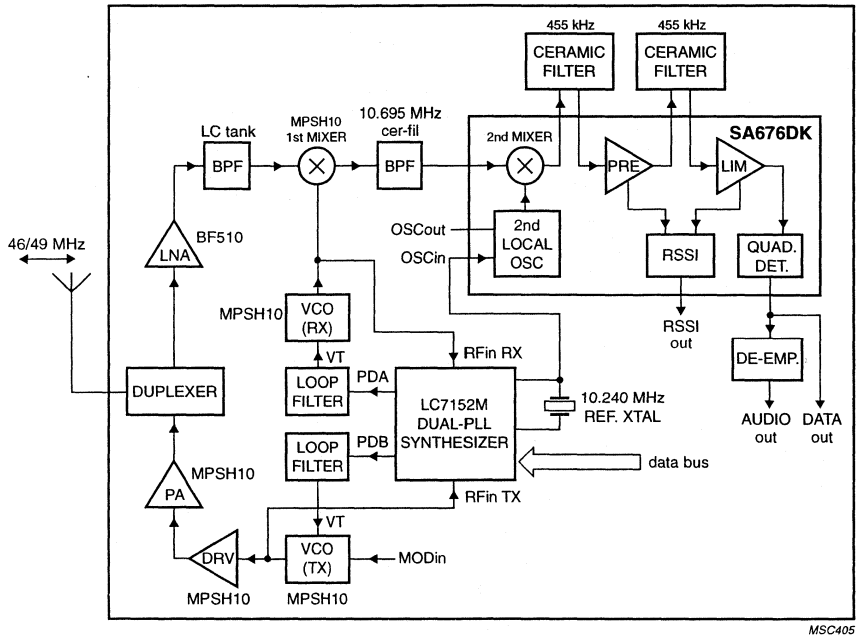


Fig.3 RF module for CT0.

PAGING

FLEX™

FLEX™ is now the de-facto high-speed paging standard with the following advantages:

- More subscribers per given frequency and shorter transmission air time
- Highly improved battery life
- Very robust signal codes (fewer missed or corrupted messages)
- Efficient traffic management for service provider possible.

The FLEXChip™ PCD5008 pager decoder has the following key features:

- FLEX™ paging protocol decoder
- Bitrates: 1600, 3200 and 6400 bps
- 16 short or 8 long addresses, 16 fixed temporary addresses
- Any-phase decoding
- RTC time base and "Over-the-air" time update support
- Compatible with synthesized receivers
- Low Battery Indication (external detector)
- Low profile LQFP32 package
- Low voltage 1.8 to 3.6 V
- Low power consumption by using hardware decoding

A demoboard and application notes are available for this decoder.

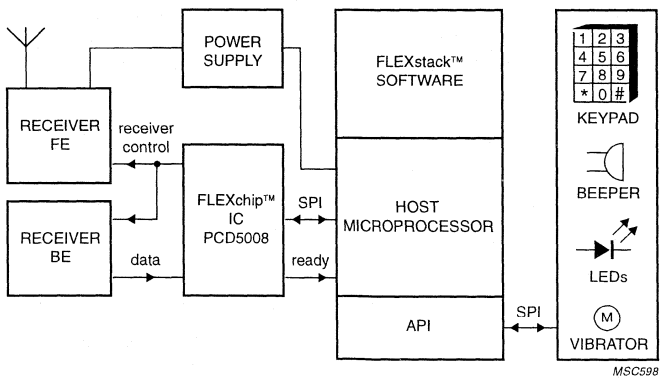


Fig.1 FLEX™ circuit diagram.

POCSAG/APOC1

We offer five advanced chips for all the key functions of beep-only, numeric and alphanumeric pagers:

UAA2080/2 - pager receiver

PCF5001 - POCSAG paging decoder

PCD5003 - advanced POCSAG paging decoder

PCD5002 - advanced POCSAG/APOC1 paging decoder

Evaluation kits and application notes are available for these components.

UAA2080/82 PAGER RECEIVERS

These are high-performance low-power radio receiver circuits primarily intended for VHF and UHF wide-area (country-wide) digital pagers. With a high level of integration, both devices can be used in very thin pagers (e.g. wrist-watch or credit card types). Employing direct FM non-return-to-zero (NRZ) frequency shift keying (FSK), the receivers are based on the direct conversion principle (zero IF). Operating up to 2400 baud, the UAA2080/82 are unique in their size, power consumption and performance advantages. The UAA2082 has additionally a low-battery detect voltage of 1.1 V; the internal oscillator is disconnected when using direct injection from a frequency synthesizer, to further reduce current consumption.

Key features include:

- high integration level
- wide frequency range
- low power consumption
- high sensitivity
- high dynamic range
- interfaces directly with the PCF5001, PCD5002, PCD5003
- QFP32, SO28 package or naked chip.

PCF5001 LOW COST POCSAG PAGING DECODER

This is a fully integrated low-power decoder and pager controller, which was specially developed for radio pagers. It interfaces directly to the UAA2080/82 digital paging receivers. It decodes the CCIR radio paging Code No.1 at 512, 1200 and 2400 bits/s data rates and includes a digital input filter for high call success rates.

Key features include:

- extremely cost efficient (low price/performance ration)
- on-chip 114-bit EEPROM storage
- wide supply voltage range (1.5 to 6 V)
- low supply current (60 A with 76.8 kHz crystal)
- data rates up to 2400 bits/s possible
- supports 4 user addresses (Receiver Identity Codes) in 2 independent frames
- drives an LED, a magnetic or piezo ceramic beeper directly and offers optional vibrator type alerting
- silent call storage (up to 8 calls)
- QFP32, SO28 package or naked chip.

PCD5002 ADVANCED POCSAG AND APOC1 PAGING DECODER

The PCD5002 is a very low power pager decoder and controller, capable of handling both standard POCSAG and the advanced APOC1 code. Data rates supported are 512, 200 and 2400 bps using a single 76.8 kHz crystal. On-chip EEPROM is programmable using a minimum supply voltage of 2.5 V.

Key features include:

- POCSAG compatible
- APOC1 compatible for extended battery economy
- data rates supported are 512, 1200 and 2400 bps using a single 76.8 kHz crystal
- advanced ACCESS synchronization algorithm
- 2-bit random and (optional) 4-bit burst error correction
- up to 6 user address frames, independently programmable
- continuous data decoding upon reception of user programmable sync word (optional)
- call alert via beeper, vibrator or LED
- separate power control of receiver and RF oscillator for battery economy
- on-chip EEPROM (384 bit) is programmable using a minimum supply voltage of 2.5 V
- on-chip SRAM buffer for message data
- wake-up interrupt for microcontroller, programmable polarity
- real Time Clock reference output
- on-chip voltage doubler
- I^2C-interface to microcontroller for transfer of data, status/control and EEPROM programming (max 100 kb/s)
- interface to UAA2080 and UAA2082 paging receivers
- wide operating voltage range 1.5 to 6.0 V

PCD5003 POCSAG PAGING DECODER

The PCD5003 is a very low power decoder and pager controller. It supports data rates of 512, 1200 and 2400 bps using a single 76.8 kHz crystal. Its on chip EEPROM is programmable with a minimum supply of 2.5 V.

Key features are:

- low operating current (50 mA ON; 25 mA OFF)
- 2-bit random and (optional) 4-bit burst address error correction
- up to 6 user addresses (RICs), in up to 6 different frames
- standard POCSAG synch. word, plus up to 4 user-programmable synch. words
- received data inversion (optional)
- synthesizer set-up and control interface (3-line serial)
- separate power control or Receiver and RF oscillator for battery economy
- on-chip SRAM buffer for message data
- direct and I^2C-bus control of operating status (ON/OFF)
- wake-up interrupt for microcontroller, programmable polarity
- built-in data filter and bit clock recovery
- low profile package LQFP32

EVALUATION KITS

OM4706 - POCSAG decoder board PCF5001

OM4718 - Test program board for PCF5001

OM4745 - 2080H 173 MHz

OM4746 - 2080H 288 MHz

OM4747 - 2080H 470 MHz

OM4748 - 2080H frequency open

OM4749 - Pager bit error rate test board

OM4759 - PALOMA SW for pager antenna calc.

OM4763 - PCD5003 POCSAG decoder system

OM5837 - Pager demo system for the PCD5008 FLEX™ decoder

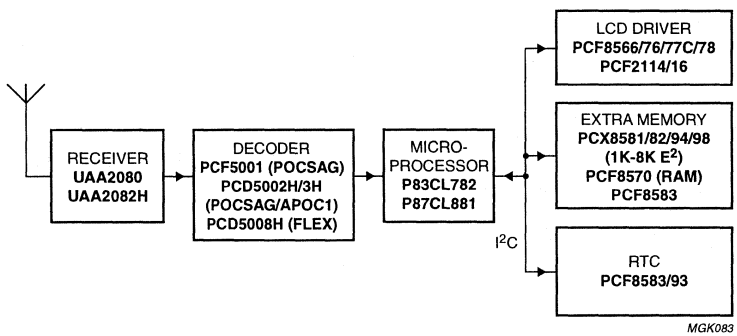


Fig.2 Paging solutions.

GENERAL

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Pro electron type numbering for discrete semiconductors	87
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TOTAL QUALITY MANAGEMENT

Philips Semiconductors is a Quality Company, renowned for the high quality of our products and service. We keep alive this tradition by constantly aiming towards one ultimate standard, that of zero defects. This aim is guided by our Total Quality Management (TQM) system, the basis of which is described in the following paragraphs.

Quality assurance

Based on ISO 9000 standards, customer standards such as Ford TQE and IBM MDQ. Our factories are certified to ISO 9000 by external inspectorates.

Partnerships with customers

PPM co-operations, design-in agreements, ship-to-stock, just-in-time and self-qualification programmes, and application support.

Partnerships with suppliers

Ship-to-stock, statistical process control and ISO 9000 audits.

Quality improvement programme

Continuous process and system improvement, design improvement, complete use of statistical process control, realization of our final objective of zero defects, and logistics improvement by ship-to-stock and just-in-time agreements.

ADVANCED QUALITY PLANNING

During the design and development of new products and processes, quality is built-in by advanced quality planning. Through failure-mode-and-effect analysis the critical parameters are detected and measures taken to ensure good performance on these parameters. The capability of process steps is also planned in this phase.

PRODUCT CONFORMANCE

The assurance of product conformance is an integral part of our quality assurance (QA) practice. This is achieved by:

- Incoming material management through partnerships with suppliers.
- In-line quality assurance to monitor process reproducibility during manufacture and initiate any necessary corrective action. Critical process steps are 100% under statistical process control.
- Acceptance tests on finished products to verify conformance with the device specification. The test results are used for quality feedback and corrective actions. The inspection and test requirements are detailed in the general quality specifications.
- Periodic inspections to monitor and measure the conformance of products.

PRODUCT RELIABILITY

With the increasing complexity of Original Equipment Manufacturer (OEM) equipment, component reliability must be extremely high. Our research laboratories and development departments study the failure mechanisms of semiconductors. Their studies result in design rules and process optimization for the highest built-in product reliability. Highly accelerated tests are applied to the products reliability evaluation. Rejects from reliability tests and from customer complaints are submitted to failure analysis, to result in corrective action.

CUSTOMER RESPONSES

Our quality improvement depends on joint action with our customer. We need our customer's inputs and we invite constructive comments on all aspects of our performance. Please contact our local sales representative.

RECOGNITION

The high quality of our products and services is demonstrated by many Quality Awards granted by major customers and international organizations.

DISCRETE SEMICONDUCTORS

Basic type number

This type designation code applies to discrete semiconductor devices (not integrated circuits), multiples of such devices, semiconductor chips and Darlington transistors.

FIRST LETTER

The first letter gives information about the material for the active part of the device.

A Germanium or other material with a band gap of 0.6 to 1 eV

B Silicon or other material with a band gap of 1 to 1.3 eV

C Gallium arsenide (GaAs) or other material with a band gap of 1.3 eV or more

R Compound materials, e.g. cadmium sulphide.

SECOND LETTER

The second letter indicates the function for which the device is primarily designed. The same letter can be used for multi-chip devices with similar elements.

In the following list low power types are defined by $R_{th\ j\text{-}mb} > 15$ K/W and power types by $R_{th\ j\text{-}mb} \leq 15$ K/W.

A Diode; signal, low power

B Diode; variable capacitance

C Transistor; low power, audio frequency

D Transistor; power, audio frequency

E Diode; tunnel

F Transistor; low power, high frequency

G multiple of dissimilar devices/miscellaneous devices; e.g. oscillators. Also with special third letter, see under "Serial number/special third letter"

H Diode; magnetic sensitive

L Transistor; power, high frequency

N Photocoupler

P Radiation detector; e.g. high sensitivity photo-transistor; with special third letter

Q Radiation generator; e.g. LED, laser; with special third letter

R Control or switching device; e.g. thyristor, low power; with special third letter

S Transistor; low power, switching

T Control and switching device; e.g. thyristor, power; with special third letter

U Transistor; power, switching

W Surface acoustic wave device

X Diode; multiplier, e.g. varactor, step recovery

Y Diode; rectifying, booster

Z Diode; voltage reference or regulator, transient suppressor diode; with special third letter.

SERIAL NUMBER/SPECIAL THIRD LETTER

The number comprises three figures running from 100 to 999 for devices primarily intended for consumer equipment, or one letter (Z, Y, X, etc.) and two figures running from 10 to 99 for devices primarily intended for industrial or professional equipment.(1) The letter has no fixed meaning, except in the following cases:

A For triacs, after second letter 'R' or 'T'

F For emitters and receivers in fibre-optic communication, after second letter 'G', 'P' or 'Q'. When the second letter is 'G', the first letter should be defined in accordance with the material of the main optical device.

L For lasers in non-fibre-optic applications, after second letter 'G' or 'Q'. When the second letter is 'G', the first letter should be defined in accordance with the material of the main optical device.

O For opto-triacs, after second letter 'R'

T For 3-state bicolour LEDs, after second letter 'Q'

W For transient voltage suppressor diodes, after second letter 'Z'.

EXAMPLES OF BASIC TYPE NUMBERS

AA112	Germanium, low power signal diode (consumer type)
ACY32	Germanium, low power AF transistor (industrial type)
BD232	Silicon, power AF transistor (consumer type)
CQY17	GaAs, light-emitting diode (industrial type)
RPY84	CdS, photo-conductive cell (industrial type).

Version letter(s)

One or two letters may be added to the basic type number to indicate minor electrical or mechanical variants of the basic type. The letters never have a fixed meaning, except that the letter 'R' indicates reverse polarity and the letter 'W' indicates a surface mounted device (SMD).

(1) When the supply of these serial numbers is exhausted, the serial number may be expanded to three figures for industrial types and four figures for consumer types.

Suffix

Sub-classification can be used for devices supplied in a wide range of variants, called associated types. The following sub-coding suffixes are in use:

VOLTAGE REFERENCE AND VOLTAGE REGULATOR DIODES

One letter and one number, preceded by a hyphen (-). The letter, if required, indicates the nominal tolerance of the Zener voltage.

A 1%

B 2%

C 5%

D 10%

E 20%.

In the case of a 3% tolerance, the letter 'F' is used.

The number denotes the typical operating (Zener) voltage, related to the nominal current rating for the entire range. The letter 'V' is used in place of the decimal point.

Example: BZY74-C6V3 or -C10.

TRANSIENT VOLTAGE SUPPRESSOR DIODES

One number, preceded by a hyphen (-). The number indicates the maximum recommended continuous reversed (stand-off) voltage, V_R. The letter 'V' is used in place of the decimal point.

Example: BZW70-9V1 or –39.

The letter 'B' may be used immediately after the last number, to indicate a bidirectional suppressor diode.

Example: BZW10-15B.

CONVENTIONAL AND CONTROLLED AVALANCHE RECTIFIER DIODES AND THYRISTORS

One number, preceded by a hyphen (-). The number indicates the rated maximum repetitive peak reverse voltage, V_{RRM}, or the rated repetitive peak off-state voltage, V_{DRM}, whichever is the lower. Reversed polarity with respect to the case is indicated by the letter 'R' immediately after the number.

Example: BYT-100 or -100R.

RADIATION DETECTORS

One number, preceded by a hyphen (-). The number indicates the depletion layer in micrometres (μm). The resolution is indicated by a version letter.

Example: BPX10-2A.

ARRAY OF RADIATION DETECTORS AND GENERATORS

One number, preceded by a hyphen (-). The number indicates the number of basic devices assembled into the array.

Examples: BPW50-6, BPW50-9, BPW50-12.

HIGH FREQUENCY POWER TRANSISTORS

One number, preceded by a hyphen (-). The number indicates the supply voltage.

Example: BLU80-24.

INTEGRATED CIRCUITS

Basic type number

This type designation code applies to semiconductor monolithic, semiconductor multi-chip, thin film, thick film and hybrid integrated circuits. The basic type number comprises three letters followed by a serial number.

FIRST AND SECOND LETTERS

Digital family circuits

The first two letters identify the family.(1)

Solitary circuits

The first letter divides solitary circuits into:

S Solitary digital circuits

T Analog circuits

U Mixed analog/digital circuits.

The second letter is a serial letter without any further significance except 'H' which stands for hybrid circuits.(2)

Microprocessors

The first two letters identify microprocessors and related circuits:

MA Microcomputer or central processing unit

MB Slice processor (functional slice of microprocessor)

(1) A logic family is an assembly of digital circuits designed to be interconnected and defined by its base electrical characteristics, such as supply voltage, power consumption, propagation delay, noise immunity.

(2) The first letter 'S' should be used for all solitary memories, to which, in the event of hybrids, the second letter 'H' should be added, for example, SH for bubble memories.

MD Related memories

ME Other related circuits such as interfaces, clocks, peripheral controllers, etc.

Charge-transfer devices and switched capacitors

The first two letters identify:

NH Hybrid circuits

NL Logic circuits

NM Memories

NS Analog signal processing using switched capacitors

NT Analog signal processing using charge-transfer devices

NX Imaging devices

NY Other related circuits.

THIRD LETTER

The third letter indicates the operating ambient temperature range:

A temperature range not specified below

B 0 to + 70 °C

C −55 to +125 °C

D −25 to + 70 °C

E −25 to + 85 °C

F −40 to + 85 °C

G −55 to + 85 °C.

If a device has another temperature range, the letter 'A' or a letter indicating a narrower temperature may be used, for example, the range of 0 to +75 °C can be indicated by 'A' or 'B'. Should two devices with the same basic type number both have temperature ranges other than those specified, one would use the letter 'A' and the other the letter 'X'.

Serial number

This may be a four-digit number assigned by Pro Electron, or the serial number (which may be a combination of figures and letters) of an existing company type designation of the manufacturer.

Version letter

A single version letter may be added to the basic type number. This indicates a minor variant of the basic type or the package. The version letter has no fixed meaning except for 'Z' which means customized wiring. The following letters are recommended for package variants:

C Cylindrical

D Ceramic dual in-line (CERDIL, CERDIP)

F Flat pack (two leads)

G Flat pack (four leads)

H Quad flat pack (QFP)

L Chip on tape (foil)

P Plastic dual in-line (DIL)

Q Quad in-line (QUIL)

T Mini pack (SOL, SO, VSO)

U Uncased chip.

Two-letter suffix

A two-letter suffix may be used instead of a single package version letter to give more information. To avoid confusion with serial numbers that end with a letter, a hyphen should precede the suffix.

FIRST LETTER (GENERAL SHAPE)

C Cylindrical

D Dual in-line (DIL)

E Power DIL (with external heatsink)

F Flat pack (leads on two sides)

G Flat pack (leads on four sides)

H Quad flat pack (QFP)

K Diamond (TO-3 family)

M Multiple in-line (except dual, triple and quad)

Q Quad in-line (QUIL)

R Power QUIL (with external heatsink)

S Single in-line (SIL)

T Triple in-line

W Leaded chip carrier (LCC)

X Leadless chip carrier (LLCC)

Y Pin grid array (PGA).

SECOND LETTER (MATERIAL)

C Metal-ceramic

G Glass-ceramic

M Metal

P Plastic.

Examples

PCF1105WP: digital IC; PC family; operating temperature range –40 to +85 °C; serial number 1105; plastic leaded chip carrier.

GMB74LS00A-DC: digital IC; GM family; operating temperature range 0 to +70 °C; company number 74LS00A; ceramic DIL package.

TDA1000P: analog IC; operating temperature range non-standard; serial number 1000; plastic DIL package.

SAC2000: solitary digital circuit; operating temperature range –55 to +125 °C; serial number 2000.

RATING SYSTEMS

The rating systems described are those recommended by the IEC in its publication number 134.

Definitions of terms used

ELECTRONIC DEVICE

An electronic tube or valve, transistor or other semiconductor device. This definition excludes inductors, capacitors, resistors and similar components.

CHARACTERISTIC

A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

BOGEY ELECTRONIC DEVICE

An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics that are directly related to the application.

RATING

A value that establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms. Limiting conditions may be either maxima or minima.

RATING SYSTEM

The set of principles upon which ratings are established and which determine their interpretation. The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

Absolute maximum rating system

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type, as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout the life of the device, no absolute maximum value for the intended service is exceeded with any device, under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

Design maximum rating system

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout the life of the device, no design maximum value for the intended service is exceeded with a bogey electronic device, under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

Design centre rating system

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

ELECTROSTATIC CHARGES

Electrostatic charges can exist in many things; for example, man-made-fibre clothing, moving machinery, objects with air blowing across them, plastic storage bins, sheets of paper stored in plastic envelopes, paper from electrostatic copying machines, and people. The charges are caused by friction between two surfaces, at least one of which is non-conductive. The magnitude and polarity of the charges depend on the different affinities for electrons of the two materials rubbing together, the friction force and the humidity of the surrounding air.

Electrostatic discharge is the transfer of an electrostatic charge between bodies at different potentials and occurs with direct contact or when induced by an electrostatic field. All of our MOS devices are internally protected against electrostatic discharge but they **can** be damaged if the following precautions are not taken.

WORK STATION

Figure 1 shows a working area suitable for safely handling electrostatic sensitive devices. It has a work bench, the surface of which is conductive or covered by an antistatic sheet. Typical resistivity for the bench surface is between 1 and 500 kΩ per cm^2. The floor should also be covered with antistatic material. The following precautions should be observed:

- Persons at a work bench should be earthed via a wrist strap and a resistor.
- All mains-powered electrical equipment should be connected via an earth leakage switch.
- Equipment cases should be earthed.
- Relative humidity should be maintained between 50 and 65%.
- An ionizer should be used to neutralize objects with immobile static charges.

RECEIPT AND STORAGE

MOS devices are packed for dispatch in antistatic/conductive containers, usually boxes, tubes or blister tape. The fact that the contents are sensitive to electrostatic discharge is shown by warning labels on both primary and secondary packing.

The devices should be kept in their original packing whilst in storage. If a bulk container is partially unpacked, the unpacking should be performed at a protected work station. Any MOS devices that are stored temporarily should be packed in conductive or antistatic packing or carriers.

ASSEMBLY

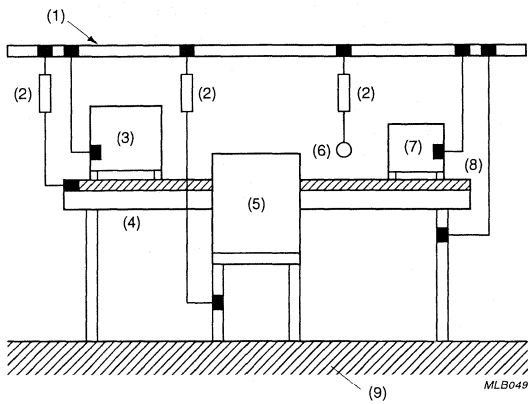
MOS devices must be removed from their protective packing with earthed component pincers or short-circuit clips. Short-circuit clips must remain in place during mounting, soldering and cleansing/drying processes. Do not remove more devices from the storage packing than are needed at any one time. Production/assembly documents should state that the product contains electrostatic sensitive devices and that special precautions need to be taken.

During assembly, ensure that the MOS devices are the last of the components to be mounted and that this is done at a protected work station.

All tools used during assembly, including soldering tools and solder baths, must be earthed. All hand tools should be of conductive or antistatic material and, where possible, should not be insulated.

Measuring and testing of completed circuit boards must be done at a protected work station. Place the soldered side of the circuit board on conductive or antistatic foam and remove the short-circuit clips. Remove the circuit board from the foam, holding the board only at the edges. Make sure the circuit board does not touch the conductive surface of the work bench. After testing, replace the circuit board on the conductive foam to await packing.

Assembled circuit boards containing MOS devices should be handled in the same way as unmounted MOS devices. They should also carry warning labels and be packed in conductive or antistatic packing.



(1) Earthing rail.
(2) Resistor (500 kΩ ± 10%, 0.5 W).
(3) Ionizer.
(4) Work bench.
(5) Chair.
(6) Wrist strap.
(7) Electrical equipment.
(8) Conductive surface/antistatic sheet.
(9) Antistatic floor.

Fig.1 Protected work station.

DEVICE DATA

(in alphanumeric sequence)

Low voltage 8-bit microcontrollers with UART, I²C-bus and ADC

P80CL580; P83CL580

FEATURES

- Full static 80C51 Central Processing Unit
- 8-bit CPU, ROM, RAM, I/O in a 56-lead VSO or 64-lead QFP package
- 256 bytes on-chip RAM Data Memory
- 6 kbytes on-chip ROM Program Memory for P83CL580
- External memory expandable up to 128 kbytes: RAM up to 64 kbytes and ROM up to 64 kbytes
- Five 8-bit ports; 40 I/O lines
- Three 16-bit Timers/Event counters
- On-chip oscillator suitable for RC, LC, quartz crystal or ceramic resonator
- Fifteen source, fifteen vector, nested interrupt structure with two priority levels
- Full duplex serial port (UART)
- I²C-bus interface for serial transfer on two lines
- Analog-to-digital converter (ADC) with Power-down mode; 4 input channels and 8-bit ADC
- Pulse Width Modulated (PWM) output (8-bit resolution)
- Watchdog Timer
- Enhanced architecture with:
  - non-page oriented instructions
  - direct addressing
  - four 8-byte RAM register banks
  - stack depth limited only by available internal RAM (maximum 256 bytes)
  - multiply, divide, subtract and compare instructions
- Reduced power consumption through Power-down and Idle modes
- Wake-up via external interrupts at Port 1
- Frequency range: 0 to 12 MHz. For ADC operation minimum 250 kHz at 2.7 V
- Supply voltage: 2.5 to 6.0 V
- Very low current consumption: typically 4.5 mA at 2.5 V and 8 MHz
- Operating ambient temperature range: –40 to +85 °C.

GENERAL DESCRIPTION

The P80CL580; P83CL580 (hereafter generally referred to as P8xCL580) is manufactured in an advanced CMOS technology. The P8xCL580 has the same instruction set as the 80C51, consisting of over 100 instructions: 49 one-byte, 46 two-byte, and 16 three-byte. The device operates over a wide range of supply voltages and has low power consumption; there are two software selectable modes for power reduction: Idle and Power-down. For emulation purposes, the P85CL580 (piggy-back version) with 256 bytes of RAM is recommended.

This data sheet details the specific properties of the P80CL580; P83CL580. For details of the 80C51 core and the I²C-bus see *"Data Handbook IC20"*.

ROMless version: P80CL580

The P80CL580 is the ROMless version of the P83CL580. The mask options on the P80CL580 are fixed as follows:

- All ports have option '1S' (standard port, HIGH after reset), except ports P1.6 and P1.7 which have option '2S' (open-drain, HIGH after reset)
- Oscillator option: Oscillator 3
- Power-on-reset option: off.

APPLICATIONS

The P8xCL580 is an 8-bit general purpose microcontroller especially suited for cordless telephone and mobile communication applications. The P8xCL580 also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities.

Full Data Sheet: on CD-ROM/WWW (Internet) or FOD-system (details in front Section/back of this HB), or updated Loose leaf or Parent HB

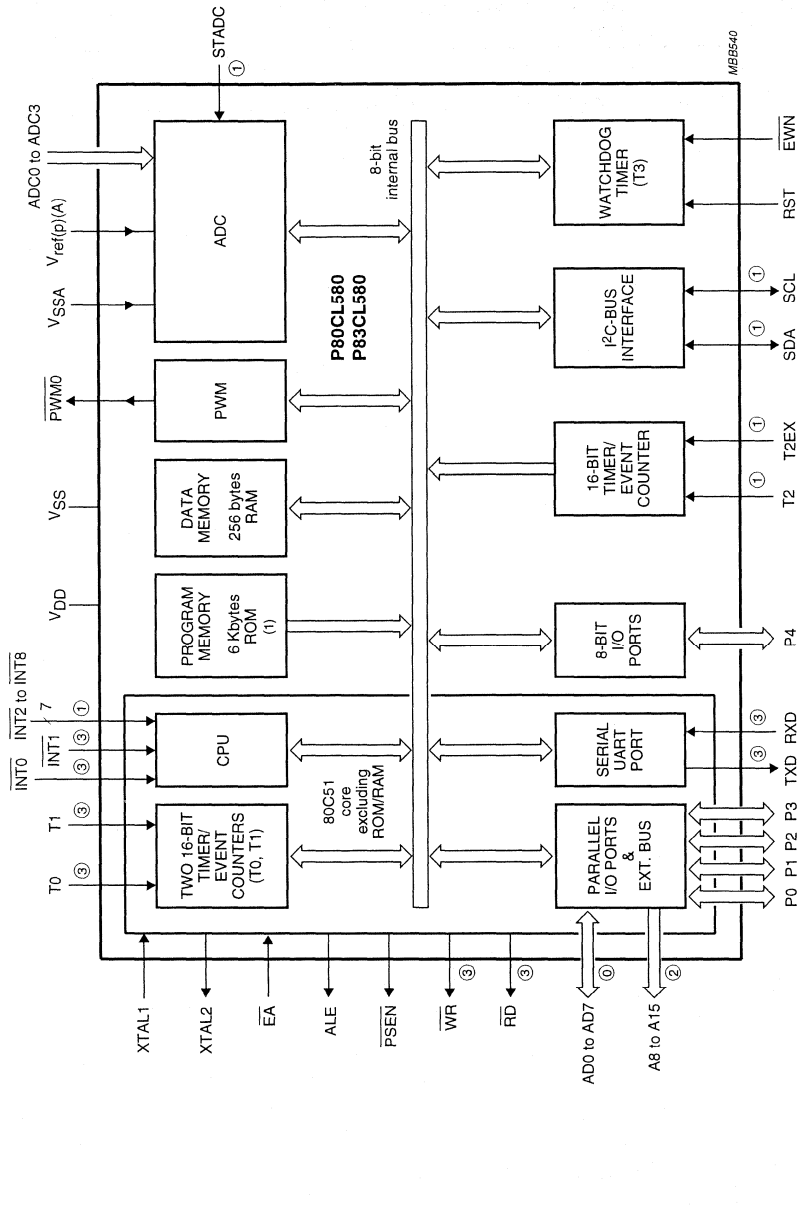
ORDERING INFORMATION

TYPE NUMBER[1]	PACKAGE		
	NAME	DESCRIPTION	VERSION
P8xCL580HFT	VSO56	plastic very small outline package; 56 leads	SOT190-1
P8xCL580HFH	QFP64	plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm	SOT319-2

Note

1. 'x' = 0 or 3. Refer to the Order Entry Form (OEF) for this device for the full type number, including options/program.

BLOCK DIAGRAM



(1) Not available in the **P80CL580**.

Fig.1 Block diagram.

FUNCTIONAL DIAGRAM

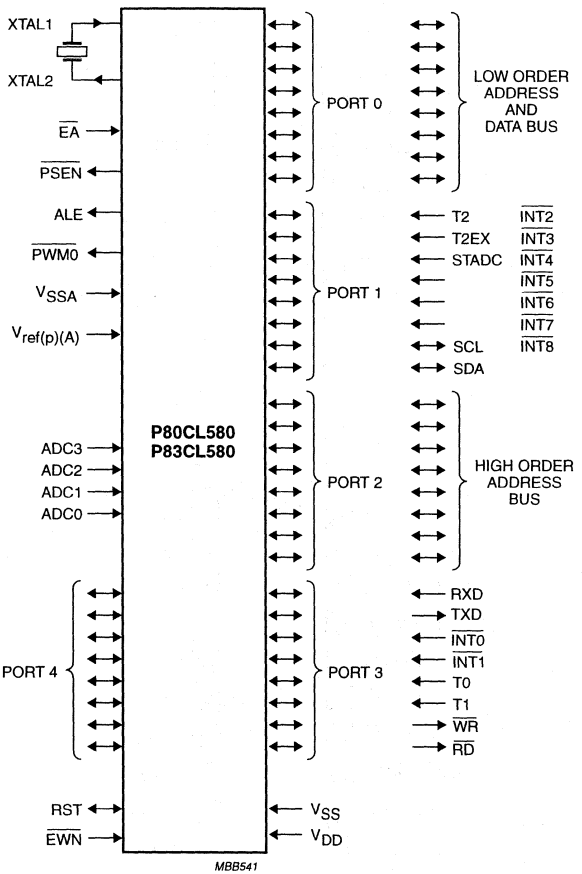


Fig.2 Functional diagram.

PINNING INFORMATION

Pinning

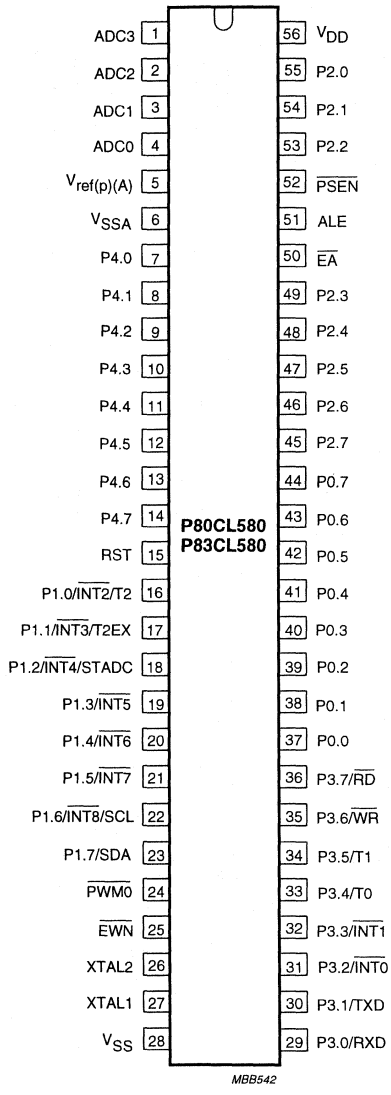


Fig.3 Pin configuration for VSO56 package.

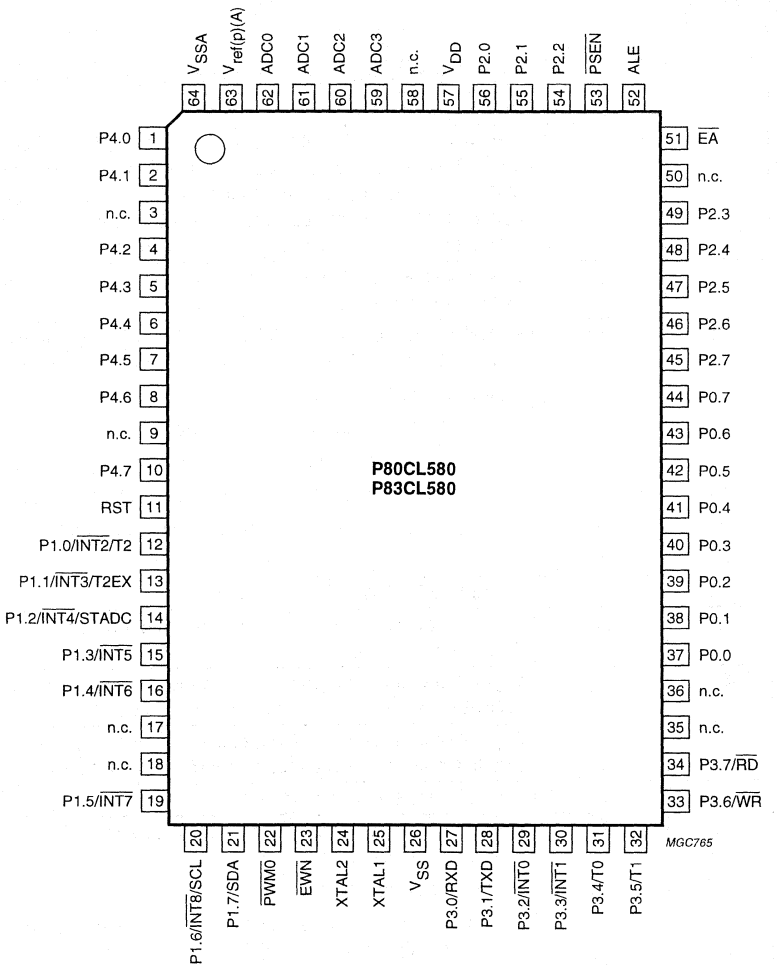


Fig.4 Pin configuration for QFP64 package.

Pin description

Table 1 Pin description for VSO56 (SOT190-1) and QFP64 (SOT319-2)

SYMBOL	PIN		DESCRIPTION
	VSO56	QFP64	
ADC3 to ADC0	1 to 4	59 to 62	4 input channels to the ADC.
$V_{ref(p)(A)}$	5	63	Positive potential of analog-to-digital conversion reference resistor.
V_{SSA}	6	64	Analog part ground.
P4.0 to P4.7	7 to 14	1, 2, 4 to 8, 10	**Port 4**: 8-bit bidirectional I/O port. (P4.0 to P4.7). Port pins that have logic 1s written to them are pulled HIGH by internal pull-ups, and in this state can be used as inputs. As inputs, Port 4 pins that are externally pulled LOW will source current (I_{IL}) due to the internal pull-ups. Port 4 output buffers can sink/source 4 LS TTL loads.
RST	15	11	**Reset**: a HIGH level on this pin for two machine cycles while the oscillator is running resets the device.
P1.0/$\overline{INT2}$/T2 P1.1/$\overline{INT3}$/T2EX P1.2/$\overline{INT4}$/STADC P1.3/$\overline{INT5}$ P1.4/$\overline{INT6}$ P1.5/$\overline{INT7}$ P1.6/$\overline{INT8}$/SCL P1.7/SDA	16 17 18 19 20 21 22 23	12 13 14 15 16 19 20 21	• **Port 1:** 8-bit bidirectional I/O port (P1.0 to P1.7). Same characteristics as Port 4, but note that P1.6 and P1.7 are open-drain only. • **Alternative functions:** – INT2 to INT8 are external interrupt inputs – STADC is the external trigger of the analog-to-digital converter – T2 and T2EX are the Timer/event counter 2 inputs – SCL and SDA are the I²C-bus clock and data lines.
$\overline{PWM0}$	24	22	**Pulse Width Modulation output 0**.
$\overline{EWN}$	25	23	**Enable Watchdog Timer**: enable for Watchdog Timer and enable Power-down mode.
XTAL2	26	24	**Crystal oscillator output**: output of the inverting amplifier of the oscillator. Left open when external clock is used.
XTAL1	27	25	**Crystal oscillator input**: input to the inverting amplifier of the oscillator, also the input for an externally generated clock source.
V_{SS}	28	26	Ground: circuit ground potential.
P3.0/RXD P3.1/TXD P3.2/$\overline{INT0}$ P3.3/$\overline{INT1}$ P3.4/T0 P3.5/T1 P3.6/$\overline{WR}$ P3.7/$\overline{RD}$	29 30 31 32 33 34 35 36	27 28 29 30 31 32 33 34	• **Port 3:** 8-bit bidirectional I/O port (P3.0 to P3.7). Same characteristics as Port 4. • **Alternative functions:** – RXD is the UART serial data input (asynchronous) or data input/output (synchronous) – TXD is the UART serial data output (asynchronous) or clock output (synchronous) – $\overline{INT0}$ and $\overline{INT1}$ are external interrupts 0 and 1 – T0 and T1 are external inputs for timers 0 and 1 – $\overline{WR}$ is the external Data Memory write strobe – $\overline{RD}$ is the external Data Memory read strobe.

SYMBOL	PIN		DESCRIPTION
	VSO56	QFP64	
P0.0 to P0.7	37 to 44	37 to 44	• **Port 0**: 8-bit open-drain bidirectional I/O port. As an open-drain output port it can sink 8 LS TTL loads. Port 0 pins that have logic 1s written to them float, and in that state will function as high impedance inputs. • **Low-order addressing**: Port 0 is also the multiplexed low-order address and data bus during access to external memory. The strong internal pull-ups are used while emitting logic 1s within the low order address.
P2.0 to P2.7	55 to 53, 49 to 45	56 to 54, 49 to 45	• **Port 2**: 8-bit bidirectional I/O port with internal pull-ups. Same characteristics as Port 4. • **High-order addressing**: Port 2 emits the high-order address byte during accesses to external memory that use 16-bit addresses (MOVX @DPTR). In this application it uses the strong internal pull-ups when emitting logic 1s. During accesses to external memory that use 8-bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.
$\overline{EA}$	50	51	**External Access**. When $\overline{EA}$ is held HIGH the CPU executes out of internal Program Memory (unless the program counter exceeds 17FFH). Holding $\overline{EA}$ LOW forces the CPU to execute out of external memory regardless of the value of the Program Counter.
ALE	51	52	**Address Latch Enable**. Output pulse for latching the low byte of the address during access to external memory. ALE is emitted at a constant rate of $1/6 \times f_{osc}$, and may be used for external timing or clocking purposes (assuming MOVX instructions are not used).
$\overline{PSEN}$	52	53	**Program Store Enable**. Output read strobe to external Program Memory. When executing code out of external Program Memory, $\overline{PSEN}$ is activated twice each machine cycle. However, during each access to external Data Memory two $\overline{PSEN}$ activations are skipped.
V_{DD}	56	57	Power supply.
n.c.	–	3, 9, 17, 18, 35, 36, 50 and 58	Not connected.

Low voltage 8-bit microcontrollers with UART and I²C-bus

P83CL781; P83CL782

FEATURES

- Full static 80C51 CPU
- 8-bit CPU, ROM, RAM, I/O in a 40-lead DIP or 44-lead QFP package
- 16 kbytes ROM, expandable externally to 64 kbytes
- 256 bytes RAM, expandable externally to 64 kbytes
- Four 8-bit ports, 32 I/O lines
- Three 16-bit timer/event counters
- External memory expandable up to 128 kbytes: RAM up to 64 kbytes and ROM up to 64 kbytes
- On-chip oscillator suitable for RC, LC, quartz crystal or ceramic resonator
- Fifteen source, fifteen vector interrupt structure with two priority levels
- Full duplex serial port (UART)
- I²C-bus interface for serial transfer on two lines
- Enhanced architecture with:
  - non-page oriented instructions
  - direct addressing
  - four 8 byte RAM register banks
  - stack depth limited only by available internal RAM (maximum 256 bytes)
  - multiply, divide, subtract and compare instructions
- Reduced power consumption through Power-down and Idle modes
- Wake-up via external interrupts at Port 1
- Single supply voltage of 1.8 to 6.0 V
- Operating ambient temperature:
  - 83CL781: –40 to +85 °C
  - 83CL782: –25 to +55 °C.
- Frequency range of DC to 12 MHz
- Very low current consumption.

GENERAL DESCRIPTION

The term P83CL78x is used throughout this data sheet to refer to both the P83CL781 and P83CL782; differences between the devices are highlighted in the text.

The P83CL78x is manufactured in an advanced CMOS technology. The P83CL78x has the same instruction set as the 80C51, consisting of over 100 instructions: 49 one-byte, 46 two-byte, and 16 three-byte. The device has low power consumption and a wide range of supply voltage; there are two software-selectable modes of reduced activity for further power reduction: Idle and Power-down. For emulation purposes, the P85CL781 (piggy-back version) with 256 bytes of RAM is recommended.

The P83CL782 is a faster version of the P83CL781 and operates at a maximum frequency of 12 MHz at $V_{DD} \geq 3.1$ V.

This data sheet details the specific properties of the P83CL78x. For details of the 80C51 core and the I²C-bus see *"Data Handbook IC20"*.

APPLICATIONS

The P83CL78x is an 8-bit general purpose microcontroller especially suited for cordless telephone applications. The P83CL78x also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities.

Full Data Sheet: on CD-ROM/WWW (Internet) or FOD-system (details in front Section/back of this HB), or updated Loose leaf or Parent HB

ORDERING INFORMATION

TYPE NUMBER[1]	PACKAGE		
	NAME	DESCRIPTION	VERSION
P83CL781HFP	DIP40	plastic dual in-line package; 40 leads (600 mil)	SOT129-1
P83CL782HDP			
P83CL781HFH	QFP44	plastic quad flat package; 44 leads (lead length 2.35 mm); body 14 × 14 × 2.2 mm	SOT205-1
P83CL782HDH			
P83CL781HFH	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2
P83CL781HDH			

Note

1. Refer to the Order Entry Form (OEF) for this device for the full type number, including options/program.

BLOCK DIAGRAM

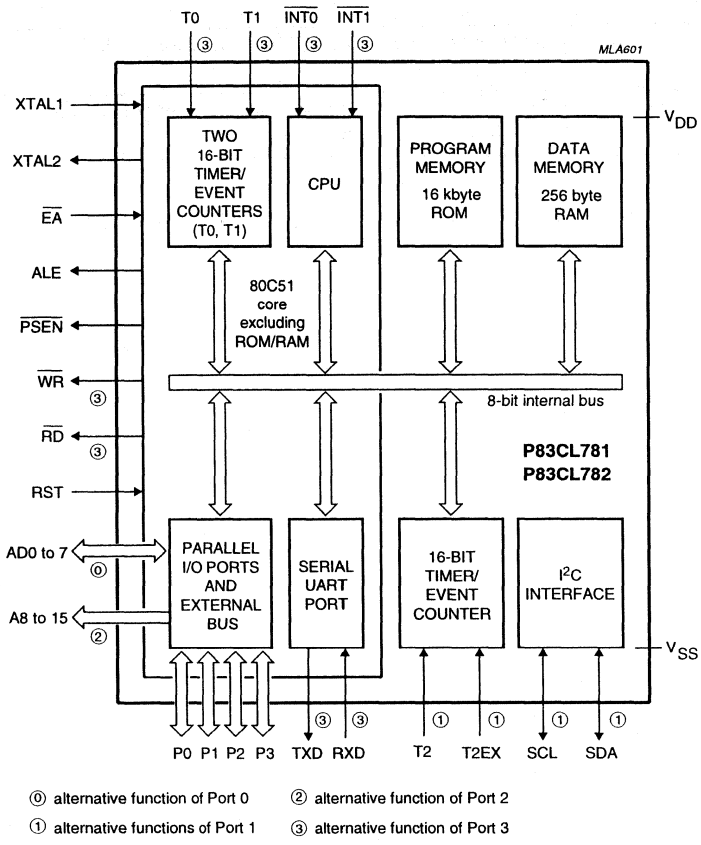


Fig.1 Block diagram.

FUNCTIONAL DIAGRAM

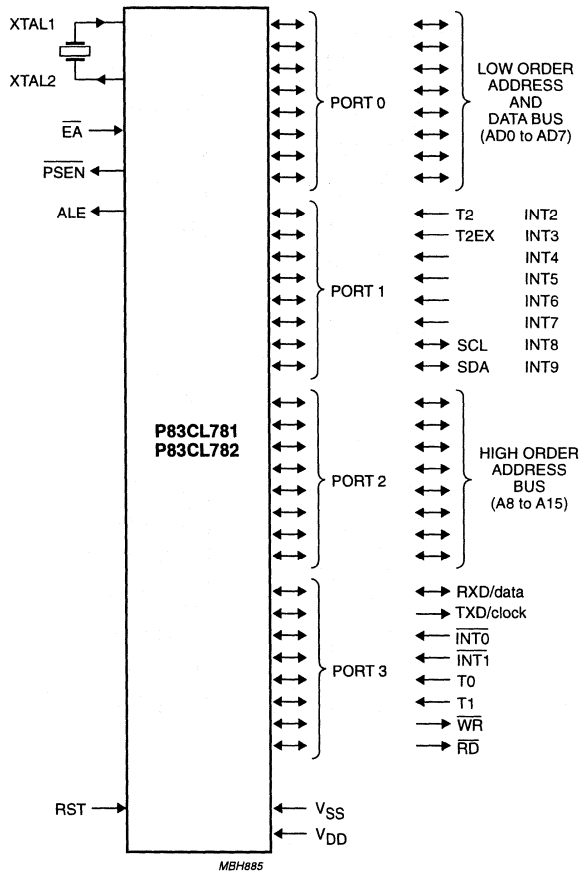


Fig.2 Functional diagram.

PINNING INFORMATION

0.1 Pinning

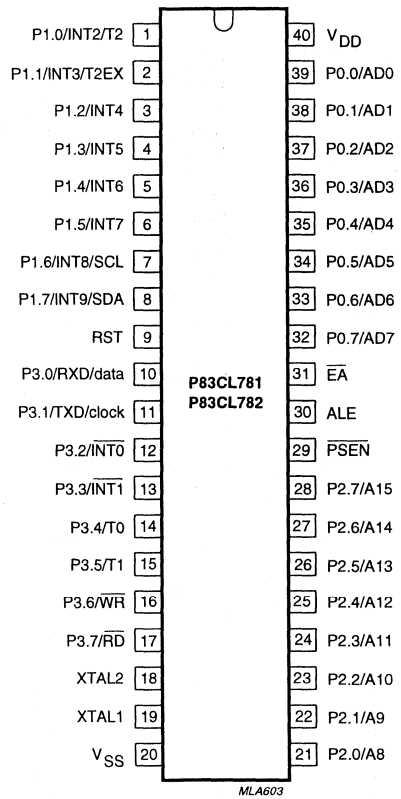


Fig.3 Pin configuration for DIP40 package.

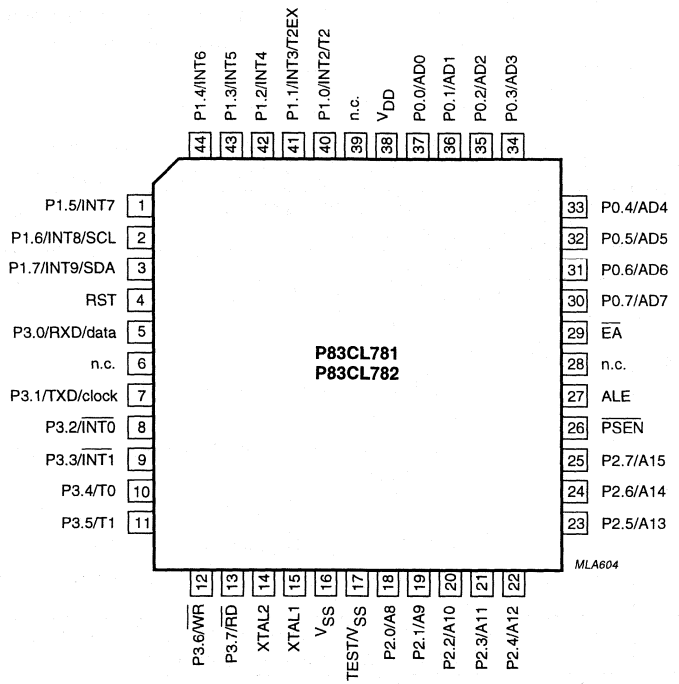


Fig.4 Pin configuration for QFP44 packages.

Pin description

SYMBOL	PIN		DESCRIPTION
	DIP40	QFP44	
P1.0/INT2/T2 P1.1/INT3/T2EX P1.2/INT4 P1.3/INT5 P1.4/INT6 P1.5/INT7 P1.6/INT8/SCL P1.7/INT9/SDA	1 2 3 4 5 6 7 8	40 41 42 43 44 1 2 3	• **Port 1:** 8-bit bidirectional I/O port (P1.0 to P1.7). Port pins that have logic 1s written to them are pulled HIGH by internal pull-ups, and in this state can be used as inputs (note that P1.6 and P1.7 are open-drain only). As inputs, Port 1 pins that are externally pulled LOW will source current (I_{IL}) due to the internal pull-ups. Port 1 output buffers can sink/source 4 LS TTL loads. • **Alternative functions:** – INT2 to INT9 are external interrupt inputs – T2 and T2EX are the Timer/event counter 2 inputs – SCL and SDA are the I²C-bus clock and data lines.
RST	9	4	**Reset:** A HIGH level on this pin for two machine cycles while the oscillator is running, resets the device.
n.c.	–	6	Not connected.
P3.0/RXD/data P3.1/TXD/clock P3.2/$\overline{\text{INT0}}$ P3.3/$\overline{\text{INT1}}$ P3.4/T0 P3.5/T1 P3.6/$\overline{\text{WR}}$ P3.7/$\overline{\text{RD}}$	10 11 12 13 14 15 16 17	5 7 8 9 10 11 12 13	• **Port 3:** 8-bit bidirectional I/O port (P3.0 to P3.7). Same characteristics as Port 1. • **Alternative functions:** – RXD/data is the UART serial data input (asynchronous) or data I/O (synchronous) – TXD/clock is the UART serial data output (asynchronous) or clock output (synchronous) – $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ are external interrupt lines – T0 and T1 are external inputs for Timer 0 and Timer 1 respectively – $\overline{\text{WR}}$ is the external memory write strobe and $\overline{\text{RD}}$ is the external memory read strobe.
XTAL2	18	14	**Crystal Output:** Output of the inverting amplifier that forms the oscillator. Left open-circuit when an external oscillator clock is used.
XTAL1	19	15	**Crystal Input:** Input to the inverting amplifier that forms the oscillator, also the input for an externally generated clock source.
V_{SS}	20	16	**Ground:** Circuit ground potential.
TEST/V_{SS}	–	17	**Test Input:** Must be connected to V_{SS} or left open.
P2.0/A8 P2.1/A9 P2.2/A10 P2.3/A11 P2.4/A12 P2.5/A13 P2.6/A14 P2.7/A15	21 22 23 24 25 26 27 28	18 19 20 21 22 23 24 25	• **Port 2:** 8-bit bidirectional I/O port (P2.0 to P2.7). Same characteristics as Port 1. • **High-order addressing:** A8 to A15 make up the high-order address byte during accesses to external memory that use 16-bit addresses (MOVX@DPTR). In this application the pins use the strong internal pull-ups when emitting logic 1's. During accesses to external memory that use 8-bit addresses (MOVX@Ri), the pins emit the contents of the P2 Special Function Register.

SYMBOL	PIN		DESCRIPTION
	DIP40	QFP44	
$\overline{PSEN}$	29	26	**Program Store Enable:** Read strobe to external Program Memory. When executing code out of external Program Memory, $\overline{PSEN}$ is activated twice each machine cycle. However, during each access to external Data Memory two $\overline{PSEN}$ activations are skipped.
ALE	30	27	**Address Latch Enable:** Latches the low byte of the address during accesses to external memory. It is activated every six oscillator periods and may be used for external timing or clocking purposes.
n.c.	–	28	Not connected.
$\overline{EA}$	31	29	**External Access:** When $\overline{EA}$ is held HIGH, the CPU executes out of the internal Program Memory (unless the Program Counter exceeds 3FFFH). When $\overline{EA}$ is held LOW, the CPU executes out of external Program Memory regardless of the value of the program counter.
P0.7/AD7	32	30	• **Port 0:** 8-bit open-drain bidirectional I/O port (P0.7 to P0.0). As an open-drain output port it can sink/source 8 LS TTL loads. Port 0 pins that have logic 1s written to them float, and in this state will function as high-impedance inputs. • **Low-order addressing:** AD7 to AD0 provide the multiplexed low-order address and data bus during accesses to external memory. In this application the pins use the strong internal pull-ups when emitting logic 1s.
P0.6/AD6	33	31	
P0.5/AD5	34	32	
P0.4/AD4	35	33	
P0.3/AD3	36	34	
P0.2/AD2	37	35	
P0.1/AD1	38	36	
P0.0/AD0	39	37	
V_{DD}	40	38	**Power supply.**
n.c.	–	39	Not connected.

UHF amplifier modules BGY120A; BGY120B

FEATURES

- Single 3.5 V nominal supply voltage
- 1 W output power
- Easy control of output power by DC voltage
- Very high efficiency (typ. 60%)
- Silicon bipolar technology
- Standby current less than 10 μA.

APPLICATIONS

- Hand-held transmitting equipment operating in the 824 to 849 MHz and 872 to 905 MHz frequency ranges.

DESCRIPTION

The BGY120A and BGY120B are two-stage UHF amplifier modules in a SOT482B package with plastic cover. Each module consists of two NPN silicon planar transistor dies mounted together with a matching and bias circuit components on a metallized ceramic substrate.
These modules produce an output power of 1 W into a load of 50 Ω with an RF drive power of 5 mW.

PINNING - SOT482B

PIN	DESCRIPTION
1	RF input
2	V_C
3	V_S
4	RF output
5	flange connected to ground

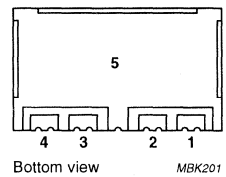


Fig.1 Simplified outline

QUICK REFERENCE DATA

RF performance at T_{mb} = 25 °C.

TYPE	MODE OF OPERATION	f (MHz)	V_S (V)	P_L (W)	G_p (dB)	η (%)	Z_S; Z_L (Ω)
BGY120A	CW	824 to 849	3.5	1	≥23	typ. 60	50
BGY120B	CW	872 to 905	3.5	1	≥23	typ. 60	50

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_S	DC supply voltage	–	5	V
V_C	DC control voltage	–	2.9	V
P_D	input drive power	–	10	mW
P_L	load power	–	1.4	W
T_{stg}	storage temperature	–40	+100	°C
T_{mb}	operating mounting-base temperature	–30	+100	°C

CHARACTERISTICS

$Z_S = Z_L = 50\ \Omega$; $P_D = 5$ mW; $V_S = 3.5$ V; $V_C \leq 2.5$ V; $T_{mb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f	frequency range					
	BGY120A		824	–	849	MHz
	BGY120B		872	–	905	MHz
I_Q	total leakage current	$V_C = 0.3$ V; $P_D < -60$ dBm	–	–	10	μA
I_C	control current		–	–	10	mA
P_L	load power	$V_C = 2.5$ V	1	–	–	W
		$V_S = 3.2$ V; $T_{mb} = 85$ °C	0.71	–	–	W
G_p	power gain	adjust V_C for $P_L = 1$ W	23	–	–	dB
η	efficiency	$V_S = 3.2$ V; adjust V_C for $P_L = 0.9$ W	55	60	–	%
H_2	second harmonic	adjust V_C for $P_L = 0.9$ W	–	–	–35	dBc
H_3	third harmonic	adjust V_C for $P_L = 0.9$ W	–	–	–40	dBc
$VSWR_{in}$	input VSWR	adjust V_C for $P_L = 0.9$ W	–	–	2 : 1	
		$V_C \leq 0.5$ V	–	–	4 : 1	
	stability	$P_L \leq 1.4$ W; $V_C = 0$ to 2.9 V; $V_S = 2.8$ to 5 V; $P_D = 4$ to 10 dBm; VSWR ≤ 6 : 1 through all phases	–	–	–60	dBc
	isolation	$V_C \leq 0.5$ V	–	-40	–	dBm
P_n	noise power	adjust V_C for $P_L = 1$ W; bandwidth = 30 kHz; $f_n = f_o + 45$ MHz	–	–	–90	dBm
d_{im}	reverse intermodulation	$P_{Tx} = 0.9$ W; $f_{int} = f_{Tx} - 45$ MHz; $P_{int} = P_{Tx} - 30$ dB; note 1	–	–	–8	dB
	ruggedness	$V_S = 5$ V; adjust V_C for $P_L = 1.4$ W; VSWR ≤ 10 : 1 through all phases	no degradation			

Note

1. With respect to P_{int}.

UHF amplifier modules BGY122A; BGY122B

FEATURES

- Single 4.8 V nominal supply voltage
- 1.2 W output power
- Easy control of output power by DC voltage
- Very high efficiency (typ. 55%)
- Silicon bipolar technology
- Standby current less than 100 μA.

APPLICATIONS

- Hand-held transmitting equipment operating in the 824 to 849 MHz and 872 to 905 MHz frequency ranges.

DESCRIPTION

The BGY122A and BGY122B are three-stage UHF amplifier modules in a SOT388B package. Each module consists of three NPN silicon planar transistor dies mounted together with matching and bias circuit components on a metallized ceramic substrate.
The modules produce an output power of 1.2 W into a load of 50 Ω with an RF drive power of 2 mW.

PINNING - SOT388B

PIN	DESCRIPTION
1	RF input
2	V_C
3	V_S
4	RF output
Flange	ground

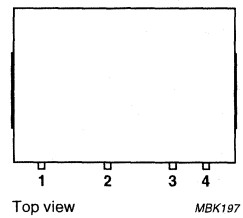


Fig.1 Simplified outline.

QUICK REFERENCE DATA

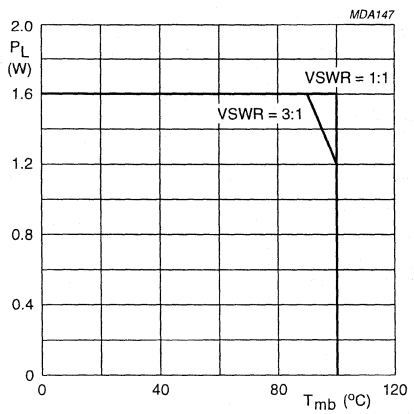
RF performance at T_{mb} = 25 °C.

TYPE	MODE OF OPERATION	f (MHz)	V_S (V)	P_L (W)	G_p (dB)	η (%)	Z_S; Z_L (Ω)
BGY122A	CW	824 to 849	4.8	1.2	≥27.8	typ. 55	50
BGY122B	CW	872 to 905	4.8	1.2	≥27.8	typ. 55	50

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_S	DC supply voltage	$V_C = 0$; $P_D = 0$	–	10	V
V_C	DC control voltage		–	3.5	V
P_D	input drive power		–	5	mW
P_L	load power		–	1.6	W
T_{stg}	storage temperature		–40	+100	°C
T_{mb}	operating mounting base temperature		–30	+100	°C



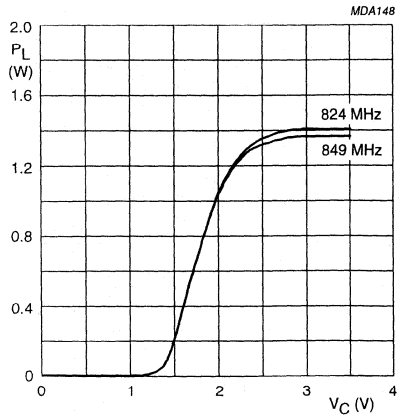
V_S = 6.5 V.

Fig.2 Load power derating curve.

CHARACTERISTICS

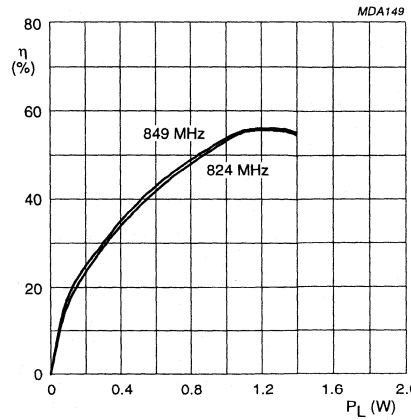
$Z_S = Z_L = 50\ \Omega$; $P_D = 2$ mW; $V_S = 4.8$ V; $V_C \leq 3$ V; $T_{mb} = 25$ °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f	frequency					
	BGY122A		824	–	849	MHz
	BGY122B		872	–	905	MHz
I_Q	total quiescent current	$V_C = 0$; $P_D < -60$ dBm	–	–	100	μA
I_C	control current	adjust V_C for $P_L = 1.2$ W	–	–	500	μA
P_L	load power	$V_C = 3$ V	1.2	–	–	W
G_p	power gain	adjust V_C for $P_L = 1.2$ W	27.8	–	–	dB
η	efficiency	adjust V_C for $P_L = 1.2$ W	50	55	–	%
H_2	second harmonic	adjust V_C for $P_L = 1.2$ W	–	–	–36	dBc
H_3	third harmonic	adjust V_C for $P_L = 1.2$ W	–	–	–36	dBc
$VSWR_{in}$	input VSWR	adjust V_C for $P_L = 1.2$ W	–	–	3 : 1	
	stability	$P_D = 0$ to +6 dBm; $V_S = 4$ to 6.5 V; $V_C = 0$ to 3 V; $P_L \leq 1.2$ W; VSWR ≤ 6 : 1 through all phases	–	–	–60	dBc
	isolation	$V_C = 0$	–	–40	–	dBm
P_n	noise power	adjust V_C for $P_L = 1.2$ W; bandwidth = 30 kHz; $f_n = f_o + 45$ MHz	–	–	–90	dBm
	ruggedness	$V_S = 6.5$ V; adjust V_C for $P_L = 1.4$ W; VSWR ≤ 10 : 1 through all phases	no degradation			



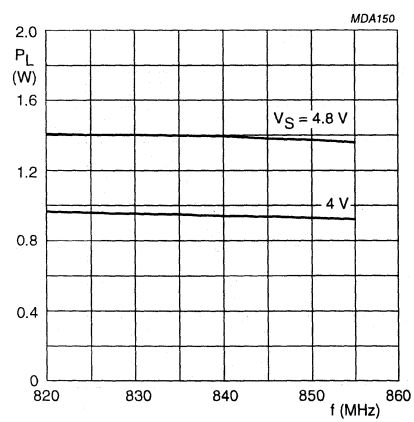
$Z_S = Z_L = 50\ \Omega$; $P_D = 2$ mW; $V_S = 4.8$ V; $T_{mb} = 25$ °C.

Fig.3 Load power as a function of control voltage; BGY122A; typical values.



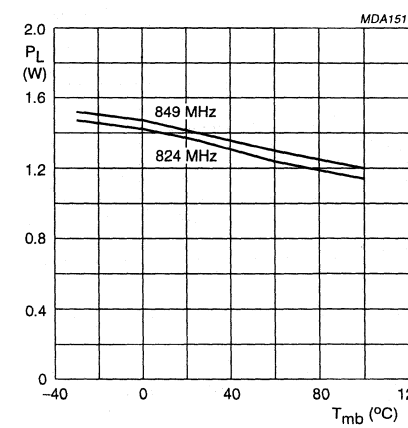
$Z_S = Z_L = 50\ \Omega$; $P_D = 2$ mW; $V_S = 4.8$ V; $T_{mb} = 25$ °C.

Fig.4 Efficiency as a function of load power; BGY122A; typical values.



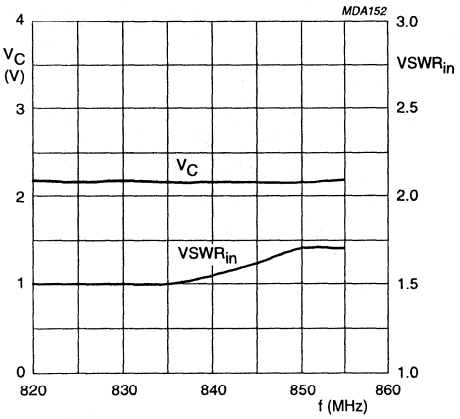
$Z_S = Z_L = 50\ \Omega$; $P_D = 2$ mW; $V_C = 3$ V; $T_{mb} = 25$ °C.

Fig.5 Load power as a function of frequency; BGY122A; typical values.



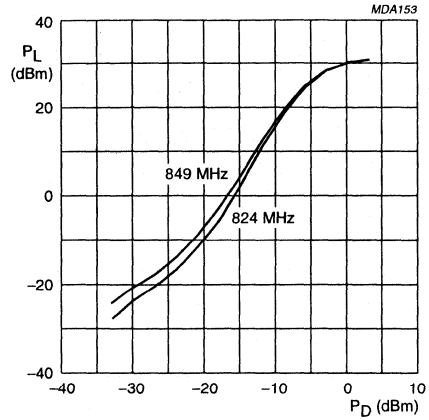
$Z_S = Z_L = 50\ \Omega$; $P_D = 2$ mW; $V_S = 4.8$ V; $V_C = 3$ V.

Fig.6 Load power as a function of mounting base temperature; BGY122A; typical values.



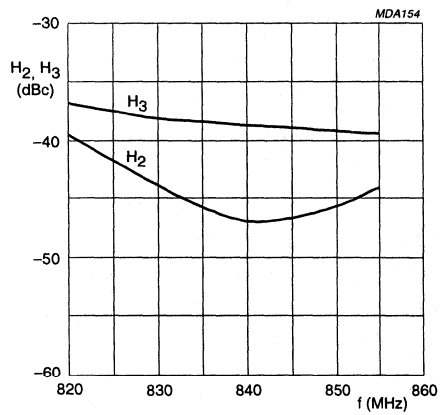
$Z_S = Z_L = 50\ \Omega$; $P_D = 2$ mW; $V_S = 4.8$ V; $P_L = 1.2$ W; $T_{mb} = 25$ °C.

Fig.7 Control voltage and input VSWR as functions of frequency; BGY122A; typical values.



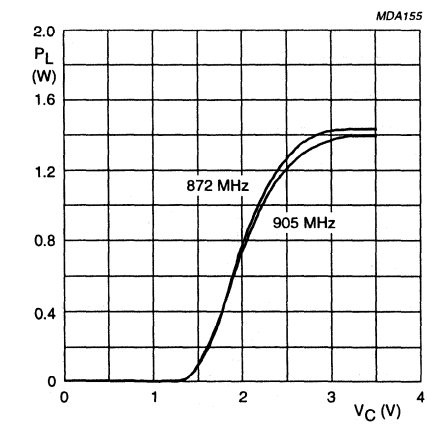
$Z_S = Z_L = 50\ \Omega$; $V_S = 4.8$ V; $V_C = 3$ V; $T_{mb} = 25$ °C.

Fig.8 Load power as a function of drive power; BGY122A; typical values.



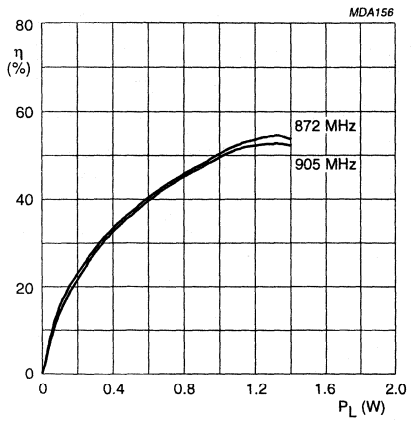
$Z_S = Z_L = 50\ \Omega$; $P_D = 2$ mW; $V_S = 4.8$ V; $P_L = 1.2$ W; $T_{mb} = 25$ °C.

Fig.9 Harmonics as a function of frequency; BGY122A; typical values.



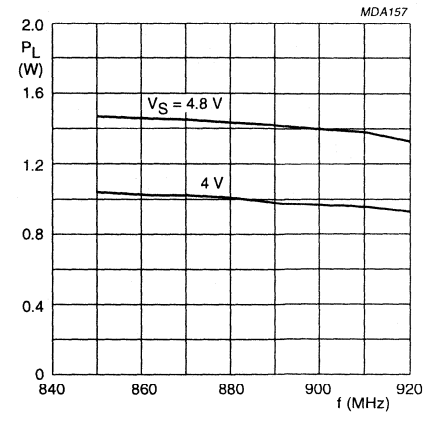
$Z_S = Z_L = 50\ \Omega$; $P_D = 2$ mW; $V_S = 4.8$ V; $T_{mb} = 25$ °C.

Fig.10 Load power as a function of control voltage; BGY122B; typical values.



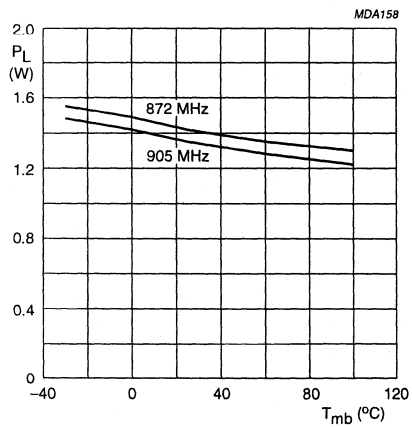
$Z_S = Z_L = 50\ \Omega$; P_D =2 mW; V_S = 4.8 V; T_{mb} = 25 °C.

Fig.11 Efficiency as a function of load power; BGY122B; typical values.



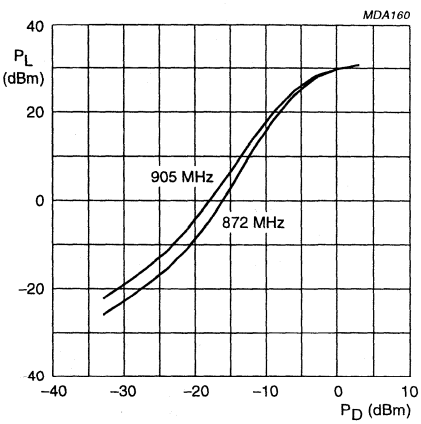
$Z_S = Z_L = 50\ \Omega$; P_D = 2 mW; V_C = 3 V; T_{mb} = 25 °C.

Fig.12 Load power as a function of frequency; BGY122B; typical values.



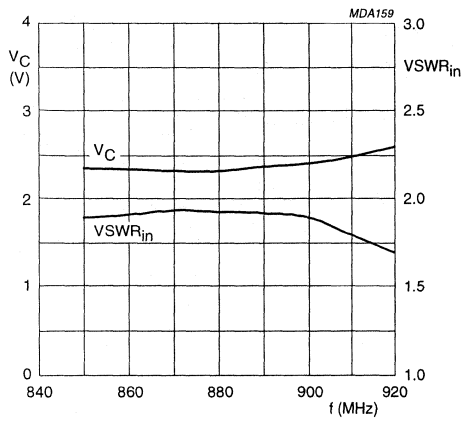
$Z_S = Z_L = 50\ \Omega$; P_D = 2 mW; V_S = 4.8 V; V_C = 3 V.

Fig.13 Load power as a function of mounting base temperature; BGY122B; typical values.



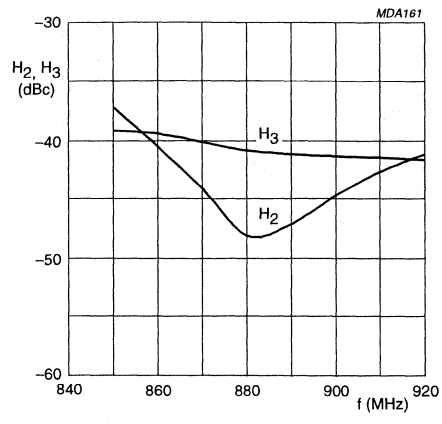
$Z_S = Z_L = 50\ \Omega$; V_S = 4.8 V; V_C = 3 V; T_{mb} = 25 °C.

Fig.14 Load power as a function of drive power; BGY122B; typical values.



$Z_S = Z_L = 50\ \Omega$; $P_D = 2$ mW; $V_S = 4.8$ V; $P_L = 1.2$ W; $T_{mb} = 25$ °C.

Fig.15 Control voltage and input VSWR as functions of frequency; BGY122B; typical values.



$Z_S = Z_L = 50\ \Omega$; $P_D = 2$ mW; $V_S = 4.8$ V; $P_L = 1.2$ W; $T_{mb} = 25$ °C.

Fig.16 Harmonics as a function of frequency; BGY122B; typical values.

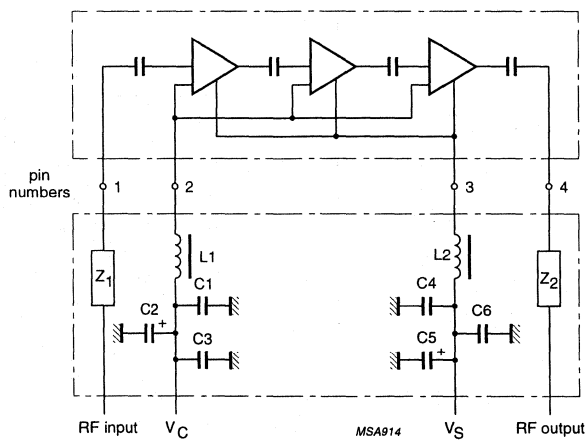
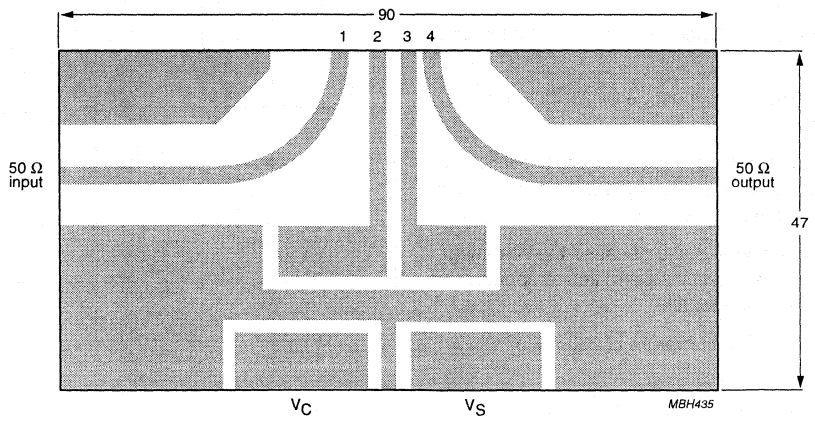


Fig.17 Test circuit.



Dimensions in mm.

Fig.18 Printed-circuit board test-fixture.

List of components (See Figs 17 and 18)

COMPONENT	DESCRIPTION	VALUE	CATALOGUE NO.
C1, C4	multilayer ceramic chip capacitor	100 nF	2222 852 47104
C2, C5	tantalum capacitor	2.2 μF; 35 V	–
C3, C6	multilayer ceramic chip capacitor	33 pF	2222 851 13339
L1, L2	Grade 4S2 Ferroxcube chip bead	–	4330 030 36300
Z_1, Z_2	stripline; note 1	50 Ω	–

Note

1. The striplines are on a double copper-clad printed-circuit board with PTFE fibreglass dielectric ($\varepsilon_r = 2.2$); thickness $^1/_{32}$ inch.

SOLDERING

The indicated temperatures are those at the solder interfaces.

Advised solder types are types with a liquidus less than or equal to 210 °C.

Solder dots or solder prints must be large enough to wet the contact areas.

Soldering can be carried out using a conveyor oven, a hot air oven, an infrared oven or a combination of these ovens. A double reflow process is permitted.

Hand soldering must be avoided because the soldering iron tip can exceed the maximum permitted temperature of 250 °C and damage the module.

The maximum allowed temperature is 250 °C for a maximum of 5 seconds.

The maximum ramp-up is 10 °C per second.

The maximum cool-down is 5 °C per second.

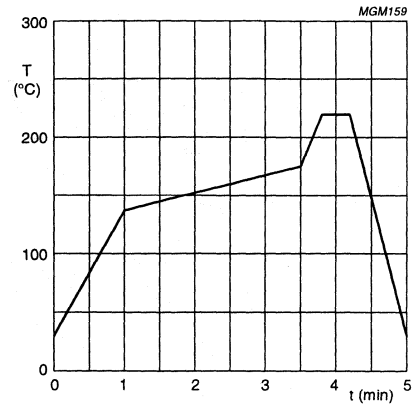


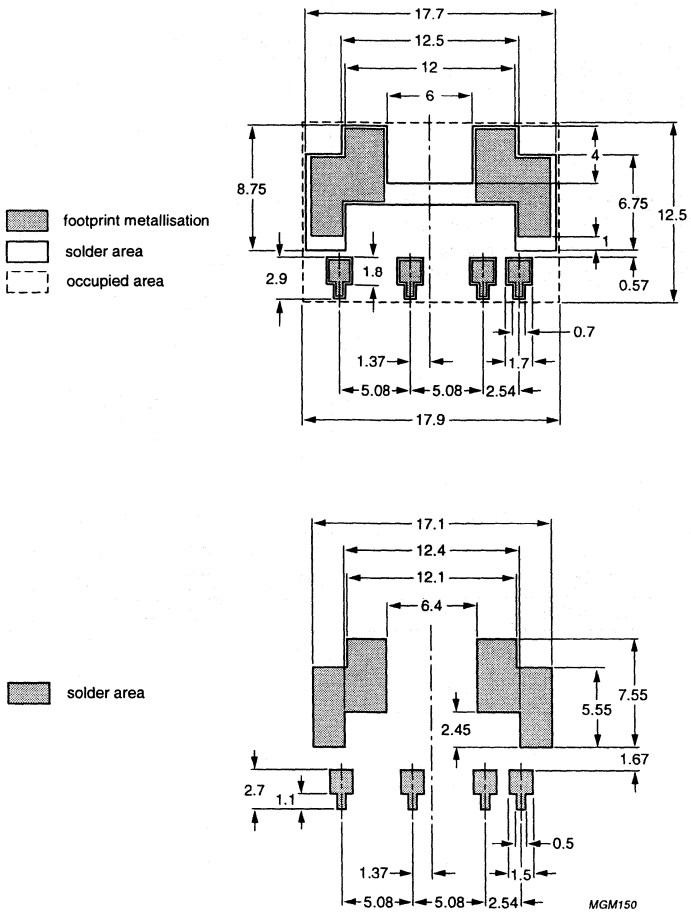
Fig.19 Recommended reflow temperature profile.

Cleaning

The following fluids may be used for cleaning:

- Alcohol
- Bio-Act (Terpene Hydrocarbon)
- Triclean B/S
- Acetone.

Ultrasonic cleaning should not be used since this can cause serious damage to the product.



Dimensions in mm.

Fig.20 Footprint SOT388B.

UHF amplifier module BGY204

FEATURES

- 4.8 V nominal supply voltage
- 3.2 W output power
- Easy control of output power by DC voltage.

APPLICATIONS

- Digital cellular radio systems with Time Division Multiple Access (TDMA) operation (GSM systems) in the 880 to 915 MHz frequency range.

DESCRIPTION

The BGY204 is a four-stage UHF amplifier module in a SOT321B package. The module consists of four NPN silicon planar transistor dies mounted together with matching and bias circuit components on a metallized ceramic substrate.

PINNING - SOT321B

PIN	DESCRIPTION
1	RF input
2	V_C
3	V_S
4	RF output
Flange	ground

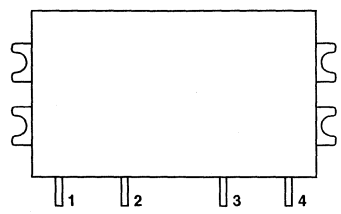


Fig.1 Simplified outline.

QUICK REFERENCE DATA

RF performance at T_{mb} = 25 °C.

MODE OF OPERATION	f (MHz)	V_S (V)	V_C (V)	P_L (W)	G_p (dB)	η (%)	Z_S; Z_L (Ω)
Pulsed; δ = 1 : 8	880 to 915	4.8	≤3.5	3.2	≥35	typ. 45	50

LIMITING VALUES

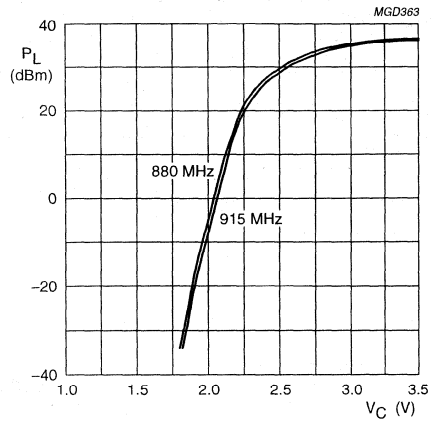
In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_S	DC supply voltage	$P_L = 0$	–	8	V
V_C	DC control voltage		–	4.5	V
P_D	input drive power		–	2	mW
P_L	load power	$V_S \leq 6.5$ V; $Z_L = 50\ \Omega$	–	4	W
T_{stg}	storage temperature		–40	+100	°C
T_{mb}	operating mounting base temperature		–30	+100	°C

CHARACTERISTICS

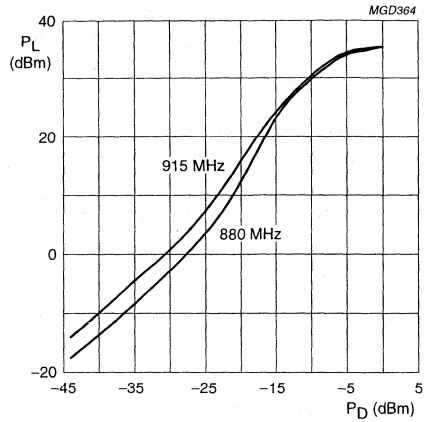
$Z_S = Z_L = 50\ \Omega$; $P_D = 1$ mW; $V_S = 4.8$ V; $V_C \leq 3.5$ V; f = 880 to 915 MHz; $T_{mb} = 25$ °C; $\delta = 1 : 8$; $t_p = 575\ \mu s$; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_Q	leakage current	$V_C = 0.5$ V	–	–	0.2	mA
I_C	control current	adjust V_C for $P_L = 3.2$ W	–	–	0.5	mA
P_L	load power		3.2	–	–	W
G_p	power gain	adjust V_C for $P_L = 3.2$ W	35	–	–	dB
η	efficiency	adjust V_C for $P_L = 3.2$ W	40	45	–	%
H_2	second harmonic	adjust V_C for $P_L = 3.2$ W	–	–	–40	dBc
H_3	third harmonic	adjust V_C for $P_L = 3.2$ W	–	–	–40	dBc
$VSWR_{in}$	input VSWR	adjust V_C for $P_L = 3.2$ W	–	–	2.5 : 1	
	stability	$P_D = 0.5$ to 2 mW; $V_S = 4$ to 6.5 V; $V_C = 0$ to 3.5 V; $P_L \leq 3.2$ W; VSWR ≤ 6 : 1 through all phases;	–	–	–60	dBc
	isolation	$V_C = 0.5$ V	–	–	–36	dBm
	control bandwidth		1	–	–	MHz
P_n	noise power	$P_L = 3.2$ W; bandwidth = 30 kHz; 20 MHz above transmitter band	–	–	–85	dBm
	ruggedness	$V_S = 6.5$ V; adjust V_C for $P_L = 3.2$ W; VSWR ≤ 10 : 1 through all phases	no degradation			



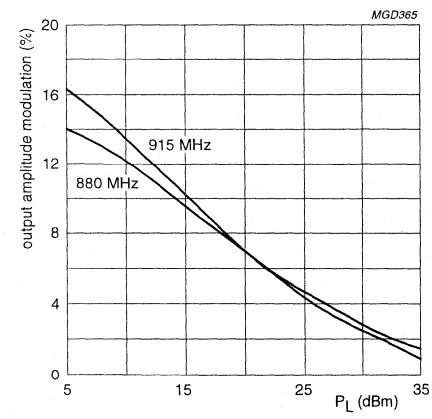
$Z_S = Z_L = 50\ \Omega$; $P_D = 0$ dBm; $V_S = 4.8$ V; $T_{mb} = 25$ °C.

Fig.2 Load power as a function of control voltage; typical values.



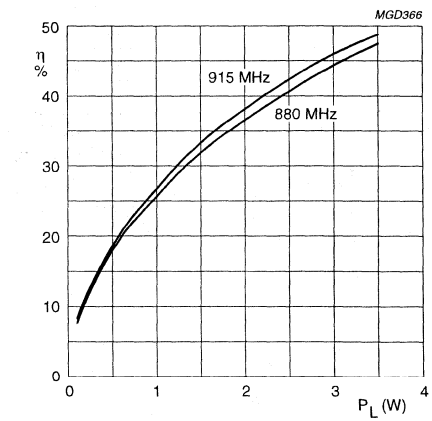
$Z_S = Z_L = 50\ \Omega$; $V_S = 4.8$ V; adjust V_C for $P_L = 3.2$ W; $T_{mb} = 25$ °C.

Fig.3 Load power as a function of drive power; typical values.



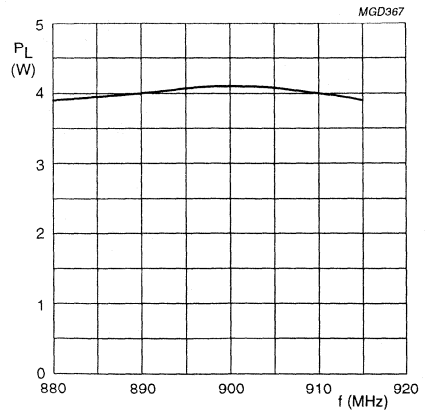
$Z_S = Z_L = 50\ \Omega$; $V_S = 4.8$ V; $T_{mb} = 25$ °C;
input amplitude modulation = 3%.

Fig.4 Output amplitude modulation as a function of load power; typical values.



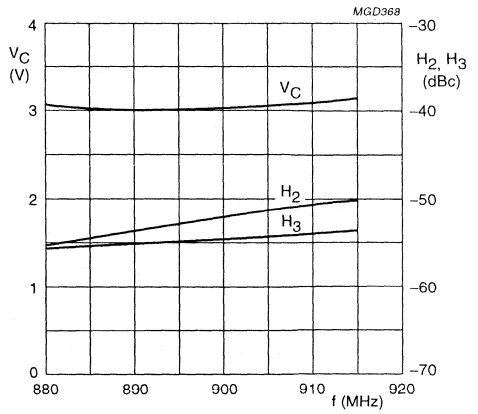
$Z_S = Z_L = 50\ \Omega$; $V_S = 4.8$ V; $T_{mb} = 25$ °C.

Fig.5 Efficiency as a function of load power; typical values.



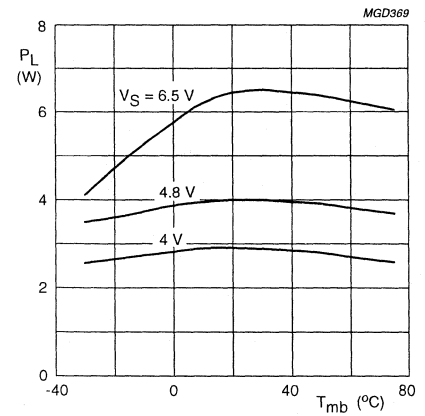
$Z_S = Z_L = 50\ \Omega$; $P_D = 0$ dBm; $V_S = 4.8$ V; $V_C = 3.5$ V; $T_{mb} = 25$ °C.

Fig.6 Load power as a function of frequency; typical values.



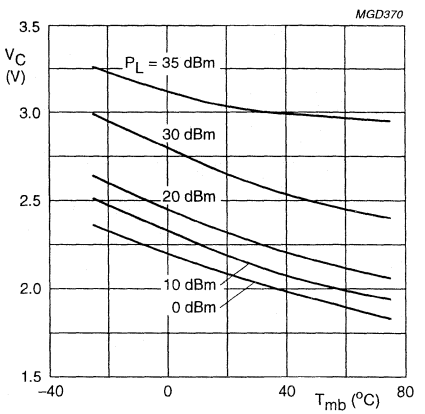
$Z_S = Z_L = 50\ \Omega$; $P_D = 0$ dBm; $V_S = 4.8$ V; $P_L = 3.2$ W; $T_{mb} = 25$ °C.

Fig.7 Control voltage and harmonics as functions of frequency; typical values.



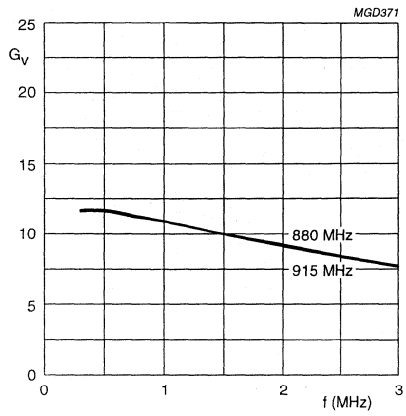
$Z_S = Z_L = 50\ \Omega$; $P_D = 0$ dBm; $V_C = 3.5$ V; f = 900 MHz.

Fig.8 Load power as a function of the mounting base temperature; typical values.



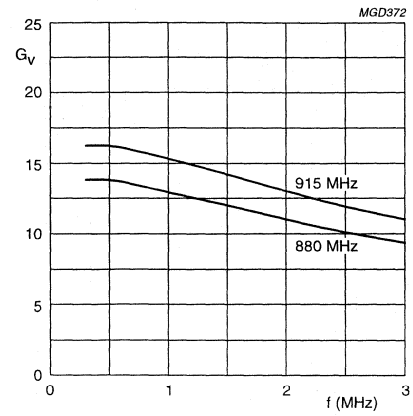
$Z_S = Z_L = 50\ \Omega$; $P_D = 0$ dBm; $V_S = 4.8$ V; f = 900 MHz.

Fig.9 Control voltage as a function of mounting base temperature; typical values.



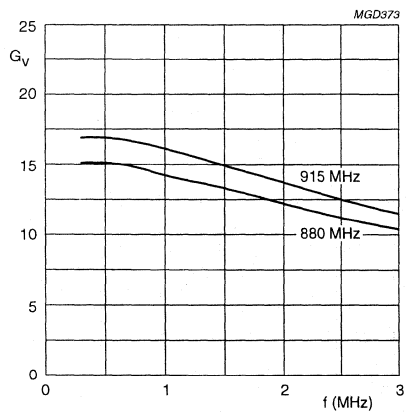
P_L = 30 dBm.
$Z_S = Z_L = 50\ \Omega$; P_D = 0 dBm; V_S = 4.8 V; T_{mb} = 25 °C.

Fig.10 Control loop voltage gain as a function of the frequency on the control pin; typical values.



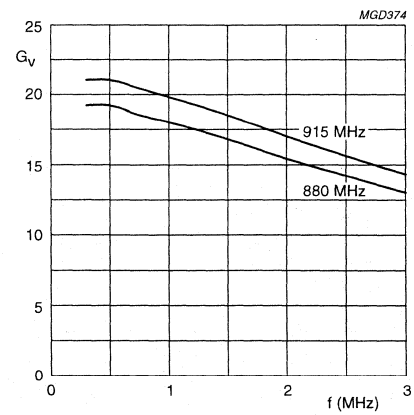
P_L = 25 dBm.
$Z_S = Z_L = 50\ \Omega$; P_D = 0 dBm; V_S = 4.8 V; T_{mb} = 25 °C.

Fig.11 Control loop voltage gain as a function of the frequency on the control pin; typical values.



P_L = 20 dBm.
$Z_S = Z_L = 50\ \Omega$; P_D = 0 dBm; V_S = 4.8 V; T_{mb} = 25 °C.

Fig.12 Control loop voltage gain as a function of frequency on the control pin; typical values.



P_L = 15 dBm.
$Z_S = Z_L = 50\ \Omega$; P_D = 0 dBm; V_S = 4.8 V; T_{mb} = 25 °C.

Fig.13 Control loop voltage gain as a function of frequency on the control pin; typical values.

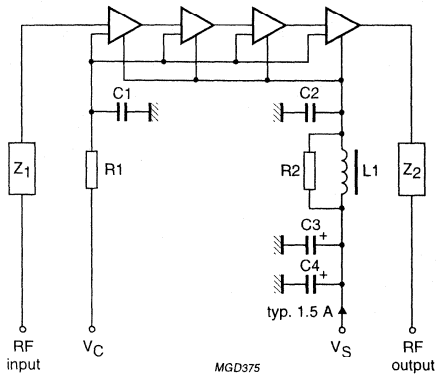
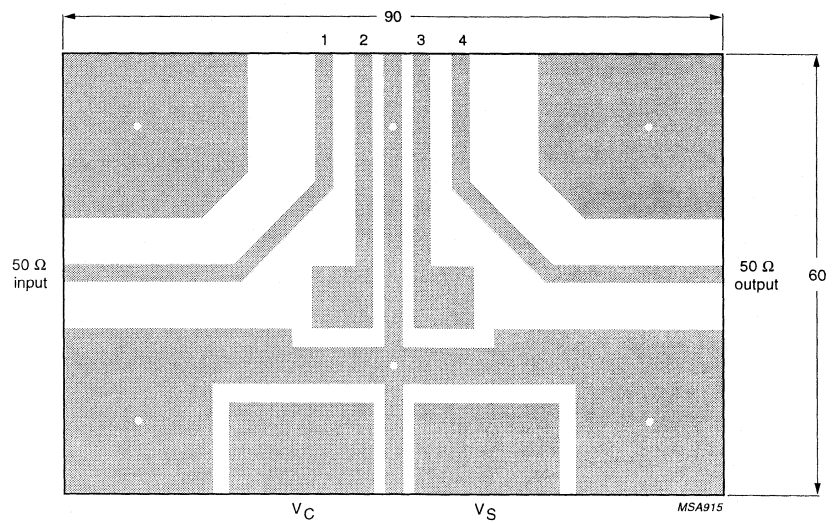


Fig.14 Test circuit.



Dimensions in mm.

Fig.15 Printed-circuit board layout.

List of components (See Fig.14)

COMPONENT	DESCRIPTION	VALUE	CATALOGUE NO.
C1, C2	multilayer ceramic chip capacitor	680 pF	–
C3	tantalum capacitor	2.2 μF; 35 V	–
C4	electrolytic capacitor	47 μF; 40 V	–
L1	Grade 3B Ferroxcube bead		4330 030 36300
Z_1, Z_2	stripline; note 1	50 Ω	–
R1	metal film resistor	100 Ω; 0.4 W	–
R2	metal film resistor	5 Ω; 0.4 W	–

Note

1. The striplines are on a double copper-clad printed-circuit board with PTFE fibreglass dielectric ($\varepsilon_r = 2.2$); thickness $^1/_{16}$ inch.

SOLDERING

The indicated temperatures are those at the solder interfaces.

Advised solder types are types with a liquidus less than or equal to 210 °C.

Solder dots or solder prints must be large enough to wet the contact areas.

Footprints for soldering should cover the module contact area +0.1 mm on all sides.

Soldering can be carried out using a conveyor oven, a hot air oven, an infrared oven or a combination of these ovens.

Hand soldering must be avoided because the soldering iron tip can exceed the maximum permitted temperature of 250 °C and damage the module.

The maximum temperature profile and soldering time is indicated as follows (see Fig.16):

t = 350 s at 100 °C

t = 300 s at 125 °C

t = 200 s at 150 °C

t = 100 s at 175 °C

t = 50 s at 200 °C

t = 5 s at 250 °C (maximum temperature).

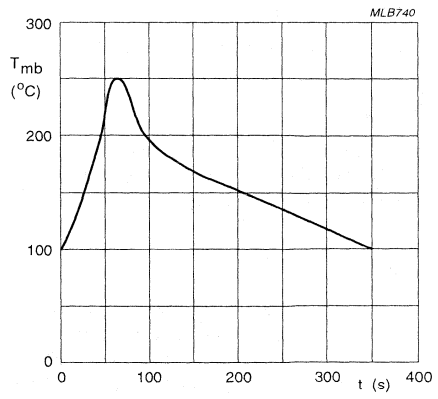


Fig.16 Maximum allowable temperature profile.

Cleaning

The following fluids may be used for cleaning:

- Alcohol
- Bio-Act (Terpene Hydrocarbon)
- Triclean B/S
- Acetone.

Ultrasonic cleaning should not be used since this can cause serious damage to the product.

UHF amplifier module BGY205

FEATURES

- 6 V nominal supply voltage
- 3.5 W pulsed output power
- Easy control of output power by DC voltage.

APPLICATIONS

- Digital cellular radio systems with Time Division Multiple Access (TDMA) operation (GSM systems) in the 880 to 915 MHz frequency range.

DESCRIPTION

The BGY205 is a four-stage UHF amplifier module in a SOT321B package. The module consists of four NPN silicon planar transistor dies mounted together with matching and bias circuit components on a metallized ceramic substrate.

PINNING - SOT321B

PIN	DESCRIPTION
1	RF input
2	V_C
3	V_S
4	RF output
Flange	ground

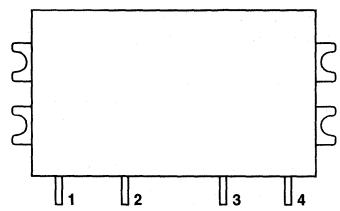


Fig.1 Simplified outline.

QUICK REFERENCE DATA

RF performance at T_{mb} = 25 °C.

MODE OF OPERATION	f (MHz)	V_S (V)	V_C (V)	P_L (W)	G_p (dB)	η (%)	Z_S; Z_L (Ω)
Pulsed; δ = 1 : 8	880 to 915	6	≤4	3.5	≥32.5	≥40	50

LIMITING VALUES

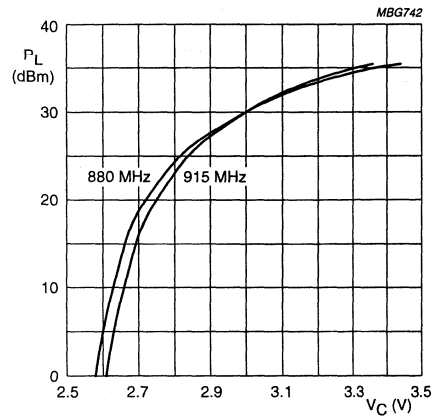
In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_S	DC supply voltage	–	8.5	V
V_C	DC control voltage	–	4.5	V
P_D	input drive power	–	7	mW
P_L	load power	–	4	W
T_{stg}	storage temperature	–40	+100	°C
T_{mb}	operating mounting base temperature	–30	+100	°C

CHARACTERISTICS

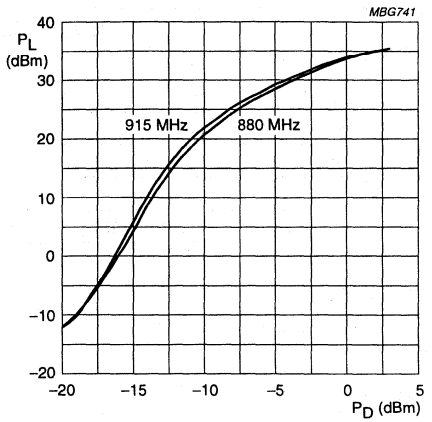
$Z_S = Z_L = 50\ \Omega$; $P_D = 3$ dBm; $V_S = 6$ V; $V_C \leq 4$ V; f = 880 to 915 MHz; $T_{mb} = 25$ °C; $\delta = 1 : 8$; $t_p = 575\ \mu s$; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_Q	leakage current	$V_C = 0.5$ V	–	–	100	μA
I_C	control current	adjust V_C for $P_L = 3.5$ W	–	–	500	μA
P_L	load power	$V_C = 4$ V	3.5	–	–	W
G_p	power gain	adjust V_C for $P_L = 3.5$ W	32.5	–	–	dB
η	efficiency	adjust V_C for $P_L = 3.5$ W	40	45	–	%
H_2	second harmonic	adjust V_C for $P_L = 3.5$ W	–	–	–40	dBc
H_3	third harmonic	adjust V_C for $P_L = 3.5$ W	–	–	–40	dBc
$VSWR_{in}$	input VSWR	adjust V_C for $P_L = 3.5$ W	–	–	2 : 1	
	stability	$P_D = 0$ to 6 dBm; $V_S = 5$ to 8.5 V; $V_C = 0$ to 4 V; $P_L \leq 3.5$ W; VSWR ≤ 6 : 1 through all phases	–	–	–60	dBc
	isolation	$V_C = 0.5$ V	–	–	–36	dBm
	control bandwidth	R1 = 0; C1 = 0; see Fig.16	1	–	–	MHz
	AM-AM conversion	P_D with 3% AM; f = 100 kHz; $P_L = 3.5$ mW to 3.5 W	–	–	12	%
P_n	noise power	$P_L = 3.5$ W; bandwidth = 30 kHz; 20 MHz above transmitter band	–	–	–85	dBm
	ruggedness	$V_S = 8.5$ V; adjust V_C for $P_L = 3.5$ W; VSWR ≤ 10 : 1 through all phases	no degradation			



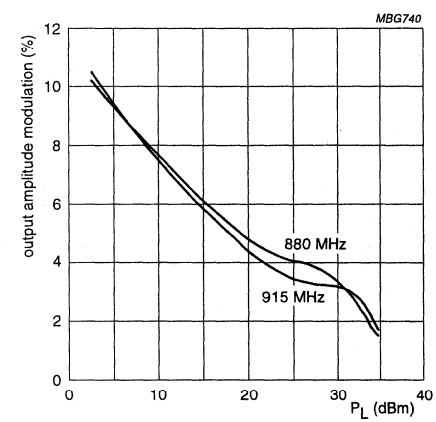
$Z_S = Z_L = 50\ \Omega$; $P_D = 3$ dBm; $V_S = 6$ V;
$T_{mb} = 25$ °C; $\delta = 1 : 8$; $t_p = 575\ \mu s$.

Fig.2 Load power as a function of control voltage; typical values.



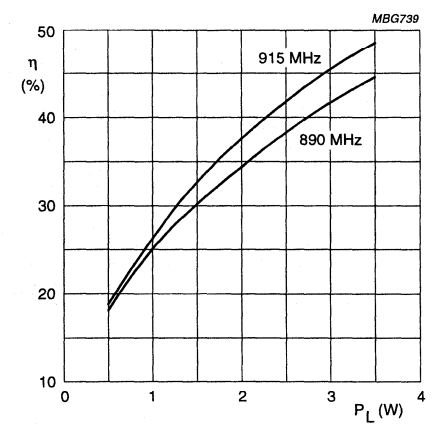
$Z_S = Z_L = 50\ \Omega$; $V_S = 6$ V; $P_L = 3.5$ mW;
$T_{mb} = 25$ °C; $\delta = 1 : 8$; $t_p = 575\ \mu s$.

Fig.3 Load power as a function of drive power; typical values.



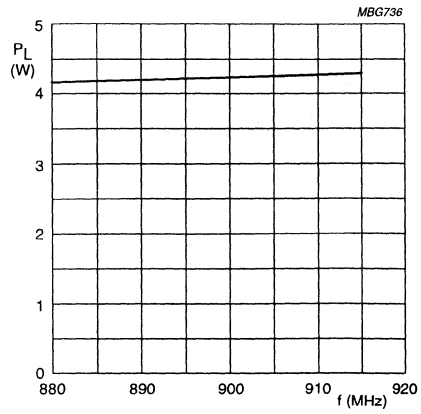
$Z_S = Z_L = 50\ \Omega$; $P_D = 3$ dBm; $V_S = 6$ V; $T_{mb} = 25$ °C;
$\delta = 1 : 8$; $t_p = 575\ \mu s$; input amplitude modulation = 3%.

Fig.4 Output amplitude modulation as a function of load power; typical values.



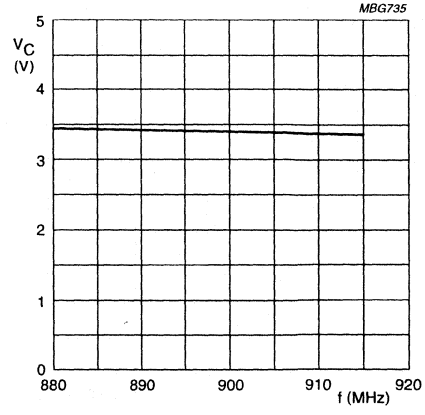
$Z_S = Z_L = 50\ \Omega$; $P_D = 3$ dBm; $V_S = 6$ V;
$T_{mb} = 25$ °C; $\delta = 1 : 8$; $t_p = 575\ \mu s$.

Fig.5 Efficiency as a function of load power; typical values.



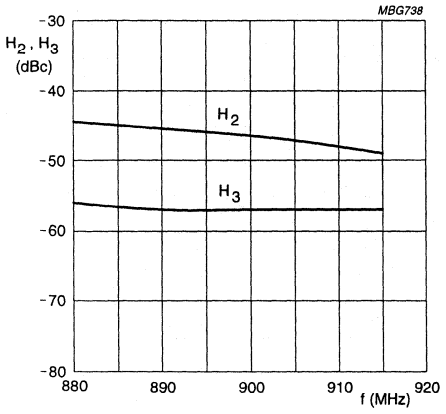
$Z_S = Z_L = 50\ \Omega$; $P_D = 3$ dBm; $V_S = 6$ V;
$V_C = 4$ V; $T_{mb} = 25$ °C; $\delta = 1 : 8$; $t_p = 575$ µs.

Fig.6 Load power as a function of frequency; typical values.



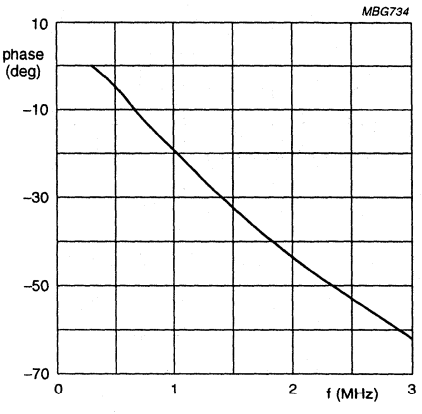
$Z_S = Z_L = 50\ \Omega$; $P_D = 3$ dBm; $V_S = 6$ V;
$P_L = 3.5$ W; $T_{mb} = 25$ °C; $\delta = 1 : 8$; $t_p = 575$ µs.

Fig.7 Control voltage as a function of frequency; typical values.



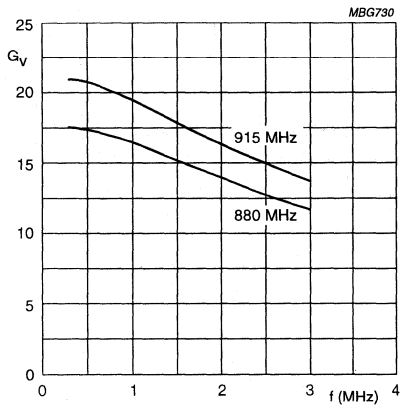
$Z_S = Z_L = 50\ \Omega$; $P_D = 3$ dBm; $V_S = 6$ V;
$P_L = 3.5$ W; $T_{mb} = 25$ °C; $\delta = 1 : 8$; $t_p = 575$ µs.

Fig.8 Harmonics as a function of frequency; typical values.



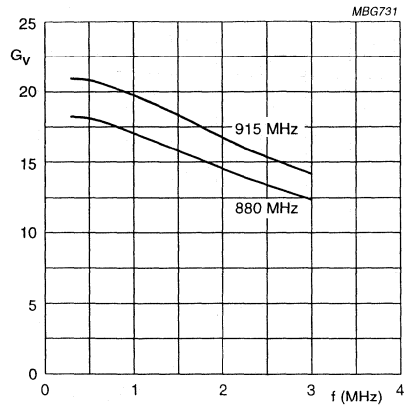
$Z_S = Z_L = 50\ \Omega$; $P_D = 3$ dBm; $V_S = 6$ V; $P_L = 15$ to 35.4 dBm;
f = 880 to 915 MHz; $T_{mb} = 25$ °C; $\delta = 1 : 8$; $t_p = 575$ µs; R1 = 0; C1 = 0.

Fig.9 Control loop phase as a function of frequency on the control pin; typical values.



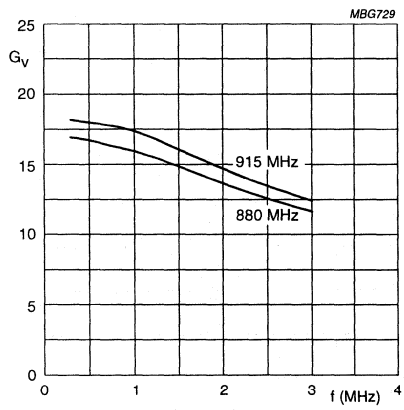
P_L = 30 dBm.
$Z_S = Z_L = 50\ \Omega$; P_D = 3 dBm; V_S = 6 V;
T_{mb} = 25 °C; δ = 1 : 8; t_p = 575 µs; R1 = 0; C1 = 0.

Fig.10 Control loop voltage gain as a function of frequency on the control pin; typical values.



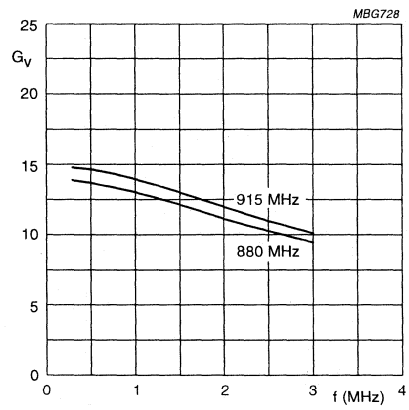
P_L = 25 dBm.
$Z_S = Z_L = 50\ \Omega$; P_D = 3 dBm; V_S = 6 V;
T_{mb} = 25 °C; δ = 1 : 8; t_p = 575 µs; R1 = 0; C1 = 0.

Fig.11 Control loop voltage gain as a function of frequency on the control pin; typical values.



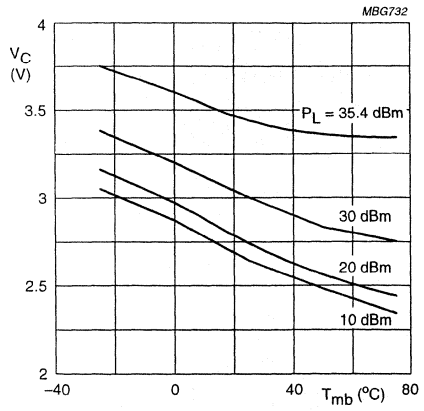
P_L = 20 dBm.
$Z_S = Z_L = 50\ \Omega$; P_D = 3 dBm; V_S = 6 V;
T_{mb} = 25 °C; δ = 1 : 8; t_p = 575 µs; R1 = 0; C1 = 0.

Fig.12 Control loop voltage gain as a function of frequency on the control pin; typical values.



P_L = 15 dBm.
$Z_S = Z_L = 50\ \Omega$; P_D = 3 dBm; V_S = 6 V;
T_{mb} = 25 °C; δ = 1 : 8; t_p = 575 µs; R1 = 0; C1 = 0.

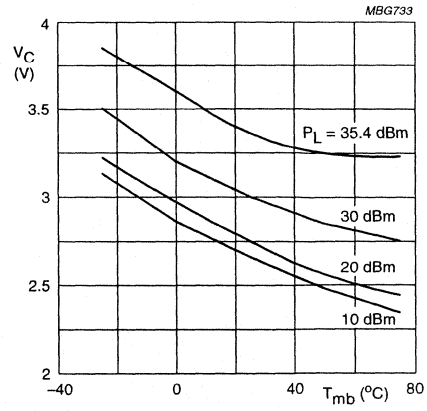
Fig.13 Control loop voltage gain as a function of frequency on the control pin; typical values.



f = 880 MHz.

$Z_S = Z_L = 50\ \Omega$; $P_D = 3$ dBm; $V_S = 6$ V; $\delta = 1 : 8$; $t_p = 575\ \mu s$.

Fig.14 Control voltage as a function of mounting base temperature; typical values.



f = 915 MHz.

$Z_S = Z_L = 50\ \Omega$; $P_D = 3$ dBm; $V_S = 6$ V; $\delta = 1 : 8$; $t_p = 575\ \mu s$.

Fig.15 Control voltage as a function of mounting base temperature; typical values.

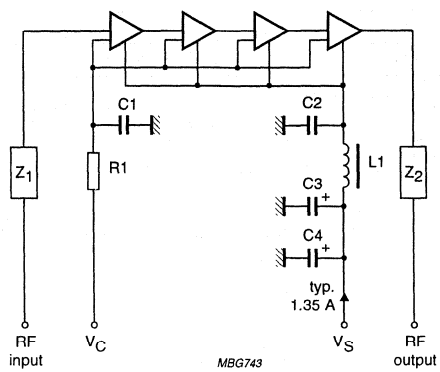
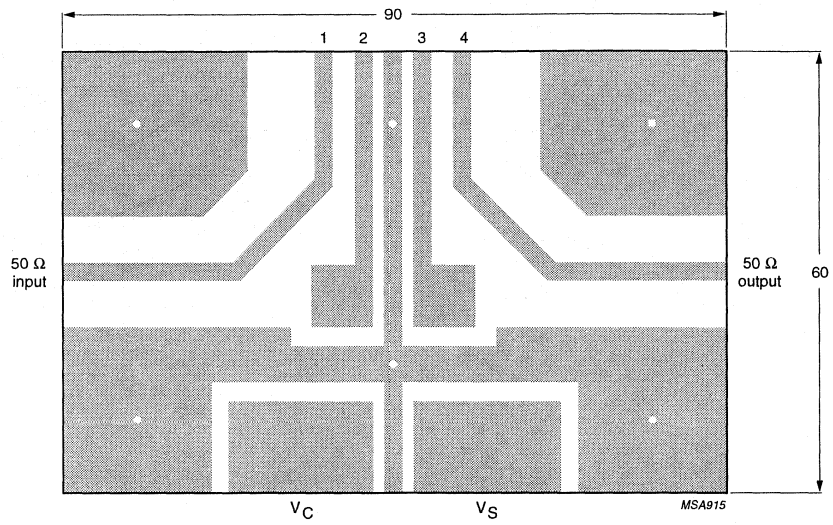


Fig.16 Test circuit.



Dimensions in mm.

Fig.17 Printed-circuit board layout.

List of components (see Fig.16)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2	multilayer ceramic chip capacitor	680 pF		2222 851 11681
C3	tantalum capacitor	2.2 μF; 35 V		–
C4	electrolytic capacitor	47 μF; 40 V		2222 030 37479
L1	Grade 4S2 Ferroxcube bead			4330 030 36300
Z_1, Z_2	stripline; note 1	50 Ω	width = 2.33 mm	–
R1	metal film resistor	100 Ω; 0.6 W		2322 156 11001

Note

1. The striplines are on a double copper-clad printed-circuit board with PTFE fibreglass dielectric (ε_r = 2.2); thickness $1/32$ inch.

SOLDERING

The indicated temperatures are those at the solder interfaces.

Advised solder types are types with a liquidus less than or equal to 210 °C.

Solder dots or solder prints must be large enough to wet the contact areas.

Footprints for soldering should cover the module contact area +0.1 mm on all sides.

Soldering can be carried out using a conveyor oven, a hot air oven, an infrared oven or a combination of these ovens.

Hand soldering must be avoided because the soldering iron tip can exceed the maximum permitted temperature of 250 °C and damage the module.

The maximum temperature profile and soldering time is indicated as follows (see Fig.18):

t = 350 s at 100 °C

t = 300 s at 125 °C

t = 200 s at 150 °C

t = 100 s at 175 °C

t = 50 s at 200 °C

t = 5 s at 250 °C (maximum temperature).

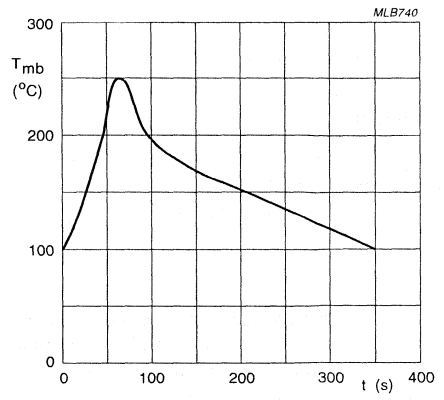


Fig.18 Maximum allowable temperature profile.

Cleaning

The following fluids may be used for cleaning:

- Alcohol
- Bio-Act (Terpene Hydrocarbon)
- Triclean B/S
- Acetone.

Ultrasonic cleaning should not be used since this can cause serious damage to the product.

UHF amplifier module BGY206

FEATURES

- 4.8 V nominal supply voltage
- 3 W output power
- Easy control of output power by DC voltage.

APPLICATIONS

- Digital cellular radio systems with Time Division Multiple Access (TDMA) operation (GSM systems) in the 880 to 915 MHz frequency range.

DESCRIPTION

The BGY206 is a three-stage UHF amplifier module in a SOT388A package. The module consists of three NPN silicon planar transistor dies mounted together with matching and bias circuit components on a metallized ceramic substrate.

PINNING - SOT388A

PIN	DESCRIPTION
1	RF input
2	V_C
3	V_S
4	RF output
Flange	ground

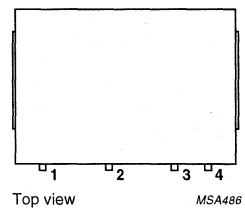


Fig.1 Simplified outline.

QUICK REFERENCE DATA

RF performance at T_{mb} = 25 °C.

MODE OF OPERATION	f (MHz)	V_S (V)	V_C (V)	P_L (W)	G_p (dB)	η (%)	Z_S; Z_L (Ω)
Pulsed; δ = 1 : 8	880 to 915	4.8	≤3.5	3	≥30	typ. 45	50

LIMITING VALUES

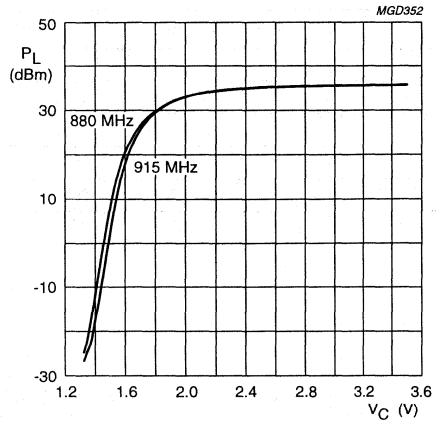
In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_S	DC supply voltage	–	7	V
V_C	DC control voltage	–	4	V
P_D	input drive power	–	10	mW
P_L	load power	–	3.5	W
T_{stg}	storage temperature	–40	+100	°C
T_{mb}	operating mounting base temperature	–30	+100	°C

CHARACTERISTICS

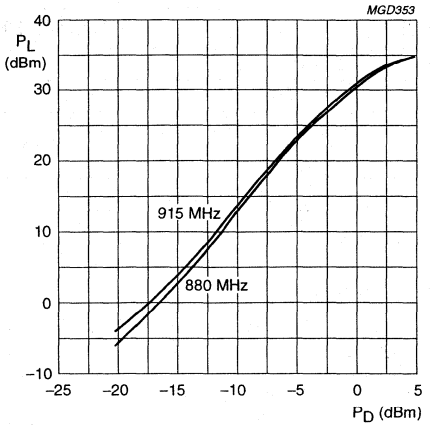
$Z_S = Z_L = 50\ \Omega$; $P_D = 3$ mW; $V_S = 4.8$ V; $V_C \leq 3.5$ V; f = 880 to 915 MHz; $T_{mb} = 25$ °C; $\delta = 1 : 8$; $t_p = 575\ \mu$s; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_Q	leakage current	$V_C = 0.5$ V	–	–	100	μA
I_C	control current	adjust V_C for $P_L = 3$ W	–	–	500	μA
P_L	load power	$V_C = 3.5$ V	3	–	–	W
G_p	power gain	adjust V_C for $P_L = 3$ W	30	–	–	dB
η	efficiency	adjust V_C for $P_L = 3$ W	–	45	–	%
H_2	second harmonic	adjust V_C for $P_L = 3$ W	–	–	–40	dBc
H_3	third harmonic	adjust V_C for $P_L = 3$ W	–	–	–40	dBc
$VSWR_{in}$	input VSWR	adjust V_C for $P_L = 3$ W	–	–	3 : 1	
	stability	$P_D = 1.5$ to 6 mW; $V_S = 4$ to 6.5 V; $V_C = 0$ to 3.5 V; $P_L \leq 3$ W; VSWR ≤ 6 : 1 through all phases;	–	–	–60	dBc
	isolation	$V_C = 0.5$ V	–	–	–36	dBm
	control bandwidth		1	–	–	MHz
P_n	noise power	$P_L = 3$ W; bandwidth = 30 kHz; 20 MHz above transmission band	–	–	–85	dBm
	ruggedness	$V_S = 6.5$ V; adjust V_C for $P_L = 3$ W; VSWR ≤ 10 : 1 through all phases;	no degradation			



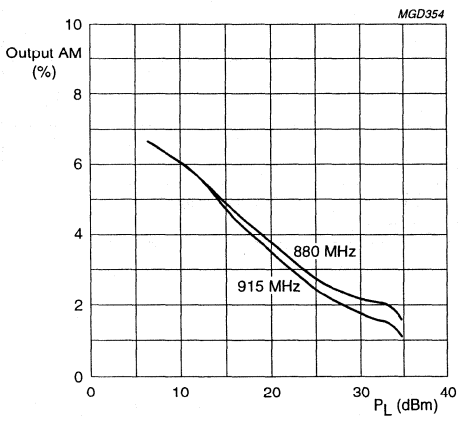
$Z_S = Z_L = 50\ \Omega$; $V_S = 4.8$ V; $P_D = 3$ mW;
$T_{mb} = 25$ °C; $\delta = 1 : 8$; $t_p = 575\ \mu$s.

Fig.2 Load power as a function of control voltage; typical values.



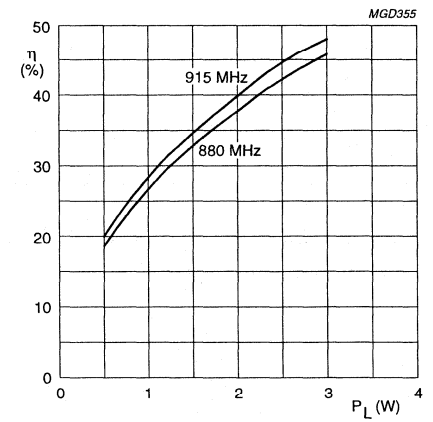
$Z_S = Z_L = 50\ \Omega$; $V_S = 4.8$ V; adjust V_C for $P_L = 3$ W;
$T_{mb} = 25$ °C; $\delta = 1 : 8$; $t_p = 575\ \mu$s.

Fig.3 Load power as a function of drive power; typical values.



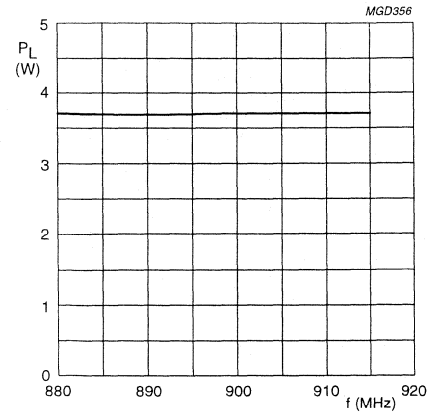
$Z_S = Z_L = 50\ \Omega$; $V_S = 4.8$ V; $P_D = 3$ mW; $T_{mb} = 25$ °C;
input amplitude modulation = 3%; $\delta = 1 : 8$; $t_p = 575\ \mu$s.

Fig.4 Output amplitude modulation as a function of load power; typical values.



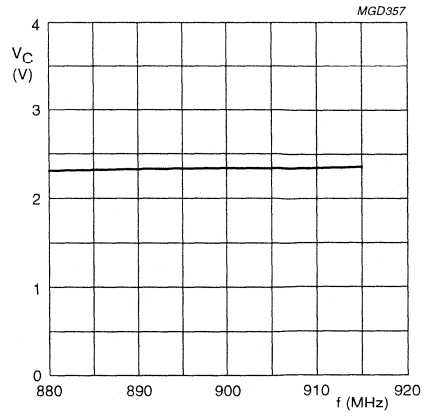
$Z_S = Z_L = 50\ \Omega$; $V_S = 4.8$ V; $P_D = 3$ mW;
$T_{mb} = 25$ °C; $\delta = 1 : 8$; $t_p = 575\ \mu$s

Fig.5 Efficiency as a function of load power; typical values.



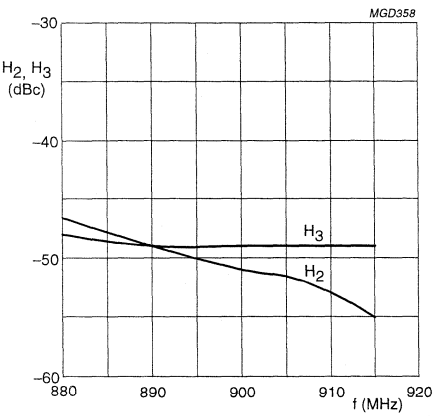
$Z_S = Z_L = 50\ \Omega$; $V_S = 4.8$ V; $P_D = 3$ mW; $V_C = 3.5$ V; $T_{mb} = 25$ °C; $\delta = 1 : 8$; $t_p = 575$ µs.

Fig.6 Load power as a function of frequency; typical values.



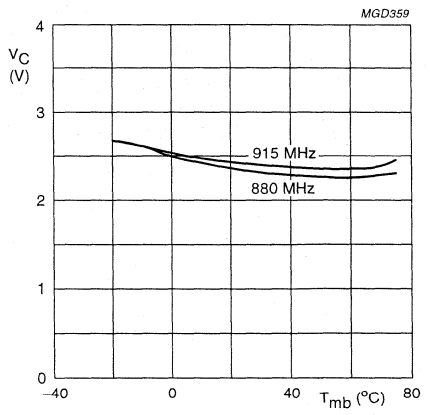
$Z_S = Z_L = 50\ \Omega$; $V_S = 4.8$ V; $P_D = 3$ mW; $P_L = 3$ W; $T_{mb} = 25$ °C; $\delta = 1 : 8$; $t_p = 575$ µs.

Fig.7 Control voltage as a function of frequency; typical values.



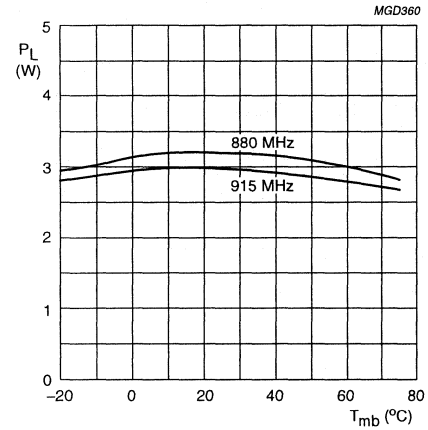
$Z_S = Z_L = 50\ \Omega$; $V_S = 4.8$ V; $P_D = 3$ mW; $P_L = 3$ W; $T_{mb} = 25$ °C; $\delta = 1 : 8$; $t_p = 575$ µs.

Fig.8 Harmonics as a function of frequency; typical values.



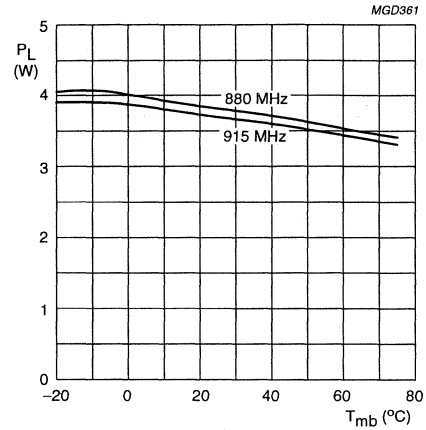
$Z_S = Z_L = 50\ \Omega$; $V_S = 4.8$ V; $P_D = 3$ mW; $P_L = 3$ W; $\delta = 1 : 8$; $t_p = 575$ µs.

Fig.9 Control voltage as a function of mounting base temperature; typical values.



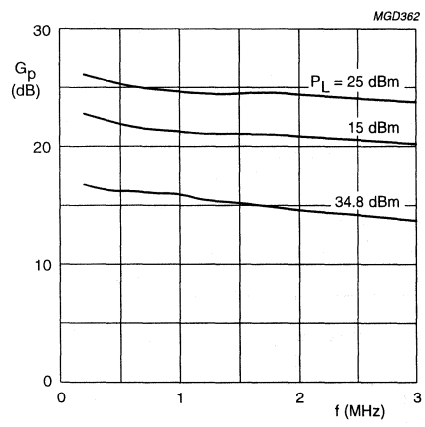
$Z_S = Z_L = 50\ \Omega$; $V_S = 4.3$ V; $P_D = 3$ mW; $V_C = 3.5$ V; $\delta = 1:8$; $t_p = 575\ \mu s$.

Fig.10 Load power as a function of mounting base temperature; typical values.



$Z_S = Z_L = 50\ \Omega$; $V_S = 4.8$ V; $P_D = 3$ mW; $V_C = 3.5$ V; $\delta = 1:8$; $t_p = 575\ \mu s$.

Fig.11 Load power as a function of mounting base temperature; typical values.



$Z_S = Z_L = 50\ \Omega$; $V_S = 4.8$ V; $P_D = 3$ mW; f = 900 MHz; C1 = 0; R1 = 100 Ω; $T_{mb} = 25$ °C; $\delta = 1:8$; $t_p = 575\ \mu s$.

Fig.12 Control loop power gain as a function of frequency on the control pin; typical values.

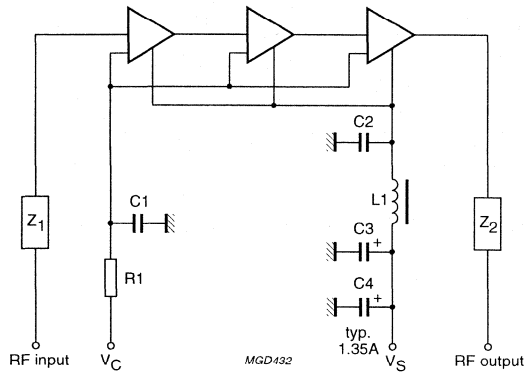
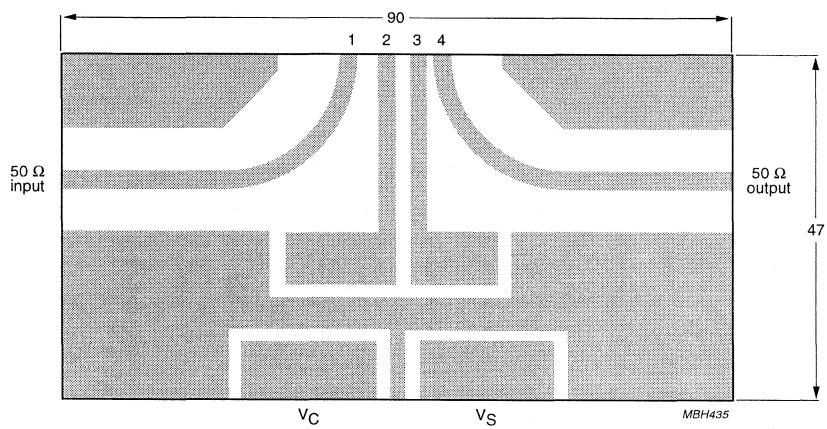


Fig.13 Test circuit.



Dimensions in mm.

Fig.14 Printed-circuit board layout.

List of components (See Fig 13)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2	multilayer ceramic chip capacitor	680 pF		2222 851 11681
C3	tantalum capacitor	2.2 μF; 35 V		–
C4	electrolytic capacitor	47 μF; 40 V		2222 030 37479
L1	Grade 4S2 Ferroxcube bead			4330 030 36300
Z_1, Z_2	stripline; note 1	50 Ω	width 2.33 mm	–
R1	metal film resistor	100 Ω; 0.6 W		2322 156 11001

Note

1. The striplines are on a double copper-clad printed-circuit board with PTFE fibreglass dielectric ($\varepsilon_r = 2.2$); thickness $1/32$ inch.

SOLDERING

The indicated temperatures are those at the solder interfaces.

Advised solder types are types with a liquidus less than or equal to 210 °C.

Solder dots or solder prints must be large enough to wet the contact areas.

Footprints for soldering should cover the module contact area +0.1 mm on all sides.

Soldering can be carried out using a conveyor oven, a hot air oven, an infrared oven or a combination of these ovens.

Hand soldering must be avoided because the soldering iron tip can exceed the maximum permitted temperature of 250 °C and damage the module.

The maximum temperature profile and soldering time is indicated as follows (see Fig.15):

t = 350 s at 100 °C

t = 300 s at 125 °C

t = 200 s at 150 °C

t = 100 s at 175 °C

t = 50 s at 200 °C

t = 5 s at 250 °C (maximum temperature).

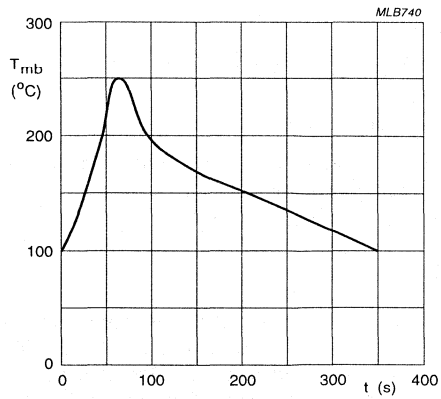


Fig.15 Maximum allowable temperature profile.

Cleaning

The following fluids may be used for cleaning:

- Alcohol
- Bio-Act (Terpene Hydrocarbon)
- Triclean B/S
- Acetone.

Ultrasonic cleaning should not be used since this can cause serious damage to the product.

UHF amplifier module BGY240

FEATURES

- 3.5 V nominal supply voltage
- 3 W output power
- Easy output power control by DC voltage.

APPLICATIONS

- Digital cellular radio systems with Time Division Multiple Access (TDMA) operation (GSM systems) in the 890 to 915 MHz frequency range.

DESCRIPTION

The BGY240 is a three-stage UHF amplifier module in a SOT388C package. The module consists of three NPN silicon planar transistor dies mounted together with matching and bias circuit components on a metallized ceramic substrate. The back of the SOT388C heatsink is plated with 5 μm PbSn.

PINNING - SOT388C

PIN	DESCRIPTION
1	RF input
2	V_C
3	V_S
4	RF output
Flange	ground

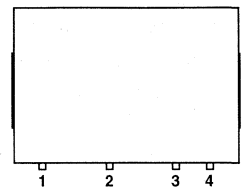


Fig.1 Simplified outline

QUICK REFERENCE DATA

RF performance at T_{mb} = 25 °C.

MODE OF OPERATION	f (MHz)	V_S (V)	V_C (V)	P_L (W)	G_p (dB)	η (%)	Z_S, Z_L (Ω)
Pulsed; δ = 1 : 8	890 to 915	3.5	≤2.2	≥3; typ. 3.5	≥35	typ. 44	50

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_S	DC supply voltage	V_C < 0.2 V; no RF	–	6	V
		V_C ≥ 0.2 V	–	5	V
V_C	DC control voltage		–	3	V
P_D	input drive power		–	5	mW
P_L	load power		–	3.8	W
T_{stg}	storage temperature		–40	+100	°C
T_{mb}	operating mounting base temperature		–30	+100	°C

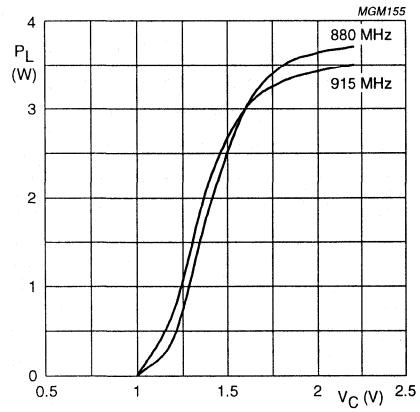
CAUTION

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

CHARACTERISTICS

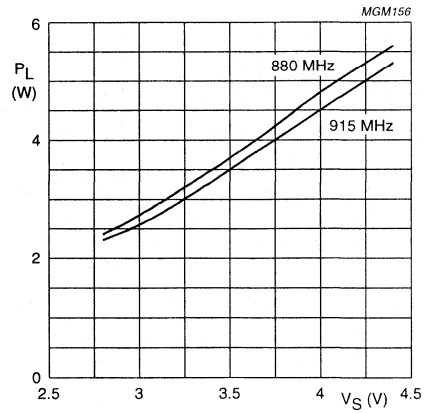
$Z_S = Z_L = 50\ \Omega$; $P_D = 1$ mW; $V_S = 3.5$ V; $V_C \leq 2.2$ V; f = 890 to 915 MHz; $T_{mb} = 25$ °C; $\delta = 1 : 8$; $t_p = 575\ \mu s$; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_Q	leakage current	$V_C = 0.2$ V	–	–	10	μA
I_{CM}	peak control current	adjust V_C for $P_L = 2.5$ W	–	–	3	mA
P_L	load power	$V_C = 2.2$ V	3	3.5	–	W
G_p	power gain	adjust V_C for $P_L = 2.5$ W	35	–	–	dB
η	efficiency	adjust V_C for $P_L = 2.5$ W	–	44	–	%
H_2	second harmonic	adjust V_C for $P_L = 2.5$ W	–	–	–35	dBc
H_3	third harmonic	adjust V_C for $P_L = 2.5$ W	–	–	–35	dBc
$VSWR_{in}$	input VSWR	adjust V_C for $P_L = 2.5$ W	–	1.8 : 1	3 : 1	
	stability	$V_S = 3$ to 5 V; $P_D = -2$ to 5 dBm; $V_C = 0$ to 2.2 V; $P_L \leq 3$ W; VSWR ≤ 12 : 1 through all phases	–	–	–60	dBc
	isolation	$V_C = 0.2$ V	–	–45	–36	dBm
P_n	noise power	$P_L = 2.5$ W; bandwidth = 30 kHz; 10 MHz above transmission band	–	–82	–80	dBm
	AM/PM conversion	$P_D = -2$ to 5 dBm; $P_L = 6$ to 34 dBm	–	–	3	deg/dB
	AM/AM conversion	P_D with 3% AM; f = 100 kHz; $P_L = 6$ to 34 dBm	–	–	12	%
t_r, t_f	carrier switching time	$P_L = 6$ to 34 dBm; time to settle within –0.5 dB of final P_L	–	1.5	2	μs
	ruggedness	$V_S = 5$ V; adjust V_C for $P_L = 3$ W; VSWR ≤ 12 : 1 through all phases	no degradation			



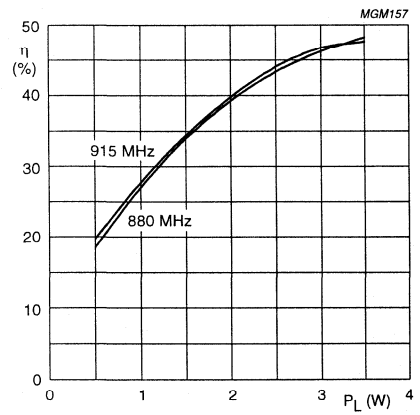
$Z_S = Z_L = 50\ \Omega$; $V_S = 3.5$ V; $P_D = 1$ mW;
$T_{mb} = 25$ °C; $\delta = 1 : 8$; $t_p = 575\ \mu$s.

Fig.2 Load power as a function of control voltage; typical values.



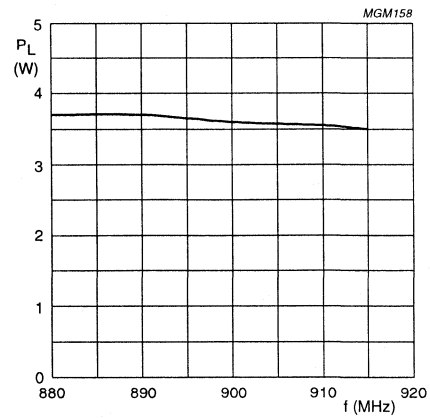
$Z_S = Z_L = 50\ \Omega$; $V_C = 2.2$ V; $P_D = 1$ mW;
$T_{mb} = 25$ °C; $\delta = 1 : 8$; $t_p = 575\ \mu$s.

Fig.3 Load power as a function of supply voltage; typical values.



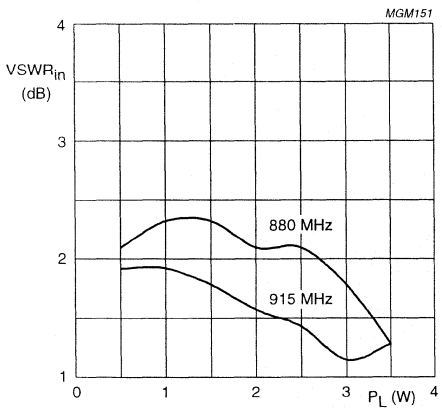
$Z_S = Z_L = 50\ \Omega$; $V_S = 3.5$ V; $P_D = 1$ mW;
$T_{mb} = 25$ °C; $\delta = 1 : 8$; $t_p = 575\ \mu$s.

Fig.4 Efficiency as a function of load power; typical values.



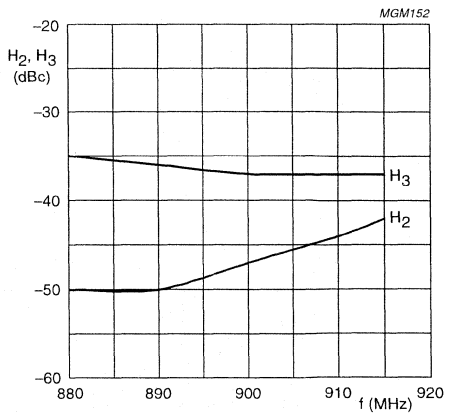
$Z_S = Z_L = 50\ \Omega$; $V_S = 3.5$ V; $P_D = 1$ mW; $V_C = 2.2$ V;
$T_{mb} = 25$ °C; $\delta = 1 : 8$; $t_p = 575\ \mu$s.

Fig.5 Load power as a function of frequency; typical values.



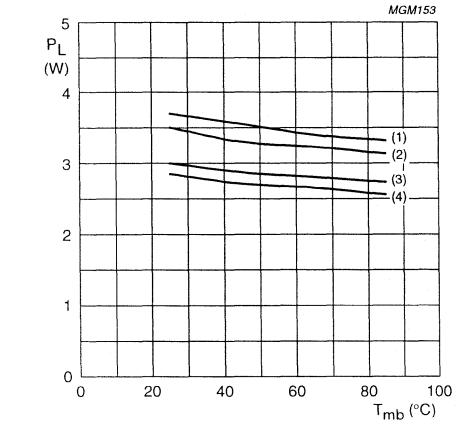
$Z_S = Z_L = 50\ \Omega$; $V_S = 3.5$ V; $P_D = 1$ mW;
$T_{mb} = 25$ °C; $\delta = 1 : 8$; $t_p = 575\ \mu s$

Fig.6 Input VSWR as a function of load power; typical values.



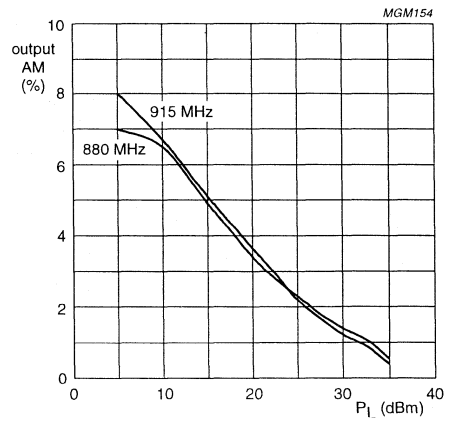
$Z_S = Z_L = 50\ \Omega$; $V_S = 3.5$ V; $P_D = 1$ mW; $P_L = 2.5$ W;
$T_{mb} = 25$ °C; $\delta = 1 : 8$; $t_p = 575\ \mu s$.

Fig.7 Harmonics as a function of frequency; typical values.



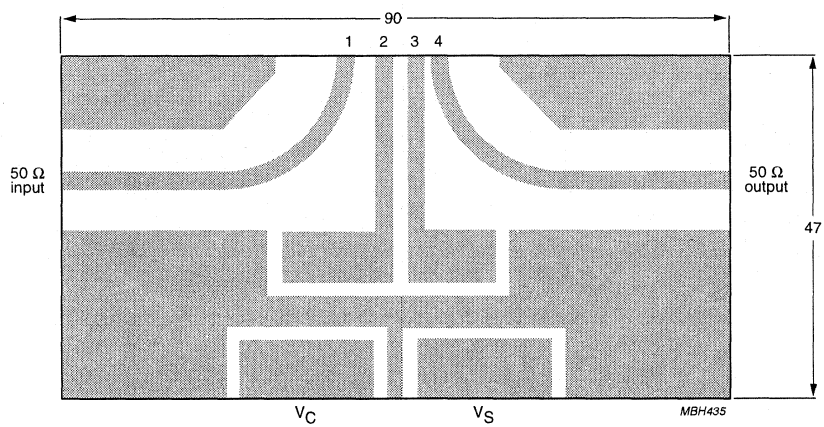
$Z_S = Z_L = 50\ \Omega$; $P_D = 1$ mW; $V_C = 2.2$ V; $\delta = 1 : 8$; $t_p = 575\ \mu s$.
(1) $V_S = 3.5$ V; f = 880 MHz.
(2) $V_S = 3.5$ V; f = 915 MHz.
(3) $V_S = 3.1$ V; f = 880 MHz.
(4) $V_S = 3.1$ V; f = 915 MHz.

Fig.8 Load power as a function of mounting base temperature; typical values.



$Z_S = Z_L = 50\ \Omega$; $V_S = 3.5$ V; $P_D = 1$ mW; $T_{mb} = 25$ °C;
$\Delta f = 100$ kHz; input amplitude modulation = 3%; $\delta = 1 : 8$; $t_p = 575\ \mu s$.

Fig.9 Output amplitude modulation as a function of load power; typical values.



Dimensions in mm.

Fig.10 Printed-circuit board test-fixture.

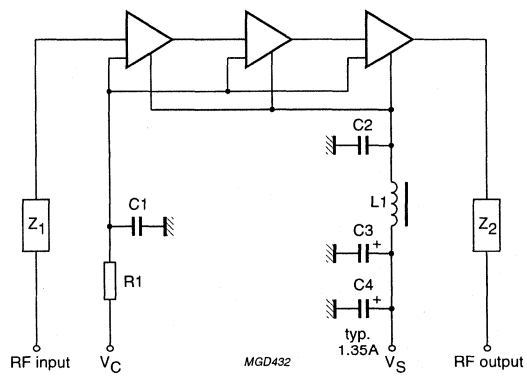


Fig.11 Test circuit.

List of components (see Fig.11)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2	multilayer ceramic chip capacitor	680 pF		2222 851 11681
C3	tantalum capacitor	2.2 μF; 35 V		–
C4	electrolytic capacitor	47 μF; 40 V		2222 030 37479
L1	Grade 4S2 Ferroxcube bead			4330 030 36300
Z_1, Z_2	stripline; note 1	50 Ω	width 2.33 mm	–
R1	metal film resistor	100 Ω; 0.6 W		2322 156 11001

Note

1. The striplines are on a double copper-clad printed-circuit board with PTFE fibreglass dielectric (ε_r = 2.2); thickness $^1/_{32}$ inch.

SOLDERING

The indicated temperatures are those at the solder interfaces.

Advised solder types are types with a liquidus less than or equal to 210 °C.

Solder dots or solder prints must be large enough to wet the contact areas.

Soldering can be carried out using a conveyor oven, a hot air oven, an infrared oven or a combination of these ovens. A double reflow process is permitted.

Hand soldering must be avoided because the soldering iron tip can exceed the maximum permitted temperature of 250 °C and damage the module.

The maximum allowed temperature is 250 °C for a maximum of 5 seconds.

The maximum ramp-up is 10 °C per second.

The maximum cool-down is 5 °C per second.

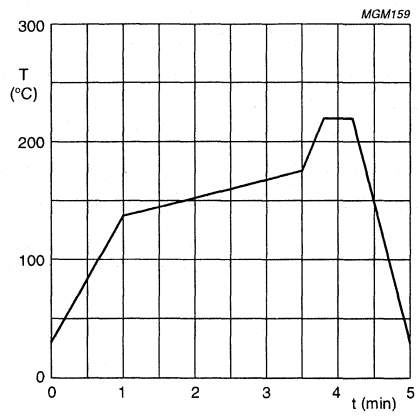


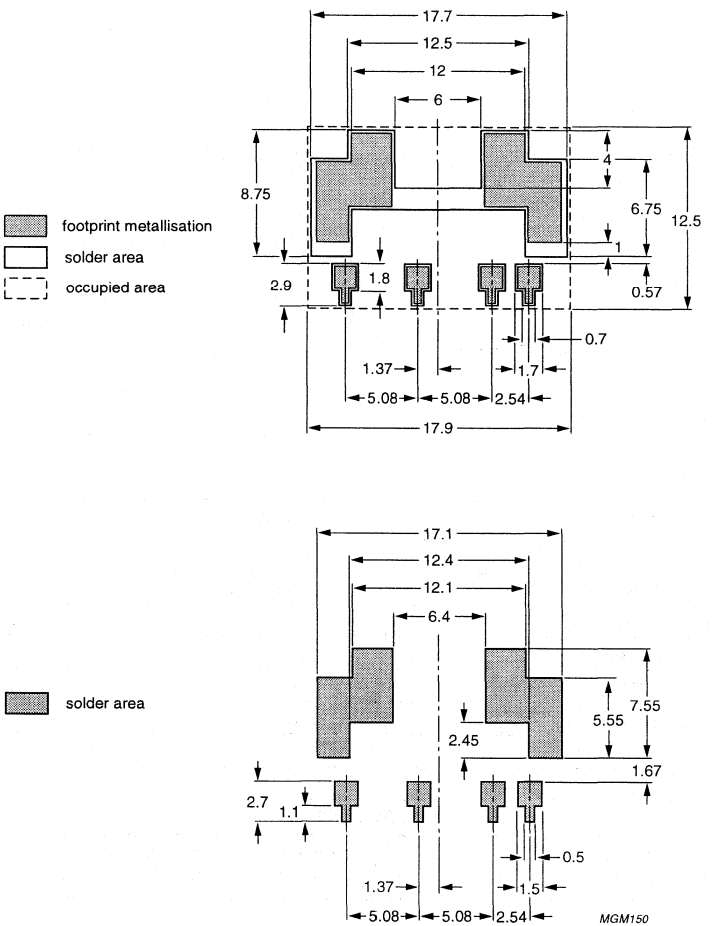
Fig.12 Recommended reflow temperature profile.

Cleaning

The following fluids may be used for cleaning:

- Alcohol
- Bio-Act (Terpene Hydrocarbon)
- Triclean B/S
- Acetone.

Ultrasonic cleaning should not be used since this can cause serious damage to the product.



Dimensions in mm.

Fig.13 Footprint SOT388C.

N-channel enhancement mode MOS transistor

BSH103

FEATURES

- Very low threshold
- High-speed switching
- No secondary breakdown
- Direct interface to C-MOS, TTL etc.

APPLICATIONS

- Power management
- DC to DC converters
- Battery powered applications
- 'Glue-logic'; interface between logic blocks and/or periphery
- General purpose switch.

DESCRIPTION

N-channel enhancement mode MOS transistor in a SOT23 SMD package.

PINNING - SOT23

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	s	source
3	d	drain

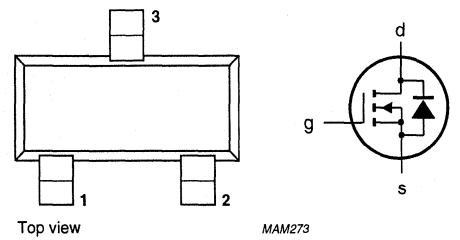


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETERS	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	30	V
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = 0.5 A	–	1	V
V_{GS}	gate-source voltage (DC)		–	±8	V
V_{GSth}	gate-source threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	0.4	–	V
I_D	drain current (DC)	T_s = 80 °C	–	0.9	A
R_{DSon}	drain-source on-state resistance	V_{GS} = 2.5 V; I_D = 0.5 A	–	0.475	Ω
P_{tot}	total power dissipation	T_s = 80 °C	–	0.5	W

CAUTION

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

N-channel enhancement mode MOS transistor

BSH103

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	30	V
V_{GS}	gate-source voltage (DC)		–	±8	V
I_D	drain current (DC)	T_s = 80 °C; note 1	–	0.85	A
I_{DM}	peak drain current	note 2	–	3.4	A
P_{tot}	total power dissipation	T_s = 80 °C	–	0.5	W
		T_{amb} = 25 °C; note 3	–	0.75	W
		T_{amb} = 25 °C; note 4	–	0.54	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–55	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 80 °C	–	0.5	A
I_{SM}	peak pulsed source current	note 2	–	2	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
4. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

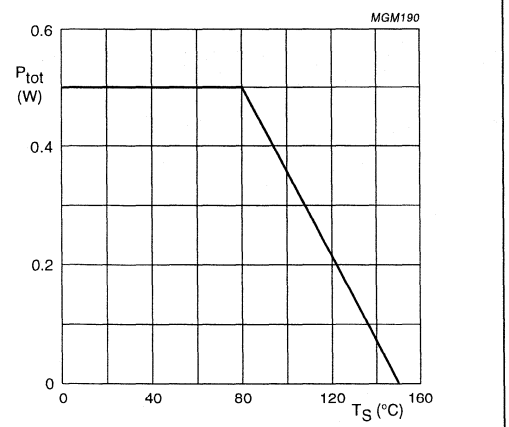
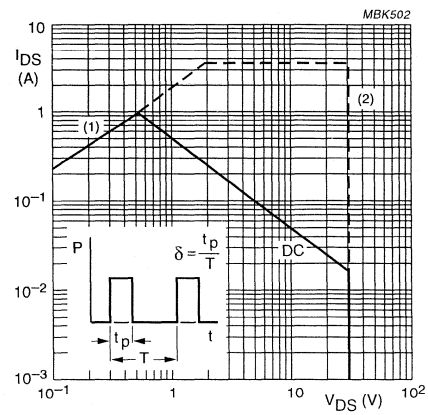


Fig.2 Power derating curve.

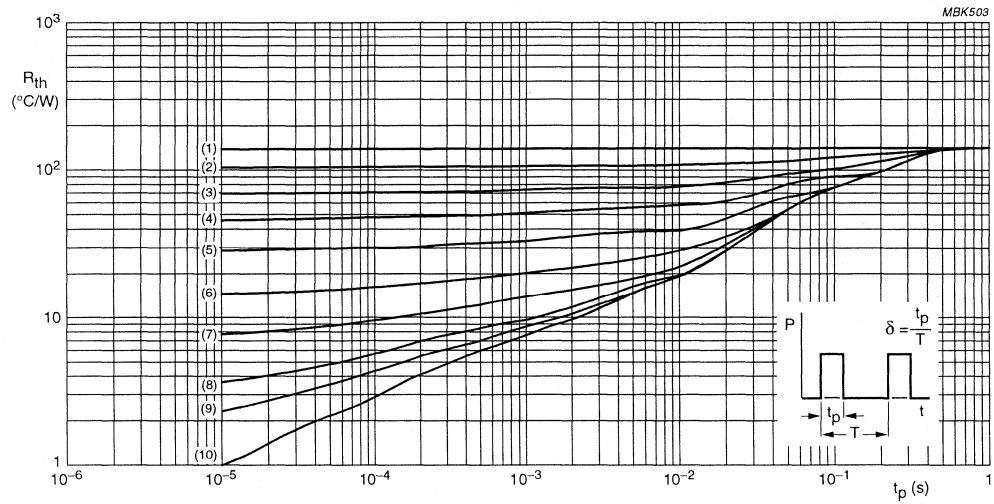


δ = 0.01; T_s = 80 °C.
(1) R_{DSon} limitation.
(2) Pulsed.

Fig.3 SOAR.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	140	K/W



(1) δ = 1. (2) δ = 0.75. (3) δ = 0.5. (4) δ = 0.33. (5) δ = 0.2.
(6) δ = 0.1. (7) δ = 0.05. (8) δ = 0.02. (9) δ = 0.01. (10) δ = 0.

Fig.4 Transient thermal resistance from junction to soldering point as a function of pulse time; typical values.

N-channel enhancement mode MOS transistor

BSH103

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 10 µA	30	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = 1 mA	0.4	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 24 V	–	–	100	nA
I_{GSS}	gate leakage current	V_{GS} = ±8 V; V_{DS} = 0	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 0.5 A	–	–	0.4	Ω
		V_{GS} = 2.5 V; I_D = 0.5 A	–	–	0.475	Ω
		V_{GS} = 1.8 V; I_D = 0.25 A	–	–	0.525	Ω
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	83	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	27	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	14	–	pF
Q_G	total gate charge	V_{GS} = 4.5 V; V_{DD} = 15 V; I_D = 0.5 A; T_{amb} = 25 °C	–	2100	–	pC
Q_{GS}	gate-source charge	V_{DD} = 15 V; I_D = 0.5 A; T_{amb} = 25 °C	–	95	–	pC
Q_{GD}	gate-drain charge	V_{DD} = 15 V; I_D = 0.5 A; T_{amb} = 25 °C	–	670	–	pC
Switching times						
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to 8 V; V_{DD} = 15 V; I_D = 0.5 A; R_{gen} = 6 Ω	–	2.5	–	ns
t_f	fall time	V_{GS} = 0 to 8 V; V_{DD} = 15 V; I_D = 0.5 A; R_{gen} = 6 Ω	–	3.5	–	ns
t_{on}	turn-on switching time	V_{GS} = 0 to 8 V; V_{DD} = 15 V; I_D = 0.5 A; R_{gen} = 6 Ω	–	6	–	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = 8 to 0 V; V_{DD} = 15 V; I_D = 0.5 A; R_{gen} = 6 Ω	–	20	–	ns
t_r	rise time	V_{GS} = 8 to 0 V; V_{DD} = 15 V; I_D = 0.5 A; R_{gen} = 6 Ω	–	7	–	ns
t_{off}	turn-off switching time	V_{GS} = 8 to 0 V; V_{DD} = 15 V; I_D = 0.5 A; R_{gen} = 6 Ω	–	27	–	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = 0.5 A	–	–	1	V
t_{rr}	reverse recovery time	I_S = 0.5 A; di/dt = –100 A/µs	–	25	–	ns

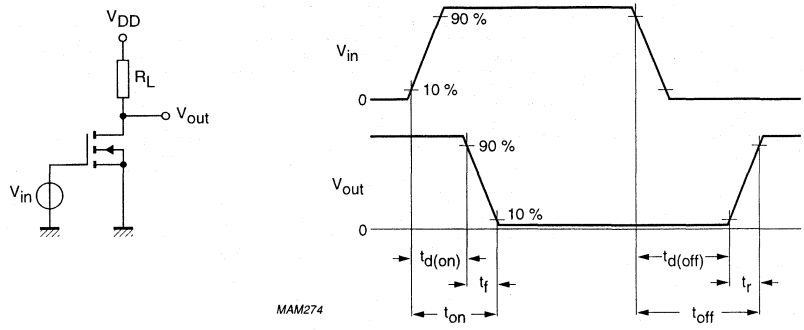
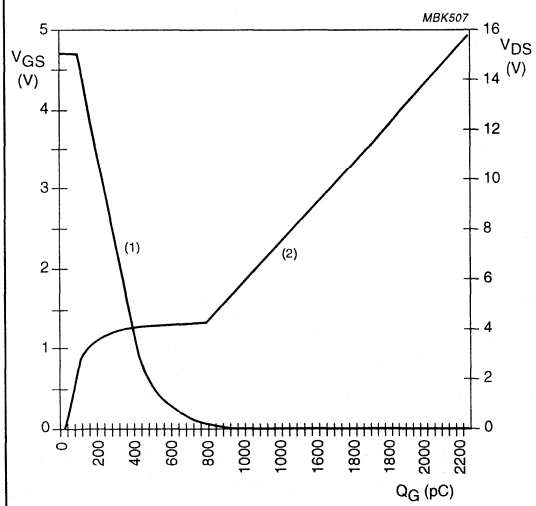
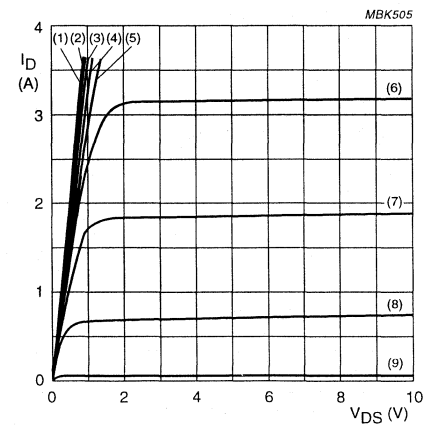


Fig.5 Switching times test circuit with input and output waveforms.



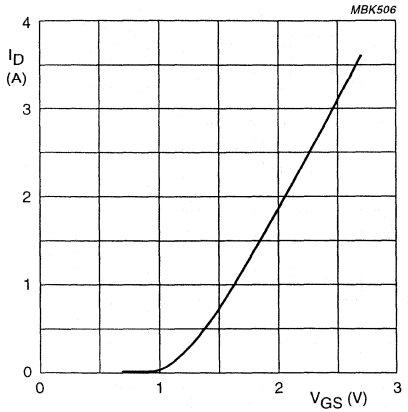
V_{DD} = 15 V; I_D = 0.5 A; T_{amb} = 25 °C.
(1) V_{DS}.
(2) V_{GS}.

Fig.6 Gate-source and drain-source voltages as functions of total gate charge; typical values.



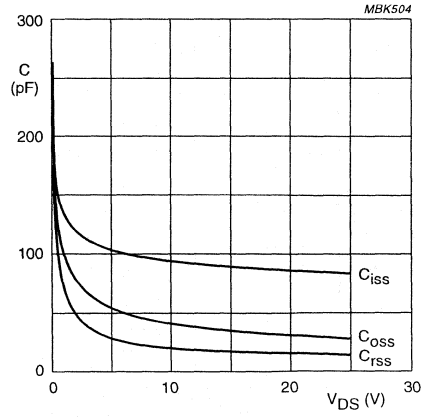
T_{amb} = 25 °C; t_p = 300 µs; δ = 0.
(1) V_{GS} = 7.5 V.
(2) V_{GS} = 5.5 V.
(3) V_{GS} = 4.5 V.
(4) V_{GS} = 3.5 V.
(5) V_{GS} = 3 V.
(6) V_{GS} = 2.5 V.
(7) V_{GS} = 2 V.
(8) V_{GS} = 1.5 V.
(9) V_{GS} = 1 V.

Fig.7 Output characteristics; typical values.



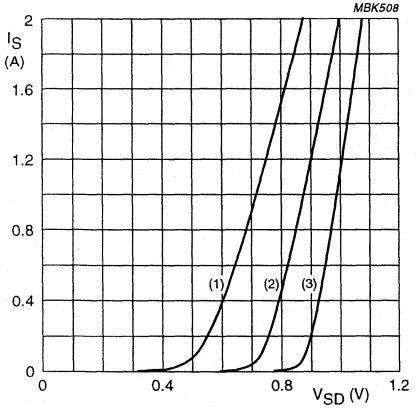
V_{DS} = 10 V; T_{amb} = 25 °C; t_p = 300 µs; δ = 0.

Fig.8 Transfer characteristic; typical values.



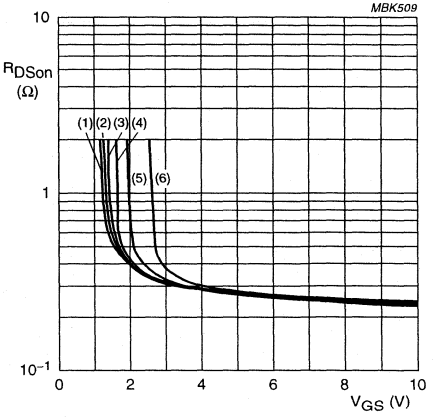
V_{GS} = 0 ; f = 1 MHz; T_{amb} = 25 °C.

Fig.9 Capacitance as a function of drain-source voltage; typical values.



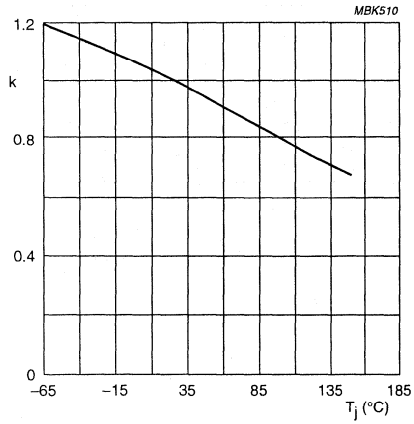
V_{GD} = 0.
(1) T_{amb} = 150 °C.
(2) T_{amb} = 25 °C.
(3) T_{amb} = −65 °C.

Fig.10 Source current as a function of source-drain diode forward voltage; typical values.



T_{amb} = 25 °C; t_p = 300 µs; δ = 0.
(1) I_D = 0.1 A.
(2) I_D = 0.22 A.
(3) I_D = 0.45 A.
(4) I_D = 0.9 A.
(5) I_D = 1.8 A.
(6) I_D = 3.6 A.

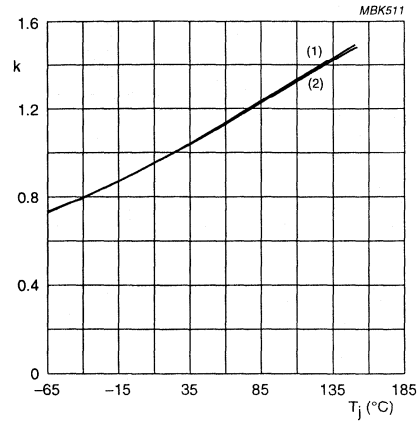
Fig.11 Drain-source on-state resistance as a function of gate-source voltage; typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$$

V_{GSth} at $V_{DS} = V_{GS}$; I_D = 1 mA.

Fig.12 Temperature coefficient of gate-source threshold voltage as a function of junction temperature; typical values.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\,°C}$$

(1) R_{DSon} at V_{GS} = 4.5 V; I_D = 0.5 mA.
(2) R_{DSon} at V_{GS} = 2.5 V; I_D = 0.5 mA.

Fig.13 Temperature coefficient of drain-source on-resistance as a function of junction temperature; typical values.

N-channel enhancement mode MOS transistor

BSH104

FEATURES

- High-speed switching
- No secondary breakdown
- Direct interface to C-MOS, TTL, etc.
- Very low threshold.

APPLICATIONS

- 'Glue-logic': interface between logic blocks and/or periphery
- Power management
- DC to DC converters
- General purpose switch
- Battery powered applications.

DESCRIPTION

N-channel enhancement mode MOS transistor in a SOT23 SMD package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	s	source
3	d	drain

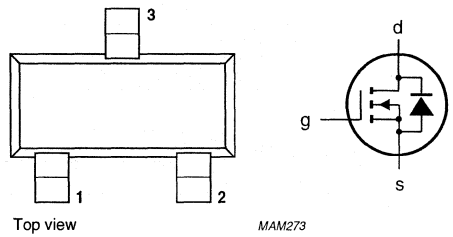


Fig.1 Simplified outline (SOT23) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	12	V
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = 0.5 A	–	1	V
V_{GS}	gate-source voltage (DC)		–	±8	V
V_{GSth}	gate-source threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	0.4	–	V
I_D	drain current (DC)	T_s = 80 °C	–	1.1	A
R_{DSon}	drain-source on-state resistance	V_{GS} = 2.5 V; I_D = 0.65 A	–	0.3	Ω
P_{tot}	total power dissipation	T_s = 80 °C	–	0.5	W

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	12	V
V_{GS}	gate-source voltage (DC)		–	±8	V
I_D	drain current (DC)	T_s = 80 °C; note 1	–	1.1	A
I_{DM}	peak drain current	note 2	–	4.5	A
P_{tot}	total power dissipation	T_s = 80 °C	–	0.5	W
		T_{amb} = 25 °C; note 3	–	0.75	W
		T_{amb} = 25 °C; note 4	–	0.54	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–55	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 80 °C	–	0.5	A
I_{SM}	peak pulsed source current	note 2	–	2	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Device mounted on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
4. Device mounted on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	140	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 10 μA	12	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = 1 mA	0.4	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 9.6 V	–	–	100	nA
I_{GSS}	gate leakage current	V_{DS} = 0; V_{GS} = ±8 V	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 0.65 A	–	–	0.23	Ω
		V_{GS} = 2.5 V; I_D = 0.65 A	–	–	0.3	Ω
		V_{GS} = 1.8 V; I_D = 0.32 A	–	–	0.4	Ω
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = 9.6 V; f = 1 MHz	–	t.b.f.	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = 9.6 V; f = 1 MHz	–	t.b.f.	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = 9.6 V; f = 1 MHz	–	t.b.f.	–	pF
Q_G	total gate charge	V_{GS} = 6 V; V_{DD} = 6 V; I_D = 0.65 A; T_{amb} = 25 °C	–	t.b.f.	–	pC
Q_{GS}	gate-source charge	V_{DD} = 6 V; I_D = 0.65 A; T_{amb} = 25 °C	–	t.b.f.	–	pC
Q_{GD}	gate-drain charge	V_{DD} = 6 V; I_D = 0.65 A; T_{amb} = 25 °C	–	t.b.f.	–	pC
Switching times						
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to 6 V; V_{DD} = 6 V; I_D = 0.65 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
t_f	fall time	V_{GS} = 0 to 6 V; V_{DD} = 6 V; I_D = 0.65 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
t_{on}	turn-on switching time	V_{GS} = 0 to 6 V; V_{DD} = 6 V; I_D = 0.65 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = 6 to 0 V; V_{DD} = 6 V; I_D = 0.65 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
t_r	rise time	V_{GS} = 6 to 0 V; V_{DD} = 6 V; I_D = 0.65 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
t_{off}	turn-off switching time	V_{GS} = 6 to 0 V; V_{DD} = 6 V; I_D = 0.65 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = 0.5 A	–	–	1	V
t_{rr}	reverse recovery time	I_S = 0.5 A; di/dt = –100 A/μs	–	t.b.f.	–	ns

N-channel enhancement mode MOS transistor

BSH105

FEATURES

- High-speed switching
- No secondary breakdown
- Direct interface to C-MOS, TTL, etc.
- Very low threshold.

APPLICATIONS

- 'Glue-logic': interface between logic blocks and/or periphery
- Relay driver
- General purpose switch
- Battery powered applications.

DESCRIPTION

N-channel enhancement mode MOS transistor in a SOT23 SMD package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT23

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	s	source
3	d	drain

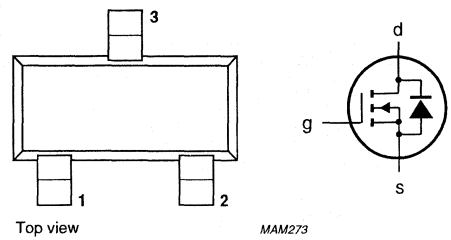


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	12	V
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = 0.5 A	–	1	V
V_{GS}	gate-source voltage (DC)		–	±8	V
V_{GSth}	gate-source threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	0.4	–	V
I_D	drain current (DC)	T_s = 80 °C	–	1.5	A
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 0.8 A	–	0.12	Ω
P_{tot}	total power dissipation	T_s = 80 °C	–	0.5	W

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	12	V
V_{GS}	gate-source voltage (DC)		–	±8	V
I_D	drain current (DC)	T_s = 80 °C; note 1	–	1.5	A
I_{DM}	peak drain current	note 2	–	6	A
P_{tot}	total power dissipation	T_s = 80 °C	–	0.5	W
		T_{amb} = 25 °C; note 3	–	0.75	W
		T_{amb} = 25 °C; note 4	–	0.54	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–55	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 80 °C	–	0.6	A
I_{SM}	peak pulsed source current	note 2	–	2.4	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Device mounted on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
4. Device mounted on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	140	K/W

N-channel enhancement mode MOS transistor

BSH105

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 10 μA	12	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = 1 mA	0.4	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 9.6 V	–	–	100	nA
I_{GSS}	gate leakage current	V_{GS} = ±8 V; V_{DS} = 0	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 0.8 A	–	–	120	mΩ
		V_{GS} = 2.5 V; I_D = 0.8 A	–	–	150	mΩ
		V_{GS} = 1.8 V; I_D = 0.4 A	–	–	230	mΩ
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = 9.6 V; f = 1 MHz	–	t.b.f.	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = 9.6 V; f = 1 MHz	–	t.b.f.	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = 9.6 V; f = 1 MHz	–	t.b.f.	–	pF
Q_G	total gate charge	V_{GS} = 6 V; V_{DD} = 6 V; I_D = 1 A; T_{amb} = 25 °C	–	t.b.f.	–	pC
Q_{GS}	gate-source charge	V_{DD} = 6 V; I_D = 1 A; T_{amb} = 25 °C	–	t.b.f.	–	pC
Q_{GD}	gate-drain charge	V_{DD} = 6 V; I_D = 1 A; T_{amb} = 25 °C	–	t.b.f.	–	pC
Switching times						
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to 6 V; V_{DD} = 6 V; I_D = 1 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
t_f	fall time	V_{GS} = 0 to 6 V; V_{DD} = 6 V; I_D = 1 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
t_{on}	turn-on switching time	V_{GS} = 0 to 6 V; V_{DD} = 6 V; I_D = 1 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = 6 to 0 V; V_{DD} = 6 V; I_D = 1 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
t_r	rise time	V_{GS} = 6 to 0 V; V_{DD} = 6 V; I_D = 1 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
t_{off}	turn-off switching time	V_{GS} = 6 to 0 V; V_{DD} = 6 V; I_D = 1 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = 0.5 A	–	–	1	V
t_{rr}	reverse recovery time	I_S = 0.5 A; di/dt = –100 A/μs	–	t.b.f.	–	ns

N-channel enhancement mode MOS transistor

BSH106

FEATURES

- High-speed switching
- No secondary breakdown
- Direct interface to C-MOS, TTL, etc.
- Very low threshold.

APPLICATIONS

- 'Glue-logic': interface between logic blocks and/or periphery
- Relay driver
- General purpose switch
- Battery powered applications.

DESCRIPTION

N-channel enhancement mode MOS transistor in a SOT363 SMD package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT363

PIN	SYMBOL	DESCRIPTION
1	d	drain
2	d	drain
3	g	gate
4	s	source
5	d	drain
6	d	drain

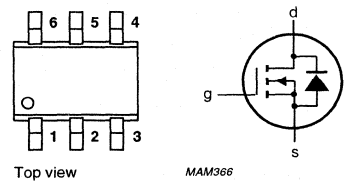


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	12	V
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = 0.5 A	–	1	V
V_{GS}	gate-source voltage (DC)		–	±8	V
V_{GSth}	gate-source threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	0.4	–	V
I_D	drain current (DC)	T_s = 80 °C	–	1.8	A
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 0.9 A	–	0.14	Ω
P_{tot}	total power dissipation	T_s = 80 °C	–	0.8	W

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	12	V
V_{GS}	gate-source voltage (DC)		–	±8	V
I_D	drain current (DC)	T_s = 80 °C; note 1	–	1.8	A
I_{DM}	peak drain current	note 2	–	7.2	A
P_{tot}	total power dissipation	T_s = 80 °C	–	0.8	W
		T_{amb} = 25 °C; note 3	–	1.1	W
		T_{amb} = 25 °C; note 4	–	0.7	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–55	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 80 °C	–	1	A
I_{SM}	peak pulsed source current	note 2	–	4	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Device mounted on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
4. Device mounted on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	87.5	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 10 μA	12	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = 1 mA	0.4	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 9.6 V	–	–	100	nA
I_{GSS}	gate leakage current	V_{GS} = ±8 V; V_{DS} = 0	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 0.9 A	–	–	140	mΩ
		V_{GS} = 2.5 V; I_D = 0.9 A	–	–	180	mΩ
		V_{GS} = 1.8 V; I_D = 0.4 A	–	–	270	mΩ
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = 9.6 V; f = 1 MHz	–	t.b.f.	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = 9.6 V; f = 1 MHz	–	t.b.f.	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = 9.6 V; f = 1 MHz	–	t.b.f.	–	pF
Q_G	total gate charge	V_{GS} = 6 V; V_{DD} = 6 V; I_D = 0.9 A; T_{amb} = 25 °C	–	t.b.f.	–	pC
Q_{GS}	gate-source charge	V_{DD} = 6 V; I_D = 0.9 A; T_{amb} = 25 °C	–	t.b.f.	–	pC
Q_{GD}	gate-drain charge	V_{DD} = 6 V; I_D = 0.9 A; T_{amb} = 25 °C	–	t.b.f.	–	pC
Switching times						
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to 6 V; V_{DD} = 6 V; I_D = 0.9 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
t_f	fall time	V_{GS} = 0 to 6 V; V_{DD} = 6 V; I_D = 0.9 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
t_{on}	turn-on switching time	V_{GS} = 0 to 6 V; V_{DD} = 6 V; I_D = 0.9 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = 6 to 0 V; V_{DD} = 6 V; I_D = 0.9 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
t_r	rise time	V_{GS} = 6 to 0 V; V_{DD} = 6 V; I_D = 0.9 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
t_{off}	turn-off switching time	V_{GS} = 6 to 0 V; V_{DD} = 6 V; I_D = 0.9 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = 0.5 A	–	–	1	V
t_{rr}	reverse recovery time	I_S = 0.5 A; di/dt = –100 A/μs	–	t.b.f.	–	ns

N-channel enhancement mode MOS transistor

BSH107

FEATURES

- High-speed switching
- No secondary breakdown
- Direct interface to C-MOS, TTL, etc.
- Very low threshold.

APPLICATIONS

- 'Glue-logic': interface between logic blocks and/or periphery
- Power management
- DC to DC converters
- General purpose switch
- Battery powered applications.

DESCRIPTION

N-channel enhancement mode MOS transistor in a SOT457 (TSOP6) SMD package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING

PIN	SYMBOL	DESCRIPTION
1	d	drain
2	d	drain
3	g	gate
4	s	source
5	d	drain
6	d	drain

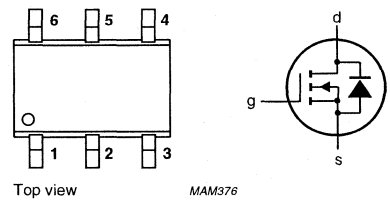


Fig.1 Simplified outline (SOT457) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	12	V
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = 0.8 A	–	1	V
V_{GS}	gate-source voltage (DC)		–	±8	V
V_{GSth}	gate-source threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	0.4	–	V
I_D	drain current (DC)	T_s = 80 °C	–	2.5	A
R_{DSon}	drain-source on-state resistance	V_{GS} = 2.5 V; I_D = 1.8 A	–	0.1	Ω
P_{tot}	total power dissipation	T_s = 80 °C	–	0.8	W

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	12	V
V_{GS}	gate-source voltage (DC)		–	±8	V
I_D	drain current (DC)	T_s = 80 °C; note 1	–	2.5	A
I_{DM}	peak drain current	note 2	–	10	A
P_{tot}	total power dissipation	T_s = 80 °C; note 1	–	0.8	W
		T_{amb} = 25 °C; note 3	–	1.09	W
		T_{amb} = 25 °C; note 4	–	0.7	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–55	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 80 °C; note 1	–	0.8	A
I_{SM}	peak pulsed source current	note 2	–	3.2	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Device mounted on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
4. Device mounted on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	87.5	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 10 μA	12	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = 1 mA	0.4	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 9.6 V	–	–	100	nA
I_{GSS}	gate leakage current	V_{DS} = 0; V_{GS} = ±8 V	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 1.3 A	–	–	0.078	Ω
		V_{GS} = 2.5 V; I_D = 1.3 A	–	–	0.1	Ω
		V_{GS} = 1.8 V; I_D = 1.3 A	–	–	0.133	Ω
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = 9.6 V; f = 1 MHz	–	t.b.f.	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = 9.6 V; f = 1 MHz	–	t.b.f.	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = 9.6 V; f = 1 MHz	–	t.b.f.	–	pF
Q_G	total gate charge	V_{GS} = 6 V; V_{DD} = 6 V; I_D = 1.3 A; T_{amb} = 25 °C	–	t.b.f.	–	pC
Q_{GS}	gate-source charge	V_{DD} = 6 V; I_D = 1.3 A; T_{amb} = 25 °C	–	t.b.f.	–	pC
Q_{GD}	gate-drain charge	V_{DD} = 6 V; I_D = 1.3 A; T_{amb} = 25 °C	–	t.b.f.	–	pC
Switching times						
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to 6 V; V_{DD} = 6 V; I_D = 1.3 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
t_f	fall time	V_{GS} = 0 to 6 V; V_{DD} = 6 V; I_D = 1.3 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
t_{on}	turn-on switching time	V_{GS} = 0 to 6 V; V_{DD} = 6 V; I_D = 1.3 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = 6 to 0 V; V_{DD} = 6 V; I_D = 1.3 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
t_r	rise time	V_{GS} = 6 to 0 V; V_{DD} = 6 V; I_D = 1.3 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
t_{off}	turn-off switching time	V_{GS} = 6 to 0 V; V_{DD} = 6 V; I_D = 1.3 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = 0.8 A	–	–	1	V
t_{rr}	reverse recovery time	I_S = 0.5 A; di/dt = –100 A/μs	–	t.b.f.	–	ns

P-channel enhancement mode MOS transistor

BSH203

FEATURES

- High-speed switching
- No secondary breakdown
- Direct interface to C-MOS, TTL, etc.

APPLICATIONS

- 'Glue-logic': interface between logic blocks and/or periphery
- Power management
- DC to DC converters
- General purpose switch
- Battery powered applications.

DESCRIPTION

P-channel enhancement mode MOS transistor in a SOT23 SMD package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	s	source
3	d	drain

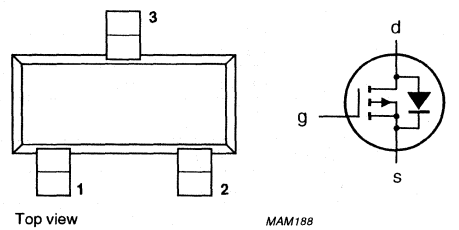


Fig.1 Simplified outline (SOT23) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–30	V
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = –0.38 A	–	–1.3	V
V_{GS}	gate-source voltage (DC)		–	±8	V
V_{GSth}	gate-source threshold voltage	V_{DS} = V_{GS}; I_D = –1 mA	–0.4	–	V
I_D	drain current (DC)	T_s = 80 °C	–	–0.54	A
R_{DSon}	drain-source on-state resistance	V_{GS} = –2.5 V; I_D = –0.3 A	–	1.12	Ω
P_{tot}	total power dissipation	T_s = 80 °C	–	0.5	W

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–30	V
V_{GS}	gate-source voltage (DC)		–	±8	V
I_D	drain current (DC)	T_s = 80 °C; note 1	–	–0.54	A
I_{DM}	peak drain current	note 2	–	–2.17	A
P_{tot}	total power dissipation	T_s = 80 °C	–	0.5	W
		T_{amb} = 25 °C; note 3	–	0.75	W
		T_{amb} = 25 °C; note 4	–	0.54	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–55	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 80 °C	–	–0.38	A
I_{SM}	peak pulsed source current	note 2	–	–1.52	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Device mounted on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
4. Device mounted on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	140	K/W

P-channel enhancement mode MOS transistor

BSH203

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = −10 μA	−30	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = −1 mA	−0.4	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = −24 V	–	–	−100	nA
I_{GSS}	gate leakage current	V_{DS} = 0; V_{GS} = ±8 V	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = −4.5 V; I_D = −0.3 A	–	–	1	Ω
		V_{GS} = −2.5 V; I_D = −0.3 A	–	–	1.12	Ω
		V_{GS} = −1.8 V; I_D = −0.15 A	–	–	1.31	Ω
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = −24 V; f = 1 MHz	–	t.b.f.	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = −24 V; f = 1 MHz	–	t.b.f.	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = −24 V; f = 1 MHz	–	t.b.f.	–	pF
Q_G	total gate charge	V_{GS} = −10 V; V_{DD} = −15 V; I_D = −0.3 A; T_{amb} = 25 °C	–	t.b.f.	–	pC
Q_{GS}	gate-source charge	V_{DD} = −15 V; I_D = −0.3 A; T_{amb} = 25 °C	–	t.b.f.	–	pC
Q_{GD}	gate-drain charge	V_{DD} = −15 V; I_D = −0.3 A; T_{amb} = 25 °C	–	t.b.f.	–	pC
Switching times						
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to −10 V; V_{DD} = −15 V; I_D = −0.3 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
t_r	rise time	V_{GS} = 0 to −10 V; V_{DD} = −15 V; I_D = −0.3 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
t_{on}	turn-on switching time	V_{GS} = 0 to −10 V; V_{DD} = −15 V; I_D = −0.3 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = −10 to 0 V; V_{DD} = −15 V; I_D = −0.3 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
t_f	fall time	V_{GS} = −10 to 0 V; V_{DD} = −15 V; I_D = −0.3 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
t_{off}	turn-off switching time	V_{GS} = −10 to 0 V; V_{DD} = −15 V; I_D = −0.3 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = −0.38 A	–	–	−1.3	V
t_{rr}	reverse recovery time	I_S = −0.5 A; di/dt = 100 A/μs	–	t.b.f.	–	ns

P-channel enhancement mode MOS transistor

BSH204

FEATURES

- High-speed switching
- No secondary breakdown
- Direct interface to C-MOS, TTL, etc.
- Very low threshold.

APPLICATIONS

- 'Glue-logic': interface between logic blocks and/or periphery
- Power management
- DC to DC converters
- General purpose switch
- Battery powered applications.

DESCRIPTION

P-channel enhancement mode MOS transistor in a SOT23 SMD package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	s	source
3	d	drain

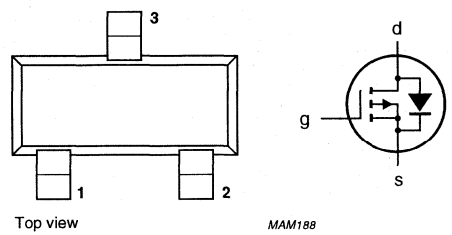


Fig.1 Simplified outline (SOT23) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–12	V
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = –0.38 A	–	–1.3	V
V_{GS}	gate-source voltage (DC)		–	±8	V
V_{GSth}	gate-source threshold voltage	V_{DS} = V_{GS}; I_D = –1 mA	–0.4	–	V
I_D	drain current (DC)	T_s = 80 °C	–	–0.7	A
R_{DSon}	drain-source on-state resistance	V_{GS} = –2.5 V; I_D = –0.4 A	–	0.75	Ω
P_{tot}	total power dissipation	T_s = 80 °C	–	0.5	W

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–12	V
V_{GS}	gate-source voltage (DC)		–	±8	V
I_D	drain current (DC)	T_s = 80 °C; note 1	–	–0.7	A
I_{DM}	peak drain current	note 2	–	–2.8	A
P_{tot}	total power dissipation	T_s = 80 °C	–	0.5	W
		T_{amb} = 25 °C; note 3	–	0.75	W
		T_{amb} = 25 °C; note 4	–	0.54	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–55	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 80 °C	–	–0.38	A
I_{SM}	peak pulsed source current	note 2	–	–1.52	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Device mounted on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
4. Device mounted on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	140	K/W

P-channel enhancement mode MOS transistor

BSH204

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = −10 μA	−12	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = −1 mA	−0.4	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = −9.6 V	–	–	−100	nA
I_{GSS}	gate leakage current	V_{DS} = 0; V_{GS} = ±8 V	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = −4.5 V; I_D = −0.4 A	–	–	0.59	Ω
		V_{GS} = −2.5 V; I_D = −0.4 A	–	–	0.75	Ω
		V_{GS} = −1.8 V; I_D = −0.2 A	–	–	1	Ω
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = −9.6 V; f = 1 MHz	–	t.b.f.	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = −9.6 V; f = 1 MHz	–	t.b.f.	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = −9.6 V; f = 1 MHz	–	t.b.f.	–	pF
Q_G	total gate charge	V_{GS} = −6 V; V_{DD} = −6 V; I_D = −0.4 A; T_{amb} = 25 °C	–	t.b.f.	–	pC
Q_{GS}	gate-source charge	V_{DD} = −6 V; I_D = −0.4 A; T_{amb} = 25 °C	–	t.b.f.	–	pC
Q_{GD}	gate-drain charge	V_{DD} = −6 V; I_D = −0.4 A; T_{amb} = 25 °C	–	t.b.f.	–	pC
Switching times						
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to −6 V; V_{DD} = −6 V; I_D = −0.4 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
t_r	rise time	V_{GS} = 0 to −6 V; V_{DD} = −6 V; I_D = −0.4 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
t_{on}	turn-on switching time	V_{GS} = 0 to −6 V; V_{DD} = −6 V; I_D = −0.4 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = −6 to 0 V; V_{DD} = −6 V; I_D = −0.4 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
t_f	fall time	V_{GS} = −6 to 0 V; V_{DD} = −6 V; I_D = −0.4 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
t_{off}	turn-off switching time	V_{GS} = −6 to 0 V; V_{DD} = −6 V; I_D = −0.4 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = −0.38 A	–	–	−1.3	V
t_{rr}	reverse recovery time	I_S = −0.5 A; di/dt = 100 A/μs	–	t.b.f.	–	ns

P-channel enhancement mode MOS transistor

BSH205

FEATURES

- High-speed switching
- No secondary breakdown
- Direct interface to C-MOS, TTL, etc.
- Very low threshold.

APPLICATIONS

- 'Glue-logic': interface between logic blocks and/or periphery
- Relay driver
- Power switching
- Battery powered applications.

DESCRIPTION

P-channel enhancement mode MOS transistor in a SOT23 SMD package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT23

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	s	source
3	d	drain

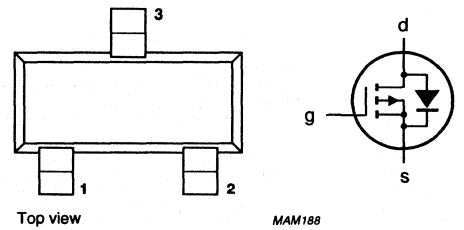


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–12	V
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = –0.5 A	–	–1	V
V_{GS}	gate-source voltage (DC)		–	±8	V
V_{GSth}	gate-source threshold voltage	V_{DS} = V_{GS}; I_D = –1 mA	–0.4	–	V
I_D	drain current (DC)	T_s = 80 °C	–	–1	A
R_{DSon}	drain-source on-state resistance	V_{GS} = –4.5 V; I_D = –0.5 A	–	0.3	Ω
P_{tot}	total power dissipation	T_s = 80 °C	–	0.5	W

P-channel enhancement mode MOS transistor

BSH205

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–12	V
V_{GS}	gate-source voltage (DC)		–	±8	V
I_D	drain current (DC)	T_s = 80 °C; note 1	–	–1	A
I_{DM}	peak drain current	note 2	–	–4	A
P_{tot}	total power dissipation	T_s = 80 °C	–	0.5	W
		T_{amb} = 25 °C; note 3	–	0.75	W
		T_{amb} = 25 °C; note 4	–	0.54	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–55	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 80 °C	–	–0.6	A
I_{SM}	peak pulsed source current	note 2	–	–2.4	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Device mounted on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
4. Device mounted on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	140	K/W

P-channel enhancement mode MOS transistor

BSH205

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = −10 μA	−12	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = −1 mA	−0.4	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = −9.6 V	–	–	−100	nA
I_{GSS}	gate leakage current	V_{GS} = ±8 V; V_{DS} = 0	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = −4.5 V; I_D = −0.5 A	–	–	0.3	Ω
		V_{GS} = −2.5 V; I_D = −0.5 A	–	–	0.38	Ω
		V_{GS} = −1.8 V; I_D = −0.3 A	–	–	0.57	Ω
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = −9.6 V; f = 1 MHz	–	t.b.f.	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = −9.6 V; f = 1 MHz	–	t.b.f.	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = −9.6 V; f = 1 MHz	–	t.b.f.	–	pF
Q_G	total gate charge	V_{GS} = −6 V; V_{DD} = −6 V; I_D = −0.85 A; T_{amb} = 25 °C	–	t.b.f.	–	pC
Q_{GS}	gate-source charge	V_{DD} = −6 V; I_D = −0.85 A; T_{amb} = 25 °C	–	t.b.f.	–	pC
Q_{GD}	gate-drain charge	V_{DD} = −6 V; I_D = −0.85 A; T_{amb} = 25 °C	–	t.b.f.	–	pC
Switching times						
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to −6 V; V_{DD} = −6 V; I_D = −0.85 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
t_r	rise time	V_{GS} = 0 to −6 V; V_{DD} = −6 V; I_D = −0.85 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
t_{on}	turn-on switching time	V_{GS} = 0 to −6 V; V_{DD} = −6 V; I_D = −0.85 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = −6 to 0 V; V_{DD} = −6 V; I_D = −0.85 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
t_f	fall time	V_{GS} = −6 to 0 V; V_{DD} = −6 V; I_D = −0.85 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
t_{off}	turn-off switching time	V_{GS} = −6 to 0 V; V_{DD} = −6 V; I_D = −0.85 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = −0.5 A	–	–	−1	V
t_{rr}	reverse recovery time	I_S = −0.5 A; di/dt = 100 A/μs	–	t.b.f.	–	ns

P-channel enhancement mode MOS transistor

BSH206

FEATURES

- High-speed switching
- No secondary breakdown
- Direct interface to C-MOS, TTL, etc.
- Very low threshold.

APPLICATIONS

- 'Glue-logic': interface between logic blocks and/or periphery
- Relay driver
- Power switching
- Battery powered applications.

DESCRIPTION

P-channel enhancement mode MOS transistor in a SOT363 SMD package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT363

PIN	SYMBOL	DESCRIPTION
1	d	drain
2	d	drain
3	g	gate
4	s	source
5	d	drain
6	d	drain

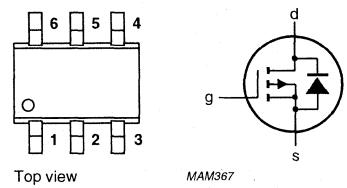


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–12	V
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = –0.5 A	–	–1	V
V_{GS}	gate-source voltage (DC)		–	±8	V
V_{GSth}	gate-source threshold voltage	V_{DS} = V_{GS}; I_D = –1 mA	–0.4	–	V
I_D	drain current (DC)	T_s = 80 °C	–	–1.2	A
R_{DSon}	drain-source on-state resistance	V_{GS} = –4.5 V; I_D = –0.6 A	–	0.36	Ω
P_{tot}	total power dissipation	T_s = 80 °C	–	0.8	W

P-channel enhancement mode MOS transistor

BSH206

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–12	V
V_{GS}	gate-source voltage (DC)		–	±8	V
I_D	drain current (DC)	T_s = 80 °C; note 1	–	–1.2	A
I_{DM}	peak drain current	note 2	–	–4.6	A
P_{tot}	total power dissipation	T_s = 80 °C	–	0.8	W
		T_{amb} = 25 °C; note 3	–	1.1	W
		T_{amb} = 25 °C; note 4	–	0.7	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–55	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 80 °C	–	–1	A
I_{SM}	peak pulsed source current	note 2	–	–4	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Device mounted on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
4. Device mounted on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	87.5	K/W

P-channel enhancement mode MOS transistor

BSH206

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = −10 μA	−12	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = −1 mA	−0.4	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = −9.6 V	–	–	−100	nA
I_{GSS}	gate leakage current	V_{GS} = ±8 V; V_{DS} = 0	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = −4.5 V; I_D = −0.6 A	–	–	0.36	Ω
		V_{GS} = −2.5 V; I_D = −0.6 A	–	–	0.45	Ω
		V_{GS} = −1.8 V; I_D = −0.3 A	–	–	0.67	Ω
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = −9.6 V; f = 1 MHz	–	t.b.f.	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = −9.6 V; f = 1 MHz	–	t.b.f.	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = −9.6 V; f = 1 MHz	–	t.b.f.	–	pF
Q_G	total gate charge	V_{GS} = −6 V; V_{DD} = −6 V; I_D = −0.6 A; T_{amb} = 25 °C	–	t.b.f.	–	pC
Q_{GS}	gate-source charge	V_{DD} = −6 V; I_D = −0.6 A; T_{amb} = 25 °C	–	t.b.f.	–	pC
Q_{GD}	gate-drain charge	V_{DD} = −6 V; I_D = −0.6 A; T_{amb} = 25 °C	–	t.b.f.	–	pC
Switching times						
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to −6 V; V_{DD} = −6 V; I_D = −0.6 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
t_r	rise time	V_{GS} = 0 to −6 V; V_{DD} = −6 V; I_D = −0.6 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
t_{on}	turn-on switching time	V_{GS} = 0 to −6 V; V_{DD} = −6 V; I_D = −0.6 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = −6 to 0 V; V_{DD} = −6 V; I_D = −0.6 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
t_f	fall time	V_{GS} = −6 to 0 V; V_{DD} = −6 V; I_D = −0.6 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
t_{off}	turn-off switching time	V_{GS} = −6 to 0 V; V_{DD} = −6 V; I_D = −0.6 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = −0.5 A	–	–	−1	V
t_{rr}	reverse recovery time	I_S = −0.5 A; di/dt = 100 A/μs	–	t.b.f.	–	ns

P-channel enhancement mode MOS transistor

BSH207

FEATURES

- High-speed switching
- No secondary breakdown
- Direct interface to C-MOS, TTL, etc.
- Very low threshold.

APPLICATIONS

- 'Glue-logic': interface between logic blocks and/or periphery
- Power management
- DC to DC converters
- General purpose switch
- Battery powered applications.

DESCRIPTION

P-channel enhancement mode MOS transistor in a SOT457 (TSOP6) SMD package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING

PIN	SYMBOL	DESCRIPTION
1	d	drain
2	d	drain
3	g	gate
4	s	source
5	d	drain
6	d	drain

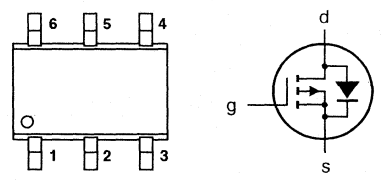


Fig.1 Simplified outline (SOT457) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–12	V
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = –0.6 A	–	–1.3	V
V_{GS}	gate-source voltage (DC)		–	±8	V
V_{GSth}	gate-source threshold voltage	V_{DS} = V_{GS}; I_D = –1 mA	–0.4	–	V
I_D	drain current (DC)	T_s = 80 °C	–	–1.55	A
R_{DSon}	drain-source on-state resistance	V_{GS} = –2.5 V; I_D = –0.82 A	–	0.25	Ω
P_{tot}	total power dissipation	T_s = 80 °C	–	0.8	W

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–12	V
V_{GS}	gate-source voltage (DC)		–	±8	V
I_D	drain current (DC)	T_s = 80 °C; note 1	–	–1.55	A
I_{DM}	peak drain current	note 2	–	–6.2	A
P_{tot}	total power dissipation	T_s = 80 °C; note 1	–	0.8	W
		T_{amb} = 25 °C; note 3	–	1.09	W
		T_{amb} = 25 °C; note 4	–	0.7	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–55	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 80 °C; note 1	–	–0.6	A
I_{SM}	peak pulsed source current	note 2	–	–2.4	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Device mounted on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
4. Device mounted on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	87.5	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = −10 μA	−12	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = −1 mA	−0.4	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = −9.6 V	–	–	−100	nA
I_{GSS}	gate leakage current	V_{DS} = 0; V_{GS} = ±8 V	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = −4.5 V; I_D = −0.82 A	–	–	0.195	Ω
		V_{GS} = −2.5 V; I_D = −0.82 A	–	–	0.25	Ω
		V_{GS} = −1.8 V; I_D = −0.41 A	–	–	0.333	Ω
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = −9.6 V; f = 1 MHz	–	t.b.f.	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = −9.6 V; f = 1 MHz	–	t.b.f.	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = −9.6 V; f = 1 MHz	–	t.b.f.	–	pF
Q_G	total gate charge	V_{GS} = −6 V; V_{DD} = −6 V; I_D = −0.82 A; T_{amb} = 25 °C	–	t.b.f.	–	pC
Q_{GS}	gate-source charge	V_{DD} = −6 V; I_D = −0.82 A; T_{amb} = 25 °C	–	t.b.f.	–	pC
Q_{GD}	gate-drain charge	V_{DD} = −6 V; I_D = −0.82 A; T_{amb} = 25 °C	–	t.b.f.	–	pC
Switching times						
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to −6 V; V_{DD} = −6 V; I_D = −0.82 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
t_r	rise time	V_{GS} = 0 to −6 V; V_{DD} = −6 V; I_D = −0.82 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
t_{on}	turn-on switching time	V_{GS} = 0 to −6 V; V_{DD} = −6 V; I_D = −0.82 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = −6 to 0 V; V_{DD} = −6 V; I_D = −0.82 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
t_f	fall time	V_{GS} = −6 to 0 V; V_{DD} = −6 V; I_D = −0.82 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
t_{off}	turn-off switching time	V_{GS} = −6 to 0 V; V_{DD} = −6 V; I_D = −0.82 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = −0.6 A	–	–	−1.3	V
t_{rr}	reverse recovery time	I_S = −0.5 A; di/dt = 100 A/μs	–	t.b.f.	–	ns

N-channel enhancement mode vertical D-MOS transistor

BSN20W

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

APPLICATIONS

- Thin and thick film circuits
- General purpose fast switching applications.

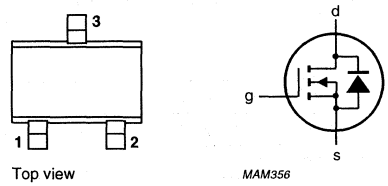
DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a 3 pin plastic SOT323 SMD package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT323

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	s	source
3	d	drain



Marking code: M8t.

Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		50	V
V_{GSth}	gate-source threshold voltage		1.8	V
I_D	drain current (DC)		80	mA
R_{DSon}	drain-source on-state resistance		15	Ω
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C; note 1	200	mW

Note

1. Device mounted on a printed-circuit board.

N-channel enhancement mode vertical D-MOS transistor

BSN20W

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	50	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)		–	80	mA
I_{DM}	peak drain current		–	300	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C; note 1	–	200	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–65	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	625	K/W

Note to the Limiting values and Thermal characteristics

1. Device mounted on a printed-circuit board.

CHARACTERISTICS

$T_j = 25$ °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0$; $I_D = 10$ µA	50	–	–	V
V_{GSth}	gate-source threshold voltage	$V_{GS} = V_{DS}$; $I_D = 1$ mA	0.4	–	1.8	V
I_{DSS}	drain-source leakage current	$V_{GS} = 0$; $V_{DS} = 40$ V	–	–	1	µA
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 20$ V; $V_{DS} = 0$	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10$ V; $I_D = 80$ mA	–	8	15	Ω
		$V_{GS} = 5$ V; $I_D = 80$ mA	–	14	20	Ω
		$V_{GS} = 2.5$ V; $I_D = 10$ mA	–	18	30	Ω
C_{iss}	input capacitance	$V_{GS} = 0$; $V_{DS} = 10$ V; $f = 1$ MHz	–	8	15	pF
C_{oss}	output capacitance	$V_{GS} = 0$; $V_{DS} = 10$ V; $f = 1$ MHz	–	7	15	pF
C_{rss}	reverse transfer capacitance	$V_{GS} = 0$; $V_{DS} = 10$ V; $f = 1$ MHz	–	2	5	pF
Switching times						
t_{on}	turn-on time	$V_{GS} = 0$ to 10 V; $V_{DD} = 20$ V; $I_D = 80$ mA	–	2	5	ns
t_{off}	turn-off time	$V_{GS} = 10$ to 0 V; $V_{DD} = 20$ V; $I_D = 80$ mA	–	5	10	ns

N-channel enhancement mode vertical D-MOS transistor

BSP030

FEATURES

- High speed switching
- No secondary breakdown
- Very low on-state resistance.

APPLICATIONS

- Motor and actuator drivers
- Power management
- Synchronized rectification.

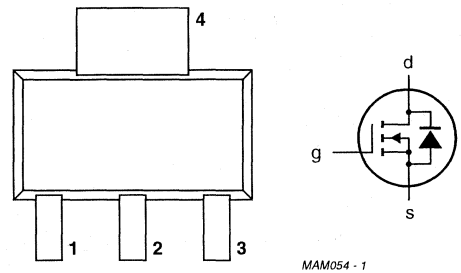
DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a 4-pin plastic SOT223 SMD package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT223

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	d	drain
3	s	source
4	d	drain



Top view

Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	30	V
V_{SD}	source-drain diode forward voltage	I_S = 1.25 A	–	1	V
V_{GS}	gate-source voltage (DC)		–	±20	V
V_{GSth}	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}	1	2.8	V
I_D	drain current (DC)	T_s = 100 °C	–	10	A
R_{DSon}	drain-source on-state resistance	I_D = 5 A; V_{GS} = 10 V	–	0.03	Ω
P_{tot}	total power dissipation	T_s = 100 °C	–	5	W

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	30	V
V_{GS}	gate-source voltage (DC)		–	±20	V
I_D	drain current (DC)	T_s = 100 °C; note 1	–	10	A
I_{DM}	peak drain current	note 2	–	40	A
P_{tot}	total power dissipation	T_s = 100 °C	–	5	W
		T_{amb} = 25 °C; note 3	–	3.3	W
		T_{amb} = 25 °C; note 4	–	1.25	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–65	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 100 °C	–	5	A
I_{SM}	peak pulsed source current	note 2	–	20	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Value based on printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
4. Value based on printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

P-channel enhancement mode vertical D-MOS transistor

BSP090

FEATURES

- High speed switching
- No secondary breakdown
- Very low on-state resistance.

APPLICATIONS

- Motor and actuator drivers
- Power management
- Synchronized rectification.

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a 4-pin plastic SOT223 SMD package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT223

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	d	drain
3	s	source
4	d	drain

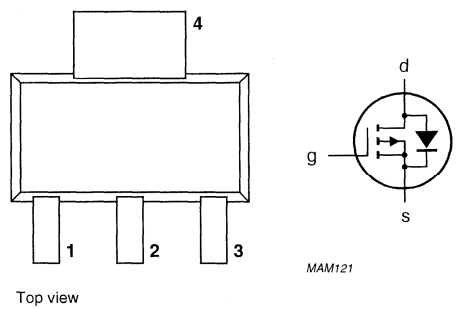


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–30	V
V_{SD}	source-drain diode forward voltage	I_S = –1.25 A	–	–1.3	V
V_{GS}	gate-source voltage (DC)		–	±20	V
V_{GSth}	gate-source threshold voltage	I_D = –1 mA; V_{DS} = V_{GS}	–1	–2.8	V
I_D	drain current (DC)	T_s = 100 °C	–	–5.7	A
R_{DSon}	drain-source on-state resistance	I_D = –2.8 A; V_{GS} = –10 V	–	0.09	Ω
P_{tot}	total power dissipation	T_s = 100 °C	–	5	W

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–30	V
V_{GS}	gate-source voltage (DC)		–	±20	V
I_D	drain current (DC)	T_s = 100 °C; note 1	–	–5.7	A
I_{DM}	peak drain current	note 2	–	–22	A
P_{tot}	total power dissipation	T_s = 100 °C	–	5	W
		T_{amb} = 25 °C; note 3	–	3.3	W
		T_{amb} = 25 °C; note 4	–	1.25	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–65	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 100 °C	–	–3.8	A
I_{SM}	peak pulsed source current	note 2	–	–15	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Device mounted on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
4. Device mounted on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

GSM 4 W power amplifier CGY2013G

FEATURES

- Power Amplifier (PA) overall efficiency 45%
- 35.5 dB gain
- 0 dBm input power
- Gain control range >55 dB
- Integrated power sensor driver
- Low output noise floor of PA < −129 dBm/Hz in GSM RX band
- Wide operating temperature range −20 to +85 °C
- LQFP 48 pin package
- Compatible with power ramping controller PCA5075
- Compatible with GSM RF transceiver SA1620.

APPLICATIONS

- 880 to 915 MHz hand-held transceivers for E-GSM applications
- 900 MHz Time Division Multiple Access (TDMA) systems.

GENERAL DESCRIPTION

The CGY2013G is a GSM class 4 GaAs Monolithic Microwave Integrated Circuit (MMIC) power amplifier specifically designed to operate at 3.6 V battery supply. The IC also includes a power sensor driver so that no directional coupler is required in the power control loop.

The PA requires only a 30 dB harmonic low-pass filter to comply with the GSM transmit spurious specification. It can be switched off and its power controlled by monitoring the actual drain voltage applied to the amplifier stages.

QUICK REFERENCE DATA

SYMBOL	PARAMETER (1)	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive supply voltage	–	3.3	–	V
I_{DD}	positive peak supply current	–	2.4	–	A
$P_{o(max)}$	maximum output power	–	35.5	–	dBm
T_{amb}	operating ambient temperature	−20	–	+85	°C

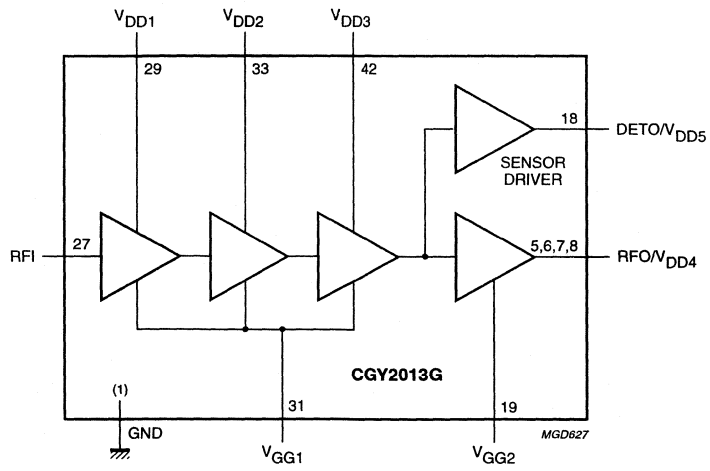
Note

1. For conditions, see Chapters "AC characteristics" and "DC characteristics".

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
CGY2013G	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

BLOCK DIAGRAM



(1) Ground pins 1 to 4, 9 to 17, 20 to 26, 28, 30, 32, 34 to 41 and 43 to 48.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
GND	1 to 4	ground
RFO/V_{DD4}	5 to 8	power amplifier output and fourth stage supply voltage
GND	9 to 17	ground
DETO/V_{DD5}	18	power sensor output and supply voltage
V_{GG2}	19	fourth stage negative gate supply voltage
GND	20 to 26	ground
RFI	27	power amplifier input
GND	28	ground
V_{DD1}	29	first stage supply voltage
GND	30	ground
V_{GG1}	31	first three stages negative gate supply voltage
GND	32	ground
V_{DD2}	33	second stage supply voltage
GND	34 to 41	ground
V_{DD3}	42	third stage supply voltage
GND	43 to 48	ground

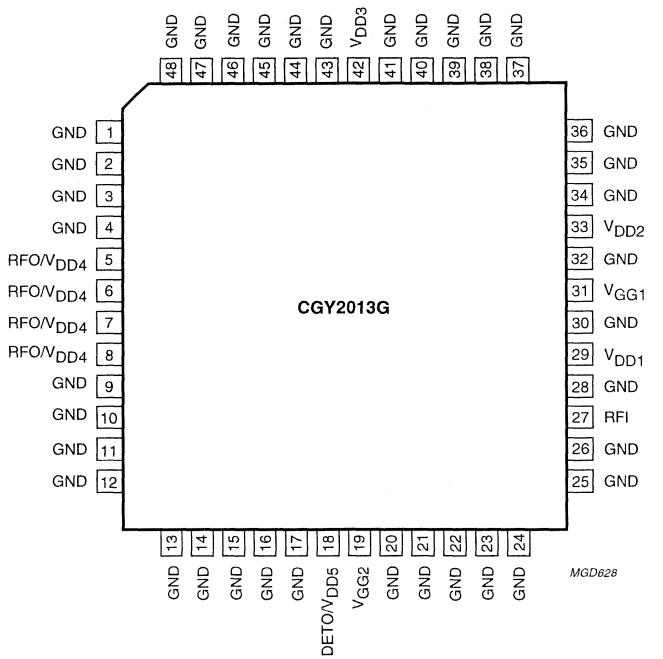


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Operating conditions

The CGY2013G is designed to meet the European Telecommunications Standards Institute (ETSI) GSM documents, the *"ETS 300 577 specification"*, which are defined as follows:

- t_{on} = 542.8 µs
- T = 4.3 ms
- Duty cycle = 1/8.

The device is specifically designed for pulse operation allowing the use of a LQFP48 plastic package.

Power amplifier

The power amplifier consists of four cascaded gain stages with an open-drain configuration. Each drain has to be loaded externally by an adequate reactive circuit which also has to be a DC path to the supply.

The amplifier bias is set using a negative voltage applied at pins V_{GG1} and V_{GG2}. This negative voltage must be present before the supply voltage is applied to the drains to avoid current overstress for the amplifier.

Power sensor driver

The power sensor driver is a buffer amplifier that delivers a signal to the DETO output pin which is proportional to the amplifier power. This signal can be detected by external diodes for power control purpose. As the sensor signal is taken from the input of the last stage of the PA, it is isolated from disturbances at the output by the reverse isolation of the PA output stage.

An impedance mismatch at the PA output therefore, does not significantly influence the signal delivered by the power sensor as this normally occurs when power sense is made using a directional coupler. Consequently the cost and space of using a directional coupler are saved.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); general operating conditions applied.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	positive supply voltage	–	7	V
V_{GG}	negative supply voltage	–	–10	V
$T_{j(max)}$	maximum operating junction temperature	–	150	°C
T_{stg}	IC storage temperature	–	150	°C
P_{tot}	total power dissipation	–	1.5	W

THERMAL CHARACTERISTICS

General operating conditions applied.

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}c}$	thermal resistance from junction to case; note 1	32	K/W

Note

1. This thermal resistance is measured under GSM pulse conditions.

DC CHARACTERISTICS

V_{DD} = 3.3 V; T_{amb} = 25 °C; general operating conditions applied; peak current values during burst; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pins RFO/V_{DD4}, V_{DD3}, V_{DD2}, V_{DD1} and DETO/V_{DD5}						
V_{DD}	positive supply voltage		0	3.3	5.5	V
I_{DD}	positive peak supply current		–	2.4	3.0	A
Pins V_{GG1} and V_{GG2}						
V_{GG1}	negative supply voltage	note 1	–	–2	–	V
V_{GG2}	negative supply voltage	note 1	–	–2	–	V
I_{GG1} + I_{GG2}	negative peak supply current		–	2.5	5	mA

Note

1. The negative bias V_{GG1} and V_{GG2} must be applied 10 µs before the power amplifier is switched on, and must remain applied until the power amplifier has been switched off.

AC CHARACTERISTICS

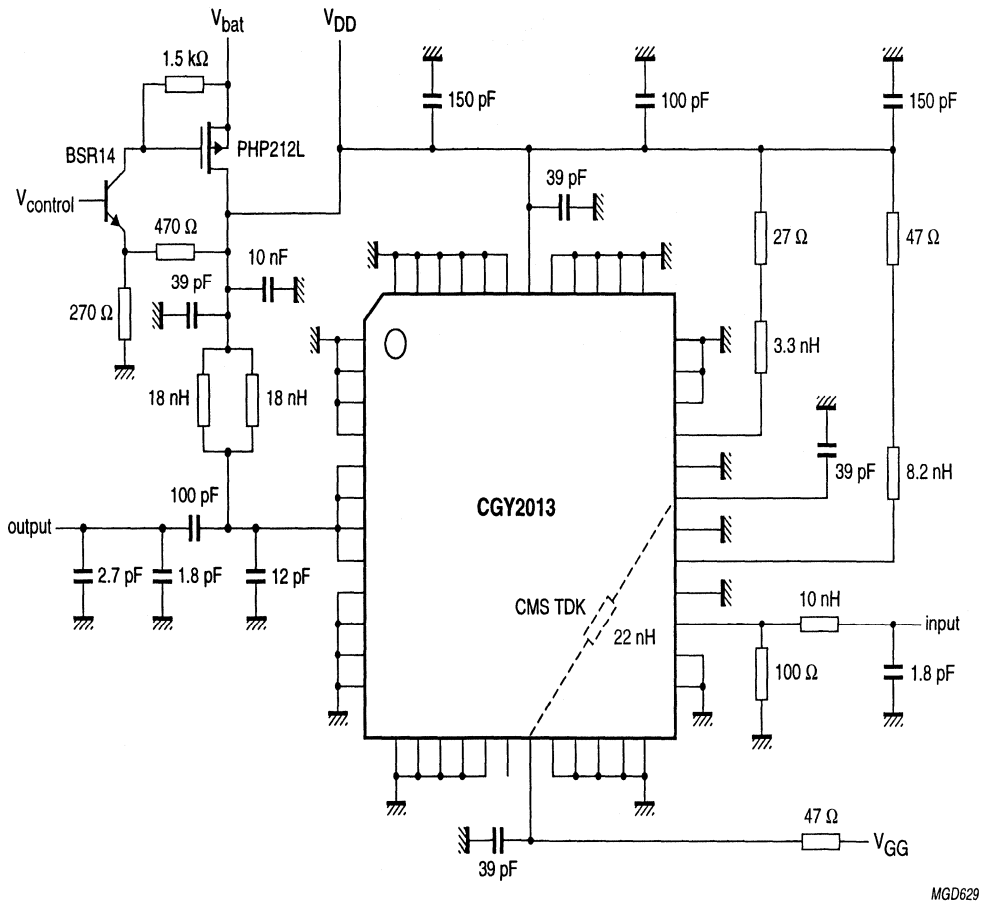
V_{DD} = 3.3 V; T_{amb} = 25 °C; general operating conditions applied; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power amplifier						
P_i	input power		−1.5	–	+1.5	dBm
S_{11}	input return loss	note 1; 50 Ω source	–	–	−6	dB
f_{RF}	RF frequency range		880	–	915	MHz
$P_{o(max)}$	maximum output power	T_{amb} = 25 °C; V_{DD} = 3.3 V	34.5	35.5	–	dBm
		T_{amb} = −20 to +85 °C; V_{DD} = 2.9 V	32.5	–	–	dBm
η	efficiency	V_{DD} = 2.9 V	–	45	–	%
$P_{o(min)}$	minimum output power	V_{DD} < 0.1 V	–	–	−20	dBm
N_{RX}	output noise in RX band	f_{RF} = 925 MHz at $P_{o(max)}$	–	–	−117	dBm/Hz
		f_{RF} = 935 MHz at $P_{o(max)}$	–	–	−129	dBm/Hz
		f_{RF} = 960 MHz at $P_{o(max)}$	–	–	−129	dBm/Hz
H2	2nd harmonic level		–	−33	−30	dBc
H3	3rd harmonic level		–	−40	−37	dBc
Stab	stability	note 2	–	–	−70	dBc
Power sensor driver						
$P_{o(DET)}$	sensor driver output power	R_L = 100 Ω; relative to PA output power into 50 Ω load	–	−23	–	dBc
$\Delta P_{o(DET)}$	driver output power variation	load VSWR < 6 : 1 at PA output	–	–	2	dB

Notes

1. Including the 100 Ω resistor connected in parallel at the power amplifier input on the evaluation board.
2. The device is adjusted to provide nominal value of load power into a 50 Ω load. The device is switched off and a 6 : 1 load replaces the 50 Ω load. The device is switched on and the phase of the 6 : 1 load is varied 360 electrical degrees during a 60 second period.

APPLICATION INFORMATION



(1) These capacitors are type: SMD0402; rest of the capacitors: SMD0603.
(2) TRL1: width: 0.3 mm; length: 16 mm.
(3) TRL2: width: 0.3 mm; length: 6.3 mm.
(4) TRL3: width: 0.3 mm; length: 20 mm.

Fig.3 Evaluation board schematic (FR4, 0.8 mm).

DCS/PCS 2 W power amplifier CGY2021G

FEATURES

- Power Amplifier (PA) overall efficiency 50% (DCS)
- 34 dB gain
- 0 dBm input power
- Gain control range >50 dB
- Integrated power sensor driver
- Low output noise floor of PA <–121 dBm/Hz in DCS/PCS RX band
- Wide operating temperature range –20 to +85 °C
- LQFP 48-pin package
- Compatible with power ramping controller PCA5077 and GaAs PA power modulator UBA1710.

APPLICATIONS

- Hand-held transceivers for DCS/PCS applications (DCS: 1710 to 1785 MHz and PCS: 1850 to 1910 MHz)
- 1800 MHz Time Division Multiple Access (TDMA) systems.

GENERAL DESCRIPTION

The CGY2021G is a DCS/PCS class 1 GaAs Monolithic Microwave Integrated Circuit (MMIC) power amplifier specifically designed to operate at 4.8 V battery supply.

The chip also includes a power sensor driver so that no directional coupler is required in the power control loop.

The PA requires only a simple low-pass filter to comply with the DCS/PCS transmit spurious specification. It can be switched off and its power controlled by monitoring the actual drain voltage applied to the amplifier stages.

QUICK REFERENCE DATA

SYMBOL	PARAMETER[1]	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive supply voltage	–	4.5	–	V
I_{DD}	positive peak supply current	–	1.4	–	A
$P_{o(max)}$	maximum output power	–	34	–	dBm
T_{amb}	operating ambient temperature	–20	–	+85	°C

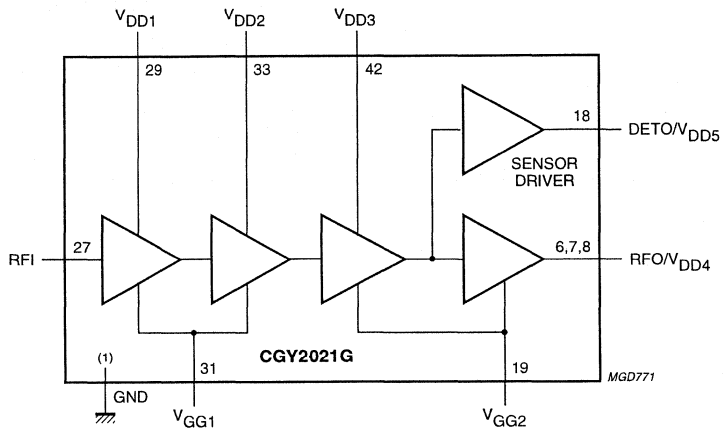
Note

1. For conditions, see Chapters "AC characteristics" and "DC characteristics".

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
CGY2021G	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

BLOCK DIAGRAM



(1) Ground pins 1 to 5, 9 to 17, 20 to 26, 28, 30, 32, 34 to 41 and 43 to 48.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
GND	1 to 5	ground
RFO/V_{DD4}	6 to 8	PA output and fourth stage supply voltage
GND	9 to 17	ground
DETO/V_{DD5}	18	power sensor output and supply voltage
V_{GG2}	19	third and fourth stage negative gate supply voltage
GND	20 to 26	ground
RFI	27	PA input
GND	28	ground
V_{DD1}	29	first stage supply voltage
GND	30	ground
V_{GG1}	31	first and second stage negative gate supply voltage
GND	32	ground
V_{DD2}	33	second stage supply voltage
GND	34 to 41	ground
V_{DD3}	42	third stage supply voltage
GND	43 to 48	ground

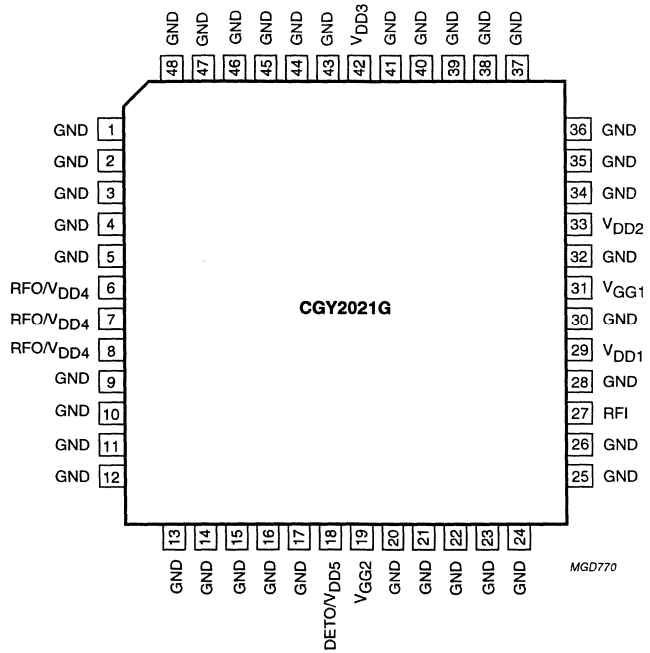


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Operating conditions

The CGY2021G is designed to meet the European Telecommunications Standards Institute (ETSI) DCS documents, the ETS 300 577 specification, which are defined as follows:

- t_{on} = 542.8 µs
- T = 4.3 ms
- Duty cycle = 1/8.

This amplifier is specifically designed for pulse operation allowing the use of a LQFP48 plastic package.

Power amplifier

The Power Amplifier (PA) consists of four cascaded gain stages with an open-drain configuration. Each drain has to be loaded externally by an adequate reactive circuit which also has to be a DC path to the supply.

The amplifier bias is set by using a negative voltage applied at pins V_{GG1} and V_{GG2}. This negative voltage must be present before the supply voltage is applied to the drains to avoid current overstress of the amplifier.

Power sensor driver

The power sensor driver is a buffer amplifier that delivers an output signal at the DETO pin which is proportional to the amplifier power. This signal can be detected by external diodes for power control purpose. As the sensor signal is taken from the input of the last stage of the PA, it is isolated from disturbances at the output by the reverse isolation of the PA output stage. An impedance mismatch at the PA output therefore does not significantly influence the signal delivered by the power sensor as this normally occurs when power sense is made using a directional coupler. Consequently, the cost and space of using a directional coupler are saved.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); general operating conditions applied.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	positive supply voltage	–	7	V
V_{GG}	negative supply voltage	–	−10	V
$T_{j(max)}$	maximum operating junction temperature	–	150	°C
T_{stg}	IC storage temperature	–	150	°C
P_{tot}	total power dissipation	–	1.3	W

THERMAL CHARACTERISTICS

General operating conditions applied.

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}c}$	thermal resistance from junction to case; note 1	45	K/W

Note

1. This thermal resistance is a typical value and is measured under DCS/PCS pulse conditions.

DC CHARACTERISTICS

V_{DD} = 4.5 V; T_{amb} = 25 °C; peak current values during burst; general operating conditions applied; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pins RFO/V_{DD4}, V_{DD3}, V_{DD2}, V_{DD1} and DETO/V_{DD5}						
V_{DD}	positive supply voltage		–	4.5	–	V
I_{DD}	positive peak supply current		–	1.4	–	A
Pins V_{GG1} and V_{GG2}						
V_{GG1}	negative supply voltage	note 1	–	−1.6	–	V
V_{GG2}	negative supply voltage	note 1	–	−1.6	–	V
$I_{GG1} + I_{GG2}$	negative peak supply current		–	–	2	mA

Note

1. The negative bias V_{GG} must be applied 10 µs before the power amplifier is switched on, and must remain applied until the power amplifier has been switched off.

AC CHARACTERISTICS

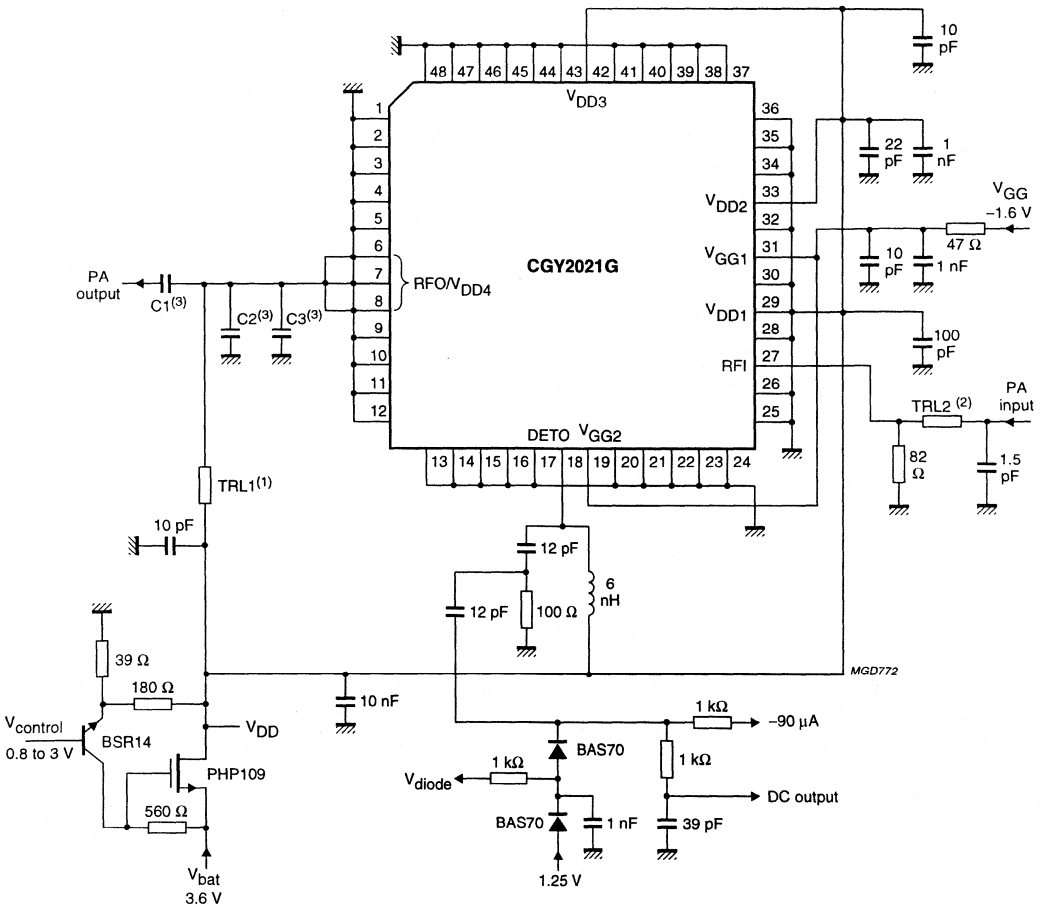
V_{DD} = 4.5 V; T_{amb} = 25 °C; general operating conditions applied; unless otherwise specified.
Measured and guaranteed on CGY2021G evaluation board.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power amplifier						
P_i	input power		–2	–	+2	dBm
S_{11}	input return loss	50 Ω source; note 1	–	–	–10	dB
f_{RF}	RF frequency range	DCS	1710	–	1785	MHz
		PCS	1850	–	1910	MHz
$P_{o(max)}$	maximum output power	T_{amb} = 25 °C; V_{DD} = 4.5 V	33	34	–	dBm
		T_{amb} = –20 to +85 °C; V_{DD} = 4.2 V	31	–	–	dBm
η	efficiency	DCS; at $P_{o(max)}$	40	50	–	%
		PCS; at $P_{o(max)}$	–	47	–	%
R_S	optimum series load resistance		–	6	–	Ω
C_S	optimum series load capacitance		–	11	–	pF
$P_{o(off)}$	isolation	PA OFF; P_i = 0 dBm	–	–50	–	dBm
N_{RX}	output noise in RX band		–	–	–121	dBm/Hz
H2	2nd harmonic level		–	–40	–	dBc
H3	3rd harmonic level		–	–35	–	dBc
Stab	stability	note 2	–	–	–50	dBc
Power sensor driver						
$P_{o(DET)}$	sensor driver output power	R_L = 100 Ω; relative to PA output power into 50 Ω load	–	–25	–	dBc

Notes

1. Including the 82 Ω resistor connected in parallel at the power amplifier input on the evaluation board.
2. The device is adjusted to provide nominal value of load power into a 50 Ω load. The device is switched off and a 6 : 1 load replaces the 50 Ω load. The device is switched on and the phase of the 6 : 1 load is varied 360 electrical degrees during a 60 seconds test period.

APPLICATION INFORMATION



All capacitors are type: SMD0603.
Thickness: 0.8 mm; substrate: FR4; $\varepsilon_r = 4.7$.
(1) TRL1: width = 0.3 mm; length = 16 mm.
(2) TRL2: width = 0.5 mm; length = 10 mm.
(3) the component values are:

SYSTEM	C1 (pF)	C2 (pF)	C3 (pF)
DCS	2.2	1.8	2.2
PCS	1.5	1.8	1.2

Fig.3 Evaluation board schematic.

DECT 500 mW power amplifier CGY2030M

FEATURES

- Power Amplifier (PA) overall efficiency 40%
- 27 dB gain
- 0 dBm input power
- Operation possible without negative supply
- Wide operating temperature range –30 to +85 °C
- SSOP16 package.

GENERAL DESCRIPTION

The CGY2030M is a GaAs Monolithic Microwave Integrated Circuit (MMIC) power amplifier specifically designed to operate at 3.6 V battery supply. When power control is not required, it can be operated without negative supply voltage.

APPLICATIONS

- 1.88 to 1.9 GHz transceivers for DECT applications
- 2 GHz transceivers (PHS, DCS).

QUICK REFERENCE DATA

SYMBOL	PARAMETER (1)	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive supply voltage	–	3.2	–	V
I_{DD}	positive peak supply current	–	400	–	mA
P_o	output power	–	27	–	dBm
T_{amb}	operating ambient temperature	–30	–	+85	°C

Note

1. For conditions, see Chapters "AC characteristics" and "DC characteristics".

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
CGY2030M	SSOP16	plastic shrink small outline package; 16 leads; body width 4.4 mm	SOT369-1

BLOCK DIAGRAM

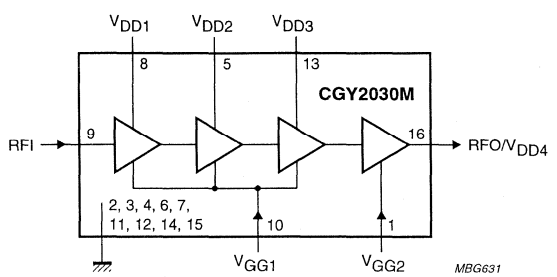


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{GG2}	1	fourth stage negative gate supply voltage
GND	2 to 4	ground
V_{DD2}	5	second stage supply voltage
GND	6 and 7	ground
V_{DD1}	8	first stage supply voltage
RFI	9	PA input
V_{GG1}	10	first second and third stages negative gate supply voltage
GND	11 and 12	ground
V_{DD3}	13	third stage supply voltage
GND	14 and 15	ground
RFO/V_{DD4}	16	PA output and fourth stage supply voltage

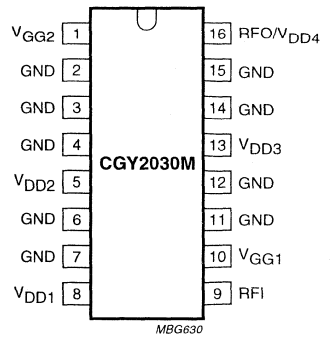


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Amplifier

The CGY2030M is a 4-stage GaAs MESFET power amplifier capable of delivering 500 mW (typ.) at 1.9 GHz into a 50 Ω load. Each amplifier stage has an open-drain configuration. The drains have to be loaded externally by adequate reactive circuits which must also provide a DC path to the supply.

The amplifier can be switched off by means of an external PNP series switch connected between the battery and the amplifier drains. This switch can also be used to vary the actual supply voltage applied to the amplifier and hence, control the output power.

This device is specifically designed to work with a maximum duty factor of 25%.

Biasing

Two modes of operation are possible:

- Mode 1
- Mode 2.

MODE 1

In the first mode, the pins V_{GG1} and V_{GG2} are simply connected together to the ground via resistors (10 kΩ in the evaluation board; see Fig.4). The amplifier biases itself internally to a negative voltage by action of the incoming RF signal. In this mode, power control cannot be achieved by varying the amplifier supply voltage; therefore it is suitable only for applications where power control is not required such as DECT.

MODE 2

If a negative bias is available, a second mode of operation is possible, in which the amplifier is biased by providing adequate negative voltages at pins V_{GG1} and V_{GG2}. In this mode, the amplifier internal bias does not depend on the incoming RF level, nor on the drain voltage, so that power control is possible by variation of the supply voltage.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	operating supply voltage		–	–	5.2	V
$V_{DD} - V_{GG}$	voltage difference between supply voltage and gate bias voltage	no input signal	–	–	8	V
$T_{j(max)}$	maximum operating junction temperature		–	–	150	°C
P_{tot}	total power dissipation		–	–	400	mW
T_{stg}	IC storage temperature		–55	–	+125	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	145	K/W

HANDLING

Do not operate or store near strong electrostatic fields. Meets class 1 ESD test requirements [Human Body Model (HBM)], in accordance with *"MIL STD 883C - method 3015"*.

DC CHARACTERISTICS

V_{DD} = 3.2 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pins RFO/V_{DD4}, V_{DD3}, V_{DD2} and V_{DD1}						
V_{DD}	positive supply voltage		2.6	3.2	4.2	V
I_{DD}	positive peak supply current		–	400	500	mA
Pins V_{GG1} and V_{GG2}; in mode 2						
V_{GG1}	bias voltage for input stages	note 1	–	–1.2	–	V
V_{GG2}	bias voltage for output stage	note 1	–	–2.0	–	V
$I_{GG(tot)}$	total gate peak current	note 2	–1	–	+1	mA

Notes

1. Negative voltages V_{GG1} and V_{GG2} must be applied before supply voltage V_{DD}.
2. Due to non linear effects at high power levels, the gate current can be either negative or positive.

AC CHARACTERISTICS

V_{DD} = 3.2 V; f_{RF} = 1900 MHz; P_i = 0 dBm; T_{amb} = 25 °C; duty factor δ = 25%; 50 Ω impedance system; measured and guaranteed on CGY2030M evaluation board (see Fig.4).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_i	input power	note 1	–3	–	+5	dBm
δ	duty factor		–	–	25	%
f_{RF}	operating frequency		–	1900	–	MHz
Measured in mode 1; without negative biasing; V_{GG1} and V_{GG2} connected to ground						
P_o	output power		26	27	28.5	dBm
η	efficiency		–	40	–	%
P_{leak}	RF leakage to output in power off state	V_{DD} = 0 V	–	–40	–	dBm
H2, H3	second and third harmonics level		–	–35	–	dBc
Stab	stability (spurious levels)	note 2	–	–60	–	dBc
Measured in mode 2; with negative biasing at pins V_{GG1} and V_{GG2}						
P_o	output power		25.5	26.5	28	dBm
η	efficiency		–	35	–	%
P_{leak}	RF leakage to output in power off state	V_{DD} = 0 V	–	–50	–	dBm

Notes

1. Self biasing guaranteed in mode 1 at minimum input power (–3 dBm) and minimum supply voltage V_{DD} (2.6 V).
2. The device is adjusted to provide nominal value of load power into a 50 Ω load. The device is switched off and a 6 : 1 load replaces the 50 Ω load. The device is switched on and the phase of the 6 : 1 load is varied 360 electrical degrees during a 60 seconds test period.

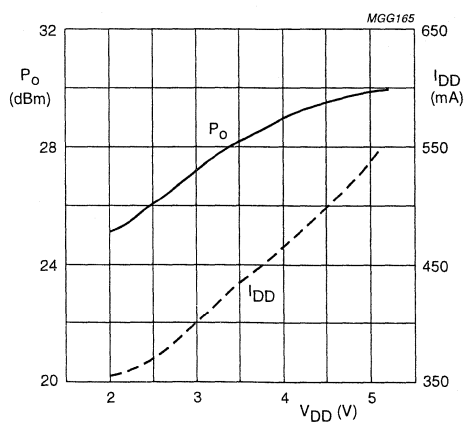
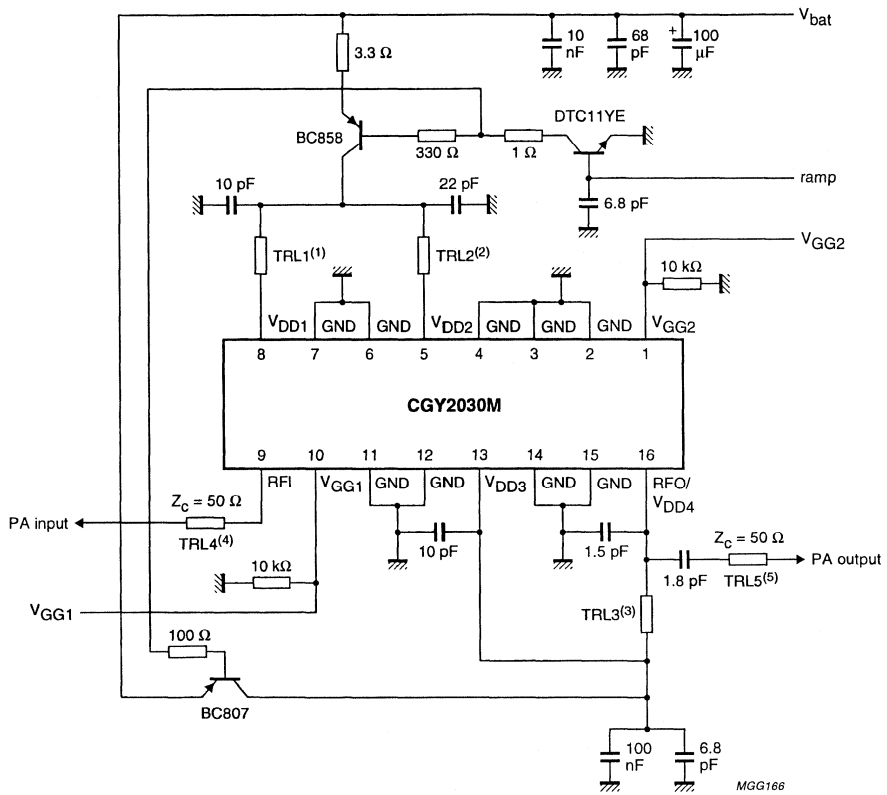


Fig.3 Typical power and current characteristics in mode 1.

APPLICATION INFORMATION

The CGY2030M is operated and tested in accordance with the circuit diagram shown in Fig.4. Supply voltage switching is achieved by two bipolar PNP transistors. One transistor switches the first and second stages and the other switches the third and fourth stages.

By switching on the last amplifier stages with some delay compared to the first stages, it is possible to get the last stages already self-biased before their supply voltage has reached its steady state value. This enables smooth power up-ramping without any power overshoot. A simpler drain switching circuit can be used if the amplifier is operated with negative biasing of the pins V_{GG1} and V_{GG2}.



Thickness: 0.8 mm; substrate: FR4; $\varepsilon_r = 4.7$.

(1) TRL1: width = 500 µm; length = 11200 µm.
(2) TRL2: width = 500 µm; length = 7770 µm.
(3) TRL3: width = 300 µm; length = 15450 µm.
(4) TRL4: width = 1600 µm; length = 12000 µm.
(5) TRL5: width = 1600 µm; length = 11000 µm.

Fig.4 Evaluation board schematic.

DECT 500 mW power amplifier CGY2032TS

FEATURES

- Power Amplifier (PA) overall efficiency 50%
- 27 dBm saturated output power
- 0 dBm input power
- 40 dB linear gain
- Operation without negative supply
- Wide operating temperature range –30 to +85 °C
- SSOP16 package.

APPLICATIONS

- 1.88 to 1.9 GHz transceivers for DECT applications
- 2 GHz transceivers (PHS, DCS and PCS).

GENERAL DESCRIPTION

The CGY2032TS is a GaAs Monolithic Microwave Integrated Circuit (MMIC) power amplifier specifically designed to operate from 3.6 V battery supply. No negative supply voltage is required for operation.

QUICK REFERENCE DATA

SYMBOL	PARAMETER[1]	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive supply voltage	–	3.2	–	V
I_{DD}	positive peak supply current	–	300	–	mA
P_o	output power	–	27	–	dBm
T_{amb}	operating ambient temperature	–30	–	+85	°C

Note

1. For conditions, see Chapters "AC characteristics" and "DC characteristics".

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
CGY2032TS	SSOP16	plastic shrink small outline package; 16 leads; body width 4.4 mm	SOT369-1

BLOCK DIAGRAM

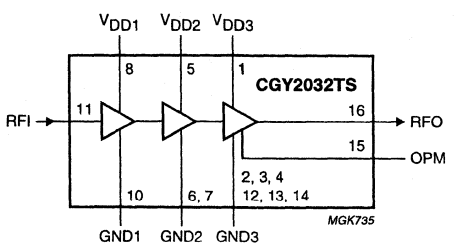


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{DD3}	1	third stage supply voltage
GND3	2 to 4 and 12 to 14	third stage ground
V_{DD2}	5	second stage supply voltage
GND2	6 and 7	second stage ground
V_{DD1}	8	first stage supply voltage
n.c.	9	not connected
GND1	10	first stage ground
RFI	11	PA input
OPM	15	output pre-matching
RFO	16	PA output

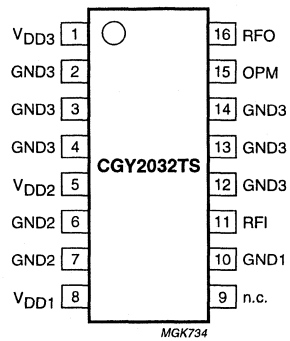


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Amplifier

The CGY2032TS is a 3-stage GaAs power amplifier capable of delivering 500 mW (typ.) at 1.9 GHz into a 50 Ω load. Each amplifier stage has an open-drain configuration. The drains have to be loaded externally by adequate reactive circuits which must also provide a DC path to the supply.

The amplifier can be switched off by means of a single external PNP or PMOS series switch connected between the battery and the amplifier drains. This switch can also be used to vary the actual supply voltage applied to the amplifier and hence, control the output power.

This device is specifically designed to work with a duty factor of 50% and can work up to 100% with good thermal performance PCBs.

Biasing

Internal biasing is provided inside the amplifier for class AB operation.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	operating supply voltage		–	5.2	V
$T_{j(max)}$	maximum operating junction temperature		–	150	°C
P_{tot}	total power dissipation	note 1	–	400	mW
P_i	input power		–	15	dBm
T_{stg}	storage temperature		–55	+125	°C

Note

1. On Philips evaluation board, P_{tot} maximum value is 700 mW.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air; note 1	145	K/W

Note

1. On Philips evaluation board, $R_{th(j-a)}$ value is typically 80 K/W.

HANDLING

Do not operate or store near strong electrostatic fields. Meets class 1 ESD test requirements [Human Body Model (HBM)], in accordance with *"MIL STD 883C - method 3015"*.

DC CHARACTERISTICS

V_{DD} = 3.2 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Pins V_{DD1}, V_{DD2} and V_{DD3}					
V_{DD}	positive supply voltage	1.0	3.2	4.2	V
I_{DD}	positive peak supply current	–	300	400	mA

AC CHARACTERISTICS

V_{DD} = 3.2 V; f_{RF} = 1900 MHz; P_i = 0 dBm; T_{amb} = 25 °C; duty factor δ = 50%; 50 Ω impedance system; measured and guaranteed on CGY2032TS evaluation board (see Fig.5).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_i	input power		–5	0	+5	dBm
δ	duty factor		–	50	100	%
P_o	output power		25	27	28	dBm
η	efficiency		–	50	–	%
P_{leak}	RF leakage to output in power off state	V_{DD} = 0 V	–35	–40	–	dBm
H2	second harmonic level		–	–	–35	dBc
H3	third harmonic level		–	–	–30	dBc
Stab	stability (spurious levels)	note 1	–	–60	–	dBc

Note

1. The device is adjusted to provide nominal value of load power into a 50 Ω load. The device is switched off and a 6 : 1 load replaces the 50 Ω load. The device is switched on and the phase of the 6 : 1 load is varied 360 electrical degrees during a 60 seconds test period.

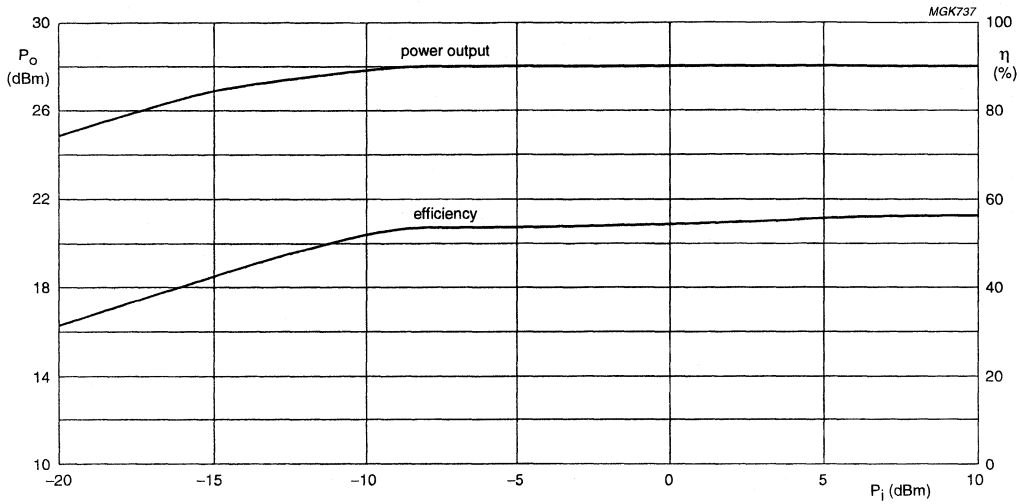


Fig.3 Typical output power and efficiency versus input power.

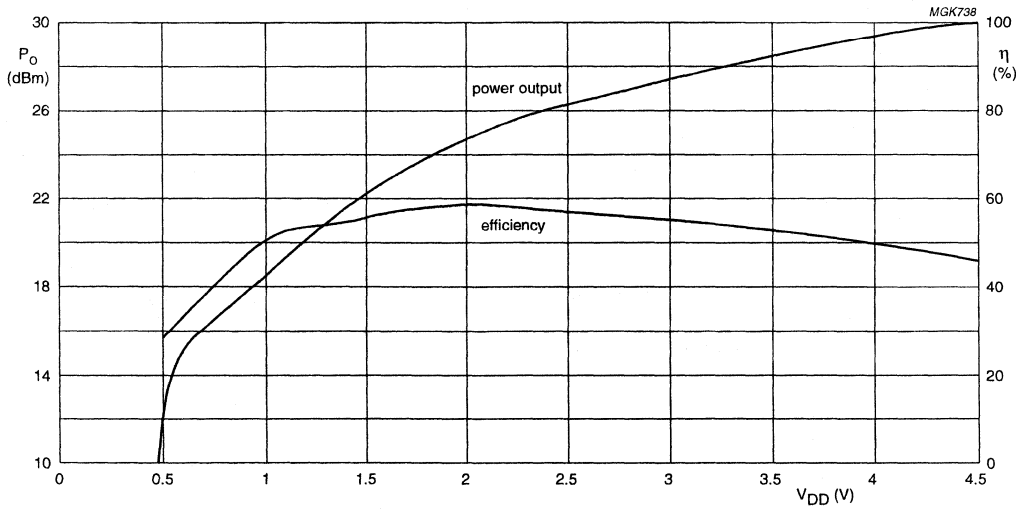
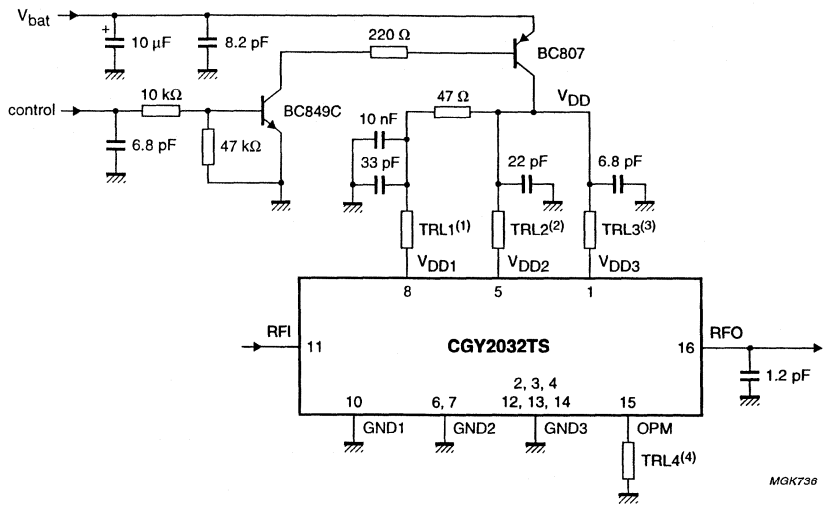


Fig.4 Typical output power and efficiency versus supply voltage.

APPLICATION INFORMATION

The CGY2032TS is operated and tested in accordance with the circuit diagram shown in Fig.5. Supply voltage switching is achieved by a single bipolar PNP transistor.



Thickness: 0.8 mm; substrate: FR4; ε_r = 4.7.
(1) TRL1: width = 500 µm; length = 9000 µm.
(2) TRL2: width = 500 µm; length = 3000 µm.
(3) TRL3: width = 500 µm; length = tbf µm.
(4) TRL4: adjusted for optimum matching.

Fig.5 Evaluation board circuit diagram.

Digital post-detection filter for FSK data receivers

OM4031T

FEATURES

- External clock frequency 30 to 80 kHz (typ. 38.4 kHz)
- Supported data rates 600, 1200, 2400 and 4800 bits/s (typ.)
- Double bandwidth option (not for 4800 bits/s)
- Schmitt-triggered inputs for optimum slope tolerance
- Enable input for power-down mode
- Open-drain output (3-state in power-down mode)
- No external components required
- Single supply voltage from 1.8 to 6.0 V
- Very low operating current (1.5 μA typ.)
- Operating temperature from −10 to +70 °C.

APPLICATIONS

- Telemetry data receivers
- RF security systems
- Low-bit-rate radio data links
- Paging applications of UAA2080 and UAA2082 with software decoding.

GENERAL DESCRIPTION

The OM4031T is intended for performance enhancement of FSK data receivers that do not have a built-in post-detection filter.

It contains a digital moving average filter to remove noise from the demodulated data. When operated from a 38.4 kHz external clock it can handle data rates of 600, 1200 and 2400 bits/s at an oversampling rate of 16. The filter bandwidth can be doubled to ease the search for bit synchronization on the output data.

To allow for jitter in the input data, a 12-bit sample is taken for the majority decision. Doubling the filter bandwidth is realised by taking the majority out of 6 samples (2400 bits/s) or by doubling the sampling rate (600 and 1200 bits/s).

An input data rate of 4800 bits/s is supported at 8 times oversampling and normal bandwidth.

All inputs are Schmitt-triggered to ensure reliable operation even at signals with long rise/fall times.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		1.8	–	6.0	V
I_{DDPD}	power-down supply current	CE = V_{SS}	–	1.0	10.0	μA
I_{DD}	operating supply current	CE = V_{DD}; note 1	–	1.5	20.0	μA
$P_{i(ref)}$	sensitivity improvement at 3% bit error rate	note 2				
		600 bits/s, 250 μs slope	–	5.3	–	dB
		1200 bits/s, 250 μs slope	–	3.6	–	dB
		2400 bits/s, 125 μs slope	–	2.0	–	dB
T_{amb}	operating ambient temperature		−10	–	+70	°C

Notes

1. V_{DD} = 2.0 V; DOUT open-circuit; input data at 20 kHz random pattern.
2. Bench evaluated for UAA2080H at 470 MHz, not factory tested.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
OM4031T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

Digital post-detection filter for FSK data receivers

OM4031T

BLOCK DIAGRAM

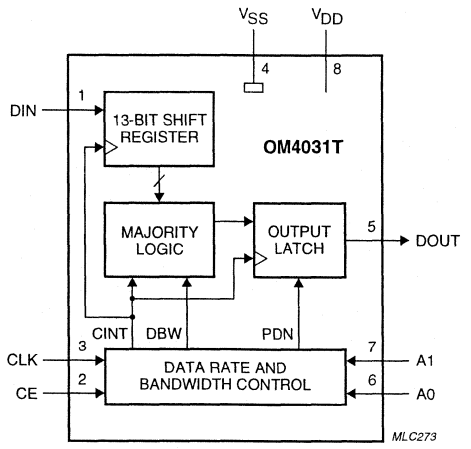


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
DIN	1	data input
CE	2	chip enable input
CLK	3	external clock input
V_{SS}	4	negative supply voltage
DOUT	5	data output (open-drain)
A0	6	data rate and bandwidth control input 0 (see Table 1)
A1	7	data rate and bandwidth control input 1 (see Table 1)
V_{DD}	8	positive supply voltage

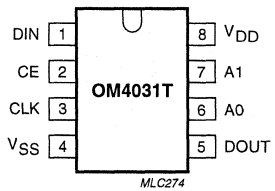


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The OM4031T digital post-detection filter oversamples the noisy binary data stream at input DIN (pin 1), and outputs a noise-reduced data stream via open-drain output DOUT (pin 5). The filter bandwidth can be doubled to ease the search for bit synchronization on the data output signal.

Input sampling takes place at 16 times the data rate. For a typical clock frequency of 38.4 kHz the nominal data rates are 600, 1200 and 2400 bits/s. A data rate of 4800 bits/s can be handled at an oversampling rate of 8 and at normal bandwidth only.

Using a different clock frequency will produce bit rates equal to the clock frequency divided by 64, 32 or 16. When the clock frequency is not an integer multiple of the data rate some edge jitter will be introduced in the output data.

The clock frequency is not very critical for the noise filtering performance: a clock frequency of 32.768 kHz could be used at 512, 1200 and 2400 bits/s without loss of performance.

Since no on-chip oscillator is available an external clock signal is required at input CLK (pin 3). Two control inputs A0 and A1 (pins 6 and 7) are used for selection of the data rate and the filter bandwidth.

A separate enable input CE (pin 2) allows the circuit to be powered down. In power-down mode (CE = LOW) the system clock is inhibited and the data output DOUT is made 3-state and remains static.

Moving average noise filter

Noise reduction is achieved by applying a moving average filter on N samples of the input data signal. In principle N can be odd or even, but in the OM4031T an even number is used (N = 12). When there is no absolute majority (equal number of ones and zeroes) the previous majority output is maintained.

An odd value for N would always produce an absolute majority and not require decision feedback. However the noise performance is worse for odd values of N, because the output can toggle at every clock (e.g. when a 101010... pattern is clocked in). For even values of N the output polarity can only change once every 3 clocks and does not toggle at all for a 101010... or a 11001100... pattern.

Using 12 out of 16 samples for the majority decision produces a filter which combines good noise reduction with a large tolerance for data jitter (maximum $\frac{1}{8}$-bit duration).

Filter implementation

The moving average filter is implemented using a 13-bit register and two state machines (COUNT and CLOCK) for the majority decision. The first stage of the shift register is used for input synchronization.

The CLOCK state machine generates the internal clock signal CINT and the bandwidth selection signal DBW in accordance with the logic levels on control lines CE, A0 and A1.

The majority decision is taken by state machine COUNT based on the contents of the input shift register and the previous decision in the output latch.

The doubled bandwidth is achieved by increasing the sampling rate by a factor of 2 for 600 and 1200 bits/s. For 2400 bits/s the number of samples for the majority decision is halved, controlled by the DBW signal. This signal is derived from the control signals as follows:

$$DBW = CE \bullet A0 \bullet \overline{A1}$$

Filter characteristic

The frequency characteristic of the moving average filter in the OM4031T is given in Fig.3 for N = 12 and N = 6.

The horizontal axis shows the normalized frequency f_N which is the ratio of the frequency f and the sampling frequency f_s. The value for f_s is given in Table 1 for the various data rates and filter bandwidths.

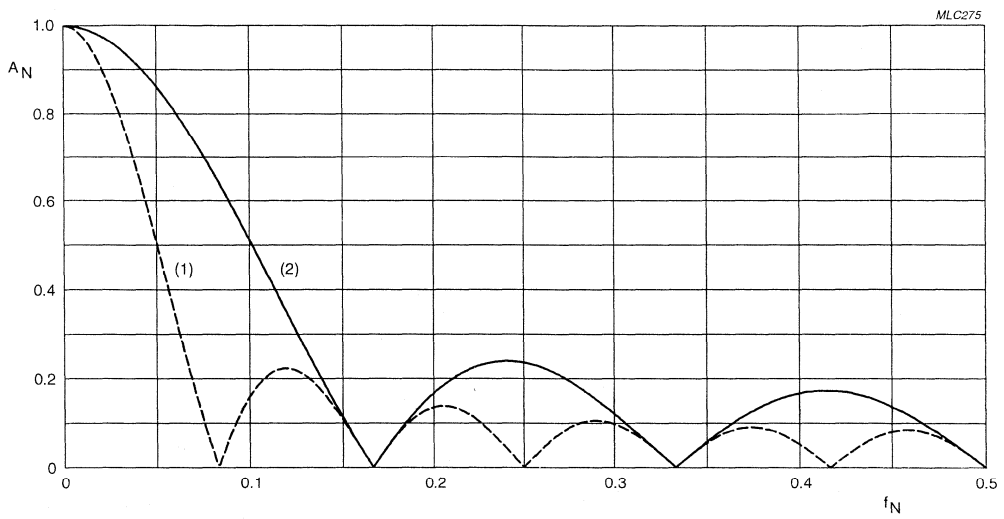
The vertical axis shows the normalized amplitude A_N.

At normal bandwidth the oversampling rate is 16, except for 4800 bits/s where it is 8. At double bandwidth the oversampling rate is 32, except for 2400 bits/s, where it is 16.

The 3 dB cut-off frequency is calculated as follows:

N = 12: $f_{co} = 0.0371 \times f_s$

N = 6: $f_{co} = 0.0748 \times f_s$



(1) N = 12.
(2) N = 6.

Fig.3 Filter transfer function of the OM4031T.

Noise reduction

The performance of the OM4031T was bench tested by measuring the sensitivity improvement (3% BER) of the UAA2080H pager receiver at various bit rates using a stand-alone pager receiver board (OM4647 at 470 MHz). The results are given in Chapter "AC Characteristics".

The OM4031T was also tested in a POCSAG pager application using software decoding together with the UAA2080H receiver.

For 12-digit numeric messages at 1200 bits/s the typical sensitivity for 80% call success rate improved by 2.8 dB, as shown in Fig.4.

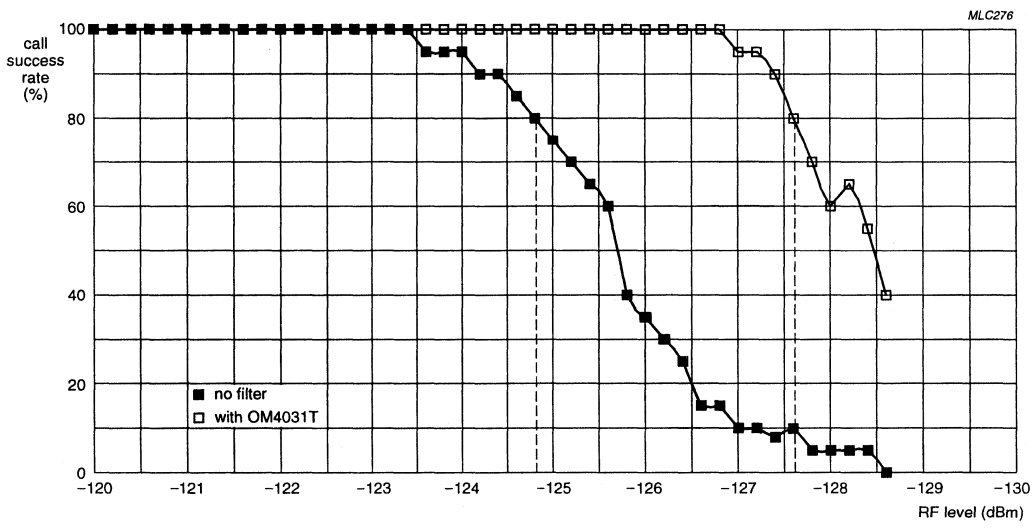


Fig.4 Paging call success rate improvement; 1200 bits/s, 12-digit numeric message.

OPERATING INSTRUCTIONS

Control signals

The operation of the OM4031T is determined by 3 control signals (CE, A0 and A1) and the clock frequency at input CLK. Table 1 shows the various possibilities for a typical clock frequency of 38.4 kHz.

The parameter N is the number of samples used in the calculation of the average bit value.

The parameter f_s is the input sampling frequency, assuming a 38.4 kHz external clock signal.

The logic levels on A0 and A1 can be changed while CE = HIGH, except to select or deselect 2400 bits/s with doubled bandwidth (A1 = LOW, A0 = HIGH). This mode must be entered or left while CE = LOW to avoid data errors on DOUT.

Table 1 Data rate and filter bandwidth selection

CE	A1	A0	N (samples)	f_s (kHz)	DATA RATE (bits/s)	
					NORMAL BANDWIDTH	DOUBLE BANDWIDTH
0	X	X	X	X	X	X
1	0	0	12	9.6	600	–
1	1	0	12	19.2	1200	600
1	0	1	6	38.4	4800(1)	2400
1	1	1	12	38.4	2400	1200

Note

1. At 4800 bits/s the oversampling rate is 8.

Power-down mode

To reduce power consumption the filter can be disabled by applying a LOW level to input CE. The result is as follows:

- The internal clock is inhibited
- Output DOUT is made 3-state and static.

Reset

The OM4031T is reset internally when power-down mode is left by applying a HIGH level to input CE. The actual reset takes place on the second falling edge on input CLK after CE = HIGH.

The status after reset is as follows:

- The shift register contains a 101010... pattern
- DOUT is made LOW.

After power-up input CE must be kept at a LOW level for at least one clock period on input CLK. This ensures a successful reset when CE is made HIGH.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	7.0	V
V_I	input voltage on any pin	−0.5	V_{DD} + 0.5	V
I_I	DC input current all pins	–	20	mA
I_O	DC output current all pins	–	20	mA
P_{tot}	total power dissipation	–	150	mW
T_{amb}	operating ambient temperature	−10	+70	°C
T_{stg}	storage temperature	−55	+125	°C

DC CHARACTERISTICS

V_{DD} = 1.8 to 6.0 V; V_{SS} = 0 V; T_{amb} = −10 to +70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage		1.8	–	6.0	V
I_{DDPD}	power-down supply voltage	CE = V_{SS}; note 1	–	1.0	10.0	µA
I_{DD}	operating supply current	CE = V_{DD}; notes 1 and 2	–	1.5	20.0	µA
Inputs A0, A1, CLK and CE						
V_{IL}	LOW level input voltage		−0.5	–	+0.3V_{DD}	V
V_{IH}	HIGH level input voltage		0.7V_{DD}	–	V_{DD} + 0.5	V
I_{LI}	input leakage current	V_I = V_{DD} or V_I = V_{SS}	–	–	1.0	µA
C_I	input capacitance	tested on sample basis	–	2.0	–	pF
Output DOUT						
I_{OL}	LOW level output current	V_{OL} = 0.4 V	1.0	–	–	mA
I_{LO}	output leakage current	V_{OH} = V_{DD}	–	–	1.0	µA

Notes

1. V_{DD} = 2.0 V; V_{IL} = V_{SS}; V_{IH} = V_{DD}; DOUT is open-circuit; clock signal at input CLK; f_{clk} = 38.4 kHz, amplitude: V_{SS} to V_{DD}; data signal at input DIN: random pattern at 20 kHz to simulate 2400 bits/s data with noise; t_r = t_f = 5 ns.
2. The operating current will be higher than specified when the input signal amplitude is less than 100% (equals V_{SS} to V_{DD}) or when longer rise/fall times are used. This is caused by the Schmitt-trigger circuits drawing extra current.

AC CHARACTERISTICS

V_{DD} = 1.8 to 6.0 V; V_{SS} = 0 V; T_{amb} = −10 to +70 °C; f_{clk} = 38.4 kHz; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
External clock						
f_{clk}	external clock frequency		30	38.4	80	kHz
Filter bandwidth (note 1)						
f_{co}	cut-off frequency (−3 dB)	normal bandwidth				
		600 bits/s	–	356	–	Hz
		1200 bits/s	–	712	–	Hz
		2400 bits/s	–	1425	–	Hz
		4800 bits/s	–	2872	–	Hz
		double bandwidth				
		600 bits/s	–	712	–	Hz
		1200 bits/s	–	1425	–	Hz
		2400 bits/s	–	2872	–	Hz
Noise reduction (note 2)						
$P_{i(ref)}$	sensitivity improvement at 3% bit error rate	note 3				
		600 bits/s, 250 µs slope	–	5.3	–	dB
		1200 bits/s, 250 µs slope	–	3.6	–	dB
		2400 bits/s, 125 µs slope	–	2.0	–	dB

Notes

1. Filter bandwidth is guaranteed by design. Values supplied are simulation results.
2. Noise reduction is not factory tested, only bench evaluated.
3. Sensitivity improvement was bench tested on the UAA2080H demonstration board OM4747. Test signal: preamble (101010...), f_{iRF} = 469.950 MHz, deviation = ±4.0 kHz, slope = 10 to 90% of amplitude, V_P = 2.05 V, T_{amb} = 25 °C. See *"UAA2080 data sheet, AC characteristics"*.

APPLICATION INFORMATION

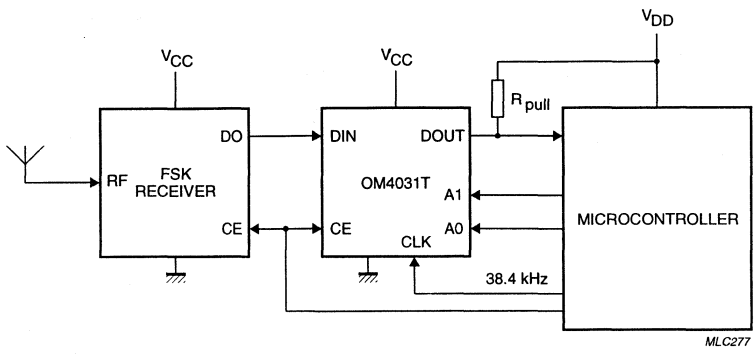


Fig.5 Typical application example.

The OM4031T will generally operate from the same power supply (V_{CC}) as the FSK data receiver providing its input data. The open-drain data output allows level shifting of the data to suit a microcontroller operating at a higher power supply voltage (V_{DD}).

The value of the pull-up resistor R_{pull} on output DOUT is determined by the type and number of input circuits to be driven. The required signal rise time must be balanced against the current drawn by the pull-up.

For the highest rate (2400 bits/s) the signal rise time should preferably be below 50 μs.

For a single CMOS input with a 10 pF capacitance R_{pull} = 1 MΩ gives a rise time of approximately 30 μs ($3 \times t_{RC}$). At V_{DD} = 2.0 V this corresponds with a current of 2 μA.

Universal LCD driver for low multiplex rates

OM4085

FEATURES

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2, 3 or 4 backplane multiplexing
- Selectable display bias configuration: static, ½ or ⅓
- Internal LCD bias generation with voltage-follower buffers
- 24 segment drives: up to twelve 8-segment numeric characters; up to six 15-segment alphanumeric characters; or any graphics of up to 96 elements
- 24 × 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- 2.0 to 6 V power supply range
- Low power consumption
- Power saving mode for extremely low power consumption in battery-operated and telephone applications
- I²C-bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 1536 segments possible)
- Cascadable with the 40 segment LCD driver PCF8576C
- Optimized pinning for single plane wiring in both single and multiple OM4085 applications
- Space-saving 40 lead plastic very small outline package (VSO40; SOT158-1)
- No external components required (even in multiple device applications)
- Manufactured in silicon gate CMOS process.

GENERAL DESCRIPTION

The OM4085 is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD) having low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 24 segments and can easily be cascaded for larger LCD applications. The OM4085 is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional I²C-bus. Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
OM4085T	VSO40	plastic very small outline package; 40 leads	SOT158-1

BLOCK DIAGRAM

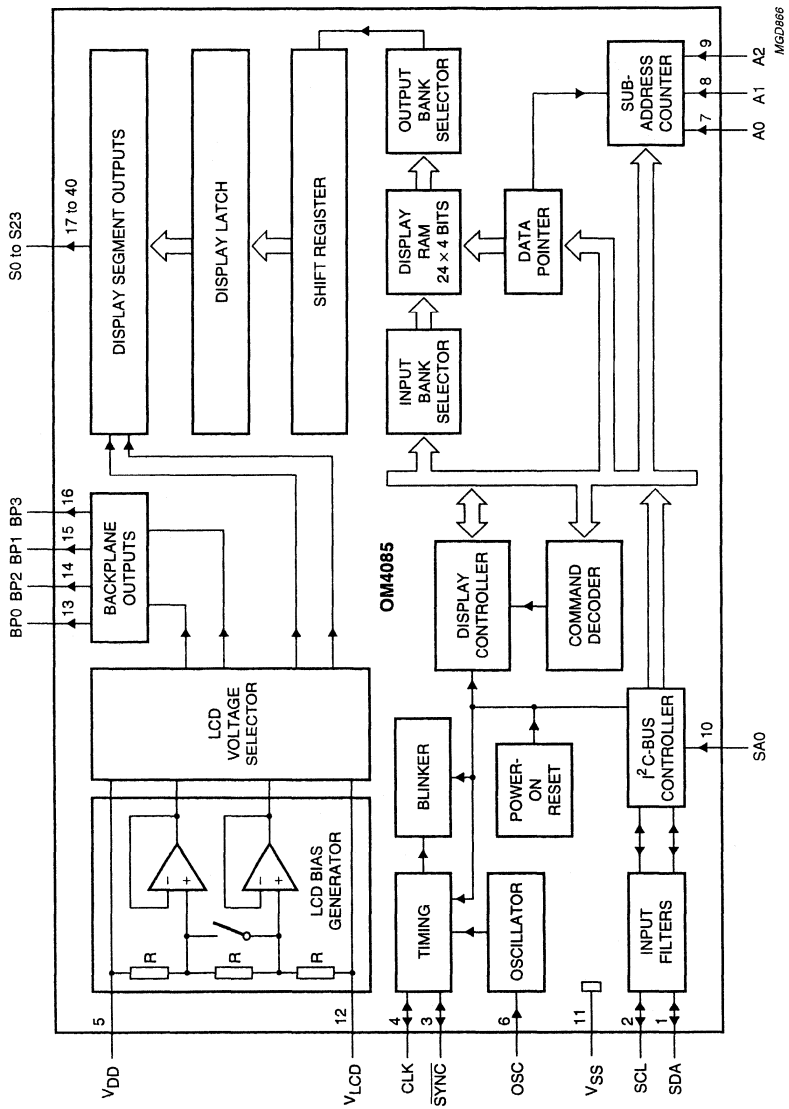


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SDA	1	I²C-bus data input/output
SCL	2	I²C-bus clock input/output
$\overline{SYNC}$	3	cascade synchronization input/output
CLK	4	external clock input/output
V_{DD}	5	positive supply voltage
OSC	6	oscillator input
A0	7	I²C-bus subaddress inputs
A1	8	
A2	9	
SA0	10	I²C-bus slave address bit 0 input
V_{SS}	11	logic ground
V_{LCD}	12	LCD supply voltage
BP0	13	LCD backplane outputs
BP2	14	
BP1	15	
BP3	16	
S0 to S23	17 to 40	LCD segment outputs

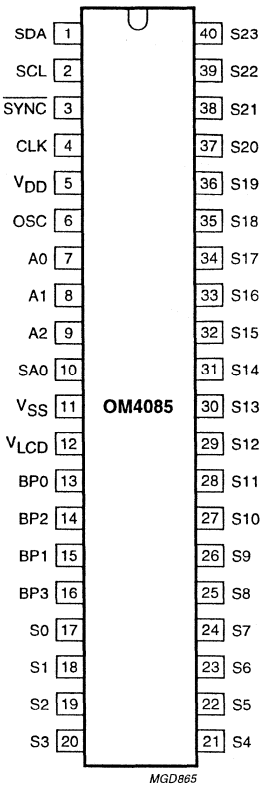


Fig.2 Pin configuration.

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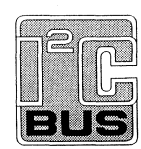


1 FEATURES

- Full static 80C51 CPU; enhanced 8-bit architecture with:
  - minimum 6 cycles per instruction (twice as fast as a standard 80C51 core)
  - non-page oriented instructions
  - direct addressing
  - four 8-byte RAM register banks
  - stack depth limited only by available internal RAM (maximum 256 bytes)
  - multiply, divide, subtract and compare instructions
- 8-bit ports:
  - P83CL883 and P87CL883: 3 (19 I/O lines)
  - P83CL884 and P87CL884: 3 (18 I/O lines)
- Program Memory:
  - P87CL883/P87CL884: 8 kbytes One Time Programmable (OTP)
  - P83CL883/P83CL884: 8 kbytes ROM
- 256 bytes RAM
- 128 bytes EEPROM Data Memory, accessed internally via I^2C-bus interface (P83CL884 and P87CL884 only)
- Amplitude Controlled Oscillator (ACO) suitable for quartz crystal or ceramic resonator
- Improved Power-on/Power-off reset (POR) circuitry
- Low Voltage Detection (LVD) with 11 software programmable levels
- Eight interrupts on Port 1:
  - edge or level sensitive triggering selectable via software
  - power-saving use for keyboard control
- Twenty source, twenty vector interrupt structure with two priority levels
- Wake-up from Power-down mode via LVD or external interrupts at Port 1
- DTMF generator (P83CL884/P87CL884 only)
- MSK modem including Manchester encoder/decoder with 2 digital outputs for analog cordless telephones (standards CT0/CT1/CT1+)
- Two standard 16-bit timer/event counters
- Additional 16-bit timer/event counter with Capture, Compare and Auto-reload function
- Watchdog Timer
- Full duplex enhanced UART with double buffering
- I^2C-bus interface for serial transfer on two lines, maximum 400 kHz
- Very low current consumption
- Single supply voltage: 2.7 to 3.6 V
- Frequency range: 3.58 MHz
- Operating temperature: –25 to +70 °C
- 28 pins SO package.

2 GENERAL DESCRIPTION

The P8xCL883/P8xCL884 - denoting the P83CL883; P87CL883; P83CL884 and P87CL884 - are manufactured in an advanced CMOS technology. The P83CL883 and P87CL883 are based on single chip technology and the P83CL884 and P87CL884 are based on MCM (Multi-Chip-Module) technology as the EEPROM is integrated on a separate chip.

The P8xCL883/P8xCL884 are 8-bit microcontrollers especially suited for low cost analog cordless telephone applications (CT0, CT1, CT1+ standards). For this purpose, features like DTMF, EEPROM, MSK modem and POR/LVD are integrated on-chip.

The device is optimized for low power consumption. The P8xCL883/P8xCL884 have two software selectable features for power reduction: Idle and Power-down modes. In addition, all derivative blocks can switch off their clock if they are inactive.

The instruction set of the P8xCL883/P8xCL884 is based on that of the 8051. The P8xCL883/P8xCL884 also function as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 46 two-byte, and 16 three-byte. Due to the missing port P2, there is no external data or memory access and the MOVX operations cannot be used.

This data sheet details the specific properties of the P8xCL883/P8xCL884; for details of the P8xCL883/P8xCL884 core and the derivative functions see the *"TELX family"* data sheet and *"Data Handbook IC20; 80C51-based 8-bit Microcontrollers"*.

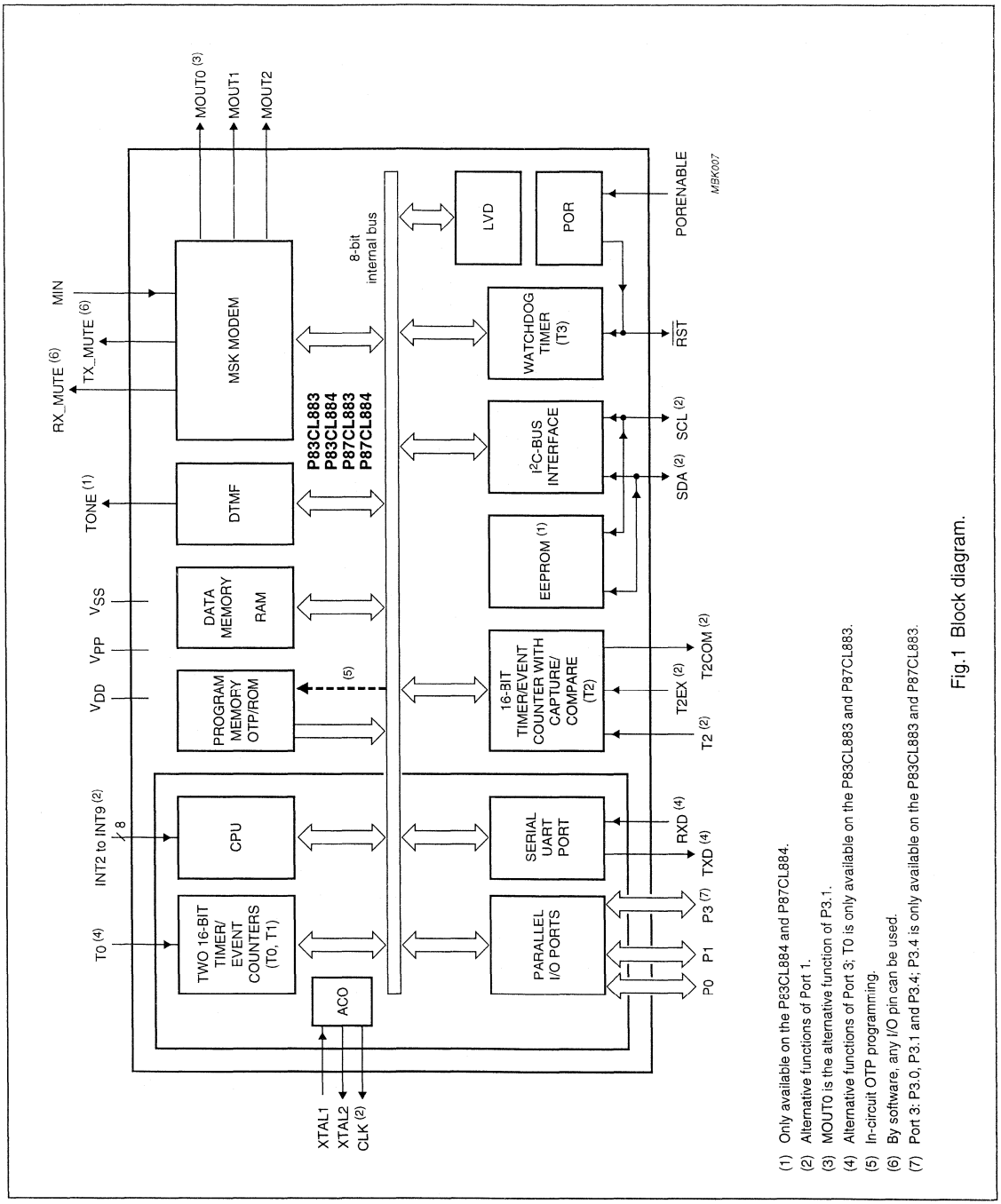
3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
P83CL883DDT	SO28[1]	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
P87CL883DDT			
P83CL884DDT			
P87CL884DDT			

Note

1. When using IR reflow soldering it is recommended that the Dry Packing instructions in the *"Quality Reference Pocketbook"* (order number 9398 510 34011) are followed.

4 BLOCK DIAGRAM

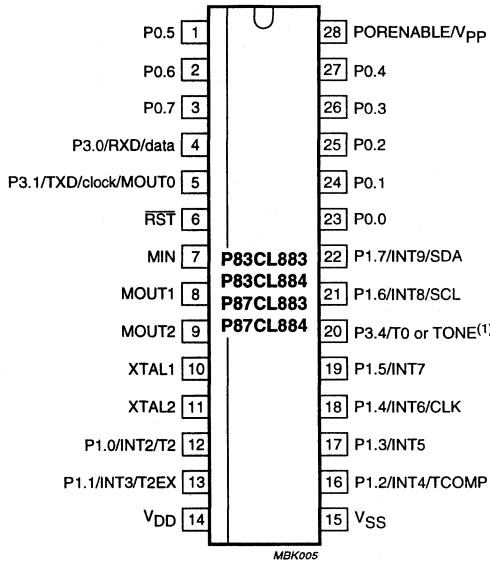


(1) Only available on the P83CL884 and P87CL884.
(2) Alternative functions of Port 1.
(3) MOUT0 is the alternative function of P3.1.
(4) Alternative functions of Port 3; T0 is only available on the P83CL883 and P87CL883.
(5) In-circuit OTP programming.
(6) By software, any I/O pin can be used.
(7) Port 3: P3.0, P3.1 and P3.4; P3.4 is only available on the P83CL883 and P87CL883.

Fig.1 Block diagram.

5 PINNING INFORMATION

5.1 Pinning



(1) **Pin 20**: P3.4/T0 on the P83CL883 and P87CL883; TONE on the P83CL884 and P87CL884.

Fig.2 Pin configuration.

5.2 Pin description

SYMBOL	PIN	DESCRIPTION
$\overline{RST}$	6	**Active low reset:** a LOW level on this pin for two machine cycles while the oscillator is running, resets the device. The $\overline{RST}$ pin is also an output which can be used to reset other ICs.
MIN	7	Digital **MSK** modem input.
MOUT1	8	Digital **MSK** modem outputs.
MOUT2	9	
XTAL1	10	**Crystal input:** Input to the Amplitude Controlled Oscillator. Also the input for an externally generated clock source.
XTAL2	11	**Crystal output:** Output of the Amplitude Controlled Oscillator. To be left non-connected when an external oscillator clock is used.
V_{DD}	14	Power supply.
V_{SS}	15	Ground.
P0.0 to P0.7	23 to 27, 1 to 3	**Port 0**: 8-bit bidirectional I/O port. Every port pin can be used as open-drain, standard port, high-impedance input or push-pull output, according to Section 6.2.
P1.0/INT2/T2	12	**Port 1**: 8-bit bidirectional I/O port with alternative functions. Every port pin except P1.6 and P1.7 (I^2C-bus pins) can be used as open-drain, standard port, high-impedance input or push-pull output, according to Section 6.2. Port P1.3 has LED drive capability. Port 1 also serves the alternative functions: **INT2 to INT9** interrupts; Timer T2 external inputs **T2** and **T2EX**; Timer T2 compare output **T2COMP**; external clock output **CLK**; I^2C-bus clock **SCL** and data in/outputs **SDA**.
P1.1/INT3/T2EX	13	
P1.2/INT4/T2COMP	16	
P1.3/INT5	17	
P1.4/INT6/CLK	18	
P1.5/INT7	19	
P1.6/INT8/SCL	21	
P1.7/INT9/SDA	22	
P3.0/RXD/data	4	**Port 3:** 3 or 2-bit bidirectional I/O port with alternative functions. Every port pin can be used as open-drain, standard port, high-impedance input or push-pull output, according to Chapter 6.2. Port 3 also serves the alternative functions: **RXD/data** is the serial port receiver data input (asynchronous) or data I/O (synchronous); **TXD/clock** is the serial port transmitter data output (asynchronous) or clock output (synchronous) or digital MSK modem output **MOUT0**; **T0** is an external input for Timer 0. **P3.4/T0** is only available on the P83CL883 and P87CL883.
P3.1/TXD/clock/ MOUT0	5	
P3.4/T0	20	
TONE	20	**DTMF** output; **TONE** is only available on the P83CL884 and P87CL884.
PORENABLE/V_{PP}	28	**PORENABLE**: Power-on-reset circuit enable. If PORENABLE = 1, the internal Power-on-reset circuit is enabled. If external reset circuitry is used, it is recommended to keep PORENABLE = 0 to reach lowest power consumption. This pin is also used for the OTP programming voltage V_{PP}.

6 FUNCTIONAL DESCRIPTION

6.1 Special Function Registers (SFRs)

Table 1 List of SFRs

REGISTER	ADDRESS (HEX)	RESET VALUE[1] (MSB..LSB)
80C51 core		
ACC	E0	00000000
B	F0	00000000
DPL	82	00000000
DPH	83	00000000
PCH	no SFR	00000000
PCL	no SFR	00000000
PCON	87	00000000
PRESC	F3	00000000
PSW	D0	00000000
SP	81	00000111
T0/T1		
TCON	88	00000000
TH0	8C	00000000
TH1	8D	00000000
TL0	8A	00000000
TL1	8B	00000000
TMOD	89	00000000
Port		
ALTP	A3	00000000
P0	80	11111111
P0CFGA	8E	11111111
P0CFGB	8F	00000000
P1	90	11111111
P1CFGA	9E	00111111
P1CFGB	9F	00000000
P3	B0	XXX1XX11
P3CFGA	BE	XXX1XX11
P3CFGB	BF	XXX0XX00
P4	C1	XXXXXXX0
TIMER2		
COMP2H	AB	00000000
COMP2L	AA	00000000
RCAP2H	CB	00000000
RCAP2L	CA	00000000

REGISTER	ADDRESS (HEX)	RESET VALUE[1] (MSB..LSB)
T2CON	C8	00000000
TH2	CD	00000000
TL2	CC	00000000
EEPROM interface		
EECON	FB	00000000
DTMF		
HGF	A2	00000000
LGF	A1	00000000
Interrupt logic		
IEN0	A8	00000000
IEN1	E8	00000000
IEN2	F1	00000000
IP0	B8	00000000
IP1	F8	00000000
IP2	F9	00000000
ISE1	E1	00000000
IX1	E9	00000000
IRQ1	C0	00000000
LVD		
LVDCON	F2	00000000
POR/ACO		
RSTAT	E6	XXX01001[2]
MSK		
MCON	D3	00000000
MBUF	D1	XXXXXXXX
MSTAT	D2	XX000000
UART		
S0BUF	99	00000000
S0CON	98	00000000
I²C-bus		
S1ADR	DB	00000000
S1CON	D8	00000000
S1DAT	DA	00000000
S1STA	D9	11111000

REGISTER	ADDRESS (HEX)	RESET VALUE[1] (MSB..LSB)
WDT		
WDCON	A5	10100101
WDTIM	FF	00000000
OTP interface		
OAH	D5	X00XXXXX
OAL	D4	XXXXXXXX
ODATA	D6	XXXXXXXX
OISYS	DC	000X0000
OTEST	D7	00000000
Reserved locations; do not write		
reserved	E7, FD	–

Notes

1. Where: X = undefined state or not implemented bit.
2. Defined by VIA mask.

6.2 I/O facilities

6.2.1 PORTS

The P8xCL883 and P8xCL884 have 19 and 18 I/O lines respectively, treated as 19 and 18 individually addressable bits or as three parallel 8-bit addressable ports.
The alternative functions are detailed below:

Port 0 Offers no alternative function.

Port 1 Used for a number of special functions:

- P1.0 to P1.7 provides the inputs for the external interrupts INT2 to INT9
- P1.2/T2COMP for external activation and Compare/Auto-reload output function of Timer 2
- P1.4/CLK for the clock output
- P1.6/SCL and P1.7/SDA for the I^2C-bus interface are real open-drain outputs or high-impedance; no other port configurations are available.

Port 2 Not available.

Port 3 Pins can be configured individually to provide:

- P3.0/RXD/data and P3.1/TXD/clock/MOUT0 are serial port receiver input and transmitter output (UART)
- P3.4/T0 as counter input; available only in P8xCL883.

To enable a Port pin alternative function, the Port bit latch in its SFR must contain a logic 1.

Each port consists of a latch (Special Function Registers P0 to P3), an output driver and input buffer. All ports have internal pull-ups. Figure 3b shows that the strong transistor 'p1' is turned on for only one oscillator period after a LOW-to-HIGH transition in the port latch. When on, it turns on 'p3' (a weak pull-up) through the inverter IN1. This inverter and transistor 'p3' form a latch which holds the logic 1.

Port P1.3 has LED drive capability.

6.2.2 PORT I/O CONFIGURATION

I/O port output configurations are determined by the settings in port configuration SFRs. There are 2 SFRs for each port, called PnCFGA and PnCFGB, where 'n' indicates the specific port number (0 to 3). One bit in each of the 2 SFRs relates to the output setting for the corresponding port pin, allowing any combination of the 2 output types to be mixed on those port pins.
For instance, the output type of Port 1 pin 3 is controlled by the setting of bit 3 in the SFRs P1CFGA and P1CFGB.

The port pins may be individually configured via SFRs with one of the following modes (P1.6 and P1.7 can be open-drain or high-impedance but never have any diodes against V_{DD}). These modes are also shown in Fig.3.

Mode 0 Open-drain; quasi-bidirectional I/O with n-channel open-drain output. Use as an output requires the connection of an external pull-up resistor; e.g. Port 0 for external memory accesses (EA = 0) or access above the built-in memory boundary. The ESD protection diodes against V_{DD} and V_{SS} are still present; see Fig.3b. Except for the I^2C pins P1.6 and P1.7, ports which are configured as open-drain still have a protection diode to V_{DD}.

Mode 1 Standard port; quasi-bidirectional I/O with pull-up. The strong pull-up 'p1' is turned on for only two oscillator periods after a LOW-to-HIGH transition in the port latch. After these two oscillator periods the port is only weakly driven through 'p2' and 'very weakly' driven through 'p3' (see Fig.3b).

Mode 2 High-impedance; this mode turns off all output drivers on a port. Thus, the pin will not source or sink current and may be used as an input-only pin with no internal drivers for an external device to overcome (see Fig.3c).

Mode 3 Push-pull; output with drive capability in both polarities. Under this mode, pins can only be used as outputs (see Fig.3d).

Tables 2 and 3 show the configuration register settings for the 4 port output types.

The electrical characteristics of each output type can be found in Chapter 8. The default port configuration after reset is given in Table 3.

Table 2 Port Configuration Registers PnCFGA and PnCFGB (n = 0 to 3) settings

MODE[1]	PnCFGA	PnCFGB	PORT OUTPUT MODE	
			NORMAL PORTS	I²C-BUS PORTS (P1.6 AND P1.7)
Mode 0	0	0	open-drain	open-drain
Mode 1	1	0	quasi-bidirectional	open-drain
Mode 2	0	1	high-impedance	high-impedance
Mode 3	1	1	push-pull	open-drain

Note

1. Mode changes may cause glitches to occur during transitions. When modifying both registers, WRITE instructions should be carried out consecutively.

Table 3 Special Function Registers for port configurations/data

REGISTER NAME	REGISTER MNEMONIC	SFR ADDRESS (HEX)	STATE AFTER RESET
Port P0 output data[1]	P0	80	1111 1111
Port P0 configuration A	P0CFGA	8E	1111 1111
Port P0 configuration B	P0CFGB	8F	0000 0000
Port P1 output data[1]	P1	90	1111 1111
Port P1 configuration A	P1CFGA	9E	0011 1111
Port P1 configuration B	P1CFGB	9F	0000 0000
Port P3 output data[1]	P3	B0	XXX1 XX11[2]
Port P3 configuration A	P3CFGA	BE	XXX1 XX11[2]
Port P3 configuration B	P3CFGB	BF	XXX0 XX00[2]

Note

1. This means that P0, P1.0 to P1.5 and P3 are initialized in Mode 1 (quasi-bidirectional, driving a weak HIGH) and the I²C-bus ports P1.6 and P1.7 are initialized in Mode 0 (open-drain, not driven).
2. Port pin P3.4 is only available on P8xCL883.

6.2.3 Alternative Port Function Register (ALTP)

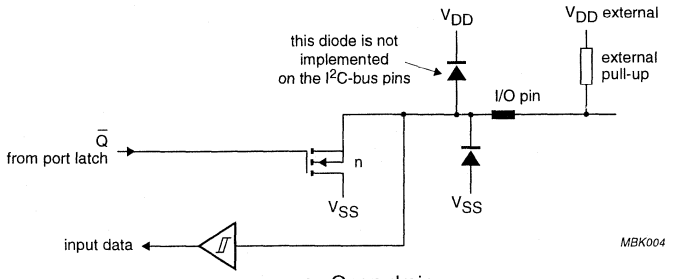
This 4-bit register controls the alternative function of some port pins.

Table 4 Alternative Port Function Register (SFR address A3H)

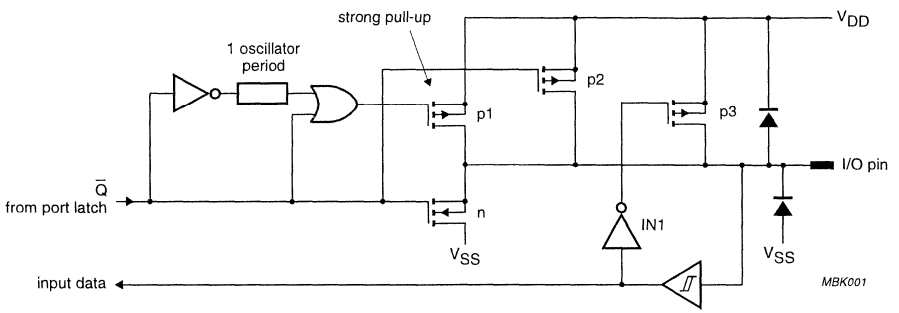
7	6	5	4	3	2	1	0
–	–	–	–	EMOUT0	ECLK	EMLDY	ETONE

Table 5 Description of ALTP bits

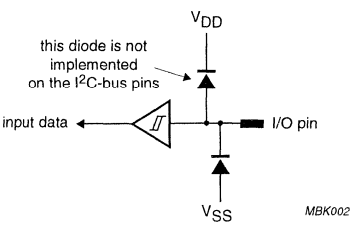
BIT	SYMBOL	DESCRIPTION
7 to 4	–	Reserved.
3	EMOUT0	If this bit is set, P3.1 will output the MOUT0 signal.
2	ECLK	If this bit is set, P1.4 is configured to be push-pull, and P1.4 will output the system clock.
1	EMLDY	If this bit is set, P1.5 is configured to be push-pull, and P1.5 will output the digital MLDY signal of the DTMF generator.
0	ETONE	If this bit is set, the TONE output of the DTMF generator is enabled.



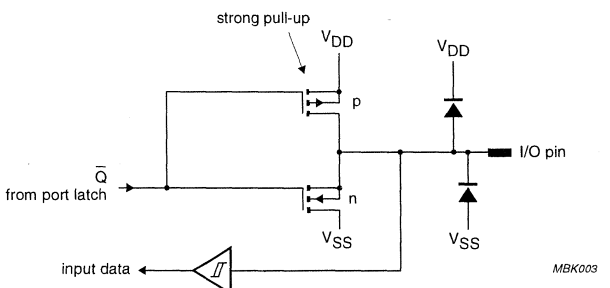
a. Open-drain.



b. Standard/quasi-bidirectional.



c. High-impedance.



d. Push-pull.

Fig.3 Port configuration options.

6.3 Timer/event counters

The P8xCL883/P8xCL884 contain three 16-bit timer/event counters: Timer 0, Timer 1 and Timer 2 which can perform the following functions:

- Measure time intervals and pulse durations
- Count events
- Generate interrupt requests
- Generate output on comparator match.

In the 'timer' mode the register is incremented every machine cycle.

Since a machine cycle consists of minimum 6 oscillator periods, the maximum count rate is $\frac{1}{6} \times f_{osc}$.

In the 'counter' mode, the register is incremented in response to a HIGH-to-LOW transition. Since it takes one machine cycle (minimum 6 oscillator periods) to recognize a HIGH-to-LOW transition, the maximum count rate is $\frac{1}{6} \times f_{osc}$. To ensure a given level is sampled, it should be held for at least one complete machine cycle.

Timer 0 and Timer 1 can be programmed independently to operate in four modes:

Mode 0 8-bit timer or 8-bit counter each with divide-by-32 prescaler.

Mode 1 16-bit time-interval or event counter.

Mode 2 8-bit time-interval or event counter with automatic reload upon overflow.

Mode 3 Timer 0 establishes TL0 and TH0 as two separate counters.

Note that the T0 input is only available on P8xCL883.

6.3.1 TIMER T2

Note that the timer T2 of the P8xCL883/P8xCL884 deviates from the timer T2 described in the *"TELX family"* data sheet.

Timer T2 is a 16-bit timer/counter that can operate either as a timer or as an event counter. These functions are selected by the state of the C/$\overline{T2}$ bit in the T2CON register. Five operating modes are available:

- Capture
- Compare
- Auto-reload
- Compare with Auto-reload
- Capture and Compare.

These modes are selected via the T2CON register.

6.3.1.1 Capture mode

In the Capture mode, two options may be selected by the EXEN2 bit in T2CON:

- If EXEN2 = 0, then Timer 2 is a 16-bit timer or counter which upon overflowing sets the Timer 2 overflow bit TF2, this may then be used to generate an interrupt.
- If EXEN2 = 1, Timer 2 operates as described above but with the additional feature that a HIGH-to-LOW transition at external input T2EX causes the current value in TL2 and TH2 to be captured into registers RCAP2L and RCAP2H respectively. In addition, the transition at T2EX causes the EXF2 bit in T2CON to be set; this may also be used to generate an interrupt.

The Capture mode is shown in Fig.4.

6.3.1.2 Compare mode

In the Compare mode, each time timer T2 is incremented, the contents of the compare registers COMP2H and COMP2L is compared with the new counter value of timer T2. When a match occurs, the interrupt flag COMP in register T2CON and port bit P1.2 are toggled. The 16-bit value held in these registers is preset by software. The first toggle after a chip reset will set the flag COMP.
The Compare mode is shown in Fig.4.

6.3.1.3 Auto-reload mode

In the Auto-reload mode there are also two options selected by the EXEN2 bit in T2CON:

- If EXEN2 = 0, then when Timer 2 rolls over, it sets the TF2 bit but also causes the Timer 2 registers to be reloaded with the 16-bit value held in registers RCAP2L and RCAP2H. The 16-bit value held in these registers is preset by software.
- If EXEN2 = 1, Timer 2 operates as described above but with the additional feature that a HIGH-to-LOW transition at external input T2EX will also trigger the 16-bit reload and set the EXF2 bit.

6.3.1.4 Compare with Auto-reload mode

The Auto-reload mode can also be used together with the Compare mode. The Auto-reload modes are shown in Fig.5.

6.3.1.5 Capture and Compare modes

The Capture and the Compare mode of timer T2 can be used separately or simultaneously. The function is chosen via the bits ECOMP, CP/$\overline{RL2}$ and TR2 in register T2CON.

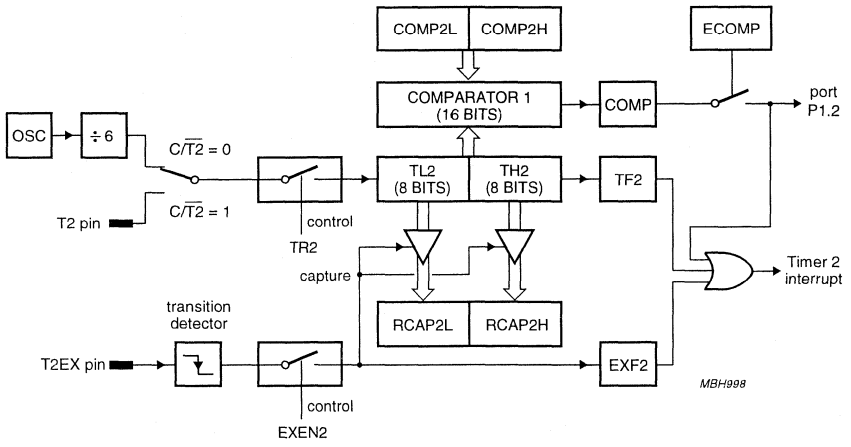


Fig.4 Timer 2 in Capture and/or Compare mode.

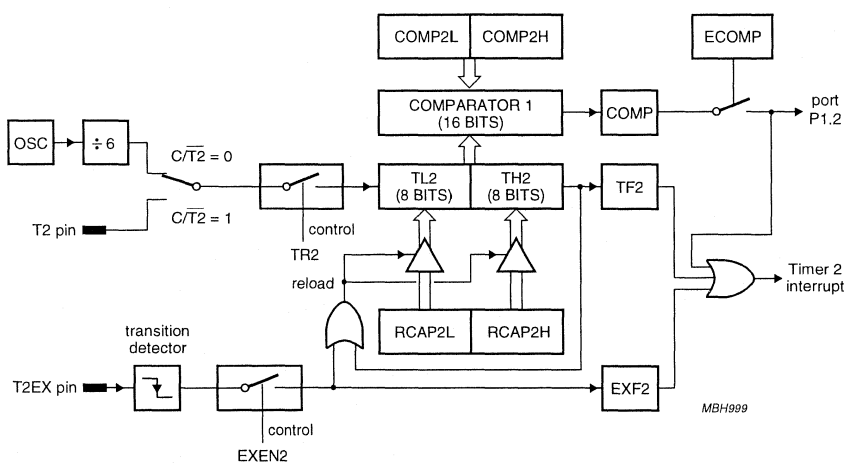


Fig.5 Timer 2 in Auto-Reload with/without Compare mode.

6.3.2 Timer/Counter 2 Control Register (T2CON)

Table 6 Timer/Counter 2 Control Register (SFR address C8H)

7	6	5	4	3	2	1	0
TF2	EXF2	COMP	ECOMP	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$

Table 7 Description of T2CON bits

BIT	SYMBOL	DESCRIPTION
7	TF2	**Timer 2 overflow flag.** TF2 is set by a Timer 2 overflow and must be cleared by software.
6	EXF2	**Timer 2 external flag.** EXF2 is set when either a capture or reload is caused by a negative transition on T2EX and when EXEN2 = 1. When Timer T2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to Timer 2 interrupt routine. EXF2 must be cleared by software.
5	COMP	**Interrupt flag.** When a match between the 16-bit compare register (COMP2L and COMP2H) and the new counter value of timer T2 occurs, the interrupt flag COMP in register T2CON and port bit P1.2 are toggled.
4	ECOMP	**Enable compare output bit.** When set by software, the controller toggles port bit P1.2 (T2COMP) when a compare match occurs.
3	EXEN2	**Timer 2 external enable flag.** When set, allows a capture or reload to occur as a result of a negative transition on T2EX. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
2	TR2	**Timer 2 start/stop control.** Control bit for Timer 2.
1	C/$\overline{T2}$	**Timer 2 timer or counter select.** C/$\overline{T2}$ = 0 selects the internal timer with a clock frequency of $\frac{1}{6} \times f_{osc}$. C/$\overline{T2}$ = 1 selects the external event counter; negative edge-triggered.
0	CP/$\overline{RL2}$	**Capture/reload flag.** When set captures will occur on negative transitions at T2EX, if EXEN2 = 1. When cleared, auto-reloads will occur either with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1.

Table 8 Timer 2 operating modes

ECOMP	CP/$\overline{RL2}$	TR2	MODE
0	0	1	16-bit Auto-reload
0	1	1	16-bit Capture
1	0	1	16-bit Compare
1	1	1	16-bit Capture and Compare
1	0	0	16-bit Compare with Auto-reload
0	0	0	off

6.4 MSK modem

For the P8xCL883/P8xCL884, MIN is no longer the alternative function of P4.0, but MIN is a separate pin. The polarity of MIN can however still be programmed with the P4.0 bit. P4.0 is a data SFR but no port logic is connected.

Only the most significant bits of MOUT, i.e. MOUT2 and MOUT1 are directly available as separate pins. In order to be able to further increase the signal quality, the MOUT0 signal is available as alternative port function of P3.1.

For controlling this alternative port function the EMOUT0 bit has been added to the Alternative Port Function Register (ALTP); see Section 6.2.3.

6.5 Watchdog Timer

The Watchdog Timer differs from the description in the *"TELX family"* data sheet in that the external $\overline{EW}$ pin does not exist on the P8xCL883/P8xCL884.

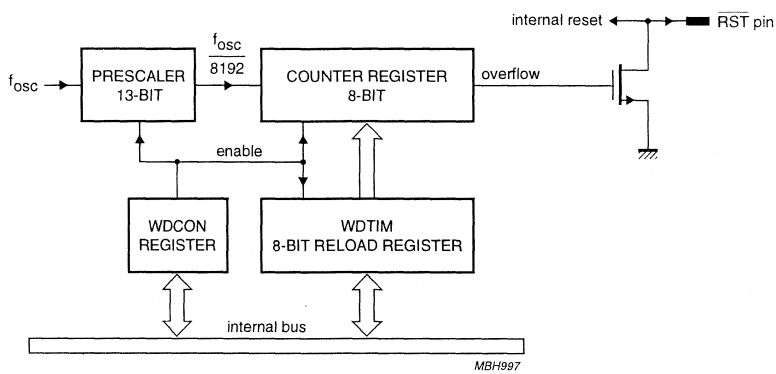


Fig.6 Functional diagram of the T3 Watchdog Timer.

6.6 OTP programming

6.6.1 OTP PROGRAMMING BY A PROGRAMMER

The 8 kbytes One Time Programmable (OTP) memory can be programmed by using a programmer (OM4260) together with a programmer adapter OM5508. Since the memory is programmable only once, programming an already programmed address results in a logical AND of the old and new code. The OTP code can be read out by the programmer for verification.

6.6.1.1 Signature bytes

The OTP memory contains three signature bytes which can be read by the programmer to identify the device. A special address space has been used for these bytes which does not influence the user address space.

The values of the signature bytes are:

(030H) = 15H, indicates manufactured by Philips Semiconductors

(031H) = C5H, indicates P87CL883 and P87CL884

(060H) = 00H, currently not used.

6.6.1.2 Security

The following protection levels are available to protect TELX applications against software piracy and unwanted access to data stored in the application.

1. Preventing programming of an already programmed OTP. Note that security Level 1 also disables In System Programming.
2. Preventing the reading of program code in OTP by disabling access of the programmer to the Program Memory. Also verification of code during In System Programming is disabled. In this mode signature and security level verification is still possible.
3. This level has the same functionality as Level 2.

Table 9 describes how these protections can be selected by programming the three least significant bits of the security byte.

Table 9 Security bits and levels of protection

BITS	LEVEL	DESCRIPTION
UUU	0	no security
UUP	1	Level 1 is activated
UPP	2	Levels 1 and 2 are activated
PPP	3	Levels 1, 2 and 3 are activated

6.6.2 In System Programming mode

In the In System Programming mode the OTP can be programmed under control of the CPU. A program to control programming has to be available in the OTP. This mode can be used to program several bytes in the OTP if the chip is already in a system e.g. to store tuning parameters.

In the In System Programming mode the complete address space OTP can be programmed.

The user should take care not to overwrite the existing code.

For In System Programming four SFRs are used to control the OTP.

Table 10 SFRs for In System Programming

SFR NAME	DESCRIPTION
OAH	OTP Address High Register
OAL	OTP Address Low Register
ODATA	OTP Data Register
OISYS	OTP In System Register

6.6.2.1 OTP In System Programming Register (OISYS)

The OISYS SFR controls the In System Programming mode. The data that has to be programmed is stored in the SFR ODATA and the address for this data in the SFRs OAH and OAL.

Table 11 OTP In System Programming Register (SFR address DCH)

7	6	5	4	3	2	1	0
–	–	–	VPon	SEC	SIG	WE	InSysMode

Table 12 Description of OISYS bits

BIT	SYMBOL	DESCRIPTION
7 to 5	–	Reserved.
4	VPon	V_{PP} status (read only).
3	SEC	Security bits enable.
2	SIG	Signature bytes enable.
1	WE	Write Enable, enables programming.
0	InSysMode	In System Programming status bit.

6.6.2.2 Mode entry

The In System Programming mode is entered by setting the InSysMode bit of the OISYS SFR. The I^2C-bus is used for data transfer in this mode. If the I^2C-bus interface is addressed by an external master, the interface generates an interrupt request. The interrupt handler can now read the OISYS SFR and determine the status of the external high voltage (VPon). If high voltage is not present the interrupt is a standard I^2C-bus interrupt.

If high voltage is present the In System Program interrupt routine has to start that writes the InSysMode bit (OISYS.0) and controls the address and data transfer.

Note that this paragraph is only applicable for the first series, it can be neglected in the future. During In System Programming the OTP memory has to be in DC read mode. This is achieved by writing 08H to the OTEST SFR. If the In System Programming mode is left 00H has to be written into the OTEST SRF.

The program voltage has to be available and stable for at least 10 µs before the mode is entered and has to be stable until the circuit has left the In System Programming mode. The high voltage can be applied for maximum 60 seconds during the complete lifetime of the circuit.

6.6.2.3 Program cycle

The data and address have to be supplied to the microcontroller and the control program has to write the SFRs: ODATA, OAH and OAL. A timer has to be initialized for a 100 µs cycle and the WE bit of the OISYS SFR has to be set. Now the core has to be set into Idle mode. As long as the circuit is in idle mode a programming pulse is applied. After the interrupt request of the timer the OTP is available for normal code fetching.

The address applied to the OAH and OAL SFRs must be in the 8 kbytes address space.

6.6.2.4 Verify for In System Programming

Verify is done in similar way as programming. The circuit is put into idle mode and at the start of this mode the sense amplifiers are switched to verify mode and a read cycle is started. The timer has to be initialized for a cycle of at least 1 µs. The address is supplied by the SFRs OAH and OAL. The WE bit of the OISYS SFR has to be reset. The OTP output data is latched in the ODATA SFR. After Idle mode is finished this SFR can be read in a normal way. To be sure that the verified data is written into the SFR it is advised to write FFH into the ODATA SFR before a verify is started.

6.6.2.5 Signature bytes and security

The signature bytes can be read by setting the SIG bit of the OISYS SFR and applying the address of the signature byte. Applying a write pulse while the SIG bit of the OISYS SFR is HIGH is forbidden although the contents of the signature bytes will never be destroyed. The signature bytes (and other test addresses) are always readable independent of the security.

Security has the same meaning as in Parallel Program mode. Security can be programmed and verified by setting the SEC bit of the OISYS SFR. The security bits can be programmed like normal bits.To program Level 1, 01H has to be loaded in the ODATA SFR. These values are 03H and 07H for Level 2 and Level 3 respectively. The SEC bit of the OISYS SFR has to be HIGH during the program cycle. Loading an address is not necessary. The timer has to be initialized for a 200 µs instead of 100 µs for security or two standard pulses have to be applied. If the SEC bit is HIGH during verify, the security bits can be read from the ODATA SFR. Verifying a normal address while security level - Level 2 or Level 3 - has been programmed will result in reading 00H.

Verifying is disabled immediately after programming Level 2 or Level 3. Programming is disabled if a verify or a reset is applied after programming security level: Level 1 or higher.

6.6.2.6 How to connect the PORENABLE/V_{PP} pin in the In System Programming mode

If the V_{PP} pin is dual-mode (e.g. PORENABLE/V_{PP}), ICs connected to the signal PORENABLE **must be able to withstand up to 13 V**, i.e. cannot have clamping diodes or low bread-down voltages. If the pin is connected to a fixed voltage (V_{DD} or V_{SS}) there must be a way of switching-off this connection on the PCB. A possible implementation is presented in Fig.7.

In the example (see Fig.7) the POR is enabled in normal mode of operation (pin PORENABLE/V_{PP} = 1 by the pull-up), but the V_{PP} source must supply enough current in R_p in order to guarantee min. 12.5 V on the PORENABLE/V_{PP} pin.

Note that if in the application the Power-on-reset is disabled (pin PORENABLE/V_{PP} = 0), applying a high voltage to the PORENABLE/V_{PP} pin will also enable the POR circuit. This will cause a reset independent of the actual V_{DD} value.

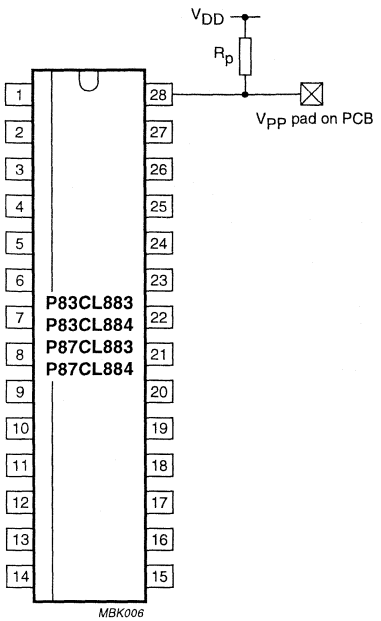


Fig.7 Example of PORENABLE/V_{PP} connection on a PCB.

6.7 Oscillator circuitry

General information on the oscillator circuitry can be found in the *"TELX family"* data sheet.

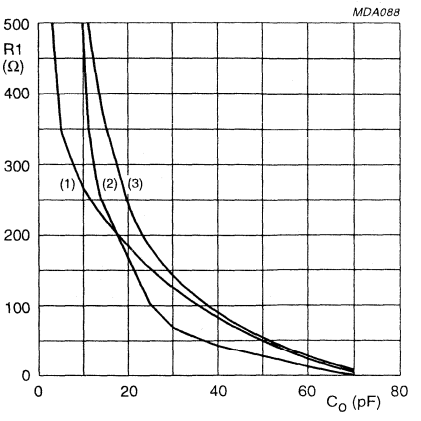
6.7.1 Resonator requirements

For correct function of the oscillator, the values of R_1 and C_0 of the chosen resonator (quartz or PXE) must be below the line shown in Fig.8a. The value of the parallel resistor R_0 must be less than 47 kΩ.

The wiring between chip and resonator should be kept as short as possible.

6.7.2 Recommended resonator types

- CSA 3.58MG (supplier Murata)
- FCR3.58M5 (supplier TDK).



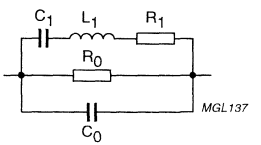
C_{1e} and C_{2e} are the external load capacitances; normally not needed due to integrated load capacitances of typically 10 pF.

(1) $C_{1e} = C_{2e} = 22$ pF.

(2) $C_{1e} = C_{2e} = 0$ pF.

(3) $C_{1e} = C_{2e} = 12$ pF.

a. Resonator curves.



b. Resonator equivalent circuit.

Fig.8 Resonator requirements for the ACO.

6.8 Emulation

The emulator for the P8xCL883/P8xCL884 uses the P87CL880 microcontroller in emulation mode.
The P87CL880 is a super-set of the P8xCL883/P8xCL884, i.e. it contains all the functions of the P8xCL883/P8xCL884 plus a number of other additional functions. It should be noted that some functional differences between P87CL880 and P8xCL883/P8xCL884 exist; see Table 13.

Table 13 Differences between functions existing in P87CL880 and P8xCL883/P8xCL884

FUNCTION	P87CL880	P8xCL883/P8xCL884
Timer 2	see P87CL880 specification	see P8xCL883/P8xCL884 specification
OTP Program Memory	32 kbytes AFPROM	8 kbytes EPROM or pre-programmed ROM
RAM	512 bytes	256 bytes
$\overline{EW}$ pin (Watchdog enable)	yes	no
Security concept	see P87CL880 specification	see P8xCL883/P8xCL884 specification
In System Programming	no	yes
Reset value of SFRs	see P87CL880 specification	see P8xCL883/P8xCL884 specification
POR	hardware programmable	fixed
Frequency	DC to 12.5 MHz	3.58 MHz
Package	QFP64	SO28

6.9 Read-Modify-Write bug

The first versions of P8xCL883/P8xCL884 and P87CL880 contain a bug which affects all instructions of type Read-Modify-Write (RMW) to an I/O port.

The instructions affected are: ANL, ORL, XRL, JBC, CPL, INC, DEC, DJNZ, MOV Px.y,C, CLR Px.y and SET Px.y. The detailed explanation of the normal function of these instructions are explained in the *"Data Handbook IC20; 80C51-based 8-bit Microcontrollers"*.

The ports affected are P0, P1 and P3 on P8xCL883/P8xCL884, and ports P0 and P3 on P87CL880. Normally, a RMW instruction first reads the value which is present on the port latch (not the state of the port pins), modifies this value, and writes it back to the port latch.

Due to a critical timing between two internal signals in the present design, the RMW instructions do not work correctly.Due to the bug, the RMW instructions on the port pins should be avoided. However, a software workaround exist.

Instead of using the normal RMW instruction, each manipulation should be done on a copy-byte of the port latch (e.g. a bit addressable RAM byte for each port), and thereafter the new value of the copy-byte should be written to the port latch. It is important that any value to be written to a port must be copied in the copy-byte, see the example in Section 6.9.1 "Example 1: Writing 'directly' to a port".

6.9.1 EXAMPLE 1: WRITING 'DIRECTLY' TO A PORT

Normally:

```
MOV P1,#53h          ;write value directly to port
```

Work-around:

```
MOV P1copy,#53h      ;write value to copy-byte
MOV P1,P1copy        ;write value of copy-byte to port
```

6.9.2 EXAMPLE 2: SETTING ONE BIT OF THE PORT

Normally:

```
SET P1.0             ;set bit 0 of port P1
```

Work-around:

```
SET P1copy.0         ;set bit 0 of port P1copy, assuming register P1copy is chosen to
                     be in the bit addressable RAM area
MOV P1, P1copy       ;write value of copy-byte to port
```

7 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	–0.5	+4.0	V
V_I	input voltage on any pin with respect to ground (V_{SS})	–0.5	V_{DD} + 0.5	V
P_{tot}	total power dissipation	–	800	mW
T_{stg}	storage temperature	–65	+150	°C

8 CHARACTERISTICS

V_{DD} = 2.7 to 3.6 V; V_{SS} = 0 V; f_{xtal} = 3.58 MHz; T_{amb} = −25 to +70 °C;
T_{amb} (during In System Programming) = +20 to +40 °C; all voltages with respect to V_{SS} unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage					
	operating		2.7	–	3.6	V
	RAM data retention in Power-down mode		1.0	–	3.6	V
	In System Programming		3.0	–	3.6	V
V_{PP}	OTP programming voltage		12.5	–	13.0	V
I_{DD}	operating supply current	V_{DD} = 3 V; note 1	–	–	2.0	mA
		V_{DD} = 3 V; T_{amb} = 25 °C; note 1; see Fig.10	–	1	–	mA
$I_{DD(id)}$	supply current Idle mode	V_{DD} = 3 V; note 2	–	–	0.55	mA
		V_{DD} = 3 V; T_{amb} = 25 °C; note 2; see Fig.11	–	0.26	–	mA
$I_{DD(pd)}$	supply current Power-down mode	V_{DD} = 3 V; T_{amb} = 25 °C; note 3; see Fig.12				
		POR and LVD enabled	–	2	5	µA
		POR and LVD disabled	–	100	–	nA
$I_{DD(block)}$	supply current per block:	V_{DD} = 3 V; T_{amb} = 25 °C; notes 4 and 5				
	EEPROM erase/write		–	460	–	µA
	DTMF	no load on TONE output	–	240	–	µA
	MSK modem		–	140	–	µA
	Watchdog		–	110	–	µA
	I^2C-bus		–	90	–	µA
	UART		–	90	–	µA
	Timer T2		–	90	–	µA
	Timer T0 or T1		–	5	–	µA
Inputs (Ports, MIN, $\overline{RST}$, MOUT0 to MOUT2, PORENABLE)						
V_{IL}	LOW-level input voltage	notes 6 and 7	0	–	$0.2V_{DD}$	V
V_{IH}	HIGH-level input voltage	note 6	$0.8V_{DD}$	–	V_{DD}	V
$\lvert I_{IL} \rvert$	LOW-level input current (ports in Mode 1)	V_{IN} = 0.4 V; note 8; see Fig.9	–	10	50	µA
$\lvert I_{IL(T)} \rvert$	LOW-level input current; HIGH-to-LOW transition (ports in Mode 1)	$V_{IN} = 0.5V_{DD}$; note 8; see Fig.9	–	200	1000	µA
$\lvert I_{LI} \rvert$	input leakage current (ports in Mode 0 or 2)	$V_{SS} \leq V_I \leq V_{DD}$	–	–	1	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Port outputs (Ports, $\overline{RST}$, MOUT0 to MOUT2)						
I_{OL}	LOW-level output current; except P1.3, SDA, SCL and MOUT2	V_{OL} = 0.4 V	2	–	–	mA
I_{OL1}	LOW-level output current; P1.3 (for LED)	V_{OL} = 0.4 V	6	–	–	mA
I_{OL2}	LOW-level output current; SDA, SCL and MOUT2	V_{OL} = 0.4 V; note 9	3	–	–	mA
I_{OH}	HIGH-level output current except P1.3; push-pull options only	$V_{OH} = V_{DD} - 0.4$ V	2	–	–	mA
I_{OH1}	HIGH-level output current P1.3 (for LED); push-pull options only	$V_{OH} = V_{DD} - 0.4$ V	6	–	–	mA
I_{OH2}	HIGH-level output current MOUT2	$V_{OH} = V_{DD} - 0.4$ V	3	–	–	mA
$I_{\overline{RST}}$	$\overline{RST}$ pull-up transistor current	V_{DD} = 3 V; $V_{OH} = V_{DD} - 0.4$ V	5	20	–	µA
		V_{DD} = 3 V; $V_{OH} = V_{SS}$	–	50	200	µA
Power-on-reset (POR); for the LVD (Low Voltage Detection) see note 10						
V_{PORH}	Power-on-reset trip level HIGH	option 5 in *"TELX family"* specification	2.13	2.37	2.61	V
V_{PORL}	Power-on-reset trip level LOW	option A in *"TELX family"* specification	1.98	2.27	2.56	V
TONE output (note 11 and Fig.13)						
$V_{HG(rms)}$	HGF voltage (RMS)	V_{DD} = 3 V	158	181	205	mV
$V_{LG(rms)}$	LGF voltage (RMS)		125	142	160	mV
$\Delta f/f$	frequency deviation		–0.6	–	+0.6	%
V_{DC}	DC voltage level		–	$0.5V_{DD}$	–	V
V_G	pre-emphasis of group		1.5	2.0	2.5	dB
THD	total harmonic distortion	V_{DD} = 3 V; T_{amb} = 25 °C; notes 5 and 12	–	25	–	dB
EEPROM (notes 5 and 13)						
$t_{E/W}$	erase/write time		8	10	12	ms
$N_{E/W}$	erase/write cycles		10^5	–	–	
t_{DR}	data retention time	T_{amb} = +70 °C	10	–	–	years
In System Programming for the OTP						
t_{prog}	program cycle time		90	100	110	µs
$t_{prog(security)}$	program cycle time security	note 14	180	200	220	µs
t_{ver}	verify cycle time		1	–	–	µs
$t_{Vpp(setup)}$	program voltage setup time		10	–	–	µs
$t_{Vpp(max)}$	maximum program voltage time	cumulative for the product lifetime	–	–	60	s
I_{Vpp}	program voltage current	In System Programming	–	–	40	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ACO (Amplitude Controlled Oscillator)						
V_{XTAL1}	external clock signal amplitude peak-to-peak		500	–	V_{DD}	mV
$Z_{i(XTAL1)}$	input impedance on XTAL1		300	1000	–	kΩ
C_{1i}; C_{2i}	input capacitance on XTAL1 and XTAL2	notes 5 and 15	–	10	–	pF

Notes

1. The operating supply current is measured with all output pins disconnected; $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; $\overline{RST} = V_{DD}$; XTAL1 driven with square wave; XTAL2 not connected; fetch of NOP instructions; all derivative blocks disabled.
2. The Idle mode supply current is measured with all output pins and $\overline{RST}$ disconnected; $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; XTAL1 driven with square wave; XTAL2 not connected; all derivative blocks disabled.
3. The Power-down current is measured with all output pins and $\overline{RST}$ disconnected; $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; XTAL1 and XTAL2 not connected;.
4. The typical currents are only for the specific block. To calculate the typical power consumption of the microcontroller, the current consumption of the CPU must be added. Example: the typical current consumption of the microcontroller in operating mode with CPU, Watchdog and UART active can be calculated as (1 + 0.11 + 0.09) mA = 1.2 mA.
5. Verified on sampling basis.
6. The input threshold voltage of P1.6/SCL and P1.7/SDA meet the I^2C-bus specification. Therefore, an input voltage below $0.3V_{DD}$ will be recognized as a logic 0 and an input voltage above $0.7V_{DD}$ will be recognized as a logic 1.
7. For pin PORENABLE the $V_{IL(max)} = 0.1V_{DD}$.
8. Not valid for pins SDA, SCL, $\overline{RST}$, MIN and PORENABLE.
9. The maximum allowed load capacitance C_L is in this case limited to around 200 pF.
10. The LVD is tested according to the specification in the data sheet *"TELX family; Chapter: Low Voltage Detection"*.
11. Values are specified for DTMF frequencies only (CEPT CS203).
12. Related to the Low Group Frequency (LGF) component (CEPT CS203).
13. After final testing the value of each EEPROM bit is typically logic 1.
14. Can also be done by two 100 µs pulses.
15. C_{1i} and C_{2i} are the total internal capacitances (including gate capacitance, leadframe capacitance).

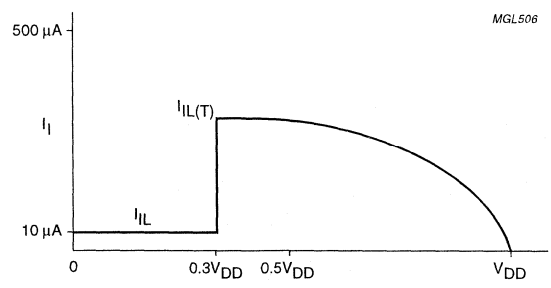


Fig.9 Input current.

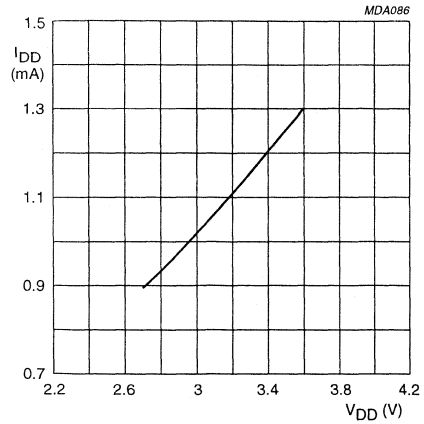


Fig.10 Typical operating current as a function of V_{DD}, T_{amb} = 25 °C.

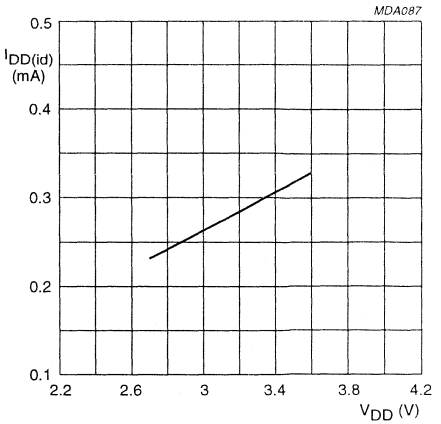
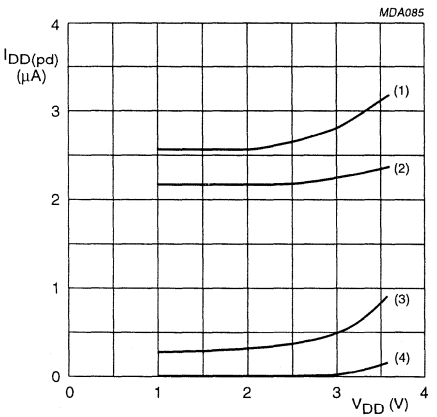
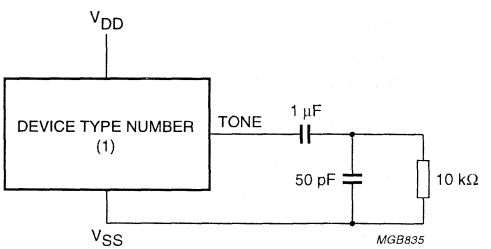


Fig.11 Typical Idle current as a function of V_{DD}, T_{amb} = 25 °C.



(1) POR and LVD enabled (T_{amb} = 70 °C).
(2) POR and LVD enabled (T_{amb} = 25 °C).
(3) POR and LVD disabled (T_{amb} = 70 °C).
(4) POR and LVD disabled (T_{amb} = 25 °C).

Fig.12 Typical Power-down current as a function of V_{DD}.



(1) P8xCL883/P8xCL884.

Fig.13 TONE output test circuit.

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TELX microcontrollers for CT0 handset/basestation applications

P83CL886; P87CL886

1 FEATURES

- Full static 80C51 CPU; enhanced 8-bit architecture with:
  - Minimum 6 cycles per instruction (twice as fast as a standard 80C51 core)
  - Non-page oriented instructions
  - Direct addressing
  - Four 8-byte RAM register banks
  - Stack depth limited only by available internal RAM (maximum 256 bytes)
  - Multiply, divide, subtract and compare instructions
- Three 8-bit ports (18 I/O lines)
- Program Memory:
  - P87CL886: 16 kbytes One Time Programmable
  - P83CL886: 16 kbytes ROM
- 512 bytes RAM
- Amplitude Controlled Oscillator (ACO) suitable for quartz crystal or ceramic resonator
- Improved Power-on/Power-off reset (POR) circuitry
- Low Voltage Detection (LVD) with 11 software programmable levels
- Eight interrupts on Port 1:
  - Edge or level sensitive triggering selectable via software
  - Power-saving use for keyboard control
- Twenty source, twenty vector interrupt structure with two priority levels
- Wake-up from Power-down mode via LVD or external interrupts at Port 1
- DTMF generator
- MSK modem including Manchester encoder/decoder with 2 digital outputs for analog cordless telephones (standards CT0/CT1/CT1+)
- Watchdog Timer
- Two standard 16-bit timer/event counters
- Additional 16-bit timer/event counter with Capture, Compare and Auto-reload function
- Full duplex enhanced UART with double buffering
- I^2C-bus interface for serial transfer on two lines, maximum 400 kHz
- Very low current consumption
- Single supply voltage: 2.7 to 3.6 V
- Frequency: 3.58 MHz
- Operating temperature: –25 to +70 °C
- 28 pin SO package.

2 GENERAL DESCRIPTION

The P8xCL886 (denoting the P83CL886 and P87CL886) are manufactured in an advanced CMOS technology and are 8-bit microcontrollers especially suited for low cost analog cordless telephone applications (CT0, CT1 and CT1+ standards). Consequently, features like DTMF, MSK modem and POR/LVD are integrated on-chip.

Both devices are optimized for low power consumption and in addition have two software selectable modes for further power reduction: Idle and Power-down modes. All derivative blocks can switch off their clock if they are inactive.

The instruction set of the P8xCL886 is based on that of the 80C51. The P8xCL886 also function as arithmetic processors having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 46 two-byte, and 16 three-byte. As port P2 is not implemented there is no external data or memory access and MOVX operations cannot be used.

This data sheet details the specific properties of the P8xCL886; for details of the P8xCL886 core and the derivative functions see the *"TELX family"* data sheet and *"Data Handbook IC20"*.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
P83CL886DFT	SO28[1]	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
P87CL886DFT			

Note

1. When using IR reflow soldering it is recommended that the Dry Packing instructions in the *"Quality Reference Pocketbook"* (order number 9398 510 34011) are followed.

4 BLOCK DIAGRAM

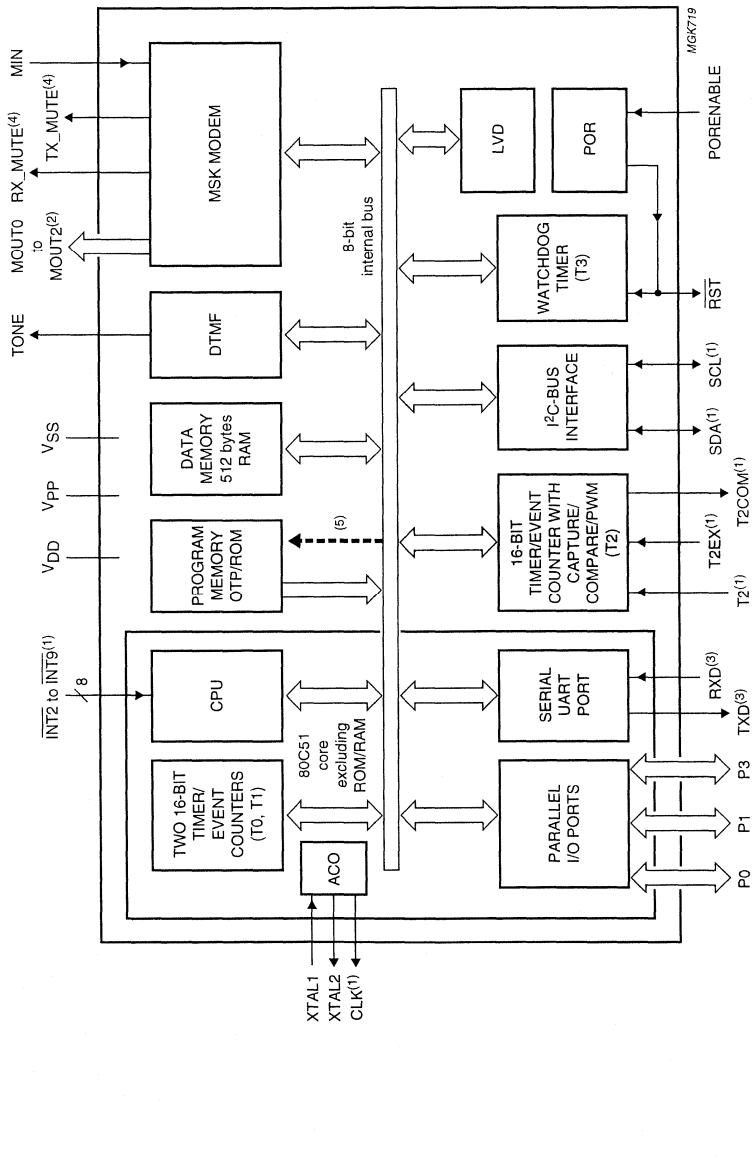


Fig.1 Block diagram.

(1) Alternative functions of Port 1.
(2) MOUT0 is the alternative function to P3.1.
(3) Alternative function of Port 3.
(4) By software any I/O port pin can be used.
(5) In-circuit OTP programming.

5 PINNING INFORMATION

5.1 Pinning

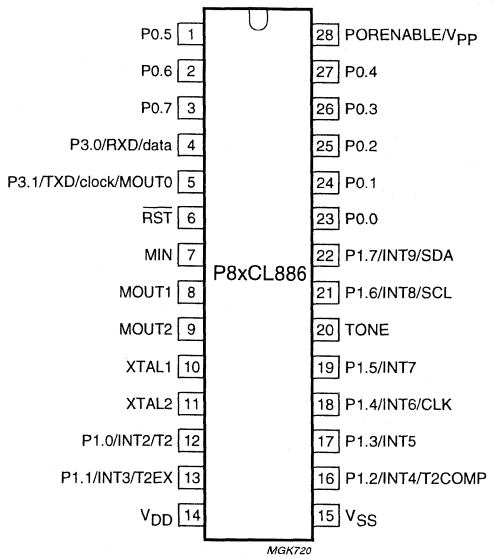


Fig.2 Pin configuration.

5.2 Pin description

Table 1 SO28 package

SYMBOL	PIN	DESCRIPTION
$\overline{RST}$	6	**Active low reset:** a LOW level on this pin for two machine cycles while the oscillator is running, resets the device. The $\overline{RST}$ pin is also an output which can be used to reset other ICs.
MIN	7	Digital **MSK** modem input.
MOUT1	8	Digital **MSK** modem outputs.
MOUT2	9	
XTAL1	10	**Crystal input:** Input to the Amplitude Controlled Oscillator. Also the input for an externally generated clock source.
XTAL2	11	**Crystal output:** Output of the Amplitude Controlled Oscillator; to be left non-connected when an external oscillator clock is used.
V_{DD}	14	Power supply.
V_{SS}	15	Ground.
P0.0 to P0.7	23 to 27, 1 to 3	**Port 0:** 8-bit bidirectional I/O port; every port pin can be used as open-drain, standard port, high-impedance input or push-pull output, according to Section 6.2.
P1.0/INT2/T2	12	**Port 1:** 8-bit bidirectional I/O port with alternative functions. Every port pin except P1.6 and P1.7 (I^2C-bus pins) can be used as open-drain, standard port, high-impedance input or push-pull output, according to Section 6.2. Port P1.3 has LED drive capability. Port 1 also serves the alternative functions: **INT2 to INT9** interrupts; Timer T2 external inputs **T2** and **T2EX**; Timer T2 compare output **T2COMP**; external clock output **CLK**; I^2C-bus clock **SCL** and data in/outputs **SDA**.
P1.1/INT3/T2EX	13	
P1.2/INT4/T2COMP	16	
P1.3/INT5	17	
P1.4/INT6/CLK	18	
P1.5/INT7	19	
P1.6/INT8/SCL	21	
P1.7/INT9/SDA	22	
P3.0/RXD/data	4	**Port 3:** 3 or 2-bit bidirectional I/O port with alternative functions. Every port pin can be used as open-drain, standard port, high-impedance input or push-pull output, according to Chapter 6.2. Port 3 also serves the alternative functions: **RXD/data** is the serial port receiver data input (asynchronous) or data I/O (synchronous); **TXD/clock** is the serial port transmitter data output (asynchronous) or clock output (synchronous) or digital MSK modem output **MOUT0**.
P3.1/TXD/clock/ MOUT0	5	
TONE	20	**DTMF** output.
PORENABLE/V_{PP}	28	**PORENABLE**: Power-on-reset circuit enable. If PORENABLE = 1, the internal Power-on-reset circuit is enabled. If external reset circuitry is used, it is recommended to keep PORENABLE = 0 to reach lowest power consumption. This pin is also used for the OTP programming voltage V_{PP}.

6 FUNCTIONAL DESCRIPTION

6.1 Special Function Registers

Table 2 Special Function Registers memory map and reset values

REGISTER NAME	REGISTER MNEMONIC	SFR ADDRESS	RESET VALUE[1]
80C51 core			
Accumulator	ACC	E0H	0000 0000
B Register	B	F0H	0000 0000
Data Pointer Low byte	DPL	82H	0000 0000
Data Pointer High byte	DPH	83H	0000 0000
Program Counter High byte	PCH	no SFR	0000 0000
Program Counter Low byte	PCL	no SFR	0000 0000
Power Control Register	PCON	87H	0000 0000
Prescaler Register	PRESC	F3H	0000 0000
Program Status Word	PSW	D0H	0000 0000
Stack Pointer	SP	81H	0000 0111
Timer 0 and Timer 1			
Timer/Counter Control Register	TCON	88H	0000 0000
Timer/Counter 0 High byte	TH0	8CH	0000 0000
Timer/Counter 1 High byte	TH1	8DH	0000 0000
Timer/Counter 0 Low byte	TL0	8AH	0000 0000
Timer/Counter 1 Low byte	TL1	8BH	0000 0000
Timer/Counter Mode Control Register	TMOD	89H	0000 0000
Ports			
Alternative Port Function Control Register	ALTP	A3H	0000 0000
Port P0 Output Data Register	P0	80H	1111 1111
Port P0 Configuration A Register	P0CFGA	8EH	1111 1111
Port P0 Configuration B Register	P0CFGB	8FH	0000 0000
Port P1 Output Data Register	P1	90H	1111 1111
Port P1 Configuration A Register	P1CFGA	9EH	0011 1111
Port P1 Configuration B Register	P1CFGB	9FH	0000 0000
Port P3 Output Data Register	P3	B0H	XXXX XX11
Port P3 Configuration A Register	P3CFGA	BEH	XXXX XX11
Port P3 Configuration B Register	P3CFGB	BFH	XXXX XX00
Port P4 Output Data Register	P4	C1H	XXXX XXX0[2]

REGISTER NAME	REGISTER MNEMONIC	SFR ADDRESS	RESET VALUE[1]
Timer 2			
Timer 2 Compare High byte	COMP2H	ABH	0000 0000
Timer 2 Compare Low byte	COMP2L	AAH	0000 0000
Timer 2 Reload/Capture High byte	RCAP2H	CBH	0000 0000
Timer 2 Reload/Capture Low byte	RCAP2L	CAH	0000 0000
Timer/Counter 2 Control Register	T2CON	C8H	0000 0000
Timer/Counter 2 High byte	TH2	CDH	0000 0000
Timer/Counter 2 Low byte	TL2	CCH	0000 0000
DTMF			
High Group Frequency Register	HGF	A2H	0000 0000
Low Group Frequency Register	LGF	A1H	0000 0000
Interrupt logic			
Interrupt Enable Register 0	IEN0	A8H	0000 0000
Interrupt Enable Register 1	IEN1	E8H	0000 0000
Interrupt Enable Register 2	IEN2	F1H	0000 0000
Interrupt Priority Register 0	IP0	B8H	0000 0000
Interrupt Priority Register 1	IP1	F8H	0000 0000
Interrupt Priority Register 2	IP2	F9H	0000 0000
Interrupt Sensitivity Register 1	ISE1	E1H	0000 0000
Interrupt Polarity Register	IX1	E9H	0000 0000
Interrupt Request Flag Register 1	IRQ1	C0H	0000 0000
Low Voltage Detection			
LVD Control Register	LVDCON	F2H	0000 0000
POR/ACO			
Reset Status Register	RSTAT	E6H	XXX0 1001[3]
MSK modem			
MSK Modem Control Register	MCON	D3H	0000 0000
MSK Modem Data Buffer	MBUF	D1H	XXXX XXXX
MSK Modem Status Register	MSTAT	D2H	XX00 0000

REGISTER NAME	REGISTER MNEMONIC	SFR ADDRESS	RESET VALUE[1]
UART			
Serial Port Buffer	S0BUF	99H	0000 0000
Serial Port Control Register	S0CON	98H	0000 0000
I²C-bus interface			
Address Register	S1ADR	DBH	0000 0000
Serial Control Register	S1CON	D8H	0000 0000
Data Shift Register	S1DAT	DAH	0000 0000
Serial Status Register	S1STA	D9H	1111 1000
Watchdog Timer			
Watchdog Timer Control Register	WDCON	A5H	1010 0101
Watchdog Timer Interval Register	WDTIM	FFH	0000 0000
OTP interface			
OTP Address High Register	OAH	D5H	X00X XXXX
OTP Address Low Register	OAL	D4H	XXXX XXXX
OTP Data Register	ODATA	D6H	XXXX XXXX
OTP In System Programming Register	OISYS	DCH	000X 0000
OTP Test Register	OTEST	C7H	0000 0000
Reserved locations, see note 4			
–	–	E7H, FDH	–

Notes

1. Where: X = undefined state or not implemented bit.
2. Only used to define MSK input polarity. Write only.
3. Defined by mask.
4. E7H and FDH are reserved locations and must not be written to.

6.2 I/O facilities

6.2.1 PORTS

The P8xCL886 have 18 I/O lines, treated as 18 individually addressable bits or as three parallel 8-bit addressable ports. The alternative functions are detailed below:

Port 0 Offers no alternative functions.

Port 1 Used for a number of special functions:

- P1.0 to P1.7 provides the inputs for the external interrupts INT2 to INT9
- P1.2/T2COMP for external activation and Compare/Auto-reload output function of Timer 2
- P1.4/CLK for the clock output
- P1.6/SCL and P1.7/SDA for the I^2C-bus interface are real open-drain outputs or high-impedance; no other port configurations are available.

Port 2 Not available.

Port 3 Pins can be configured individually to provide:

- P3.0/RXD/data and P3.1/TXD/clock/MOUT0 are serial port receiver input and transmitter output (UART).

To enable a Port pin alternative function, the Port bit latch in its SFR must contain a logic 1.

Each port consists of a latch (Special Function Registers P0 to P3), an output driver and input buffer. All ports have internal pull-ups. Figure 3b shows that the strong transistor 'p1' is turned on for only one oscillator period after a LOW-to-HIGH transition in the port latch. When on, it turns on 'p3' (a weak pull-up) through the inverter IN1. This inverter and transistor 'p3' form a latch which holds the logic 1.

Port P1.3 has LED drive capability.

6.2.2 PORT I/O CONFIGURATION

I/O port output configurations are determined by the settings in the port configuration SFRs. There are 2 SFRs for each port: PnCFGA and PnCFGB, where 'n' indicates the specific port number (0 to 3).

One bit in each of the 2 SFRs relates to the output setting for the corresponding port pin, allowing any combination of the 2 output types to be mixed on those port pins. For instance, the output type of Port 1 pin 3 is controlled by the setting of bit 3 in the SFRs P1CFGA and P1CFGB.

The port pins may be individually configured via SFRs with one of the following modes (P1.6 and P1.7 can be open-drain or high-impedance but never have any diodes against V_{DD}). These modes are also shown in Fig.3.

Mode 0 Open-drain; quasi-bidirectional I/O with n-channel open-drain output. Use as an output requires the connection of an external pull-up resistor; e.g. Port 0 for external memory accesses (EA = 0) or access above the built-in memory boundary. The ESD protection diodes against V_{DD} and V_{SS} are still present; see Fig.3b Except for the I^2C pins P1.6 and P1.7, ports which are configured as open-drain still have a protection diode to V_{DD}.

Mode 1 Standard port; quasi-bidirectional I/O with pull-up. The strong pull-up 'p1' is turned on for only two oscillator periods after a LOW-to-HIGH transition in the port latch. After these two oscillator periods the port is only weakly driven through 'p2' and 'very weakly' driven through 'p3' see Fig.3b.

Mode 2 High-impedance; this mode turns off all output drivers on a port. Thus, the pin will not source or sink current and may be used as an input-only pin with no internal drivers for an external device to overcome see Fig.3c.

Mode 3 Push-pull; output with drive capability in both polarities. Under this mode, pins can only be used as outputs see Fig.3d.

Tables 3 and 4 show the configuration register settings for the 4 port output types.

The electrical characteristics of each output type can be found in Chapter 8. The default port configuration after reset is given in Table 4.

Table 3 Port Configuration Registers PnCFGA and PnCFGB (n = 0,1 and 3) settings

MODE[1]	PnCFGA	PnCFGB	PORT OUTPUT CONFIGURATION	
			NORMAL PORTS	I²C-BUS PORTS (P1.6 AND P1.7)
Mode 0	0	0	open-drain	open-drain
Mode 1	1	0	quasi-bidirectional	open-drain
Mode 2	0	1	high-impedance	high-impedance
Mode 3	1	1	push-pull	open-drain

Note

1. Mode changes may cause glitches to occur during transitions. When modifying both registers, WRITE instructions should be carried out consecutively.

Table 4 Special Function Registers for port configurations/data

REGISTER NAME	REGISTER MNEMONIC	SFR ADDRESS (HEX)	STATE AFTER RESET
Port P0 Output Data[1]	P0	80	11111111
Port P0 Configuration A	P0CFGA	8E	11111111
Port P0 Configuration B	P0CFGB	8F	00000000
Port P1 Output Data[1]	P1	90	11111111
Port P1 Configuration A	P1CFGA	9E	00111111
Port P1 Configuration B	P1CFGB	9F	00000000
Port P3 Output Data[1]	P3	B0	XXXXXX11
Port P3 Configuration A	P3CFGA	BE	XXXXXX11
Port P3 Configuration B	P3CFGB	BF	XXXXXX00

Note

1. This means that P0, P1.0 to P1.5 and P3 are initialized in Mode 1 (quasi-bidirectional, driving a weak HIGH) and the I²C-bus ports P1.6 and P1.7 are initialized in Mode 0 (open-drain, not driven).

6.2.3 Alternative Port Function Control Register (ALTP)

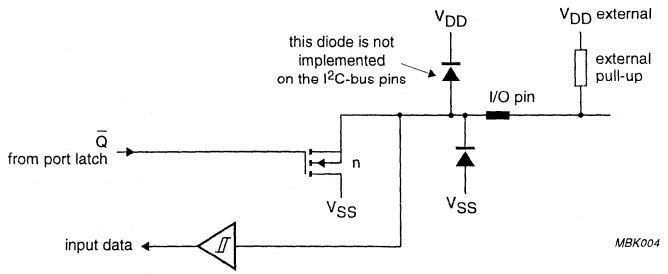
This 4-bit register controls the alternative functions of certain port pins.

Table 5 Alternative Port Function Register (SFR address A3H)

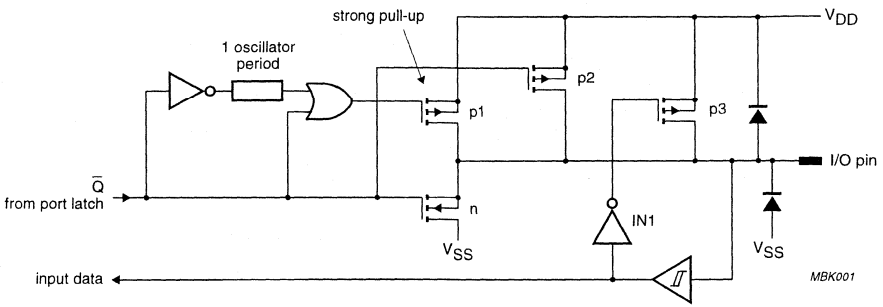
7	6	5	4	3	2	1	0
–	–	–	–	EMOUT0	ECLK	EMLDY	ETONE

Table 6 Description of ALTP bits

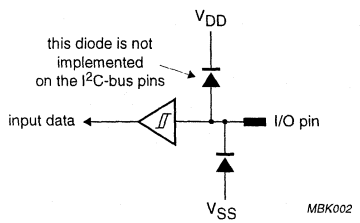
BIT	SYMBOL	DESCRIPTION
7 to 4	–	reserved
3	EMOUT0	**Enable MOUT0.** If this bit is set, P3.1 will output the MOUT0 signal.
2	ECLK	**Enable Clock.** If this bit is set, P1.4 is configured to be push-pull, and P1.4 will output the system clock.
1	EMLDY	**Enable MLDY.** If this bit is set, P1.5 is configured to be push-pull, and P1.5 will output the digital MLDY signal of the DTMF generator.
0	ETONE	**Enable TONE.** If this bit is set, the TONE output of the DTMF generator is enabled.



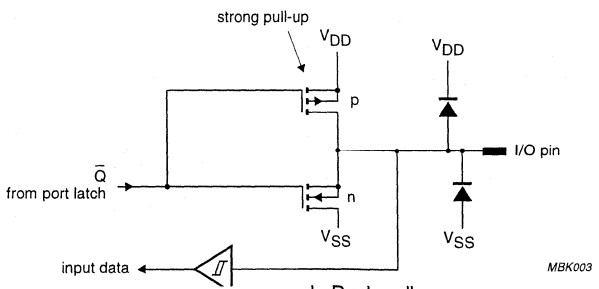
a. Open-drain.



b. Standard/quasi-bidirectional.



c. High-impedance.



d. Push-pull.

Fig.3 Port configuration options.

6.3 Timer/event counters

The P8xCL886 contain three 16-bit timer/event counters: Timer 0, Timer 1 and Timer 2 which can perform the following functions:

- Measure time intervals and pulse durations
- Count events (T2 only, no external input for T0/T1)
- Generate interrupt requests
- Generate output on comparator match.

In the 'timer' mode the register is incremented every machine cycle.

Since a machine cycle consists of minimum 6 oscillator periods, the maximum count rate is $1/6 \times f_{osc}$.

In the 'counter' mode, the register is incremented in response to a HIGH-to-LOW transition. Since it takes one machine cycle (minimum 6 oscillator periods) to recognize a HIGH-to-LOW transition, the maximum count rate is $1/6 \times f_{osc}$. To ensure a given level is sampled, it should be held for at least one complete machine cycle.

Timer 0 and Timer 1 can be programmed independently to operate in four modes:

Mode 0 8-bit timer or 8-bit counter each with divide-by-32 prescaler.

Mode 1 16-bit time-interval or event counter.

Mode 2 8-bit time-interval or event counter with automatic reload upon overflow.

Mode 3 Timer 0 establishes TL0 and TH0 as two separate counters.

6.3.1 TIMER T2

Note that the timer T2 of the P8xCL886 deviates from the timer T2 described in the *"TELX family"* data sheet.

Timer T2 is a 16-bit timer/counter that can operate either as a timer or as an event counter. These functions are selected by the state of the C/$\overline{T2}$ bit in the T2CON register. Five operating modes are available:

- Capture
- Compare
- Auto-reload
- Compare with Auto-reload
- Capture and Compare.

These modes are selected via the T2CON register.

6.3.1.1 Capture mode

In the Capture mode, two options may be selected by the EXEN2 bit in T2CON:

- If EXEN2 = 0, then Timer 2 is a 16-bit timer or counter which upon overflowing sets the Timer 2 overflow bit TF2, this may then be used to generate an interrupt.
- If EXEN2 = 1, Timer 2 operates as described above but with the additional feature that a HIGH-to-LOW transition at external input T2EX causes the current value in TL2 and TH2 to be captured into registers RCAP2L and RCAP2H respectively. In addition, the transition at T2EX causes the EXF2 bit in T2CON to be set; this may also be used to generate an interrupt.

The Capture mode is shown in Fig.4.

6.3.1.2 Compare mode

In the Compare mode, each time timer T2 is incremented, the contents of the compare registers COMP2H and COMP2L are compared with the new counter value of timer T2. When a match occurs, the interrupt flag COMP in register T2CON and port bit P1.2 are toggled. The 16-bit value held in these registers is preset by software. The first toggle after a reset will set the flag COMP. The Compare mode is shown in Fig.4.

6.3.1.3 Auto-reload mode

In the Auto-reload mode there are also two options selected by the EXEN2 bit in T2CON:

- If EXEN2 = 0, then when Timer 2 rolls over, it sets the TF2 bit but also causes the Timer 2 registers to be reloaded with the 16-bit value held in registers RCAP2L and RCAP2H. The 16-bit value held in these registers is preset by software.
- If EXEN2 = 1, Timer 2 operates as described above but with the additional feature that a HIGH-to-LOW transition at external input T2EX will also trigger the 16-bit reload and set the EXF2 bit.

6.3.1.4 Compare with Auto-reload mode

The Auto-reload mode can be used together with the Compare mode. The Auto-reload modes are shown in Fig.5.

6.3.1.5 Capture and Compare modes

The Capture and the Compare mode of timer T2 can be used separately or simultaneously. The function is chosen via the bits ECOMP, CP/$\overline{RL2}$ and TR2 in register T2CON.

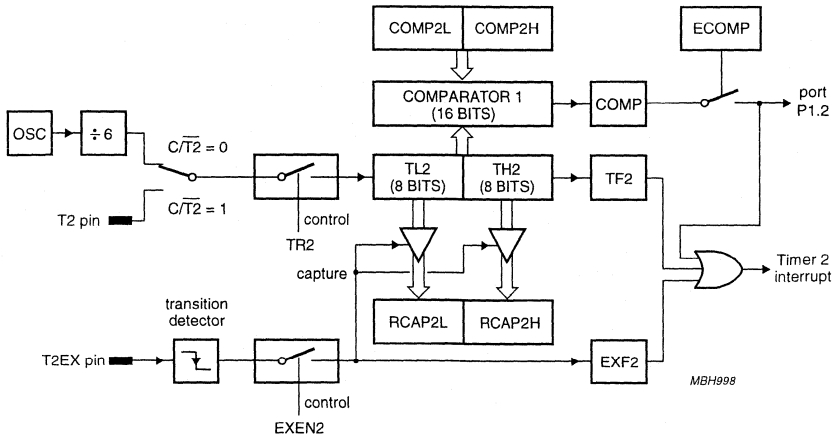


Fig.4 Timer 2 in Capture and/or Compare mode.

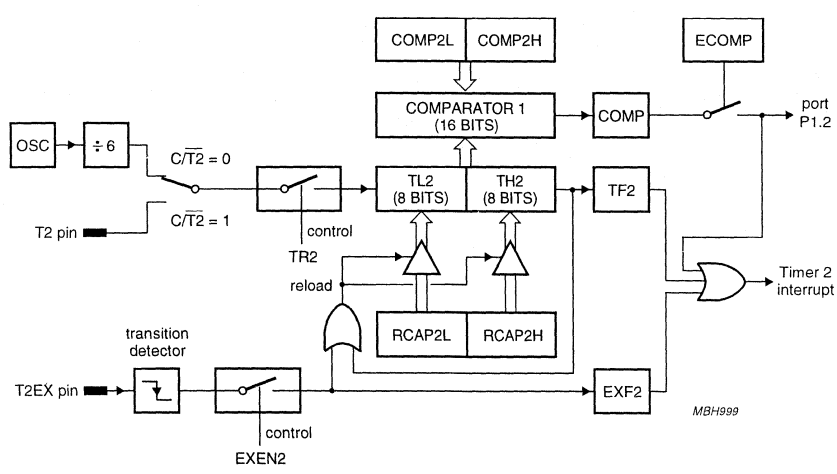


Fig.5 Timer 2 in Auto-Reload with/without Compare mode.

6.3.2 Timer/Counter 2 Control Register (T2CON)

Table 7 Timer/Counter 2 Control Register (SFR address C8H)

7	6	5	4	3	2	1	0
TF2	EXF2	COMP	ECOMP	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$

Table 8 Description of T2CON bits

BIT	SYMBOL	DESCRIPTION
7	TF2	**Timer 2 overflow flag.** TF2 is set by a Timer 2 overflow and must be cleared by software.
6	EXF2	**Timer 2 external flag.** EXF2 is set when either a capture or reload is caused by a negative transition on T2EX and when EXEN2 = 1. When Timer T2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to Timer 2 interrupt routine. EXF2 must be cleared by software.
5	COMP	**Interrupt flag**. When a match between the 16-bit compare register (COMP2L and COMP2H) and the new counter value of timer T2 occurs, the interrupt flag COMP in register T2CON and port bit P1.2 are toggled.
4	ECOMP	**Enable compare output bit.** When set by software, the controller toggles port bit P1.2 (T2COMP) when a compare match occurs.
3	EXEN2	**Timer 2 external enable flag.** When set, allows a capture or reload to occur as a result of a negative transition on T2EX. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
2	TR2	**Timer 2 start/stop control.** Control bit for Timer 2.
1	C/$\overline{T2}$	**Timer 2 timer or counter select.** C/$\overline{T2}$ = 0 selects the internal timer with a clock frequency of $\frac{1}{6} \times f_{osc}$. C/$\overline{T2}$ = 1 selects the external event counter; negative edge-triggered.
0	CP/$\overline{RL2}$	**Capture/reload flag.** When set captures will occur on negative transitions at T2EX, if EXEN2 = 1. When cleared, auto-reloads will occur either with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1.

Table 9 Timer 2 operating modes

ECOMP	CP/$\overline{RL2}$	TR2	MODE
0	0	1	16-bit Auto-reload
0	1	1	16-bit Capture
1	0	1	16-bit Compare
1	1	1	16-bit Capture and Compare
1	0	0	16-bit Compare with Auto-reload
0	0	0	off

6.4 MSK modem

For the P8xCL886, MIN has its own dedicated pin and is no longer the alternative function of P4.0. The polarity of MIN can however still be programmed with the P4.0 bit. P4.0 is a data SFR but no port logic is connected.

Only the most significant bits of MOUT, i.e. MOUT2 and MOUT1 are directly available as separate pins. In order to be able to further increase the signal quality, the MOUT0 signal is available as alternative port function of P3.1.

For controlling this alternative port function the EMOUT0 bit has been added to the Alternative Port Function Register (ALTP); see Section 6.2.3.

6.5 Watchdog Timer (T3)

The Watchdog Timer differs from the description given in the *"TELX family"* data sheet in that the external $\overline{EW}$ pin does not exist on the P8xCL886.

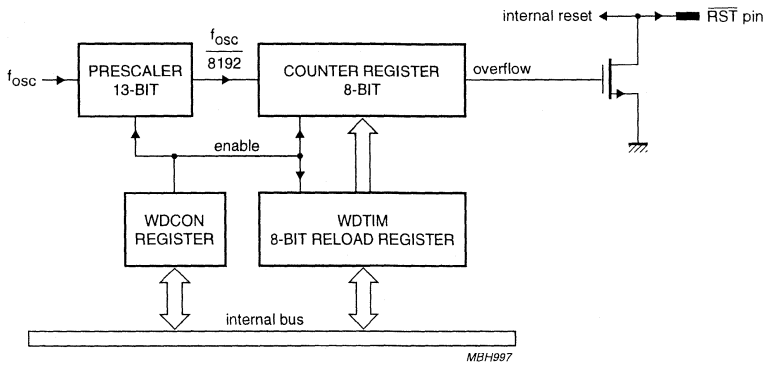


Fig.6 Functional diagram of the Watchdog Timer.

6.6 OTP programming

6.6.1 OTP PROGRAMMING BY A PROGRAMMER

The 16 kbytes One Time Programmable (OTP) memory can be programmed by using a programmer (OM4260) together with a programmer adapter OM5508. Since the memory is programmable only once, programming an already programmed address results in a logical AND of the old and new code. The OTP code can be read out by the programmer for verification.

6.6.1.1 Signature bytes

The OTP memory contains three signature bytes which can be read by the programmer to identify the device. A special address space has been used for these bytes which does not influence the user address space.

The values of the signature bytes are:

(030H) = 15H, indicates manufactured by Philips Semiconductors

(031H) = C8H, indicates P87CL886

(060H) = 00H, currently not used.

6.6.1.2 Security

The following protection levels are available to protect TELX applications against software piracy and unwanted access to data stored in the application.

1. Preventing programming of an already programmed OTP. Note that security Level 1 also disables In System Programming.
2. Preventing the reading of program code in OTP by disabling access of the programmer to the Program Memory. Also verification of code during In System Programming is disabled. In this mode signature and security level verification is still possible.
3. This level has the same functionality as Level 2.

Table 10 describes how these protection levels can be selected by programming the three least significant bits of the security byte.

Table 10 Protection level selection

BITS	LEVEL	DESCRIPTION
UUU	0	no security
UUP	1	Level 1 is activated
UPP	2	Levels 1 and 2 are activated
PPP	3	Levels 1, 2 and 3 are activated

6.6.2 IN SYSTEM PROGRAMMING MODE

In the In System Programming mode the OTP can be programmed under the control of the CPU. A control program must be available in the OTP. This mode can be used to program several bytes in the OTP if the chip is already in a system e.g. to store tuning parameters.

In the In System Programming mode the complete address space OTP can be programmed.

The user should take care not to overwrite the existing code.

For In System Programming four SFRs are used to control the OTP.

Table 11 SFRs for In System Programming

SFR NAME	DESCRIPTION
OAH	OTP Address High Register
OAL	OTP Address Low Register
ODATA	OTP Data Register
OISYS	OTP In System Register; see Section 6.6.2.5

6.6.2.1 Mode entry

The In System Programming mode is entered by setting the InSysMode bit of the OISYS SFR. The I^2C-bus is used for data transfer in this mode. If the I^2C-bus interface is addressed by an external master, the interface generates an interrupt request. The interrupt handler can now read the OISYS SFR and determine the status of the external high voltage (VPon). If high voltage is not present the interrupt is a standard I^2C-bus interrupt.

If high voltage is present the In System Program interrupt routine has to start writing the InSysMode bit (OISYS.0) and control the address and data transfer.

During In System Programming the OTP memory has to be in DC read mode. This is achieved by writing 08H to the OTEST SFR. If the In System Programming mode is left, 00H must be written into the OTEST SFR.

The program voltage has to be available and stable for at least 10 µs before the mode is entered and must remain stable until the circuit has left the In System Programming mode. The high voltage can be applied for maximum 60 seconds during the complete lifetime of the circuit.

6.6.2.2 Program cycle

The data and address have to be supplied to the microcontroller and the control program must write to the

SFRs: ODATA, OAH and OAL. A timer has to be initialized for a 100 µs cycle and the WE bit of the OISYS SFR has to be set. Now the core must be set into the Idle mode. As long as the circuit is in Idle mode a programming pulse is applied. After the interrupt request of the timer the OTP is available for normal code fetching.

The address applied to the OAH and OAL SFRs must be in the 16 kbytes address space.

6.6.2.3 Verify for In System Programming

Verify is done in a similar way as programming. The circuit is put into the Idle mode and at the start of this mode the sense amplifiers are switched to verify mode and a read cycle is started. The timer has to be initialized for a cycle of at least 1 µs. The address is supplied by the SFRs OAH and OAL. The WE bit of the OISYS SFR has to be reset. The OTP output data is latched in the ODATA SFR. After Idle mode is finished this SFR can be read in the normal way.

To be sure that the verified data is written into the SFR it is advised to write FFH into the ODATA SFR before a verify is started.

6.6.2.4 Signature bytes and security

Signature bytes can be read by setting the SIG bit of the OISYS SFR and applying the address of the signature byte. Applying a write pulse while the SIG bit of the OISYS SFR is HIGH is forbidden although the contents of the signature bytes will never be destroyed. The signature bytes (and other test addresses) are always readable independent of the security.

Security has the same meaning as in Parallel Program mode. Security can be programmed and verified by setting the SEC bit of the OISYS SFR. The security bits can be programmed like normal bits. To program Level 1, 01H must be loaded in the ODATA SFR. These values are 03H and 07H for Level 2 and Level 3 respectively. The SEC bit of the OISYS SFR must be HIGH during the program cycle. Loading an address is not necessary. The timer must be initialized for 200 µs instead of 100 µs for security or two standard pulses must be applied. If the SEC bit is HIGH during verify, the security bits can be read from the ODATA SFR. Verifying a normal address while security level (Level 2 or Level 3) has been programmed will result in reading 00H.

Verifying is disabled immediately after programming Level 2 or Level 3. Programming is disabled if a verify or a reset is applied after programming security level: Level 1 or higher.

6.6.2.5 OTP In System Programming Register (OISYS)

The OISYS SFR controls the In System Programming mode. The data to be programmed is stored in the SFR ODATA and the address for this data in the SFRs OAH and OAL.

Table 12 OTP In System Programming Register (SFR address DCH)

7	6	5	4	3	2	1	0
–	–	–	VPon	SEC	SIG	WE	InSysMode

Table 13 Description of OISYS bits

BIT	SYMBOL	DESCRIPTION
7 to 5	–	reserved
4	VPon	V_{PP} status (read only)
3	SEC	security bits enable
2	SIG	signature bytes enable
1	WE	Write Enable, enables programming
0	InSysMode	In System Programming status bit

6.6.2.6 *How to connect the PORENABLE/V_{PP} pin in the In System Programming mode*

If the V_{PP} pin is dual-mode (e.g. PORENABLE/V_{PP}), ICs connected to the signal PORENABLE **must be able to withstand up to 13 V**, i.e. cannot have clamping diodes or low break-down voltages. If the pin is connected to a fixed voltage (V_{DD} or V_{SS}) there must be a way of switching-off this connection on the PCB. A possible implementation is presented in Fig.7.

In the example (see Fig.7) the POR is enabled in normal mode of operation (pin PORENABLE/V_{PP} = 1 by the pull-up), but the V_{PP} source must supply enough current in R_p in order to guarantee a minimum of 12.5 V on the PORENABLE/V_{PP} pin.

Note that if in the application the Power-on-reset is disabled (pin PORENABLE/V_{PP} = 0), applying a high voltage to the PORENABLE/V_{PP} pin will also enable the POR circuit. This will cause a reset independent of the actual V_{DD} value.

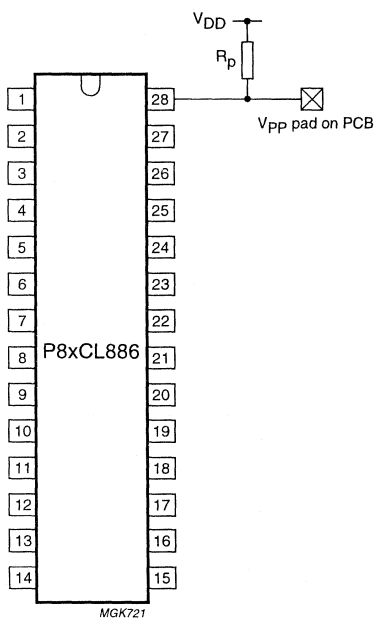


Fig.7 Example of PORENABLE/V_{PP} connection on a PCB.

6.7 Oscillator circuitry

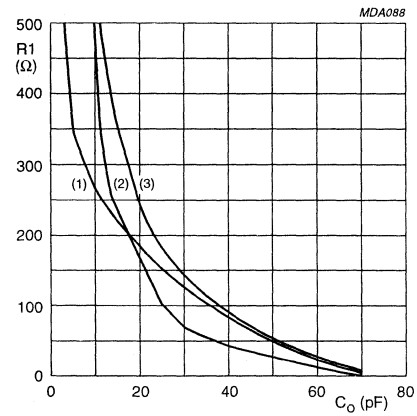
General information on the oscillator circuitry can be found in the *"TELX family"* data sheet.

6.7.1 RESONATOR REQUIREMENTS

For correct function of the oscillator, the values of R_1 and C_0 of the chosen resonator (quartz or PXE) must be below the line shown in Fig.8a. The value of the parallel resistor R_0 must be less than 47 kΩ. The wiring between chip and resonator should be kept as short as possible.

6.7.2 RECOMMENDED RESONATOR TYPES

- CSA 3.58MG (supplier Murata)
- FCR3.58M5 (supplier TDK).



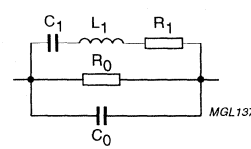
C_{1e} and C_{2e} are the external load capacitances; normally not needed due to integrated load capacitances of typically 10 pF.

(1) $C_{1e} = C_{2e}$ = 22 pF.

(2) $C_{1e} = C_{2e}$ = 0 pF.

(3) $C_{1e} = C_{2e}$ = 12 pF.

a. Resonator curves.



b. Resonator equivalent circuit.

Fig.8 Resonator requirements for the ACO.

6.8 Emulation

The emulator for the P8xCL886 uses the P87CL880 microcontroller in emulation mode. The P87CL880 is a super-set of the P8xCL886, i.e. it contains all the functions of the P8xCL886 plus a number of other additional functions. It should be noted that some functional differences between the P87CL880 and the P8xCL886 exist; see Table 14.

Table 14 Differences between functions existing in P87CL880 and P8xCL886

FUNCTION	P87CL880	P8xCL886
Timer 2	see P87CL880 specification	see P8xCL886 specification
OTP Program Memory	32 kbytes AFPROM	16 kbytes EPROM or pre-programmed ROM
$\overline{EW}$ pin (Watchdog enable)	yes	no
Security concept	see P87CL880 specification	see P8xCL886 specification
In System Programming	no	yes
Reset value of SFRs	see P87CL880 specification	see P8xCL886 specification
POR	hardware programmable	fixed
Frequency	DC to 12.5 MHz	3.58 MHz
Read-Modify-Write bug	Yes	No

6.9 Read-Modify-Write bug

The first version of P87CL880 which is used in the emulator for the P8xCL886 contains a bug which affects all instructions of type Read-Modify-Write (RMW) to an I/O port. The instructions affected are: ANL, ORL, XRL, JBC, CPL, INC, DEC, DJNZ, MOV Px.y, C, CLR Px.y and SET Px.y. Detailed explanations of the normal function of these instructions are explained in *"Data Handbook IC20"*.

The ports affected are port P0 and P3 on P87CL880.

Normally, a RMW instruction first reads the value which is present on the port latch (not the state of the port pins), modifies this value, and writes it back to the port latch.

Due to a critical timing between two internal signals in the present design, the RMW instructions do not work correctly.

Due to the bug, the RMW instructions on the port pins should be avoided. However, a software work around exist.

Instead of using the normal RMW instruction, each manipulation should be done on a copy-byte of the port latch (e.g. a bit addressable RAM byte for each port), and thereafter the new value of the copy-byte should be written to the port latch. It is important that any value to be written to a port must be copied in the copy-byte, see Example 1.

6.9.1 Example 1: Writing 'directly' to a port

Normally:

```
MOV P1,#53h          ;write value directly to port
```

Work-around:

```
MOV P1copy,#53h      ;write value to copy-byte
MOV P1,P1copy        ;write value of copy-byte to port
```

6.9.2 Example 2: Setting one bit of the port

Normally:

```
SET P1.0             ;set bit 0 of port P1
```

Work-around:

```
SET P1copy.0         ;set bit 0 of port P1copy, assuming register P1copy is chosen to
                     be in the bit addressable RAM area
MOV P1, P1copy       ;write value of copy-byte to port
```

7 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	–0.5	+4.0	V
V_I	input voltage on any pin with respect to ground (V_{SS})	–0.5	V_{DD} + 0.5	V
P_{tot}	total power dissipation	–	800	mW
T_{stg}	storage temperature	–65	+150	°C

8 CHARACTERISTICS

V_{DD} = 2.7 to 3.6 V; V_{SS} = 0 V; f_{xtal} = 3.58 MHz; T_{amb} = –25 to +70 °C; (during In System Programming T_{amb} = 20 to 40 °C). All voltages with respect to V_{SS} unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage					
	operating		2.7	–	3.6	V
	RAM data retention in Power-down mode		1.0	–	3.6	V
	In System Programming		3.0	–	3.6	V
V_{PP}	OTP programming voltage		12.5	–	13.0	V
I_{DD}	operating supply current	V_{DD} = 3 V; note 1	–	–	2.0	mA
		V_{DD} = 3 V; T_{amb} = 25 °C; note 1; see Fig.9	–	1	–	mA
$I_{DD(id)}$	supply current Idle mode	V_{DD} = 3 V; note 2	–	–	0.55	mA
		V_{DD} = 3 V; T_{amb} = 25 °C; note 2; see Fig.10	–	0.26	–	mA
$I_{DD(pd)}$	supply current Power-down mode	V_{DD} = 3 V; T_{amb} = 25 °C; note 3; see Fig.11				
		POR and LVD enabled	–	2	5.0	µA
		POR and LVD disabled	–	100	–	nA
$I_{DD(block)}$	supply current per block:	V_{DD} = 3 V; T_{amb} = 25 °C; notes 4 and 5				
	DTMF	no load on TONE output	–	240	–	µA
	MSK modem		–	140	–	µA
	Watchdog		–	110	–	µA
	I^2C-bus		–	90	–	µA
	UART		–	90	–	µA
	Timer T2		–	90	–	µA
	Timer T0 or T1		–	5	–	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs (Ports, MIN, RST, MOUT0 to MOUT2 and PORENABLE)						
V_{IL}	LOW-level input voltage	notes 6 and 7	0	–	$0.2V_{DD}$	V
V_{IH}	HIGH-level input voltage	note 6	$0.8V_{DD}$	–	V_{DD}	V
$\lvert I_{IL} \rvert$	LOW-level input current (ports in Mode 1)	V_{IN} = 0.4 V; note 8; see Fig.13	–	10	50	µA
$\lvert I_{IL(T)} \rvert$	LOW-level input current; HIGH-to-LOW transition (ports in Mode 1)	$V_{IN} = 0.5V_{DD}$; note 8; see Fig.13	–	200	1000	µA
$\lvert I_{LI} \rvert$	input leakage current (ports in Mode 0 or 2)	$V_{SS} \leq V_I \leq V_{DD}$	–	–	1	µA
Port outputs (Ports, RST and MOUT0 and MOUT2)						
I_{OL}	LOW-level output current; except P1.3, SDA, SCL and MOUT2	V_{OL} = 0.4 V	2	–	–	mA
I_{OL1}	LOW-level output current P1.3 (for LED)	V_{OL} = 0.4 V	6	–	–	mA
I_{OL2}	LOW-level output current; SDA, SCL and MOUT2	V_{OL} = 0.4 V; note 9	3	–	–	mA
I_{OH}	HIGH-level output current except P1.3; push-pull options only	$V_{OH} = V_{DD} - 0.4$ V	2	–	–	mA
I_{OH1}	HIGH-level output current P1.3 (for LED); push-pull options only	$V_{OH} = V_{DD} - 0.4$ V	6	–	–	mA
I_{OH2}	HIGH-level output current MOUT2	$V_{OH} = V_{DD} - 0.4$ V	3	–	–	mA
$I_{\overline{RST}}$	$\overline{RST}$ pull-up transistor current	V_{DD} = 3 V; $V_{OH} = V_{DD} - 0.4$ V	5	20	–	µA
		V_{DD} = 3 V; $V_{OH} = V_{SS}$	–	50	200	µA
Power-on-reset (POR); for the LVD (Low Voltage Detection) see note 10						
V_{PORH}	Power-on-reset trip level HIGH	option 5 in *"TELX family"* specification	2.13	2.37	2.61	V
V_{PORL}	Power-on-reset trip level LOW	option A in *"TELX family"* specification	1.98	2.27	2.56	V
TONE output (note 11 and Fig.12)						
$V_{HGF(rms)}$	HGF voltage (RMS)	V_{DD} = 3 V	158	181	205	mV
$V_{LGF(rms)}$	LGF voltage (RMS)		125	142	160	mV
$\Delta f/f$	frequency deviation		–0.6	–	+0.6	%
V_{DC}	DC voltage level		–	$0.5V_{DD}$	–	V
V_G	pre-emphasis of group		1.5	2.0	2.5	dB
THD	total harmonic distortion	V_{DD} = 3 V; T_{amb} = 25 °C; notes 5 and 12	–	25	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
In System Programming for the OTP						
t_{prog}	program cycle time		90	100	110	µs
t_{prog} (security)	program cycle time security	note 13	180	200	220	µs
t_{ver}	verify cycle time		1	–	–	µs
$t_{Vpp(setup)}$	program voltage setup time		10	–	–	µs
$t_{Vpp(max)}$	maximum program voltage time	cumulative for the product lifetime	–	–	60	s
I_{Vpp}	program voltage current	In system programming	–	–	40	mA
ACO (Amplitude Controlled Oscillator)						
V_{XTAL1}	external clock signal amplitude peak-to-peak		500	–	V_{DD}	mV
$Z_{i(XTAL1)}$	input impedance on XTAL1		300	1000	–	kΩ
C_{1i}; C_{2i}	input capacitance on XTAL1 and XTAL2	notes 5 and 14	–	10	–	pF

Notes

1. The operating supply current is measured with all output pins disconnected; $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; $\overline{RST} = V_{DD}$; XTAL1 driven with square wave; XTAL2 not connected; fetch of NOP instructions; all derivative blocks disabled.
2. The Idle mode supply current is measured with all output pins and $\overline{RST}$ disconnected; $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; XTAL1 driven with square wave; XTAL2 not connected; all derivative blocks disabled.
3. The Power-down current is measured with all output pins and $\overline{RST}$ disconnected; $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; XTAL1 and XTAL2 not connected.
4. The typical currents are only for the specific block. To calculate the typical power consumption of the microcontroller, the current consumption of the CPU must be added. Example: the typical current consumption of the microcontroller in operating mode with CPU, Watchdog Timer and UART active can be calculated as (1 + 0.11 + 0.09) mA = 1.2 mA.
5. Verified on sampling basis.
6. The input threshold voltage of P1.6/SCL and P1.7/SDA meet the I^2C-bus specification. Therefore, an input voltage below $0.3V_{DD}$ will be recognized as a logic 0 and an input voltage above $0.7V_{DD}$ will be recognized as a logic 1.
7. For the PORENABLE pin, $V_{IL(max)}$ is $0.1V_{DD}$.
8. Not valid for pins SDA, SCL, $\overline{RST}$, MIN and PORENABLE.
9. The maximum allowed load capacitance C_L is in this case limited to approximately 200 pF.
10. The LVD is tested according to the specification in the data sheet *"TELX family; Chapter: Low Voltage Detection"*.
11. Values are specified for DTMF frequencies only (CEPT CS203).
12. Related to the Low Group Frequency (LGF) component (CEPT CS203).
13. Can also be done by two 100 µs pulses.
14. C_{1i} and C_{2i} are the total internal capacitances (including gate capacitance and leadframe capacitance).

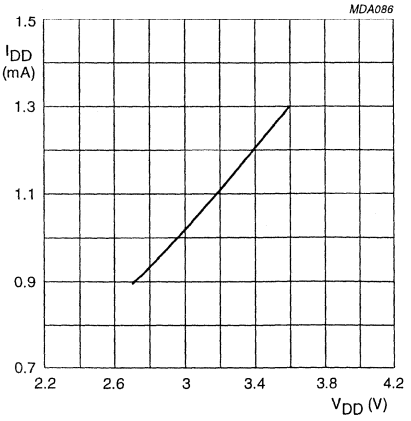


Fig.9 Typical operating current as a function of V_{DD}; T_{amb} = 25 °C.

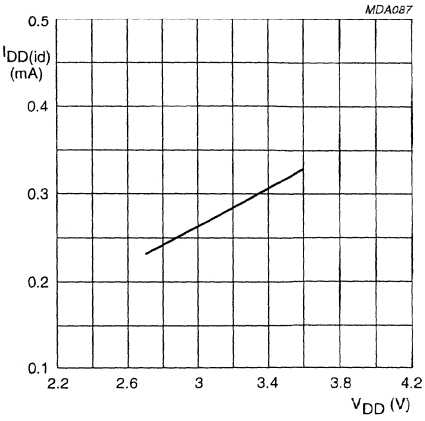
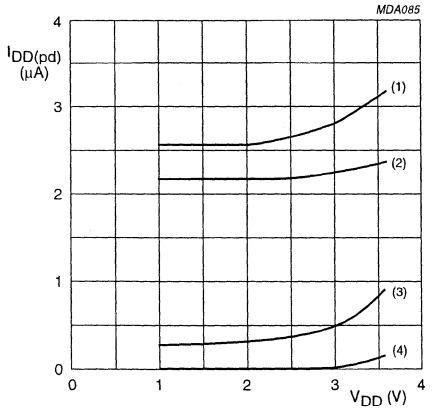
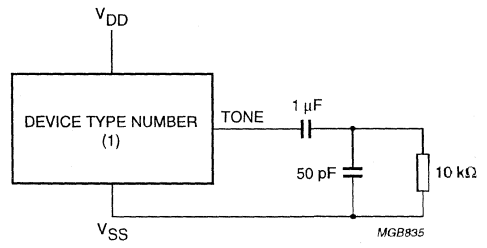


Fig.10 Typical Idle current as a function of V_{DD}; T_{amb} = 25 °C.



(1) POR and LVD enabled (T_{amb} = 70 °C).
(2) POR and LVD enabled (T_{amb} = 25 °C).
(3) POR and LVD disabled (T_{amb} = 70 °C).
(4) POR and LVD disabled (T_{amb} = 25 °C).

Fig.11 Typical Power-down current as a function of V_{DD}.



(1) P83CL887/P87CL887

Fig.12 TONE output test circuit.

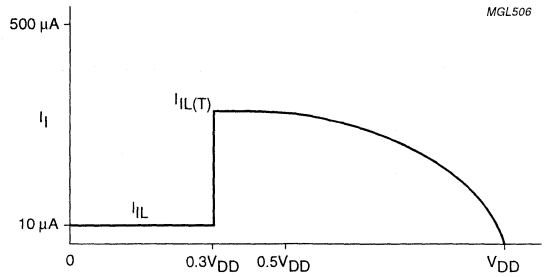


Fig.13 Input current.

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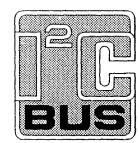


1 FEATURES

- Full static 80C51 CPU; enhanced 8-bit architecture with:
  - Minimum 6 cycles per instruction (twice as fast as a standard 80C51 core)
  - Non-page oriented instructions
  - Direct addressing
  - Four 8-byte RAM register banks
  - Stack depth limited only by available internal RAM (maximum 256 bytes)
  - Multiply, divide, subtract and compare instructions
- Three 8-bit ports (18 I/O lines)
- Program Memory:
  - P87CL887: 12 kbytes One Time Programmable
  - P83CL887: 12 kbytes ROM
- 512 bytes RAM
- Amplitude Controlled Oscillator (ACO) suitable for quartz crystal or ceramic resonator
- Improved Power-on/Power-off reset (POR) circuitry
- Low Voltage Detection (LVD) with 11 software programmable levels
- Eight interrupts on Port 1:
  - Edge or level sensitive triggering selectable via software
  - Power-saving use for keyboard control
- Twenty source, twenty vector interrupt structure with two priority levels
- Wake-up from Power-down mode via LVD or external interrupts at Port 1
- DTMF generator
- MSK modem including Manchester encoder/decoder with 2 digital outputs for analog cordless telephones (standards CT0/CT1/CT1+)
- Watchdog Timer
- Two standard 16-bit timer/event counters
- Additional 16-bit timer/event counter with Capture, Compare and Auto-reload function
- Full duplex enhanced UART with double buffering
- I^2C-bus interface for serial transfer on two lines, maximum 400 kHz
- Very low current consumption
- Single supply voltage: 2.7 to 3.6 V
- Frequency: 3.58 MHz
- Operating temperature: –25 to +70 °C
- 28 pin SO package.

2 GENERAL DESCRIPTION

The P8xCL887 (denoting the P83CL887 and P87CL887) are manufactured in an advanced CMOS technology and are 8-bit microcontrollers especially suited for low cost analog cordless telephone applications (CT0, CT1 and CT1+ standards). Consequently, features like DTMF, MSK modem and POR/LVD are integrated on-chip.

Both devices are optimized for low power consumption and in addition have two software selectable modes for further power reduction: Idle and Power-down modes. All derivative blocks can switch off their clock if they are inactive.

The instruction set of the P8xCL887 is based on that of the 80C51. The P8xCL887 also function as arithmetic processors having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 46 two-byte, and 16 three-byte. As port P2 is not implemented there is no external data or memory access and MOVX operations cannot be used.

This data sheet details the specific properties of the P8xCL887; for details of the P8xCL887 core and the derivative functions see the *"TELX family"* data sheet and *"Data Handbook IC20"*.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
P83CL887DFT	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
P87CL887DFT			

4 BLOCK DIAGRAM

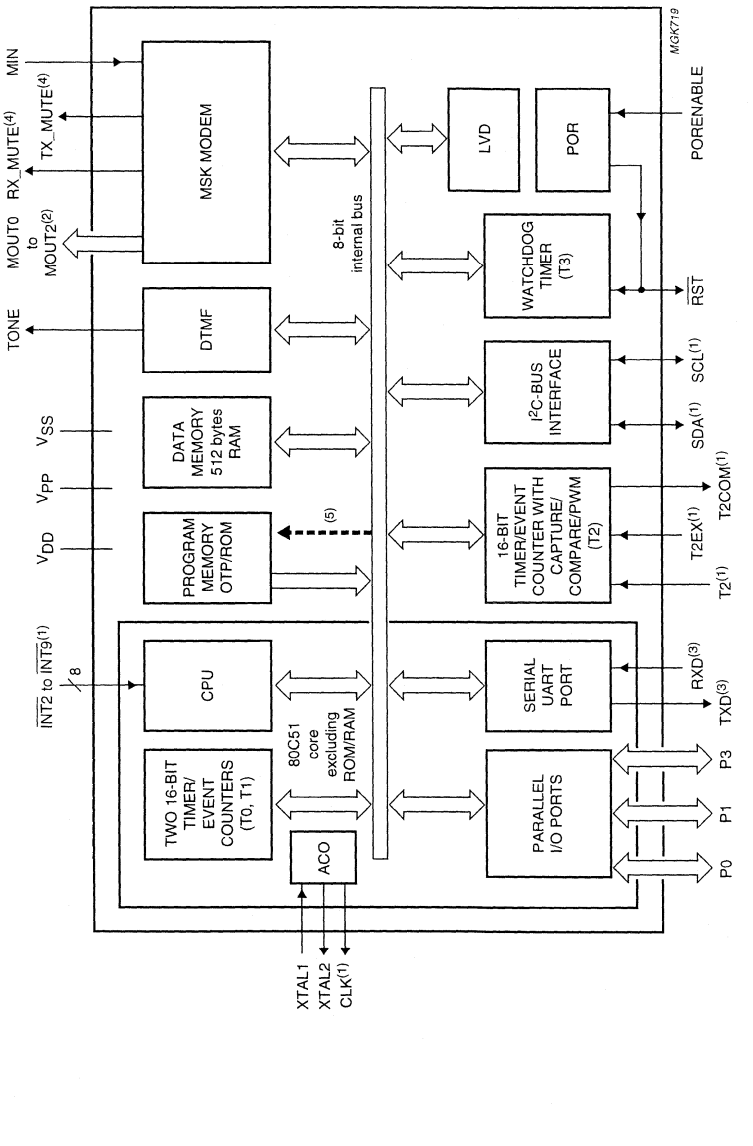


Fig.1 Block diagram.

(1) Alternative functions of Port 1.
(2) MOUT0 is the alternative function to P3.1.
(3) Alternative function of Port 3.
(4) By software any I/O port pin can be used.
(5) In-circuit OTP programming.

5 PINNING INFORMATION

5.1 Pinning

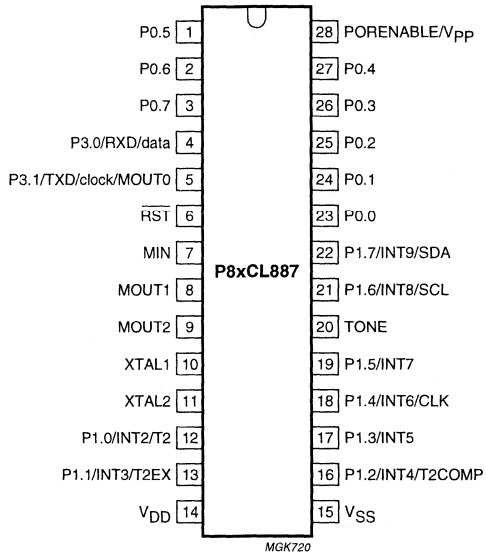


Fig.2 Pin configuration.

5.2 Pin description

Table 1 SO28 package

SYMBOL	PIN	DESCRIPTION
$\overline{RST}$	6	**Active low reset:** a LOW level on this pin for two machine cycles while the oscillator is running, resets the device. The $\overline{RST}$ pin is also an output which can be used to reset other ICs.
MIN	7	Digital **MSK** modem input.
MOUT1	8	Digital **MSK** modem outputs.
MOUT2	9	
XTAL1	10	**Crystal input:** Input to the Amplitude Controlled Oscillator. Also the input for an externally generated clock source.
XTAL2	11	**Crystal output:** Output of the Amplitude Controlled Oscillator; to be left non-connected when an external oscillator clock is used.
V_{DD}	14	Power supply.
V_{SS}	15	Ground.
P0.0 to P0.7	23 to 27, 1 to 3	**Port 0:** 8-bit bidirectional I/O port; every port pin can be used as open-drain, standard port, high-impedance input or push-pull output, according to Section 6.2.
P1.0/INT2/T2	12	**Port 1:** 8-bit bidirectional I/O port with alternative functions. Every port pin except P1.6 and P1.7 (I^2C-bus pins) can be used as open-drain, standard port, high-impedance input or push-pull output, according to Section 6.2. Port P1.3 has LED drive capability. Port 1 also serves the alternative functions: **INT2 to INT9** interrupts; Timer T2 external inputs **T2** and **T2EX**; Timer T2 compare output **T2COMP**; external clock output **CLK**; I^2C-bus clock **SCL** and data in/outputs **SDA**.
P1.1/INT3/T2EX	13	
P1.2/INT4/T2COMP	16	
P1.3/INT5	17	
P1.4/INT6/CLK	18	
P1.5/INT7	19	
P1.6/INT8/SCL	21	
P1.7/INT9/SDA	22	
P3.0/RXD/data	4	**Port 3:** 3 or 2-bit bidirectional I/O port with alternative functions. Every port pin can be used as open-drain, standard port, high-impedance input or push-pull output, according to Chapter 6.2. Port 3 also serves the alternative functions: **RXD/data** is the serial port receiver data input (asynchronous) or data I/O (synchronous); **TXD/clock** is the serial port transmitter data output (asynchronous) or clock output (synchronous) or digital MSK modem output **MOUT0**.
P3.1/TXD/clock/ MOUT0	5	
TONE	20	**DTMF** output.
PORENABLE/V_{PP}	28	**PORENABLE**: Power-on-reset circuit enable. If PORENABLE = 1, the internal Power-on-reset circuit is enabled. If external reset circuitry is used, it is recommended to keep PORENABLE = 0 to reach lowest power consumption. This pin is also used for the OTP programming voltage V_{PP}.

6 FUNCTIONAL DESCRIPTION

6.1 Special Function Registers

Table 2 Special Function Registers memory map and reset values

REGISTER NAME	REGISTER MNEMONIC	SFR ADDRESS	RESET VALUE[1]
80C51 core			
Accumulator	ACC	E0H	0000 0000
B Register	B	F0H	0000 0000
Data Pointer Low byte	DPL	82H	0000 0000
Data Pointer High byte	DPH	83H	0000 0000
Program Counter High byte	PCH	no SFR	0000 0000
Program Counter Low byte	PCL	no SFR	0000 0000
Power Control Register	PCON	87H	0000 0000
Prescaler Register	PRESC	F3H	0000 0000
Program Status Word	PSW	D0H	0000 0000
Stack Pointer	SP	81H	0000 0111
Timer 0 and Timer 1			
Timer/Counter Control Register	TCON	88H	0000 0000
Timer/Counter 0 High byte	TH0	8CH	0000 0000
Timer/Counter 1 High byte	TH1	8DH	0000 0000
Timer/Counter 0 Low byte	TL0	8AH	0000 0000
Timer/Counter 1 Low byte	TL1	8BH	0000 0000
Timer/Counter Mode Control Register	TMOD	89H	0000 0000
Ports			
Alternative Port Function Control Register	ALTP	A3H	0000 0000
Port P0 Output Data Register	P0	80H	1111 1111
Port P0 Configuration A Register	P0CFGA	8EH	1111 1111
Port P0 Configuration B Register	P0CFGB	8FH	0000 0000
Port P1 Output Data Register	P1	90H	1111 1111
Port P1 Configuration A Register	P1CFGA	9EH	0011 1111
Port P1 Configuration B Register	P1CFGB	9FH	0000 0000
Port P3 Output Data Register	P3	B0H	XXXX XX11
Port P3 Configuration A Register	P3CFGA	BEH	XXXX XX11
Port P3 Configuration B Register	P3CFGB	BFH	XXXX XX00
Port P4 Output Data Register	P4	C1H	XXXX XXX0[2]

REGISTER NAME	REGISTER MNEMONIC	SFR ADDRESS	RESET VALUE[1]
Timer 2			
Timer 2 Compare High byte	COMP2H	ABH	0000 0000
Timer 2 Compare Low byte	COMP2L	AAH	0000 0000
Timer 2 Reload/Capture High byte	RCAP2H	CBH	0000 0000
Timer 2 Reload/Capture Low byte	RCAP2L	CAH	0000 0000
Timer/Counter 2 Control Register	T2CON	C8H	0000 0000
Timer/Counter 2 High byte	TH2	CDH	0000 0000
Timer/Counter 2 Low byte	TL2	CCH	0000 0000
DTMF			
High Group Frequency Register	HGF	A2H	0000 0000
Low Group Frequency Register	LGF	A1H	0000 0000
Interrupt logic			
Interrupt Enable Register 0	IEN0	A8H	0000 0000
Interrupt Enable Register 1	IEN1	E8H	0000 0000
Interrupt Enable Register 2	IEN2	F1H	0000 0000
Interrupt Priority Register 0	IP0	B8H	0000 0000
Interrupt Priority Register 1	IP1	F8H	0000 0000
Interrupt Priority Register 2	IP2	F9H	0000 0000
Interrupt Sensitivity Register 1	ISE1	E1H	0000 0000
Interrupt Polarity Register	IX1	E9H	0000 0000
Interrupt Request Flag Register 1	IRQ1	C0H	0000 0000
Low Voltage Detection			
LVD Control Register	LVDCON	F2H	0000 0000
POR/ACO			
Reset Status Register	RSTAT	E6H	XXX0 1001[3]
MSK modem			
MSK Modem Control Register	MCON	D3H	0000 0000
MSK Modem Data Buffer	MBUF	D1H	XXXX XXXX
MSK Modem Status Register	MSTAT	D2H	XX00 0000

REGISTER NAME	REGISTER MNEMONIC	SFR ADDRESS	RESET VALUE[1]
UART			
Serial Port Buffer	S0BUF	99H	0000 0000
Serial Port Control Register	S0CON	98H	0000 0000
I^2C-bus interface			
Address Register	S1ADR	DBH	0000 0000
Serial Control Register	S1CON	D8H	0000 0000
Data Shift Register	S1DAT	DAH	0000 0000
Serial Status Register	S1STA	D9H	1111 1000
Watchdog Timer			
Watchdog Timer Control Register	WDCON	A5H	1010 0101
Watchdog Timer Interval Register	WDTIM	FFH	0000 0000
OTP interface			
OTP Address High Register	OAH	D5H	X00X XXXX
OTP Address Low Register	OAL	D4H	XXXX XXXX
OTP Data Register	ODATA	D6H	XXXX XXXX
OTP In System Programming Register	OISYS	DCH	000X 0000
OTP Test Register	OTEST	C7H	0000 0000
Reserved locations, see note 4			
–	–	E7H, FDH	–

Notes

1. Where: X = undefined state or not implemented bit.
2. Only used to define MSK input polarity. Write only.
3. Defined by mask.
4. E7H and FDH are reserved locations and must not be written to.

6.2 I/O facilities

6.2.1 PORTS

The P8xCL887 have 18 I/O lines, treated as 18 individually addressable bits or as three parallel 8-bit addressable ports. The alternative functions are detailed below:

Port 0 Offers no alternative functions.

Port 1 Used for a number of special functions:

- P1.0 to P1.7 provides the inputs for the external interrupts INT2 to INT9
- P1.2/T2COMP for external activation and Compare/Auto-reload output function of Timer 2
- P1.4/CLK for the clock output
- P1.6/SCL and P1.7/SDA for the I^2C-bus interface are real open-drain outputs or high-impedance; no other port configurations are available.

Port 2 Not available.

Port 3 Pins can be configured individually to provide:

- P3.0/RXD/data and P3.1/TXD/clock/MOUT0 are serial port receiver input and transmitter output (UART).

To enable a Port pin alternative function, the Port bit latch in its SFR must contain a logic 1.

Each port consists of a latch (Special Function Registers P0 to P3), an output driver and input buffer. All ports have internal pull-ups. Figure 3b shows that the strong transistor 'p1' is turned on for only one oscillator period after a LOW-to-HIGH transition in the port latch. When on, it turns on 'p3' (a weak pull-up) through the inverter IN1. This inverter and transistor 'p3' form a latch which holds the logic 1.

Port P1.3 has LED drive capability.

6.2.2 PORT I/O CONFIGURATION

I/O port output configurations are determined by the settings in the port configuration SFRs. There are 2 SFRs for each port: PnCFGA and PnCFGB, where 'n' indicates the specific port number (0 to 3).

One bit in each of the 2 SFRs relates to the output setting for the corresponding port pin, allowing any combination of the 2 output types to be mixed on those port pins. For instance, the output type of Port 1 pin 3 is controlled by the setting of bit 3 in the SFRs P1CFGA and P1CFGB.

The port pins may be individually configured via SFRs with one of the following modes (P1.6 and P1.7 can be open-drain or high-impedance but never have any diodes against V_{DD}). These modes are also shown in Fig.3.

Mode 0 Open-drain; quasi-bidirectional I/O with n-channel open-drain output. Use as an output requires the connection of an external pull-up resistor; e.g. Port 0 for external memory accesses (EA = 0) or access above the built-in memory boundary. The ESD protection diodes against V_{DD} and V_{SS} are still present; see Fig.3b Except for the I^2C pins P1.6 and P1.7, ports which are configured as open-drain still have a protection diode to V_{DD}.

Mode 1 Standard port; quasi-bidirectional I/O with pull-up. The strong pull-up 'p1' is turned on for only two oscillator periods after a LOW-to-HIGH transition in the port latch. After these two oscillator periods the port is only weakly driven through 'p2' and 'very weakly' driven through 'p3' see Fig.3b.

Mode 2 High-impedance; this mode turns off all output drivers on a port. Thus, the pin will not source or sink current and may be used as an input-only pin with no internal drivers for an external device to overcome see Fig.3c.

Mode 3 Push-pull; output with drive capability in both polarities. Under this mode, pins can only be used as outputs see Fig.3d.

Tables 3 and 4 show the configuration register settings for the 4 port output types.

The electrical characteristics of each output type can be found in Chapter 8. The default port configuration after reset is given in Table 4.

Table 3 Port Configuration Registers PnCFGA and PnCFGB (n = 0, 1 and 3) settings

MODE[1]	PnCFGA	PnCFGB	PORT OUTPUT CONFIGURATION	
			NORMAL PORTS	I²C-BUS PORTS (P1.6 AND P1.7)
Mode 0	0	0	open-drain	open-drain
Mode 1	1	0	quasi-bidirectional	open-drain
Mode 2	0	1	high-impedance	high-impedance
Mode 3	1	1	push-pull	open-drain

Note

1. Mode changes may cause glitches to occur during transitions. When modifying both registers, WRITE instructions should be carried out consecutively.

Table 4 Special Function Registers for port configurations/data

REGISTER NAME	REGISTER MNEMONIC	SFR ADDRESS (HEX)	STATE AFTER RESET
Port P0 Output Data[1]	P0	80	11111111
Port P0 Configuration A	P0CFGA	8E	11111111
Port P0 Configuration B	P0CFGB	8F	00000000
Port P1 Output Data[1]	P1	90	11111111
Port P1 Configuration A	P1CFGA	9E	00111111
Port P1 Configuration B	P1CFGB	9F	00000000
Port P3 Output Data[1]	P3	B0	XXXXXX11
Port P3 Configuration A	P3CFGA	BE	XXXXXX11
Port P3 Configuration B	P3CFGB	BF	XXXXXX00

Note

1. This means that P0, P1.0 to P1.5 and P3 are initialized in Mode 1 (quasi-bidirectional, driving a weak HIGH) and the I²C-bus ports P1.6 and P1.7 are initialized in Mode 0 (open-drain, not driven).

6.2.3 Alternative Port Function Control Register (ALTP)

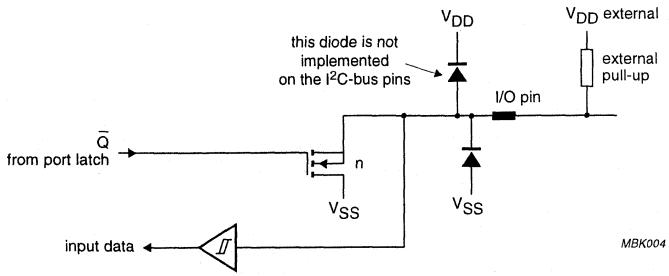
This 4-bit register controls the alternative functions of certain port pins.

Table 5 Alternative Port Function Register (SFR address A3H)

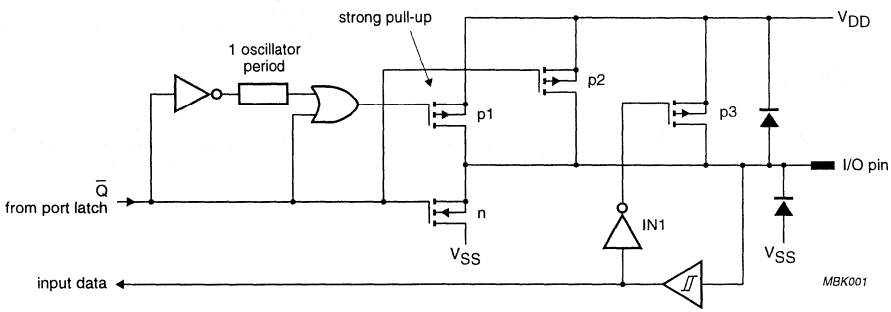
7	6	5	4	3	2	1	0
–	–	–	–	EMOUT0	ECLK	EMLDY	ETONE

Table 6 Description of ALTP bits

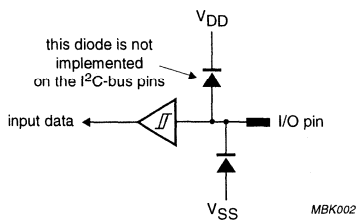
BIT	SYMBOL	DESCRIPTION
7 to 4	–	Reserved.
3	EMOUT0	**Enable MOUT0.** If this bit is set, P3.1 will output the MOUT0 signal.
2	ECLK	**Enable Clock.** If this bit is set, P1.4 is configured to be push-pull, and P1.4 will output the system clock.
1	EMLDY	**Enable MLDY.** If this bit is set, P1.5 is configured to be push-pull, and P1.5 will output the digital MLDY signal of the DTMF generator.
0	ETONE	**Enable TONE.** If this bit is set, the TONE output of the DTMF generator is enabled.



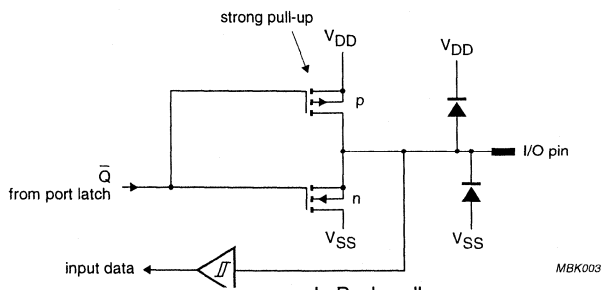
a. Open-drain.



b. Standard/quasi-bidirectional.



c. High-impedance.



d. Push-pull.

Fig.3 Port configuration options.

6.3 Timer/event counters

The P8xCL887 contain three 16-bit timer/event counters: Timer 0, Timer 1 and Timer 2 which can perform the following functions:

- Measure time intervals and pulse durations
- Count events (T2 only, no external input for T0/T1)
- Generate interrupt requests
- Generate output on comparator match.

In the 'timer' mode the register is incremented every machine cycle.

Since a machine cycle consists of minimum 6 oscillator periods, the maximum count rate is $1/6 \times f_{osc}$.

In the 'counter' mode, the register is incremented in response to a HIGH-to-LOW transition. Since it takes one machine cycle (minimum 6 oscillator periods) to recognize a HIGH-to-LOW transition, the maximum count rate is $1/6 \times f_{osc}$. To ensure a given level is sampled, it should be held for at least one complete machine cycle.

Timer 0 and Timer 1 can be programmed independently to operate in four modes:

Mode 0 8-bit timer or 8-bit counter each with divide-by-32 prescaler.

Mode 1 16-bit time-interval or event counter.

Mode 2 8-bit time-interval or event counter with automatic reload upon overflow.

Mode 3 Timer 0 establishes TL0 and TH0 as two separate counters.

6.3.1 TIMER T2

Note that the timer T2 of the P8xCL887 deviates from the timer T2 described in the *"TELX family"* data sheet.

Timer T2 is a 16-bit timer/counter that can operate either as a timer or as an event counter. These functions are selected by the state of the C/$\overline{T2}$ bit in the T2CON register. Five operating modes are available:

- Capture
- Compare
- Auto-reload
- Compare with Auto-reload
- Capture and Compare.

These modes are selected via the T2CON register.

6.3.1.1 Capture mode

In the Capture mode, two options may be selected by the EXEN2 bit in T2CON:

- If EXEN2 = 0, then Timer 2 is a 16-bit timer or counter which upon overflowing sets the Timer 2 overflow bit TF2, this may then be used to generate an interrupt.
- If EXEN2 = 1, Timer 2 operates as described above but with the additional feature that a HIGH-to-LOW transition at external input T2EX causes the current value in TL2 and TH2 to be captured into registers RCAP2L and RCAP2H respectively. In addition, the transition at T2EX causes the EXF2 bit in T2CON to be set; this may also be used to generate an interrupt.

The Capture mode is shown in Fig.4.

6.3.1.2 Compare mode

In the Compare mode, each time timer T2 is incremented, the contents of the compare registers COMP2H and COMP2L are compared with the new counter value of timer T2. When a match occurs, the interrupt flag COMP in register T2CON and port bit P1.2 are toggled. The 16-bit value held in these registers is preset by software. The first toggle after a reset will set the flag COMP. The Compare mode is shown in Fig.4.

6.3.1.3 Auto-reload mode

In the Auto-reload mode there are also two options selected by the EXEN2 bit in T2CON:

- If EXEN2 = 0, then when Timer 2 rolls over, it sets the TF2 bit but also causes the Timer 2 registers to be reloaded with the 16-bit value held in registers RCAP2L and RCAP2H. The 16-bit value held in these registers is preset by software.
- If EXEN2 = 1, Timer 2 operates as described above but with the additional feature that a HIGH-to-LOW transition at external input T2EX will also trigger the 16-bit reload and set the EXF2 bit.

6.3.1.4 Compare with Auto-reload mode

The Auto-reload mode can be used together with the Compare mode. The Auto-reload modes are shown in Fig.5.

6.3.1.5 Capture and Compare modes

The Capture and the Compare mode of timer T2 can be used separately or simultaneously. The function is chosen via the bits ECOMP, CP/$\overline{RL2}$ and TR2 in register T2CON.

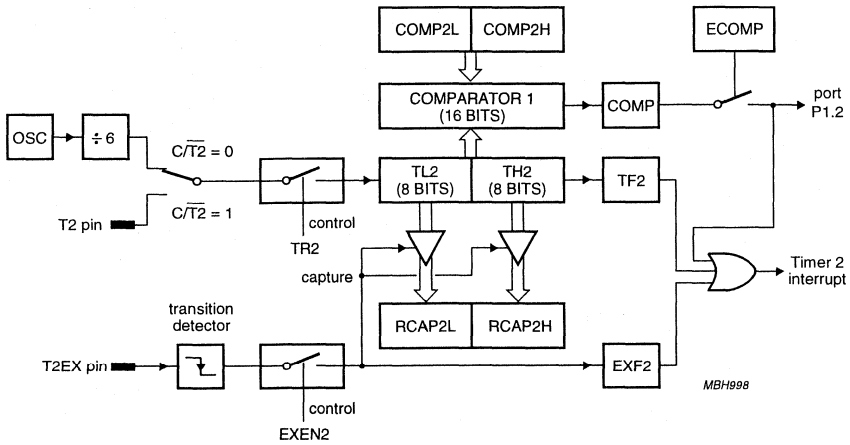


Fig.4 Timer 2 in Capture and/or Compare mode.

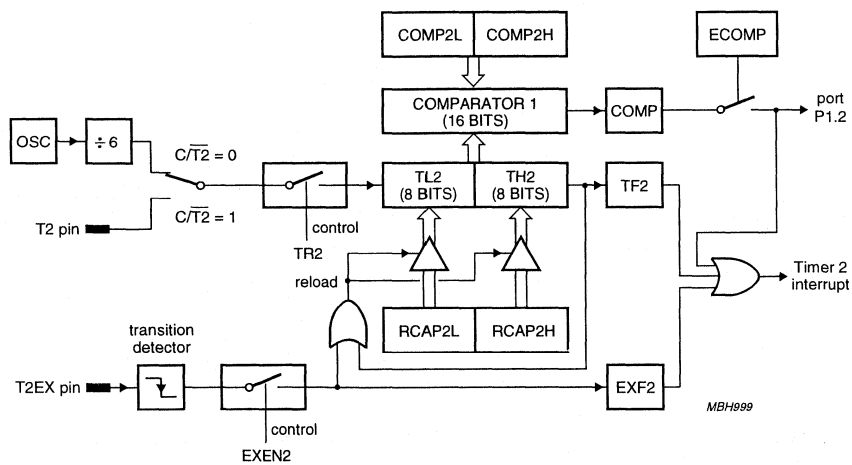


Fig.5 Timer 2 in Auto-Reload with/without Compare mode.

6.3.2 Timer/Counter 2 Control Register (T2CON)

Table 7 Timer/Counter 2 Control Register (SFR address C8H)

7	6	5	4	3	2	1	0
TF2	EXF2	COMP	ECOMP	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$

Table 8 Description of T2CON bits

BIT	SYMBOL	DESCRIPTION
7	TF2	**Timer 2 overflow flag.** TF2 is set by a Timer 2 overflow and must be cleared by software.
6	EXF2	**Timer 2 external flag.** EXF2 is set when either a capture or reload is caused by a negative transition on T2EX and when EXEN2 = 1. When Timer T2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to Timer 2 interrupt routine. EXF2 must be cleared by software.
5	COMP	**Interrupt flag.** When a match between the 16-bit compare register (COMP2L and COMP2H) and the new counter value of timer T2 occurs, the interrupt flag COMP in register T2CON and port bit P1.2 are toggled.
4	ECOMP	**Enable compare output bit.** When set by software, the controller toggles port bit P1.2 (T2COMP) when a compare match occurs.
3	EXEN2	**Timer 2 external enable flag.** When set, allows a capture or reload to occur as a result of a negative transition on T2EX. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
2	TR2	**Timer 2 start/stop control.** Control bit for Timer 2.
1	C/$\overline{T2}$	**Timer 2 timer or counter select.** C/$\overline{T2}$ = 0 selects the internal timer with a clock frequency of $\frac{1}{6} \times f_{osc}$. C/$\overline{T2}$ = 1 selects the external event counter; negative edge-triggered.
0	CP/$\overline{RL2}$	**Capture/reload flag.** When set captures will occur on negative transitions at T2EX, if EXEN2 = 1. When cleared, auto-reloads will occur either with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1.

Table 9 Timer 2 operating modes

ECOMP	CP/$\overline{RL2}$	TR2	MODE
0	0	1	16-bit Auto-reload
0	1	1	16-bit Capture
1	0	1	16-bit Compare
1	1	1	16-bit Capture and Compare
1	0	0	16-bit Compare with Auto-reload
0	0	0	off

6.4 MSK modem

For the P8xCL887, MIN has its own dedicated pin and is no longer the alternative function of P4.0. The polarity of MIN can however still be programmed with the P4.0 bit. P4.0 is a data SFR but no port logic is connected.

Only the most significant bits of MOUT, i.e. MOUT2 and MOUT1 are directly available as separate pins. In order to be able to further increase the signal quality, the MOUT0 signal is available as alternative port function of P3.1.

For controlling this alternative port function the EMOUT0 bit has been added to the Alternative Port Function Register (ALTP); see Section 6.2.3.

6.5 Watchdog Timer (T3)

The Watchdog Timer differs from the description given in the *"TELX family"* data sheet in that the external $\overline{EW}$ pin does not exist on the P8xCL887.

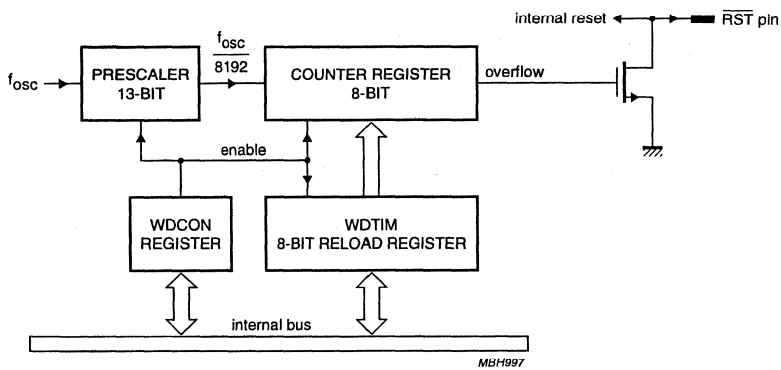


Fig.6 Functional diagram of the Watchdog Timer.

6.6 OTP programming

6.6.1 OTP PROGRAMMING BY A PROGRAMMER

The 12 kbytes One Time Programmable (OTP) memory can be programmed by using a programmer (OM4260) together with a programmer adapter OM5508. Since the memory is programmable only once, programming an already programmed address results in a logical AND of the old and new code. The OTP code can be read out by the programmer for verification.

6.6.1.1 Signature bytes

The OTP memory contains three signature bytes which can be read by the programmer to identify the device. A special address space has been used for these bytes which does not influence the user address space.

The values of the signature bytes are:

(030H) = 15H, indicates manufactured by Philips Semiconductors

(031H) = C8H, indicates P87CL887

(060H) = 00H, currently not used.

6.6.1.2 Security

The following protection levels are available to protect TELX applications against software piracy and unwanted access to data stored in the application.

1. Preventing programming of an already programmed OTP. Note that security Level 1 also disables In System Programming.
2. Preventing the reading of program code in OTP by disabling access of the programmer to the Program Memory. Also verification of code during In System Programming is disabled. In this mode signature and security level verification is still possible.
3. This level has the same functionality as Level 2.

Table 10 describes how these protection levels can be selected by programming the three least significant bits of the security byte.

Table 10 Protection level selection

BITS	LEVEL	DESCRIPTION
UUU	0	no security
UUP	1	Level 1 is activated
UPP	2	Levels 1 and 2 are activated
PPP	3	Levels 1, 2 and 3 are activated

6.6.2 IN SYSTEM PROGRAMMING MODE

In the In System Programming mode the OTP can be programmed under the control of the CPU. A control program must be available in the OTP. This mode can be used to program several bytes in the OTP if the chip is already in a system e.g. to store tuning parameters.

In the In System Programming mode the complete address space OTP can be programmed.

The user should take care not to overwrite the existing code.

For In System Programming four SFRs are used to control the OTP.

Table 11 SFRs for In System Programming

SFR NAME	DESCRIPTION
OAH	OTP Address High Register
OAL	OTP Address Low Register
ODATA	OTP Data Register
OISYS	OTP In System Register; see Section 6.6.2.5

6.6.2.1 Mode entry

The In System Programming mode is entered by setting the InSysMode bit of the OISYS SFR. The I^2C-bus is used for data transfer in this mode. If the I^2C-bus interface is addressed by an external master, the interface generates an interrupt request. The interrupt handler can now read the OISYS SFR and determine the status of the external high voltage (VPon). If high voltage is not present the interrupt is a standard I^2C-bus interrupt.

If high voltage is present the In System Program interrupt routine has to start writing the InSysMode bit (OISYS.0) and controls the address and data transfer.

During In System Programming the OTP memory has to be in DC read mode. This is achieved by writing 08H to the OTEST SFR. If the In System Programming mode is left, 00H must be written into the OTEST SFR.

The program voltage has to be available and stable for at least 10 µs before the mode is entered and must remain stable until the circuit has left the In System Programming mode. The high voltage can be applied for maximum 60 seconds during the complete lifetime of the circuit.

6.6.2.2 *Program cycle*

The data and address have to be supplied to the microcontroller and the control program must write to the SFRs: ODATA, OAH and OAL. A timer has to be initialized for a 100 µs cycle and the WE bit of the OISYS SFR has to be set. Now the core must be set into the Idle mode. As long as the circuit is in Idle mode a programming pulse is applied. After the interrupt request of the timer the OTP is available for normal code fetching.

The address applied to the OAH and OAL SFRs must be in the 12 kbytes address space.

6.6.2.3 *Verify for In System Programming*

Verify is done in a similar way as programming. The circuit is put into the Idle mode and at the start of this mode the sense amplifiers are switched to verify mode and a read cycle is started. The timer has to be initialized for a cycle of at least 1 µs. The address is supplied by the SFRs OAH and OAL. The WE bit of the OISYS SFR has to be reset. The OTP output data is latched in the ODATA SFR. After Idle mode is finished this SFR can be read in the normal way.

To be sure that the verified data is written into the SFR it is advised to write FFH into the ODATA SFR before a verify is started.

6.6.2.4 *Signature bytes and security*

Signature bytes can be read by setting the SIG bit of the OISYS SFR and applying the address of the signature byte. Applying a write pulse while the SIG bit of the OISYS SFR is HIGH is forbidden although the contents of the signature bytes will never be destroyed. The signature bytes (and other test addresses) are always readable independent of the security.

Security has the same meaning as in Parallel Program mode. Security can be programmed and verified by setting the SEC bit of the OISYS SFR. The security bits can be programmed like normal bits. To program Level 1, 01H must be loaded in the ODATA SFR. These values are 03H and 07H for Level 2 and Level 3 respectively. The SEC bit of the OISYS SFR must be HIGH during the program cycle. Loading an address is not necessary. The timer must be initialized for 200 µs instead of 100 µs for security or two standard pulses must be applied. If the SEC bit is HIGH during verify, the security bits can be read from the ODATA SFR. Verifying a normal address while security level (Level 2 or Level 3) has been programmed will result in reading 00H.

Verifying is disabled immediately after programming Level 2 or Level 3. Programming is disabled if a verify or a reset is applied after programming security level: Level 1 or higher.

6.6.2.5 *OTP In System Programming Register (OISYS)*

The OISYS SFR controls the In System Programming mode. The data to be programmed is stored in the SFR ODATA and the address for this data in the SFRs OAH and OAL.

Table 12 OTP In System Programming Register (SFR address DCH)

7	6	5	4	3	2	1	0
–	–	–	VPon	SEC	SIG	WE	InSysMode

Table 13 Description of OISYS bits

BIT	SYMBOL	DESCRIPTION
7 to 5	–	reserved
4	VPon	V_{PP} status (read only)
3	SEC	security bits enable
2	SIG	signature bytes enable
1	WE	Write Enable, enables programming
0	InSysMode	In System Programming status bit

6.6.2.6 How to connect the PORENABLE/V_{PP} pin in the In System Programming mode

If the V_{PP} pin is dual-mode (e.g. PORENABLE/V_{PP}), ICs connected to the signal PORENABLE **must be able to withstand up to 13 V**, i.e. cannot have clamping diodes or low break-down voltages. If the pin is connected to a fixed voltage (V_{DD} or V_{SS}) there must be a way of switching-off this connection on the PCB. A possible implementation is presented in Fig.7.

In the example (see Fig.7) the POR is enabled in normal mode of operation (pin PORENABLE/V_{PP} = 1 by the pull-up), but the V_{PP} source must supply enough current in R_p in order to guarantee a minimum of 12.5 V on the PORENABLE/V_{PP} pin.

Note that if in the application the Power-on-reset is disabled (pin PORENABLE/V_{PP} = 0), applying a high voltage to the PORENABLE/V_{PP} pin will also enable the POR circuit. This will cause a reset independent of the actual V_{DD} value.

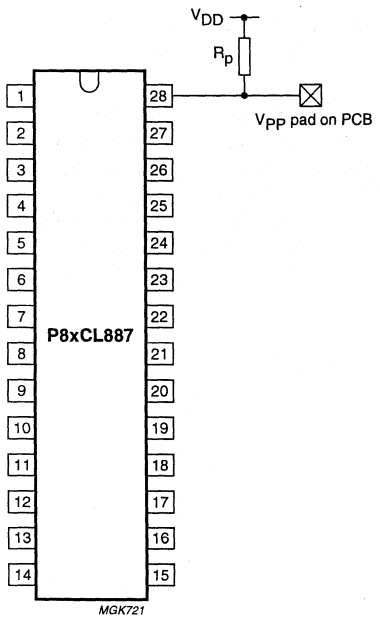


Fig.7 Example of PORENABLE/V_{PP} connection on a PCB.

6.7 Oscillator circuitry

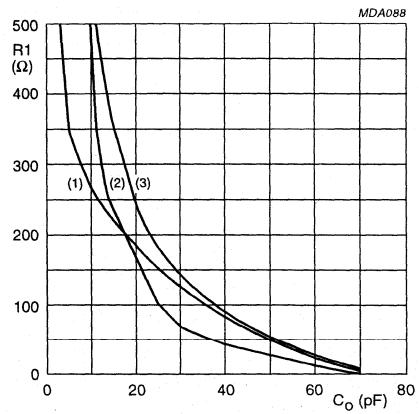
General information on the oscillator circuitry can be found in the *"TELX family"* data sheet.

6.7.1 Resonator requirements

For correct function of the oscillator, the values of R_1 and C_0 of the chosen resonator (quartz or PXE) must be below the line shown in Fig.8a. The value of the parallel resistor R_0 must be less than 47 kΩ. The wiring between chip and resonator should be kept as short as possible.

6.7.2 Recommended resonator types

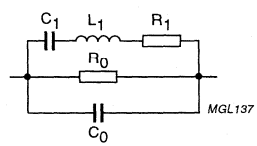
- CSA 3.58MG (supplier Murata)
- FCR3.58M5 (supplier TDK).



C_{1e} and C_{2e} are the external load capacitances; normally not needed due to integrated load capacitances of typically 10 pF.

(1) $C_{1e} = C_{2e}$ = 22 pF.
(2) $C_{1e} = C_{2e}$ = 0 pF.
(3) $C_{1e} = C_{2e}$ = 12 pF.

a. Resonator curves.



b. Resonator equivalent circuit.

Fig.8 Resonator requirements for the ACO.

6.8 Emulation

The emulator for the P8xCL887 uses the P87CL880 microcontroller in emulation mode. The P87CL880 is a super-set of the P8xCL887, i.e. it contains all the functions of the P8xCL887 plus a number of other additional functions. It should be noted that some functional differences between the P87CL880 and the P8xCL887 exist; see Table 14.

Table 14 Differences between functions existing in P87CL880 and P8xCL887

FUNCTION	P87CL880	P8XCL887
Timer 2	see P87CL880 specification	see P8xCL887 specification
OTP Program Memory	32 kbytes AFPROM	12 kbytes EPROM or pre-programmed ROM
$\overline{EW}$ pin (Watchdog enable)	yes	no
Security concept	see P87CL880 specification	see P8xCL887 specification
In System Programming	no	yes
Reset value of SFRs	see P87CL880 specification	see P8xCL887 specification
POR	hardware programmable	fixed
Frequency	DC to 12.5 MHz	3.58 MHz
Read-Modify-Write bug	Yes	No

6.9 Read-Modify-Write bug

The first version of P87CL880 which is used in the emulator for the P8xCL887 contains a bug which affects all instructions of type Read-Modify-Write (RMW) to an I/O port. The instructions affected are: ANL, ORL, XRL, JBC, CPL, INC, DEC, DJNZ, MOV Px.y, C, CLR Px.y and SET Px.y. Detailed explanations of the normal function of these instructions are explained in *"Data Handbook IC20"*.

The ports affected are port P0 and P3 on P87CL880.

Normally, a RMW instruction first reads the value which is present on the port latch (not the state of the port pins), modifies this value, and writes it back to the port latch.

Due to a critical timing between two internal signals in the present design, the RMW instructions do not work correctly.

Due to the bug, the RMW instructions on the port pins should be avoided. However, a software work around exist.

Instead of using the normal RMW instruction, each manipulation should be done on a copy-byte of the port latch (e.g. a bit addressable RAM byte for each port), and thereafter the new value of the copy-byte should be written to the port latch. It is important that any value to be written to a port must be copied in the copy-byte, see Example 1.

6.9.1 Example 1: Writing 'directly' to a port

Normally:

```
MOV P1,#53h          ;write value directly to port
```

Work-around:

```
MOV P1copy,#53h      ;write value to copy-byte
MOV P1,P1copy        ;write value of copy-byte to port
```

6.9.2 Example 2: Setting one bit of the port

Normally:

```
SET P1.0             ;set bit 0 of port P1
```

Work-around:

```
SET P1copy.0         ;set bit 0 of port P1copy, assuming register P1copy is chosen to
                     be in the bit addressable RAM area
MOV P1, P1copy       ;write value of copy-byte to port
```

7 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	+4.0	V
V_I	input voltage on any pin with respect to ground (V_{SS})	−0.5	V_{DD} + 0.5	V
P_{tot}	total power dissipation	–	800	mW
T_{stg}	storage temperature	−65	+150	°C

8 CHARACTERISTICS

V_{DD} = 2.7 to 3.6 V; V_{SS} = 0 V; f_{xtal} = 3.58 MHz; T_{amb} = −25 to +70 °C; (during In System Programming T_{amb} = 20 to 40 °C). All voltages with respect to V_{SS} unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage					
	operating		2.7	–	3.6	V
	RAM data retention in Power-down mode		1.0	–	3.6	V
	In System Programming		3.0	–	3.6	V
V_{PP}	OTP programming voltage		12.5	–	13.0	V
I_{DD}	operating supply current	V_{DD} = 3 V; note 1	–	–	2.0	mA
		V_{DD} = 3 V; T_{amb} = 25 °C; note 1; see Fig.9	–	1	–	mA
$I_{DD(id)}$	supply current Idle mode	V_{DD} = 3 V; note 2	–	–	0.55	mA
		V_{DD} = 3 V; T_{amb} = 25 °C; note 2; see Fig.10	–	0.26	–	mA
$I_{DD(pd)}$	supply current Power-down mode	V_{DD} = 3 V; T_{amb} = 25 °C; note 3; see Fig.11				
		POR and LVD enabled	–	2	5.0	µA
		POR and LVD disabled	–	100	–	nA
$I_{DD(block)}$	supply current per block:	V_{DD} = 3 V; T_{amb} = 25 °C; notes 4 and 5				
	DTMF	no load on TONE output	–	240	–	µA
	MSK modem		–	140	–	µA
	Watchdog		–	110	–	µA
	I^2C-bus		–	90	–	µA
	UART		–	90	–	µA
	Timer T2		–	90	–	µA
	Timer T0 or T1		–	5	–	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs (Ports, MIN, RST, MOUT0 to MOUT2 and PORENABLE)						
V_{IL}	LOW-level input voltage	notes 6 and 7	0	–	$0.2V_{DD}$	V
V_{IH}	HIGH-level input voltage	note 6	$0.8V_{DD}$	–	V_{DD}	V
$\lvert I_{IL} \rvert$	LOW-level input current (ports in Mode 1)	V_{IN} = 0.4 V; note 8; see Fig.13	–	10	50	µA
$\lvert I_{IL(T)} \rvert$	LOW-level input current; HIGH-to-LOW transition (ports in Mode 1)	$V_{IN} = 0.5V_{DD}$; note 8; see Fig.13	–	200	1000	µA
$\lvert I_{LI} \rvert$	input leakage current (ports in Mode 0 or 2)	$V_{SS} \leq V_I \leq V_{DD}$	–	–	1	µA
Port outputs (Ports, RST and MOUT0 and MOUT2)						
I_{OL}	LOW-level output current; except P1.3, SDA, SCL and MOUT2	V_{OL} = 0.4 V	2	–	–	mA
I_{OL1}	LOW-level output current P1.3 (for LED)	V_{OL} = 0.4 V	6	–	–	mA
I_{OL2}	LOW-level output current; SDA, SCL and MOUT2	V_{OL} = 0.4 V; note 9	3	–	–	mA
I_{OH}	HIGH-level output current except P1.3; push-pull options only	$V_{OH} = V_{DD} - 0.4$ V	2	–	–	mA
I_{OH1}	HIGH-level output current P1.3 (for LED); push-pull options only	$V_{OH} = V_{DD} - 0.4$ V	6	–	–	mA
I_{OH2}	HIGH-level output current MOUT2	$V_{OH} = V_{DD} - 0.4$ V	3	–	–	mA
$I_{\overline{RST}}$	$\overline{RST}$ pull-up transistor current	V_{DD} = 3 V; $V_{OH} = V_{DD} - 0.4$ V	5	20	–	mA
		V_{DD} = 3 V; $V_{OH} = V_{SS}$	–	50	200	mA
Power-on-reset (POR); for the LVD (Low Voltage Detection) see note 10						
V_{PORH}	Power-on-reset trip level HIGH	option 5 in *"TELX family"* specification	2.13	2.37	2.61	V
V_{PORL}	Power-on-reset trip level LOW	option A in *"TELX family"* specification	1.98	2.27	2.56	V
TONE output (note 11 and Fig.12)						
$V_{HGF(rms)}$	HGF voltage (RMS)	V_{DD} = 3 V	158	181	205	mV
$V_{LGF(rms)}$	LGF voltage (RMS)		125	142	160	mV
$\Delta f/f$	frequency deviation		−0.6	–	+0.6	%
V_{DC}	DC voltage level		–	$0.5V_{DD}$	–	V
V_G	pre-emphasis of group		1.5	2.0	2.5	dB
THD	total harmonic distortion	V_{DD} = 3 V; T_{amb} = 25 °C; notes 5 and 12	–	25	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
In System Programming for the OTP						
t_{prog}	program cycle time		90	100	110	µs
t_{prog} (security)	program cycle time security	note 13	180	200	220	µs
t_{ver}	verify cycle time		1	–	–	µs
$t_{Vpp(setup)}$	program voltage setup time		10	–	–	µs
$t_{Vpp(max)}$	maximum program voltage time	cumulative for the product lifetime	–	–	60	s
I_{Vpp}	program voltage current	In system programming	–	–	40	mA
ACO (Amplitude Controlled Oscillator)						
V_{XTAL1}	external clock signal amplitude peak-to-peak		500	–	V_{DD}	mV
$Z_{i(XTAL1)}$	input impedance on XTAL1		300	1000	–	kΩ
C_{1i}; C_{2i}	input capacitance on XTAL1 and XTAL2	notes 5 and 14	–	10	–	pF

Notes

1. The operating supply current is measured with all output pins disconnected; $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; $\overline{RST} = V_{DD}$; XTAL1 driven with square wave; XTAL2 not connected; fetch of NOP instructions; all derivative blocks disabled.
2. The Idle mode supply current is measured with all output pins and $\overline{RST}$ disconnected; $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; XTAL1 driven with square wave; XTAL2 not connected; all derivative blocks disabled.
3. The Power-down current is measured with all output pins and $\overline{RST}$ disconnected; $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; XTAL1 and XTAL2 not connected.
4. The typical currents are only for the specific block. To calculate the typical power consumption of the microcontroller, the current consumption of the CPU must be added. Example: the typical current consumption of the microcontroller in operating mode with CPU, Watchdog Timer and UART active can be calculated as (1 + 0.11 + 0.09) mA = 1.2 mA.
5. Verified on sampling basis.
6. The input threshold voltage of P1.6/SCL and P1.7/SDA meet the I^2C-bus specification. Therefore, an input voltage below $0.3V_{DD}$ will be recognized as a logic 0 and an input voltage above $0.7V_{DD}$ will be recognized as a logic 1.
7. For the PORENABLE pin, $V_{IL(max)}$ is $0.1V_{DD}$.
8. Not valid for pins SDA, SCL, $\overline{RST}$, MIN and PORENABLE.
9. The maximum allowed load capacitance C_L is in this case limited to approximately 200 pF.
10. The LVD is tested according to the specification in the data sheet *"TELX family; Chapter: Low Voltage Detection"*.
11. Values are specified for DTMF frequencies only (CEPT CS203).
12. Related to the Low Group Frequency (LGF) component (CEPT CS203).
13. Can also be done by two 100 µs pulses.
14. C_{1i} and C_{2i} are the total internal capacitances (including gate capacitance and leadframe capacitance).

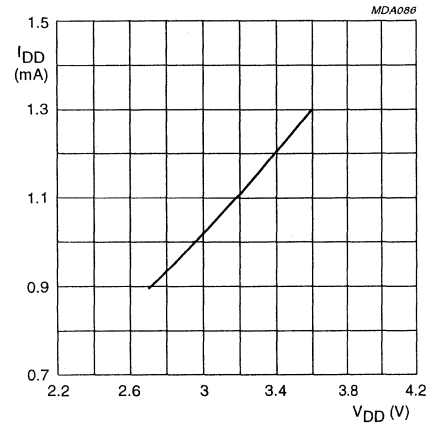


Fig.9 Typical operating current as a function of V_{DD}; T_{amb} = 25 °C.

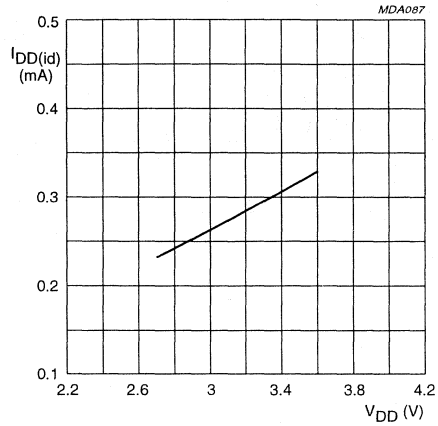
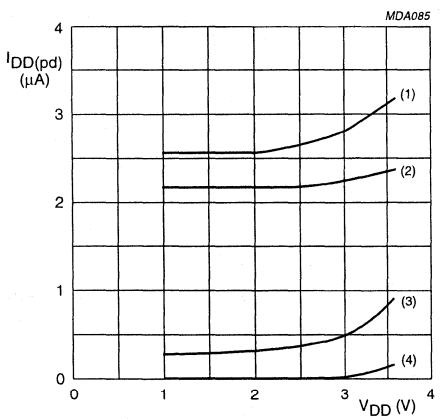
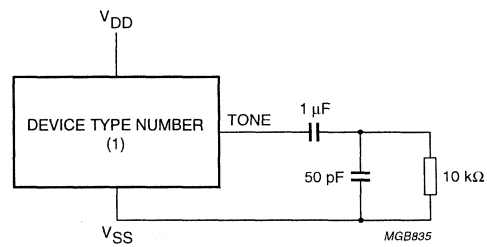


Fig.10 Typical Idle current as a function of V_{DD}; T_{amb} = 25 °C.



(1) POR and LVD enabled (T_{amb} = 70 °C).
(2) POR and LVD enabled (T_{amb} = 25 °C).
(3) POR and LVD disabled (T_{amb} = 70 °C).
(4) POR and LVD disabled (T_{amb} = 25 °C).

Fig.11 Typical Power-down current as a function of V_{DD}.



(1) P83CL887/P87CL887

Fig.12 TONE output test circuit.

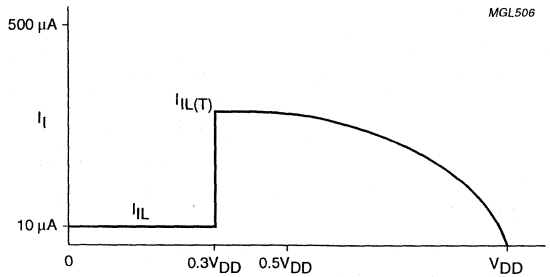


Fig.13 Input current.

Low voltage 16-bit microcontroller P90CL301BFH (C100)

FEATURES

- Fully 68000 software compatible
- Static design with 32-bit internal structure
- Power saving modes: Power-down, Standby and Idle mode
- External clock input: 27 MHz at 2.7 V
- Single supply voltage of 2.7 to 3.6 V; down to 1.8 V for RAM retention
- 68000 compatible bus interface
- Intel 8051 compatible bus interface
- 16 Mbytes program/data address range
- 8 programmable chip-selects
- Dynamic bus sizing, 16 or 8-bit memory bus port size
- 56 powerful instruction types:
  - 5 basic data types, and
  - 14 addressing modes
- 7 programmable interrupt inputs:
  - a Non-Maskable Interrupt input (NMIN)
  - 14 auto-vectored interrupts and 7 interrupt priority levels
- 24 port pins (multiplexed with other functions)
- 2 UART serial interfaces; an independent baud rate generator with two programmable outputs (UART0 and UART1)
- UART queue with maximum 256 bytes
- I^2C-bus serial interface 100 kbaud
- 2 timer arrays including:
  - two 16-bit reference counters and 8-bit programmable prescalers
  - six 16-bit match/capture registers with equality comparators
- Watchdog Timer with 21-bit resolution
- Two 8-bit Pulse Width Modulation (PWM) outputs with 8-bit prescaler
- Four 8-bit Analog-to-Digital Converter (ADC) inputs with Power-down mode
- 512 bytes RAM on-chip
- On-Circuit Emulation (ONCE) mode and internal Test-ROM (256 bytes) for on-board testing
- 80-pin LQFP package
- Temperature range –40 to +85 °C
- 0.5 micron CMOS low voltage technology.

DESCRIPTION

The P90CL301BFH is a highly integrated low-voltage 16/32-bit microcontroller especially suitable for digital mobile systems such as GSM, DCS1900, IS54/95 and other applications requiring low voltage, low power consumption and high computing power. It is fully software compatible with the 68000.

The P90CL301BFH optimizes system cost by providing both standard as well as advanced peripheral functions on-chip. The P90CL301BFH has a full static design and special Idle, Standby and Power-down modes which allow further reduction of the total system power consumption. An 80-pin LQFP package dramatically reduces system size requirements.

Compatibility between P90CL301AFH and P90CL301BFH

For functional compatibility between P90CL301AFH (SAC1 process) and P90CL301BFH (C100 process), the following points should be considered when using the P90CL301BFH:

- **Wake-up**; to wake-up the processor from Power-down mode via the activation of an external SPn pin, it is necessary to enable the interrupt mode first by setting the corresponding bit in the SPCON register.
- **SYSCON register**; for the P90CL301AFH bits 11 to 15 in the SYSCON register should not be set in order to keep additional functionality in the P90CL301BFH inactive.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			TEMPERATURE RANGE (°C)
	NAME	DESCRIPTION	VERSION	
P90CL301BFH	LQFP80	plastic low profile quad flat package; 80 leads; body 12 × 12 × 1.4 mm	SOT315-1	−40 to +85

BLOCK DIAGRAM

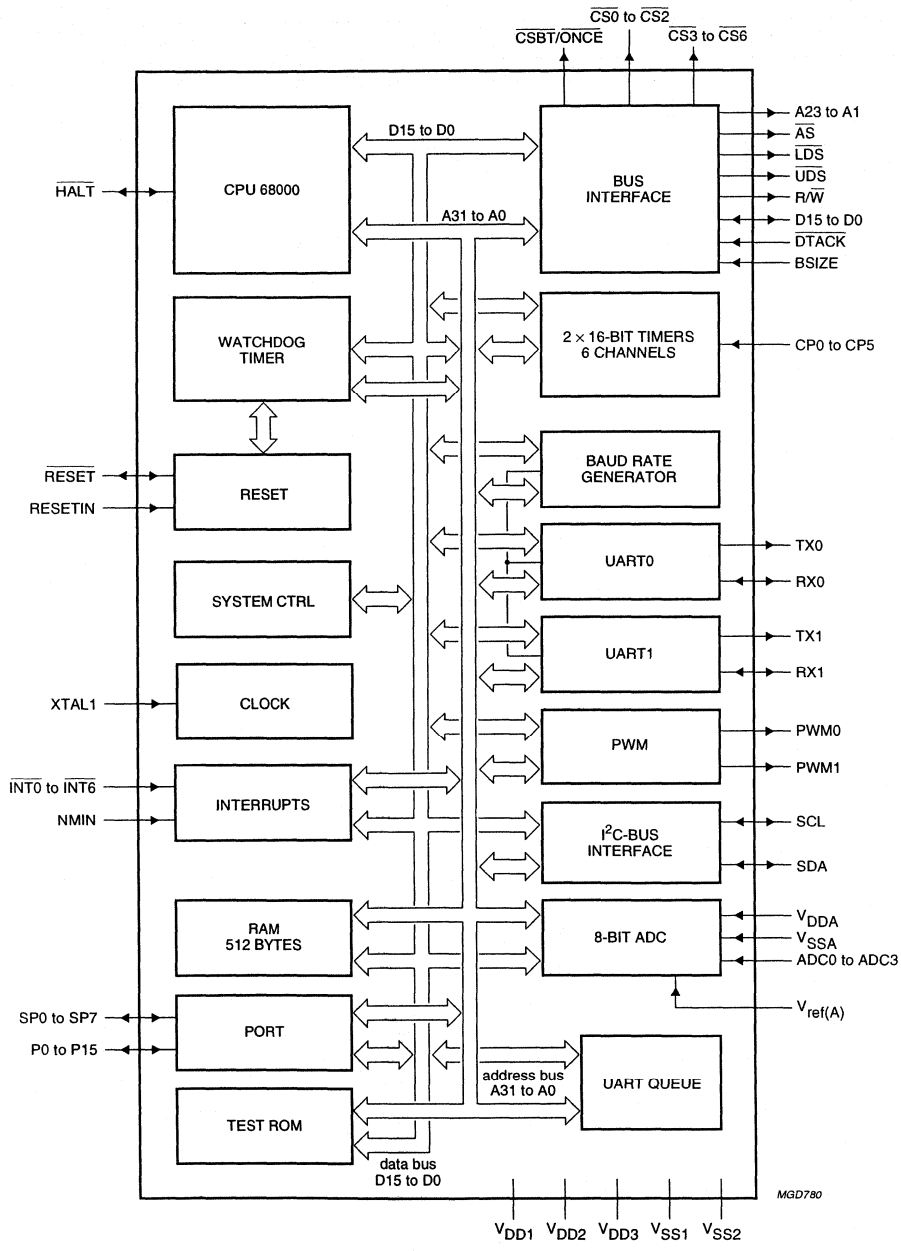


Fig.1 P90CL301BFH block diagram.

PINNING INFORMATION

Pinning

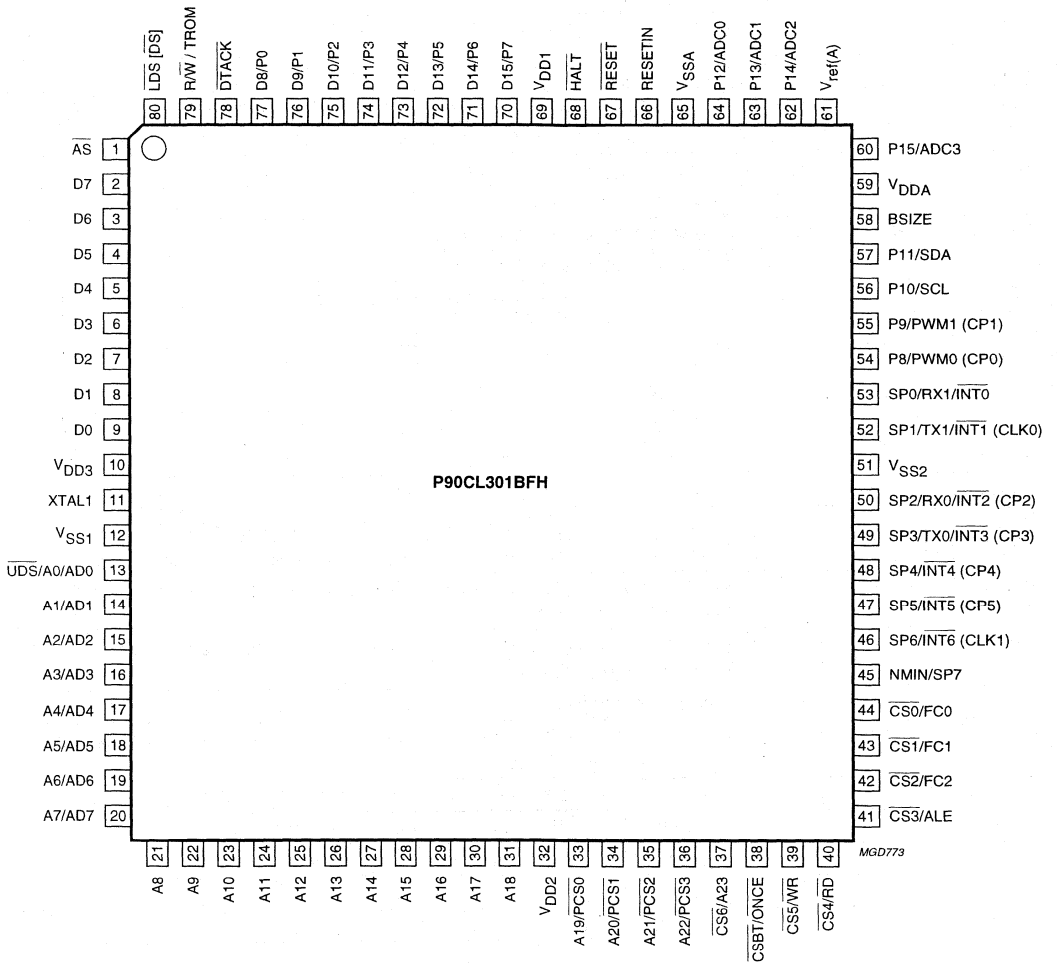


Fig.2 Pinning diagram of the P90CL301BFH (LQFP80).

Pin description

Table 1 Pin description for the P90CL301BFH

SYMBOL[1]	PIN	DESCRIPTION
$\overline{AS}$	1	address strobe
D7 to D0	2 to 9	lower 8-bits of data bus
V_{DD3}	10	supply voltage; third pin
XTAL1	11	external clock input
V_{SS1}	12	ground; first pin
$\overline{UDS}$/A0/AD0	13	upper data strobe or LSB of address bus or LSB of 8051 address/data
A1/AD1 to A7/AD7	14 to 20	lower 7-bits of the 68000 address bus or lower 7-bits of the 8051 bus
A8 to A18	21 to 31	upper 11-bits of the 68000 address bus
V_{DD2}	32	supply voltage; second pin
A19/$\overline{PCS0}$ to A22/$\overline{PCS3}$	33 to 36	upper 4-bits of the address bus or 8051 bus chip-select
$\overline{CS6}$/A23	37	chip-select 6 or address bit 23
$\overline{CSBT}$/$\overline{ONCE}$	38	chip-select boot or ONCE mode forced input
$\overline{CS5}$/$\overline{WR}$	39	chip-select 5 or 8051 bus write strobe
$\overline{CS4}$/$\overline{RD}$	40	chip-select 4 or 8051 bus read strobe
$\overline{CS3}$/ALE	41	chip-select 3 or 8051 bus address latch
$\overline{CS2}$/FC2 to $\overline{CS0}$/FC0	42 to 44	chip-select 2 to 0 or data bus function code 2 to 0
NMIN/SP7	45	Non-Maskable Interrupt or second port pin (bit 7)
SP6/$\overline{INT6}$ (CLK1)	46	second port pin (bit 6) external interrupt input 6 (external clock of timer 1)
SP5/$\overline{INT5}$ (CP5)	47	second port pin (bit 5) or external interrupt input 5 (Timer 1 capture input 5)
SP4/$\overline{INT4}$ (CP4)	48	second port pin (bit 4) or external interrupt input 4 (Timer 1 capture input 4)
SP3/TX0/$\overline{INT3}$ (CP3)	49	second port pin (bit 3) or Transmit data for UART0 or external interrupt input 3 (Timer 1 capture input 3)
SP2/RX0/$\overline{INT2}$ (CP2)	50	second port pin (bit 2) or Receive data for UART0 or external interrupt input 2 (Timer 0 capture input 2)
V_{SS2}	51	ground; second pin
SP1/TX1/$\overline{INT1}$ (CLK0)	52	second port pin (bit 1) or transmit data for UART1 or external interrupt input 1 (external clock of Timer 0)
SP0/RX1/$\overline{INT0}$	53	second port pin (bit 0) or receive data for UART1 or external interrupt input 0
P8/PWM0 (CP0)	54	port pin (bit 8) or PWM0 output (Timer 0 capture input 0)
P9/PWM1 (CP1)	55	port pin (bit 9) or PWM1 output (Timer 0 capture input 1)
P10/SCL	56	port pin (bit 10) or I^2C-bus Serial Clock.
P11/SDA	57	port pin (bit 11) or I^2C-bus Serial Data.
BSIZE	58	data bus size; 8 or 16-bit wide
V_{DDA}	59	ADC supply voltage
P15/ADC3	60	port pin (bit 15) or ADC input 3
$V_{ref(A)}$	61	ADC reference voltage
P14/ADC2 to P12/ADC0	62 to 64	port pin (bit 14 to bit 12) or ADC inputs 2 to 0
V_{SSA}	65	ADC ground
RESETIN	66	external Power-on-reset input

SYMBOL[1]	PIN	DESCRIPTION
$\overline{RESET}$	67	reset (bidirectional)
$\overline{HALT}$	68	halt (bidirectional)
V_{DD1}	69	supply voltage; first pin
D15/P7 to D8/P0	70 to 77	upper 8-bits of data bus or 8-bit Port 7 to Port 0; the selected function after reset is defined by pin BSIZE
$\overline{DTACK}$	78	data transfer acknowledge
R/$\overline{W}$ / TROM	79	read/write bus control or Test-ROM forced input
$\overline{LDS}$ [$\overline{DS}$]	80	lower data strobe [word data strobe]

Note

1. The following notation is used to describe the multiple pin definitions:
   a) Function1/Function2/Function3: multiplexed functions on the same pin. During and after reset the Function1 is selected.
   b) Function1 (Function2): function done in parallel.
   c) Function1 [Function2]: equivalent function.

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1 FEATURES

- Bellcore's 'CPE Alerting Signal (CAS)' and BT's 'Loop State Tone Alert Signal' detection
- BT's 'Idle State Tone Alert Signal' by means of monitoring the input signal level.
- 1200 baud FSK (Frequency Shift Keying) demodulator conform Bell 202 and CCITT V23 standards
- Ring or polarity change detector
- Ring period measurement
- Low battery comparator
- Signal level detector
- On-hook and off-hook application according to *"Bellcore TR-NWT-000030"* and *"SR-TSV-002476"* specifications
- Receive sensitivity of –37.8 dBm (in 600 Ω) for CAS
- 2.5 to 3.6 V supply; low power standby mode
- Selectable 1 second or 1 minute timebase interrupt
- 3.58 MHz and 32.768 kHz crystal oscillators
- SO16 package.

2 APPLICATIONS

- Analog Display Services Interface (ADSI) phones
- Feature phones and adjunct boxes with Bellcore CID (Caller-ID), CIDCW (Caller-ID on Call Waiting) and CNAM (Caller-Name) systems
- Computer Telephony Integrated (CTI) systems.

3 GENERAL DESCRIPTION

The PCD3316 is a low power mixed signal CMOS integrated circuit for receiving physical layer signals like Bellcore's CAS and the signals used in similar services. The device is capable of a very high precision detection of the dual tone (2130 and 2750 Hz) by using a patented digital algorithm. The PCD3316 can be used for on-hook and off-hook CID, CIDCW and CNAM applications.

For timing purposes the PCD3316 can be programmed to generate an interrupt signal to the microcontroller every second or every minute. These timings are derived from an on chip 32.768 kHz oscillator.

Also incorporated in the device are an FSK receiver/demodulator and a Ring or Polarity Change detector.

The status of the PCD3316, the received FSK data bytes and the ringer period can be read and many options can be selected via the I^2C-bus serial interface.

Two on-chip oscillators are available.
One 3.58 MHz oscillator for all internal functions and a low frequency 32.768 kHz oscillator for the 1 second or 1 minute timing.

In Power-down mode only the polarity comparators and the 32.768 kHz oscillator are active. The CAS detection, the FSK receiver and the 3.58 MHz oscillator can be enabled separately. Detection of a polarity change on the inputs POL0 or POL1, the reception of an FSK data byte, the detection of a CAS tone or a timebase interrupt is signalled to the microcontroller by an interrupt request signal (IRQ). The microcontroller can communicate with the PCD3316 device via the serial interface.

The PCD3316 is designed for use in a microcontroller controlled system.

The device is available in a SO16 package.

A demonstration board OM5843 is available.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD3316T	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1

5 BLOCK DIAGRAM

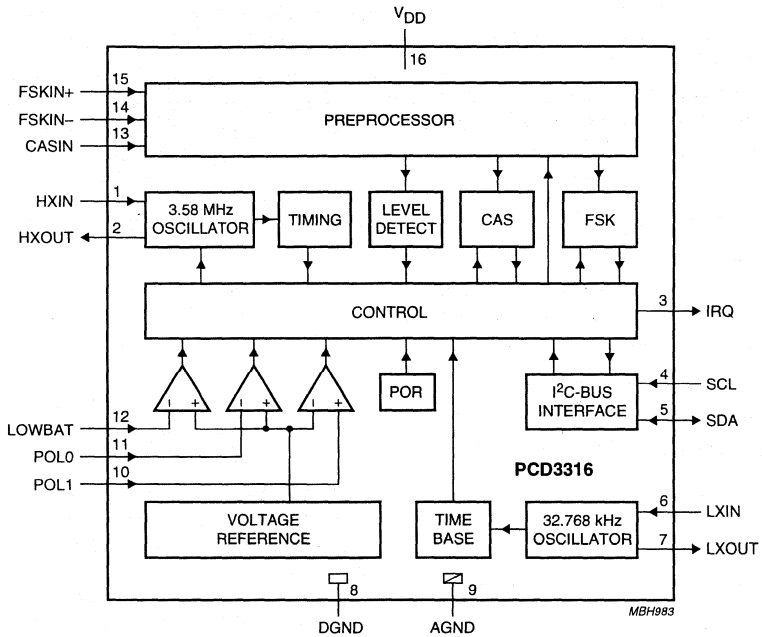


Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	I/O	DESCRIPTION
HXIN	1	I	3.58 MHz crystal oscillator input
HXOUT	2	O	3.58 MHz crystal oscillator output
IRQ	3	O	interrupt output; programmable active HIGH or active LOW
SCL	4	I	serial clock line of I^2C-bus
SDA	5	I/O	serial data line of I^2C-bus
LXIN	6	I	32.768 kHz crystal oscillator input
LXOUT	7	O	32.768 kHz crystal oscillator output
DGND	8	–	digital ground
AGND	9	–	analog ground
POL1	10	I	polarity detector input 1
POL0	11	I	polarity detector input 0
LOWBAT	12	I	low battery detector input
CASIN	13	I	input pin for CAS signal
FSKIN–	14	I	negative input for FSK signal
FSKIN+	15	I	positive input for FSK signal
V_{DD}	16	–	supply

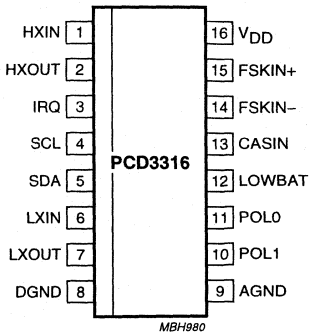


Fig.2 Pin configuration.

7 FUNCTIONAL DESCRIPTION

7.1 Preprocessor and analog inputs

The preprocessor for the CAS detection and the FSK receiver incorporates an A/D converter and a digital bandpass filter.

The LOWBAT input of the PCD3316 can be used for low battery detection. The voltage on the LOWBAT pin is compared with an internal voltage reference circuit. When the LOWBAT voltage drops below the reference voltage, Status register, bit 5 is set to logic 1.

The PCD3316 can be forced in a Power-down state by switching off the 3.58 MHz system clock and the A/D converter. This is done by setting Mode register 2, bit 7 to logic 0. To guarantee correct operation the following order of actions must be performed: (see also Section 7.8 about interrupts)

1. Switch off CAS and FSK detection (if turned on)
2. Read the interrupt register (thus clearing pending interrupts generated by the CAS and FSK detector)
3. Switch off the 3.58 MHz oscillator by clearing bit 7 of Mode register 2.

Two low power comparators (inputs POL0 and POL1) and the 32.768 kHz clock are always active. They can be used for ring or line polarity reversal detection. The POL on/off bit (Mode register 1, bit 4) must be set to enable generation of an interrupt when a polarity change occurs. The result of the two comparators can be read in bits 7 and 6 (POL0 and POL1) of the Status register (see Section 7.4).

No 3.58 MHz clock is needed for the generation of a polarity interrupt.

7.2 CAS detection

After a Power-on reset or after enabling the CAS detector the internal registers of the CAS detection function are initialized. The initialization takes a maximum of 100 periods of the 3.58 MHz clock.

If the CAS detection is enabled the PCD3316 will generate an interrupt (Interrupt register, bit 1 is set) when a correct dual tone (2130 and 2750 Hz) is detected. Interrupts will be blocked when the signal level on the CAS input is below the threshold in the level detector.

7.3 FSK reception

The FSK receiver function can be enabled by setting the FSK on/off bit (Mode register 1, bit 7).

In the FSK transmission specification of BT and Bellcore a channel seizure is transmitted first (sequence of 1010..). After the channel seizure a block of marks and finally the data pattern is sent (see Fig.3). These mark bits are detected by the PCD3316 which sets the FSK-BOM Indication bit (Status register, bit 4). The FSK-BOM Indication bit is reset when the FSK receiver is disabled.

If the FSK-BOM Indication bit is set, the FSK receiver will generate an interrupt after it has received a complete data word. An FSK data word consists of one start bit (space), followed by eight data bits and one stop bit (mark). Interrupts will therefore not be generated during the channel seizure and during the block of marks. When a valid data word has been received, FSK data is available in the FSK data register.

By clearing the FSK BOM-mask on/off bit (Mode register 1, bit 6), the FSK receiver will not wait with the generation of interrupts until a Begin Of Mark (BOM) has been detected but will handle the channel seizure as normal data. The block of marks which is a string of logic 1 will still not generate interrupts because there are no start bits

After the generation of an interrupt the IRQ pin will become active (see Fig.4), and the FSK Interrupt bit is set (Interrupt register, bit 5). The received data is available in the FSK data register.

The FSK-OVR Error bit (Status register, bit 3) indicates that a previous byte is lost due to an overrun.
The FSK-FRM Error bit (Status register, bit 2) indicates an incorrect start- or stop-bit. These frame errors indicate that there are synchronization problems.

The on-chip level detector can be used to detect a carrier loss during FSK transmission. FSK data can be rejected when the signal level is below the reference level, this to avoid that noise is interpreted as data. (Interrupt register, bit 4 is logic 1)

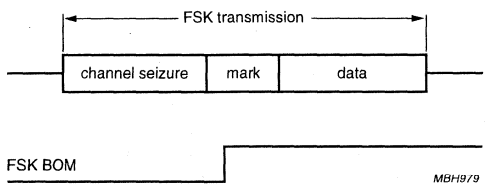


Fig.3 FSK transmission specification.

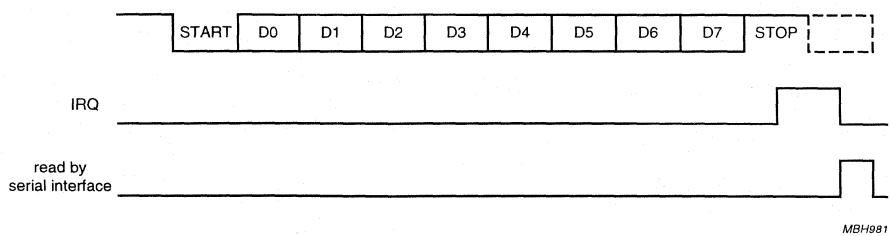


Fig.4 IRQ generation after reading a valid data byte.

7.4 Ring or polarity change detector

For ring and polarity change detection two comparators are available in the PCD3316. The reference level of the comparators is set internally by the reference voltage generator. The voltage levels on the two polarity comparator inputs, POL0 and POL1, are compared with the reference voltage V_{ref}. If POL0 < V_{ref} or POL1 > V_{ref}, POL0 and POL1 of the Status register (Status register, bit 7 and 6) are set respectively and reset if POL0 > V_{ref} and POL1 < V_{ref}. Every time the POL0 status bit changes from logic 1 to logic 0, a POL0 interrupt is generated. Every time the POL1 status bit changes from logic 0 to logic 1, a POL1 interrupt is generated.

The period time of a POL1-POL0-POL1 sequence is available in the Ringer period register. It is preset to 255 on Power-on and updated every time a POL1 interrupt is generated. The sequence is:

- Power-on:
  - Ringer period register = 255
- First POL1 interrupt:
  - Ringer period register = 255
- First POL1 interrupt after a POL0 interrupt:
  - Ringer period register = new time
- First POL1 interrupt after more than $^{255}/_{2048}$ s:
  - Ringer period register = 255.

The period is given in multiples of $^{1}/_{2048}$ s. The maximum value is 255.

The POL1-POL0-POL1 sequence is recognized when one or more POL1 interrupts are generated followed by one or more POL0 interrupts, followed by a POL1 interrupt.

The 32.768 kHz clock is needed for the generation of a polarity interrupt.

7.5 Low battery detection

The low battery voltage detection input (pin LOWBAT) is connected to the positive input of a comparator.
The negative input is connected to the internal reference voltage. If the voltage on the LOWBAT input pin is less than the reference voltage V_{ref}, the LOW-BAT Indication (Status register, bit 5) is set. If the LOWBAT input rises above V_{ref} again, the LOW-BAT Indication is cleared.

The 32.768 kHz clock signal must be available.

The LOW-BAT Indication bit does not generate interrupts, thus the bit should be polled.

Table 1 Selection of interrupt modes

MODE REGISTER 2		INTERRUPT REGISTER	INTERRUPT
TB on/off (BIT 6)	SEC/MIN (BIT 5)		
0	X (don't care)	bit 7 = 0; bit 6 = 0	no time base interrupt (time base is reset)
1	0	bit 7 = 1; bit 6 = 0	every minute an interrupt is generated; no second interrupt;
1	1	bit 7 = 1; bit 6 = 1	every second an interrupt is generated; every minute an interrupt is generated

7.6 Level detect

When the input signal level on the FSK or the CAS input (the one that is selected) is below a threshold of typically −40 dBm, the Low Level bit will be set (Interrupt register, bit 4). The level detector can be used to observe a carrier loss during FSK transmission and to detect the 'Idle State Tone Alert Signal' for British Telecom.

The signal power on the input can be monitored by polling the register bit since it will not generate an interrupt. The Low Level bit will be updated every 8 ms. When FSK and CAS are both disabled the signal level on the FSK input is measured

The 32.768 kHz clock signal must be available.

7.7 Time base

The 32.768 kHz oscillator is used to generate either a 1 second or a 1 minute interrupt signal. If the TB on/off bit is set (Mode register 2, bit 6) every second or minute an interrupt is generated and MIN Interrupt and/or SEC Interrupt bits (Interrupt register, bit 7 and 6) are set. After reading the Interrupt register the interrupt is cleared.
The SEC/MIN (Mode register 2, bit 5) selects whether every second (SEC/MIN is set) or every minute (SEC/MIN is cleared) an interrupt is generated. All possible selections are shown in Table 1. Resetting bit TB on/off in Mode register 2 will only disable time base interrupts, and the 32 kHz oscillator will continue to run.

7.8 Interrupt

The interrupt request output (IRQ) is active HIGH by default. The polarity of the IRQ output can be made active LOW by the INT Polarity HIGH/LOW bit (Mode register 1, bit 3). The IRQ pin is in 3-state when not active, so an external pull-up or pull-down resistor is required.
The interrupt cause is indicated by the flags in the Interrupt register. Interrupt flags are set by hardware but must be reset by software. All flags of the Interrupt register are reset when the register is read via I^2C-bus interface.

The IRQ pin is deactivated at the positive edge of SCL which reads the first data bit of the Interrupt register. The IRQ pin will stay inactive for one SCL cycle. IRQ can handle a next interrupt after the next positive edge of SCL.

7.9 The internal Power-on reset (POR)

The device contains an on-chip Power-on reset circuitry which activates a reset as long as V_{DD} is below a predefined level $V_{POR(H)}$. If V_{DD} exceeds $V_{POR(H)}$, the 3.58 MHz oscillator will start. The PCD3316 is initialized and the internal registers are set to the default value (see Section 7.13). It takes a maximum of 100 cycles of the 3.58 MHz clock to initialize all internal functions. The POR circuitry also ensures, that the chip will be switched off as soon as a falling V_{DD} reaches a predefined level ($V_{POR(L)}$).

7.10 3.58 MHz oscillator circuitry

The 3.58 MHz oscillator is needed for the FSK receiver and the CAS detection. This on-chip amplitude controlled oscillator circuitry is a single-stage inverting amplifier biased by an internal feedback resistor R_{fb}. The oscillator circuit is shown in Fig.5. When using a quartz resonator to drive the oscillator, normally no external components are needed. When using ceramic resonators to drive the oscillator, in some cases external components are needed depending on the ceramic resonator specifications (refer to product specification). Two different configurations are shown in Fig.7a and b.

To drive the device with an external clock source, apply the external clock signal to HXIN, and leave HXOUT to float, as shown in Fig.7c. If the amplitude of the input signal is less than V_{DD} to GND or a sine wave is applied, capacitive decoupling is needed as shown in Fig.7d.

In the Power-down mode (Mode register 2, bit 7 = 0), the oscillator is stopped and HXIN and HXOUT are internally pulled LOW. The current of the whole oscillator is switched off.

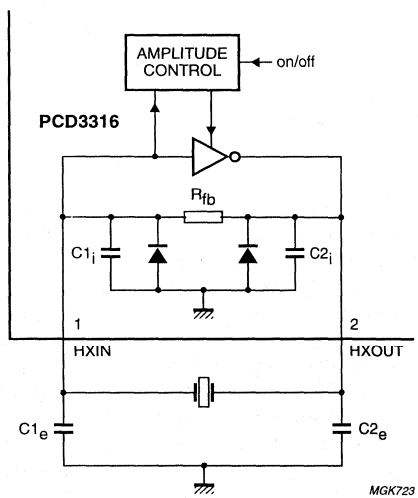
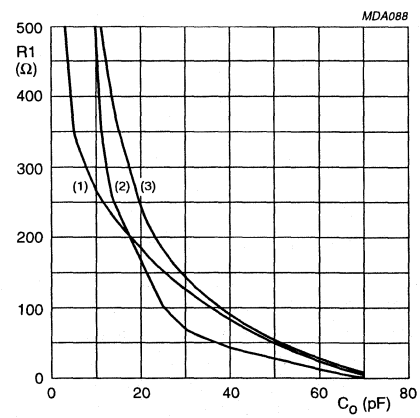


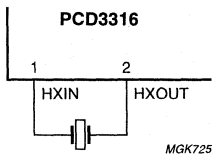
Fig.5 Oscillator.



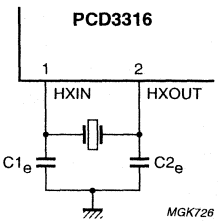
C_{1e} and C_{2e} are the external load capacitances (see Fig.7b). Normally, they are not needed (curve 2) due to integrated load capacitances of 10 pF.

(1) $C_{1e} = C_{2e} = 22$ pF.
(2) $C_{1e} = C_{2e} = 0$ pF.
(3) $C_{1e} = C_{2e} = 12$ pF.

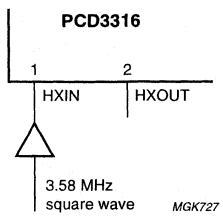
Fig.6 Resonator requirements for the ACO (see Fig.8 for equivalent circuit).



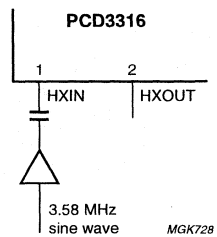
a. Standard oscillator (quartz or PXE).



b. Oscillator (quartz or PXE) with external capacitors.



c. External clock (square wave).



d. External clock (sine wave).

Fig.7 3.58 MHz oscillator configurations.

For correct function of the oscillator, the values of R_1 and C_0 of the chosen resonator in Fig.8 (quartz or PXE) must be below the line shown in Fig.6. The value of the parallel resistor R_0 must be less than 47 kΩ.

Recommended resonator types are:

- CSA 3.58MG (supplier Murata)
- FCR 3.58M5 (supplier TDK).

The wiring between chip and resonator should be kept as short as possible.

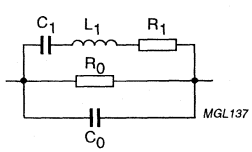


Fig.8 Resonator equivalent circuit.

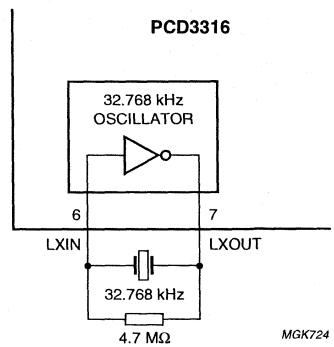


Fig.9 Connections of the 32kHz oscillator.

7.11 32 kHz oscillator

The 32.768 kHz oscillator is enabled permanently and is used to generate either a 1 second or 1 minute interrupt. The 32.768 kHz clock is also used for the 'Ring or polarity change detector', the 'Low battery detection' and the 'Level detect' function.

An external 32.768 kHz signal may be applied to pin LXIN while leaving pin LXOUT not connected.

The 32 kHz oscillator requires an external 32.768 kHz quartz crystal and an external feedback resistor (4.7 MΩ) between the LXIN and LXOUT pins. See Fig.9.

7.12 Serial interface

The serial interface of the PCD3316 is the I²C-bus. A detailed description of the I²C-bus specification, including applications, is given in the brochure: *"The I²C-bus and how to use it"*, order no. 9398 393 40011 or *"I²C Peripherals Data Handbook IC12"*, order no. 9397 750 01647.

7.12.1 Characteristics of the I²C-bus (see Fig.10)

A device generating a message is a 'transmitter', a device receiving a message is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are called the 'slaves'. The PCD3316 operates in the slave transmitter/receiver mode only.

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

7.12.2 Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as a stop condition (P) (see Fig.11).

7.12.3 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal (see Fig.12).

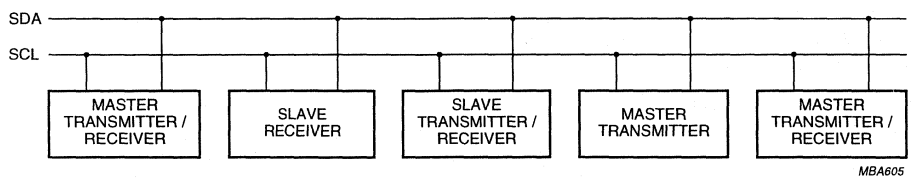


Fig.10 I²C-bus configuration.

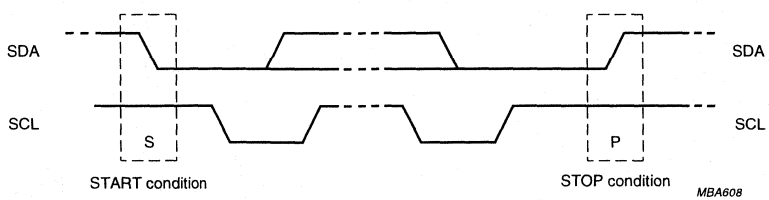


Fig.11 Start and stop conditions for the I²C-bus.

7.12.4 ACKNOWLEDGE

The number of data bytes transferred between the start and the stop conditions from the transmitter to the receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge-related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges must pull down the SDA line during the acknowledge clock period (SCL LOW + HIGH) immediately after the 8th SCL pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

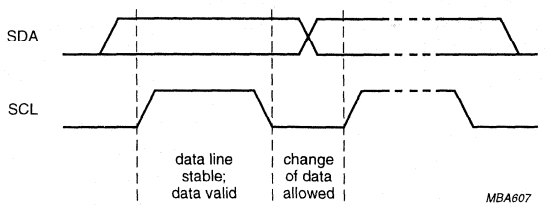


Fig.12 I²C-bus bit transfer.

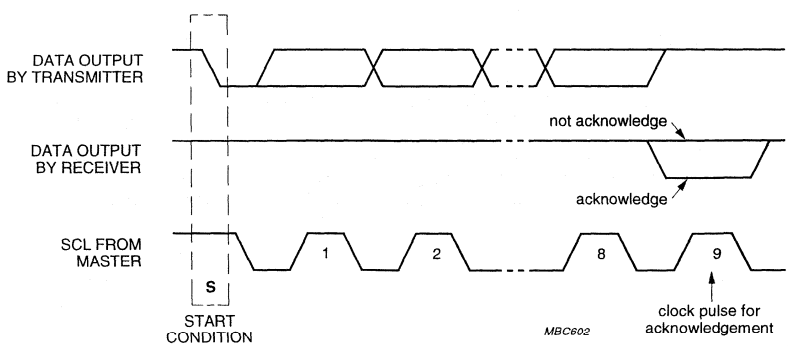


Fig.13 I²C-bus acknowledge.

7.12.5 I²C-BUS PROTOCOL

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always carried out with first byte transmitted after the start procedure. One I²C slave address is reserved for the PCD3316, E0H (1110 0000 for write and 1110 0001 for read).

The I²C protocol is shown in Figs 14 and 15. Two different sequences are considered, the WRITE sequence and the READ sequence. Both sequences are initiated with a start condition (S) from the I²C-bus master which is followed by the PCD3316 slave address with the read bit cleared. The first byte after the I²C address is interpreted as the address of a PCD3316 register.

During the write sequence the register address of the PCD3316 is auto-incremented on each acknowledge. The write sequence is ended with a stop condition from the master. If the addressed register is read-only or non-existent, nothing will be changed.

For the read sequence the bus master issues a repeated start condition followed by the PCD3316 slave address with the read bit set. Then data is read from previously set address and sent out. When the master responds with an acknowledge the address of the register is autoincremented and the slave will put the data from the next register on the bus. The read sequence is stopped when the master stops giving an acknowledge and generates a stop condition. When a non-existing register is addressed the PCD3316 will return FFH. Existing register addresses are shown in Section 7.13. An additional register address (73H) is reserved for test purposes. This address cannot be reached with the auto-increment function of the I²C-interface.

7.12.6 I²C-BUS BIT RATE

When a microcontroller is used that implements an I²C-bus in software, the bit rate of the I²C-bus can be critical during reception of FSK. The collection of the interrupt data and FSK-data from the PCD3316 takes 48 bits on the I²C-bus. With an FSK baud rate of 1200 (corresponds to 1200 bits per second) the minimal speed of the I²C-bus should be 5.76 kbits/s. Additional interrupts generated by the time base of the PCD3316 will cause the processor to collect extra information from the PCD3316. As a consequence, the FSK-data can be overrun in the PCD3316 and one data byte will be lost. In this case, the time base interrupt should be suppressed while FSK is active. This can be done by setting the INT-SUP on/off bit (bit 4 in Mode register 2). The TB on/off bit (bit 6 in Mode register 2) will still be set but the IRQ output will not be activated by the time base interrupt. Any time base interrupt can be detected by the microcontroller when an FSK interrupt is processed by reading the Interrupt register.

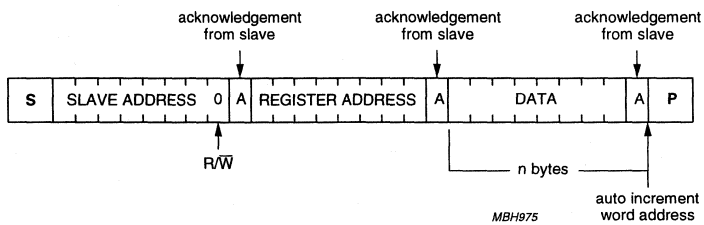


Fig.14 I²C-bus write sequence.

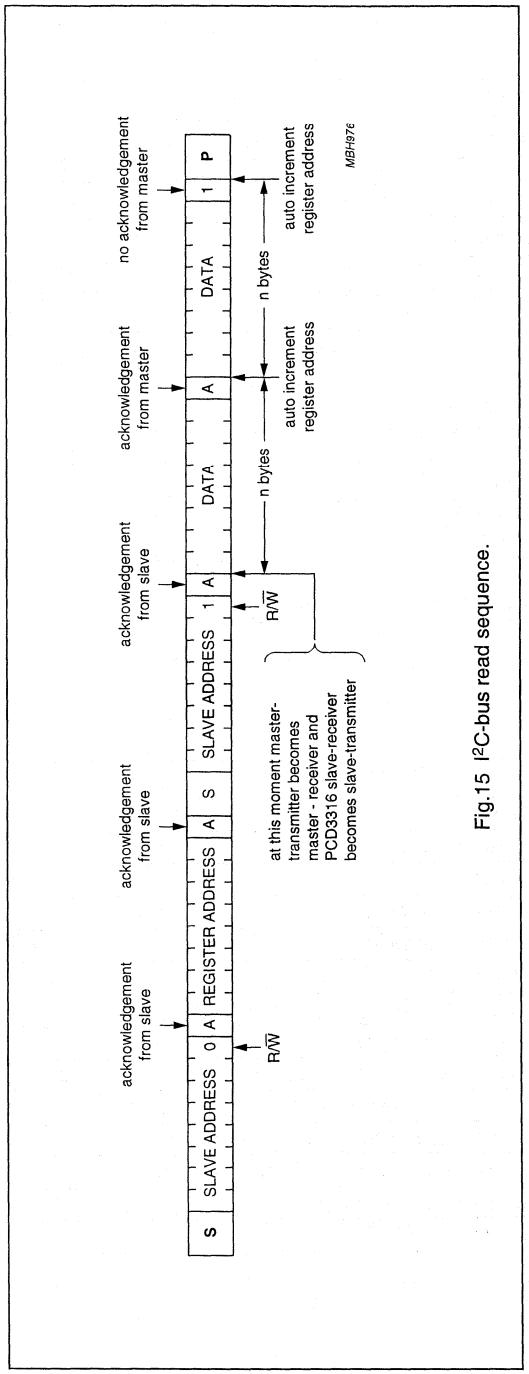


Fig.15 I²C-bus read sequence.

7.13 Register overview

Table 2 Register contents

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Interrupt register CIDINT; address 00H; read only; see Table 3							
MIN Interrupt	SEC Interrupt	FSK Interrupt	Low Level Status	POL1 Interrupt	POL0 Interrupt	CAS Interrupt	RES
FSK data register CIDFSK; address 01H; read only; see Table 4							
D7	D6	D5	D4	D3	D2	D1	D0
Status register CIDSTA; address 02H; read only; see Table 5							
POL1	POL0	LOW-BAT Indication	FSK-BOM Indication	FSK-OVR Error	FSK-FRM Error	RES	RES
Ringer period register CIDRNG; address 03H; read only; see Table 6							
D7	D6	D5	D4	D3	D2	D1	D0
Mode register 1 CIDMD1; address 04H; read/write; see Table 7							
FSK on/off	FSK BOM-mask on/off	CAS on/off	POL on/off	INT Polarity HIGH/LOW	RES	RES	RES
Mode register 2 CIDMD2; address 05H; read/write; see Table 8							
XTAL on/off	TB on/off	SEC/MIN	INT-SUP on/off	RES	RES	VERSION 1	VERSION 0

7.14 Detailed register descriptions

Table 3 Description of the Interrupt register bits

BIT	SYMBOL	DEFAULT	DESCRIPTION
CIDINT.7	MIN Interrupt	0	0: no interrupt request
			1: one minute interrupt request
CIDINT.6	SEC Interrupt	0	0: no interrupt request
			1: one second interrupt request
CIDINT.5	FSK Interrupt	0	0: no FSK interrupt or FSK disabled
			1: FSK interrupt, one byte received
CIDINT.4	Low Level Status	0	0: signal level on selected input above power reference (no interrupt)
			1: signal level on selected input below power reference (no Interrupt)
CIDINT.3	POL1 Interrupt	0	0: no zero to one changes on POL1 input or polarity interrupt disabled
			1: a one to zero input change on the POL1 input is detected
CIDINT.2	POL0 Interrupt	0	0: no one to zero changes on POL0 input or polarity interrupt disabled
			1: a zero to one input change on the POL0 input is detected
CIDINT.1	CAS Interrupt	0	0: no CAS signal detected or CAS disabled
			1: CAS signal detected
CIDINT.0	RES	0	reserved bit

Table 4 Description of FSK data bits

BIT	SYMBOL	DESCRIPTION
CIDFSK.7 to CIDFSK.0	D7 to D0	If an FSK interrupt has occurred and no FSK error is detected, the FSK data register contains valid data.

Table 5 Description of the status register bits.

BIT	SYMBOL	DESCRIPTION
CIDSTA.7	POL1	0: POL1 input < V_{ref}
		1: POL1 input > V_{ref}
CIDSTA.6	POL0	0: POL0 input > V_{ref}
		1: POL0 input < V_{ref}
CIDSTA.5	LOW-BAT Indication	0: LOWBAT input > V_{ref}
		1: LOWBAT input < V_{ref}
CIDSTA.4	FSK-BOM Indication	0: begin of mark period not yet detected
		1: begin of mark period detected
CIDSTA.3	FSK-OVR Error	0: no FSK overrun error
		1: FSK overrun error, data byte(s) lost
CIDSTA.2	FSK-FRM Error	0: no FSK frame error
		1: FSK frame error, stop bit was wrong
CIDSTA.1	RES	reserved bit
CIDSTA.0	RES	reserved bit

Table 6 Description of CIDRNG bits

BIT	SYMBOL	DESCRIPTION
CIDRNG7 to CIDRNG0	D7 to D0	time between two positive edges of the POL1 comparator output (between two positive edges of POL1 one positive edge of POL0 must have been detected)

Table 7 Description of the Mode register 1 bits.

BIT	SYMBOL	DEFAULT	DESCRIPTION
CIDMD1.7	FSK on/off	0	0: FSK receiver disabled
			1: FSK receiver enabled
CIDMD1.6	FSK BOM-mask on/off	1	0: enable FSK interrupts before mark period
			1: disable FSK interrupts before mark period
CIDMD1.5	CAS on/off	0	0: CAS detector disabled
			1: CAS detector disabled
CIDMD1.4	POL on/off	1	0: disable interrupts due to polarity change
			1: enable interrupts due to polarity change
CIDMD1.3	INT polarity HIGH/LOW	1	0: interrupt pin active LOW
			1: interrupt pin active HIGH
CIDMD1.2	RES	0	reserved bit
CIDMD1.1	RES	0	reserved bit
CIDMD1.0	RES	0	reserved bit

Table 8 Description of the Mode register 2 bits

BIT	SYMBOL	DEFAULT	DESCRIPTION
CIDMD2.7	XTAL on/off	1	0: disable 3.58 MHz oscillator
			1: enable 3.58 MHz oscillator
CIDMD2.6	TB on/off	1	0: disable 32.768 kHz timebase
			1: enable 32.768 kHz timebase
CIDMD2.5	SEC/MIN	0	0: every minute a timebase interrupt
			1: every second a timebase interrupt
CIDMD2.4	INT-SUP on/off	1	0: enable SEC/MIN interrupts during FSK reception
			1: disable SEC/MIN interrupts during FSK reception
CIDMD2.3	RES	0	reserved bit
CIDMD2.2	RES	0	reserved bit
CIDMD2.1	RES	0	reserved bit
CIDMD2.0	RES	0	reserved bit

8 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	4.0	V
V_I	input voltage on any pin	−0.5	V_{DD} + 0.5	V
P_{tot}	total power dissipation	−	800	mW
T_{stg}	storage temperature	−50	+125	°C

9 ELECTRICAL CHARACTERISTICS

V_{DD} = 2.5 to 3.6 V; T_{amb} = −25 to +70 °C; HXIN = 3.579545 MHz ±0.05%; LXIN = 32.768 kHz ±0.1%; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	note 1	2.5	3.3	3.6	V
$V_{POR(H)}$	power-on reset high voltage		1.85	2.05	2.25	V
$V_{hys(POR)}$	power-on reset hysteresis voltage	note 2	50	100	150	mV
I_{DD}	supply currents	V_{DD} = 2.5 V				
	power down	note 3	−	30	45	µA
	operating	notes 3 and 4	−	2.0	2.3	mA
Low voltage and polarity comparators (pins LOWBAT, POL0 and POL1)						
V_{hys}	hysteresis voltage of POL0, POL1 and LOWBAT inputs		−	20	−	mV
I_i	input current	note 5	−	−	1	µA
Internal reference						
V_{ref}	reference voltage level		1.125	1.25	1.375	V
$P_{i(ref)}$	input signal reference power	in 600 Ω load, note 6	−43.8	−	−37.8	dBm
$t_{r(level)}$	input signal to Low Level bit rise time	input signal power < $P_{i(ref)}$	−	−	8	ms
$t_{f(level)}$	input signal to Low Level bit fall time	input signal power > $P_{i(ref)}$	−	−	8	ms
Logical output (pin IRQ) (see note 7)						
I_{OL}	LOW level output current	V_{IRQ} = 0.4 V	2	−	−	mA
I_{OH}	HIGH level output current	V_{IRQ} = V_{DD} − 0.4 V	2	−	−	mA
FSK receiver (pins FSKIN+ and FSKIN−)						
Z_i	input impedance FSKIN+ to FSKIN−		−	1.4	−	MΩ
$Z_{source(max)}$	maximum source impedance		−	−	200	kΩ
$P_{i(FSKIN)}$	input signal power	in 600 Ω load; note 8	−45	−	0	dBm
$TH_{ns(FSK)}$	no signal threshold	in 600 Ω load	−43.8	−	−37.8	dBm
S/N_{FSK}	signal-to-noise ratio	200 to 3400 Hz	20	−	−	dB
$\lvert V_{dif} \rvert$	differential voltage between mark and space (twist)		−	−	10	dB
f_D	data transmission rate		1180	1200	1212	bits/s

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_s	space frequency		2068	–	2222	Hz
f_m	mark frequency		1188	–	1320	Hz
CAS detector (pin CASIN)						
Z_i	input impedance CASIN to V_{ref}		–	1.4	–	MΩ
$Z_{source(max)}$	maximum source impedance		–	–	200	kΩ
P_i	input signal power	in 600 Ω load	–37.8	–	0	dBm
$TH_{ns(CAS)}$	no signal threshold (CAS)	in 600 Ω load	–43.8	–	–37.8	dBm
f_l	low tone frequency		–	2130	–	Hz
f_h	high tone frequency		–	2750	–	Hz
Δf_{max}	maximum frequency deviation	note 9	–0.5	–	+0.5	%
V_{dif}	differential voltage level (twist)	note 9	–	–	6	dB
t_{dt}	dual tone detection time		60	–	–	ms
I^2C interface (pins SCL and SDA); see Figs 16 and 17						
V_{IL}	LOW level input voltage	note 10	0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage	note 10	$0.7V_{DD}$	–	V_{DD}	V
I_{OL1}	LOW level output current for pin SDA (open drain)	$V_{O(SDA)}$ = 0.4V	2	–	–	mA
C_i	capacitance for each I/O pin		–	–	10	pF
f_{SCL}	SCL clock frequency		–	–	100	kHz
t_{BUF}	bus free time		4.7	–	–	µs
$t_{SU;STA}$	start condition set-up time		4.7	–	–	µs
$t_{HD;STA}$	start condition hold time		4.0	–	–	µs
t_{LOW}	SCL LOW time		4.7	–	–	µs
t_{HIGH}	SCL HIGH time		4.0	–	–	µs
t_r	maximum SCL and SDA rise time	note 11	–	–	1000	ns
t_f	maximum SCL and SDA fall time	note 11	–	–	300	ns
$t_{SU;DAT}$	data set-up time		250	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	–	ns
$t_{VD;DAT}$	SCL LOW to data out valid time		–	–	3.4	µs
$t_{SU;STO}$	stop condition set-up time		4.0	–	–	µs
3.58 MHz oscillator (pins HXIN and HXOUT)						
$V_{HXIN(p-p)}$	external clock signal amplitude (peak-to-peak value)		0.5	–	V_{DD}	V
$Z_{i(HXIN)}$	input impedance on pin HXIN		300	1000	–	kΩ
C_{1i}; C_{2i}	input capacitance on pins HXIN and HXOUT	note 12	–	10	–	pF
32 kHz oscillator (pins LXIN and LXOUT)						
g_m	transconductance	$V_{i(p-p)} < 50$ mV	2	4	10	µS
$C_{i(LXIN)}$	LXIN input capacitance		–	13	–	pF
$C_{o(LXOUT)}$	LXOUT output capacitance		–	10	–	pF

Notes to the characteristics.

1. Except for FSK and CAS detection, all circuitry works already when $V_{DD} > V_{POR(H)}$. Since the I^2C-bus interface will work (starts to acknowledge), the application can start reading the LOWBAT bit (Status register, bit 5) to check whether the supply voltage has reached the operating voltage level. A voltage divider network can be connected to pins V_{DD}, LOWBAT and GND such that $V_{LOWBAT} = V_{ref}$ if $V_{DD} = V_{DD(min)}$.
2. The Power-on reset low level is defined as $V_{POR(L)} = V_{POR(H)} - V_{hys(POR)}$. By design $V_{POR(L)}$ is always lower than $V_{POR(H)}$.
3. 32 kHz oscillator on (Min, Sec interrupt, Polarity change, Low battery and Level detection available).
4. 3.58 MHz oscillator on (device fully operational).
5. $GND < V_I < V_{DD}$. The leakage currents are generally very small, <1 nA. The value given here, 1 μA, is a maximum that can occur after an Electrostatic Stress on the pin.
6. When FSK is selected the signal power is measured between 1000 Hz and 2200 Hz. When CAS is selected signal levels are measured between 2000 and 2800Hz.
7. The IRQ pin is implemented as a 3-state pin which is only active (either HIGH or LOW) when an interrupt comes. A pull-up or pull-down has to be connected to define the line when no interrupt is generated.
8. Verified on sampling basis.
9. According to Bellcore specification: near end speech level ≤ -7 dBm ASL (ASL = Active Speech Level, referenced to 600 Ω, according to method B of recommendation P.56.
10. The input threshold voltage of SCL and SDA meet the I^2C-bus specification. Therefore, an input voltage below $0.3V_{DD}$ will be recognized as a logic 0 and an input voltage above $0.7V_{DD}$ will be recognized as a logic 1.
11. Maximum capacitive load for each bus line is 400 pF.
12. C_{1i} and C_{2i} are the total internal capacitances (including gate capacitance and leadframe capacitance).

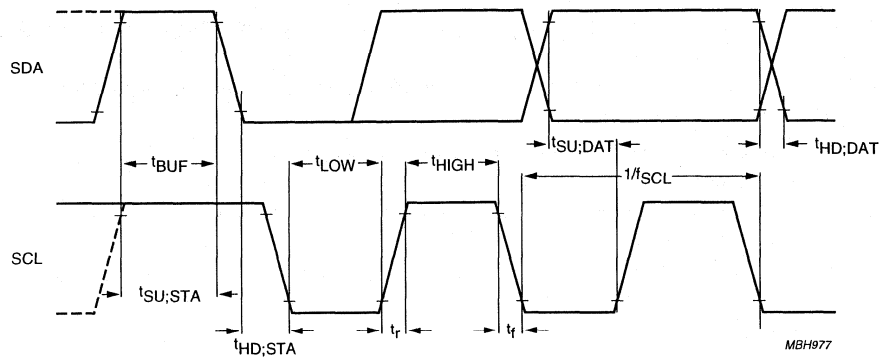


Fig.16 I²C-bus timing.

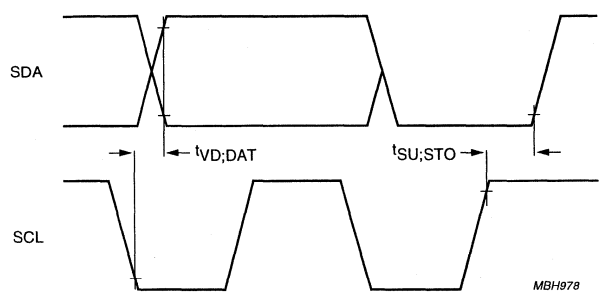
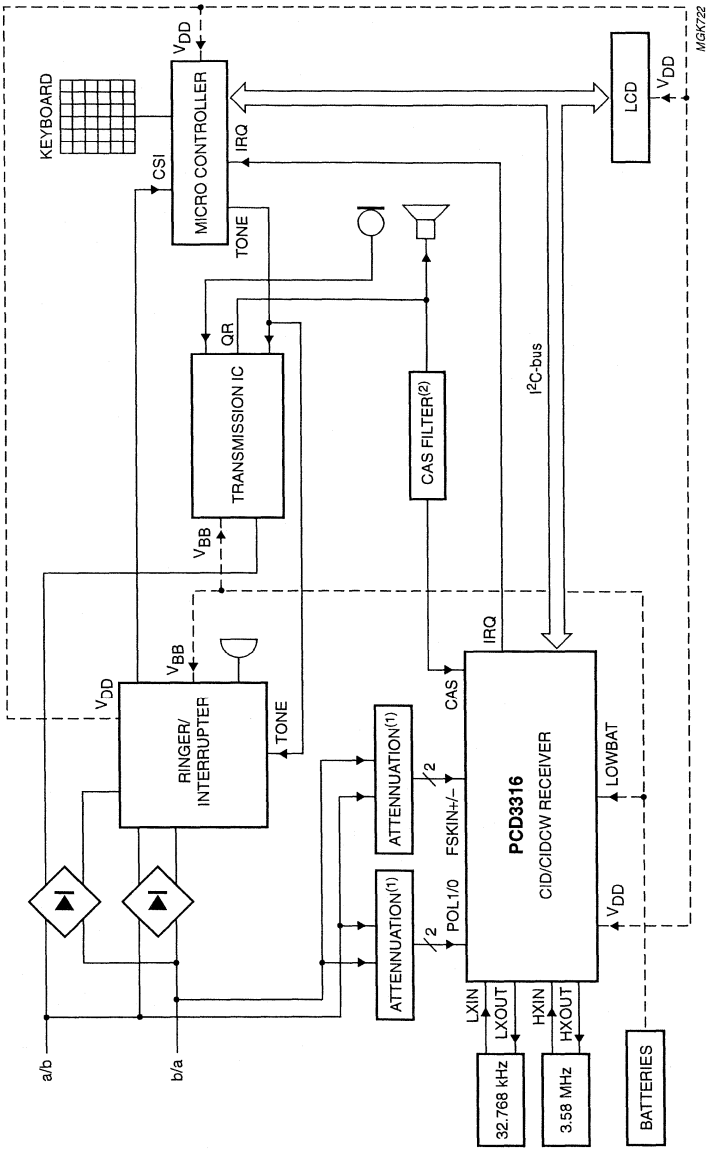


Fig.17 I²C-bus timing.

10 APPLICATION INFORMATION



A demo-board (OM5843) of this configuration is available. Please contact your Philips sales office.

(1) See Fig.19.

(2) See Fig.20.

Fig.18 Application diagram for a telephone with CID/CW functionality.

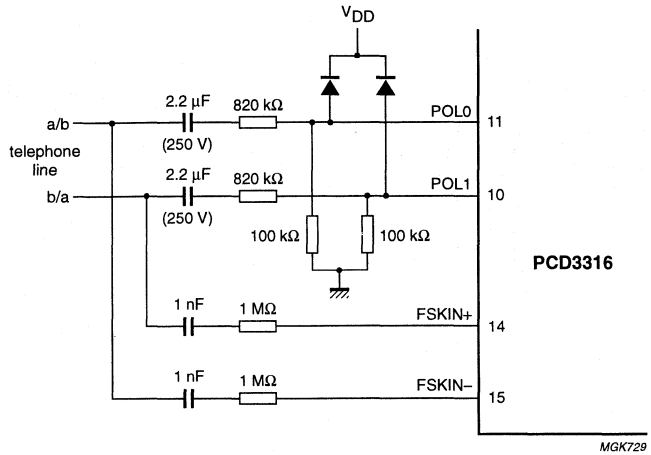


Fig.19 Attenuation networks to connect the polarity and FSK inputs to the telephone line.

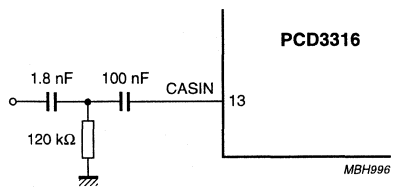


Fig.20 High-pass filter (cut-off frequency ≈ 1 kHz) to improve performance of CAS detection.

Advanced POCSAG and APOC-1 Paging Decoder

PCD5002

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Advanced POCSAG and APOC-1 Paging Decoder

PCD5002

1 FEATURES

- Wide operating supply voltage range: 1.5 to 6.0 V
- EEPROM programming requires only 2.0 V supply
- Low operating current: 50 μA typ. (ON), 25 μA typ. (OFF)
- Temperature range –25 to +70 °C
- *"CCIR radio paging Code No. 1"* (POCSAG) compatible
- Supports Advanced Pager Operator's Code Phase 1 (APOC-1) for extended battery economy
- 512, 1200 and 2400 bits/s data rates using 76.8 kHz crystal
- Built-in data filter (16-times oversampling) and bit clock recovery
- Advanced ACCESS® synchronization algorithm
- 2-bit random and (optional) 4-bit burst error correction
- Up to 6 user addresses (RICs), each with 4 functions/alert cadences
- Up to 6 user address frames, independently programmable
- Standard POCSAG sync word, plus up to 4 user programmable sync words
- Continuous data decoding upon reception of user programmable sync word (optional)
- Received data inversion (optional)
- Call alert via beeper, vibrator or LED
- 2-level acoustic alert using single external transistor
- Alert control: automatic (POCSAG type), via cadence register or alert input pin
- Separate power control of receiver and RF oscillator for battery economy
- Synthesizer set-up and control interface (3-line serial)
- On-chip EEPROM for storage of user addresses (RICs), pager configuration and synthesizer data
- On-chip SRAM buffer for message data
- Slave I²C-bus interface to microcontroller for transfer of message data, status/control and EEPROM programming (data transfer at up to 100 kbits/s)
- Wake-up interrupt for microcontroller, programmable polarity
- Direct and I²C-bus control of operating status (ON/OFF)
- Battery-low indication (external detector)
- Out-of-range condition indication
- Real time clock reference output
- On-chip voltage doubler
- Interfaces directly to UAA2080 and UAA2082 paging receivers.

2 APPLICATIONS

- Advanced display pagers (POCSAG and APOC-1)
- Basic alert-only pagers
- Information services
- Personal organizers
- Telepoint
- Telemetry/data transmission.

3 GENERAL DESCRIPTION

The PCD5002 is a very low power pager decoder and controller, capable of handling both standard POCSAG and the advanced APOC-1 code. Continuous data decoding upon reception of a dedicated sync word is available for news pager applications.

Data rates supported are 512, 1200 and 2400 bits/s using a single 76.8 kHz crystal. On-chip EEPROM is programmable using a minimum supply voltage of 2.0 V, allowing 'over-the-air' programming. I²C-bus compatible.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD5002H	LQFP32	plastic low profile quad flat package; 32 leads; body 7 × 7 × 1.4 mm	SOT358-1
PCD5002U/10	–	film-frame carrier (naked die) 32 pads	–

5 LICENSE

Supply of this IC does neither convey nor express an implied license under any patent right to use this in any APOC application.

6 BLOCK DIAGRAM

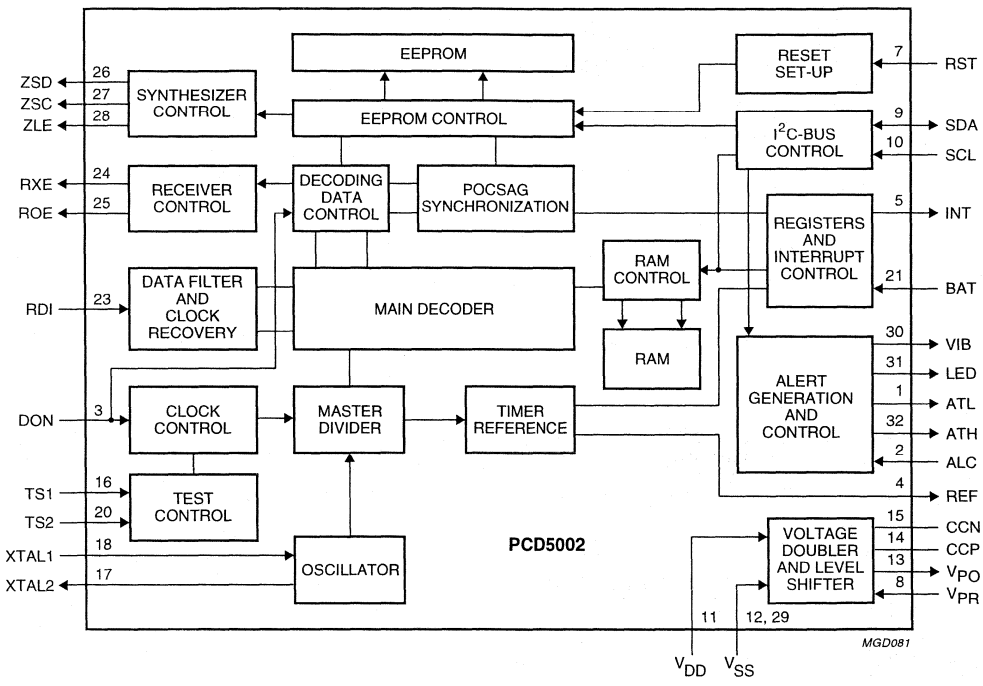


Fig.1 Block diagram.

7 PINNING

SYMBOL	PIN	DESCRIPTION
ATL	1	alert LOW level output
ALC	2	alert control input (normally LOW by internal pull-down)
DON	3	direct ON/OFF input (normally LOW by internal pull-down)
REF	4	real time clock frequency reference output
INT	5	interrupt output
n.c.	6	not connected
RST	7	reset input (normally LOW by internal pull-down)
V_{PR}	8	external positive voltage reference input
SDA	9	I²C-bus serial data input/output
SCL	10	I²C-bus serial clock input
V_{DD}	11	main positive supply voltage
V_{SS}	12	main negative supply voltage
V_{PO}	13	voltage converter positive output
CCP	14	voltage converter shunt capacitor (positive side)
CCN	15	voltage converter shunt capacitor (negative side)
TS1	16	test input 1 (normally LOW by internal pull-down)
XTAL2	17	decoder crystal oscillator output
XTAL1	18	decoder crystal oscillator input
n.c.	19	not connected
TS2	20	test input 2 (normally LOW by internal pull-down)
BAT	21	battery sense input
n.c.	22	not connected
RDI	23	received data input (POCSAG or APOC-1)
RXE	24	receiver circuit enable output
ROE	25	receiver oscillator enable output
ZSD	26	synthesizer serial data output
ZSC	27	synthesizer serial clock output
ZLE	28	synthesizer latch enable output
V_{SS}	29	main negative supply voltage
VIB	30	vibrator motor drive output
LED	31	LED drive output
ATH	32	alert HIGH level output

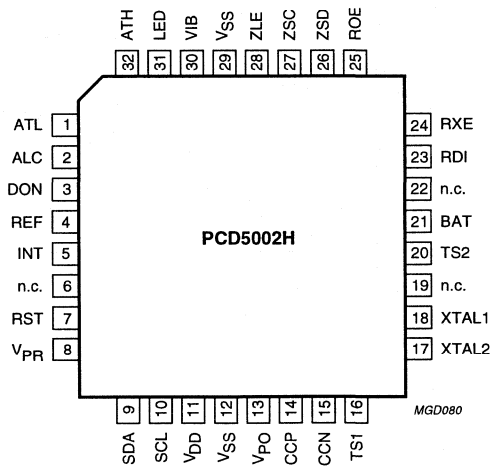


Fig.2 Pin configuration for SOT358-1 (LQFP32).

8 FUNCTIONAL DESCRIPTION

8.1 Introduction

The PCD5002 is a very low power decoder and pager controller specifically designed for use in new generation radio pagers. The architecture of the PCD5002 allows for flexible application in a wide variety of radio pager designs.

The PCD5002 is fully compatible with *"CCIR Radio paging Code No. 1"* (also known as the POCSAG code) operating at data rates of 512, 1200 and 2400 bits/s using a single oscillator crystal of 76.8 kHz.

The PCD5002 also supports the new Advanced Pager Operator's Code Phase 1 (APOC-1). This compatible extension to the POCSAG code improves battery economy by introducing 'cycles' and batch numbering. A cycle consists of 5 or 15 standard POCSAG batches. Each pager will be allocated a batch number in addition to its POCSAG address and it will only search for its address during this batch.

In addition to the standard POCSAG sync word (used also in APOC-1) the PCD5002 is also capable of recognizing up to 4 User Programmable Sync Words (UPSWs). This permits the reception of both private services and POCSAG or APOC-1 transmissions via the same radio channel. As an option reception of a UPSW may activate Continuous Data Decoding (CDD).

Used together with the Philips UAA2080 or UAA2082 paging receiver, the PCD5002 offers a highly sophisticated, miniature solution for the radio paging market. Control of an RF synthesizer circuit is also provided to ease alignment and channel selection.

On-chip EEPROM provides storage for user addresses (Receiver Identity Codes or RICs) and Special Programmed Functions (SPFs) and UPSWs, which eliminates the need for external storage devices and interconnection. For other non-volatile storage 20 bytes of general purpose EEPROM are available. The low EEPROM programming voltage makes the PCD5002 well suited for 'over-the-air' programming/reprogramming.

On request from an external controlling device or automatically (by SPF programming), the PCD5002 will provide standard POCSAG alert cadences by driving a standard acoustic 'beeper'. Non-standard alert cadences may be generated via a cadence register or a dedicated control input.

The PCD5002 can also produce a HIGH level acoustic alert as well as drive an LED indicator and a vibrator motor via external bipolar transistors.

The PCD5002 contains a low-power, high-efficiency voltage converter (doubler) designed to provide a higher voltage supply to LCD drivers or microcontrollers. In addition, an independent level shifted interface is provided allowing communication to a microcontroller operating at a higher voltage than the PCD5002.

Interface to such an external device is provided by an I^2C-bus which allows received call identity and message data, data for the programming of the internal EEPROM, alert control and pager status information to be transferred between the devices. Pager status includes features provided by the PCD5002 such as battery-low and out-of-range indications. A dedicated interrupt line minimizes the required microcontroller activity.

A selectable low frequency timing reference is provided for use in real time clock functions.

Data synchronization is achieved by the Philips patented ACCESS® algorithm ensuring that maximum advantage is made of the POCSAG code structure particularly in fading radio signal conditions. The algorithm allows for data synchronization without preamble detection whilst minimizing battery power consumption. The APOC-1 code uses an extended version of the ACCESS® synchronization algorithm.

Random (and optional) burst error correction techniques are applied to the received data to optimize the call success rate without increasing the falsing rate beyond specified POCSAG levels.

8.2 The POCSAG paging code

A transmission using the *"CCIR Radio paging Code No. 1"* (POCSAG code) is constructed in accordance with the following rules (see Fig.3).

The transmission is started by sending a **preamble**, consisting of at least 576 continuously alternating bits (10101010...). The preamble is followed by an arbitrary number of batch blocks. Only complete batches are transmitted.

Each **batch** comprises 17 codewords of 32 bits each. The first codeword is a synchronization codeword with a fixed pattern. The **sync** word is followed by 8 frames (0 to 7) of 2 codewords each, containing message information. A codeword in a frame can either be an address, message or idle codeword.

Idle codewords also have a fixed pattern and are used to fill empty frames or to separate messages.

Address codewords are identified by an MSB at logic 0 and are coded as shown in Fig.3. A user address or RIC consists of 21 bits. Only the upper 18 bits are encoded in the address codeword (bits 2 to 19). The lower 3 bits designate the frame number (0 to 7) in which the address is transmitted.

Four different call types ('numeric', 'alphanumeric' and two 'alert only' types) can be distinguished. The call type is determined by two function bits in the address codeword (bits 20 and 21), as shown in Table 1.

Alert-only calls consist only of a single address codeword. Numeric and alphanumeric calls have message codewords following the address. A message causes the frame structure to be temporarily suspended. Message codewords are sent until the message is completed, with only the sync words being transmitted in their expected positions.

Message codewords are identified by an MSB at logic 1 and are coded as shown in Fig.3. The message information is stored in a 20-bit field (bits 2 to 21).

The standard data format is determined by the call type: 4 bits per digit for numeric messages and 7 bits per (ASCII) character for alphanumeric messages.

Each codeword is protected against transmission errors by 10 CRC check bits (bits 22 to 31) and an even-parity bit (bit 32). This permits correction of a maximum of 2 random errors or up to 3 errors in a burst of 4 bits (a 4-bit burst error) per codeword.

8.3 The APOC-1 paging code

The APOC-1 paging code is fully POCSAG compatible and involves the introduction of batch grouping and a Batch Zero Identifier. This reserved address codeword indicates the start of a 'cycle' of 5 or 15 batches long and is transmitted immediately after a sync word.

Cycle transmission must be coherent i.e. a transmission starting an integer number of cycle periods after the start of the previous one.

Broadcast message data may be included in a transmission. This information may occupy any number of message codewords and immediately follows the batch zero identifier of the first cycle after preamble.
The presence of data is indicated by the function bits in the batch zero identifier: 1,1 indicates 'no broadcast data'. Any other combination indicates a broadcast message.

The PCD5002 can be configured for POCSAG or APOC-1 operation via SPF programming. The batch zero identifier is programmable and can be stored in any identifier location in EEPROM.

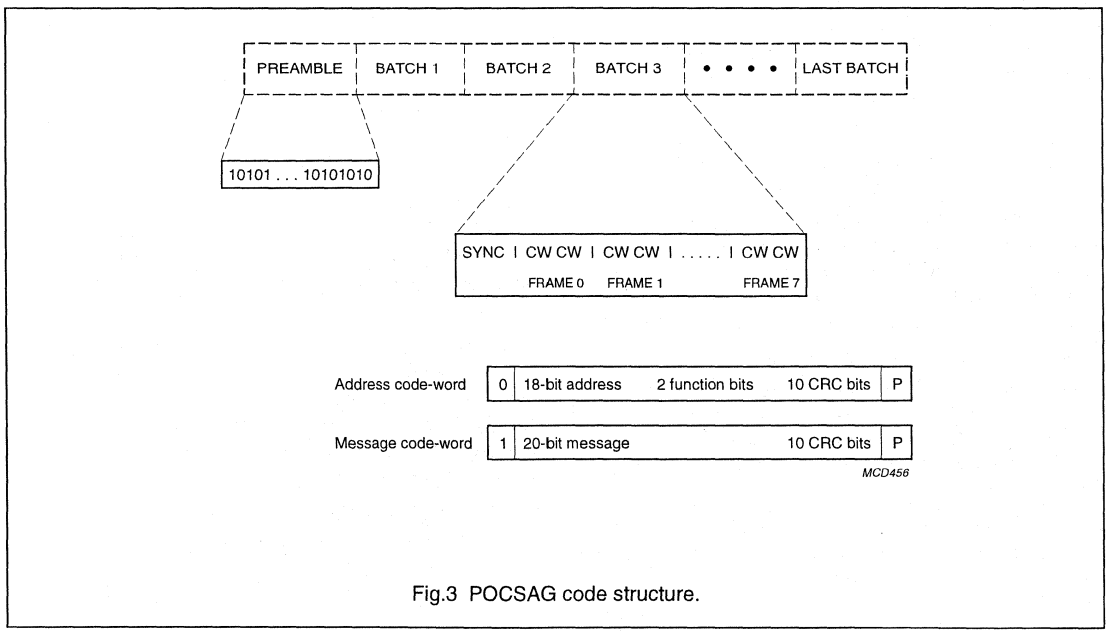


Fig.3 POCSAG code structure.

Table 1 POCSAG recommended call types and function bits

BIT 20 (MSB)	BIT 21 (LSB)	CALL TYPE	DATA FORMAT
0	0	numeric	4-bits per digit
0	1	alert only 1	–
1	0	alert only 2	–
1	1	alphanumeric	7-bits per ASCII character

The POCSAG standard only allows combinations of data formats and function code bits as given in Table 1. However, other (non-standard) combinations will be decoded normally by the PCD5002.

8.4 Error correction

In the PCD5002 error correction methods have been implemented as shown in Table 2.

Random error correction is default for both address and message codewords. In addition, burst error correction can be enabled by SPF programming. Up to 3 erroneous bits in a 4-bit burst can be corrected.

The error type detected for each codeword is identified in the message data output to the microcontroller, allowing rejection of calls with too many errors.

Table 2 Error correction

ITEM	CORRECTION
Preamble	4 random errors in 31 bits
Synchronization codeword	2 random errors in 32 bits
Address codeword	2 random errors, plus 4-bit burst errors (optional)
Message codeword	2 random errors, plus 4-bit burst errors (optional)

8.5 Operating states

The PCD5002 has 2 operating states:

- ON status
- OFF status.

The operating state is determined by a Direct Control input (DON) and bit D4 in the control register (see Table 3).

Table 3 Truth table for decoder operating status

DON INPUT	CONTROL BIT D4	OPERATING STATUS
0	0	OFF
0	1	ON
1	0	ON
1	1	ON

8.6 ON status

In the ON status the decoder pulses the receiver and oscillator enable outputs (RXE and ROE respectively) according to the code structure and the synchronization algorithm. Data received serially at the data input (RDI) is processed for call reception.

The data protocol can be POCSAG or APOC-1. Continuous data decoding upon reception of a special sync word is also supported. The data protocol is selected by SPF programming.

Reception of a valid paging call is signalled to the microcontroller by an interrupt signal. The received address and message data can then be read via the I^2C-bus interface.

8.7 OFF status

In the OFF status the decoder will neither activate the receiver or oscillator enable outputs, nor process any data at the data input. The crystal oscillator remains active to permit communication with the microcontroller.

In both operating states an accurate timing reference is available via the REF output. Using SPF programming the signal periodicity may be selected as 32.768 kHz, 50 Hz, 2 Hz or $1/60$ Hz.

8.8 Reset

The decoder can be reset by applying a positive pulse on input pin RST. For successful reset at power-on, a HIGH level must be present on the RST pin while the device is powering-up.

This can be applied by the microcontroller, or via a suitable RC power-on reset circuit connected to the RST input. Reset circuit details and conditions during and after a reset are described in Chapter 9.

8.9 Bit rates

The PCD5002 can be configured for data rates of 512, 1200 or 2400 bits/s by SPF programming. These data rates are derived from a single 76.8 kHz oscillator frequency.

8.10 Oscillator

The oscillator circuit is designed to operate at 76.8 kHz. Typically, a tuning fork crystal will be used as a frequency source. Alternatively, an external clock signal can be applied to pin XTAL1 (amplitude = V_{DD} to V_{SS}), but a slightly higher oscillator current is consumed. A 2.2 MΩ feedback resistor connected between XTAL1 and XTAL2 is required for proper operation.

To allow easy oscillator adjustment (e.g. by a variable capacitor) a 32.768 kHz reference frequency can be selected at output REF by SPF programming.

8.11 Input data processing

Data input is binary and fully asynchronous. Input bit rates of 512, 1200 and 2400 bits/s are supported. As a programmable option, the polarity of the received data can be inverted before further processing.

The input data is noise filtered by a digital filter. Data is sampled at 16 times the data rate and averaged by majority decision.

The filtered data is used to synchronize an internal clock generator by monitoring transitions. The recovered clock phase can be adjusted in steps of $1/8$ or $1/32$ bit period per received bit.

The larger step size is used when bit synchronization has not been achieved, the smaller when a valid data sequence has been detected (e.g. preamble or sync word).

8.12 Battery saving

Current consumption is reduced by switching off internal decoder sections whenever the receiver is not enabled.

To further increase battery efficiency, reception and decoding of an address codeword is stopped as soon as the uncorrected address field differs by more than 3 bits from the enabled RICs. If the next codeword must be received again, the receiver is re-enabled thus observing the programmed establishment times t_{RXE} and t_{ROE}.

The current consumption of the complete pager can be minimized by separately activating the RF oscillator circuit (using output ROE) before activating the rest of the receiver. This is possible using the UAA2082 receiver which has external biasing for the oscillator circuit.

8.13 POCSAG Synchronization strategy

In the ON status the PCD5002 synchronizes to the POCSAG data stream by the Philips ACCESS® algorithm. A flow diagram is shown in Fig.4. Where 'sync word' is used, this implies both the standard POCSAG sync word and any enabled User Programmable Sync Word (UPSW).

Several modes of operation can be distinguished depending on the synchronization state. Each mode uses a different method to obtain or retain data synchronization. The receiver and oscillator enable outputs (RXE and ROE respectively) are switched accordingly, with the appropriate establishment times (t_{RXON} and t_{ROON} respectively).

Before comparing received data with preamble, an enabled sync word or programmed user addresses, the appropriate error correction is applied.

Initially, after switching to the ON status, the decoder is in **switch-on** mode. Here the receiver will be enabled for a period up to 3 batches, testing for preamble and the sync word. Failure to detect preamble or the sync word will cause the device to switch to the 'carrier off' mode.

When preamble is detected it will cause the device to switch to the **preamble receive** mode, in which a sync word is searched for. The receiver will remain enabled while preamble is detected. When neither sync word nor preamble is found within a 1 batch duration the 'carrier off' mode is entered.

Upon detection of a sync word the **data receive** mode is entered. The receiver is activated only during enabled user address frames and sync word periods. When an enabled user address has been detected, the receiver will be kept enabled for message codeword reception until the call termination criteria are met.

During call reception data bytes are stored in an internal SRAM buffer, capable of storing 2 batches of message data.

Messages are transmitted contiguously, only interrupted by sync words at the beginning of each batch.

When a message extends beyond the end of a batch no testing for sync takes place. Instead, a message data transfer will be initiated by an interrupt to the external controller. Data reception continues normally after a period corresponding to the sync word duration.

If any message codeword is found to be uncorrectable, the 'data fail' mode is entered and no data transfer will be attempted at the next sync word position. Instead, a test for sync word will be carried out.

In the **data fail** mode message reception continues normally for 1 batch duration. When a sync word is detected at the expected position the decoder returns to the 'data receive' mode. If the sync word again fails to appear, then batch synchronization is deemed lost. Call reception is then terminated and the 'fade recovery' mode is entered.

The **fade recovery** mode is intended to scan for sync word and preamble over an extended window (nominal position ± 8 bits). This is performed for a period of up to 15 batches, allowing recovery of synchronization from long fades in the radio signal. Detection of preamble causes switching to the 'preamble receive' mode, while sync word detection causes switching to the 'data receive' mode. When neither is found within a period of 15 batches, the radio signal is considered lost and the 'carrier off' mode is entered.

The purpose of the **carrier off** mode is to detect a valid radio transmission and synchronize to it quickly and efficiently. Because transmissions may start at random, the decoder enables the receiver for 1 codeword in every 18 codewords looking for preamble or sync word.
By using a buffer containing 32 bits (n bits from the current scan, 32 –n from the previous scan) effectively every batch bit position can be tested within a continuous transmission of at least 18 batches. Detection of preamble causes the device to switch to the 'preamble receive' mode, while sync word detection causes the device to switch to the 'data receive' mode.

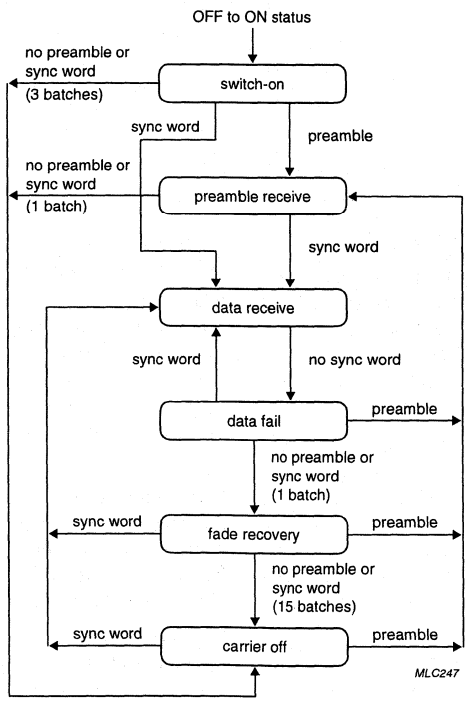


Fig.4 ACCESS® synchronization algorithm for POCSAG.

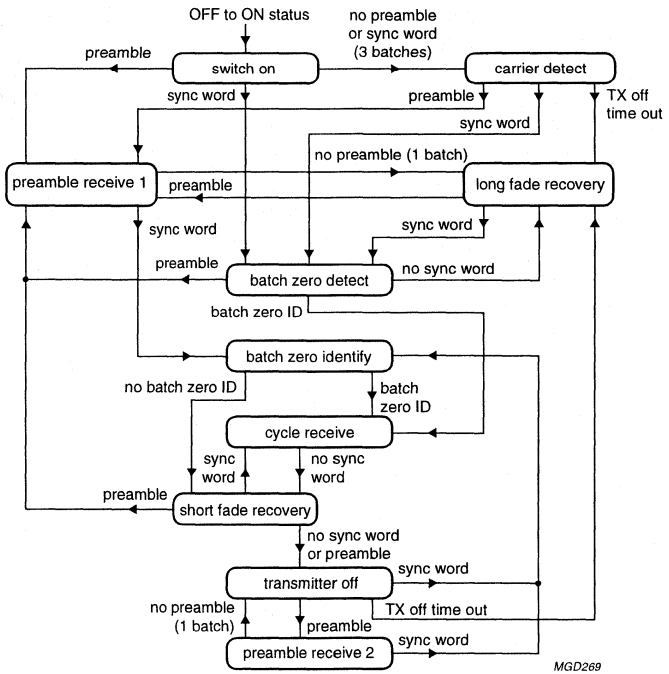


Fig.5 APOC-1 synchronization algorithm.

8.14 APOC-1 synchronization strategy

The synchronization strategy in APOC-1 is an extended version of the ACCESS® scheme and is illustrated in Fig.5. The PCD5002 counts the number of batches in a transmission, starting from the first batch received after preamble. Counter overflow occurs due to the size of a cycle, as determined by SPF programming.

Initially, after switching to the ON status, the decoder will be in the **switch-on** mode. Here the receiver will be enabled for up to 3 batches, testing for preamble and sync word. Detection of preamble causes the device to switch to the 'preamble receive' mode, while any enabled sync word enters the 'batch zero detect' mode. Failure to detect either will cause the device to switch to the 'carrier detect' mode.

In the **preamble receive 1** mode the PCD5002 searches for a sync word, the receiver remaining enabled while preamble is detected. As soon as an enabled sync word is found the 'batch zero identify' mode is started.

If preamble is not found within one batch duration then the 'long fade recovery' mode is entered.

When in **batch zero detect** mode the PCD5002 switches on every batch to maintain synchronization and check for the batch zero identifier. Detection of the batch zero identifier activates the 'cycle receive' mode. When synchronization is lost the 'long fade recovery' mode is entered. 'preamble receive' mode is entered when preamble is detected.

In the **batch zero identify** mode the first codeword immediately after the sync word of the first batch is compared with the programmed batch zero identifier. Failure to detect the batch zero identifier will cause the device to enter the 'short fade recovery' mode.

When this comparison is successful the function bits determine whether any broadcast message will follow. Any function bit combination other than '1,1' will cause the PCD5002 to accept message codewords until terminated by a valid address codeword.

After reception of any broadcast message data the PCD5002 continues to operate in the 'cycle receive' mode.

In the **cycle receive** mode the PCD5002 enables call reception in only one programmed batch per cycle. Sync word detection takes place from 2 bits before to 2 bits after the expected sync word position of this batch. If the sync word is not detected then the position of the current sync word will be maintained and the 'short fade recovery' mode will be entered.

When a valid sync word is found user address codeword detection takes place, as in normal POCSAG code. Any following message codewords are received normally. If a message extends into a subsequent batch containing a batch zero identifier, then the batch zero identifier is detected normally and message reception will continue.

Data reception is suspended after the programmed batch until the same batch position in the next cycle. The exception being when a received call continues into the next batch.

In the **short fade recovery** mode the programmed data receive batch will continue to be checked for user address codewords. In addition the first codeword after the programmed batch is checked for sync word or preamble.

When a valid sync word is detected the 'cycle receive' mode is re-entered, while detection of preamble causes the device to switch to the 'preamble receive' mode. When neither is found then the 'transmitter off' mode is entered.

In the **transmitter off** mode a time-out is set to a pre-programmed duration. This time-out corresponds to the maximum time between subsequent transmissions (preamble to preamble).

The PCD5002 then checks the first batch of every cycle for sync word or preamble. The programmed data receive batch is ignored (unless it is batch 0).

Table 4 Synchronization window tolerance as a function of bit rate

TIME FROM LOSS OF SIGNAL	TOLERANCE		
	512 (bits/s)	1200 (bits/s)	2400 (bits/s)
≤ 30 s	4 bits	4 bits	4 bits
≤ 60 s	4 bits	4 bits	8 bits
≤ 120 s	4 bits	8 bits	16 bits
≤ 240 s	8 bits	16 bits	32 bits

Synchronization checking is performed over a window ranging from 'n' bits before to 'n' bits after the expected sync word position. The window tolerance 'n' depends on the time since the 'transmitter off' mode was entered and on the selected bit rate (see Table 4).

When a sync word is detected in this widened synchronization window the PCD5002 enters the 'batch zero identify' mode. Time-out expiry before a sync word has been detected causes the device to switch to the 'long fade recovery' mode.

Detection of preamble in the 'transmitter off' mode initiates the **preamble receive 2** mode. Operation in this mode is identical to 'preamble receive mode. Failure to detect preamble for one batch period will cause the device to switch back to the 'transmitter off' mode. This prevents inadvertent loss of cycle synchronization due to spurious signals resembling preamble.

The **carrier detect** mode is identical to the 'carrier off' mode in standard POCSAG operation. Upon first entry the transmitter off time-out is started. The receiver is enabled to receive one codeword in every 18 codewords to check for sync word and preamble. This check is performed on the last available 32 bits for every received bit.

The 'preamble receive' mode is entered if preamble is detected. If a valid sync word is found the 'batch zero detect' mode is entered. If neither has been detected and the time-out expires, then the 'long fade recovery' mode is entered.

The **long fade recovery** mode is intended to quickly regain synchronization in fading conditions (not caused by the transmitter switching off between transmissions) or when having been out of range, while maintaining acceptable battery economy.

Initially, the receiver is switched off until one cycle duration after the last enabling in the 'transmitter off' mode. The receiver is then enabled for a 2 codeword period in which each contiguous group of 32 bits is tested for **any decodable** POCSAG codeword (including sync word) and preamble. Single-bit error correction is applied.

If a codeword is detected, the receiver enable period is extended by another codeword duration and the above test is repeated. This process continues while valid codewords are received.

Detection of preamble will cause the device to switch to the 'preamble receive' mode, while sync word detection will cause the device to switch to the 'batch zero detect' mode. When neither is detected during the 2 codeword window or any following 32-bit group, the receiver will be disabled.

If valid codewords are detected but no sync word or preamble is detected over a period of 18 codewords, the receiver is also disabled.

Data sampling, as previously described, is repeated one cycle duration after the moment the receiver was last activated.

8.15 Call termination

Call reception is terminated:

- Upon reception of any address codeword (including Idle codeword but excluding the batch zero identifier in APOC-1 operation) requiring no more than single bit error correction
- In 'data fail' mode, when a sync word is not detected at the expected batch position
- When a forced call termination command is received from an external controller.

The last method permits an external controller to stop call reception, depending on the number and type of errors which occurred in a call. After a forced call termination the decoder will enter the 'data fail' mode.

The type of error correction as well as the call termination conditions are indicated by status bits in the message data output.

Following call termination, transfer of the data received since the previous sync word period is initiated by an interrupt to the external controller.

8.16 Call data output format

POCSAG call information is stored in the decoder SRAM in blocks of 3 bytes per codeword. Each stored call consists of a call header, followed by message data blocks and a call terminator. In the event of concatenated messages the call terminator is replaced with the call header of the next message. An alert-only call only has a call header and a call terminator.

The formats of a call header, a message data block and a call terminator are shown in Tables 5, 7 and 9.

A **Call Header** contains information on the last sync word received, the RIC which began call reception and the type of error correction performed on the address codeword.

A **Message Data** block contains the data bits from a message codeword plus the type of error correction performed. No deformatting is performed on the data bits: numeric data appear as 4-bit groups per digit, alphanumeric data has a 7-bit ASCII representation.

The **Call Terminator** contains information on the last sync word received, information on the way the call was terminated (forced call termination command, loss of sync word in 'data fail' mode) and the type of error correction performed on the terminating codeword.

8.17 Error type indication

Table 11 shows how the different types of detected errors are encoded in the call data output format.

A message codeword containing more than a single bit error (bit E3 = 1) may appear as an address codeword (bit M1 = 0) after error correction. In this event the codeword is processed as message data and does not cause call termination.

8.18 Data transfer

Data transfer is initiated either during sync word periods or as soon as the receiver is disabled after call termination. If the SRAM buffer is full, data transfer is initiated immediately during the next codeword.

When the PCD5002 is ready to transfer received call data an external interrupt will be generated via output INT. Any message data can be read by accessing the RAM output register via the I^2C-bus interface. Bytes will be output starting from the position indicated by the RAM read pointer.

Table 5 Call header format

BYTE NUMBER	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
1	0	S3	S2	S1	R3	R2	R1	DF
2	0	S3	S2	S1	R3	R2	R1	0
3	X	X	F0	F1	E3	E2	E1	0

Table 6 Call header bit identification

BITS (MSB to LSB)	IDENTIFICATION
S3 to S1	identifier number of sync word for current batch (7 = standard POCSAG)
R3 to R1	identifier number of user address (RIC)
DF	data fail mode indication (1 = data fail mode); note 1
F0 and F1	function bits of received address codeword (bits 20 and 21)
E3 to E1	detected error type; see Table 11; E3 = 0 in a concatenated call header

Note

1. The DF bit in the call header is set:
   a) When the sync word of the batch in which the (beginning of the) call was received, did not match the standard POCSAG or a user-programmed sync word. The sync word identifier (bits S3 to S1) will then be made 0.
   b) When any codeword of a previous call received in the same batch was uncorrectable.

Table 7 Message data format

BYTE NUMBER	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
1	M2	M3	M4	M5	M6	M7	M8	M9
2	M10	M11	M12	M13	M14	M15	M16	M17
3	M18	M19	M20	M21	E3	E2	E1	M1

Table 8 Message data bit identification

BITS (MSB to LSB)	IDENTIFICATION
M2 to M21	message codeword data bits
E3 to E1	detected error type; see Table 11
M1	message codeword flag

Table 9 Call terminator format

BYTE NUMBER	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
1	FT	S3	S2	S1	0	0	0	DF
2	FT	S3	S2	S1	0	0	0	X
3	X	X	X	X	E3	E2	E1	0

Table 10 Call terminator bit identification

BITS (MSB to LSB)	IDENTIFICATION
FT	forced call termination (1 = yes)
S3 to S1	identifier number of last sync word
DF	data fail mode indication (1 = data fail mode); note 1
F0 and F1	function bits of received address codeword (bits 20 and 21)
E3 to E1	detected error type; see Table 11; E3 = 0 in a call terminator

Note

1. The DF bit in the call terminator is set:
   a) When any call data codeword in the terminating batch was uncorrectable, while in 'data receive' mode.
   b) When the sync word at the start of the terminating batch did not match the standard POCSAG or a user-programmed sync word, while in 'data fail' mode.

Table 11 Error type identification (note 1)

E3	E2	E1	ERROR TYPE	NUMBER OF ERRORS
0	0	0	no errors - correct codeword	0
0	0	1	parity bit in error	1
0	1	0	single bit error	1 + parity
0	1	1	single bit error and parity error	1
1	0	0	not used	–
1	0	1	4-bit burst error and parity error	3 (e.g.1101)
1	1	0	2-bit random error	2
1	1	1	uncorrectable codeword	3 or more

Note

1. POCSAG code allows a maximum of 3 bit errors to be detected per codeword.

Successful call termination occurs on reception of a valid address codeword with less than 2 bit errors.
Unsuccessful termination occurs when a sync word is not detected while in the 'data fail' mode.

It is generally possible to distinguish these two conditions using the sync word identifier number (bits S3 to S1); the identifier number will be non-zero for correct termination, and zero for sync word failure.

Only when a call is received in the 'data fail' mode and the call is terminated before the end of the batch, is it not possible to distinguish unsuccessful from successful termination.

Reception of message data can be terminated at any time by transmitting a forced call termination command to the status register via the I^2C-bus. Any call received will then be terminated immediately and the 'data fail' mode will be entered.

8.19 Continuous data decoding

Apart from transmissions in the POCSAG or APOC-1 format, the PCD5002 is also capable of decoding continuous transmissions with the same codeword structure. Any user-programmable sync word (UPSW) may be designated to enable continuous data decoding.

When a Continuous Data Decoding (CDD) sync word is detected at any sync word position, the receiver remains enabled from then on. Status bits D1 and D0 show the CDD mode to be active.

All codewords are decoded and their data fields are stored in SRAM. The usual error information is appended. No distinction is made between address and message codewords: codeword bit 0 is treated as a data bit and is stored in bit M1 of the 3-byte output format.

Codewords received at the expected sync word positions (POCSAG batch size) are matched against standard POCSAG sync word, all enabled UPSWs and preamble.

Data output to an external controller is initiated by an interrupt at the next sync word position, after reception of 16 codewords.

The call header preceding the data has a different structure from normal POCSAG or APOC-1 data. The data header format is shown in Table 12.

Continuous data decoding continues until one of the following conditions occur:

- The decoder is switched to the OFF state
- A Forced Call Termination (FCT) command is received via the I²C-bus
- Preamble is detected at the sync word position
- Standard POCSAG sync word or an enabled non-CDD sync word is detected.

Only a forced call termination command will be indicated in the SRAM data by a call terminator. In the other events continuous data decoding will stop without notification.

Upon forced termination the 'fade recovery' mode is entered. Detection of preamble causes the device to switch to the 'preamble receive' mode. Detection of a standard sync word or any enabled non-continuous UPSW will cause the device to switch to the 'data receive' mode.

Continuous data decoding will continue in the next batch if any enabled CDD sync word is detected or no enabled sync word is detected.

8.20 Receiver and oscillator control

A paging receiver and an RF oscillator circuit can be controlled independently via enable outputs RXE and ROE respectively. Their operating periods are optimized according to the synchronization mode of the decoder. Each enable signal has its own programmable establishment time (see Table 14).

8.21 External receiver control and monitoring

An external controller may enable the receiver control outputs continuously via an I²C-bus command, overruling the normal enable pattern. Data reception continues normally. This mode can be exited by means of a reset or an I²C-bus command.

External monitoring of the receiver control output RXE is possible via bit D6 in the status register, when enabled via the control register (D2 = 1). Each change of state of output RXE will generate an external interrupt at output INT.

Table 12 Continuous data header format

BYTE NUMBER	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
1	0	X	X	X	C3	C2	C1	0
2	0	C3	C2	C1	C3	C2	C1	0
3	X	X	F0	F1	E3	E2	E1	0

Table 13 Data header bit identification

BITS (MSB to LSB)	IDENTIFICATION
C3 to C1	identifier number of continuous data decoding sync word
F0 and F1	function bits of received address codeword (bits 20 and 21)
E3 to E1	detected error type (see Table 11); E3 = 0 in a concatenated call header

8.22 Battery condition input

A logic signal from an external sense circuit, signalling battery condition, can be applied to the BAT input. This input is sampled each time the receiver is disabled (RXE ↓ 0).

When enabled via the control register (D2 = 0), the condition of input BAT is reflected in bit D6 of the status register. Each change of state of bit D6 causes an external interrupt at output INT.

When using the UAA2080 pager receiver a battery-low condition corresponds to a logic HIGH level. With a different sense circuit the reverse polarity can be used as well, because every change of state is signalled to an external controller.

After a reset the initial condition of the battery-low indicator in the status register is zero.

Table 14 Receiver and oscillator establishment times (note 1)

CONTROL OUTPUT	ESTABLISHMENT TIME				UNIT
RXE	5	10	15	30	ms
ROE	20	30	40	50	ms

Note

1. The exact values may differ slightly from the above values, depending on the bit rate (see Table 25).

8.23 Synthesizer control

Control of an external frequency synthesizer is possible via a dedicated 3-line serial interface (outputs ZSD, ZSC and ZLE). This interface is common to a number of available synthesizers. The synthesizer is enabled using the oscillator enable output ROE.

The frequency parameters must be programmed in EEPROM. Two blocks of maximum 24 bits each can be stored. Any unused bits must be programmed at the beginning of a block: only the last bits are used by the synthesizer.

When the function is selected by SPF programming (SPF byte 01, bit D6), data is transferred to the synthesizer each time the PCD5002 is switched from the OFF to the ON status. Transfer takes place serially in two blocks, starting with bit 0 (MSB) of block 1 (see Table 28).

Data bits on ZSD change on the falling edges of ZSC. After clocking all bits into the synthesizer, a latch enable pulse copies the data to the internal divider registers. A timing diagram is illustrated in Fig.6.

The data output timing is synchronous, but has a pause in the bitstream of each block. This pause occurs in the 13th bit while ZSC is LOW. The nominal pause duration t_p depends on the programmed bit rate for data reception and is shown in Table 15. The total duration of the 13th bit is given by $t_{ZCL} + t_p$.

A similar pause occurs between the first and the second data block. The delay between the first latch enable pulse and the second data block is given by $t_{ZDL2} + t_p$.
The complete start-up timing of the synthesizer interface is illustrated in Fig.13.

Table 15 Synthesizer programming pause

BIT RATE (bit/s)	t_p (clocks)	t_p (μs)
512	119	1549
1200	33	430
2400	1	13

8.24 Serial microcontroller interface

The PCD5002 has an I²C-bus serial microcontroller interface capable of operating at 400 kbits/s.
The PCD5002 is a slave transceiver with a 7-bit I²C-bus address 39 (bits A6 to A0 = 0100111).

Data transmission requires 2 lines: SDA (data) and SCL (clock), each with an external pull-up resistor. The clock signal (SCL) for any data transmission must be generated by the external controlling device.

A transmission is initiated by a START condition (S: SCL = 1, SDA = ↓) and terminated by a STOP condition (P: SCL = 1, SDA = ↑).

Data bits must be stable when SCL is HIGH. If there are multiple transmissions, the STOP condition can be replaced with a new START condition.

Data is transferred on a byte basis, starting with a device address and a read/write indicator. Each transmitted byte must be followed by an acknowledge bit A (active LOW). If a receiving device is not ready to accept the next complete byte, it can force a bus wait state by holding SCL LOW.

The general I²C-bus transmission format is illustrated in Fig.7. Formats for master/slave communication are illustrated in Fig.8.

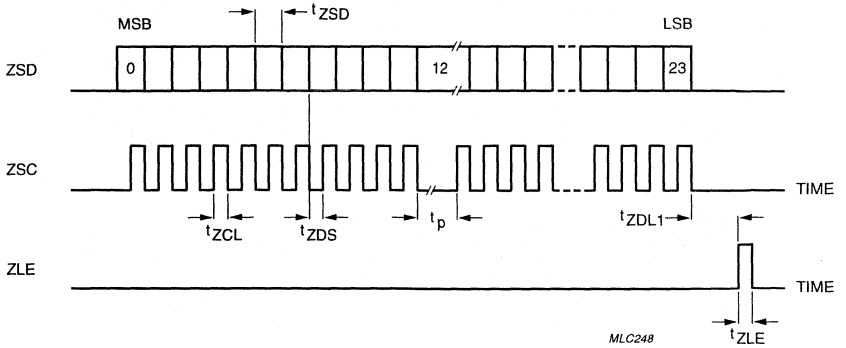


Fig.6 Synthesizer interface timing.

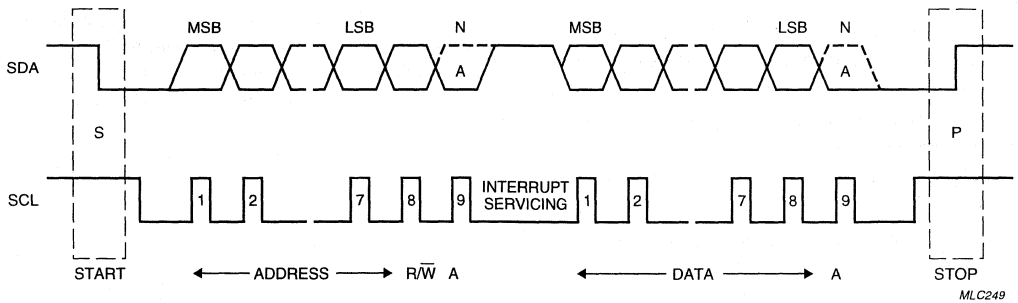
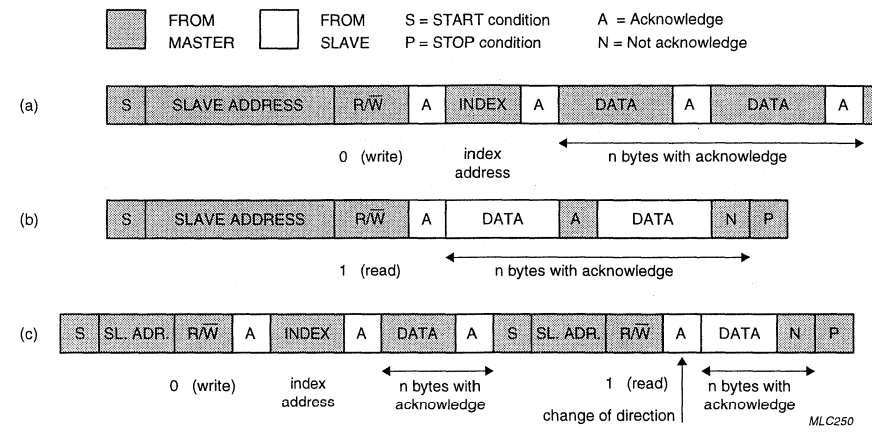


Fig.7 I²C-bus message format.



(a) Master writes to slave.
(b) Master reads from slave.
(c) Combined format (shown: write plus read).

Fig.8 Message types.

8.25 Decoder I²C-bus access

All internal access to the PCD5002 takes place via the I²C-bus interface. For this purpose the internal registers, SRAM and EEPROM have been memory mapped and are accessed via an **index register**. Table 16 shows the index addresses of all internal blocks.

Registers are addressed directly, while RAM and EEPROM are addressed indirectly via address pointers and I/O registers.

Remark: The EEPROM memory map is non-contiguous and is organized as a matrix.
The EEPROM address pointer contains both row and column indicators.

Data written to read-only bits will be ignored. Values read from write-only bits are undefined and must be ignored.

Each I²C-bus write message to the PCD5002 must start with its slave address, followed by the index address of the memory element to be accessed. An I²C-bus read message uses the last written index address as a data source. The different I²C-bus message types are shown in Fig.8.

As a slave the PCD5002 cannot initiate bus transfers by itself. To prevent an external controller from having to monitor the operating status of the decoder, all important events generate an external interrupt on output INT.

Table 16 Index register

ADDRESS(1)	REGISTER FUNCTION	ACCESS
00H	status	R
00H	control	W
01H	real time clock: seconds	R/$\overline{W}$
02H	real time clock: $^1/_{100}$ second	R/$\overline{W}$
03H	alert cadence	W
04H	alert set-up	W
05H	periodic interrupt modulus	W
05H	periodic interrupt counter	R
06H	RAM write address pointer	R
07H	EEPROM address pointer	R/$\overline{W}$
08H	RAM read address pointer	R/$\overline{W}$
09H	RAM data output	R
0AH	EEPROM data input/output	R/$\overline{W}$
0BH to 0FH	unused	note 2

Notes

1. The index register only uses the least significant nibble, the upper 4 bits are ignored.
2. Writing to registers 0B to 0F has no effect, reading produces meaningless data.

8.26 External interrupt

The PCD5002 can signal events to an external controller via an interrupt signal at output INT. The interrupt polarity is programmable via SPF programming. The interrupt source is shown in the status register.

Interrupts are generated by the following events (more than one event is possible):

- Call data available for output (bit D2)
- SRAM pointers becoming equal (bit D3)
- Expiry of periodic time-out (bit D7)
- Expiry of alert time-out (bit D4)
- Change of state in out-of-range indicator (bit D5)
- Change of state in battery-low indicator or in receiver control output RXE (bit D6).

Immediate interrupts are generated by status bits D3, D4, D6 (RXE monitoring) and D7. Bits D2, D5 and D6 (BAT monitoring) generate interrupts as soon as the receiver is disabled (RXE = 0).

When call data is available (D2 = 1) but the receiver remains switched on, an interrupt is generated at the next sync word position.

The interrupt output INT is reset after completion of a status read operation.

8.27 Status/Control register

The status/control register consists of two independent registers, one for reading (status) and one for writing (control).

The status register shows the current operating condition of the decoder and the cause(s) of an external interrupt. The control register activates/deactivates certain functions. Tables 17 and 18 show the bit allocations of both registers.

All status bits will be reset after a status read operation except for the out-of-range, battery-low and receiver enable indicator bits (see note 1 to Table 17).

Table 17 Status register (00H; read)

BIT[1]	VALUE	DESCRIPTION
D1 and D0	0 0	no new call data
	0 1	new call received (POCSAG or APOC-1)
	1 0	continuous decoding data available
	1 1	batch zero data available (APOC-1)
D3 and D2	0 0	no data to be read (default after reset)
	0 1	RAM read/write pointers different; data to be read
	1 0	RAM read/write pointers equal; no more data to read
	1 1	RAM buffer full or overflow
D4	1	alert time-out expired
D5	1	out-of-range
D6	1	BAT input HIGH or RXE output active (selected by control bit D2)
D7	1	periodic timer interrupt

Note

1. After a status read operation bits D3, D4 and D7 are always reset, bits D1 and D0 only when no second call is pending. D2 is reset when the RAM is empty (read and write pointers equal).

Table 18 Control register (00H; write)

BIT (MSB: D7)	VALUE	DESCRIPTION
D0	1	forced call termination (automatically reset after termination)
D1	1	EEPROM programming enable
D2	0	BAT input selected for monitoring (status bit D6)
	1	RXE output selected for monitoring (status bit D6)
D3	1	receiver continuously enabled (RXE = 1, ROE = 1)
D4	0	decoder in OFF status (while DON = 0)
	1	decoder in ON status
D5 to D7	X	not used: ignored when written

8.28 Pending interrupts

A secondary status register is used for storing status bits of pending interrupts. This occurs:

- When a new call is received while the previous one was not yet acknowledged by reading the status register
- When an interrupt occurs during a status read operation.

After completion of the status read the primary register is loaded with the contents of the secondary register, which is then reset. An immediate interrupt is then generated, output INT becoming active 1 decoder clock cycle after it was reset following the status read.

Remark: In the event of multiple pending calls, only the status bits of the last call are retained.

8.29 Out-of-range indication

The out-of-range condition occurs when entering the 'fade recovery' or 'carrier off' mode in POCSAG, or 'transmitter off' or 'carrier detect' mode in APOC-1. This condition is reflected in bit D5 of the status register. The out-of-range condition is reset when either preamble or a valid sync word is detected.

The out-of-range bit (D5) in the status register is updated each time the receiver is disabled (RXE $\downarrow$ 0). Every change of state in bit D5 generates an interrupt.

8.30 Real time clock

The PCD5002 provides a periodic reference pulse at output REF. The frequency of this signal can be selected by SPF programming:

- 32768 Hz
- 50 Hz (square-wave)
- 2 Hz
- $1/60$ Hz.

The 32768 Hz signal does not have a fixed period, it consists of 32 pulses distributed over 75 main oscillator cycles at 76.8 kHz. The timing is illustrated in Fig.15.

When programmed for $1/60$ Hz (1 pulse per minute) the pulse at output REF is held off while the receiver is enabled.

Except for the 50 Hz frequency the pulse width t_{RFP} is equal to one decoder clock period.

The real time clock counter runs continuously irrespective of the operating condition of the PCD5002. It contains a **seconds register** (maximum 59) and a **$1/100$ second register** (maximum 99), which can be read from or written to via the I^2C-bus. The bit allocation of both registers is shown in Tables 19 and 20.

Table 19 Real time clock; seconds register (01H; read/write)

BIT (MSB D7)	VALUE	DESCRIPTION
D0	–	1 s
D1	–	2 s
D2	–	4 s
D3	–	8 s
D4	–	16 s
D5	–	32 s
D6	X	not used: ignored when written, undetermined when read
D7	X	not used: ignored when written, undetermined when read

Table 20 Real time clock; $1/100$ second register (02H; read/write)

BIT (MSB D7)	VALUE	DESCRIPTION
D0	–	0 01 s
D1	–	0.02 s
D2	–	0.04 s
D3	–	0.08 s
D4	–	0.16 s
D5	–	0.32 s
D6	–	0.64 s
D7	X	not used: ignored when written, undetermined when read

8.31 Periodic interrupt

A periodic interrupt can be realised with the periodic interrupt counter. This 8-bit counter is incremented every $1/100$ s and produces an interrupt when it reaches the value stored in the periodic interrupt modulus register.
The counter register is then reset and counting continues.

Operation is started by writing a non-zero value to the modulus register. Writing a zero will stop interrupt generation immediately and will halt the periodic interrupt counter after 2.55 s.

The modulus register is write-only, the counter register is read only. Both registers have the same index address (05H).

8.32 Received call delay

Call reception (detection of an enabled RIC) causes both the periodic interrupt modulus and the counter register to be reset.

Since the periodic interrupt counter runs for another 2.55 s after a reset, the received call delay (in $1/100$ s units) can be determined by reading the counter register.

Table 21 Alert set-up register (04H; write)

BIT (MSB D7)	VALUE	DESCRIPTION
D0	0	call alert via cadence register
	1	POCSAG call alert (pattern selected by D7 and D6)
D1	0	LOW level acoustic alert (ATL), pulsed vibrator alert (25 Hz)
	1	HIGH level acoustic alert (ATL + ATH), continuous vibrator alert
D2	0	normal alerts (acoustic and LED)
	1	warbled alerts: 16 Hz (LED: on/off, ATL/ATH: alternate f_{AWH}, f_{AWL})
D3	1	acoustic alerts enable (ATL, ATH)
D4	1	vibrator alert enabled (VIB)
D5	1	LED alert enabled (LED)
D7 and D6[1]	0 0	POCSAG alert pattern FC = 00, see Fig.9 (a)
	0 1	POCSAG alert pattern FC = 01, see Fig.9 (b)
	1 0	POCSAG alert pattern FC = 10, see Fig.9 (c)
	1 1	POCSAG alert pattern FC = 11, see Fig.9 (d)

Note

1. Bits D7 and D6 correspond to function bits 20 and 21 respectively in the address codeword, which designate the POCSAG call type as shown in Table 1.

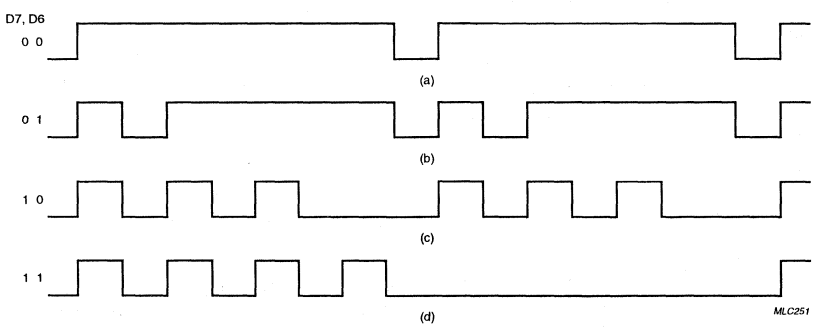


Fig.9 POCSAG alert patterns.

8.33 Alert generation

The PCD5002 is capable of controlling 3 different alert transducers, acoustic beeper (HIGH and LOW level), LED and vibrator motor. The associated outputs are ATH/ATL, LED and VIB respectively. ATL is an open-drain output capable of directly driving an acoustic alerter via a resistor. The other outputs require external transistors.

Each alert output can be individually enabled via the alert set-up register. Alert level and warble can be separately selected. The alert pattern can either be standard POCSAG or determined via the alert cadence register. Direct alert control is possible via input ALC.

The alert set-up register is shown in Table 21.

Standard POCSAG alerts can be selected by setting bit D0 in the alert set-up register, bits D6 and D7 determining the alert pattern used.

8.34 Alert cadence register (03H; write)

When not programmed for POCSAG alerts (alert set-up register bit D0 = 0), the 8-bit alert cadence register determines the alert pattern. Each bit represents a 62.5 ms time slot, a logic 1 activating the enabled alert transducers. The bit pattern is rotated with the MSB (bit D7) being output first and the LSB (bit D0) last.

When the last time slot (bit D0) is initiated an interrupt is generated to allow loading of a new pattern. When the pattern is not changed it will be repeated. Writing a zero to the alert cadence register will halt alert generation within 62.5 ms.

8.35 Acoustic alert

Acoustic alerts are generated via outputs ATL and ATH. For LOW level alerts only ATL is active, while for HIGH level alerts ATH is also active. ATL is driven in counter phase with ATH.

The alert level is controlled by bit D1 in the alert set-up register.

When D1 is reset, for standard POCSAG alerts (D0 = 1) a LOW level acoustic alert is generated during the first 4 s (ATL), followed by 12 s at HIGH level (ATL + ATH). When D1 is set, the full 16 s are at HIGH level. An interrupt is generated after the full alert time has elapsed (indicated by bit D4 in the status register).

When using the alert cadence register, D1 would normally be updated by external control when the alert time-out interrupt occurs at the start of the 8th cadence time slot. Since D1 acts immediately on the alert level, it is advisable to reset the last bit of the previous pattern to prevent unwanted audible level changes.

8.36 Vibrator alert

The vibrator output (VIB) is activated continuously during a standard POCSAG alert or whenever the alert cadence register is non-zero.

Two alert levels are supported, LOW level (25 Hz square-wave) and HIGH level (continuous). The vibrator level is controlled by bit D1 in the alert set-up register.

8.37 LED alert

The LED output pattern corresponds either to the selected POCSAG alert or to the contents of the alert cadence register. No equivalent exists for HIGH/LOW level alerts.

8.38 Warbled alert

When enabled, by setting bit D2 in the alert set-up register, the signals on outputs ATL, ATH and LED are warbled with a 16 Hz modulation frequency. Output LED is switched on and off at the modulation rate, while outputs ATL and ATH switch between f_{AWH} and f_{AWL} alerter frequencies.

8.39 Direct alert control

A direct alert control input (ALC) is available for generating user alarm signals (e.g. battery-low warning). A HIGH level on input ALC activates all enabled alert outputs, overruling any ongoing alert patterns.

8.40 Alert priority

Generation of a standard POCSAG alert (D0 = 1) overrides any alert pattern in the alert cadence register. After completion of the standard alert, the original cadence is restarted from its last position. The alert set-up register will now contain the settings for the standard alert.

The highest priority has been assigned to the alert control input (ALC). All enabled alert outputs will be activated while ALC is set. Outputs are activated/deactivated in synchrony with the decoder clock. Activation requires an extra delay of 1 clock when no alerts are being generated.

When input ALC is reset, acoustic alerting does not cease until the current output frequency cycle has been completed.

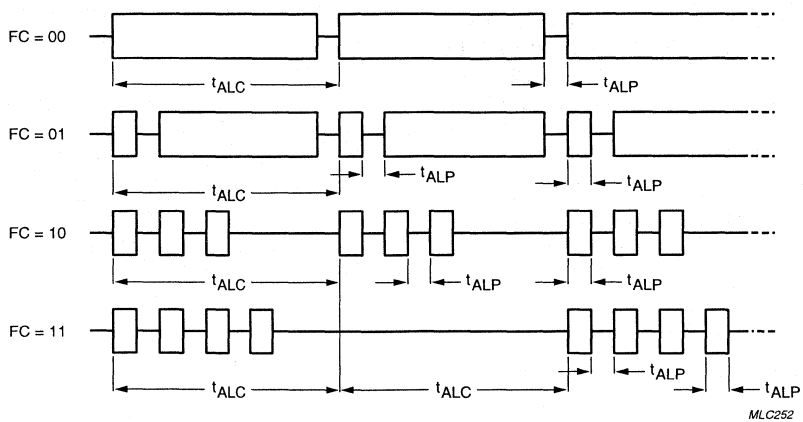


Fig.10 POCSAG alert timing.

8.41 Cancelling alerts

Standard POCSAG alerts (manual or automatic) are cancelled by resetting bit D0 in the alert set-up register. User defined alerts are cancelled by writing a zero to the alert cadence register. Any ongoing alert is cancelled when a reset pulse is applied to input RST.

8.42 Automatic POCSAG alerts

Standard alert patterns have been defined for each POCSAG call type, as indicated by the function bits in the address codeword (see Table 1). The timing of these alert patterns is shown in Fig.10. After completion of the full 16 s alert period an interrupt is generated by status bit D4.

When enabled by SPF programming (SPF byte 03, bit D2) standard POCSAG alerts will be automatically generated at outputs ATL, ATH, LED and VIB upon call reception. The alert pattern matches the call type as indicated by the function bits in the received address codeword.

The original settings of the alert set-up register will be lost. Bit D0 is reset after completion of the alert.

8.43 SRAM access

The on-chip SRAM can hold up to 96 bytes of call data. Each call consists of a call header (3 bytes), message data blocks (3 bytes per codeword) and a call terminator (3 bytes).

The RAM is filled by the decoder and can be read via the I^2C-bus interface. The RAM is accessed indirectly by a read address pointer and a data output register. A write address pointer indicates the position of the last message byte stored.

Status register bit D2 is set when the read and write pointers are different. It is reset only when the SRAM pointers become equal during reading, i.e. when the RAM becomes empty.

Status bit D3 is set when the read and write pointers become equal. This can be due to a RAM empty or a RAM full condition. It is reset after a status read operation.

Interrupts are generated as follows:

- When status bit D2 is set and the receiver is disabled (RXE = 0); data is available for reading
- Immediately when status bit D3 is set: RAM is either empty (status bit D2 = 0) or full (status bit D2 = 1).

To avoid loss of data due to RAM overflow at least 3 bytes of data must be read during reception of the codeword following the 'RAM full' interrupt.

8.44 RAM write address pointer (06H; read)

The RAM write address pointer is automatically incremented during call reception, because the decoder writes each data byte to RAM. The RAM write address pointer can only be read. Values range from 00H to 5FH. Bit D7 (MSB) is not used and its value is undefined when read. When a call data byte is written to location 5FH, the write address pointer wraps around to 00H. This does not necessarily imply a RAM full condition.

8.45 RAM read address pointer (08H; read/write)

The RAM read address pointer is automatically incremented after reading a data byte via the RAM output register.

The RAM read address pointer can be accessed for reading and writing.

The values range from 00H to 5FH. When at 5FH a read operation will cause wrapping around to 00H. Bit D7 (MSB) is not used; it is ignored when written to and undefined when read from.

8.46 RAM data output register (09H; read)

The RAM data output register contains the byte addressed by the RAM read address pointer and can only be read. Each read operation causes an increment of the RAM read address pointer.

8.47 EEPROM access

The EEPROM is intended for storage of user addresses (RICs), sync words and special programmed function (SPF) bits representing the decoder configuration.

The EEPROM can store 48 bytes of information and is organized as a matrix of 8 rows by 6 columns.
The EEPROM is accessed indirectly via an address pointer and a data I/O register.

The EEPROM is protected against inadvertent writing by means of the programming enable bit in the control register (bit D1).

The EEPROM memory map is non-contiguous. Figure 11 shows both the EEPROM organization and the access method.

Identifier locations contain RICs or sync words. A total of 20 unassigned bytes are available for general purpose storage.

8.48 EEPROM address pointer (07H; read/write)

An EEPROM location is addressed via the EEPROM address pointer. It is incremented automatically each time a byte is read from or written to via the EEPROM data I/O register.

The EEPROM address pointer contains two counters for the row and the column number. Bits D2 to D0 contain the column number (0 to 5) and bits D5 to D3 the row number (0 to 7). Bits D7 and D6 of the address pointer are not used. Data written to these bits will be ignored, while their values are undefined when read.

The column and row counters are connected in series. Upon overflow of the column counter (column = 5) the row counter is automatically incremented and the column counter wraps to 0. On overflow the row counter wraps from 7 to 0.

8.49 EEPROM data I/O register (0AH; read/write)

The byte addressed by the EEPROM address pointer can be written to or read from via the EEPROM data I/O register. Each access automatically increments the EEPROM address pointer.

8.50 EEPROM access limitations

Since the EEPROM address pointer is used during data decoding, the EEPROM may not be accessed while the receiver is active (RXE = 1). It is advisable to switch to the OFF state before accessing the EEPROM.

The EEPROM cannot be written to unless the EEPROM programming enable bit (bit D1) in the control register is set.

For writing a minimum programmed supply voltage (V_{PG}) is required (2.0 V typ.). The programmed supply current (I_{PG}) required during writing is approximately 500 μA.

8.51 EEPROM read operation

EEPROM read operations must start at a valid address in the non-contiguous memory map. Single byte or block reads are permitted.

8.52 EEPROM write operation

EEPROM write operations must always take place in blocks of 6 bytes, starting at the beginning of a row. Programming a single byte will reset the other bytes in the same row. Modifying a single byte in a row requires re-writing the unchanged bytes with their old contents.

After writing each block a pause of 7.5 ms (max.) is required to complete the internal programming operation. During this time the external microcontroller may generate an I²C-bus STOP condition. If another I²C-bus transfer is initiated the decoder will pull SCL LOW during this pause.

After writing the EEPROM programming enable bit (D1) in, the control register must be reset.

8.53 Invalid write address

When an invalid write address is used, the column counter bits (D2 to D0) are forced to zero before being loaded into the address pointer. The row counter bits are used normally.

8.54 Incomplete programming sequence

A programming sequence may be aborted by an I²C-bus STOP condition. The EEPROM programming enable bit (D1) in the control register must then be reset.

Any bytes received from the last 6-byte block will be ignored and the contents of this (incomplete) EEPROM block will remain unchanged.

8.55 Unused EEPROM locations

A total of 20 EEPROM bytes are available for general purpose storage (see Table 22).

Table 22 Unused EEPROM addresses

ROW	HEX
0	04 and 05(1)
5	28 to 2D
6	30 to 35
7	38 to 3D

Note

1. When using bytes 04H and 05H, care must be taken to preserve the SPF information stored in bytes 00H to 03H.

8.56 Special programmed function allocation

The SPF bit allocation in the EEPROM is shown in Tables 23 to 27. The SPF bits are located in row 0 of the EEPROM and occupy 4 bytes.

Bytes 04H and 05H are not used and are available for general purpose storage.

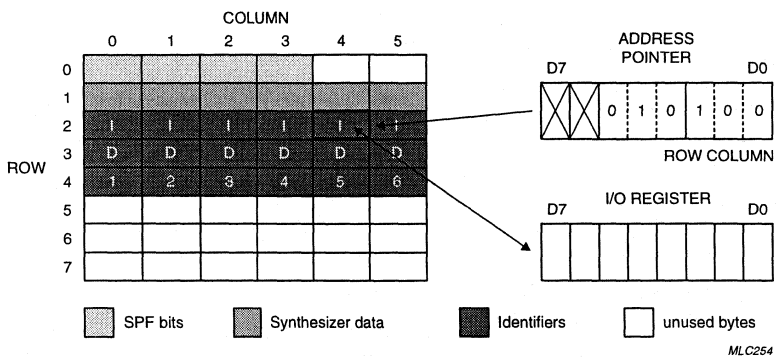


Fig.11 EEPROM organization and access.

Table 23 Special programmed functions (EEPROM address 00H)

BIT (MSB: D7)	VALUE	DESCRIPTION
D0	0	POCSAG decoding enabled
	1	APOC-1 decoding enabled
D1	0	cycle length: 5 batches
	1	cycle length: 15 batches
D5 to D2 (MSB: D5)	0 to 4	batch number (D1 = 0, MSB is ignored)
	0 to 14	batch number (D1 = 1)
D6	1	continuous data decoding enabled
D7	1	received data inversion enabled

Table 24 Special programmed functions (EEPROM address 01H)

BIT (MSB: D7)	VALUE	DESCRIPTION
D1 and D0	0 0	5 ms receiver establishment time (nominal); note 1
	0 1	10 ms
	1 0	15 ms
	1 1	30 ms
D3 and D2	0 0	20 ms oscillator establishment time (nominal); note 1
	0 1	30 ms
	1 0	40 ms
	1 1	50 ms
D5 and D4	0 0	512 bits/s received bit rate
	0 1	1024 bits/s (not used in POCSAG)
	1 0	1200 bits/s
	1 1	2400 bits/s
D6	1	synthesizer interface enabled (programming at switch-on)
D7	1	voltage converter enabled

Note

1. Since the exact establishment time is related to the programmed bit rate, Table 25 shows the values for the various bit rates.

Table 25 Establishment time as a function of bit rate

NOMINAL ESTABLISHMENT TIME	ACTUAL ESTABLISHMENT TIME			
	512 (bits/s)	1024 (bits/s)	1200 (bits/s)	2400 (bits/s)
5 ms	5.9 ms (3 bits)	5.9 ms (6 bits)	5 ms (6 bits)	5 ms (12 bits)
10 ms	11.7 ms (6 bits)	11.7 ms (12 bits)	10 ms (12 bits)	10 ms (24 bits)
15 ms	15.6 ms (8 bits)	15.6 ms (16 bits)	16.7 ms (20 bits)	16.7 ms (40 bits)
20 ms	23.4 ms (12 bits)	23.4 ms (24 bits)	20 ms (24 bits)	20 ms (48 bits)
30 ms	31.2 ms (16 bits)	31.2 ms (32 bits)	26.7 ms (32 bits)	26.7 ms (64 bits)
40 ms	39.1 ms (20 bits)	39.1 ms (40 bits)	40 ms (48 bits)	40 ms (96 bits)
50 ms	46.9 ms (24 bits)	46.9 ms (48 bits)	53.3 ms (64 bits)	53.3 ms (128 bits)

Table 26 Special programmed functions (EEPROM address 02H)

BIT (MSB: D7)	VALUE	DESCRIPTION
D0	X	not used
D1	X	not used
D3 and D2	0 0	32768 Hz real time clock reference
	0 1	50 Hz square wave
	1 0	2 Hz
	1 1	$^1/_{60}$ Hz
D4	1	signal test mode enabled (REF and INT outputs)
D5	0	burst error correction enabled
D7 and D6	00	30 s (+ 0.5 s max.) transmitter off time-out
	01	60 s (+ 1 s max.)
	10	120 s (+ 2 s max.)
	11	240 s (+ 4 s max.)

Table 27 Special programmed functions (EEPROM address 03H)

BIT (MSB: D7)	VALUE	DESCRIPTION
D1 and D0	0 0	2048 Hz acoustic alerter frequency
	0 1	2731 Hz
	1 0	4096 Hz
	1 1	3200 Hz
D2	1	automatic POCSAG alert generation enabled
D3	X	not used
D4	X	not used
D5	X	not used
D6	0	INT output polarity: active LOW
	1	INT output polarity: active HIGH
D7	X	not used

8.57 Synthesizer programming data

Data for programming a PLL synthesizer via pins ZSD, ZSC and ZLE can be stored in row 1 of the EEPROM. Six bytes are available starting with address 08H.

Data is transferred in two serial blocks of 24 bits each, starting with bit 0 (MSB) of block 1. Any unused bits must be programmed at the beginning of a block.

Table 28 Synthesizer programming data (EEPROM address 08H to 0DH)

ADDRESS (HEX)	BIT (MSB: D7)	DESCRIPTION
08	D7 to D0	bits 0 to 7 of data block 1 (bit 0 is MSB)
09	D7 to D0	bits 8 to 15
0A	D7 to D0	bits 16 to 23
0B	D7 to D0	bits 0 to 7 of data block 2 (bit 0 is MSB)
0C	D7 to D0	bits 8 to 15
0D	D7 to D0	bits 16 to 23

8.58 Identifier storage allocation

Up to 6 different identifiers can be stored in EEPROM for matching with incoming data. The PCD5002 can distinguish two types of identifiers:

- User addresses (RIC)
- User Programmable Sync Words (UPSW)
- Batch zero identifiers
- Continuous data decoding (CDD) sync words.

Identifiers are stored in EEPROM rows 2, 3 and 4. Each identifier location consists of 3 bytes in the same column. The identifier number is equal to the column number + 1.

Each identifier can be individually enabled. The standard POCSAG sync word is always enabled and has identifier number 7.

The identifier type is determined by bits D2 and D0 of identifier byte 3, as shown in Table 31.

Identifiers 1 and 2 always represent RICs or batch zero identifiers. The last 4 identifiers (numbers 3 to 6) can represent any identifier type.

A UPSW represents an unused address and must differ by more than 6 bits from preamble to guarantee detection.

A batch zero identifier marks the start of a new cycle in the APOC-1 protocol. It is only recognized when APOC-1 decoding has been enabled (SPF byte 00, bit D0).

Reception of a CDD sync word initiates continuous data decoding. CDD sync words are only recognized when continuous data decoding has been enabled (SPF byte 00, bit 6).

Table 29 shows the memory locations of the 6 identifiers. The bit allocation per identifier is given in Table 30.

Table 29 Identifier storage allocation (EEPROM address 10H to 25H)

ADDRESS (HEX)	BYTE	DESCRIPTION
10 to 15	1	identifier number 1 to 6
18 to 1D	2	identifier number 1 to 6
20 to 25	3	identifier number 1 to 6

Table 30 Identifier bit allocation

BYTE	BIT (MSB: D7)	DESCRIPTION
1	D7 to D0	bits 2 to 9 of POCSAG codeword (RIC or UPSW); notes 1 and 2
2	D7 to D0	bits 10 to 17
3	D7 and D6	bits 18 and 19
	D5	frame number bit FR3 (RIC); note 3
	D4	frame number bit FR2 (RIC)
	D3	frame number bit FR1 (RIC)
	D2	identifier type selection (0 = UPSW, 1 = RIC); note 4
	D1	identifier enable (1 = enabled)
	D0	batch zero ID/continuous decoding (1 = enabled)

Notes

1. The bit numbering corresponds with the numbering in a POCSAG codeword; bit 1 is the flag bit (0 = address, 1 = message).
2. A UPSW needs 18 bits to be matched for successful identification. Bit 1 (MSB) must be logic 0. Bits 2 to 19 contain the identifier bit pattern, they are followed by 2 predetermined random (function) bits and the UPSW is completed by 10 CRC error correction bits and an even-parity bit.
3. Bits FR3 to FR1 (MSB: FR3) contain the 3 least significant bits of the 21-bit RIC.
4. Identifiers 1 and 2 (RIC only) will be disabled by programming bit D2 as logic 0.

Table 31 Identifier types

BYTE 3, BIT D2	BYTE 3, BIT D0	DESCRIPTION
0	0	user programmable sync word (UPSW)
0	1	continuous data decoding (CDD) sync word
1	0	normal user address (RIC)
1	1	batch zero identifier

8.59 Voltage doubler

An on-chip voltage doubler provides an unregulated DC output for supplying an LCD or a low power microcontroller at output V_{PO}. An external ceramic capacitor of 100 nF (typ.) is required between pins CCN and CCP. The voltage doubler is enabled via SPF programming.

8.60 Level-shifted interface

All interface lines are suited for communication with a microcontroller operating from a higher supply voltage. The external device must have a common reference at V_{SS} of the PCD5002.

The reference voltage for the level-shifted interface must be applied to input V_{PR}. If required this could be the on-chip voltage doubler output V_{PO}. When the microcontroller has a separate (regulated) supply it should be connected to V_{PR}.

The level-shifted interface lines are RST, DON, ALC, REF and INT.

The I^2C-bus interface lines SDA and SCL can be level-shifted independently of V_{PR} by the standard external pull-up resistors.

8.61 Signal test mode

A special 'signal test' mode is available for monitoring the performance of a receiver circuit together with the front-end of the PCD5002.

For this purpose the output of the digital noise filter and the recovered bit clock are made available at outputs REF and INT respectively. All synchronization and decoding functions are normally active.

The 'signal test' mode is activated/deactivated by SPF programming.

9 OPERATING INSTRUCTIONS

9.1 Reset conditions

When the PCD5002 is reset by applying a HIGH level to input RST, the condition of the decoder is as follows:

- OFF status (irrespective of DON input level)
- REF output frequency 32768 Hz
- All internal counters reset
- Status/control register reset
- INT output at LOW level
- No alert transducers selected
- LED, VIB and ATH outputs at LOW level
- ATL output high-impedance
- SDA and SCL inputs high-impedance
- Voltage converter disabled.

The programmed functions are activated within t_{RSU} after release of the reset condition (RST LOW). The settings affecting the external operation of the PCD5002 are as follows:

- REF output frequency
- Voltage converter
- INT output polarity
- Signal test mode.

When input DON is HIGH, the decoder starts operating in ON status immediately following t_{RSU}.

9.2 Power-on reset circuit

During power-up of the PCD5002 a HIGH level of minimum duration t_{RST} = 50 µs must be applied to pin RST. This is to prevent EEPROM corruption which might otherwise occur because of the undefined contents of the Control register.

The reset signal can be applied by the external microcontroller or by an RC power-on reset circuit on pin RST (C to V_{PR}, R to V_{SS}). Such an RC-circuit should have a time constant of at least $3t_{RST}$ = 150 µs.

Input RST has an internal high-ohmic pull-down resistor (nominal 2 MΩ at 2.5 V supply) which could be used together with a suitable external capacitor connected to V_{PR} to create a power-on reset signal. However, since this pull-down resistor varies considerably with processing and supply voltage, the resulting time constant is inaccurate.

A more accurate reset duration can be realised with an additional external resistor connected to V_{SS}. Recommended minimum values in this case are C = 2.2 nF and R = 100 kΩ (see Fig.16).

9.3 Reset timing

The start-up time for the crystal oscillator may exceed 1 s (typ. 800 ms). It is advisable to apply a reset condition, at least during the first part of this period. The minimum reset pulse duration t_{RST} is 50 µs.

During reset the oscillator is active, but clock signals are inhibited internally. Once the reset condition is released the end of the oscillator start-up period can be detected by a rising edge on output INT.

During a reset the voltage converter clock (V_{clk}) is held at zero. The resulting output voltage drop may cause problems when the external resetting device is powered by the internal voltage doubler. A sufficiently large buffer capacitor connected between output V_{PO} and V_{SS} must be provided to supply the microcontroller during reset. The voltage at V_{PO} will not drop below V_{DD} – 0.7 V.

Immediately after a reset all programmable internal functions will start operating according to a programmed value of 0. During the first 8 full clock cycles (t_{RSU}) all programmed values are loaded from EEPROM.

After reset the receiver outputs RXE and ROE become active immediately, if DON is HIGH and the synthesizer is disabled. When the synthesizer is enabled, RXE and ROE will only become active after the second pulse on ZLE completes the loading of synthesizer data.

The full reset timing is illustrated in Fig.12. The start-up timing including synthesizer programming is illustrated in Fig.13.

9.4 Initial programming

A newly-delivered PCD5002 has EEPROM contents which are undefined. The EEPROM should therefore be programmed, followed by a reset to activate the SPF settings, before any attempt is made to use the device.

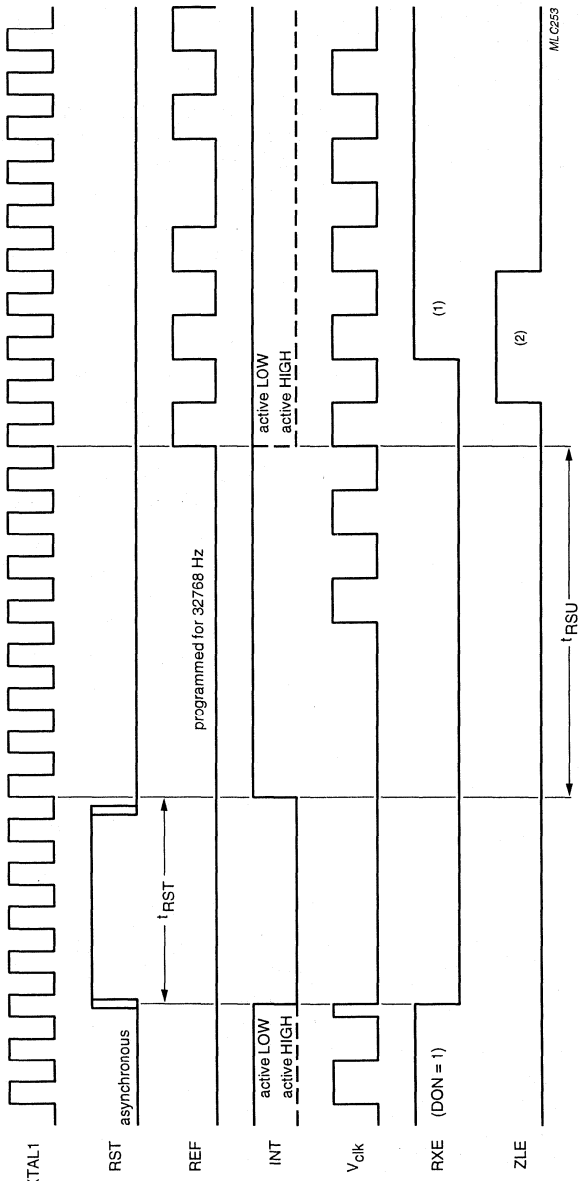


Fig.12 Reset timing.

(1) The RXE output signal is shown for disabled synthesizer. When the synthesizer is enabled RXE is held off until after the second pulse on ZLE (programming complete).

(2) The ZLE output signal is shown for enabled synthesizer and DON = 1. When DON = 0 output ZLE remains HIGH until ON state is entered (DON = 1 or control register bit D4 = 1).

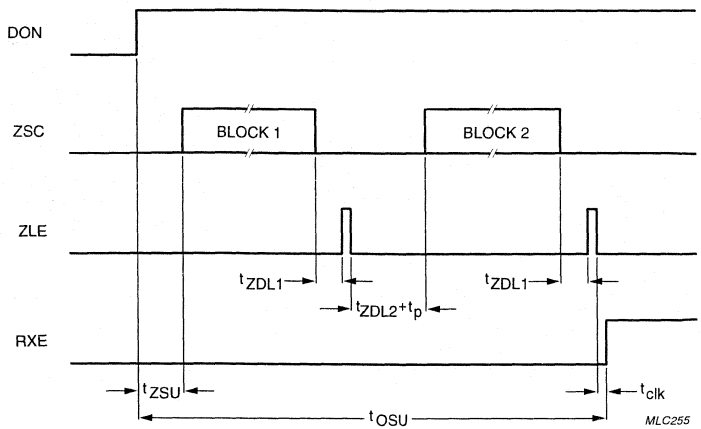


Fig.13 Start-up timing including synthesizer programming.

10 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		−0.5	+7.0	V
V_{PR}	external reference voltage input	$V_{PR} \geq V_{DD} - 0.8$ V	−0.5	+7.0	V
V_n	voltage on pins ALC, DON, RST, SDA and SCL	$V_n \leq 7.0$ V	$V_{SS} - 0.8$	$V_{PR} + 0.8$	V
V_{n1}	input voltage on any other pin	$V_{n1} \leq 7.0$ V	$V_{SS} - 0.8$	$V_{DD} + 0.8$	V
P_{tot}	total power dissipation		–	250	mW
P_O	power dissipation per output		–	100	mW
T_{amb}	operating ambient temperature		−25	+70	°C
T_{stg}	storage temperature		−55	+125	°C

11 DC CHARACTERISTICS

V_{DD} = 2.7 V; V_{PR} = 2.7 V; V_{SS} = 0 V; T_{amb} = −25 to +70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage	voltage converter disabled	1.5	2.7	6.0	V
V_{PR}	external reference voltage input	$V_{PR} \geq V_{DD} - 0.8$ V	1.5	2.7	6.0	V
I_{DD0}	supply current (OFF)	note 1	–	25.0	40.0	µA
I_{DD1}	supply current (ON)	note 1; DON = V_{DD}	–	50.0	80.0	µA
V_{PG}	programming supply voltage	voltage converter disabled	2.0	–	6.0	V
		voltage converter enabled	2.0	–	3.0	V
I_{PG}	programming supply current		–	–	800	µA
Inputs						
V_{IL}	LOW level input voltage					
	RDI, BAT		V_{SS}	–	$0.3V_{DD}$	V
	DON, ALC, RST		V_{SS}	–	$0.3V_{PR}$	V
	SDA, SCL		V_{SS}	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage					
	RDI, BAT		$0.7V_{DD}$	–	V_{DD}	V
	DON, ALC, RST		$0.7V_{PR}$	–	V_{PR}	V
	SDA, SCL		$0.7V_{DD}$	–	V_{PR}	V
I_{IL}	LOW level input current pins RDI, BAT,TS1, TS2, DON, ALC and RST	T_{amb} = 25 °C; $V_I = V_{SS}$	0	–	−0.5	µA
I_{IH}	HIGH level input current	T_{amb} = 25 °C				
	TS1, TS2	$V_I = V_{DD}$	6	–	20	µA
	RDI, BAT	$V_I = V_{DD}$; RXE = 0	6	–	20	µA
	RDI, BAT	$V_I = V_{DD}$; RXE = 1	0	–	0.5	µA
	DON, ALC, RST	$V_I = V_{PR}$	250	500	850	nA
Outputs						
I_{OL}	LOW level output current	T_{amb} = 25 °C				
	VIB, LED	V_{OL} = 0.3 V	80	–	–	µA
	ATH	V_{OL} = 0.3 V	250	–	–	µA
	INT, REF	V_{OL} = 0.3 V	80	–	–	µA
	ZSD, ZSC, ZLE	V_{OL} = 0.3 V	70	–	–	µA
	ATL	V_{OL} = 1.2 V; note 2	13	27	55	mA
	ROE, RXE	V_{OL} = 0.3 V	80	–	–	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{OH}	HIGH level output current	T_{amb} = 25 °C				
	VIB, LED	V_{OH} = 0.7 V	−0.6	–	−2.4	mA
	ATH	V_{OH} = 0.7 V	−3.0	–	−11.0	mA
	INT, REF	V_{OH} = 2.4 V	−80	–	–	µA
	ZSD, ZSC, ZLE	V_{OH} = 2.4 V	−60	–	–	µA
	ATL	ATL high-impedance; note 3	–	–	−0.5	µA
	ROE, RXE	V_{OH} = 2.4 V	−600	–	–	µA

Notes

1. Inputs: SDA and SCL pulled up to V_{DD}; all other inputs connected to V_{SS}.
   Outputs: RXE and ROE logic 0; REF: f_{ref} = 1/60 Hz; all other outputs open-circuit.
   Oscillator: no crystal; external clock f_{osc} = 76800 Hz; amplitude: V_{SS} to V_{DD}.
   Voltage convertor disabled (SPF byte 01, bit D7 = 0; see Table 24).
2. Maximum output current is subject to absolute maximum ratings per output (see Chapter 10).
3. When ATL (open drain output) is not activated it is high impedance.

12 DC CHARACTERISTICS (WITH VOLTAGE CONVERTER)

V_{DD} = 2.7 V; V_{SS} = 0 V; V_{PR} = V_{PO}; T_{amb} = −25 to +70 °C; C_s = 100 nF; voltage converter enabled.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		1.5	–	3.0	V
$V_{PO(0)}$	output voltage; no load	V_{DD} = 2.7; I_{PO} = 0	–	5.4	–	V
V_{PO}	output voltage	V_{DD} = 2 V; I_{PO} = −250 µA	3.0	3.5	–	V
I_{PO}	output current	V_{DD} = 2 V; V_{PO} = 2.7 V	−400	−650	–	µA
		V_{DD} = 3 V; V_{PO} = 4.5 V	−650	−900	–	µA

13 OSCILLATOR CHARACTERISTICS

Quartz crystal type: MX-1V or equivalent.
Quartz crystal parameters: f = 76 800 Hz; $R_{S(max)}$ = 35 kΩ; C_L = 8 pF; C_0 = 1.4 pF; C_1 = 1.5 fF.
Maximum overall tolerance: $\pm 200 \times 10^{-6}$ (includes: cutting, temperature, aging) for POCSAG, $\pm 55 \times 10^{-6}$ for APOC-1 ('transmitter off' mode).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{XO}	output capacitance XTAL2		–	10	–	pF
g_m	oscillator transconductance	V_{DD} = 1.5 V	6	12	–	µS

14 AC CHARACTERISTICS

V_{DD} = 2.7 V; V_{SS} = 0 V; V_{PR} = 2.7 V; T_{amb} = 25 °C;. f_{osc} = 76800 Hz.

SYMBOLS	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
System clock						
T_{clk}	system clock period	f_{osc} = 76800 Hz	–	13.02	–	µs
Call alert frequencies						
f_{AL}	alert frequency	SPF byte 03H; bits:				
		D1, D0 = 0 0	–	2048	–	Hz
		D1, D0 = 0 1	–	2731	–	Hz
		D1, D0 = 1 0	–	3200	–	Hz
		D1, D0 = 1 1	–	4096	–	Hz
f_{AW}	warbled alert; modulation frequency	alert set-up bit D2 = 1; outputs ATL, ATH and LED	–	16	–	Hz
f_{AWH}	warbled alert; high acoustic alert frequency	alert set-up bit D2 = 1; outputs ATL and ATH	–	f_{AL}	–	Hz
f_{AWL}	warbled alert; low acoustic alert frequency	alert set-up bit D2 = 1; outputs ATL and ATH	–	$\frac{1}{2}f_{AL}$	–	Hz
f_{VBP}	pulsed vibrator frequency (square wave)	low-level alert	–	25	–	Hz
Call alert duration						
t_{ALT}	alert time-out period		–	16	–	s
t_{ALL}	ATL output time-out period	low-level alert	–	4	–	s
t_{ALH}	ATH output time-out period	high-level alert	–	12	–	s
t_{VBL}	VIB output time-out period	low-level alert	–	4	–	s
t_{VBH}	VIB output time-out period	high-level alert	–	12	–	s
t_{ALC}	alert cycle period		–	1	–	s
t_{ALP}	alert pulse duration		–	125	–	ms
Real time clock reference						
f_{ref}	real time clock reference frequency	SPF byte 02H; bits:				
		D3, D2 = 0 0; note 1	–	32768	–	Hz
		D3, D2 = 0 1; note 2	–	50	–	Hz
		D3, D2 = 1 0	–	2	–	Hz
		D3, D2 = 1 1	–	$\frac{1}{60}$	–	Hz
t_{RFP}	real time clock reference pulse duration	all reference frequencies except 50 Hz (square wave)	–	13.02	–	µs

SYMBOLS	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Receiver control						
t_{RXT}	RXE and ROE transition time	C_L = 5 pF	–	100	–	ns
t_{RXON}	RXE establishment time (nominal values: actual duration is bit rate dependent, see Table 25)	SPF byte 01H; bits:				
		D1, D0 = 0 0	–	5	–	ms
		D1, D0 = 0 1	–	10	–	ms
		D1, D0 = 1 0	–	15	–	ms
		D1, D0 = 1 1	–	30	–	ms
t_{ROON}	ROE establishment time (nominal values: actual duration is bit rate dependent, see Table 25)	SPF byte 01H; bits:				
		D3, D2 = 0 0	–	20	–	ms
		D3, D2 = 0 1	–	30	–	ms
		D3, D2 = 1 0	–	40	–	ms
		D3, D2 = 1 1	–	50	–	ms
I²C-bus interface						
f_{SCL}	SCL clock frequency		0	–	100	kHz
t_{LOW}	SCL clock low period		4.7	–	–	µs
t_{HIGH}	SCL clock HIGH period		4.0	–	–	µs
$t_{SU;DAT}$	data set-up time		250	–	–	ns
$t_{HD;DAT}$	data hold time		500	–	–	ns
t_r	SDA and SCL rise time		–	–	1000	ns
t_f	SDA and SCL fall time		–	–	300	ns
C_B	capacitive bus line load		–	–	400	pF
$t_{SU;STA}$	START condition set-up time		4.7	–	–	µs
$t_{HD;STA}$	START condition hold time		4.0	–	–	µs
$t_{SU;STO}$	STOP condition set-up time		4.0	–	–	µs
Reset						
t_{RST}	external reset duration		50	–	–	µs
t_{RSU}	set-up time after reset	oscillator running	–	–	105	µs
t_{OSU}	set-up time after switch-on	oscillator running	–	–	4	ms
Data input						
t_{TDI}	data input transition time	see Fig.14	–	–	100	µs
t_{DI1}	data input logic 1 duration	see Fig.14	t_{BIT}	–	∞	
t_{DI0}	data input logic 0 duration	see Fig.14	t_{BIT}	–	∞	
POCSAG data timing (512 bits/s)						
f_{DI}	data input rate	SPF byte 01H; D5 = 0; D4 = 0	–	512	–	bits/s
t_{BIT}	bit duration		–	1.9531	–	ms
t_{CW}	codeword duration		–	62.5	–	ms
t_{PA}	preamble duration		1125	–	–	ms
t_{BAT}	batch duration		–	1062.5	–	ms

SYMBOLS	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
POCSAG data timing (1200 bits/s)						
f_{DI}	data input rate	SPF byte 01H; D5 = 1; D4 = 0	–	1200	–	bits/s
t_{BIT}	bit duration		–	833.3	–	µs
t_{CW}	codeword duration		–	26.7	–	ms
t_{PA}	preamble duration		480	–	–	ms
t_{BAT}	batch duration		–	453.3	–	ms
POCSAG data timing (2400 bits/s)						
f_{DI}	data input rate	SPF byte 01H; D5 = 1; D4 = 1	–	2400	–	bits/s
t_{BIT}	bit duration		–	416.6	–	µs
t_{CW}	codeword duration		–	13.3	–	ms
t_{PA}	preamble duration		240	–	–	ms
t_{BAT}	batch duration		–	226.6	–	ms
APOC-1 batch timing						
t_{SB}	cycle duration	SPF byte 00H; bit D2 = 0 (5 batches)	–	2720	–	bits
		SPF byte 00H; bit D2 = 0 (15 batches)	–	8160	–	bits
Synthesizer control						
t_{ZSU}	synthesizer set-up duration	oscillator running; note 3	1	–	2	bits
f_{ZSC}	output clock frequency	note 4	–	38400	–	Hz
t_{ZCL}	clock pulse duration		–	13.02	–	µs
t_{ZSD}	data bit duration	note 4	–	26.04	–	µs
t_{ZDS}	data bit set-up time		–	13.02	–	µs
t_{ZDL1}	data load enable delay		–	91.15	–	µs
t_{ZLE}	load enable pulse duration		–	13.02	–	µs
t_{ZDL2}	inter block delay		–	117.19	–	µs

Notes

1. 32768 Hz reference signal; 32 pulses per 75 clock cycles, alternately separated by 1 or 2 pulse periods (pulse duration: t_{RFP}). The timing is shown in Fig.15.
2. 50 Hz reference signal: square wave.
3. Duration depends on programmed bit rate; after reset t_{ZSU} = 1.5 bits.
4. Nominal values; pause in 12th data bit (see Table 11).

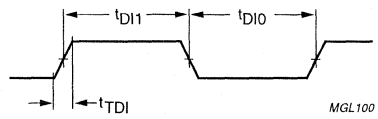


Fig.14 Data input timing.

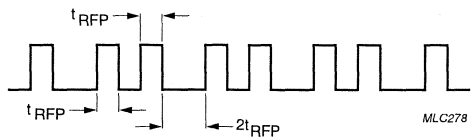
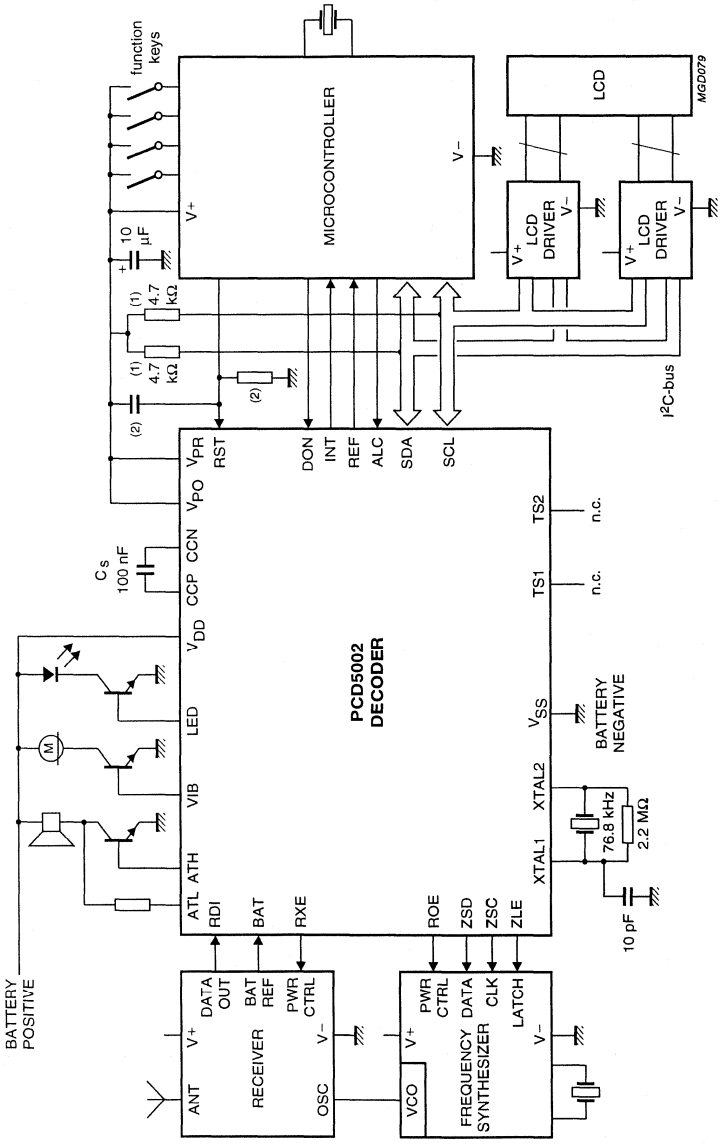


Fig.15 Timing of the 32 768 Hz reference signal.

15 APPLICATION INFORMATION



(1) Value depends on number of devices attached.
(2) Values should be chosen to give a time constant of at least 150 µs. C = 2.2 nF and R = 100 kΩ are recommended.

Fig.16 Typical application example (display pager).

Advanced POCSAG Paging Decoder PCD5003

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Advanced POCSAG Paging Decoder PCD5003

1 FEATURES

- Wide operating supply voltage range: 1.5 to 6.0 V
- EEPROM programming requires only 2.0 V supply
- Low operating current: 50 µA typ. (ON), 25 µA typ. (OFF)
- Temperature range: –25 to +70 °C
- *"CCIR Radio paging Code No. 1"* (POCSAG) compatible
- 512, 1200 and 2400 bits/s data rates using 76.8 kHz crystal
- Built-in data filter (16-times oversampling) and bit clock recovery
- Advanced ACCESS® synchronization algorithm
- 2-bit random and (optional) 4-bit burst error correction
- Up to 6 user addresses (RICs), each with 4 functions/alert cadences
- Up to 6 user address frames, independently programmable
- Standard POCSAG sync word, plus up to 4 user programmable sync words
- Received data inversion (optional)
- Call alert via beeper, vibrator or LED
- 2-level acoustic alert using single external transistor
- Alert control: automatic (POCSAG type), via cadence register or alert input pin
- Separate power control of receiver and RF-oscillator for battery economy
- Synthesizer set-up and control interface (3-line serial)
- On-chip EEPROM for storage of user addresses (RICs), pager configuration and synthesizer data
- On-chip SRAM buffer for message data
- Slave I²C-bus interface to microcontroller for transfer of message data, status/control and EEPROM programming (data transfer at up to 400 kbits/s)
- Wake-up interrupt for microcontroller, programmable polarity
- Direct and I²C-bus control of operating status (ON/OFF)
- Battery-low indication (external detector)
- Out-of-range condition indication
- Real time clock reference output
- On-chip voltage doubler
- Interfaces directly to UAA2080 and UAA2082 paging receivers.

2 APPLICATIONS

- Display pagers, basic alert-only pagers
- Information services
- Personal organizers
- Telepoint
- Telemetry/data transmission.

3 GENERAL DESCRIPTION

The PCD5003 is a very low power POCSAG decoder and pager controller. It supports data rates of 512, 1200 and 2400 bits/s using a single 76.8 kHz crystal. On-chip EEPROM is programmable using a minimum supply voltage of 2.0 V, allowing 'over-the-air' programming. The PCD5003 is fast I²C-bus compatible (maximum 400 kbits/s).

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD5003H	LQFP32	plastic low profile quad flat package; 32 leads; body 7 × 7 × 1.4 mm	SOT358-1
PCD5003U/10	–	film-frame carrier (naked die) 32 pads	–

5 BLOCK DIAGRAM

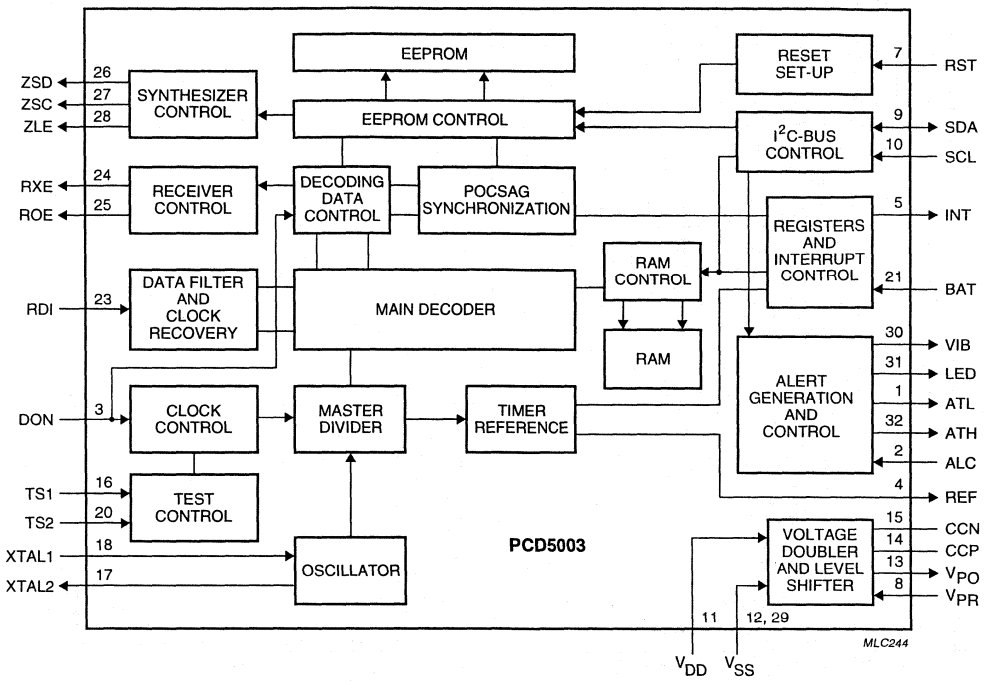


Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	DESCRIPTION
ATL	1	alert LOW level output
ALC	2	alert control input (normally LOW by internal pull-down)
DON	3	direct ON/OFF input (normally LOW by internal pull-down)
REF	4	real time clock frequency reference output
INT	5	interrupt output
n.c.	6	not connected
RST	7	reset input (normally LOW by internal pull-down)
V_{PR}	8	external positive voltage reference input
SDA	9	I^2C-bus serial data input/output
SCL	10	I^2C-bus serial clock input
V_{DD}	11	main positive supply voltage
V_{SS}	12	main negative supply voltage
V_{PO}	13	voltage converter positive output
CCP	14	voltage converter shunt capacitor (positive side)
CCN	15	voltage converter shunt capacitor (negative side)
TS1	16	test input 1 (normally LOW by internal pull-down)
XTAL2	17	decoder crystal oscillator output
XTAL1	18	decoder crystal oscillator input
n.c.	19	not connected
TS2	20	test input 2 (normally LOW by internal pull-down)
BAT	21	battery sense input
n.c.	22	not connected
RDI	23	received POCSAG data input
RXE	24	receiver circuit enable output
ROE	25	receiver oscillator enable output
ZSD	26	synthesizer serial data output
ZSC	27	synthesizer serial clock output
ZLE	28	synthesizer latch enable output
V_{SS}	29	main negative supply voltage
VIB	30	vibrator motor drive output
LED	31	LED drive output
ATH	32	alert HIGH level output

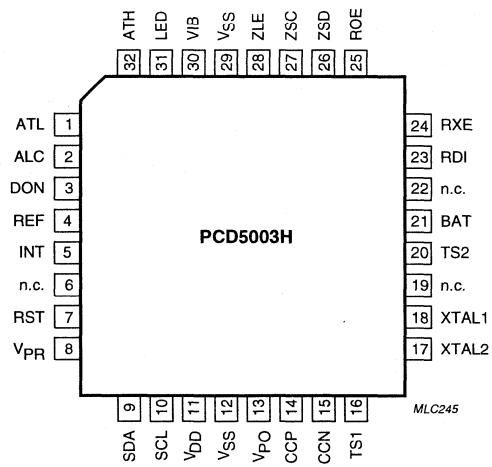


Fig.2 Pin configuration for SOT358-1 (LQFP32).

7 FUNCTIONAL DESCRIPTION

7.1 Introduction

The PCD5003 is a very low power decoder and pager controller specifically designed for use in new generation radio pagers. The architecture of the PCD5003 allows for flexible application in a wide variety of radio pager designs.

The PCD5003 is fully compatible with *"CCIR Radio paging Code No. 1"* (also known as the POCSAG code) operating at data rates of 512, 1200 and 2400 bits/s using a single oscillator crystal of 76.8 kHz.

In addition to the standard POCSAG sync word the PCD5003 is also capable of recognizing up to 4 User Programmable Sync Words (UPSWs). This permits the reception of both private services and POCSAG transmissions via the same radio channel.

Used together with the Philips UAA2080 or UAA2082 paging receiver, the PCD5003 offers a highly sophisticated, miniature solution for the radio paging market. Control of an RF synthesizer circuit is also provided to ease alignment and channel selection.

On-chip EEPROM provides storage for user addresses (Receiver Identity Codes or RICs) and Special Programmed Functions (SPFs), which eliminates the need for external storage devices and interconnection. For other non-volatile storage 20 bytes of general purpose EEPROM are available. The low EEPROM programming voltage makes the PCD5003 well- suited for 'over-the-air' programming/reprogramming.

On request from an external controlling device or automatically (by SPF programming), the PCD5003 will provide standard POCSAG alert cadences by driving a standard acoustic 'beeper'. Non-standard alert cadences may be generated via a cadence register or a dedicated control input.

The PCD5003 can also produce a HIGH level acoustic alert as well as drive an LED indicator and a vibrator motor via external bipolar transistors.

The PCD5003 contains a low-power, high-efficiency voltage converter (doubler) designed to provide a higher voltage supply to LCD drivers or microcontrollers. In addition, an independent level shifted interface is provided allowing communication to a microcontroller operating at a higher voltage than the PCD5003.

Interface to such an external device is provided by an I^2C-bus which allows received call identity and message data, data for the programming of the internal EEPROM, alert control and pager status information to be transferred between the devices. Pager status includes features provided by the PCD5003 such as battery-low and out-of-range indications. A dedicated interrupt line minimizes the required microcontroller activity.

A selectable low frequency timing reference is provided for use in real time clock functions.

Data synchronization is achieved by the Philips patented ACCESS® algorithm ensuring that maximum advantage is made of the POCSAG code structure particularly in fading radio signal conditions. The algorithm allows for data synchronization without preamble detection whilst minimizing battery power consumption.

Random and (optional) burst error correction techniques are applied to the received data to optimize on call success rate without increasing falsing rate beyond specified POCSAG levels.

7.2 The POCSAG paging code

A transmission using the *"CCIR Radio paging Code No. 1"* (POCSAG code) is constructed in accordance with the following rules (see Fig.3).

The transmission is started by sending a **preamble**, consisting of at least 576 continuously alternating bits (10101010...). The preamble is followed by an arbitrary number of batch blocks. Only complete batches are transmitted.

Each **batch** comprises 17 codewords of 32 bits each. The first codeword is a synchronization codeword with a fixed pattern. The **sync** word is followed by 8 frames (0 to 7)
of 2 codewords each, containing message information. A codeword in a frame can either be an address, message or idle codeword.

Idle codewords also have a fixed pattern and are used to fill empty frames or to separate messages.

Address codewords are identified by an MSB of logic 0 and are coded as shown in Fig.3. A user address or RIC consists of 21 bits. Only the upper 18 bits are encoded in the address codeword (bits 2 to 19).
The lower 3 bits designate the frame number (0 to 7) in which the address is transmitted.

Four different **call types** ('numeric', 'alphanumeric' and two 'alert only' types) can be distinguished on each user address. The call type is determined by two function bits in the address codeword (bits 20 and 21), as shown in Table 1.

Alert-only calls only consist of a single address codeword. Numeric and alphanumeric calls have message codewords following the address. A message causes the frame structure to be temporarily suspended. Message codewords are sent until the message is completed, with only the sync words being transmitted in their expected positions.

Message codewords are identified by an MSB of logic 1 and are coded as shown in Fig.3. The message information is stored in a 20-bit field (bits 2 to 21). The data format is determined by the call type: 4 bits per digit for numeric messages and 7 bits per (ASCII) character for alphanumeric messages.

Each codeword is protected against transmission errors by 10 CRC check bits (bits 22 to 31) and an even-parity bit (bit 32). This permits correction of maximum 2 random errors or up to 3 errors in a burst of 4 bits (a 4-bit burst error) per codeword.

The POCSAG standard recommends the use of combinations of data formats and function bits, as given in Table 1. Other (non-standard) combinations will be received normally by the PCD5003. Message data is not deformatted.

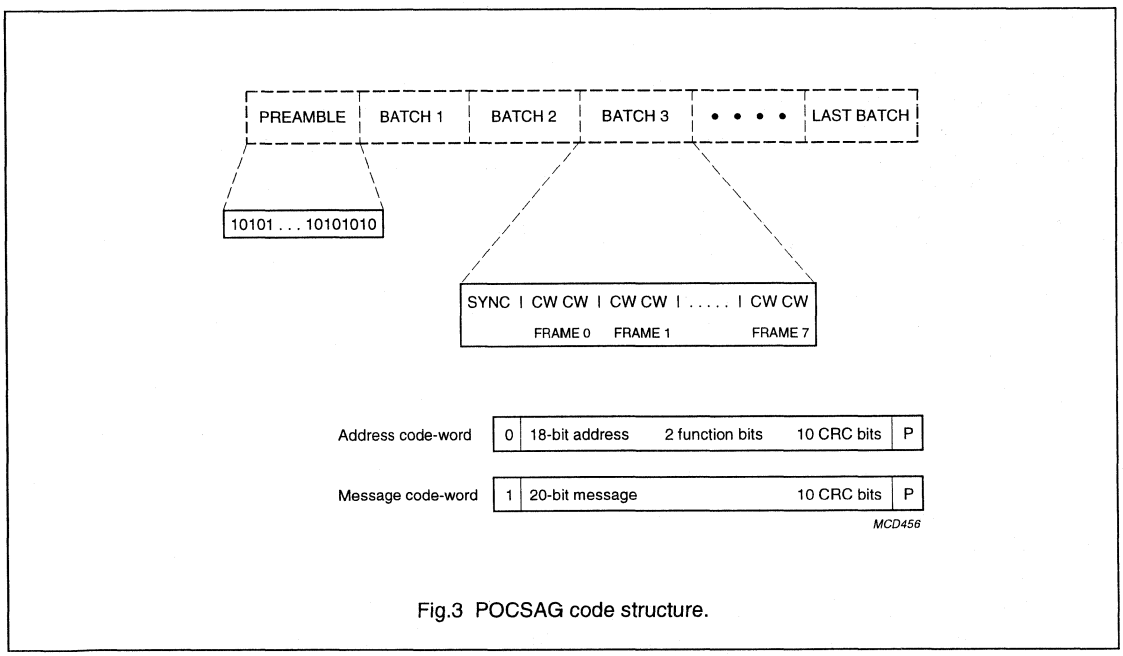


Fig.3 POCSAG code structure.

Table 1 POCSAG recommended call types and function bits

BIT 20 (MSB)	BIT 21 (LSB)	CALL TYPE	DATA FORMAT
0	0	numeric	4-bits per digit
0	1	alert only 1	–
1	0	alert only 2	–
1	1	alphanumeric	7-bits per ASCII character

7.3 Error correction

Table 2 Error correction

ITEM	DESCRIPTION
Preamble	4 random errors in 31 bits
Synchronization codeword	2 random errors in 32 bits
Address codeword	2 random errors, plus: 4-bit burst errors (optional)
Message codeword	2 random errors, plus: 4-bit burst errors (optional)

In the PCD5003 error correction methods have been implemented as shown in Table 2.

Random error correction is default for both address and message codewords. In addition, burst error correction can be enabled by SPF programming. Up to 3 erroneous bits in a 4-bit burst can be corrected.

The error type detected for each codeword is identified in the message data output to the microcontroller, allowing rejection of calls with too many errors.

7.4 Operating states

The PCD5003 has 2 operating states:

- ON status
- OFF status.

The operating state is determined by a Direct Control input (DON) and bit D4 in the control register (see Table 3).

Table 3 Truth table for decoder operating status

DON INPUT	CONTROL BIT D4	OPERATING STATUS
0	0	OFF
0	1	ON
1	0	ON
1	1	ON

7.5 ON status

In ON status the decoder pulses the receiver and oscillator enable outputs (respectively RXE and ROE) according to the code structure and the synchronization algorithm. Data received serially at the data input (RDI) is processed for call receipt. Reception of a valid paging call is signalled to the microcontroller by means of an interrupt signal. The received address and message data can then be read via the I^2C-bus interface.

7.6 OFF status

In OFF status the decoder will neither activate the receiver or oscillator enable outputs, nor process any data at the data input. The crystal oscillator remains active to permit communication with the microcontroller.

In both operating states an accurate timing reference is available via the REF output. By SPF programming the signal periodicity may be selected as 32.768 kHz, 50 Hz, 2 Hz or $1/60$ Hz.

7.7 Reset

The decoder can be reset by applying a positive pulse on input pin RST. A power-on reset circuit consisting of an RC network can be connected to this input as well. Conditions during and after a reset are described in Chapter "Operating instructions".

For successful reset at power-on, a HIGH level must be present on the RST pin while the device is powering-up. This can be applied by the microcontroller, or via a suitable RC power-on reset circuit connected to the RST input. Reset circuit details and conditions during and after a reset are described in Chapter 8

7.8 Bit rates

The PCD5003 can be configured for data rates of 512, 1200 or 2400 bit/s by SPF programming. These data rates are derived from a single 76.8 kHz oscillator frequency.

7.9 Oscillator

The oscillator circuit is designed to operate at 76.8 kHz. Typically, a tuning fork crystal will be used as a frequency source. Alternatively, an external clock signal can be applied to pin XTAL1 (amplitude = V_{DD} to V_{SS}), but a slightly higher oscillator current is consumed. A 2.2 MΩ feedback resistor connected between XTAL1 and XTAL2 is required for proper operation.

To allow easy oscillator adjustment (e.g. by means of a variable capacitor) a 32.768 kHz reference frequency can be selected at output REF by SPF programming.

7.10 Input data processing

Data input is binary and fully asynchronous. Input bit rates of 512, 1200 and 2400 bits/s are supported. As a programmable option, the polarity of the received data can be inverted before further processing.

The input data is noise filtered by means of a digital filter. Data is sampled at 16 times the data rate and averaged by majority decision.

The filtered data is used to synchronize an internal clock generator by monitoring transitions. The recovered clock phase can be adjusted in steps of $1/8$ or $1/32$ bit period per received bit.

The larger step size is used when bit synchronization has not been achieved, the smaller when a valid data sequence has been detected (e.g. preamble or sync word).

7.11 Battery saving

Current consumption is reduced by switching off internal decoder sections whenever the receiver is not enabled.

To further increase battery efficiency, reception and decoding of an address codeword is stopped as soon as the uncorrected address field differs by more than 3 bits from the enabled RICs. If the next codeword must be received again, the receiver is re-enabled thus observing the programmed establishment times t_{RXE} and t_{RDE}.

The current consumption of the complete pager can be minimized by separately activating the RF oscillator circuit (at output ROE) before activating the rest of the receiver. This is possible with the UAA2082 receiver which has external biasing for the oscillator circuit.

7.12 Synchronization strategy

In ON status the PCD5003 synchronizes to the POCSAG data stream by means of the Philips ACCESS® algorithm. A flow diagram is shown in Fig.4. Where 'sync word' is used, this implies both the standard POCSAG sync word and any enabled User Programmable Sync Word (UPSW).

Several modes of operation can be distinguished depending on the synchronization state. Each mode uses a different method to obtain or retain data synchronization. The receiver and oscillator enable outputs (respectively RXE and ROE) are switched accordingly, with the appropriate establishment times (respectively t_{RXON} and t_{ROON}).

Before comparing received data with preamble, an enabled sync word or programmed user addresses, the appropriate error correction is applied.

Initially, after switching to ON status, the decoder is in **switch-on** mode. Here the receiver will be enabled for a period up to 3 batches, testing for preamble and sync word. Failure to detect preamble or sync word will cause switching to 'carrier off' mode.

Detection of preamble switches to **preamble receive** mode, in which sync word is looked for. The receiver will remain enabled while preamble is detected. When neither sync word nor preamble is found within 1 batch duration 'carrier off' mode is entered.

Upon detection of a sync word the **data receive** mode is entered. The receiver is activated only during enabled user address frames and sync word periods. When an enabled user address has been detected, the receiver will be kept enabled for message codeword reception until the call termination criteria are met.

During call reception data bytes are stored in an internal SRAM buffer, capable of storing 2 batches of message data.

Messages are transmitted contiguously, only interrupted by sync words at the beginning of each batch. When a message extends beyond the end of a batch, no testing for sync takes place. Instead, a message data transfer will be initiated by an interrupt to the external controller. Data reception continues normally after a period corresponding to the sync word duration.

If any message codeword is found to be uncorrectable, 'data-fail' mode is entered and no data transfer will be attempted at the next sync word position. Instead, a test for sync word will be carried out.

In the **data fail** mode message reception continues normally for 1 batch duration. Upon detection of sync word at the expected position the decoder returns to 'data receive' mode. If sync word again fails to appear, batch synchronization is deemed lost. Call reception is then terminated and 'fade recovery' mode is entered.

The **fade recovery** mode is intended to scan for sync word and preamble over an extended window (nominal position ±8 bits).

This is done for a period of up to 15 batches, allowing recovery of synchronization from long fades in the radio signal. Detection of preamble switches to 'preamble receive' mode, while sync word detection switches to 'data receive' mode. When neither is found within a period of 15 batches, the radio signal is considered lost and 'carrier off' mode is entered.

The purpose of **carrier off** mode is to detect a valid radio transmission and synchronize to it quickly and efficiently. Because transmissions may start at random, the decoder enables the receiver for 1 codeword in every 18 codewords looking for preamble or sync word. By using a buffer containing 32 bits (n bits from the current scan, 32 – n from the previous scan) effectively every batch bit position can be tested within a continuous transmission of at least 18 batches. Detection of preamble switches to 'preamble receive' mode, while sync word detection switches to 'data receive' mode.

7.13 Call termination

Call reception is terminated:

- Upon reception of any address codeword (including Idle codeword) requiring no more than single bit error correction
- In 'data fail' mode, when a sync word is not found at the expected batch position
- When a forced call termination command is received from an external controller.

The last method permits an external controller to stop call reception depending on the number and type of errors which occurred in a call. After a forced call termination the decoder will enter 'data fail' mode.

The type of error correction as well as the call termination conditions are indicated by status bits in the message data output.

Following call termination, transfer of the data received since the previous sync word period is initiated by means of an interrupt to the external controller.

7.14 Call data output format

POCSAG call information is stored in the decoder SRAM in blocks of 3 bytes per codeword. Each stored call consists of a call header, followed by message data blocks and concluded by a call terminator. In the event of concatenated messages the call terminator is replaced with the call header of the next message. An alert-only call only has a call header and a call terminator.

The formats of a call header, a message data block and a call terminator are shown in Tables 4, 6 and 8.

A **Call Header** contains information on the last sync word received, the RIC which began call reception and the type of error correction performed on the address codeword.

A **Message Data** block contains the data bits from a message codeword plus the type of error correction performed. No deformatting is done on the data bits: numeric data appear as 4-bit groups per digit, alphanumeric data have a 7-bit ASCII representation.

The **Call Terminator** contains information on the last sync word received, information on the way the call was terminated (forced call termination command, loss of sync word in 'data fail' mode) and the type of error correction performed on the terminating codeword.

7.15 Sync word indication

The sync word recognized by the PCD5003 is shown in the call header (bits S3 to S1). The decimal value represents the identifier number in the EEPROM of the UPSW in question. A value of 7 indicates the standard POCSAG sync word.

7.16 Error type indication

Table 10 shows how the different types of detected errors are encoded in the call data output format.

A message codeword containing more than a single bit error (bit E3 = 1) may appear as an address codeword (bit M1 = 0) after error correction. In this event the codeword is processed as message data and does not cause call termination.

7.17 Data transfer

Data transfer is initiated either during sync word periods or as soon as the receiver is disabled after call termination. If the SRAM buffer is full, data transfer is initiated immediately during the next codeword.

When the PCD5003 is ready to transfer received call data an external interrupt will be generated via output INT. Any message data can be read by accessing the RAM output register via the I^2C-bus interface. Bytes will be output starting from the position indicated by the RAM read pointer.

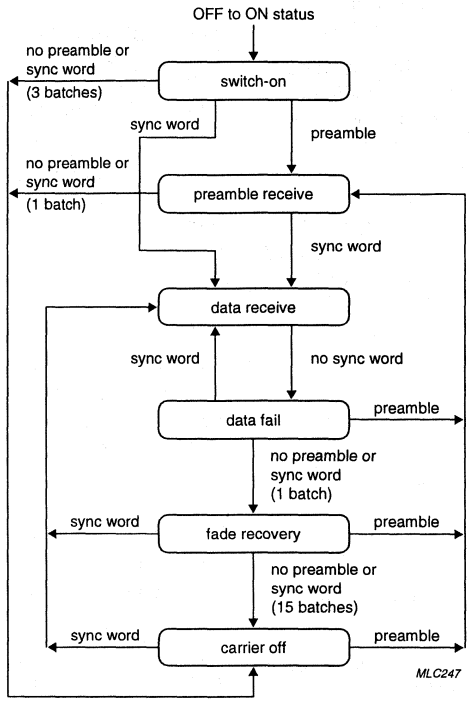


Fig.4 ACCESS® synchronization algorithm.

Table 4 Call header format

BYTE NUMBER	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
1	0	S3	S2	S1	R3	R2	R1	DF
2	0	S3	S2	S1	R3	R2	R1	0
3	X	X	F0	F1	E3	E2	E1	0

Table 5 Call header bit identification

BITS (MSB to LSB)	IDENTIFICATION
S3 to S1	identifier number of sync word for current batch (7 = standard POCSAG)
R3 to R1	identifier number of user address (RIC)
DF	data fail mode indication (1 = data fail mode); note 1
F0 and F1	function bits of received address codeword (bits 20, 21)
E3 to E1	detected error type; see Table 10; E3 = 0 in a concatenated call header

Note

1. The DF bit in the call header is set:
   a) When the sync word of the batch in which the (beginning of the) call was received, did not match the standard POCSAG or a user-programmed sync word. The sync word identifier (bits S3 to S1) will then be made 0.
   b) When any codeword of a previous call received in the same batch was uncorrectable.

Table 6 Message data format

BYTE NUMBER	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
1	M2	M3	M4	M5	M6	M7	M8	M9
2	M10	M11	M12	M13	M14	M15	M16	M17
3	M18	M19	M20	M21	E3	E2	E1	M1

Table 7 Message data bit identification

BITS (MSB to LSB)	IDENTIFICATION
M2 to M21	message codeword data bits
E3 to E1	detected error type; see Table 10
M1	message codeword flag

Table 8 Call terminator format

BYTE NUMBER	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
1	FT	S3	S2	S1	0	0	0	DF
2	FT	S3	S2	S1	0	0	0	X
3	X	X	X	X	E3	E2	E1	0

Table 9 Call terminator bit identification

BITS (MSB to LSB)	IDENTIFICATION
FT	forced call termination (1 = yes)
S3 to S1	identifier number of last sync word
DF	data fail mode indication (1 = data fail mode); note 1
E3 to E1	detected error type; see Table 10; E3 = 0 in a call terminator

Note

1. The DF bit in the call terminator is set:
   a) When any call data codeword in the terminating batch was uncorrectable, while in 'data receive' mode.
   b) When the sync word at the start of the terminating batch did not match the standard POCSAG or a user-programmed sync word, while in 'data fail' mode.

Table 10 Error type identification (note 1)

E3	E2	E1	ERROR TYPE	NUMBER OF ERRORS
0	0	0	no errors - correct codeword	0
0	0	1	parity bit in error	1
0	1	0	single bit error	1 + parity
0	1	1	single bit error and parity error	1
1	0	0	not used	
1	0	1	4-bit burst error and parity error	3 (e.g.1101)
1	1	0	2-bit random error	2
1	1	1	uncorrectable codeword	3 or more

Note

1. POCSAG code allows a maximum of 3 bit errors to be detected per codeword.

Successful call termination occurs by reception of a valid address codeword with less than 2 bit errors.
Unsuccessful termination occurs when sync word is not detected while in 'data fail' mode.

It is generally possible to distinguish these two conditions using the sync word identifier number (bits S3 to S1); the identifier number will be non-zero for correct termination, and zero for sync word failure.

Only when a call is received in 'data fail' mode and the call is terminated before the end of the batch, is it not possible to distinguish unsuccessful from correct termination.

Reception of message data can be terminated at any time by transmitting a forced call termination command to the control register via the I²C-bus. Any call received will then be terminated immediately and 'data fail' mode will be entered.

7.18 Receiver and oscillator control

A paging receiver and an RF oscillator circuit can be controlled independently via enable outputs RXE and ROE respectively. Their operating periods are optimized according to the synchronization mode of the decoder. Each enable signal has its own programmable establishment time (see Table 11).

7.19 External receiver control and monitoring

An external controller may enable the receiver control outputs continuously via an I²C-bus command, overruling the normal enable pattern. Data reception continues normally. This mode can be left by means of a reset or an I²C-bus command.

External monitoring of the receiver control output RXE is possible via bit D6 in the status register, when enabled via the control register (D2 = 1). Each change of state of output RXE will generate an external interrupt at output INT.

7.20 Battery condition input

A logic signal from an external sense circuit signalling battery condition can be applied to the BAT input. This input is sampled each time the receiver is disabled (RXE ↓ 0).

When enabled via the control register (D2 = 0), the condition of input BAT is reflected in bit D6 of the status register. Each change of state of bit D6 causes an external interrupt at output INT.

When using the UAA2080 pager receiver a battery-low condition corresponds to a logic HIGH-level. With a different sense circuit the reverse polarity can be used as well, because every change of state is signalled to an external controller.

After a reset the initial condition of the battery-low indicator in the status register is zero.

Table 11 Receiver and oscillator establishment times (note 1)

CONTROL OUTPUT	ESTABLISHMENT TIME				UNIT
RXE	5	10	15	30	ms
ROE	20	30	40	50	ms

Note

1. The exact values may differ slightly from the above values, depending on the bit rate (see Table 22).

7.21 Synthesizer control

Control of an external frequency synthesizer is possible via a dedicated 3-line serial interface (outputs ZSD, ZSC and ZLE). This interface is common to a number of available synthesizers. The synthesizer is enabled using the oscillator enable output ROE.

The frequency parameters must be programmed in EEPROM. Two blocks of maximum 24 bits each can be stored. Any unused bits must be programmed at the beginning of a block: only the last bits are used by the synthesizer.

When the function is selected by SPF programming (SPF byte 01, bit D6), data is transferred to the synthesizer each time the PCD5003 is switched from OFF to ON status. Transfer takes place serially in two blocks, starting with bit 0 (MSB) of block 1 (see Table 25).

Data bits on ZSD change on the falling flanks of ZSC. After clocking all bits into the synthesizer, a latch enable pulse copies the data to the internal divider registers. A timing diagram is given in Fig.5.

The data output timing is synchronous, but has a pause in the bit stream of each block. This pause occurs in the 13th bit while ZSC is LOW. The nominal pause duration t_p depends on the programmed bit rate for data reception and is shown in Table 12. The total duration of the 13th bit is given by $t_{ZCL} + t_p$.

A similar pause occurs between the first and the second data block. The delay between the first latch enable pulse and the second data block is given by $t_{ZDL2} + t_p$.
The complete start-up timing of the synthesizer interface is given in Fig.12.

Table 12 Synthesizer programming pause

BIT RATE (bit/s)	t_p (clocks)	t_p (μs)
512	119	1549
1200	33	430
2400	1	13

7.22 Serial microcontroller interface

The PCD5003 has an I²C-bus serial microcontroller interface capable of operating at 400 kbits/s.
The PCD5003 is a slave transceiver with a 7-bit I²C-bus address 39 (bits A6 to A0 = 0100111). Together with the R/$\overline{W}$ bit the first byte of an I²C-bus message then becomes 4EH (write) or 4FH (read).

Data transmission requires 2 lines: SDA (data) and SCL (clock), each with an external pull-up resistor. The clock signal (SCL) for any data transmission must be generated by the external controlling device.

A transmission is initiated by a start condition (S: SCL = 1, SDA = ↓) and terminated by a stop condition (P: SCL = 1, SDA = ↑).

Data bits must be stable when SCL is HIGH. If there are multiple transmissions, the stop condition can be replaced with a new start condition.

Data is transferred on a byte basis, starting with a device address and a read/write indicator. Each transmitted byte must be followed by an acknowledge bit ACK (active LOW). If a receiving device is not ready to accept the next complete byte, it can force a bus wait state by holding SCL LOW.

The general I²C-bus transmission format is shown in Fig.6. Formats for master/slave communication are shown in Fig.7.

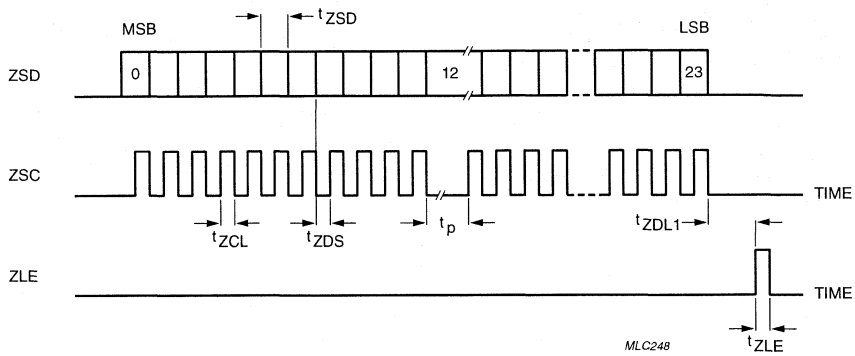


Fig.5 Synthesizer interface timing.

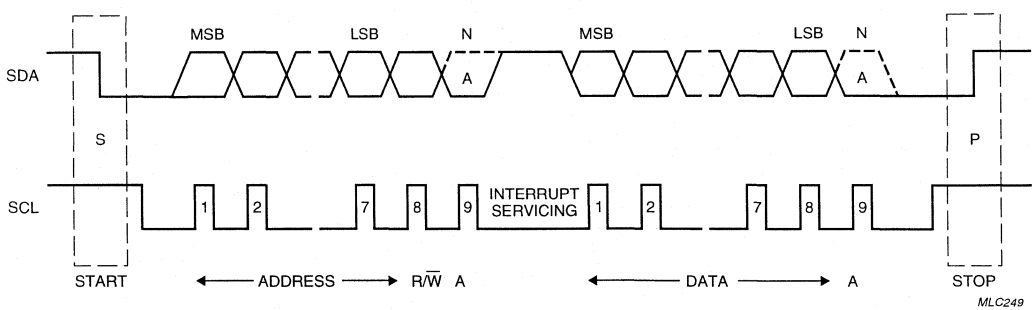
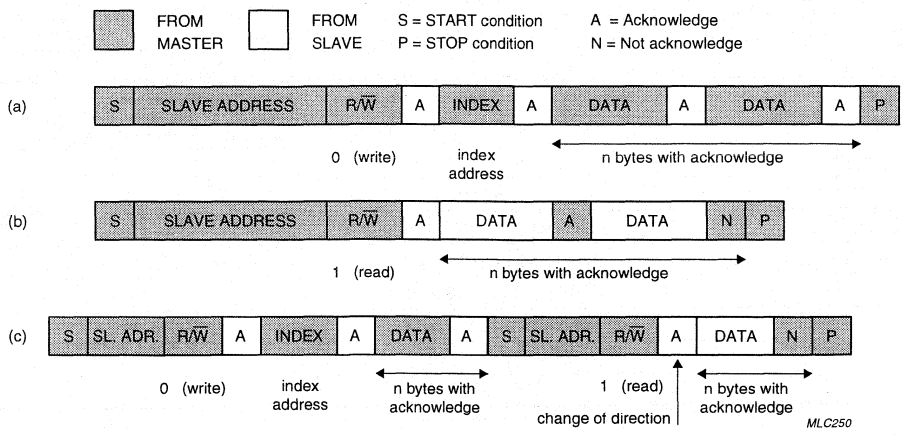


Fig.6 I²C-bus message format.



(a) Master writes to slave.
(b) Master reads from slave.
(c) Combined format (shown: write plus read).

Fig.7 Message types.

7.23 Decoder I²C-bus access

All internal access to the PCD5003 takes place via I²C-bus interface. For this purpose the internal registers, SRAM and EEPROM have been memory mapped and are accessed via an **index register**. Table 13 shows the index addresses of all internal blocks.

Registers are addressed directly, while RAM and EEPROM are addressed indirectly via address pointers and I/O registers.

Remark: The EEPROM memory map is non-contiguous and organized as a matrix.
The EEPROM address pointer contains both row and column indicators.

Data written to read-only bits will be ignored. Values read from write-only bits are undefined and must be ignored.

Each I²C write message to the PCD5003 must start with its slave address, followed by the index address of the memory element to be accessed. An I²C read message uses the last written index address as a data source. The different I²C-bus message types are shown in Fig.7.

As a slave the PCD5003 cannot initiate bus transfers by itself. To prevent an external controller from having to monitor the operating status of the decoder, all important events generate an external interrupt on output INT.

Table 13 Index register

ADDRESS[1]	REGISTER FUNCTION	ACCESS
00H	status	R
00H	control	W
01H	real time clock: seconds	R/W
02H	real time clock: $^1/_{100}$ second	R/W
03H	alert cadence	W
04H	alert set-up	W
05H	periodic interrupt modulus	W
05H	periodic interrupt counter	R
06H	RAM write address pointer	R
07H	EEPROM address pointer	R/W
08H	RAM read address pointer	R/W
09H	RAM data output	R
0AH	EEPROM data input/output	R/W
0BH to 0FH	unused	note 2

Notes

1. The index register only uses the least significant nibble, the upper 4 bits are ignored.
2. Writing to registers 0B to 0F has no effect, reading produces meaningless data.

7.24 External interrupt

The PCD5003 can signal events to an external controller via an interrupt signal on output INT. The interrupt polarity is programmable via SPF programming. The interrupt source is shown in the status register.

Interrupts are generated by the following events (more than one event possible):

- Call data available for output (bit D2)
- SRAM pointers becoming equal (bit D3)
- Expiry of periodic time-out (bit D7)
- Expiry of alert time-out (bit D4)
- Change of state in out-of-range indicator (bit D5)
- Change of state in battery-low indicator or in receiver control output RXE (bit D6).

Immediate interrupts are generated by status bits D3, D4, D6 (RXE monitoring) and D7. Bits D2, D5 and D6 (BAT monitoring) generate interrupts as soon as the receiver is disabled (RXE = 0).

When call data is available (D2 = 1) but the receiver remains switched on, an interrupt is generated at the next sync word position.

The interrupt output INT is reset after completion of a status read operation.

7.25 Status/Control register

The status/control register consists of two independent registers, one for reading (status) and one for writing (control).

The status register shows the current operating condition of the decoder and the cause(s) of an external interrupt. The control register activates/deactivates certain functions. Tables 14 and 15 show the bit allocations of both registers.

All status bits will be reset after a status read operation except for the out-of-range, battery-low and receiver enable indicator bits (see note 1 to Table 14).

Status bit D0 is set when call reception is started by detection of an enabled RIC (user address). This does not generate an interrupt.

Table 14 Status register (00H; read)

BIT[1]	VALUE	DESCRIPTION
D1 and D0	0 0	no new call data
	0 1	new call received
	1 0	reserved for future use
	1 1	reserved for future use
D3 and D2	0 0	no data to be read (default after reset)
	0 1	RAM read/write pointers different: data to be read
	1 0	RAM read/write pointers equal: no more data to read
	1 1	RAM buffer full or overflow
D4	1	alert time-out expired
D5	1	out-of-range
D6	1	BAT input HIGH or RXE output active (selected by control bit D2)
D7	1	periodic timer interrupt

Note

1. After a status read operation bits D3, D4 and D7 are always reset, bits D1 and D0 only when no second call is pending. D2 is reset when the RAM is empty (read and write pointers equal).

Table 15 Control register (00H; write)

BIT (MSB: D7)	VALUE	DESCRIPTION
D0	1	forced call termination (automatically reset after termination)
D1	1	EEPROM programming enable
D2	0	BAT input selected for monitoring (status bit D6)
	1	RXE output selected for monitoring (status bit D6)
D3	1	receiver continuously enabled (RXE = 1, ROE = 1)
D4	0	decoder in OFF status (while DON = 0)
	1	decoder in ON status
D5 to D7	X	not used: ignored when written

7.26 Pending interrupts

A secondary status register is used for storing status bits of pending interrupts. This occurs:

- When a new call is received while the previous one was not yet acknowledged by reading the status register
- When an interrupt occurs during a status read operation.

After completion of the status read the primary register is loaded with the contents of the secondary register, which is then reset. Next, an immediate interrupt is generated, output INT becoming active 1 decoder clock cycle after it was reset following the status read.

Remark: In the event of multiple pending calls, only the status bits of the last call are retained.

7.27 Out-of-range Indication

The out-of-range condition occurs when entering fade recovery or 'carrier off' mode. This condition is reflected in bit D5 of the status register. The out-of-range condition is reset when either preamble or a valid sync word is detected.

The out-of-range bit (D5) in the status register is updated each time the receiver is disabled (RXE $\downarrow$ 0). Every change of state in bit D5 generates an interrupt.

7.28 Real time clock

The PCD5003 provides a periodic reference pulse at output REF. The frequency of this signal can be selected by SPF programming:

- 32768 Hz
- 50 Hz (square-wave)
- 2 Hz
- $1/60$ Hz.

The 32768 Hz signal does not have a fixed period: it consists of 32 pulses distributed over 75 main oscillator cycles at 76.8 kHz. The timing is shown in Fig.14.

When programmed for $1/60$ Hz (1 pulse per minute) the pulse at output REF is held off while the receiver is enabled.

Except for the 50 Hz frequency the pulse width t_{RFP} is equal to one decoder clock period.

The real time clock counter runs continuously irrespective of the operating condition of the PCD5003. It contains a **seconds register** (maximum 59) and a **$1/100$ second register** (maximum 99), which can be read or written via the I²C-bus. The bit allocation of both registers is shown in Tables 16 and 17.

Table 16 Real time clock; seconds register (01H; read/write)

BIT (MSB D7)	VALUE	DESCRIPTION
D0	–	1 s
D1	–	2 s
D2	–	4 s
D3	–	8 s
D4	–	16 s
D5	–	32 s
D6	X	not used: ignored when written, undetermined when read
D7	X	not used: ignored when written, undetermined when read

Table 17 Real time clock; $1/100$ second register (02H; read/write)

BIT (MSB D7)	VALUE	DESCRIPTION
D0	–	0 01 s
D1	–	0.02 s
D2	–	0.04 s
D3	–	0.08 s
D4	–	0.16 s
D5	–	0.32 s
D6	–	0.64 s
D7	X	not used: ignored when written, undetermined when read

7.29 Periodic interrupt

A periodic interrupt can be realised with the Periodic Interrupt Counter. This 8-bit counter is incremented every $1/100$ second and produces an interrupt when it reaches the value stored in the Periodic Interrupt Modulus register. The Counter register is then reset and counting continues.

Operation is started by writing a non-zero value to the Modulus register. Writing a zero will stop interrupt generation immediately and will halt the Periodic Interrupt Counter after 2.55 seconds.

The Modulus register is write-only, the Counter register can only be read. Both registers have the same index address (05H).

7.30 Received call delay

Call reception causes both the Periodic Interrupt Modulus and the Counter register to be reset.

Since the Periodic Interrupt Counter runs for another 2.55 seconds after a reset, the received call delay (in $1/100$ second units) can be determined by reading the Counter register.

Table 18 Alert set-up register (04H; write)

BIT (MSB: D7)	VALUE	DESCRIPTION
D0	0	call alert via cadence register
	1	POCSAG call alert (pattern selected by D7, D6)
D1	0	LOW level acoustic alert (ATL), pulsed vibrator alert (25 Hz)
	1	HIGH level acoustic alert (ATL + ATH), continuous vibrator alert
D2	0	normal alerts (acoustic and LED)
	1	warbled alerts: 16 Hz (LED: on/off, ATL/ATH: alternate f_{AWH}, f_{AWL})
D3	1	acoustic alerts enable (ATL, ATH)
D4	1	vibrator alert enabled (VIB)
D5	1	LED alert enabled (LED)
D7 and D6[1]	0 0	POCSAG alert pattern FC = 00, see Fig.8(a)
	0 1	POCSAG alert pattern FC = 01, see Fig.8(b)
	1 0	POCSAG alert pattern FC = 10, see Fig.8(c)
	1 1	POCSAG alert pattern FC = 11, see Fig.8(d)

Note

1. Bits D7 and D6 correspond to function bits 20 and 21 respectively in the address codeword, which designate the POCSAG call type as shown in Table 1.

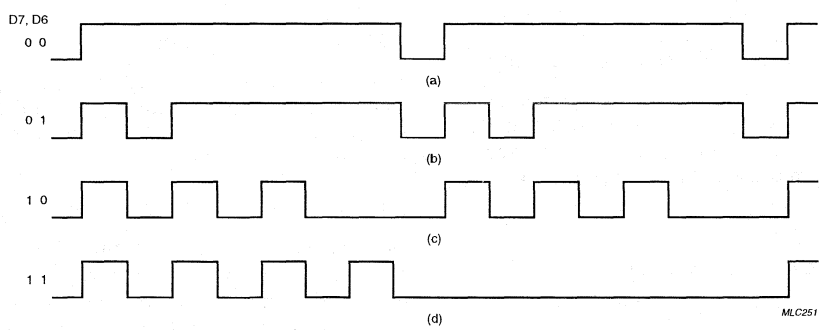


Fig.8 POCSAG alert patterns.

7.31 Alert generation

The PCD5003 is capable of controlling 3 different alert transducers: acoustic beeper (HIGH and LOW level), LED and vibrator motor. The associated outputs are ATH/ATL, LED and VIB respectively. ATL is an open drain output capable of directly driving an acoustic alerter via a resistor. The other outputs require external transistors.

Each alert output can be individually enabled via the alert set-up register. Alert level and warble can be separately selected. The alert pattern can either be standard POCSAG or determined via the alert cadence register. Direct alert control is possible via input ALC.

The alert set-up register is shown in Table 18.

Standard POCSAG alerts can be selected by setting bit D0 in the alert set-up register, bits D6 and D7 determining the alert pattern used.

Automatic generation via all alert outputs of the POCSAG alert pattern matching the received call type can be enabled by SPF programming (SPF byte 03, bit D2).

7.32 Alert cadence register (03H; write)

When not programmed for POCSAG alerts (alert set-up register bit D0 = 0), the 8-bit alert cadence register determines the alert pattern. Each bit represents a 62.5 ms time slot, a logic 1 activating the enabled alert transducers. The bit pattern is rotated with the MSB (bit D7) being output first and the LSB (bit D0) last.

When the last time slot (bit D0) is started an interrupt is generated to allow loading of a new pattern. When the pattern is not changed it will be repeated. Writing a zero to the alert cadence register will halt alert generation.

7.33 Acoustic alert

Acoustic alerts are generated via outputs ATL and ATH. For LOW level alerts only ATL is active, while for HIGH level alerts ATH is also active. ATL is driven in counter phase with ATH.

The alert level is controlled by bit D1 of the alert set-up register.

When D1 is reset, for standard POCSAG alerts (D0 = 1) a LOW level acoustic alert is generated during the first 4 seconds (ATL), followed by 12 seconds at HIGH level (ATL + ATH). When D1 is set, the full 16 seconds are at HIGH level. An interrupt is generated upon expiry of the full alert time.

When using the alert cadence register, D1 would normally be updated by external control when the alert time-out interrupt occurs at the start of the 8th cadence time slot. Since D1 acts immediately on the alert level, it is advised to reset the last bit of the previous pattern to prevent unwanted audible level changes.

7.34 Vibrator alert

The vibrator output (VIB) is activated continuously during a standard POCSAG alert or whenever the alert cadence register is non-zero.

Two alert levels are supported: LOW level (25 Hz square-wave) and HIGH level (continuous). The vibrator level is controlled by bit D1 in the alert set-up register.

7.35 LED alert

The LED output pattern corresponds either to the selected POCSAG alert or to the contents of the alert cadence register. No equivalent exists for HIGH/LOW level alerts.

7.36 Warbled alert

When enabled by setting bit D2 in the alert set-up register, the signals on outputs ATL, ATH and LED are warbled with a 16 Hz modulation frequency. Output LED is switched on and off at the modulation rate, while outputs ATL and ATH switch between f_{AWH} and f_{AWL} alerter frequencies.

7.37 Direct alert control

A direct alert control input (ALC) is available for generating user alarm signals (e.g. battery-low warning). A HIGH level on input ALC activates all enabled alert outputs, overruling any ongoing alert patterns.

7.38 Alert priority

Generation of a standard POCSAG alert (D0 = 1) overrides any alert pattern in the alert cadence register. After completion of the standard alert, the original cadence is restarted from the position it was left at. The alert set-up register will now contain the settings for the standard alert.

The highest priority has been assigned to the alert control input (ALC). All enabled alert outputs will be activated while ALC is set. Outputs are activated/deactivated synchronous with the decoder clock. Activation requires an extra delay of 1 clock when no alerts are being generated.

When input ALC is reset, acoustic alerting does not cease until the current output frequency cycle has been completed.

7.39 Cancelling alerts

Standard POCSAG alerts (manual or automatic) are cancelled by resetting bit D0 in the alert set-up register. User defined alerts are cancelled by writing a zero to the alert cadence register. Any ongoing alert is cancelled when a reset pulse is applied to input RST.

7.40 Automatic POCSAG alerts

Standard alert patterns have been defined for each POCSAG call type, as indicated by the function bits in the address codeword (see Table 1). The timing of these alert patterns is shown in Fig.9.

When enabled by SPF programming (SPF byte 03, bit D2) standard POCSAG alerts will automatically be generated on outputs ATL, ATH, LED and VIB upon call reception. The alert pattern matches the call type as indicated by the function bits in the received address codeword.

The original settings of the alert set-up register will be lost. Bit D0 is reset after completion of the alert.

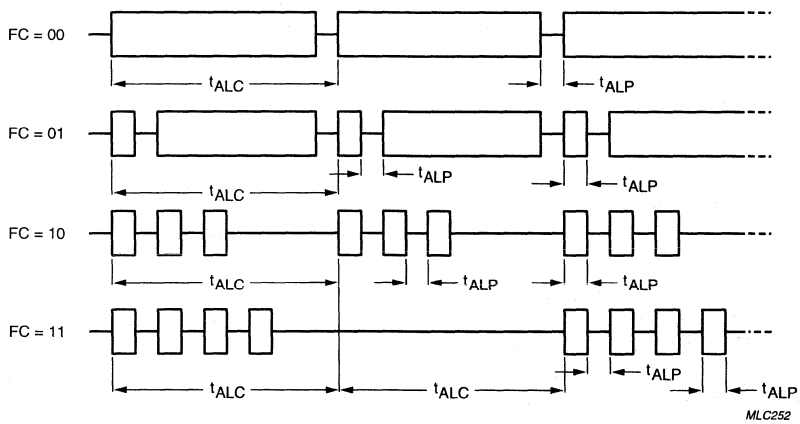


Fig.9 POCSAG alert timing.

7.41 SRAM access

The on-chip SRAM can hold up to 96 bytes of call data. Each call consists of a call header (3 bytes), message data blocks (3 bytes per codeword) and a call terminator (3 bytes).

The RAM is filled by the decoder and can be read via the I^2C-bus interface. The RAM is accessed indirectly by means of a read address pointer and a data output register. A write address pointer indicates the first byte after the last message byte stored.

Status register bit D2 is set when the read and write pointers are different. It is reset only when the SRAM pointers become equal during reading, i.e. when the RAM becomes empty.

Status bit D3 is set when the read and write pointers become equal. This can be due to a RAM empty or a RAM full condition. It is reset after a status read operation.

Interrupts are generated as follows:

- When status bit D2 is set and the receiver is disabled (RXE = 0): data is available for reading
- Immediately when status bit D3 is set: RAM is either empty (status bit D2 = 0) or full (status bit D2 = 1).

To avoid loss of data due to RAM overflow at least 3 bytes of data must be read during reception of the codeword following the 'RAM full' interrupt.

7.42 RAM write address pointer (06H; read)

The RAM write address pointer is automatically incremented during call reception, as the decoder writes each data byte to RAM. The RAM write address pointer can only be read. Values range from 00H to 5FH.
Bit D7 (MSB) is not used and its value is undefined when read.

7.43 RAM read address pointer (08H; read/write)

The RAM read address pointer is automatically incremented after reading a data byte via the RAM output register.

It can be accessed for writing as well as reading.

The values range from 00H to 5FH. When at 5FH a read operation will cause wrapping around to 00H. Bit D7 (MSB) is not used; it is ignored when written and undefined when read.

7.44 RAM data output register (09H; read)

The RAM data output register contains the byte addressed by the RAM read address pointer. It can only be read, each read operation causing an increment of the RAM read address pointer.

7.45 EEPROM access

The EEPROM is intended for storage of user addresses (RICs), sync words and special programmed function (SPF) bits representing the decoder configuration.

The EEPROM can store 48 bytes of information and is organized as a matrix of 8 rows by 6 columns.
The EEPROM is accessed indirectly via an address pointer and a data I/O register.

The EEPROM is protected against inadvertent writing by means of the programming enable bit in the control register (bit D1).

The EEPROM memory map is non-contiguous as can be seen in Fig.10, which shows both the EEPROM organization and the access method.

Identifier locations contain RICs or sync words. A total of 20 unassigned bytes is available for general purpose storage.

7.46 EEPROM address pointer (07H; read/write)

An EEPROM location is addressed via the EEPROM address pointer. It is incremented automatically each time a byte is read or written via the EEPROM data I/O register.

The EEPROM address pointer contains two counters, for the row and the column number. Bits D2 to D0 contain the column number (0 to 5) and bits D5 to D3 the row number (0 to 7). Bits D7 and D6 of the address pointer are not used. Data written to these bits will be ignored, while their values are undefined when read.

The column and row counters are connected in series. Upon overflow of the column counter (column = 5) the row counter is automatically incremented and the column counter wraps to 0. On overflow the row counter wraps from 7 to 0.

7.47 EEPROM data I/O register (0AH; read/write)

The byte addressed by the EEPROM address pointer can be written or read via the EEPROM Data I/O register. Each access automatically increments the EEPROM address pointer.

7.48 EEPROM access limitations

Since the EEPROM address pointer is used during data decoding, the EEPROM may not be accessed while the receiver is active (RXE = 1). It is advised to switch to OFF state before accessing the EEPROM.

The EEPROM cannot be written unless the EEPROM programming enable bit (bit D1) in the control register is set.

For writing a minimum supply voltage V_{PG} is required (2.0 V typ.). The supply current needed during writing (I_{PG}) will be ≈500 μA.

Any modified SPF settings (bytes 0 to 3) only take effect after a decoder reset. Modified identifiers are active immediately.

7.49 EEPROM read operation

EEPROM read operations must start at a valid address in the non-contiguous memory map. Single-byte or block reads are permitted.

7.50 EEPROM write operation

EEPROM write operations must always take place in blocks of 6 bytes, starting at the beginning of a row. Programming a single byte will reset the other bytes in the same row. Modifying a single byte in a row requires re-writing the unchanged bytes with their old contents.

After writing each block a pause of maximum 7.5 ms is required to complete the programming operation internally. During this time the external microcontroller may generate an I²C-bus stop condition. If another I²C-bus transfer is started the decoder will pull SCL LOW during this pause.

After writing the EEPROM programming enable bit (D1) in the control register must be reset.

7.51 Invalid write address

When an invalid write address is used, the column counter bits (D2 to D0) are forced to zero before being loaded into the address pointer. The row counter bits are used normally.

7.52 Incomplete programming sequence

A programming sequence may be aborted by an I²C-bus stop condition. Next, the EEPROM programming enable bit (D1) in the control register must be reset.

Any bytes received of the last 6-byte block will be ignored and the contents of this (incomplete) EEPROM block will remain unchanged.

7.53 Unused EEPROM locations

A total of 20 EEPROM bytes is available for general purpose storage (see Table 19).

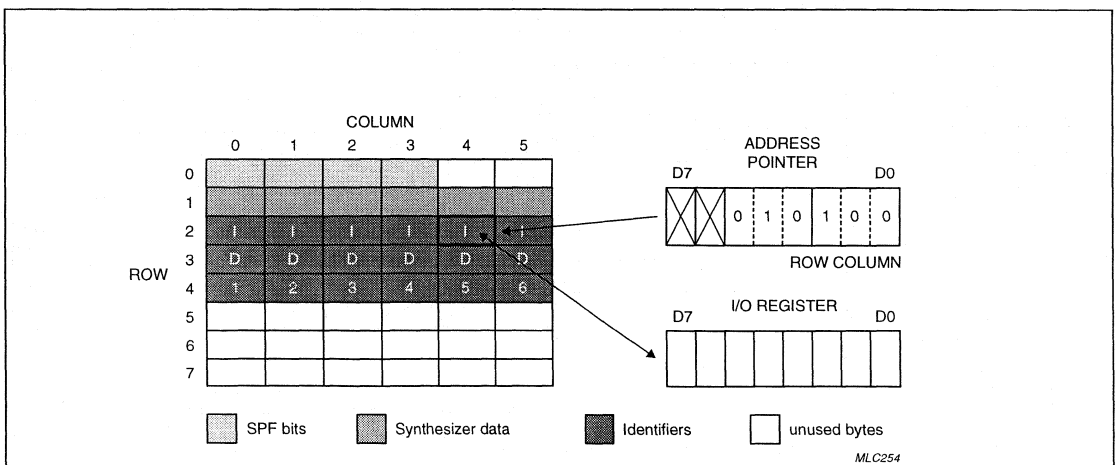


Fig.10 EEPROM organization and access.

Table 19 Unused EEPROM addresses

ROW	HEX
0	04 and 05[1]
5	28 to 2D
6	30 to 35
7	38 to 3D

Note

1. When using bytes 04H and 05H, care must be taken to preserve the SPF information stored in bytes 00H to 03H.

7.54 Special programmed function allocation

The SPF bit allocation in the EEPROM is shown in Tables 20 to 24. The SPF bits are located in row 0 of the EEPROM and occupy 4 bytes.

Bytes 04H and 05H are not used and are available for general purpose storage.

The contents of SPF (bytes 0 to 3) are read into the associated logic only when the decoder is reset (HIGH level in input RST).

Table 20 Special Programmed Functions (EEPROM address 00H)

BIT (MSB: D7)	VALUE	DESCRIPTION
D0	X	reserved for future use; logic 0 when read
D1	X	reserved for future use
D2	X	reserved for future use
D3	X	reserved for future use
D4	X	reserved for future use
D5	X	reserved for future use
D6	X	reserved for future use; logic 0 when read
D7	1	received data inversion enabled

Table 21 Special Programmed Functions (EEPROM address 01H)

BIT (MSB: D7)	VALUE	DESCRIPTION
D1 and D0	0 0	5 ms receiver establishment time (nominal); note 1
	0 1	10 ms
	1 0	15 ms
	1 1	30 ms
D3 and D2	0 0	20 ms oscillator establishment time (nominal); note 1
	0 1	30 ms
	1 0	40 ms
	1 1	50 ms
D5 and D4	0 0	512 bits/s received bit rate
	0 1	1024 bits/s (not used in POCSAG)
	1 0	1200 bits/s
	1 1	2400 bits/s
D6	1	synthesizer interface enabled (data is output via ZSD, ZSC and ZLE at decoder switch-on)
D7	1	voltage converter enabled

Note

1. Since the exact establishment time is related to the programmed bit rate, Table 22 shows the values for the various bit rates.

Table 22 Establishment time as a function of bit rate

NOMINAL ESTABLISHMENT TIME	ACTUAL ESTABLISHMENT TIME			
	512 bits/s	1024 bits/s	1200 bits/s	2400 bits/s
5 ms	5.9 ms (3 bits)	5.9 ms (6 bits)	5.0 ms (6 bits)	5.0 ms (12 bits)
10 ms	11.7 ms (6 bits)	11.7 ms (12 bits)	10.0 ms (12 bits)	10.0 ms (24 bits)
15 ms	15.6 ms (8 bits)	15.6 ms (16 bits)	16.7 ms (20 bits)	16.7 ms (40 bits)
20 ms	23.4 ms (12 bits)	23.4 ms (24 bits)	20.0 ms (24 bits)	20.0 ms (48 bits)
30 ms	31.2 ms (16 bits)	31.2 ms (32 bits)	26.7 ms (32 bits)	26.7 ms (64 bits)
40 ms	39.1 ms (20 bits)	39.1 ms (40 bits)	40.0 ms (48 bits)	40.0 ms (96 bits)
50 ms	46.9 ms (24 bits)	46.9 ms (48 bits)	53.3 ms (64 bits)	53.3 ms (128 bits)

Table 23 Special Programmed Functions (EEPROM address 02H)

BIT (MSB: D7)	VALUE	DESCRIPTION
D0	X	not used
D1	X	not used
D3 and D2	0 0	32768 Hz real time clock reference
	0 1	50 Hz square-wave
	1 0	2 Hz
	1 1	$1/60$ Hz
D4	1	signal test mode enabled (REF and INT outputs)
D5	0	burst error correction enabled
D7 and D6	X X	reserved for future use

Table 24 Special Programmed Functions (EEPROM address 03H)

BIT (MSB: D7)	VALUE	DESCRIPTION
D1 and D0	0 0	2048 Hz acoustic alerter frequency
	0 1	2731 Hz
	1 0	4096 Hz
	1 1	3200 Hz
D2	1	automatic POCSAG alert generation enabled
D3	X	not used
D4	X	not used
D5	X	not used
D6	0	INT output polarity: active LOW
	1	INT output polarity: active HIGH
D7	X	not used

7.55 Synthesizer programming data

Data for programming a PLL synthesizer via pins ZSD, ZSC and ZLE can be stored in row 1 of the EEPROM. Six bytes are available starting from address 08H.

Data is transferred in two serial blocks of 24 bits each, starting with bit 0 (MSB) of block 1. Any unused bits must be programmed at the beginning of a block.

7.56 Identifier storage allocation

Up to 6 different identifiers can be stored in EEPROM for matching with incoming data. The PCD5003 can distinguish two types of identifiers:

- User addresses (RIC)
- User Programmable Sync Words (UPSW).

Identifiers are stored in EEPROM rows 2, 3 and 4. Each identifier location consists of 3 bytes in the same column. The identifier number is equal to the column number + 1.

Only the last 4 identifiers (numbers 3 to 6) can be programmed as a UPSW. Identifiers 1 and 2 always represent RICs. A UPSW represents an unused address and must differ by more than 6 bits from preamble to guarantee detection.

The standard POCSAG sync word is always enabled and has identifier number 7.

Table 26 shows the memory locations of the 6 identifiers. The bit allocation per identifier is given in Table 27.

Table 25 Synthesizer programming data (EEPROM address 08H to 0DH)

ADDRESS (HEX)	BIT (MSB: D7)	DESCRIPTION
08	D7 to D0	bits 0 to 7 of data block 1 (bit 0 is MSB)
09	D7 to D0	bits 8 to 15
0A	D7 to D0	bits 16 to 23
0B	D7 to D0	bits 0 to 7 of data block 2 (bit 0 is MSB)
0C	D7 to D0	bits 8 to 15
0D	D7 to D0	bits 16 to 23

Table 26 Identifier storage allocation (EEPROM address 10H to 25 H)

ADDRESS (HEX)	BYTE	DESCRIPTION
10 to 15	1	identifier number 1 to 6
18 to 1D	2	identifier number 1 to 6
20 to 25	3	identifier number 1 to 6

Table 27 Identifier bit allocation

BYTE	BIT (MSB: D7)	DESCRIPTION
1	D7 to D0	bits 2 to 9 of POCSAG codeword (RIC or UPSW); notes 1 and 2
2	D7 to D0	bits 10 to 17
3	D7 and D6	bits 18 and 19
	D5	frame number bit FR3 (RIC); note 3
	D4	frame number bit FR2 (RIC)
	D3	frame number bit FR1 (RIC)
	D2	identifier type selection (0 = UPSW, 1 = RIC); note 4
	D1	identifier enable (1 = enabled)
	D0	reserved for future use, logic 0 when read

Notes

1. The bit numbering corresponds with the numbering in a POCSAG codeword: bit 1 is the flag bit (0 = address, 1 = message).
2. A UPSW needs 18 bits to be matched for successful identification. Bit 1 (MSB) must be logic 0; bits 2 to 19 contain the identifier bit pattern; they are followed by 2 predetermined random (function) bits and the UPSW is completed by 10 CRC error correction bits and an even-parity bit.
3. Bits FR3 to FR1 (MSB: FR3) contain the 3 least significant bits of the 21-bit RIC.
4. Identifiers 1 and 2 (RIC only) will be disabled by programming bit D2 as logic 0.

7.57 Voltage doubler

An on-chip voltage doubler provides an unregulated DC output for supplying an LCD or a low power microcontroller on output V_{PO}. An external ceramic capacitor of typical 100 nF is required between pins CCN and CCP. The voltage doubler is enabled via SPF programming.

7.58 Level-shifted interface

All interface lines are suited for communication with a microcontroller operating from a higher supply voltage. The external device must have a common reference at V_{SS} of the PCD5003.

The reference voltage for the level-shifted interface must be applied to input V_{PR}. This could be the on-chip voltage doubler output V_{PO} if required. When the microcontroller has a separate (regulated) supply this separate supply voltage should be connected to V_{PR}.

The level-shifted interface lines are: RST, DON, ALC, REF, INT.

The I^2C-bus interface lines SDA and SCL can be level-shifted independently of V_{PR} by means of the standard external pull-up resistors.

7.59 Signal test mode

A special 'signal test' mode is available for monitoring the performance of a receiver circuit together with the front-end of the PCD5003.

For this purpose the output of the digital noise filter and the recovered bit clock are made available at outputs REF and INT respectively. All synchronization and decoding functions are normally active.

The 'signal test' mode is activated/deactivated by SPF programming.

8 OPERATING INSTRUCTIONS

8.1 Reset conditions

When the PCD5003 is reset by applying a HIGH-level on input RST, the condition of the decoder is as follows:

- OFF status (irrespective of DON input level)
- REF output frequency 32768 Hz
- All internal counters reset
- Status/control register reset
- INT output at LOW-level
- No alert transducers selected
- LED, VIB and ATH outputs at LOW level
- ATL output high impedance
- SDA, SCL inputs high impedance
- Voltage converter disabled.

Within t_{RSU} after release of the reset condition (RST LOW) the programmed functions are activated. The settings affecting the external operation of the PCD5003 are as follows:

- REF output frequency
- Voltage converter
- INT output polarity
- Signal test mode.

When input DON is HIGH, the decoder starts operating in ON status immediately following t_{RSU}.

8.2 Power-on reset circuit

During power-up of the PCD5003 a HIGH level of minimum duration t_{RST} = 50 µs must be applied to pin RST. This is to prevent EEPROM corruption which might otherwise occur because of the undefined contents of the Control register.

The reset signal can be applied by the external microcontroller or by an RC power-on reset circuit on pin RST (C to V_{PR}, R to V_{SS}). Such an RC-circuit should have a time constant of at least $3t_{RST}$ = 150 µs.

Input RST has an internal high-ohmic pull-down resistor (nominal 2 MΩ at 2.5 V supply) which could be used together with a suitable external capacitor connected to V_{PR} to create a power-on reset signal. However, since this pull-down resistor varies considerably with processing and supply voltage, the resulting time constant is inaccurate.

A more accurate reset duration can be realised with an additional external resistor connected to V_{SS}. Recommended minimum values in this case are C = 2.2 nF and R = 100 kΩ (see Fig.15).

8.3 Reset timing

The start-up time for the crystal oscillator may exceed 1 second (typ. 800 ms). It is advised to apply a reset condition at least during the first part of this period. The minimum reset pulse duration t_{RST} is 50 µs.

During reset the oscillator is active, but clock signals are inhibited internally. Once the reset condition is released the end of the oscillator start-up period can be detected by a rising edge on output INT.

During a reset the voltage converter clock (V_{clk}) is held at zero. The resulting output voltage drop may cause problems when the external resetting device is powered by the internal voltage doubler. A sufficiently large buffer capacitor between output V_{PO} and V_{SS} must be provided to supply the microcontroller during reset. The voltage at V_{PO} will not drop below V_{DD} – 0.7 V.

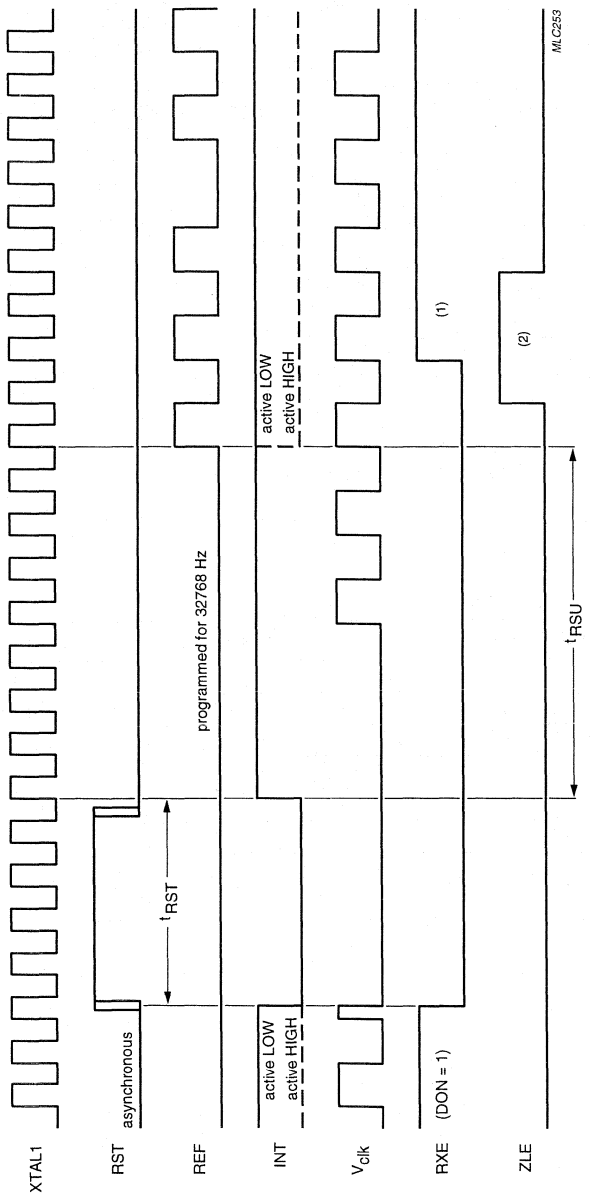
Immediately after a reset all programmable internal functions will start operating according to a programmed value of 0. During the first 8 full clock cycles (t_{RSU}) all programmed values are loaded from EEPROM.

After reset the receiver outputs RXE and ROE become active immediately, if DON is HIGH and the synthesizer is disabled. When the synthesizer is enabled, RXE and ROE will only become active after the second pulse on ZLE completes the loading of synthesizer data.

The full reset timing is shown in Fig.11. The start-up timing including synthesizer programming is given in Fig.12.

8.4 Initial programming

A newly-delivered PCD5002 has EEPROM contents which are undefined. The EEPROM should therefore be programmed, followed by a reset to activate the SPF settings, before any attempt is made to use the device.



(1) The RXE output signal is shown for disabled synthesizer. When the synthesizer is enabled RXE is held off until after the second pulse on ZLE (programming complete).

(2) The ZLE output signal is shown for enabled synthesizer and DON = 1. When DON = 0 output ZLE remains HIGH until ON state is entered (DON = 1 or control register bit D4 = 1).

Fig.11 Reset timing.

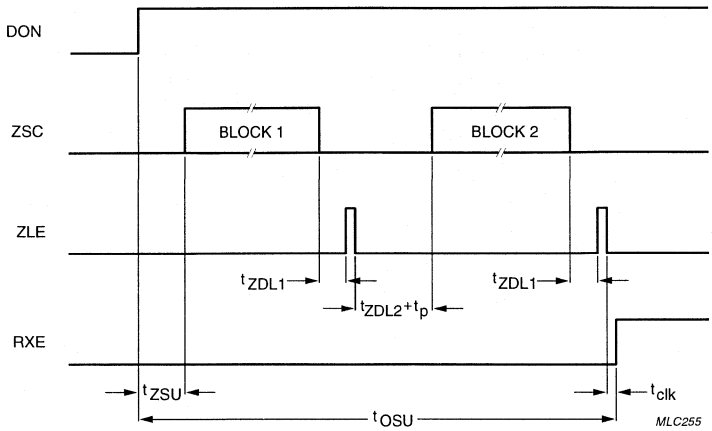


Fig.12 Start-up timing including synthesizer programming.

9 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		−0.5	+7.0	V
V_{PR}	external reference voltage input	$V_{PR} \geq V_{DD} - 0.8$ V	−0.5	+7.0	V
V_n	voltage on pins ALC, DON, RST, SDA and SCL	$V_n \leq 7.0$ V	$V_{SS} - 0.8$	$V_{PR} + 0.8$	V
V_{n1}	voltage on any other pin	$V_{n1} \leq 7.0$ V	$V_{SS} - 0.8$	$V_{DD} + 0.8$	V
P_{tot}	total power dissipation		–	250	mW
P_O	power dissipation per output		–	100	mW
T_{amb}	operating ambient temperature		−25	+70	°C
T_{stg}	storage temperature		−55	+125	°C

10 DC CHARACTERISTICS

V_{DD} = 2.7 V; V_{PR} = 2.7 V; V_{SS} = 0 V; T_{amb} = −25 to +70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage	voltage converter disabled	1.5	2.7	6.0	V
V_{PR}	external reference voltage input	$V_{PR} \geq V_{DD} - 0.8$ V	1.5	2.7	6.0	V
I_{DD0}	supply current (OFF)	note 1	–	25.0	40.0	µA
I_{DD1}	supply current (ON)	note 1; DON = V_{DD}	–	50.0	80.0	µA
V_{PG}	programming supply voltage	voltage converter disabled	2.0	–	6.0	V
		voltage converter enabled	2.0	–	3.0	V
I_{PG}	programming supply current		–	–	800	µA
Inputs						
V_{IL}	LOW level input voltage					
	RDI, BAT		V_{SS}	–	$0.3V_{DD}$	V
	DON, ALC, RST		V_{SS}	–	$0.3V_{PR}$	V
	SDA, SCL		V_{SS}	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage					
	RDI, BAT		$0.7V_{DD}$	–	V_{DD}	V
	DON, ALC, RST		$0.7V_{PR}$	–	V_{PR}	V
	SDA, SCL		$0.7V_{DD}$	–	V_{PR}	V
I_{IL}	LOW level input current pins RDI, BAT,TS1, TS2, DON, ALC and RST	T_{amb} = 25 °C; $V_I = V_{SS}$	0	–	−0.5	µA
I_{IH}	HIGH level input current	T_{amb} = 25 °C				
	TS1, TS2	$V_I = V_{DD}$	6	–	20	µA
	RDI, BAT	$V_I = V_{DD}$; RXE = 0	6	–	20	µA
	RDI, BAT	$V_I = V_{DD}$; RXE = 1	0	–	0.5	µA
	DON, ALC, RST	$V_I = V_{PR}$	250	500	850	nA
Outputs						
I_{OL}	LOW level output current	T_{amb} = 25 °C				
	VIB, LED	V_{OL} = 0.3 V	80	–	–	µA
	ATH	V_{OL} = 0.3 V	250	–	–	µA
	INT, REF	V_{OL} = 0.3 V	80	–	–	µA
	ZSD, ZSC, ZLE	V_{OL} = 0.3 V	70	–	–	µA
	ATL	V_{OL} = 1.2 V; note 2	13	27	55	mA
	ROE, RXE	V_{OL} = 0.3 V	80	–	–	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{OH}	HIGH level output current	T_{amb} = 25 °C				
	VIB, LED	V_{OH} = 0.7 V	−0.6	–	−2.4	mA
	ATH	V_{OH} = 0.7 V	−3.0	–	−11.0	mA
	INT, REF	V_{OH} = 2.4 V	−80	–	–	µA
	ZSD, ZSC, ZLE	V_{OH} = 2.4 V	−60	–	–	µA
	ATL	ATL high-impedance; note 3	–	–	−0.5	µA
	ROE, RXE	V_{OH} = 2.4 V	−600	–	–	µA

Notes

1. Inputs: SDA and SCL pulled up to V_{DD}; all other inputs connected to V_{SS}.
   Outputs: RXE and ROE logic 0; REF: f_{ref} = 1/60 Hz; all other outputs open-circuit.
   Oscillator: no crystal; external clock f_{osc} = 76800 Hz; amplitude: V_{SS} to V_{DD}.
   Voltage convertor disabled (SPF byte 01, bit D7 = 0; see Table 21).
2. Maximum output current is subject to absolute maximum ratings per output (see Chapter 9).
3. When ATL (open drain output) is not activated it is high impedance.

11 DC CHARACTERISTICS (WITH VOLTAGE CONVERTER)

V_{DD} = 2.7 V; V_{SS} = 0 V; V_{PR} = V_{PO}; T_{amb} = −25 to +70 °C; C_s = 100 nF; voltage converter enabled.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		1.5	–	3.0	V
$V_{PO(0)}$	output voltage; no load	V_{DD} = 2.7; I_{PO} = 0	–	5.4	–	V
V_{PO}	output voltage	V_{DD} = 2.0 V; I_{PO} = −250 µA	3.0	3.5	–	V
I_{PO}	output current	V_{DD} = 2.0 V; V_{PO} = 2.7 V	−400	−650	–	µA
		V_{DD} = 3.0 V; V_{PO} = 4.5 V	−650	−900	–	µA

12 OSCILLATOR CHARACTERISTICS

Quartz crystal type: MX-1V or equivalent.
Quartz crystal parameters: f = 76 800 Hz; $R_{S(max)}$ = 35 kΩ; C_L = 8 pF; C_0 = 1.4 pF; C_1 = 1.5 fF.
Maximum overall tolerance: ±200 × 10^{-6} (includes: cutting, temperature, aging).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{XO}	output capacitance XTAL2		–	10	–	pF
g_m	oscillator transconductance	V_{DD} = 1.5 V	6	12	–	µS

13 EEPROM CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
N_{EW}	erase/write cycles		1000	10000	–	
t_{DR}	data retention time	T_{amb} = +70 °C; note 1	10	–	–	years

Note

1. Retention cannot be guaranteed for naked dies (PCD5003U/10).

14 AC CHARACTERISTICS

V_{DD} = 2.7 V; V_{SS} = 0 V; V_{PR} = 2.7 V; T_{amb} = 25 °C;. f_{osc} = 76800 Hz.

SYMBOLS	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
System clock						
T_{clk}	system clock period	f_{osc} = 76800 Hz	–	13.02	–	µs
Call alert frequencies						
f_{AL}	alert frequency	SPF byte 03H; bits:				
		D1, D0 = 0 0	–	2048	–	Hz
		D1, D0 = 0 1	–	2731	–	Hz
		D1, D0 = 1 0	–	3200	–	Hz
		D1, D0 = 1 1	–	4096	–	Hz
f_{AW}	warbled alert; modulation frequency	alert set-up bit D2 = 1; outputs ATL, ATH, LED	–	16	–	Hz
f_{AWH}	warbled alert; high acoustic alert frequency	alert set-up bit D2 = 1; outputs ATL, ATH	–	f_{AL}	–	Hz
f_{AWL}	warbled alert; low acoustic alert frequency	alert set-up bit D2 = 1; outputs ATL, ATH	–	$\frac{1}{2}f_{AL}$	–	Hz
f_{VBP}	pulsed vibrator frequency (square-wave)	low-level alert	–	25	–	Hz
Call alert duration						
t_{ALT}	alert time-out period		–	16	–	s
t_{ALL}	ATL output time-out period	low-level alert	–	4	–	s
t_{ALH}	ATH output time-out period	high-level alert	–	12	–	s
t_{VBL}	VIB output time-out period	low -level alert	–	4	–	s
t_{VBH}	VIB output time-out period	high-level alert	–	12	–	s
t_{ALC}	alert cycle period		–	1	–	s
t_{ALP}	alert pulse duration		–	125	–	ms
Real time clock reference						
f_{ref}	real time clock reference frequency	SPF byte 02H; bits:				
		D3, D2 = 0 0; note 1	–	32768	–	Hz
		D3, D2 = 0 1; note 2	–	50	–	Hz
		D3, D2 = 1 0	–	2	–	Hz
		D3, D2 = 1 1	–	$\frac{1}{60}$	–	Hz
t_{RFP}	real time clock reference pulse duration	all reference frequencies except 50 Hz (square-wave)	–	13.02	–	µs

SYMBOLS	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Receiver control						
t_{RXT}	RXE, ROE transition time	C_L = 5 pF	–	100	–	ns
t_{RXON}	RXE establishment time (nominal values: actual duration is bit rate dependent, see Table 22)	SPF byte 01H; bits:				
		D1, D0 = 0 0	–	5	–	ms
		D1, D0 = 0 1	–	10	–	ms
		D1, D0 = 1 0	–	15	–	ms
		D1, D0 = 1 1	–	30	–	ms
t_{ROON}	ROE establishment time (nominal values: actual duration is bit rate dependent, see Table 22)	SPF byte 01H; bits:				
		D3, D2 = 0 0	–	20	–	ms
		D3, D2 = 0 1	–	30	–	ms
		D3, D2 = 1 0	–	40	–	ms
		D3, D2 = 1 1	–	50	–	ms
I²C-bus interface						
f_{SCL}	SCL clock frequency		0	–	400	kHz
t_{LOW}	SCL clock low period		1.3	–	–	µs
t_{HIGH}	SCL clock HIGH period		0.6	–	–	µs
$t_{SU;DAT}$	data set-up time		100	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	–	ns
t_r	SDA, SCL rise time		–	–	300	ns
t_f	SDA, SCL fall time		note 3	–	300	ns
C_B	capacitive bus line load		–	–	400	pF
$t_{SU;STA}$	START condition set-up time		0.6	–	–	µs
$t_{HD;STA}$	START condition hold time		0.6	–	–	µs
$t_{SU;STO}$	STOP condition set-up time		0.6	–	–	µs
Reset						
t_{RST}	external reset duration		50	–	–	µs
t_{RSU}	set-up time after reset	oscillator running	–	–	105	µs
t_{OSU}	set-up time after switch-on	oscillator running	–	–	4	ms
Data input						
t_{TDI}	data input transition time	see Fig.13	–	–	100	µs
t_{DI1}	data input logic 1 duration	see Fig.13	t_{BIT}	–	∞	
t_{DI0}	data input logic 0 duration	see Fig.13	t_{BIT}	–	∞	
POCSAG data timing (512 bits/s)						
f_{DI}	data input rate	SPF byte 01H; bits D5, D4 = 0 0	–	512	–	bits/s
t_{BIT}	bit duration		–	1.9531	–	ms
t_{CW}	codeword duration		–	62.5	–	ms
t_{PA}	preamble duration		1125	–	–	ms
t_{BAT}	batch duration		–	1062.5	–	ms

SYMBOLS	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
POCSAG data timing (1200 bits/s)						
f_{DI}	data input rate	SPF byte 01H; bits D5, D4 = 1 0	–	1200	–	bits/s
t_{BIT}	bit duration		–	833.3	–	µs
t_{CW}	codeword duration		–	26.7	–	ms
t_{PA}	preamble duration		480	–	–	ms
t_{BAT}	batch duration		–	453.3	–	ms
POCSAG data timing (2400 bits/s)						
f_{DI}	data input rate	SPF byte 01H; bits D5, D4 = 1 1	–	2400	–	bits/s
t_{BIT}	bit duration		–	416.6	–	µs
t_{CW}	codeword duration		–	13.3	–	ms
t_{PA}	preamble duration		240	–	–	ms
t_{BAT}	batch duration		–	226.6	–	ms
Synthesizer control						
t_{ZSU}	synthesizer set-up duration	oscillator running; note 4	1	–	2	bits
f_{ZSC}	output clock frequency	note 5	–	38400	–	Hz
t_{ZCL}	clock pulse duration		–	13.02	–	µs
t_{ZSD}	data bit duration	note 5	–	26.04	–	µs
t_{ZDS}	data bit set-up time		–	13.02	–	µs
t_{ZDL1}	data load enable delay		–	91.15	–	µs
t_{ZLE}	load enable pulse duration		–	13.02	–	µs
t_{ZDL2}	inter block delay		–	117.19	–	µs

Notes

1. 32768 Hz reference signal: 32 pulses per 75 clock cycles, alternately separated by 1 or 2 pulse periods (pulse duration: t_{RFP}). The timing is shown in Fig.14.
2. 50 Hz reference signal: square-wave.
3. The fall time may be faster than prescribed in the I^2C-bus specification for very low load capacitance values. To increase the fall time external capacitance is required.
4. Duration depends on programmed bit rate; after reset t_{ZSU} = 1.5 bits.
5. Nominal values; pause in 12th data bit (see Table 12).

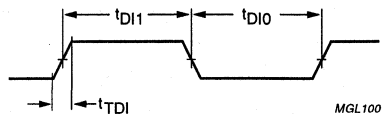


Fig.13 Data input timing.

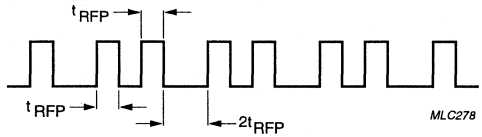
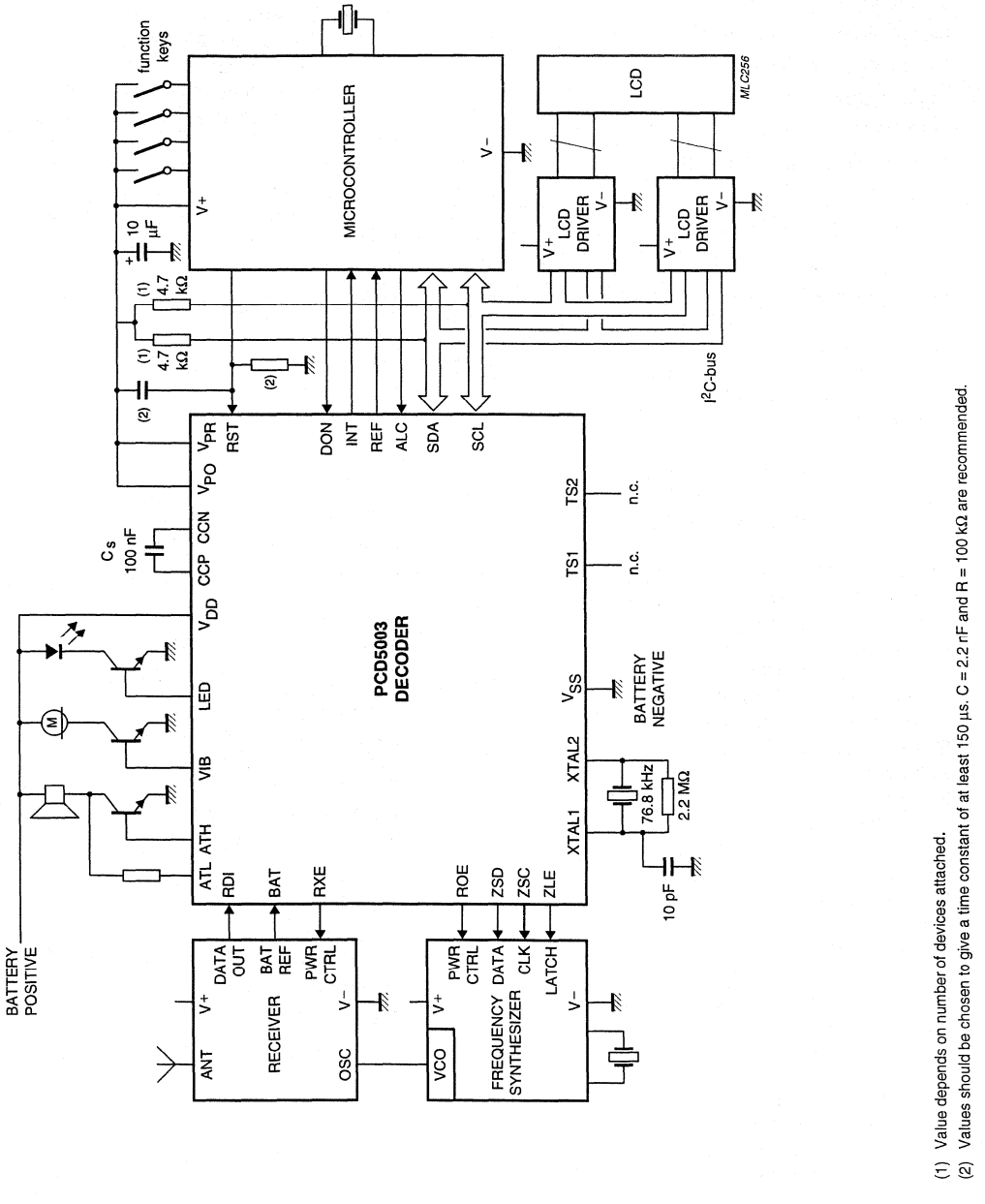


Fig.14 Timing of the 32 768 Hz reference signal.

15 APPLICATION INFORMATION



(1) Value depends on number of devices attached.
(2) Values should be chosen to give a time constant of at least 150 µs. C = 2.2 nF and R = 100 kΩ are recommended.

Fig.15 Typical application example (display pager).

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FLEX™ Pager Decoder PCD5008

1 FEATURES

- FLEX™ paging protocol signal processor
- 16 programmable user address words
- 16 fixed temporary addresses
- 1600, 3200 and 6400 bit/s decoding
- Any-phase or single-phase decoding
- Uses standard serial peripheral interface (SPI) in slave mode
- Allows low current power-down mode operation of host processor
- Highly programmable receiver control
- Real-time clock time base
- FLEX™ fragmentation and group messaging support
- Real-time clock over-the-air update support
- Compatible with synthesized receivers
- Low battery indication (external detector)
- Low cost LQFP32 plastic package
- Operates using a 76.8 kHz crystal
- Very low power consumption
- Operates at low supply voltage.

2 APPLICATIONS

- Numeric FLEX™ pagers
- Alphanumeric FLEX™ pagers
- Remote metering
- Car security systems
- Personal digital assistants.

3 GENERAL DESCRIPTION

This data sheet describes the operation of the PCD5008 integrated paging decoder. It is fully compatible with the Motorola FLEXchip™ IC.

The PCD5008, also referred to as the decoder, simplifies implementation of a FLEX™ paging device, by being able to interface with several off-the-shelf paging receivers and host microcontrollers/processors. Its primary function is to process information received and demodulated from a FLEX™ radio paging channel, select messages addressed to the paging device and communicate the message information to the host.

Motorola FLEXstack™ software, installed on the product host processor, communicates with the PCD5008 and interprets the codewords that are passed to the host.

The PCD5008 operates the paging receiver in an efficient power consumption mode and enables the host to operate in a low-power mode when no message is being received.

4 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		1.8	2.2	3.6	V
I_{DD}	supply current	see Sections 10 and 12	–	6.8	–	µA
T_{amb}	operating ambient temperature		−25	+25	+70	°C
f_{EXTAL}	clock frequency		–	76.8	–	kHz

5 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD5008H	LQFP32	plastic low profile quad flat package; 32 leads; body 7 × 7 × 1.4 mm	SOT358-1

6 BLOCK DIAGRAM

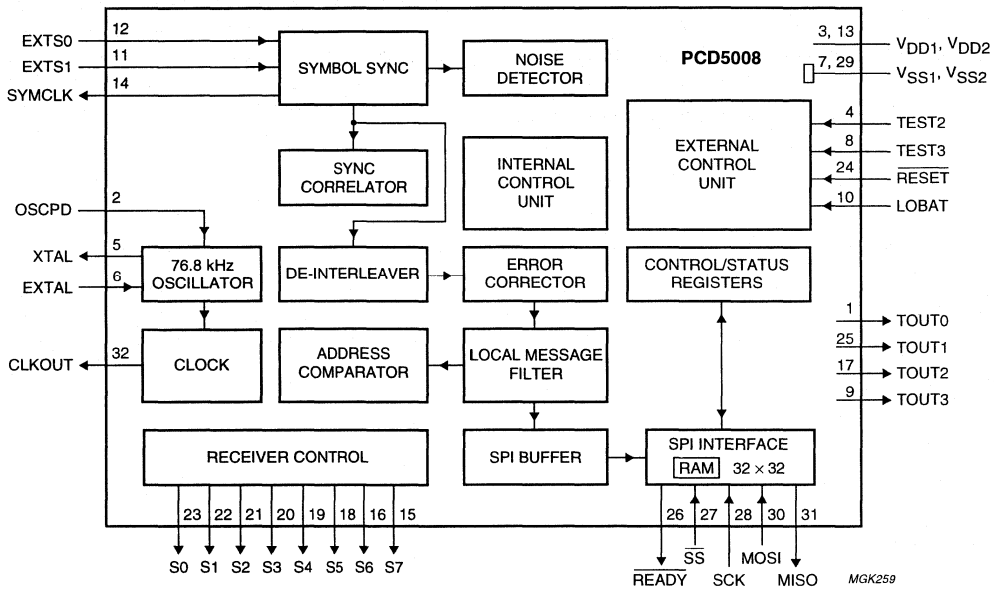

Fig.1 Functional block diagram for PCD5008 pager decoder.

7 PINNING

SYMBOL	PIN	I/O	DESCRIPTION
TOUT0	1	O	3-state test output; note 1
OSCPD	2	I	internal oscillator power-down; connected to V_{SS} when using the internal oscillator, connected to V_{DD} when using an external source
V_{DD1}	3	–	supply voltage, internally connected to V_{DD2}
TEST2	4	I	manufacturing test mode input pin; has to be connected to V_{SS}
XTAL	5	O	76.8 kHz crystal oscillator output
EXTAL	6	I	76.8 kHz crystal oscillator input or external clock input
V_{SS1}	7	–	ground supply, internally connected to V_{SS2}
TEST3	8	I	manufacturing test mode input pin; has to be connected to V_{SS}
TOUT3	9	O	3-state test output; note 1
LOBAT	10	I	low battery voltage detect input
EXTS1	11	I	most significant bit (MSB) of the symbol currently being decoded
EXTS0	12	I	least significant bit (LSB) of the symbol currently being decoded
V_{DD2}	13	–	supply voltage, internally connected to V_{DD1}
SYMCLK	14	O	recovered symbol clock output
S7	15	O	receiver control output port, 3-state
S6	16	O	receiver control output port, 3-state
TOUT2	17	O	3-state test output; note 1
S5	18	O	receiver control output port, 3-state
S4	19	O	receiver control output port, 3-state
S3	20	O	receiver control output port, 3-state
S2	21	O	receiver control output port, 3-state
S1	22	O	receiver control output port, 3-state
S0	23	O	receiver control output port, 3-state
$\overline{\text{RESET}}$	24	I	active LOW reset input
TOUT1	25	O	3-state test output; note 1
$\overline{\text{READY}}$	26	O	output driven LOW when the PCD5008 is ready for an SPI packet
$\overline{\text{SS}}$	27	I	slave select input for SPI communications
SCK	28	I	serial clock input for SPI communications
V_{SS2}	29	–	ground supply, internally connected to V_{SS1}
MOSI	30	I	data input for SPI communications
MISO	31	O	data output for SPI communications (3-state)
CLKOUT	32	O	38.4 kHz clock output (derived from 76.8 kHz oscillator)

Note

1. These test outputs may be either left unconnected or connected to V_{SS} in the application.

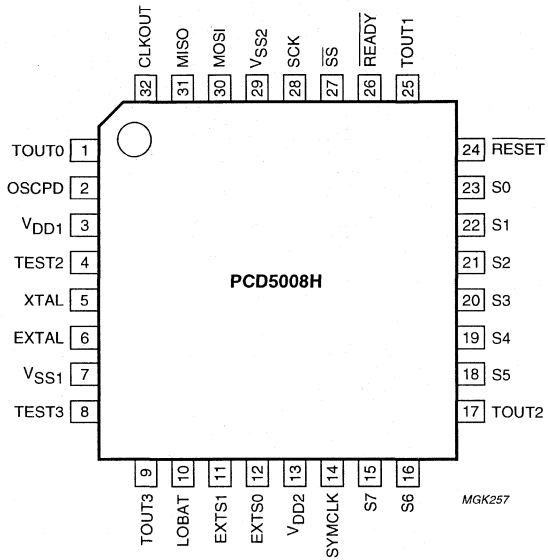

Fig.2 Pin configuration.

8 FUNCTIONAL DESCRIPTION

8.1 General

The PCD5008 simplifies implementation of a FLEX™ paging device by interfacing with off-the-shelf components such as a paging receiver and a microcontroller or microprocessor (called a host). The PCD5008 is fully compatible with FLEXstack™ software which provides a complete, platform independent, software driver for the PCD5008.

The PCD5008 fully supports all non-roaming aspects of the FLEX™ protocol (version G1.8), and can operate in either single-phase or any-phase mode. The PCD5008 supports FLEX™ dynamic grouping, allowing up to 16 temporary addresses to be enabled simultaneously. It is also capable of retrieving real time information from a FLEX™ channel.

The PCD5008 connects to any receiver capable of providing a 2-bit digital signal. The PCD5008 operates the paging receiver in an efficient power consumption mode. The PCD5008 has 8 receiver control lines used for warming up, operating and shutting down a receiver in stages.

The PCD5008 has the ability to detect a battery-low signal from an external detector during the receiver control sequences.

The PCD5008 carries out the following functions:

- Synchronises to a FLEX™ data stream
- Processes received, demodulated information
- Performs de-interleaving and error correction
- Selects calls addressed to the paging device using up to 16 programmable addresses
- Communicates the message information to the host.

The PCD5008 interfaces to a host through a serial peripheral interface (SPI). The host can then interpret the message information in an appropriate manner (numeric, alphanumeric, binary, etc.). This function is provided by the FLEXstack™ software.

The PCD5008 enables the host to operate in a low power mode when no message information for the paging device is being received. It has a 38.4 kHz clock output capable of driving other devices, and has a 1-minute timer that offers low-power support for a real-time clock function on the host. The host can use receiver control lines which are not required by the receiver as expansion ports to control other peripheral devices.

8.2 Clocking, reset and start-up

8.2.1 Oscillator

The PCD5008 uses an inverting crystal oscillator. The clock signal for the internal circuitry is derived from the oscillator input pin EXTAL through a Schmitt trigger buffer. Alternatively, an external clock signal can be fed in at input pin EXTAL, in this case the internal oscillator can be disabled by pulling the OSCPD input pin HIGH. This reduces current consumption. When using a crystal, an external feedback resistor and the load capacitances need to be connected to pins EXTAL and XTAL (Fig.18). See Section 12 for the recommended crystal parameters and the specification of the oscillator transconductance to guarantee correct start-up.

8.2.2 Reset and start-up conditions

The PCD5008 is reset by pulling the $\overline{\text{RESET}}$ input LOW. After releasing the $\overline{\text{RESET}}$ by pulling it HIGH, the PCD5008 counts 76800 clock cycles (typically 1 second) before pulling $\overline{\text{READY}}$ LOW to indicate that the decoder is ready for configuration via the SPI.

See Fig.3 and Section 11 for the PCD5008 timing specifications when power is applied.

See Fig.4 and Section 11 for the PCD5008 timing specifications when it is reset.

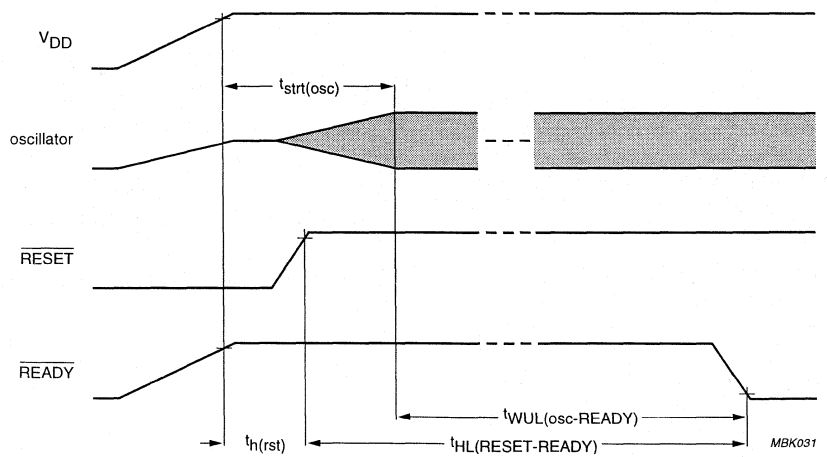

Fig.3 Start-up timing.

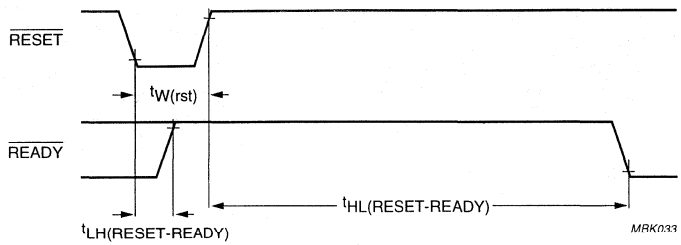

Fig.4 Reset timing.

8.3 Serial peripheral interface (SPI)

8.3.1 General

All data communication between the PCD5008 and the host is done via the SPI using 32-bit data packets at data rates up to 1 Mbit/s. SPI transfers are full-duplex and can be initiated by either the host which acts as the SPI master providing the data clock for packet transfer, or the PCD5008 as an SPI slave.

The host can send packets to configure or control the PCD5008 or a checksum packet to validate SPI communication (Section 8.4.2). The PCD5008 buffers data packets, relating to received data, into a 32 packet transmit buffer. The PCD5008 can send either a status packet, a part ID packet, or packets from the transmit buffer. In the event of a buffer overflow, the PCD5008 stops decoding and clears the transmit buffer.

8.3.2 SPI interconnect

Connection on the PCD5008 consists of a $\overline{\text{READY}}$ pin and 4 SPI pins ($\overline{\text{SS}}$, SCK, MOSI and MISO):

$\overline{\text{READY}}$: output signal; indicates that data is available from the PCD5008

$\overline{\text{SS}}$: SPI select; used as PCD5008 chip select

SCK: serial clock; output from the host used for clocking data

MOSI: master output slave input; data output from the host

MISO: master input slave output; data output from the PCD5008.

8.3.3 SPI TRANSFER INITIATED BY THE HOST

The following steps occur when the host initiates an SPI packet transfer, see Fig.5 for event timings:

1. The host selects the PCD5008 by driving the $\overline{SS}$ pin LOW.
2. The PCD5008 indicates that it is ready to start the SPI transfer by driving the $\overline{READY}$ pin LOW.
3. The host clocks each of the 32 bits of the SPI packet by pulsing SCK. Both the host and the PCD5008 sample data on the rising edge of SCK. Packets are sent MSB first.
4. The PCD5008 pulls the $\overline{READY}$ line HIGH, to indicate that the transfer is complete.
5. The host waits until the $\overline{READY}$ line is pulled HIGH, then de-selects the PCD5008 SPI by driving the $\overline{SS}$ pin HIGH.
6. The first 5 steps are repeated for each additional packet.

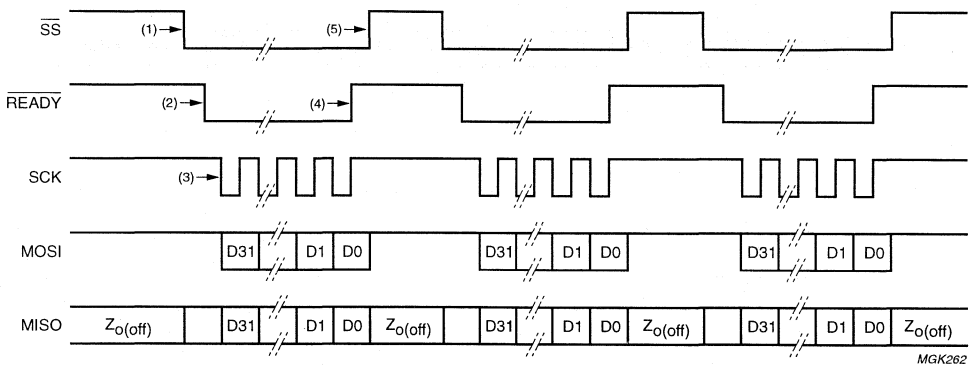

Fig.5 Typical multiple SPI transfers initiated by the host.

8.3.4 SPI TRANSFER INITIATED BY THE DECODER

The following steps occur when the PCD5008 initiates an SPI packet transfer, see Fig.6 for event timings:

1. The PCD5008 initiates the SPI transfer by driving the $\overline{READY}$ pin LOW.
2. If the PCD5008 is not already selected, the host selects the PCD5008 SPI by driving the $\overline{SS}$ pin LOW.
3. The host clocks each of the 32 bits of the SPI packet by pulsing SCK. Both the host and the PCD5008 sample data on the rising edge of SCK. Packets are sent MSB first.
4. The PCD5008 pulls the $\overline{READY}$ line HIGH, to indicate that the transfer is complete.
5. The host may then either de-select the SPI interface of the PCD5008 (Fig.7) by driving the $\overline{SS}$ pin HIGH or maintain $\overline{SS}$ LOW to continue sending packets to the PCD5008.

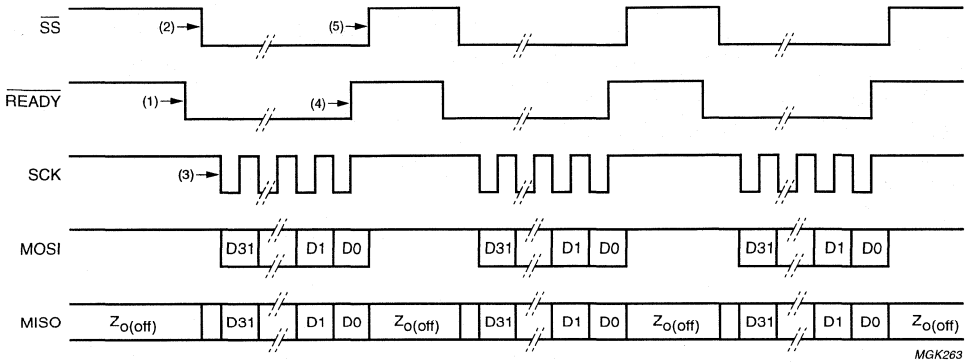

Fig.6 Typical multiple SPI transfers initiated by the PCD5008.

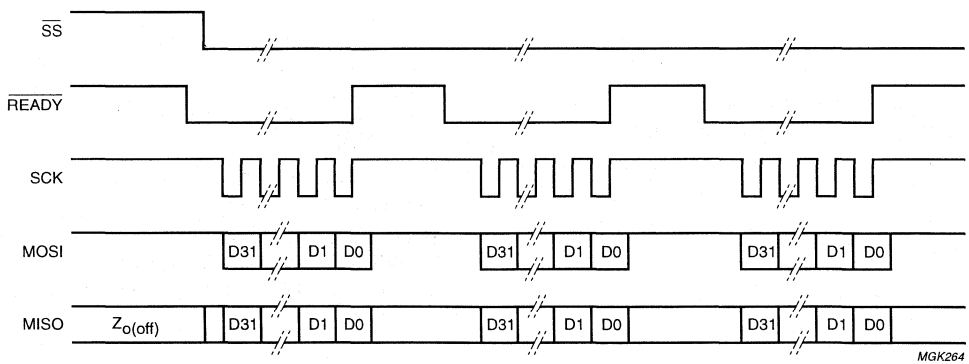

Fig.7 Multiple SPI transfers initiated by the PCD5008 with $\overline{SS}$ maintained LOW.

8.3.5 SPI PACKET FORMAT

SPI data packets consist of an 8-bit ID (byte 3), followed by 24 bits of information (byte 2 to byte 0). See Table 1, note that bit 7 of byte 3 is the first bit on the bus.

8.3.6 SPI TIMING

See Fig.8 and Section 11 for the timing specifications of the SPI.

Table 1 Packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	D31	D30	D29	D28	D27	D26	D25	D24
2	D23	D22	D21	D20	D19	D18	D17	D16
1	D15	D14	D13	D12	D11	D10	D9	D8
0	D7	D6	D5	D4	D3	D2	D1	D0

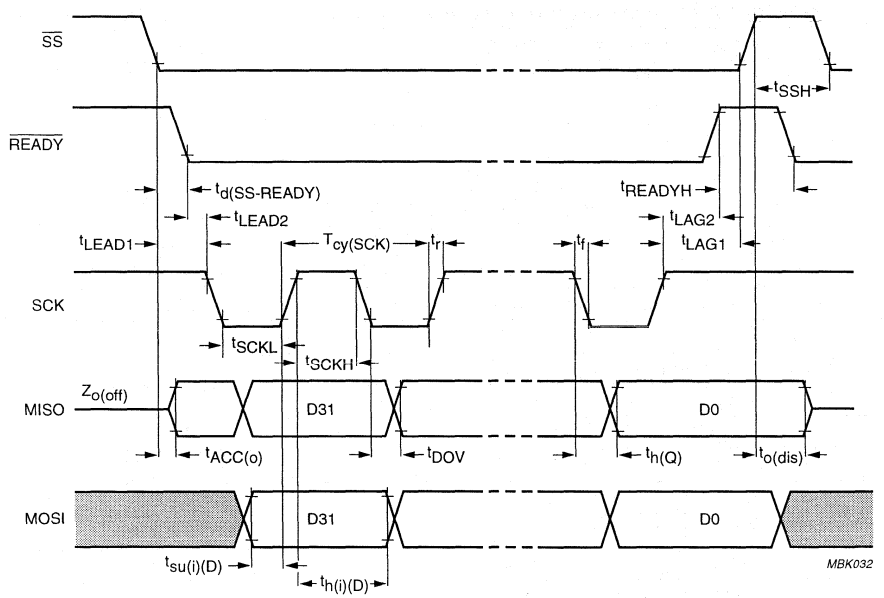

Fig.8 SPI timing.

8.3.7 HOST-TO-DECODER PACKETS OVERVIEW

This section summarises the packets which can be sent from the host to the decoder.

Table 2 Host-to-decoder packet ID map

PACKET		
ID (HEX)	**TYPE**	**SECTION**
00	checksum	8.4.6
01	configuration	8.4.4
02	control	8.4.7
03	all frame mode	8.8.3
04 to 0E	reserved (host should never send)	–
0F	receiver line control	8.5.7
10	receiver control configuration (off setting)	8.5.4
11	receiver control configuration (warm-up 1 setting)	8.5.5.3
12	receiver control configuration (warm-up 2 setting)	8.5.5.3
13	receiver control configuration (warm-up 3 setting)	8.5.5.3
14	receiver control configuration (warm-up 4 setting)	8.5.5.3
15	receiver control configuration (warm-up 5 setting)	8.5.5.3
16	receiver control configuration (3200 sps sync. setting)	8.5.6.2
17	receiver control configuration (1600 sps sync. setting)	8.5.6.2
18	receiver control configuration (3200 sps data setting)	8.5.6.2
19	receiver control configuration (1600 sps data setting)	8.5.6.2
1A	receiver control configuration (shut-down 1 setting)	8.5.8.1
1B	receiver control configuration (shut-down 2 setting)	8.5.8.1
1C to 1F	special (ignored by decoder)	–
20	frame assignment (frames 112 to 127)	8.6.7
21	frame assignment (frames 96 to 111)	8.6.7
22	frame assignment (frames 80 to 95)	8.6.7
23	frame assignment (frames 64 to 79)	8.6.7
24	frame assignment (frames 48 to 63)	8.6.7
25	frame assignment (frames 32 to 47)	8.6.7
26	frame assignment (frames 16 to 31)	8.6.7
27	frame assignment (frames 0 to 15)	8.6.7
28 to 77	reserved (host should never send)	–
78	user address enable	8.6.6
79 to 7F	reserved (host should never send)	–
80	user address assignment (user address 0)	8.6.6
81	user address assignment (user address 1)	8.6.6
82	user address assignment (user address 2)	8.6.6
83	user address assignment (user address 3)	8.6.6
84	user address assignment (user address 4)	8.6.6
85	user address assignment (user address 5)	8.6.6

PACKET		
ID (HEX)	**TYPE**	**SECTION**
86	user address assignment (user address 6)	8.6.6
87	user address assignment (user address 7)	8.6.6
88	user address assignment (user address 8)	8.6.6
89	user address assignment (user address 9)	8.6.6
8A	user address assignment (user address 10)	8.6.6
8B	user address assignment (user address 11)	8.6.6
8C	user address assignment (user address 12)	8.6.6
8D	user address assignment (user address 13)	8.6.6
8E	user address assignment (user address 14)	8.6.6
8F	user address assignment (user address 15)	8.6.6
90 to FF	reserved (host should never send)	–

8.3.8 DECODER-TO-HOST PACKETS OVERVIEW

This section summarises the packets which can be sent from the PCD5008 to the host (Table 3).

Table 3 Decoder-to-host packet ID map

PACKET		
ID (HEX)	**TYPE**	**SECTION**
00	block information word	8.7.9
01	address	8.7.2
02 to 57	vector or message (ID is word number in frame)	8.7.3, 8.7.8
58 to 7E	reserved	–
7F	status	8.4.9
80 to FE	reserved	–
FF	part ID	8.4.5

8.4 Configuration and synchronisation

8.4.1 GENERAL

After a reset, all configuration data has to be (re)loaded into the PCD5008 by the host using the SPI. PCD5008 features which do not change during operation are configured using the configuration packet (Section 8.4.4), the receiver control packets (Section 8.5) and the address configuration packets (Section 8.6). PCD5008 features which can be changed during operation are configured using the control packet. The checksum packet ensures proper communication between the host and the PCD5008.

8.4.2 SPI SECURITY ALGORITHM

The PCD5008 provides a security algorithm to verify correct SPI operation (Figs 9 and 10). The PCD5008 maintains a checksum register equal to the result of XORing the 24 data bits of every packet it receives, except the checksum packet 00H and special packets 1CH to 1FH. When the PCD5008 is reset, the internal checksum register is initialized to the 24 bit part ID defined in the part ID packet.

Immediately following a reset and whenever the host sends a packet other than a checksum packet, the SPI output of status and data (SPI transmit) is disabled. The PCD5008 then initiates SPI transfers continuously, sending the part ID packet (Section 8.4.5). Note that when SPI transmit is disabled all decoding and timing functions are unaffected. The SPI transmit can be enabled by sending a checksum packet for which the checksum value matches the checksum register.

Any checksum packets sent when the SPI transmit is enabled, are ignored by the PCD5008 irrespective of the value of the checksum packet data bits. Thus when the PCD5008 initiates an SPI transfer and the host has no data to send, the host should send the checksum packet so as not to disable the SPI transmit. The data in the checksum packet could be a null packet (32 bit stream of all zeros).

Sending a packet other than the checksum packet when the SPI transmit is enabled causes the SPI transmit to be disabled until a checksum packet is sent with the correct value. Thus when the host re-configures the PCD5008 after a reset, the SPI transmit is disabled until the host sends a checksum packet at the end of the configuration data, with the checksum value equal to the result of XORing together the data bits of each of the configuring packets and the data bits of the part ID packet.

If the SPI transmit is enabled and there is data in the transmit buffer, the PCD5008 initiates an SPI transfer sending a packet from its transmit buffer. The PCD5008 sends the status packet (which is not buffered) when the host initiates an SPI transfer and the transmit buffer is empty.

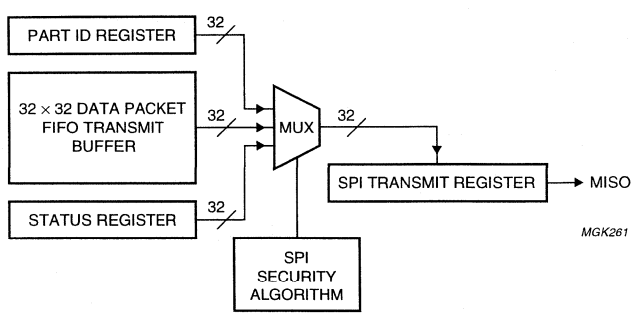

Fig.9 SPI transmit functional block diagram.

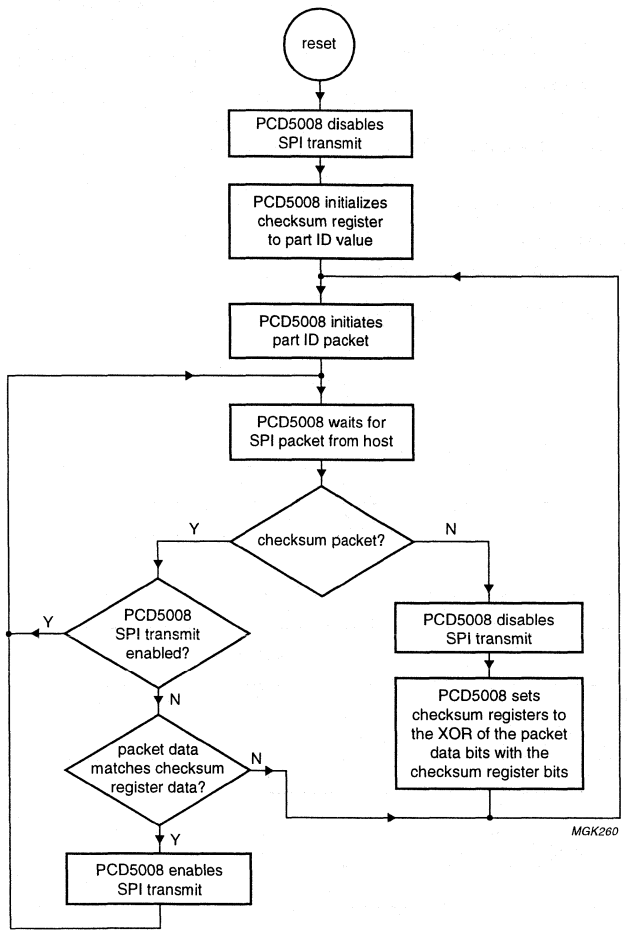

Fig.10 SPI security algorithm.

8.4.3 CONFIGURATION SEQUENCE

A typical configuration and synchronisation sequence would be as follows, see Fig.11 for event timings:

1. The PCD5008 is reset by the host.
2. After 1 second the PCD5008 interrupts the host to read the part ID by pulling the $\overline{\text{READY}}$ line LOW.
3. The host pulls $\overline{\text{SS}}$ LOW at the start of each SPI transfer and clocks out the part ID data.
4. The host configures the following aspects of PCD5008 operation:
   a) General configuration (Section 8.4.4)
   b) Receiver operation (Section 8.5)
   c) FLEX™ CAPCODE configuration (Section 8.6).

   The PCD5008 writes a part ID packet in response to each incoming packet.
5. At the end of each packet the PCD5008 pulls the $\overline{\text{READY}}$ line HIGH, and then LOW again to indicate that packet processing is complete.
6. The host writes a control packet to enable FLEX™ decoding in the PCD5008 (Section 8.4.7).
7. The host writes a checksum packet to enable SPI data output by the PCD5008 (Section 8.4.2).
8. On recognising a SYNC word, the PCD5008 synchronises to the channel.
9. The PCD5008 initiates an SPI transfer writing the status packet, indicating that it is now in synchronous mode.

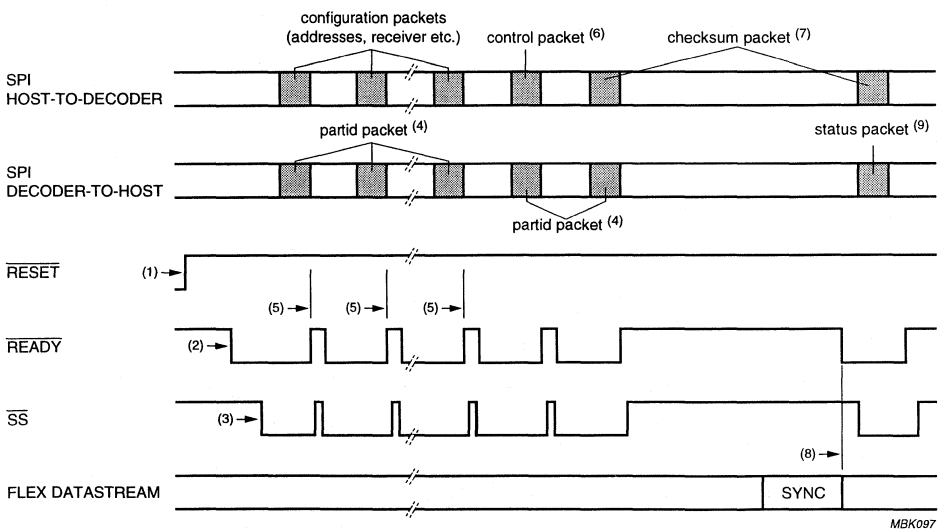

Fig.11 Typical configuration and synchronisation sequence.

8.4.4 CONFIGURATION PACKET (ID = 01H)

The configuration packet defines a number of different configuration options for the PCD5008. The PCD5008 ignores this packet when decoding is enabled, i.e. the ON bit in the control packet is set (Table 11).

OFD: oscillator frequency difference (Tables 4 and 5). These bits represent the maximum frequency difference between the 76.8 kHz oscillator (accounting for ageing, temperature variation, manufacturing tolerance etc.) and the worst case transmitter bit rate (specified in FLEX™ as ±25 parts per million (ppm), see Section 16.3.1). For example, if the transmitter tolerance is ±25 ppm and the 76.8 kHz oscillator tolerance is ±140 ppm, the transmitter-oscillator frequency difference is ±165 ppm and OFD should be cleared (300 ppm max.). Value after reset = 0. Note that configuring a smaller frequency difference in this packet results in lower power consumption due to higher receiver battery save ratios.

SME: synchronous mode enable (Table 5). When this bit is set, a status packet is sent automatically whenever the synchronous mode update (SMU) bit in the status packet is set. This happens whenever a change occurs in the synchronous mode (SM) status bit, which indicates that the decoder is synchronized to a FLEX™ data stream. The host can use the SM bit in the status packet as an in-range/out-of-range indication. Value after reset = 0.

MOT: maximum off time (Table 5). When this bit is set, the PCD5008 assumes that there can be up to 1 minute between transmitted frames on the paging system. When this bit is clear, the PCD5008 assumes that there can be up to 4 minutes between transmitted frames on the paging system. This setting is determined by the service provider. Value after reset = 0.

COD: clock output disable (Table 5). When this bit is clear, a 38.4 kHz signal is output on the CLKOUT pin. When this bit is set, the CLKOUT pin is driven HIGH. Note that setting and clearing this bit can cause pulses on the CLKOUT pin that are less than one half the 38.4 kHz period. Also note that when the clock output is enabled, the CLKOUT pin always outputs the 38.4 kHz signal even when the PCD5008 is in reset. Value after reset = 0.

MTE: minute timer enable (Table 5). When this bit is set, a status packet is sent at one minute intervals with the minute time-out (MT) bit in the status packet set. When this bit is clear, the internal 1-minute timer stops counting. See Section 8.4.8 for details of 1-minute timer operation. Value after reset = 0.

LBP: low battery polarity (Table 5). This bit defines the polarity of the PCD5008's LOBAT pin: When this bit is set, a HIGH at input LOBAT represents a low battery condition. The LB bit in the status packet is initialized to the inverse (i.e. inactive) value of the LBP bit when the PCD5008 is turned on (by setting the ON bit in the control packet). When the PCD5008 is turned on, the first low battery update in the status packet is sent to the host when a low battery condition is detected on the LOBAT pin. Value after reset = 0.

SP: signal polarity (Tables 5, 6 and 7). These bits set the polarity of EXTS1 and EXTS0 input signals. The polarity of the EXTS1 and EXTS0 bits is determined by the receiver design. Value after reset = 0.

Table 4 Maximum oscillator frequency difference

OFD_1	OFD_0	FREQUENCY DIFFERENCE (ppm)
0	0	±300
0	1	±150
1	0	±75
1	1	±0

Table 5 Configuration packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	OFD_1	OFD_0
1	0	0	0	0	0	0	SP_1	SP_0
0	SME	MOT	COD	MTE	LBP	0	0	0

Table 6 Input signal polarity

SP_1	SP_0	SIGNAL POLARITY	
		EXTS1	EXTS0
0	0	normal	normal
0	1	normal	inverted
1	0	inverted	normal
1	1	inverted	inverted

Table 7 FLEX™ 4 level FSK modulation selection

EXTS1	EXTS0	FSK MODULATION AT SP = 0,0 (Hz)
1	0	+4800
1	1	+1600
0	1	−1600
0	0	−4800

8.4.5 PART ID PACKET (ID = FFH)

The part ID packet is output by the PCD5008 SPI whenever the SPI transmit is disabled due to the checksum feature.

MDL: model (Table 8). The PCD5008 model value is 0.

CID: compatibility ID (Table 8). This value describes other parts with the same model number, which are compatible with this part. The PCD5008 compatibility value is 1. Devices which implement a superset of PCD5008 functionality have MDL cleared and CID_0 set.

REV: revision (Table 8). This identifies the manufacturing version of the PCD5008. For the PCD5008 the value is 6. Compatible parts have values in the range 0 to 5.

8.4.6 CHECKSUM PACKET (ID = 00H)

See Table 9 for checksum packet bit assignment.

CV: checksum value (24 bits), see Section 8.4.2.

Table 8 Part ID packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	1	1	1	1	1	1	1	1
2	MDL_1	MDL_0	CID_{13}	CID_{12}	CID_{11}	CID_{10}	CID_9	CID_8
1	CID_7	CID_6	CID_5	CID_4	CID_3	CID_2	CID_1	CID_0
0	REV_7	REV_6	REV_5	REV_4	REV_3	REV_2	REV_1	REV_0

Table 9 Checksum packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	0	0	0	0	0	0	0
2	CV_{23}	CV_{22}	CV_{21}	CV_{20}	CV_{19}	CV_{18}	CV_{17}	CV_{16}
1	CV_{15}	CV_{14}	CV_{13}	CV_{12}	CV_{11}	CV_{10}	CV_9	CV_8
0	CV_7	CV_6	CV_5	CV_4	CV_3	CV_2	CV_1	CV_0

8.4.7 CONTROL PACKET (ID = 02H)

The control packet defines a number of different control bits for the PCD5008.

FF: force frame 0 to 7 (Table 11). When set, each of these bits forces the PCD5008 to decode one of the FLEX™ frames 0 to 7 irrespective of the system collapse value (for details of collapse values see Section 8.6.2). For example, if the system collapse causes the PCD5008 to decode frames 0, 32, 64 and 96, setting FF_2 causes the PCD5008 to also decode FLEX™ frame 2. This may be used to acquire transmitted time information. Value after reset = 0.

SPM: single phase mode (Table 11). When this bit is set, the PCD5008 decodes only one of the transmitted phases. When this bit is clear, the PCD5008 decodes all transmitted phases. This value is determined by the CAPCODE (Section 8.6). A change to this bit while the PCD5008 is on does not take effect until the next block 0 of a frame. Value after reset = 0.

PS: phase select (Tables 10 and 11). When the SPM bit is set, these bits define which phase the PCD5008 shall decode. This value is determined by the CAPCODE (Section 8.6). A change to these bits, while the PCD5008 is on, does not take effect until the next block 0 of a frame. Value after reset = 0.

Table 10 Phase selection (PS bits)

PS_1	PS_0	DECODED PHASE (BASED ON FLEX™ DATA RATE)		
		1600 bit/s	3200 bit/s	6400 bit/s
0	0	A	A	A
0	1	A	A	B
1	0	A	C	C
1	1	A	C	D

SBI: send block information words (BIW) 2 to 4 (Table 11). When this bit is set, BIWs with time and date information and BIWs received in error are sent to the host, (Section 8.7.9). Value after reset = 0.

MTC: minute timer clear (Table 11). Setting this bit causes the 1-minute timer to restart from 0 (Section 8.4.8).

ON: turn on decoder (Table 11). When this bit is set, the PCD5008 decodes FLEX™ signals. If this bit is cleared, signal processing stops. However, to assure proper operation, the PCD5008 requires that it be set into asynchronous mode when turned off. To achieve that the following sequence must be used:

1. Send control packet with ON bit clear (decoder off)
2. Send control packet with ON bit set (decoder on)
3. Send control packet with ON bit clear (decoder off).

Timing between these steps is specified below and is measured from the positive edge of the last clock of one packet to the positive edge of the last clock of the next packet.

- The minimum time between steps 1 and 2 is the greater of 2 ms or the programmed shut-down time.
  The programmed shut-down time is the sum of all of the times programmed in the used receiver shut-down settings packets.
- There is no maximum time between steps 1 and 2
- The minimum time between steps 2 and 3 is 2 ms
- The maximum time between steps 2 and 3 is the programmed warm-up time minus 2 ms.
  The programmed warm-up time is the sum of all the times programmed in the used receiver warm-up settings packets.

8.4.8 OPERATING THE 1-MINUTE TIMER

The PCD5008 provides a 1-minute timer which allows the host to implement a time-of-day function while maintaining low-power operation. The 1-minute timer is enabled using the MTE bit in the configuration packet (Section 8.4.4). When the 1-minute timer is enabled, a status packet is sent at 1-minute intervals with the MT bit set (Section 8.4.9). When the MTE bit is clear, the internal 1-minute timer stops counting. When the host sends a control packet with MTC bit set, the 1-minute timer restarts from 0. This allows accurate setting of a time-of-day function.

Table 11 Control packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	0	0	0	0	0	1	0
2	FF_7	FF_6	FF_5	FF_4	FF_3	FF_2	FF_1	FF_0
1	0	SPM	PS_1	PS_0	0	0	0	0
0	0	SBI	0	MTC	0	0	0	ON

8.4.9 STATUS PACKET (ID = 7FH)

The status packet contains various types of information that the host may require and is sent to the host:

- Whenever the PCD5008 is polled and has no other data to send
- On events for which the PCD5008 is configured to send the status packet (Sections 8.4.4 and 8.4.7). In this case, the PCD5008 prompts the host to read a status packet for the following conditions:
  - SMU bit in the status packet and the SME bit in the configuration packet are set
  - MT bit in the status packet and the MTE bit in the configuration packet are set
  - EOF bit in the status packet is set
  - LBU bit in the status packet is set
  - BOE bit in the status packet is set.

FIV: frame information valid (Table 12). This bit is set, when a valid frame information word has been received since becoming synchronous to the system and the f and c fields contain valid values. If this bit is clear, no valid frame information words have been received since the PCD5008 became synchronous to the system. This value changes from 0 to 1 at the end of block 0 (Fig.17) of the frame in which the first frame information word was properly received. It is cleared when the PCD5008 goes into asynchronous mode (see SM bit below). This bit is initialized to 0 when the PCD5008 is reset and when the PCD5008 is turned off by clearing the ON bit in the control packet.

f: current frame number (Table 12). This value is updated every frame regardless of whether the PCD5008 needs to decode the frame. This value changes to its proper value for a frame at the end of block 0 of the frame. The value of these bits is not guaranteed when FIV is 0.

c: current system cycle number (Table 12). This value is updated every frame regardless of whether the PCD5008 needs to decode the frame. This value changes to its proper value for a frame at the end of block 0 of the frame. The value of these bits is not guaranteed when FIV is 0.

SM: synchronous mode (Table 12). This bit is set, when the PCD5008 is synchronous to the system.
The PCD5008 sets this bit when the first synchronization words are received. It clears this bit when synchronisation to the FLEX™ signal is lost. This bit is initialized to 0 when the PCD5008 is reset and when it is turned off by clearing the ON bit in the control packet.

SMU: synchronous mode update (Table 12). This bit is set if the SM bit has been updated in this packet. After the PCD5008 has been turned on, this bit is set when the first synchronization words are found (SM changes to 1) or when the first synchronization search period (meaning the receiver is active during this time) expires (SM stays 0), after the PCD5008 is turned on. The latter condition gives the host the option of assuming the paging device is in range when it is turned on, and displaying out-of-range only after the initial search period expires. After the initial synchronous mode update, the SMU bit is set whenever the PCD5008 switches from/to synchronous mode. The bit is cleared when read. Changes in the SM bit due to turning off the PCD5008 does not set the SMU bit. This bit is initialized to 0 when the PCD5008 is reset.

LB: low battery (Table 12). Set to the value last read from the LOBAT pin. The host controls when the LOBAT pin is read via the receiver control packets. This bit is initialized to 0 at reset. It is also initialized to the inverse of the LBP bit in the configuration packet, when the PCD5008 is turned on, by setting the ON bit in the control packet.

LBU: low battery update (Table 12). This bit is set if the value on two consecutive reads of the LOBAT pin yielded different results. The bit is cleared when read. The host controls when the LOBAT pin is read via the receiver control packets. Changes in the LB bit due to turning on the PCD5008 do not cause the LBU bit to be set. This bit is initialized to 0 when the PCD5008 is reset.

MT: minute time-out (Table 12). Set if one minute has elapsed. The bit is cleared when read. This bit is initialized to 0 when the PCD5008 is reset.

EOF: end of frame (Table 12). Set when the PCD5008 is in all frame mode (AFM) (Section 8.8.3), and the end of the frame has been reached. The PCD5008 is in the AFM if the AFM enable counter is non-zero, if any temporary address enabled (TAE) counter is non-zero (Section 8.8.3) or if the FAF bit in the AFM packet is set. The bit is cleared when read and initialized to 0 when the PCD5008 is reset.

BOE: buffer overflow error (Table 12). Set when information has been lost owing to slow host response time. When the PCD5008 detects that its SPI transmit buffer has overflowed, it clears the transmit buffer, turns off decoding by clearing the ON bit in the control packet, and sets this bit. The bit is cleared when read. This bit is initialized to 0 when the PCD5008 is reset.

x: unused bits (Table 12). The value of these bits is not guaranteed.

8.5 Receiver control interface

8.5.1 General

The PCD5008 has 8 programmable receiver control lines, S0 to S7. The host can program via SPI packets what setting is applied to the receiver control lines, the duration of warm-up and shut-down stages and the polling of the LOBAT pin. This programmability allows the PCD5008 to interface with many off-the-shelf receiver ICs. Note that these packets are ignored when sent while decoding is enabled (ON bit is set in the control packet).

8.5.2 Low battery detection

The PCD5008 can be configured to poll the LOBAT pin at the end of every receiver control setting. This check can be enabled or disabled for each receiver control setting. If the poll is enabled for a setting, the pin is read just before the PCD5008 activates the next setting on the receiver control lines. The PCD5008 sends a status packet whenever the value differs from the previous time that the LOBAT pin was polled.

8.5.3 Receiver settings at reset

The receiver control ports are 3-state outputs which are set to high impedance when the PCD5008 is reset, until the corresponding FRS bit in the receiver line control packet is set or the PCD5008 is turned on for the first time after a reset (by setting the ON bit in the control packet). This allows the designer to force the receiver control lines to the receiver off setting with external pull-up or pull-down resistors before the host can configure these settings in the PCD5008.

8.5.4 Receiver off state (ID = 10H)

The receiver off state is configured by the receiver off setting packet (Table 13), which defines the settings to be applied when the PCD5008 decides to switch the receiver off.

LBC: low battery check (Table 13). If this bit is set, the PCD5008 checks the status of the LOBAT port just before leaving the receiver off state. Value after reset = 0.

CLS: control line setting (Table 13). This is the value to be output on the receiver control lines for the receiver off state. Value after reset = 0.

ST: step time (Table 13). This sets the duration of the warm-up off time. The setting is in steps of 625 µs. Valid values are 625 µs (ST = 01H) to 159.375 ms (ST = FFH). Value after reset = 01H.

Table 12 Status packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	1	1	1	1	1	1	1
2	FIV	f_6	f_5	f_4	f_3	f_2	f_1	f_0
1	SM	LB	x	x	c_3	c_2	c_1	c_0
0	SMU	LBU	x	MT	x	EOF	x	BOE

Table 13 Receiver off setting packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	0	0	1	0	0	0	0
2	0	0	0	0	LBC	0	0	0
1	CLS_7	CLS_6	CLS_5	CLS_4	CLS_3	CLS_2	CLS_1	CLS_0
0	ST_7	ST_6	ST_5	ST_4	ST_3	ST_2	ST_1	ST_0

8.5.5 RECEIVER WARM-UP SEQUENCES

8.5.5.1 Normal receiver warm-up sequence

The PCD5008 allows for up to 6 steps associated with warming up the receiver. When the PCD5008 turns on the receiver while decoding, it starts the warm-up sequence 160 ms before it requires valid signals at the EXTS1 and EXTS0 input pins.

1. The PCD5008 leaves the receiver control lines in the off state for the programmed warm-up off time.
2. The first warm-up setting, if enabled, is applied to the receiver control lines for the amount of time programmed for that setting.
3. Subsequent warm-up settings are applied to the receiver control lines for their corresponding time until a disabled warm-up setting is found.
4. At the end of the last used warm-up setting, the 1600 symbols per second (sps) sync. setting or the 3200 sps sync. setting is applied to the receiver control lines depending on the PCD5008 current state.

The PCD5008 must be configured such that the sum of all of the used warm-up times and the warm-up off time does not exceed 160 ms.

If it exceeds 160 ms, the PCD5008 executes the receiver shut-down sequence 160 ms after the start of the warm-up off time. If the sum of all of the used warm-up times and the warm-up off times is less than 160 ms, the receiver remains in the 1600 sps sync. setting or the 3200 sps sync. setting from the end of the last used warm-up setting until valid signals are expected (160 ms after the start of the warm-up off time). Figure 12 shows the receiver warm-up sequence while decoding, when all warm-up settings are enabled.

8.5.5.2 First receiver warm-up sequence

When the PCD5008 is turned on by setting the ON bit in the control packet, the receiver warm-up sequence differs from the sequence described in Section 8.5.5.1. After the ON bit is set no receiver warm-up off time is applied, instead the PCD5008 immediately begins to apply the receiver warm-up settings. When a disabled warm-up setting is found, the decoder applies 3200 sps sync. setting to the receiver control lines. The decoder then expects valid signals after the 3200 sps sync. warm-up time. Figure 13 shows the receiver warm-up sequence when the PCD5008 is first turned on and when all warm-up settings are enabled.

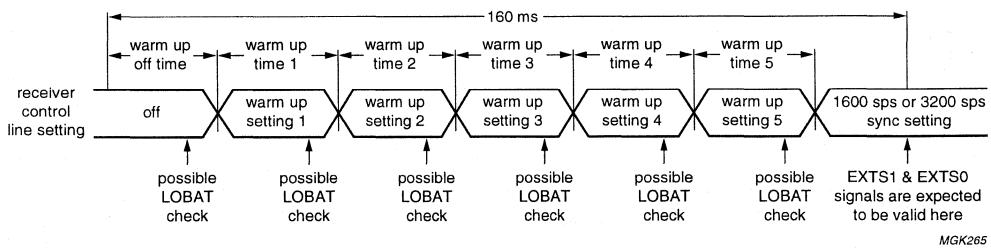

Fig.12 Receiver warm-up sequence while decoding.

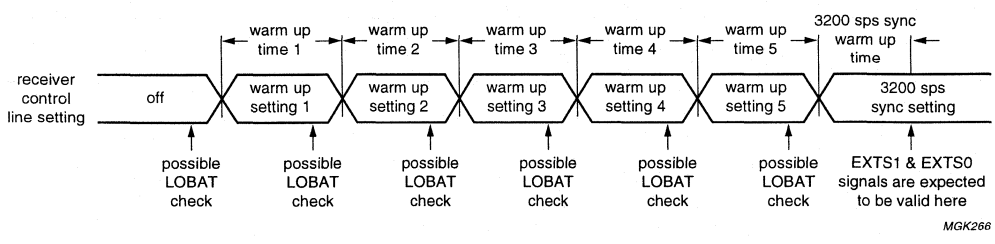

Fig.13 First receiver warm-up sequence after turning decoding on.

8.5.5.3 Receiver warm-up setting packets (ID = 11H to 15H)

CLS: control line setting (Table 15). This is the value to be output on the receiver control lines (S0 to S7) for this receiver warm-up state. Value after reset = 0.

SE: step enable (Table 15). The receiver setting is enabled when the bit is set. If the bit is cleared then that step in the receiver warm-up sequence is disabled and all following steps are ignored. Value after reset = 0.

LBC: low battery check (Table 15). If this bit is set, the PCD5008 checks the status of the LOBAT port just before leaving this receiver warm-up state. Value after reset = 0.

ST: step time (Table 15). This sets the duration time for receiver warm-up until the next receiver state. The setting is in 625 µs steps.
Valid values: 625 µs (ST = 01H) to 79.375 ms (ST = 7FH).
Value after reset = 01H.

s: setting number, see Tables 14 and 15 for the s names and values and location in the receiver warm-up packet.

Table 14 Receiver warm-up setting numbers

s_3	s_2	s_1	s_0	SETTING NAME
0	0	0	1	warm-up 1
0	0	1	0	warm-up 2
0	0	1	1	warm-up 3
0	1	0	0	warm-up 4
0	1	0	1	warm-up 5

Table 15 Receiver warm-up setting packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	0	0	1	s_3	s_2	s_1	s_0
2	SE	0	0	0	LBC	0	0	0
1	CLS_7	CLS_6	CLS_5	CLS_4	CLS_3	CLS_2	CLS_1	CLS_0
0	0	ST_6	ST_5	ST_4	ST_3	ST_2	ST_1	ST_0

8.5.6 ACTIVE RECEIVER STATES

8.5.6.1 General

In addition to the warm-up and shut-down states, the PCD5008 has four active receiver states. When these settings are applied to the receiver control lines, the PCD5008 is decoding the EXTS1 and EXTS0 input signals. The timing of these signals and their duration depends on the FLEX™ data stream. Because of this, there is no time setting associated with these settings (with the exception of the 3200 sps sync. setting).

The four settings are as follows:

1600 sps sync. setting: applied when the PCD5008 searches for a 1600 sps signal.

3200 sps sync. setting: applied when the PCD5008 searches for a 3200 sps signal.

1600 sps data setting: applied after the PCD5008 has found the C or $\overline{C}$ sync. word in the sync 2 section of a 1600 sps frame.

3200 sps data setting: applied after the PCD5008 has found the C or $\overline{C}$ sync. word in the sync 2 section of a 3200 sps frame.

Figure 14 shows some examples of how these settings are used in the PCD5008.

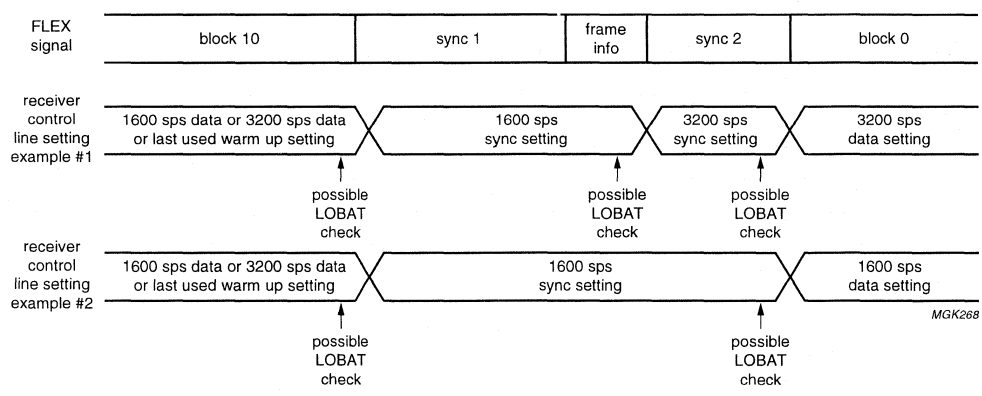

Fig.14 Examples of receiver control transitions.

8.5.6.2 Receiver on setting packets (ID = 16H to 19H)

LBC: low battery check (Table 17). If this bit is set, the PCD5008 checks the status of the LOBAT port just before leaving this receiver sync. setting state. Value after reset = 0.

CLS: control line setting (Table 17). This is the value to be output on the receiver control lines for this receiver sync. setting state. Value after reset = 0.

ST: step time (Table 17). This sets the waiting time, before expecting good signals at EXTS1 and EXTS0 at the end of the warm-up sequence, after turning decoding on. The setting is in steps of 625 µs. Valid values are: 625 µs (ST = 01H) to 79.375 ms (ST = 7FH). Value after reset = 01H.

LBC: low battery check (Table 18). If this bit is set, the PCD5008 checks the status of the LOBAT port just before leaving this receiver on state. Value after reset = 0.

CLS: control line setting (Table 18). This is the value to be output on the receiver control lines (S0 to S7) for this receiver on state. Value after reset = 0.

s: setting number, see Tables 16 and 18 for the s names and values and location in the receiver on setting packet.

Table 16 s names and values

s_3	s_2	s_1	s_0	SETTING NAME
0	1	1	1	1600 sps sync.
1	0	0	0	3200 sps data
1	0	0	1	1600 sps data

8.5.7 FORCING RECEIVER LINES (ID = 0FH)

This packet (Table 19) enables host control over the receiver control line (S0 to S7) settings in all modes except reset. In reset, the receiver control lines are high impedance.

FRS: force receiver setting (Table 19). Setting a bit causes the associated CLS bit in this packet to override the internal receiver control settings on the corresponding receiver control line. Clearing a bit returns control of the corresponding receiver control line to the PCD5008. Value after reset = 0.

CLS: control line setting (Table 19). This bit setting is applied to the corresponding receiver control line if the associated FRS bit is set in this packet. Value after reset = 0.

Table 17 3200 sps sync. setting packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	0	0	1	0	1	1	0
2	0	0	0	0	LBC	0	0	0
1	CLS_7	CLS_6	CLS_5	CLS_4	CLS_3	CLS_2	CLS_1	CLS_0
0	0	ST_6	ST_5	ST_4	ST_3	ST_2	ST_1	ST_0

Table 18 Receiver on setting packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	0	0	1	s_3	s_2	s_1	s_0
2	0	0	0	0	LBC	0	0	0
1	CLS_7	CLS_6	CLS_5	CLS_4	CLS_3	CLS_2	CLS_1	CLS_0
0	0	0	0	0	0	0	0	0

Table 19 Receiver line control packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	0	0	0	1	1	1	1
2	0	0	0	0	0	0	0	0
1	FRS_7	FRS_6	FRS_5	FRS_4	FRS_3	FRS_2	FRS_1	FRS_0
0	CLS_7	CLS_6	CLS_5	CLS_4	CLS_3	CLS_2	CLS_1	CLS_0

8.5.8 RECEIVER SHUT-DOWN SEQUENCE

The PCD5008 allows up to 3 steps associated with shutting down the receiver. When the PCD5008 decides to turn off the receiver, the first shut-down setting, if enabled, is applied to the receiver control lines for the corresponding shut-down time. At the end of the last used shut-down time, the receiver off setting is applied to the receiver control lines. If the first shut-down setting is not enabled, the PCD5008 switches directly from the receiver on to the receiver off setting.

Figure 15 shows the receiver shut-down sequence when all shut-down settings are enabled. If the receiver is on or being warmed up when the decoder is turned off (by clearing the ON bit in the control packet), the PCD5008 immediately executes the receiver shut-down sequence. If the PCD5008 is executing the shut-down sequence when turned on (with the ON bit in the control packet set) the PCD5008 completes the shut-down sequence before starting the warm-up sequence.

8.5.8.1 Receiver shut-down setting packets (ID = 1A to 1BH)

SE: step enable (Table 21). The receiver setting is enabled when the bit is set. If the bit is cleared then that step in the receiver shut-down sequence is disabled and all following steps are ignored. Value after reset = 0.

LBC: low battery check (Table 21). If this bit is set, the PCD5008 checks the status of the LOBAT port just before leaving this receiver shut-down state. Value after reset = 0.

CLS: control line setting (Table 21). This is the value to be output on the receiver control lines (S0 to S7) for this receiver shut-down state. Value after reset = 0.

ST: step time (Table 21). This sets the duration time for receiver shut-down, until the next receiver state. The setting is in steps of 625 µs. Valid values are 625 µs (ST = 01H) to 39.375 ms (ST = 3FH). Value after reset = 01H.

s: setting number, see Tables 20 and 21 for the s names and values and location in the receiver shut-down packet.

Table 20 s names and values

s	SETTING NAME
0	shut-down 1
1	shut-down 2

Table 21 Receiver shut-down stages

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	0	0	1	1	0	1	s
2	SE	0	0	0	LBC	0	0	0
1	CLS_7	CLS_6	CLS_5	CLS_4	CLS_3	CLS_2	CLS_1	CLS_0
0	0	0	ST_5	ST_4	ST_3	ST_2	ST_1	ST_0

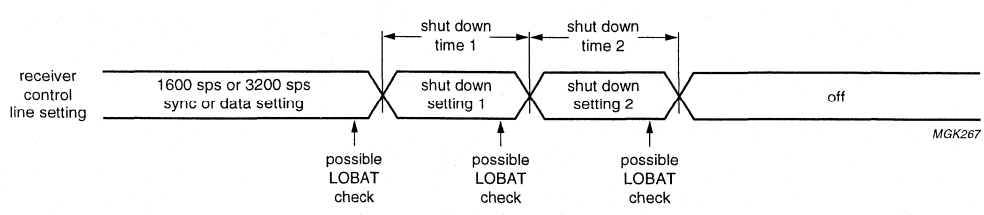

Fig.15 Receiver shut-down sequence.

8.6 Configuration of the FLEX™ CAPCODE

8.6.1 GENERAL

A CAPCODE specifies a decoder address, the collapse value of the address and whether single-phase, any-phase or all-phase address. The PCD5008 supports single-phase and any-phase operation. The FLEX™ protocol provides a standard mechanism to derive phase and frame in which an address should be transmitted. If this mechanism is not used, a CAPCODE also specifies the phase and frame assigned to the address.

8.6.2 CAPCODE FORMAT

The FLEX™ CAPCODE consist of a series of decimal and alphabetic fields, see Fig.16 for the field definitions.

When the FLEX™ standard pager collapse value of 4 (battery cycle of 16 frames) is used, the pager collapse field can be omitted.

The collapse value is a number between 0 and 7 and defines how often the decoding device looks for messages on the FLEX™ channel. For a given collapse value b, the decoding device looks in every 2^b frames. Thus an address with an assigned base frame of 3 and a collapse value of 5 typically looks for messages in frame 3 and every 32 frames thereafter (i.e. frames 3, 35, 67 and 99).

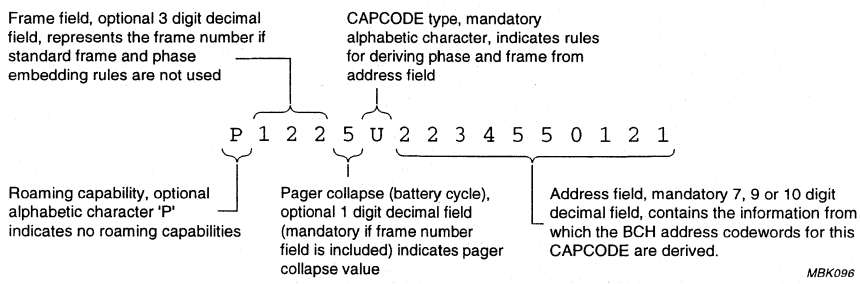

Fig.16 CAPCODE format.

8.6.3 CAPCODE RANGES

A CAPCODE represents user addresses ranging from 1 to 5370810366. A short CAPCODE can have address values below 2031615 and are represented in the data stream by a single address codeword. Some short addresses have been reserved for special purposes: information service addresses, network addresses, temporary (group) addresses and operator messaging addresses. A long CAPCODE represents addresses situated above 2101248 subdivided into categories (uncoordinated, global, country) to allow different allocation schemes to coexist.

Table 22 defines the address usage assignment. All addresses not listed in this table are not defined and reserved for future use.

Table 22 CAPCODE assignment table

CAPCODE ADDRESS VALUE		DESCRIPTION
from	to	
0000000000		illegal
0000000001	0001933312	short addresses
0001933313	0001998848	illegal
0001998849	0002009087	reserved for future use
0002009088	0002025471	Information service addresses
0002025472	0002029567	network addresses
0002029568	0002029583	temporary addresses
0002029584	0002029599	operator messaging addresses
0002029600	0002031614	reserved for future use
0002031615	0002101248	invalid, not used
0002101249	0102101250	long address set 1-2 uncoordinated
0102101251	0402101250	long address set 1-2 country; note 1
0402101251	1075843072	long address set 1-2 global; note 2
1075843073	2149584896	long address set 1-3 global; note 2
2149584897	3223326720	long address set 1-4 global; note 2
3223326721	3923326750	long address set 2-3 country; note 1
3923326751	4280000000	long address set 2-3 reserved
4280000001	4285000000	long address set 2-3 information service, global; notes 2 and 3
4285000001	4290000000	long address set 2-3 information service, country; notes 1 and 3
4290000001	4291000000	long address set 2-3 information service, world-wide; notes 3 and 4
4291000001	4297068542	reserved for future use

Notes

1. Country: the addresses are coordinated within each country and with countries along borders.
2. Global: address is coordinated to be unique world-wide.
3. Information service: currently, the rules governing the use of these addresses are not defined.
4. World-wide: 1000 addresses are assigned to each country for world-wide use.

8.6.4 ADDRESS CALCULATION

Address codeword values generally do not coincide with (part of) the user address as specified in the CAPCODE. To find the address codewords corresponding to a user address a conversion has to be done (Table 24). The type of conversion depends on the CAPCODE range in which the user address is located. Note that addresses are transmitted LSB first (differently to POCSAG).

Short addresses, are transmitted in a single address codeword where as long addresses are transmitted in two consecutive address codewords. The first codeword of a long address contains the lower part of the address, the second codeword the upper part. By combining two long address codewords from different banks 6 long address ranges are created: 1-2, 1-3, 1-4, 2-3, 2-4 and 3-4. Ranges 2-4 and 3-4 are as yet undefined and reserved.

Table 24 describes how to calculate the 21 bit address codeword which is transmitted over the air.

Table 23 Address word range definitions

TYPE	HEX VALUE
Idle word (illegal address)	000000
Long address 1	000001 to 008000
Short address	008001 to 1E0000
Long address 3	1E0001 to 1E8000
Long address 4	1E8001 to 1F0000
Short address (reserved)	1F0001 to 1F27FF
Information service address	1F2800 to 1F67FF
Network address	1F6800 to 1F77FF
Temporary address	1F7800 to 1F780F
Operator messaging address	1F7810 to 1F781F
Short address (reserved)	1F7820 to 1F7FFE
Long address 2	1F7FFF to 1FFFFE
Idle word (illegal address)	1FFFFF

Table 24 Address word calculation

TYPE	LOWER ADDRESS CODEWORD; notes 1, 2 and 4	UPPER ADDRESS CODEWORD; notes 1, 3 and 4
Short address	CAPCODE + 8000	note 5
Long address, range 1-2	1 + ((CAPCODE – 1F9001) MOD 8000)	1FFFFF – ((CAPCODE – 1F9001) DIV 8000)
Long address, ranges 1-3 and 1-4	1 + ((CAPCODE – 1F9001) MOD 8000)	1D8000 + ((CAPCODE – 1F9001) DIV 8000)
Long address, range 2-3; note 6	1F7FFF + ((CAPCODE – 1F8FFF) MOD 8000)	1C8000 + ((CAPCODE – 1F8FFF) DIV 8000)

Notes

1. All numbers are in hexadecimal format.
2. The MOD operator gives the remainder of an integer division.
3. The DIV operator is the integer division.
4. CAPCODE refers to the value of the address field in a FLEX™ CAPCODE.
5. A short address consists of a single codeword.
6. The upper codeword range in bank 2 is used from the highest address downwards, i.e. the lowest value of the CAPCODE produces a codeword value of 1FFFFEH.

8.6.5 PHASE AND FRAME CALCULATION

The method for specifying the phase and base frame of a pager is specified in the CAPCODE type:

- The phase, base frame are extracted by standard rules from the user address field in the CAPCODE (CAPCODE types A to L).
- The phase is indicated by the CAPCODE type (Table 25) and the base frame is specified in the frame field of the CAPCODE (CAPCODE types U to Z).

For easy allocation of (up to 4) consecutive CAPCODEs having the same phase and frame, an offset in the range 0 to 3 is subtracted from the user address for the purposes of phase and frame extraction. The offset is determined by the CAPCODE type.

The standard rules for extracting phase and base frame from the user address are (phase numbers 0 to 3 correspond to phases A to D)

Phase number = ((Address – Offset) DIV 4) MOD 4

Frame = ((Address – Offset) DIV 16) MOD 128

where DIV is the integer division and MOD is the remainder of an integer division.

For a CAPCODE which does not use the standard rules for extracting phase and base frame (CAPCODE types U to Z) the 3-digit frame field 000 to 127 and a single digit decimal pager collapse 0 to 5 can precede the CAPCODE type. When these fields are not included, the paging device or the subscriber database must be accessed to determine the assigned frame and collapse value.

Table 25 Frame and phase extraction for different CAPCODE types

CAPCODE TYPE	PAGER TYPE	FRAME/PHASE EXTRACTION
A	single-phase	standard rules: Offset: 0
B	single-phase	standard rules: Offset: 1
C	single-phase	standard rules: Offset: 2
D	single-phase	standard rules; Offset: 3
E	any-phase	standard rules; Offset: 0
F	any-phase	standard rules; Offset: 1
G	any-phase	standard rules; Offset: 2
H	any-phase	standard rules; Offset: 3
I	all-phase; note 1	standard rules; Offset: 0
J	all-phase; note 1	standard rules; Offset: 1
K	all-phase; note 1	standard rules; Offset: 2
L	all-phase; note 1	standard rules; Offset: 3
U	single-phase	no frame extraction rules, phase-A
V	single-phase	no frame extraction rules, phase-B
W	single-phase	no frame extraction rules, phase-C
X	single-phase	no frame extraction rules, phase-D
Y	any-phase	no frame extraction rules, any-phase
Z	all-phase; note 1	no frame extraction rules, all-phase

Note

1. All-phase decoding is not defined in FLEX™ G1.8 and, therefore, is not supported by the PCD5008.

8.6.6 CONFIGURATION OF USER ADDRESSES (ID = 78H, 80H TO 8FH)

The PCD5008 has 16 user address locations which can be programmed as long or short, and configured as priority and/or tone-only. After a reset all address locations are disabled. Short addresses occupy a single location, long addresses occupy two locations. The first word of a long address must be in an even address location and the second word must be in the address index immediately following the first word. Address location containing long addresses of the 2-3 and 2-4 set (Section 8.6.3) must follow any address locations programmed as long addresses of the 1-2, 1-3 and 1-4 set.

User addresses are programmed using the address assignment packets, and are enabled and disabled using the address enable packet. To allow easy reprogramming of user addresses without disrupting normal operation, the host can send address assignment packets while the PCD5008 is on. In this case, the host must disable the user address location(s) by clearing the corresponding user address enable (UAE) bit in the UAE packet before changing any of the bits in the corresponding address assignment packet.

a: address location (Table 26). This specifies which address location is being configured. A zero in this field corresponds to address index zero (AI = 0) in the address packet received from the PCD5008 when an address is detected (Section 8.7.2).

LA: long address (Table 26). When this bit is set, the address is configured as a long address. Both words of a long address must have this bit set.

TOA: tone-only address (Table 26). When this bit is set, the PCD5008 considers this address a tone-only address and does not decode a vector word when the address is received. Both words of a long, tone only address must have this bit set.

A: address word (Table 26). This is the 21 bit value of the address word (A20 = MSB). Valid FLEX™ messaging addresses must be used. For the conversion from a CAPCODE (Section 8.6.4).

UAE: user address enable (Table 27). When a bit is set, the corresponding user address location is enabled. When it is cleared, the corresponding user address location is disabled. UAE_0 corresponds to the user address location configured using a packet ID of 80H and UAE_{15} corresponds to the user address location configured using a packet ID of 8FH. In some instances, if an invalid FLEX™ messaging address is programmed, it is not detected even when the address is enabled. Value after reset = 0.

Table 26 Address assignment packet bit assignments (ID = 80H to 8FH)

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	1	0	0	0	a_3	a_2	a_1	a_0
2	0	LA	TOA	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}
1	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8
0	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0

Table 27 Address enable packet bit assignments (ID = 78H)

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	1	1	1	1	0	0	0
2	0	0	0	0	0	0	0	0
1	UAE_{15}	UAE_{14}	UAE_{13}	UAE_{12}	UAE_{11}	UAE_{10}	UAE_9	UAE_8
0	UAE_7	UAE_6	UAE_5	UAE_4	UAE_3	UAE_2	UAE_1	UAE_0

8.6.7 CONFIGURATION OF ASSIGNED FRAMES AND PAGER COLLAPSE (ID = 20H TO 27H)

The assigned frame and collapse value determine the frames in which the decoding device typically looks for messages (other system factors can cause the decoding device to look in other frames in addition to the typical frames).

The PCD5008 must be configured explicitly to receive all required frames by setting the associated assigned frame (AF) bits. For each enabled CAPCODE these are the base frame and the associated frames implied by the pager collapse value. For example if the PCD5008 has one enabled address and it is assigned to base frame 3 with a collapse value of 4, the AF bits for frames 3, 19, 35, 51, 67, 83, 99 and 115 should be set and the AF bits for all other frames should be cleared. There are 8 frame assignment packets each capable of assigning a range of 16 consecutive frame numbers.

f: frame range, see Table 29 for location in the frame assignment packet and Table 28 for the AFs and values. The value determines which 16 frames out of a range of 128 correspond to the 16 AF bits in the packet. At least one of these bits must have been set when the PCD5008 is turned on by setting the ON bit in the control packet. Value after reset = 0.

AF: assigned frame (Table 29). If a bit is set, the PCD5008 decodes the associated FLEX™ frame and scans its contents for enabled addresses. Value after reset = 0.

Table 28 Frame assignment ranges

f_2	f_1	f_0	AF_{15}	AF_0
0	0	0	frame 127	frame 112
0	0	1	frame 111	frame 96
0	1	0	frame 95	frame 80
0	1	1	frame 79	frame 64
1	0	0	frame 63	frame 48
1	0	1	frame 47	frame 32
1	1	0	frame 31	frame 16
1	1	1	frame 15	frame 0

8.6.8 CONFIGURATION OF ASSIGNED PHASE

The assigned phase is required only for single-phase devices. It determines the phase (A, B, C, or D) in which the messages are received. For details of phase calculation see Section 8.6.5. For details of programming the assigned phase see Section 8.4.7.

Table 29 Frame assignment packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	0	1	0	0	f_2	f_1	f_0
2	0	0	0	0	0	0	0	0
1	AF_{15}	AF_{14}	AF_{13}	AF_{12}	AF_{11}	AF_{10}	AF_9	AF_8
0	AF_7	AF_6	AF_5	AF_4	AF_3	AF_2	AF_1	AF_0

8.7 Call data packets

8.7.1 GENERAL

The PCD5008 sends data extracted from the FLEX™ signal to the host in SPI packets using the following packet types:

- BIW packets which contain data transmitted in BIWs
- Address packets which indicate that a call has been detected and give additional information about call attributes
- Vector packets which indicate the call type and indicate which message word numbers (WN) are associated with the call
- Message packets which contain the information contained within the message codewords of a call.

For more information about the function of these packets within the FLEX™ datastream see Section 8.8.

8.7.2 ADDRESS PACKET (ID = 01H)

Information from address codewords in received calls is sent to the host in address packets. If less than 3 bit errors are detected in a received address word and it matches an enabled address assigned to the PCD5008, the address packet is sent to the host processor. The address packet contains the call address, the location in the datastream of the associated vector, and other miscellaneous call data.

PA: priority address (Table 30). This bit is set if the address was received as a priority address.

p: phase (Table 30). This is the phase on which the address was detected (0 = A, 1 = B, 2 = C and 3 = D).

LA: long address (Table 30). This bit is set if the address was programmed in the PCD5008 as a LA.

AI: address index (Table 30). This index identifies which address was detected. Valid values are 00H to 0FH, corresponding to the 16 programmable address words and 80H to 8FH, corresponding to the 16 temporary addresses (Section 8.8.4). For long addresses, the address packet is only sent once with AI referring to the second word of the address.

TOA: tone-only address (Table 30). Set this bit if the address was programmed in the PCD5008 as a tone-only address. No vector word is sent for tone-only addresses.

WN: word number of vector (2 to 87 decimal) (Table 30). The location of the vector within this frame for the detected address. This value is invalid for this packet if the TOA bit is set.

x: unused bits (Table 30). The value of these bits is not guaranteed.

8.7.3 VECTOR PACKETS (ID = 02H TO 57H)

Information from vector codewords in received calls is sent to the host in vector packets. For any address packet sent to the host (except tone-only addresses), a corresponding vector packet is always sent.

The ID of the vector packet is the word number where the vector word was received in the frame. The host must associate vector packets with a call by searching for an address packet previously received on the same phase and with WN bits which match the ID of the vector packet.

The vector type of a vector packet indicates the format of a call as one of:

- Numeric (3 types)
- Short message/tone-only
- Hex/binary
- Alphanumeric
- Secure message
- Short instruction.

The numeric, hex/binary, alphanumeric, and secure message vector packets indicate the location and number of message word packets in the message field. If more than two bit errors are detected in the vector word (via BCH calculations, parity calculations, check character calculations, or value validation) the e bit is set and the message words are not sent.

Table 30 Address packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	0	0	0	0	0	0	1
2	PA	p_1	p_0	LA	x	x	x	x
1	AI_7	AI_6	AI_5	AI_4	AI_3	AI_2	AI_1	AI_0
0	TOA	WN_6	WN_5	WN_4	WN_3	WN_2	WN_1	WN_0

8.7.4 NUMERIC VECTOR PACKET

WN: word number of vector (2 to 87 decimal) (Table 31). WN describes the location of the vector word in the frame.

e: error (Table 31). Set if more than 2 bit errors are detected in the word, if the check character calculation fails after error correction has been performed, or if the vector value is determined to be invalid.

p: phase (Table 31). This is the phase on which the vector was found (0 = A, 1 = B, 2 = C and 3 = D).

K: first check bits of the message checksum (Table 31 and Section 8.8.6).

n: number of message words in the message (Table 31), including the second vector word for long addresses, (000 = 1 word message, 001 = 2 word message, etc.). For long addresses, the first message word is located in the word location that immediately follows the associated vector.

b: word number of message start in the message field (3 to 87 decimal) (Table 31). For long addresses, the word number indicates the location of the second message word.

x: unused bits (Table 31). The value of these bits is not guaranteed.

V: vector type identifier (Table 32).

Table 31 Numeric vector packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	WN_6	WN_5	WN_4	WN_3	WN_2	WN_1	WN_0
2	e	p_1	p_0	x	x	V_2	V_1	V_0
1	x	x	K_3	K_2	K_1	K_0	n_2	n_1
0	n_0	b_6	b_5	b_4	b_3	b_2	b_1	b_0

Table 32 Numeric vector definitions

V_2	V_1	V_0	TYPE	DESCRIPTION
0	1	1	standard numeric	No special formatting of characters is specified.
1	0	0	special format numeric	Formatting of the received characters is predetermined by special rules in the host (e.g. inserting spaces and dashes).
1	1	1	numbered numeric	Received information is numbered by the service provider to indicate all messages have been properly received.

8.7.5 SHORT MESSAGE/TONE-ONLY VECTOR PACKET

V: vector type identifier, these bits set to 010 for a short message/tone-only vector (Table 33).

WN: word number of vector (2 to 87 decimal) (Table 33). WN describes the location of the vector word in the frame.

e: error (Table 33). Set if more than 2 bit errors are detected in the word, if the check character calculation fails after error correction has been performed, or if the vector value is determined to be invalid.

p: phase (Table 33). This is the phase on which the vector was found (0 = A, 1 = B, 2 = C and 3 = D).

t: message type (Tables 33 and 34). These bits define the meaning of the d bits in this packet.

x: unused bits (Table 33). The value of these bits is not guaranteed.

d: data bits whose definition depends on the value of t in this packet according to Table 34. Note that if this vector is received on a long address and the e bit in this packet is not set, the decoder sends a message packet from the word location immediately following the vector packet. Except for the short message on a non-network address (t = 0), all messages bits in the message packet are unused and should be ignored.

Table 33 Short message/tone-only vector packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	WN_6	WN_5	WN_4	WN_3	WN_2	WN_1	WN_0
2	e	p_1	p_0	x	x	V_2	V_1	V_0
1	x	x	d_{11}	d_{10}	d_9	d_8	d_7	d_6
0	d_5	d_4	d_3	d_2	d_1	d_0	t_1	t_0

Table 34 Short message/tone-only vector definitions

t_1	t_0	d_{11}	d_{10}	d_9	d_8	d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0	DESCRIPTION
0	0	c_3	c_2	c_1	c_0	b_3	b_2	b_1	b_0	a_3	a_2	a_1	a_0	first 3 numeric characters; note 1
0	1	s_8	s_7	s_6	s_5	s_4	s_3	s_2	s_1	s_0	S_2	S_1	S_0	8 sources (S) and 9 unused bits (s)
1	0	s_1	s_0	R_0	N_5	N_4	N_3	N_2	N_1	N_0	S_2	S_1	S_0	8 sources (S), message retrieval flag (R), message number (N) and 2 unused bits (s)
1	1													spare message type

Note

1. For long addresses, an extra 5 characters are sent in the message packet immediately following the vector packet.

8.7.6 HEX/BINARY, ALPHANUMERIC, SECURE MESSAGE VECTORS

V: vector type identifier (Table 35).

WN: word number of vector (2 to 87 decimal) (Table 36). WN describes the location of the vector word in the frame.

e: error (Table 36). Set if more than 2 bit errors are detected in the word, if the check character calculation fails after error correction has been performed, or if the vector value is determined to be invalid.

p: phase (Table 36). This is the phase on which the vector was found (0 = A, 1 = B, 2 = C and 3 = D).

n: number of message words in this frame (Table 36), including the first message word that immediately follows a long address vector. Valid values are 1 to 85 decimal.

b: word number of message start in the message field (Table 36). Valid values are 3 to 87 decimal.

x: unused bits (Table 36). The value of these bits is not guaranteed.

Note that for long addresses, the first message packet is sent from the word location immediately following the word location of the vector packet. The b bits indicate the second message word in the message field if one exists.

Table 35 Non-numeric vector definitions

V_2	V_1	V_0	TYPE
0	0	0	secure
1	0	1	alphanumeric
1	1	0	hex/binary

Table 36 Hex/binary, alphanumeric and secure message vector packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	WN_6	WN_5	WN_4	WN_3	WN_2	WN_1	WN_0
2	e	p_1	p_0	x	x	V_2	V_1	V_0
1	x	x	n_6	n_5	n_4	n_3	n_2	n_1
0	n_0	b_6	b_5	b_4	b_3	b_2	b_1	b_0

8.7.7 SHORT INSTRUCTION VECTOR

V: these bits are set 001 for a short instruction vector.

WN: word number of vector (2 to 87 decimal) (Table 37). WN describes the location of the vector word in the frame.

e: error (Table 37). Set if more than 2 bit errors are detected in the word, if the check character calculation fails after error correction has been performed, or if the vector value is determined to be invalid.

p: phase (Table 37). This is the phase on which the vector was found (0 = A, 1 = B, 2 = C and 3 = D).

i: instruction type (Tables 37 and 38). These bits define the meaning of the d bits in this packet.

x: unused bits (Table 37). The value of these bits is not guaranteed.

d: data bits whose definition depend on the value of the i bits in this packet according to Table 38. Note that if this vector is received on a long address and the e bit in this packet is not set, the decoder sends a message packet immediately following the vector packet. All message bits in the message packet are unused and should be ignored.

Table 37 Short instruction vector packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	WN_6	WN_5	WN_4	WN_3	WN_2	WN_1	WN_0
2	e	p_1	p_0	x	x	V_2	V_1	V_0
1	x	x	d_{10}	d_9	d_8	d_7	d_6	d_5
0	d_4	d_3	d_2	d_1	d_0	i_2	i_1	i_0

Table 38 Short instruction vector definitions

i_2	i_1	i_0	d_{10}	d_9	d_8	d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0	DESCRIPTION
0	0	0	a_3	a_2	a_1	a_0	f_6	f_5	f_4	f_3	f_2	f_1	f_0	temporary address assignment, note 1
0	0	1												reserved
0	1	0												reserved
0	1	1												reserved
1	0	0												reserved
1	0	1												reserved
1	1	0												reserved
1	1	1												reserved for test

Note

1. Assigned temporary address index a and associated frame number f (Section 8.8.4).

8.7.8 MESSAGE PACKETS (ID = 03H TO 57H)

8.7.8.1 General

The message field follows the vector field in the FLEX™ protocol. It contains the message data, checksum information, and may contain fragment and message numbers (Sections 8.8.7 and 8.8.5). If the error bit of a vector word is not set and the vector word indicates that there are message words associated with the page, the message words are sent in message packets to the host.

The ID of the message packet is the word number where the message word was received in the frame.

WN: word number of message word (3 to 87 decimal) (Table 40). WN describes the location of the message word in the frame.

e: error (Table 40). Set if more than 2 bit errors are detected in the word.

p: phase (Table 40). This is the phase on which the vector was found (0 = A, 1 = B, 2 = C and 3 = D).

i: these are the information bits of the message word (Table 40). The definition of these i bits depends on the vector type and which word of the message is being received.

8.7.8.2 Numeric Message

FLEX™ numeric messages are encoded using the 4-bit BCD encoded characters sets described in Table 39. Characters are placed in codewords along with additional information about the message as described in Tables 41 and 42 and the following definitions. The 4-bit numeric characters of the message are designated as letters a, b, c, d, ... z, A, B etc.

Only codewords containing the numeric message are to be transmitted. The space character CH is used to fill any unused 4-bit characters in the last word and zeros to fill any remaining partial characters. The checksum includes only the codewords comprising the shortened message, along with the space and fill characters used to fill in the last word.

Table 39 Standard and alternate numeric character sets (Peoples Republic of China (ROC) option 'on' and 'off')

B_3	B_2	B_1	B_0	CHARACTER	
				ROC 'on'	ROC 'off'
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	2	2
0	0	1	1	3	3
0	1	0	0	4	4
0	1	0	1	5	5
0	1	1	0	6	6
0	1	1	1	7	7
1	0	0	0	8	8
1	0	0	1	9	9
1	0	1	0	A	Spare
1	0	1	1	B	U
1	1	0	0	Space	Space
1	1	0	1	C	–
1	1	1	0	D	]
1	1	1	1	E	[

Table 40 Message packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	WN_6	WN_5	WN_4	WN_3	WN_2	WN_1	WN_0
2	e	p_1	p_0	i_{20}	i_{19}	i_{18}	i_{17}	i_{16}
1	i_{15}	i_{14}	i_{13}	i_{12}	i_{11}	i_{10}	i_9	i_8
0	i_7	i_6	i_5	i_4	i_3	i_2	i_1	i_0

K: least significant 2 bits of 6 bit message checksum (Tables 41 and 42), most significant 4 bits are in the vector word. See Section 8.8.6 for a description of message checksums.

N: message number (Table 42). See Section 8.8.7 for a description of message numbering.

R: message retrieval flag (Table 42). When this bit is set, the pager expects this message to be numbered. See Section 8.8.7 for a description of message numbering.

S: special format, (Table 42). In the numbered message format, when this bit is set, a special display format should be used. Spaces and dashes, specified by the host, are inserted into the received message to ease reading of the message. This feature may avoid the transmission of an additional word on the channel. The actual format is undefined in FLEX™ and may be determined by the manufacturer.

Table 41 Standard (V = 011) or special format (V = 100) 4, 10, 15, 20, 25, 31, 36, or 41 characters

MESSAGE WORD	i_0	i_1	i_2	i_3	i_4	i_5	i_6	i_7	i_8	i_9	i_{10}	i_{11}	i_{12}	i_{13}	i_{14}	i_{15}	i_{16}	i_{17}	i_{18}	i_{19}	i_{20}
1st	K_4	K_5	a_0	a_1	a_2	a_3	b_0	b_1	b_2	b_3	c_0	c_1	c_2	c_3	d_0	d_1	d_2	d_3	e_0	e_1	e_2
2nd	e_3	f_0	f_1	f_2	f_3	g_0	g_1	g_2	g_3	h_0	h_1	h_2	h_3	i_0	i_1	i_2	i_3	j_0	j_1	j_2	j_3
3rd	k_0	k_1	k_2	k_3	l_0	l_1	l_2	l_3	m_0	m_1	m_2	m_3	n_0	n_1	n_2	n_3	o_0	o_1	o_2	o_3	q_0
4th	q_1	q_2	q_3	r_0	r_1	r_2	r_3	s_0	s_1	s_2	s_3	t_0	t_1	t_2	t_3	u_0	u_1	u_2	u_3	v_0	v_1
5th	v_2	v_3	w_0	w_1	w_2	w_3	y_0	y_1	y_2	y_3	z_0	z_1	z_2	z_3	A_0	A_1	A_2	A_3	B_0	B_1	B_2
6th	B_3	C_0	C_1	C_2	C_3	D_0	D_1	D_2	D_3	E_0	E_1	E_2	E_3	F_0	F_1	F_2	F_3	G_0	G_1	G_2	G_3
7th	H_0	H_1	H_2	H_3	I_0	I_1	I_2	I_3	J_0	J_1	J_2	J_3	V_0	V_1	V_2	V_3	L_0	L_1	L_2	L_3	M_0
8th	M_1	M_2	M_3	O_0	O_1	O_2	O_3	P_0	P_1	P_2	P_3	Q_0	Q_1	Q_2	Q_3	T_0	T_1	T_2	T_3	U_0	U_1

Table 42 Numbered (V = 111) 2, 8, 13, 18, 23, 29, 34, or 39 numeric characters

MESSAGE WORD	i_0	i_1	i_2	i_3	i_4	i_5	i_6	i_7	i_8	i_9	i_{10}	i_{11}	i_{12}	i_{13}	i_{14}	i_{15}	i_{16}	i_{17}	i_{18}	i_{19}	i_{20}
1st	K_4	K_5	N_0	N_1	N_2	N_3	N_4	N_5	R_0	S_0	a_0	a_1	a_2	a_3	b_0	b_1	b_2	b_3	c_0	c_1	c_2
2nd	c_3	d_0	d_1	d_2	d_3	e_0	e_1	e_2	e_3	f_0	f_1	f_2	f_3	g_0	g_1	g_2	g_3	h_0	h_1	h_2	h_3
3rd	i_0	i_1	i_2	i_3	j_0	j_1	j_2	j_3	k_0	k_1	k_2	k_3	l_0	l_1	l_2	l_3	m_0	m_1	m_2	m_3	n_0
4th	n_1	n_2	n_3	o_0	o_1	o_2	o_3	q_0	q_1	q_2	q_3	r_0	r_1	r_2	r_3	s_0	s_1	s_2	s_3	t_0	t_1
5th	t_2	t_3	u_0	u_1	u_2	u_3	v_0	v_1	v_2	v_3	w_0	w_1	w_2	w_3	y_0	y_1	y_2	y_3	z_0	z_1	z_2
6th	z_3	A_0	A_1	A_2	A_3	B_0	B_1	B_2	B_3	C_0	C_1	C_2	C_3	D_0	D_1	D_2	D_3	E_0	E_1	E_2	E_3
7th	F_0	F_1	F_2	F_3	G_0	G_1	G_2	G_3	H_0	H_1	H_2	H_3	I_0	I_1	I_2	I_3	J_0	J_1	J_2	J_3	V_0
8th	V_1	V_2	V_3	L_0	L_1	L_2	L_3	M_0	M_1	M_2	M_3	O_0	O_1	O_2	O_3	P_0	P_1	P_2	P_3	Q_0	Q_1

8.7.8.3 Alphanumeric Message

FLEX™ alphanumeric messages are encoded using the 7-bit encoded alphanumeric character set defined in Table 43. Characters are placed in codewords along with additional information about the message as described in Tables 44 and 45 and the following definitions. The 7-bit characters of the message are designated lower case letters a, b, c, d, etc.

Alphanumeric messages can be sent as fragments. See Section 8.8.5 for a description of message fragmentation.

Control characters that are not acted upon by the pager are ignored in the display process (do not require display space) but are stored in memory for possible download to an external device. The ASCII character ETX (03H) should be used to fill any unused 7-bit characters in a word.

Where symbolic characters (e.g. Chinese, Kanji etc.) are being transmitted, special rules for fragment and message termination are defined in Section 8.8.5.1.

Each 7 bit field, starting with the second character of the second word in the message (first character of the second word in all remaining fragments), represents standard ASCII (ISO 646-1983E) characters with options for certain international characters.

Table 43 FLEX™ alphanumeric character set

LEAST SIGNIFICANT 4-BITS OF CHARACTER (HEX)	MOST SIGNIFICANT 3-BITS OF CHARACTER (HEX)							
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
0	NUL	DLE	SP	0	@	P	‘	p
1	SOH	DC1	!	1	A	Q	a	q
2	STX	DC2	“	2	B	R	b	r
3	ETX	DC3	#	3	C	S	c	s
4	EOT	DC4	$	4	D	T	d	t
5	ENQ	NAK	%	5	E	U	e	u
6	ACK	SYN	&	6	F	V	f	v
7	BEL	ETB	’	7	G	W	g	w
8	BS	CAN	(	8	H	X	h	x
9	TAB	EM	)	9	I	Y	i	y
A	LF	SUB	*	:	J	Z	j	z
B	VT	ESC	+	;	K	[	k	{
C	FF	FS	,	<	L	\	l	|
D	CR	GS	-	=	M	]	m	}
E	SO	RS	.	>	N	^	n	~
F	SI	US	/	?	O	_	o	DEL

K: 10 bit fragment checksum (Tables 44 and 45). See Section 8.8.6 for a description of message checksum.

C: 1 bit message continued flag (Tables 44 and 45). When this bit is set, fragments of this message are to be expected in following frames. See Section 8.8.5 for a description of message fragmentation.

F: 2 bit message fragment number (Tables 44 and 45). This is a modulo 3 message fragment number which is incremented by 1 in successive message fragments. See Section 8.8.5 for a description of message fragmentation.

N: message number (Tables 44 and 45). See Section 8.8.7 for a description of message numbering.

M: 1 bit mail drop flag (Table 44). When this bit is set, it indicates the message is to be stored in a special area in memory and is written over existing data automatically in that memory space.

R: message retrieval flag (Table 44). When this bit is set, the pager expects this message to be numbered. See Section 8.8.7 for a description of message numbering.

S: 7 bit signature field (Table 44). The signature is defined to be the 1's complement of the binary sum over the total message (all fragments). 7 bits at a time are taken (on alpha character boundary) starting with the first 7 bits directly following the signature field, $a_6a_5a_4a_3a_2a_1a_0$, $b_6b_5b_4b_3b_2b_1b_0$, etc. The 7 LSBs of the result are transmitted as the message signature.

U, V: fragmentation control bits (Table 45). This field exists in all fragments except the first fragment. It is used to support character position tracking in each fragment when symbolic characters (character made up of 1, 2 or 3 ASCII characters) are transmitted using the alphanumeric message type. The default value is 0,0. See Section 8.8.5.1 for a description of fragment control.

Table 44 Vector type V = 101 first fragment

MESSAGE WORD	i_0	i_1	i_2	i_3	i_4	i_5	i_6	i_7	i_8	i_9	i_{10}	i_{11}	i_{12}	i_{13}	i_{14}	i_{15}	i_{16}	i_{17}	i_{18}	i_{19}	i_{20}
1st	K_0	K_1	K_2	K_3	K_4	K_5	K_6	K_7	K_8	K_9	C_0	F_0	F_1	N_0	N_1	N_2	N_3	N_4	N_5	R_0	M_0
2nd	S_0	S_1	S_2	S_3	S_4	S_5	S_6	a_0	a_1	a_2	a_3	a_4	a_5	a_6	b_0	b_1	b_2	b_3	b_4	b_5	b_6
3rd	c_0	c_1	c_2	c_3	c_4	c_5	c_6	d_0	d_1	d_2	d_3	d_4	d_5	d_6	e_0	e_1	e_2	e_3	e_4	e_5	e_6
4th	f_0	f_1	f_2	f_3	f_4	f_5	f_6	g_0	g_1	g_2	g_3	g_4	g_5	g_6	h_0	h_1	h_2	h_3	h_4	h_5	h_6
5th	i_0	i_1	i_2	i_3	i_4	i_5	i_6	j_0	j_1	j_2	j_3	j_4	j_5	j_6	k_0	k_1	k_2	k_3	k_4	k_5	k_6
...																					
nth	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i

Table 45 Vector type V = 101 other fragments

MESSAGE WORD	i_0	i_1	i_2	i_3	i_4	i_5	i_6	i_7	i_8	i_9	i_{10}	i_{11}	i_{12}	i_{13}	i_{14}	i_{15}	i_{16}	i_{17}	i_{18}	i_{19}	i_{20}
1st	K_0	K_1	K_2	K_3	K_4	K_5	K_6	K_7	K_8	K_9	C_0	F_0	F_1	N_0	N_1	N_2	N_3	N_4	N_5	U_0	V_0
2nd	a_0	a_1	a_2	a_3	a_4	a_5	a_6	b_0	b_1	b_2	b_3	b_4	b_5	b_6	c_0	c_1	c_2	c_3	c_4	c_5	c_6
3rd	d_0	d_1	d_2	d_3	d_4	d_5	d_6	e_0	e_1	e_2	e_3	e_4	e_5	e_6	f_0	f_1	f_2	f_3	f_4	f_5	f_6
4th	g_0	g_1	g_2	g_3	g_4	g_5	g_6	h_0	h_1	h_2	h_3	h_4	h_5	h_6	i_0	i_1	i_2	i_3	i_4	i_5	i_6
5th	j_0	j_1	j_2	j_3	j_4	j_5	j_6	k_0	k_1	k_2	k_3	k_4	k_5	k_6	l_0	l_1	l_2	l_3	l_4	l_5	l_6
...																					
nth	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i

8.7.8.4 Hex/binary message

FLEX™ hexadecimal/binary messages may be encoded using any word size (blocking length) in the range 1 to 16 bits. Words are placed in codewords along with additional information about the message as described in Tables 46 and 47 and these definitions. The message data in Tables 46 and 47 have blocking lengths of 4 bits; words are designated lower case letters a, b, c, d etc.

Hexadecimal/binary messages can be sent as fragments. See Section 8.8.5 for a description of message fragmentation. Messages and message fragments are terminated, or interrupted in the case of a non-terminating fragment, on the last full character boundary in the last codeword. Unused bits are cleared if the last valid data bit is logic 1, or set if the last valid data bit is logic 0. If the terminating fragment exactly fills its last codeword, an additional codeword is sent to indicate the location of the last character. This codeword is filled with logic 0s if the last valid data bit is logic 1 and filled with logic 1s if the last valid data bit is logic 0.

Fields K to N make up the first word of a message and the first word of every fragment in a long message.

K: 12 bit fragment checksum (Tables 46 and 47). See Section 8.8.6 for a description of message checksums.

C: 1 bit message continued flag (Tables 46 and 47). When this bit is set, fragments of this message are to be expected in following frames. See Section 8.8.5 for a description of message fragmentation.

F: 2 bit message fragment number (Tables 46 and 47). This is a modulo 3 message fragment number which is incremented by 1 in successive message fragments. See Section 8.8.5 for a description of message fragmentation.

N: message number (Tables 46 and 47). See Section 8.8.7 for a description of message numbering.

H: 1 bit header message flag (Table 46). It is a header message only when this bit is set, otherwise it is a data message. A header message is a displayable tag associated with a non-displayable data message. The header message (which is sent first) and the data message, both have the same message number.

The second codeword of the first fragment of a hex/binary message contains fields R to S. These fields are only transmitted in the first fragment of a message.

R: message retrieval flag (Table 46). When this bit is set, the pager expects this message to be numbered. See Section 8.8.7 for a description of message numbering.

s: 5 bit field reserved for future use (Table 46). Default value = 00000.

M: 1 bit mail drop flag, see Table 46. When this bit is set, the message is to be stored in a special area in memory to overwrite existing data in the same memory space.

D: 1 bit display direction field (Table 46). D = 0 display left to right, D = 1 display right to left (valid only when data sent as characters i.e. blocking length not equal 0001).

B: 4 bit blocking length (Table 46). Indicates bits per character. $B_3B_2B_1B_0$ = 0001 = 1 bit per character (binary/transparent data), 1111 = 15 bits per character, 0000 = 16 bits per character. Data with a blocking length other than 1 is assumed to be displayed on a character by character basis (default value = 0001). Note: Tables 46 and 47 show B = 4 bit blocking length.

S: 8 bit signature field (Table 46). The 1's complement of the binary sum, taken 8 bits at a time, over the total message prior to formatting into fragments. The first 8 bits following the signature field are summed with the following 8 bits, $b_3b_2b_1b_0a_3a_2a_1a_0 + d_3d_2d_1d_0c_3c_2c_1c_0$, etc. continuing to the last valid data bit in the last word of the last fragment (the sum does not include termination bits). The 8 LSBs of the result are inverted (1's complement) and transmitted as the message signature.

8.7.8.5 Secure message

FLEX™ secure messages are encoded using the 7-bit FLEX™ alphanumeric character set (Section 8.7.8.3). These characters are placed in codewords along with additional information about the message as described in Table 48 and the following definitions. In Table 48, 7-bit characters of the message are designated lower case letters a, b, c, d etc.

Secure messages follow the same fragmentation and termination rules as alphanumeric messages (Section 8.7.8.3).

K: 10 bit fragment checksum (Table 48). See Section 8.8.6 for a description of message checksums.

C: 1 bit message continued flag (Table 48). When this bit is set, fragments of this message are to be expected in following frames. See Section 8.8.5 for a description of message fragmentation.

F: 2 bit message fragment number (Table 48). This is a modulo 3 message fragment number which is incremented by 1 in successive message fragments. See Section 8.8.5 for a description of message fragmentation.

N: message number (Table 48). See Section 8.8.7 for a description of message numbering.

s: spare bits (Table 48), are not used and are set to 0.

Table 46 Vector type V = 110 first fragment

MESSAGE WORD	i_0	i_1	i_2	i_3	i_4	i_5	i_6	i_7	i_8	i_9	i_{10}	i_{11}	i_{12}	i_{13}	i_{14}	i_{15}	i_{16}	i_{17}	i_{18}	i_{19}	i_{20}
1st	K_0	K_1	K_2	K_3	K_4	K_5	K_6	K_7	K_8	K_9	K_{10}	K_{11}	C_0	F_0	F_1	N_0	N_1	N_2	N_3	N_4	N_5
2nd	R_0	M_0	D_0	H_0	B_0	B_1	B_2	B_3	s_0	s_1	s_2	s_3	s_4	S_0	S_1	S_2	S_3	S_4	S_5	S_6	S_7
3rd	a_0	a_1	a_2	a_3	b_0	b_1	b_2	b_3	c_0	c_1	c_2	c_3	d_0	d_1	d_2	d_3	e_0	e_1	e_2	e_3	f_0
4th	f_1	f_2	f_3	g_0	g_1	g_2	g_3	h_0	h_1	h_2	h_3	i_0	i_1	i_2	i_3	j_0	j_1	j_2	j_3	k_0	k_1
5th	k_2	k_3	l_0	l_1	l_2	l_3	m_0	m_1	m_2	m_3	n_0	n_1	n_2	n_3	o_0	o_1	o_2	o_3	q_0	q_1	q_2
6th	q_3	r_0	r_1	r_2	r_3	s_0	s_1	s_2	s_3	t_0	t_1	t_2	t_3	u_0	u_1	u_2	u_3	v_0	v_1	v_2	v_3
...																					
nth	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i

Table 47 Vector type V = 110 all other fragments

MESSAGE WORD	i_0	i_1	i_2	i_3	i_4	i_5	i_6	i_7	i_8	i_9	i_{10}	i_{11}	i_{12}	i_{13}	i_{14}	i_{15}	i_{16}	i_{17}	i_{18}	i_{19}	i_{20}
1st	K_0	K_1	K_2	K_3	K_4	K_5	K_6	K_7	K_8	K_9	K_{10}	K_{11}	C_0	F_0	F_1	N_0	N_1	N_2	N_3	N_4	N_5
2nd	a_0	a_1	a_2	a_3	b_0	b_1	b_2	b_3	c_0	c_1	c_2	c_3	d_0	d_1	d_2	d_3	e_0	e_1	e_2	e_3	f_0
3rd	f_1	f_2	f_3	g_0	g_1	g_2	g_3	h_0	h_1	h_2	h_3	i_0	i_1	i_2	i_3	j_0	j_1	j_2	j_3	k_0	k_1
4th	k_2	k_3	l_0	l_1	l_2	l_3	m_0	m_1	m_2	m_3	n_0	n_1	n_2	n_3	o_0	o_1	o_2	o_3	q_0	q_1	q_2
5th	q_3	r_0	r_1	r_2	r_3	s_0	s_1	s_2	s_3	t_0	t_1	t_2	t_3	u_0	u_1	u_2	u_3	v_0	v_1	v_2	v_3
...																					
nth	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i

Table 48 Vector type V = 000 all fragments

MESSAGE WORD	i_0	i_1	i_2	i_3	i_4	i_5	i_6	i_7	i_8	i_9	i_{10}	i_{11}	i_{12}	i_{13}	i_{14}	i_{15}	i_{16}	i_{17}	i_{18}	i_{19}	i_{20}
1st	K_0	K_1	K_2	K_3	K_4	K_5	K_6	K_7	K_8	K_9	C_0	F_0	F_1	N_0	N_1	N_2	N_3	N_4	N_5	s_0	s_1
2nd	a_0	a_1	a_2	a_3	a_4	a_5	a_6	b_0	b_1	b_2	b_3	b_4	b_5	b_6	c_0	c_1	c_2	c_3	c_4	c_5	c_6
3rd	d_0	d_1	d_2	d_3	d_4	d_5	d_6	e_0	e_1	e_2	e_3	e_4	e_5	e_6	f_0	f_1	f_2	f_3	f_4	f_5	f_6
4th	g_0	g_1	g_2	g_3	g_4	g_5	g_6	h_0	h_1	h_2	h_3	h_4	h_5	h_6	i_0	i_1	i_2	i_3	i_4	i_5	i_6
5th	j_0	j_1	j_2	j_3	j_4	j_5	j_6	k_0	k_1	k_2	k_3	k_4	k_5	k_6	l_0	l_1	l_2	l_3	l_4	l_5	l_6
...																					
nth	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i

8.7.9 Block Information Word (BIW) packet (ID = 00H)

The FLEX™ protocol allows systems to transmit time information using block information words. The information carried in a BIW depends on the BIW word format (Table 49). The first BIW of each phase, carrying information about the frame structure, is used internally by the PCD5008 and is never transmitted to the host.

The PCD5008 can be configured to send all time and date BIWs (BIW001, BIW010 and BIW101) to the host by setting the SBI bit in the control packet, see Section 8.4.7. When the SBI bit is set and a BIW is received with an uncorrectable number of bit errors, the PCD5008 sends the BIW to the host indicating that the codeword was received in error (regardless of the BIW word format). The PCD5008 does not support decoding of vector and message words associated with the data/system message BIW101.

System providers supporting local time transmissions are required to transmit at least one time related BIW in each phase transmitted in frame 0, cycle 0. The time transmitted is the local time for the transmitted time zone and refers to the actual time at the leading edge of the first bit of sync. 1 of frame 0 of the current cycle.
See Tables 50, 51, 52 and 53 and the following bit definitions of the time related BIWs.

e: error (Table 49). Set if more than 2 bit errors are detected in the word or if the check character calculation fails after error correction has been performed.

p: phase (Table 49), is the phase on which the BIW was found (0 = A, 1 = B, 2 = C and 3 = D).

x: unused bits (Table 49). Their value is not guaranteed.

f: word format type (Table 49). The value of these bits modify the meaning of the s bits in this packet as described in Tables 50, 51 and 52. If the e bit is not set, this field is one of 001, 010 or 101.

s: BIW information bits (Table 49). The definition of these bits depend on the f bits in this packet.

m: month field (Table 50). 0001 to 1100 binary correspond to January to December in month order.

d: day field (Table 50). 00001 to 11111 binary correspond to 1 to 31 days in the month.

Table 49 BIW packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	0	0	0	0	0	0	0
2	e	p_1	p_0	x	x	f_2	f_1	f_0
1	x	x	s_{13}	s_{12}	s_{11}	s_{10}	s_9	s_8
0	s_7	s_6	s_5	s_4	s_3	s_2	s_1	s_0

Table 50 Month/day/year BIW definitions

f_2	f_1	f_0	s_{13}	s_{12}	s_{11}	s_{10}	s_9	s_8	s_7	s_6	s_5	s_4	s_3	s_2	s_1	s_0
0	0	1	m_3	m_2	m_1	m_0	d_4	d_3	d_2	d_1	d_0	Y_4	Y_3	Y_2	Y_1	Y_0

Table 51 Second/minute/hour BIW definitions

f_2	f_1	f_0	s_{13}	s_{12}	s_{11}	s_{10}	s_9	s_8	s_7	s_6	s_5	s_4	s_3	s_2	s_1	s_0
0	1	1	S_2	S_1	S_0	M_5	M_4	M_3	M_2	M_1	M_0	H_4	H_3	H_2	H_1	H_0

Table 52 Accurate seconds/daylight savings time/time zone; system message BIW definitions

f_2	f_1	f_0	s_{13}	s_{12}	s_{11}	s_{10}	s_9	s_8	s_7	s_6	s_5	s_4	s_3	s_2	s_1	s_0	DESCRIPTION
1	0	1	S_2	S_1	S_0	x	L_0	z_4	z_3	z_2	z_1	z_0	0	1	0	X	system message; note 1

Note

1. When the $s_3s_2s_1s_0$ field is 0100 or 0101, then s_4 to s_{13} are defined as above, when the $s_3s_2s_1s_0$ field does not have one of these values, the system message does not contain time related information and is not sent to the host.

Y: year field (Table 50). This represents the year with modulo 32 arithmetic. 00000 to 11111 binary representing years 1994 to 2025 and 2026 to 2057.

S: seconds field (Table 51). This represents a coarse value of the seconds field. These bits represent the seconds in $\frac{1}{8}$ minute (7.5 s) increments. 000 to 111 binary correspond to 0 to 52.5 seconds.

M: minute field (Table 51). 000000 to 111011 binary correspond to 0 to 59 minutes.

H: hour field (Table 51). 00000 to 10111 binary correspond to 0 to 23 hours.

S: accurate seconds (Table 52). This field provides a more accurate seconds reference and can be used to adjust the seconds to within 1 second. This field represents the time that should be added to the coarse seconds in $\frac{1}{64}$ minute increments.

L: daylight savings time (Table 52). When this bit is set, the time being transmitted is local standard time. When it is clear, the time being transmitted is daylight savings time.

z: time zone (Table 52). These bits indicate the time zone for the time which is being transmitted. The offset from GMT is the offset for local standard time. Table 53 describes the values for **z**.

Table 53 Time zone values

z_4	z_3	z_2	z_1	z_0	TIME ZONE
0	0	0	0	0	GMT
0	0	0	0	1	GMT + 01:00h
0	0	0	1	0	GMT + 02:00h
0	0	0	1	1	GMT + 03:00h
0	0	1	0	0	GMT + 04:00h
0	0	1	0	1	GMT + 05:00h
0	0	1	1	0	GMT + 06:00h
0	0	1	1	1	GMT + 07:00h
0	1	0	0	0	GMT + 08:00h
0	1	0	0	1	GMT + 09:00h
0	1	0	1	0	GMT + 10:00h
0	1	0	1	1	GMT + 11:00h
0	1	1	0	0	GMT + 12:00h
0	1	1	0	1	GMT + 03:30h
0	1	1	1	0	GMT + 04:30h
0	1	1	1	1	GMT + 05:30h
1	0	0	0	0	reserved
1	0	0	0	1	GMT + 05:45h
1	0	0	1	0	GMT + 06:30h
1	0	0	1	1	GMT + 09:30h
1	0	1	0	0	GMT – 03:30h
1	0	1	0	1	GMT – 11:00h
1	0	1	1	0	GMT – 10:00h
1	0	1	1	1	GMT – 09:00h
1	1	0	0	0	GMT – 08:00h
1	1	0	0	1	GMT – 07:00h
1	1	0	1	0	GMT – 06:00h
1	1	0	1	1	GMT – 05:00h
1	1	1	0	0	GMT – 04:00h
1	1	1	0	1	GMT – 03:00h
1	1	1	1	0	GMT – 02:00h
1	1	1	1	1	GMT – 01:00h

8.8 Message reception

8.8.1 FLEX™ SIGNAL STRUCTURE

The FLEX™ signal transmitted on the radio channel (See Fig.17) consists of a series of four minute cycles, each cycle having 128 frames at 1.875 seconds per frame. A pager may be assigned to process any number of the frames. Battery saving is performed for frames which are not assigned. The FLEX™ signal can assign additional frames to the pager using collapse, fragmentation, temporary addressing or carry-on information within the FLEX™ signal.

Each FLEX™ frame has a synchronization portion followed by an eleven block data portion, each block lasting 160 milliseconds. The synchronization portion indicates the rate at which the data portion is transmitted, 1600, 3200 or 6400 bits per second (bps). The 1600 bps rate is transmitted at 1600 symbols per second (sps) using 2 level FSK modulation and consists of a single phase of information at 1600 bps, phase-A. The 3200 bps rate is transmitted at either 1600 sps using 4 level FSK modulation or 3200 sps using 2 level FSK modulation and consists of two concurrent phases of information at 1600 bps, phase-A and phase-C. The 6400 bps rate is transmitted at 3200 sps using 4 level FSK modulation and consists of four concurrent phases of information at 1600 bps (phase-A, -B, -C and -D).

Each block has eight interleaved words per phase, thus there are 88 codewords (numbered 0 to 87) per phase in every frame. Each word has information contained within an error correcting code which allows for bit error correction and detection. The 88 words in each phase are organized into a block information field, an address field, a vector field, a message field, and an idle field. The boundaries between the fields are independent of the block boundaries. Furthermore, at 3200 and 6400 bps, the information in one phase is independent of the information in a concurrent phase, and the boundaries between the fields of one phase are unrelated to the boundaries between the fields in a concurrent phase.

The synchronization portion consists of: a first sync. signal at 1600 bps; a frame information word having the frame number 0 to 127 (7 bits) and the cycle number 0 to 14 (4 bits); and a second sync. signal at the data rate of the interleaved portion.

The block information field contains BIWs. These can be used for determining time and date information and certain paging system information.

The address field contains addresses assigned to paging devices. Addresses are used to identify information sent to individual paging devices and/or groups of paging devices. Information in the FLEX™ signal may indicate that an address is a priority address. An address may be either a short (one word) address or a long (two word) address. An address may be a tone-only address in which case there is no additional information associated with the address. If an address is not a tone-only address, then there is an associated vector word in the vector field. Information in the FLEX™ signal indicates the location of the vector word in the vector field associated with the address. A pager may perform battery saving at the end of the address field when its address(es) is not detected.

The vector field consists of a series of vector words. Depending upon the type of message, a vector word (or words in the case of a long address) may either contain all of the information necessary for the message, or indicate the location of message words in the message field comprising the message information. Short addresses have one associated vector word in the vector field. Long addresses have one associated vector word in the vector field directly followed by the first message codeword of the call.

The message field consists of a series of information words containing message information. The message information may be formatted in ASCII, BCD or binary depending upon the message type.

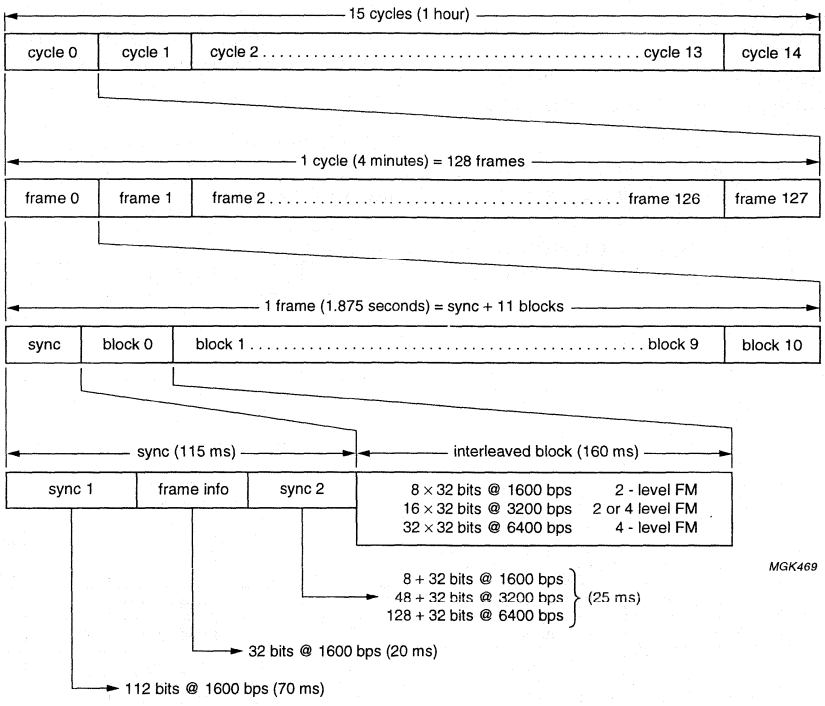

Fig.17 FLEX™ signal structure.

8.8.2 MESSAGE BUILDING

The PCD5008 sends data from the FLEX™ signal to the host in packets. Data is transmitted one block at a time, and one phase at a time. For a 2 phase transmission, information in block 0 phase-A is converted into packets and sent to the host, then information in block 0 phase-C is sent to the host followed by information in block 1 phase-A and then information in block 1 phase-C etc. Codewords for different calls may therefore be interleaved, so the host must use the phase and word number embedded in each packet to associate that packet with a particular call.

The phase and word number of the vector packet provides a unique key which allows the host to associate all the data for a particular call within a frame. The host must then use information embedded in the vector word to calculate what message word locations are associated with the vector.

Table 54 FLEX™ transmission sequence

BLOCK	WORD	PHASE-A	PHASE-C
0	0	BIW1; note 1	BIW1; note 1
	1	addr; note 2	BIW
	2	addr; note 2	BIW
	3	$addr_1$	addr; note 2
	4	$addr_2$	addr; note 2
	5	vect; note 2	long $addr_3$ (cw 1)
	6	vect; note 2	long $addr_3$ (cw 2)
	7	$vect_1$	addr; note 2
1	8	$vect_2$	vect; note 2
	9	$mess_1$ (cw 1)	vect; note 2
	10	$mess_1$ (cw 2)	$vect_3$; note 3
	11	$mess_1$ (cw 3)	$mess_3$ (cw 1); note 4
	12	$mess_2$ (cw 1)	mess; note 2
	13	$mess_2$ (cw 2)	mess; note 2
	14	$mess_2$ (cw 3)	$mess_3$ (cw 2)
	15	$mess_2$ (cw 4)	$mess_3$ (cw 3)

Notes

1. Phases begin with BIW1, which is not sent to the host.
2. Codewords not addressed to the pager.
3. Vector for long address indicates the location of the second and third message words.
4. For long addresses, the first message word immediately follows the vector.

Tables 54 and 55 show an example of receiving three messages (possibly portions of fragmented or group messages), and two BIW packets in the first two blocks of a 2 phase 3200 bps FLEX™ frame in case of an any-phase pager. Table 54 shows the block number, word number and word content of both phase-A and phase-C (subscripts indicate the call number). In a 6400 bps FLEX™ frame, there would be four phases: A, B, C and D; in a 1600 bps signal there would be only phase-A. Table 55 shows the sequence of packets transmitted to the host.

Table 55 PCD5008 packet sequence

PACKET	PHASE	PACKET TYPE	WORD NO.	COMMENT
1	A	address	7	note 1
2	A	address	8	note 1
3	A	vector	7	pointer to phase-A word 9
4	C	BIW	n.a.	note 2
5	C	BIW	n.a.	note 2
6	C	long address	10	note 1
7	A	vector	8	pointer to phase-A word 12
8	A	message	9	$mess_1$ (cw 1)
9	A	message	10	$mess_1$ (cw 2)
10	A	message	11	$mess_1$ (cw 3)
11	A	message	12	$mess_2$ (cw 1)
12	A	message	13	$mess_2$ (cw 2)
13	A	message	14	$mess_2$ (cw 3)
14	A	message	15	$mess_2$ (cw 4)
15	C	vector	10	pointer to phase-A word 14
16	C	message	11	$mess_3$ (cw 1)
17	C	message	14	$mess_3$ (cw 2)
18	C	message	15	$mess_3$ (cw 3)

Notes

1. Word number in an address is that of the corresponding vector.
2. BIW sent if BIW reception enabled by SBI bit in the control packet.

8.8.3 ALL FRAME MODE (ID = 03H)

The FLEX™ protocol requires pagers to be capable of receiving data in frames other than pagers' programmed frames and frames implied by collapse values. This is achieved in the PCD5008 by all frame mode (AFM) which is required to implement the following features:

- Fragmented messages Section 8.8.5)
- Temporary addresses (Section 8.8.4).

The PCD5008 enters AFM automatically and when in AFM, it decodes every FLEX™ frame irrespective of whether it is a programmed frame. In AFM the PCD5008 sends a status packet with the end-of-frame (EOF) bit set at the end of every frame. In addition the host can force AFM by sending an AFM packet with the force all frame mode (FAF) bit set.

The PCD5008 contains a number of counters which are used to track the number of active calls requiring AFM. These consist of an AFM counter for tracking the number of active fragmented messages and 16 temporary address enable (TAE) counters which count the number of times each temporary address has been enabled. These counters are automatically incremented when a corresponding vector is received, i.e.:

- A short instruction vector indicating a temporary address has been assigned to this pager
- A vector indicating a message for this pager with a format which allows fragmentation.

The host must determine when no further data can be received for a message associated with a temporary address, or a fragmented message, and send an AFM packet, see Table 56, to decrement the appropriate counter. AFM remains active until the host determines that no further data can be sent to it outside programmed frames, i.e:

- The TAE counters are all zero indicating that no further temporary message data is expected
- The AFM counter is zero indicating that no further data is expected for fragmented messages
- The FAF bit is clear.

Both the AFM counter and the TAE counters can only be incremented internally by the PCD5008 and can only be decremented by the host via AFM packet. Neither the TAE counters nor the AFM counter can be incremented past the value 127 (it does not roll-over) or decremented past the value 0. The TAE counters and the AFM counter are cleared on a reset and when the decoder is turned off.

DAF: decrement all frame mode counter, see Table 56. Setting this bit decrements the AFM counter by one. If a packet is sent with this bit clear, the AFM counter is not affected. Value after reset = 0.

FAF: force all frame mode, see Table 56. Setting this bit forces the PCD5008 to enter AFM. If this bit is clear, the PCD5008 may or may not be in AFM depending on the status of the AFM counter and the TAE counters. This functionality may be useful in acquiring transmitted time information. Value after reset = 0.

DTA: decrement temporary address enable counter, see Table 56. When a bit in this word is set, the corresponding TAE counter is decremented by one. When a bit is clear, the corresponding TAE counter is not affected. When a TAE counter reaches zero, the temporary address is disabled. Value after reset = 0.

Table 56 All frame mode packet bit assignments

BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3	0	0	0	0	0	0	1	1
2	DAF	FAF	0	0	0	0	0	0
1	DTA_{15}	DTA_{14}	DTA_{13}	DTA_{12}	DTA_{11}	DTA_{10}	DTA_9	DTA_8
0	DTA_7	DTA_6	DTA_5	DTA_4	DTA_3	DTA_2	DTA_1	DTA_0

8.8.4 TEMPORARY ADDRESSES

FLEX™ allows dynamic group calls in which a common message is sent to a group of paging devices. This is achieved by assigning the same temporary address (TA) to each pager in the group using the pagers' personal addresses and the short instruction vector. The short instruction vector causes the TA to be active in the next occurrence of a specific frame (if the designated frame is equal to the present frame the host is to interpret this as the next occurrence of this frame in the following cycle).

FLEX™ specifies sixteen TAs which remain valid for one message starting in the specified frame and remaining valid throughout the following frames to the completion of the message. The FLEX™ protocol restricts the placement of TAs such that once assigned to a specific frame they cannot occur in the FLEX™ transmission before that frame.

The PCD5008 uses AFM (Section 8.8.3) to allow the reception of TAs outside programmed frames.
The sequence for the host and the PCD5008 to operate a TA is:

1. The PCD5008 receives an address codeword followed by a vector codeword with $V_2V_1V_0 = 001$ and $I_2I_1I_0 = 000$ indicating a short instruction vector which assigns a TA to this pager.
2. The PCD5008 passes the address and vector codeword to the host as packets and increments the corresponding TA counter and enters AFM.
3. The host examines the vector packet to identify which TA is assigned and the frame in which the TA is expected.
4. The PCD5008 continues to decode all of the frames and passes any address information, vector information and message information to the host followed by a status packet indicating the end of each frame and the current frame number.
5. The host processes data packets received while the PCD5008 is in AFM. It uses the AFM packet to decrement the appropriate TA counter when no further data can be expected for the corresponding TA. This occurs when:
   a) The TA is not found in the assigned frame.
   b) The TA is found in the frame it was assigned and was not a fragmented message.
   c) The TA is found in the assigned frame was a fragmented message and the rules for message fragmentation (Section 8.8.5) indicate that no further data can be expected. In this case the host must send an AFM packet with both the DAF and the appropriate DTA bits set in order to terminate both the fragmented message and the TA.
6. The above operation is repeated for every enabled TA.

8.8.5 MESSAGE FRAGMENTATION

The FLEX™ frame length limits the maximum number of message codewords that can be associated with an address codeword. Messages longer than 84 codewords must be sent as several fragments. The PCD5008 uses AFM (Section 8.8.3) to allow the reception of fragmented messages.

The fragments of a message are sent in sequence. Each fragment contains a checksum character to detect errors in the fragment, a message number to identify which message the fragment is a part, and the continue bit which either indicates that more fragments are in queue or that the last fragment has been received. Each fragment also contains a fragment number starting with 3 for the first fragment and then incremented through the sequence 0, 1 or 2 in subsequent fragments. This allows the detection of missing fragments.

Message fragments may not be separated by more than 32 frames (1 minute) or 128 frames (4 minutes), as indicated by the service provider. During the reception of a fragmented message, the PCD5008 examines every frame for additional fragments until the last fragment is encountered or the host determines that more than 32 or 128 frames have elapsed since the reception of the previous message fragment.

The sequence for the host and the PCD5008 to receive a fragmented message is as follows:

1. The PCD5008 receives an address codeword followed by a vector indicating one of:
   a) Secure (vector type = 000)
   b) Alphanumeric (vector type = 101)
   c) Hexadecimal/binary (vector type = 110).

   The PCD5008 passes the address, vector and message codewords to the host as packets and increments its internal AFM counter and enters AFM.
2. While in AFM, the PCD5008 decodes all of the frames passing any address, vector and message information to the host followed by a status packet indicating the end of each frame and the current frame number.
3. Every time the host receives a secure, alphanumeric or hexadecimal/binary vector packet, it inspects the message continued flag (C) in the first message packet:
   a) If this is not a fragmented message (C is clear and no fragmented messages are in progress for this address and message number), then the host decrements the AFM counter by sending an AFM packet to the PCD5008 with the DAF bit set. If the fragmented message was received on a temporary address, then the appropriate DTA bit should also be set in the AFM packet.
   b) If this is the first fragment of a fragmented message (C is set and no fragmented messages are in progress for this address and message number), then the host does not decrement the AFM counter and expects further fragments to be received for this address in subsequent frames.
   c) If this is the second or subsequent fragment of a fragmented message and further fragments will follow, (C is set and a fragmented message is in progress for this address and message number), then the host decrements the AFM counter by sending an AFM packet to the PCD5008 with the DAF bit set.
   d) If this is the last fragment of a fragmented message, (C is clear and a fragmented message is in progress for this address and message number), then the host decrements the AFM counter by 2, sending 2 AFM packets to the PCD5008 with the DAF bit set. If the fragmented message was received on a TA, then one of these AFM packets should also have the appropriate DTA bit set.
4. If, on receiving a status packet, the host determines that more than 32 or 128 frames have elapsed since the reception of a fragment for a fragmented message then the host decrements the AFM counter by sending an AFM packet to the PCD5008 with the DAF bit set. If the fragmented message was received on a TA, then the appropriate DTA bit should also be set in the AFM packet.
5. When no fragmented messages are in progress (the AFM counter = 0) and no TAs are pending (all TA counters = 0) and the FAF bit is clear in the AFM packet, the PCD5008 leaves AFM.

As an alternative to the above scheme, the host may choose to decrement the AFM counter at the end of the entire message by decrementing it once for each fragment received. This method is limited to a maximum of 127 fragments.

Tables 57 and 58 show examples of message reception with and without message fragmentation.

Table 57 Alphanumeric message without fragmentation

PACKET		PHASE	AFM COUNTER	COMMENT
NUMBER	TYPE			
1st	address 1	A	0	address 1 is received
2nd	vector 1	A	1	vector = alphanumeric type
3rd	message	A	1	message word received; C bit = 0; no more fragments are expected
4th	AFM		0	host writes AFM packet to the PCD5008 with the DAF bit = 1

Table 58 Alphanumeric message with fragmentation

PACKET		PHASE	AFM COUNTER	COMMENT
NUMBER	TYPE			
1st	address 1	A	0	address 1 is received
2nd	vector 1	A	1	vector = alphanumeric type
3rd	message	A	1	message word received; C bit = 1; message is fragmented, more expected
4th	status		1	end of frame indication (EOF = 1)
5th	address 1	B	1	address 1 is received
6th	vector 1	B	2	vector = alphanumeric type
7th	message	B	2	message word received; C bit = 1; message is fragmented, more expected
8th	AFM		1	host writes AFM packet to the PCD5008 with the DAF bit = 1
9th	status		1	end of frame indication (EOF = 1)
10th	address 1	A	1	address 1 is received
11th	vector 1	A	2	vector = alphanumeric type
12th	message	A	2	message word received; C bit = 0; no more fragments are expected
13th	AFM		1	host writes AFM packet to the PCD5008 with the DAF bit = 1
14th	AFM		0	host writes AFM packet to the PCD5008 with the DAF bit = 1

8.8.5.1 Fragmentation of non-7-Bit character sets

FLEX™ alphanumeric messages can be used to send symbolic characters like Chinese, Kanji, etc. In this case several ASCII characters are used to represent each symbolic character. Enhanced fragmentation (EF) rules are provided by FLEX™ to allow character positions within a fragment to be determined in the event of missing fragments under poor signal conditions:

1. The pager must remove <NUL> characters from the end of fragments (where they are used as fill characters) so that the displayed message is not affected. To determine character boundaries, <NUL> (00H) characters in all other positions must be considered a result of channel errors. This allows each fragment to end with a complete character and does not disrupt pagers which do not follow all the EF rules.
2. The last fragment of a message containing symbolic characters is completed by filling unused character positions with <ETX> (03H) characters or <NUL> characters. When a message ends at exactly the last character position of the last BCH codeword, no additional <ETX> is required.
3. The U and V bits (Table 45) which aid decoding, are available in all fragments following the initial fragment. In the first fragment the message starts in the default character mode (U and V = 10). For subsequent fragments the definition of the U and V field is as shown in Table 59. When the U and V field is 00, characters may be split between fragments. When the U and V field is not 00, each fragment starts on a character boundary with the character mode defined as in Table 59.

8.8.6 MESSAGE CHECKSUMS

FLEX™ provides a message checksum facility for alphanumeric, numeric, hex/binary, and secure messages. The checksum is calculated by summing the information bits of each codeword in the message or message fragment (including control information and termination characters and bits in the last message codeword). Information bits of each codeword are broken into three groups as indicated in Table 60. Bits i_0, i_8 and i_{16} are the LSBs of each group and bit i_0 is the first bit of the codeword to be transmitted. The 3 groups are for each codeword are added to form a binary sum. The message checksum is the 1's complement of the LSBs of the binary sum, where the number of bits taken is determined by the message type (Section 8.7.8).

In the case of the 6-bit message checksum used in numeric messages, a binary sum is first calculated as described above. The binary sum is then truncated to its 8 LSBs, then the 2 MSBs are shifted right by 6 bits and added to the least significant 6 bits to form a new binary sum. The 6 LSBs of this new sum are taken and 1's complemented to form the 6-bit message checksum.

8.8.7 MESSAGE NUMBERING

FLEX™ messages may be numbered (Section 8.7.8), in this case the system controller assigns message numbers (for each paging address separately) starting at 0 and progressing up to a maximum of 63 in numerical order. The maximum roll-over number is defined in the pager code plug to accommodate values set in the system infrastructure. When message numbers are not received in order, the subscriber should assume a message has been missed. When a message number is missed, the subscriber or the pager may determine the missing message number(s) allowing a request to be made for retrieval.

Messages which can be received out of sequence are indicated by clearing the message retrieval flag R. Messages with R cleared number should not be included in the missed message calculation.

In case of fragmented messages, this number is also used to identify fragments of the same message. Multiple messages to the same address must have separate message numbers.

Table 59 Fragmentation control bit definitions

U_0	V_0	DEFINITION
0	0	EF not supported in controller
0	1	reserved (for a second alternate character mode)
1	0	default character mode start position 1
1	1	alternate character mode start position 1

Table 60 Bit groups for message checksums

i_0	i_1	i_2	i_3	i_4	i_5	i_6	i_7	i_8	i_9	i_{10}	i_{11}	i_{12}	i_{13}	i_{14}	i_{15}	i_{16}	i_{17}	i_{18}	i_{19}	i_{20}
group 1								group 2								group 3				

9 LIMITING VALUES

In accordance with the absolute maximum rating system (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage	note 1	−0.5	+5.0	V
I_{DD}	supply current		–	50	mA
I_I	DC input current (any input)		−10	+10	mA
I_O	DC output current (any output)		−10	+10	mA
V_I	input voltages (all inputs)	note 2	−0.5	V_{DD} + 0.5	V
P_{tot}	total power dissipation		–	300	mW
P_O	power dissipation per output		–	10	mW
T_{amb}	operating ambient temperature		−25	+70	°C
T_{stg}	storage temperature		−65	+150	°C

Notes

1. V_{DD1} and V_{DD2} respectively V_{SS1} and V_{SS2} are internally connected and must be at the same potential.
2. $V_{I(max)}$ = 5.0 V.

10 DC CHARACTERISTICS

T_{amb} = −25 to +70 °C; V_{DD} = 2.2 V; f = 76.8 kHz; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		1.8	2.2	3.6	V
$I_{DD(stby)}$	standby supply current	on = 0; note 1	–	4.2	10	µA
I_{DD}	average operating supply current	on = 1; note 2	–	4.4	–	µA
Digital inputs: OSCPD, TEST2, TEST3, $\overline{\text{RESET}}$, LOBAT, EXTS0, EXTS1, $\overline{\text{SS}}$ and MOSI						
V_{IL}	LOW-level input voltage		–	–	$0.2V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.8V_{DD}$	–	–	V
I_{LI}	LOW/HIGH-level input leakage current		–	–	1	µA
Digital outputs: MISO, $\overline{\text{READY}}$, CLKOUT, SYMCLK and S0 to S7						
V_{OL}	LOW-level output voltage	I_{sink} = 0.8 mA	–	0.12	0.4	V
V_{OH}	HIGH-level output voltage	I_{source} = −0.8 mA	V_{DD} − 0.4	V_{DD} − 0.15	–	V
I_{LO}	LOW/HIGH-level output leakage current	3-state outputs	–	–	1	µA

Notes

1. External clock signal (frequency = 76.8 kHz, amplitude = V_{SS} to V_{DD}) at pin EXTAL; OSCPD = HIGH; test inputs = LOW; other Inputs = HIGH; outputs unconnected (note that any additional capacitive load at pin CLKOUT increases the supply current); SPI transmit enabled; to obtain the supply current of an application with a crystal connected as in Fig.18, a typical oscillator current of 2.4 µA needs to be added to this value (see Chapter 12); T_{amb} = 25 °C.
2. As note 1, but PCD5008 configured via SPI and synchronous to a typical FLEX™ data stream (collapse value = 4), T_{amb} = 25 °C.

11 AC CHARACTERISTICS

T_{amb} = −25 to +70 °C, V_{DD} = 1.8 to 3.6 V, f_{EXTAL} = 76.8 kHz, maximum load capacitance = 50 pF connected to any digital output; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reset timing						
$t_{W(rst)}$	$\overline{\text{RESET}}$ pulse width		200	–	–	ns
$t_{LH(RESET-READY)}$	$\overline{\text{RESET}}$ LOW to $\overline{\text{READY}}$ HIGH		–	–	200	ns
$t_{HL(RESET-READY)}$	$\overline{\text{RESET}}$ HIGH to $\overline{\text{READY}}$ LOW	stable 76.8 kHz clock	–	1	–	s
Start-up timing						
$t_{strt(osc)}$	oscillator start-up time	as Fig.18	–	1	–	s
$t_{h(rst)}$	$\overline{\text{RESET}}$ hold time		200	–	–	ns
$t_{HL(RESET-READY)}$	$\overline{\text{RESET}}$ HIGH to $\overline{\text{READY}}$ LOW	note 1	–	76800	–	T
$t_{WUL(osc-READY)}$	oscillator warmed up to $\overline{\text{READY}}$ LOW		–	1	–	s
SPI timing						
f_{SCK}	operating frequency		0	–	1	MHz
$T_{cy(SCK)}$	cycle time		1000	–	–	ns
t_{LEAD1}	select lead time		200	–	–	ns
t_{LAG1}	de-select lag time		200	–	–	ns
$t_{d(SS-READY)}$	$\overline{\text{SS}}$-to-$\overline{\text{READY}}$ delay time	previous packet did not program an address word; note 2	–	–	80	µs
		previous packet programmed an address word; note 2	–	–	420	µs
t_{READYH}	$\overline{\text{READY}}$ HIGH time		50	–	–	µs
t_{LEAD2}	$\overline{\text{READY}}$ lead time		200	–	–	ns
t_{LAG2}	$\overline{\text{READY}}$ lag time		–	–	200	ns
$t_{su(i)(D)}$	MOSI data setup time		200	–	–	ns
$t_{h(i)(D)}$	MOSI data hold time		200	–	–	ns
$t_{ACC(o)}$	MISO access time		0	–	200	ns
$t_{o(dis)}$	MISO disable time		–	–	300	ns
t_{DOV}	MISO data valid time		–	–	200	ns
$t_{h(Q)}$	MISO data hold time		0	–	–	ns
t_{SSH}	$\overline{\text{SS}}$ HIGH time		200	–	–	ns
t_{SCKH}	SCK HIGH time		300	–	–	ns
t_{SCKL}	SCK LOW time		300	–	–	ns
t_r	SCK rise time	10% to 90% V_{DD}	–	–	1	µs
t_f	SCK fall time	10% to 90% V_{DD}	–	–	1	µs

Notes

1. T is one period of the 76.8 kHz clock source. Note that from power-up, the oscillator start-up time can influence the availability and period of clock strobes. This can affect the $\overline{\text{RESET}}$ HIGH to $\overline{\text{READY}}$ LOW timing.
2. When the host re-programs an address word with a host-to-decoder packet ID > 7FH, there is an added delay before the PCD5008 is ready for another packet.

12 OSCILLATOR CHARACTERISTICS

T_{amb} = −25 to +70 °C; note 1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_1	external capacitor at pin EXTAL	note 1	–	15	–	pF
C_2	external capacitor at pin XTAL	note 1	–	15	–	pF
R_f	external feedback resistor	note 1	–	10	–	MΩ
$g_{m(osc)}$	oscillator transconductance	V_{DD} = 1.8 V	9.4	16	–	µS
$g_{m(osc)}$	oscillator transconductance	V_{DD} = 3.6 V	–	24	50	µS
I_{osc}	oscillator operating supply current	V_{DD} = 2.2 V; note 2	–	2.4	–	µA

Notes

1. Designed for quartz crystal type: SEIKO VTC200 or equivalent; Parameters: f = 76800Hz, R_S = 35 kΩ (max.), $C_L = (C_1 // C_2) + C_{stray}$ = 8 to 12 pF, C_0 = crystal shunt capacitance = 0.8 pF (typ.), C_f = typical parasitic pin capacitance = 2 pF; maximum overall frequency tolerance (including transmitter) is 300 ppm (Section 8.4.4).
2. Extracted from evaluations under conditions as in Fig.18; this value is strongly dependent on external conditions (load and parasitic capacitances).

13 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	80	K/W

14 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

15 QUALITY SPECIFICATION

In accordance with *"SNW-FQ-611-E"*. The number of the quality specification can be found in the *"Quality Reference Handbook"*. The handbook can be ordered using the code 9397 750 00192.

16 TEST AND APPLICATION INFORMATION

16.1 Example application

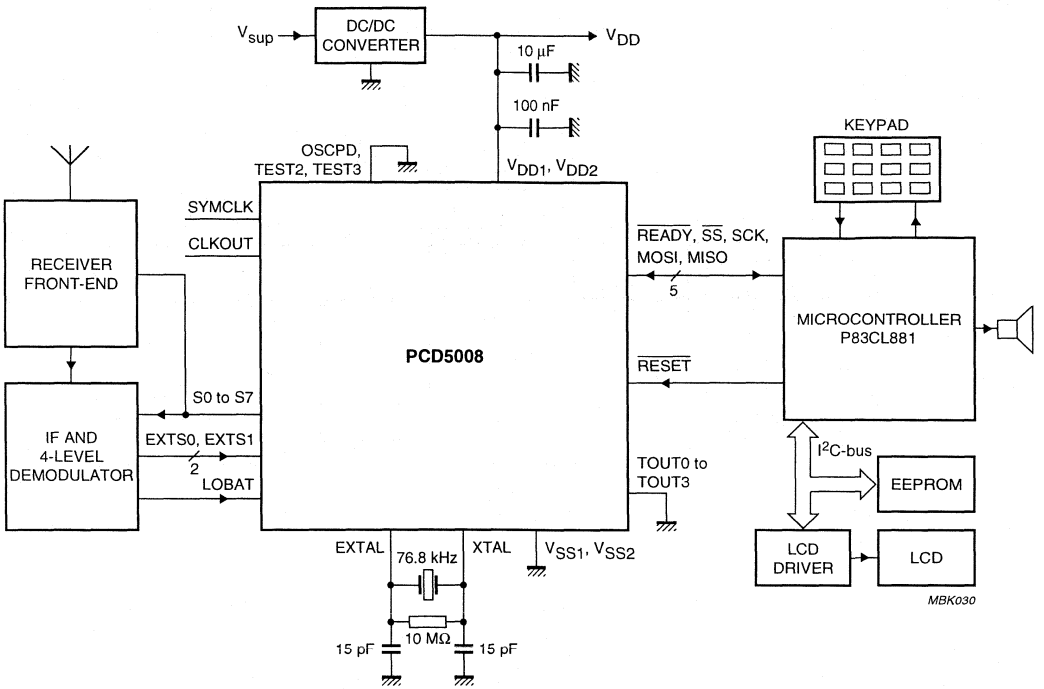

Fig.18 Example application.

16.2 System block diagram

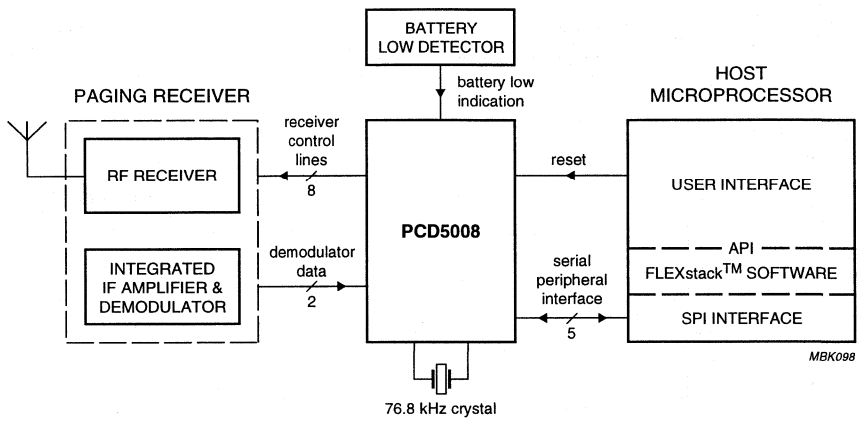

Fig.19 System block diagram.

16.3 FLEX™ encoding and decoding rules

The encoding and decoding rules identify the minimum requirements which must be met by the paging device, paging terminal or other encoding equipment to properly format a FLEX™ data stream for RF transmission and to successfully decode it.

16.3.1 FLEX™ ENCODING RULES

The FLEX™ encoding rules are as follows:

- The stability of the encoder clock used to establish time positions of FLEX™ frames must be no worse than ±25 ppm (including worst case temperature and aging effects).
- A maximum of 2 occurrences of an identical individual or radio group address is allowed in any frame for unfragmented messages. This rule applies across all phases in a multi-phase frame. For example, for decoding devices that support any-phase addressing, an any-phase address may appear at once in two different phases in a single multi-phase frame.
- Once an individual or radio group address is used to begin transmitting a fragmented message, that same address must not be used to start a new fragmented transmission until the first fragmented transmission has been completed.
- For the duration of time that an individual or radio group address is being used to send a fragmented message, that same address must not appear more than once in any frame to send an unfragmented message.
- Once a specific dynamic group address (temporary address) is assigned to a group, it must not be reused until its associated message has been transmitted in its entirety. Given this constraint, the same dynamic group address can only appear once in any frame.
- A dynamic group address cannot be used to set up a second dynamic group.
- Messages using any of the three defined numeric vectors ($V_2V_1V_0$ = 011, 100 and 111) cannot be fragmented, and thus must be completely contained in a single frame.
- Fragments of the same message must be sent at a frequency of at least 1 every 32 frames (i.e. at least once a minute) or 1 every 128 frames (i.e. at least once every 4 minutes) as specified by the service provider.
- Enhanced message fragmenting for symbolic character transmission requires that the encoder track character boundaries within each fragment in order to avoid character splitting.
- Message numbering as an optional feature is offered by some carriers and available on an individual subscriber basis.
- Message numbers must be assigned sequentially in ascending order.
- Message number sequences must be separately maintained for each individual and radio group address.
- Message numbers are not used (retrieval message number disabled) in conjunction with a dynamic group address.
- When a missed message is re-transmitted from message retrieval storage, the message must have R = 0 to avoid creating an out of sequence message which may cause the pager to indicate a missed message.

16.3.2 FLEX™ DECODING RULES

The FLEX™ decoding rules are as follows:

- FLEX™ decoding devices may implement either single-phase addressing or any-phase addressing.
- FLEX™ decoding devices that support the numeric vector type ($V_2V_1V_0$ = 011) must also support the short message vector ($V_2V_1V_0$ = 010) with the message type (t_1t_0) set to 00.
- FLEX™ decoding devices that support the alphanumeric vector type ($V_2V_1V_0$ = 101) must support the numeric vector type ($V_2V_1V_0$ = 011) and the short message vector ($V_2V_1V_0$ = 010) with the message type (t_1t_0) set to 00, FLEX™ paging devices that implement any-phase and support the alphanumeric vector type ($V_2V_1V_0$ = 101) must also support the short instruction vector ($V_2V_1V_0$ = 001) with the instruction type ($i_2i_1i_0$) set to 000.
- FLEX™ decoding devices must be capable of decoding frames at all of the following combinations of data rate and modulation mode. They are: 1600 bps 2 level; 3200 bps 2 level; 3200 4 level and 6400 bps 4 level.
- FLEX™ decoding devices must be designed to tolerate 4 minute fragment separation times.

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1 FEATURES

- On-chip pre-programmed Communication Controller with embedded firmware for implementation of Traffic Bearer Control (TBC), MAC message handling, scanning, and control of the device's other functional units.
- Portable Part (PP) modes
- TDMA frame (de)multiplexing
- Encryption
- Scrambling
- CRC generation and checking
- Beacon transmission control (by P00 packets)
- On-chip comparator for receive data slicer function (only available in the LQFP80 package)
- Switches up to12 active speech channels from speech interface to 1152 kbit/s. radio interface, and vice versa
- Dual channel speech/data capability
- Received Signal Strength Indication (RSSI) measurement, with on-chip 6-bits peak/hold detector
- Quality control report
- Digital Phase Locked Loop (DPLL)
- Synchronization (handset to active bearer, base station to cluster of RFPs)
- Seamless handover procedure
- Fast (hardware) and slow (software) mute function
- 1 kbyte extended RAM memory
- On-chip crystal oscillator (13.824 MHz)
- Programmable microcontroller clock frequency
- Programmable interrupts
- Watchdog with two programmable time-outs
- Low power consumption in standby mode
- Low supply voltage (2.7 to 5.5 V)
- SACMOS technology.

2 GENERAL DESCRIPTION

The PCD5041 DECT Burst Mode Controller (BMC) is a custom IC that performs the DECT Physical Layer and MAC Layer time-critical functions, for use in DECT handset products which comply with the following standards (and updates):

- DECT CI part 2: Physical layer (DE/RES 3001-2)
- DECT CI part 3 : Medium Access Control layer (DE/RES 3001-3)
- DECT CI part 7: Security features for DECT (DE/RES 3001-7)
- DECT CI part 9: Public Access Profile (DE/RES 3001-9).

The PCD5041 has interfaces to:

- ADPCM CODECs in the handset mode
- A radio transceiver; the interface is fully decoded, and includes power-down signals
- An external microcontroller.

The PCD5041 is designed to be connected to an ADPCM CODEC (Philips' PCD5032, for example) and an 80C51-type microcontroller. Other microcontrollers (e.g. 68000) and CODECs can also be supported.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD5041H	QFP64	plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT319-2
PCD5041HZ	LQFP80	plastic low profile quad flat package; 80 leads; body 12 × 12 × 1.4 mm	SOT315-1

4 BLOCK DIAGRAM

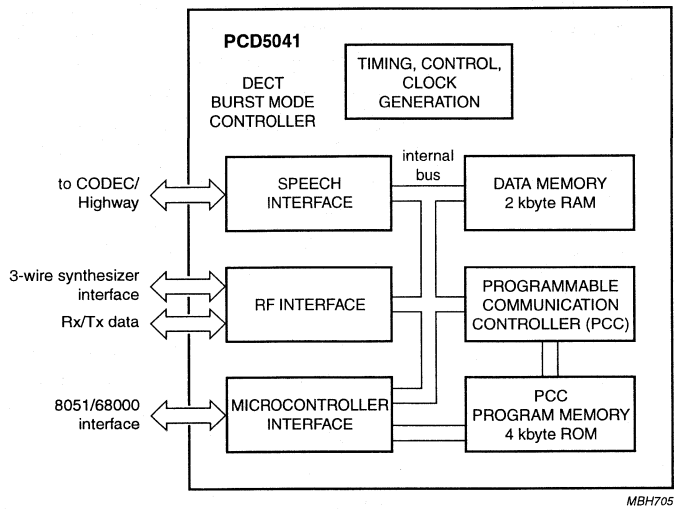

Fig.1 Block diagram.

5 PINNING (see Figs 2 and 3)

SYMBOL	PIN		TYPE[2]	DESCRIPTION
	QFP64	LQFP80[1]		
AD0 to AD7	1 to 8	80, 1, and 3 to 7	I/O	address/Data bus
ALE	9	9	I	address latch enable
$\overline{CS}$	10	11	I	chip select (active LOW)
A8 to A10	13 to 11	14 to 12	I	address bus
V_{DD1}	14	15	P	positive supply 1
PROC_CLK	15	16	O	microcontroller clock; programmable from $f_{CLK}/64$ to f_{CLK}, where f_{CLK} is the crystal oscillator frequency
V_{SS1}	16	17	P	negative supply 1
XTAL1	17	20	I	crystal oscillator input
XTAL2	18	21	O	crystal oscillator output
V_{SS2}	19	22	P	negative supply
RESET_OUT	20	23	O	watchdog timer output; intended to reset the external microcontroller when expired
$\overline{RD}$	21	24	I	read (active LOW)
$\overline{WR}$	22	25	I	write (active LOW)
$\overline{RDY}$	23	26	O	ready signal (active LOW), to initiate wait states in the microcontroller (open drain)

SYMBOL	PIN		TYPE[2]	DESCRIPTION
	QFP64	LQFP80[1]		
$\overline{INT}$	24	27	O	interrupt (active LOW)
CLK100	25	29	O	100 Hz frame timer
V_{SS3}	26	31	P	negative supply 3
DO	27	32	O	3-state data output on the speech interface
FS3	–	33	I/O	8 kHz framing signal to ADPCM CODEC 1 output, for simple base + handset, otherwise 8 kHz framing input
FS1	28	34	I/O	8 kHz framing signal to ADPCM CODEC 1 output, for simple base + handset, otherwise 8 kHz framing input
FS4	–	35	I/O	8 kHz framing signal to ADPCM CODEC 1 output, for simple base + handset, otherwise 8 kHz framing input
FS2	29	36	O	8 kHz framing signal to ADPCM CODEC 2 in the base station mode
DI	30	37	I	data input on the speech interface
DCK	31	38	O	simple base + handset; 1152 kHz data clock (output), otherwise 2048 kHz data clock (input) signal
CLK3	32	39	O	3.456 MHz clock (nominal value, used to adjust system timing)
ANT_SW	33	40	O	selects one of two antennas
$\overline{T\_ENABLE}$	34	41	O	Transmitter Enable (active LOW)
T_POWER_RMP	35	43	O	Transmitter Power Ramp control
RMT_STAT	36	44	I	serial 8-bit data can be read in for each slot; REMote radio
SYNTH_LOCK	37	45	I	lock indication from synthesizer
V_{SS4}	38	46	P	negative supply 4
REF_CLK	39	47	O	reference frequency for the synthesizer, i.e. the crystal oscillator clock f_{CLK}
V_{DD2}	40	48	P	positive supply 2
S_ENABLE	41	49	O	synthesizer enable
S_CLK	42	51	O	clock signal, to be used with S_DATA
S_DATA	43	52	O	serial data to the synthesizer
S_POWER_DWN	44	53	O	synthesizer power-down control
VCO_BND_SW	45	54	O	VCO bandswitch control signal
1200 HZ	46	55	O	control signal for dual synthesizer schemes
T_DATA	47	56	O	serial output data to transmitter
SET_OFF_IN	48	57	I	switches off the crystal oscillator, and prevents all RF signals from becoming active
TEST1	49	58	I	selects various test modes.; normal operation set to 0
RSSI_AN	50	60	I	analog signal (for basic DECT systems), peak signal strength measured after a lowpass filter
TEST2	51	–	I	selects various test modes; normal operation set to 0
TEST3	52	61	I	selects various test modes; normal operation set to 0
R_DATA	53	63	I	receive data

SYMBOL	PIN		TYPE[2]	DESCRIPTION
	QFP64	LQFP80[1]		
$\overline{R\_ENABLE}$	54	64	O	receiver enable (active LOW)
R_POWER_DWN	55	65	O	receiver power-down
$\overline{COMP\_NE}$	–	66	I	digital input comparator not_enable (active LOW)
SLICE_CTR	56	67	O	slice time constant control
COMP_OUT	–	68	O	digital comparator output
V_{DD3}	57	69	P	positive supply 3
V_{SS5}	58	70	P	negative supply 5
COMP_INM	–	71	I	analog comparator input negative
V_{REF}	59	72	I	reference input for the A/D converter
COMP_INP	–	73	I	analog input positive
$V_{DD(RAM)}$	60	74	P	power supply for data RAM
SYNCPORT	61	76	I/O	in the base station the signal is the SYNCPORT
RESET	62	77	I	BMC master reset signal
MEM_SEL	63	78	I	selects PCC program memory at microcontroller interface
EN_WATCHDOG	64	79	I	enable watchdog input; when HIGH, the watchdog timer of the BMC is enabled

Notes

1. Un-referenced pins for the LQFP80 package are not connected. FS3, FS4 and the comparator signals are only available in the LQFP80 package.
2. **All** signals which are input or I/O, and which can be floating, need to be pulled up to V_{DD} or down to V_{SS} in order to protect the device against cross-currents. Exceptions are VREF and RSSI_AN, which do not have to be protected.

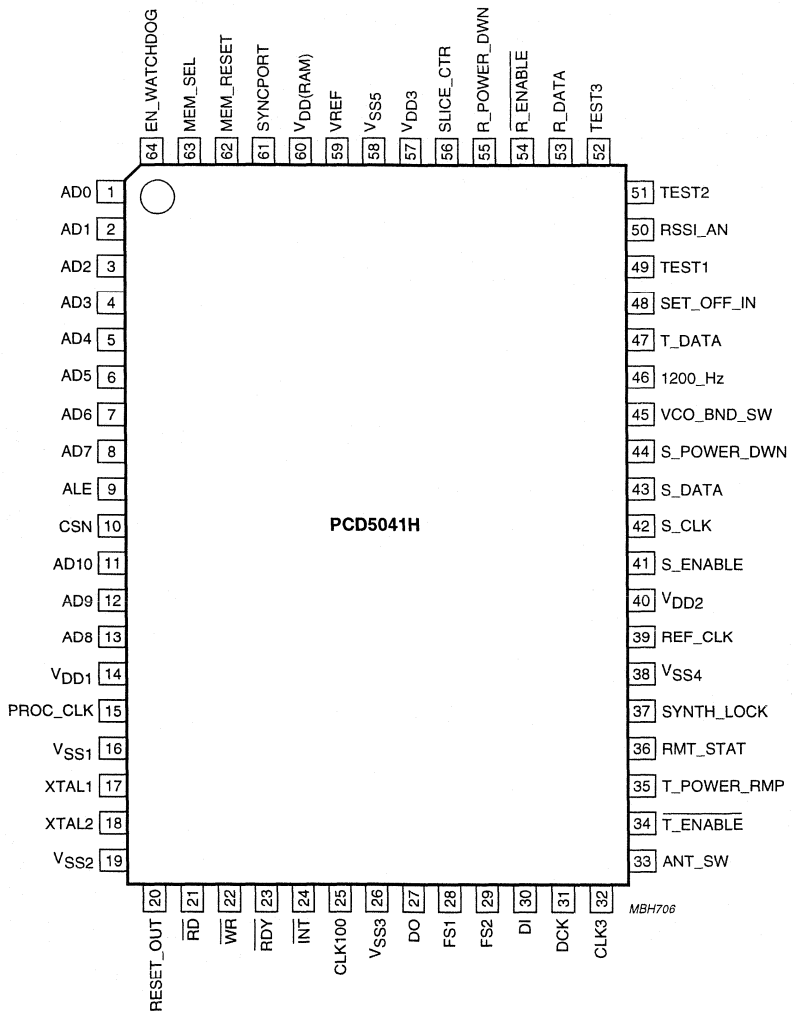

Fig.2 Pin configuration, PCD5041H (QFP64 package).

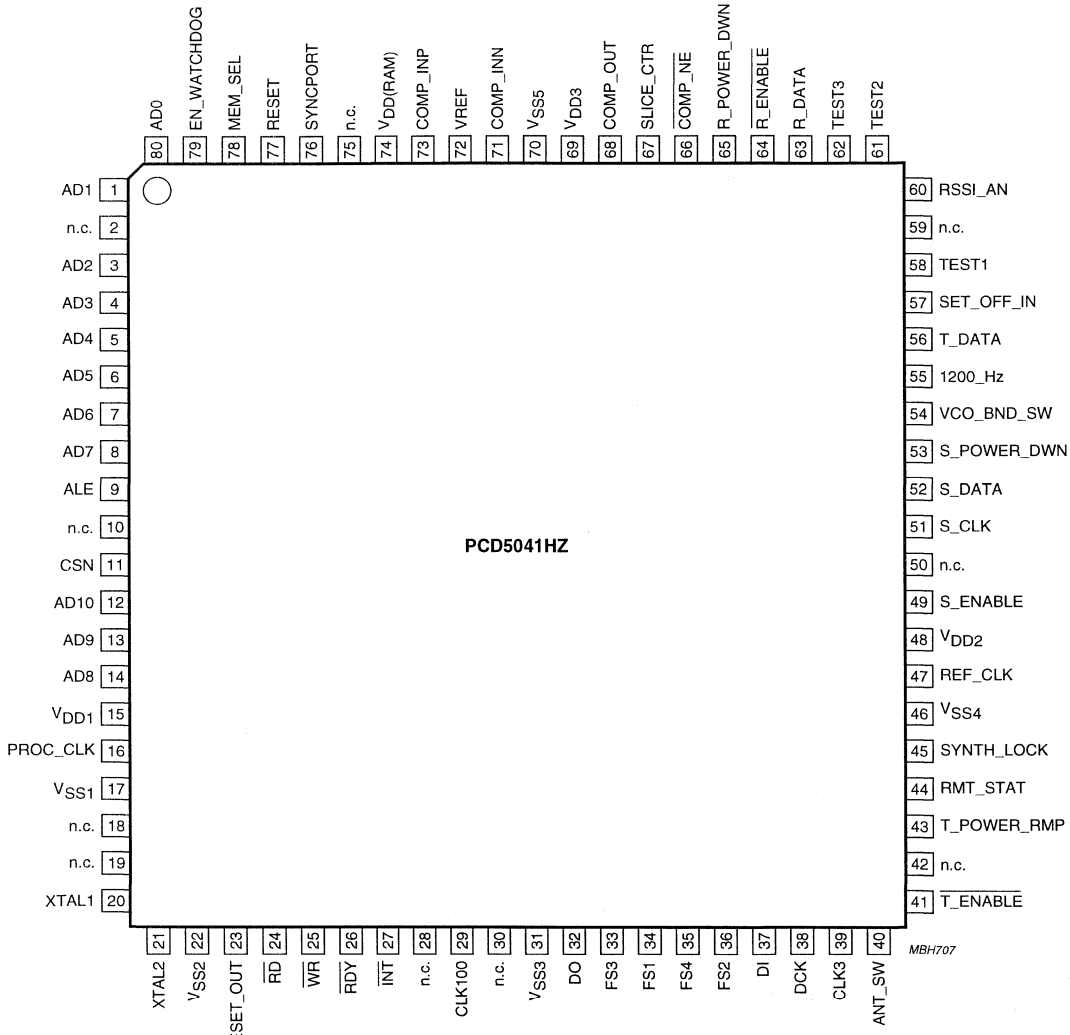

Fig.3 Pin configuration, PCD5041HZ (LQFP80 package).

6 FUNCTIONAL DESCRIPTION (see Fig.1)

The PCD5041 has dedicated hardware blocks containing logic for time-critical functions requiring bit or byte-time accuracy. Other functions requiring only slot-time accuracy are performed by software in the Programmable Communication Controller (PCC). This approach offers maximum flexibility during prototyping.

6.1 Internal bus and data memory

6.1.1 INTERNAL BUS

The function of the internal bus is:

- To provide access for all functional blocks to the common data memory
- To provide access for the microcontroller-interface and the PCC to all other functional blocks.

All functional blocks (speech-interface, RF-interface, microcontroller-interface and PCC) can autonomously use the internal bus to communicate with the common data memory.

A bus controller is used to handle the bus priority mechanism. When several blocks request access simultaneously, the request with the highest priority is handled first.

6.1.2 DATA MEMORY

A large part of the data memory is used for the bit rate adaptation between the DECT radio interface and the speech interface. The data memory also acts as the main communication interface between the external microprocessor and the PCC.

In a handset, the device uses only 1 kbyte of the common data memory. The remaining 1 kbyte can be used by the microcontroller as an extended data memory for the higher layer software. The microcontroller is not aware of the fact that it is sharing the memory with the PCD5041. From the microcontroller's point of view, the PCD5041's microcontroller-interface plus the common data memory behave as a standard RAM device.

6.2 Clock generation and correction (see Fig.4)

The device has an on-chip 13.824 MHz crystal oscillator. From this source, a few frequencies are derived for internal and external use. Frequencies generated for external use are:

- 13.824 MHz for the synthesizer reference (pin REF_CLK). This output is only provided if the synthesizer power-down control (output on pin S_POWER_DWN) is not selected.
- 0.144 to 13.824 MHz for the microcontroller clock (pin PROC_CLK)
- 3.456 MHz for the ADPCM CODEC (pin CLK3)
- 1200 Hz (pin 1200_HZ) for dual synthesizer switching
- 100 Hz (pin CLK100) indicates start of frame.

Nominally, the frequency on pin CLK3 is 3.456 MHz. This frequency is obtained by dividing the crystal frequency by 4. Sometimes, the crystal frequency will be divided by 3 or by 5, to synchronize the combination of the ADPCM CODEC and the device to an external source. For the handset application, the PCD5041 can be synchronized to the incoming radio channel, using the 'slot synchronization' event of one active channel, so the handset is locked to one base station.

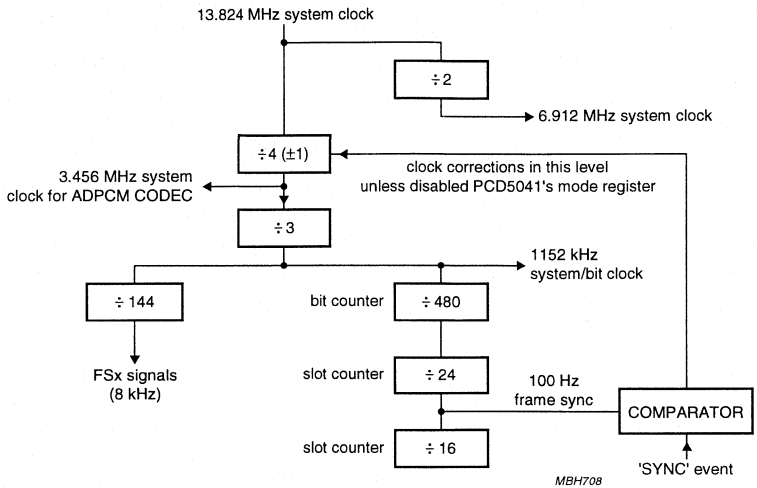

Fig.4 Internal clocking scheme of the PCD5041.

6.3 Programmable communication controller and program memory

6.3.1 PCC

The PCC is a RISC-type controller and is used to control functions which are slot-time accurate. It is well suited for bit manipulation, and runs at a clock frequency of 6.912 MHz (equivalent to 3.4Mips). After finishing a task, it switches to a power saving state, from which it returns after a pre-programmed time.

6.3.2 PCC FUNCTIONS

The most important functions of the PCC are to:

- Perform the appropriate actions on received messages: PMID and FMID checking, RFPI checking, TBC handling
- Prepare A-field messages for transmission
- Prepare the RF-interface for the coming slot
- Perform the procedures for RSSI and set-up scan, maintain scan counters and timers, assemble the RSSI field in the common data memory
- Filter events and indicate them to the microcontroller by interrupt.

6.4 Speech interface

The speech interface block performs the following functions:

- Connection to a 1152 kbit/s interface in a handset and a simple base station in the so called '12 slot mode'
- Autonomous storing/fetching of ADPCM speech data in/from the PCD5041's common data memory, using internal addressing logic
- Muting of speech data
- Local call.

6.4.1 12-SLOT MODE

This is the normal operating mode for the PCD5041. The 12-slot mode is selected if up to 4 ADPCM CODECs are connected to the PCD5041, where the PCD5041 is the master of these CODECs. In a handset, or in a simple base stations which is connected with up to 4 analog lines to the public network, the PCD5041 is master of the CODECs. Each CODEC is connected with a separate framing reference signal (FS1 to FS4) to the PCD5041. In the QFP64 package, 2 framing signals FS1 and FS2 are available, whereas in the LQFP80 package 4 framing signals can be used (FS1 to FS4). When more CODECs

are to be connected, the FS5 to FS12 signals have to be generated externally. When using the framing signals FS1 to FS4, no interface logic is required when using the PCD5032 ADPCM CODEC.

A speech-slot control table is used to determine where to store/fetch speech data for transmission and reception. The hardware speech-interface is capable of addressing the right speech buffer for the relevant speech slot, and will maintain a counter carrying the offset to the correct stored/fetched address.

6.4.2 MUTING

Due to various reasons the quality of the incoming speech data may be degraded significantly. By muting the speech data, these disturbances are not audible (or are less audible) to the user. The PCD5041 performs two types of muting:

- Fast muting
- Slow muting.

Fast muting, which is performed by the PCD5041 automatically, is nothing more than a repetition of the previously received frame (80 speech samples) to the ADPCM CODEC. It is issued if no Sync word was detected. Slow muting is issued by the microcontroller, after having detected a degradation of quality. A slow mute is implemented as a continuous '0000' nibble transmission to the ADPCM CODEC, until slow mute is released.

6.4.3 LOCAL CALL

A local call option is implemented, in order to loopback data from one CODEC to another CODEC, and vice versa, see Fig.5.

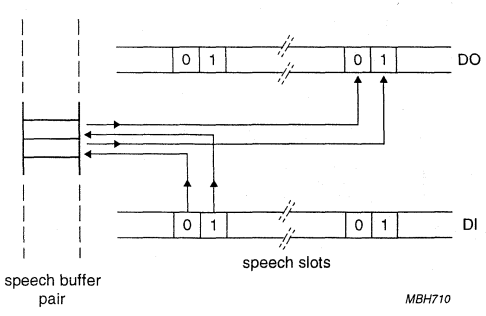

Fig.5 Local call switching on speech interface.

6.5 RF interface

Most of the functions performed by the RF interface are under control of the PCC. Specifically, the processing of non-speech data and the programming of functions and registers is done via the PCC.

6.5.1 SERIAL TRANSMITTER

The serial receiver processes the data, which comes from the RF section, and which is already filtered by the synchronization part. The data is latched, using the recovered data clock.

The serial receiver will collect the complete A-field and B-field and store it in the common data memory. Before the A-field is received, the A-field start address is programmed by the PCC. Upon reception of A-field nibbles, the address is updated by the serial receiver. Meanwhile, the PCC will program the B-field start address.

In Fig.6 the data flow in the serial receiver is shown. Note that almost no decoding of messages is required. Only the header of the A-field needs to be decoded to check if a ciphered message is being received or transmitted, which requires the ciphering to be switched on in the A-field also.

6.5.2 SERIAL RECEIVER

The serial transmitter performs the reverse of the receiver functions. Several blocks used in the receiver are also used in the transmitter. Amongst these are the CRC-generators, the scrambler, and the address registers. Figure 7 shows the serial transmitter structure.

By transmitting the X-CRC twice, the Z-field is transmitted. The handling of the address registers is the same for the transmitter. Transmission of the synchronization sequence (S-field) is done using the same method as the A-field and B-field. The S-field is stored in the common data memory and will be fetched by the transmitter, just before transmission.

Two additional functions are not shown in Fig.7:

- In the handset the data in the serial transmitter may be advanced by a programmable number of bit periods. This is done to compensate for the delay in the RF section
- The transmitted data can be inverted (using a switch in the PCD5041 mode register), in order to connect the PCD5041 to VCOs requiring negative modulation.

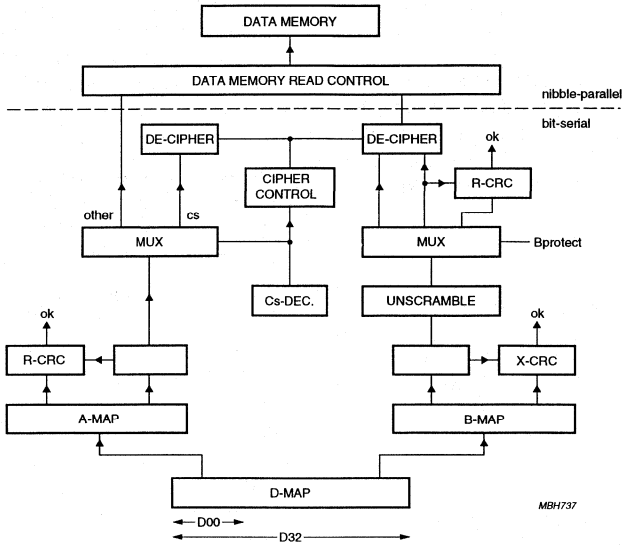

Fig.6 Serial receiver structure.

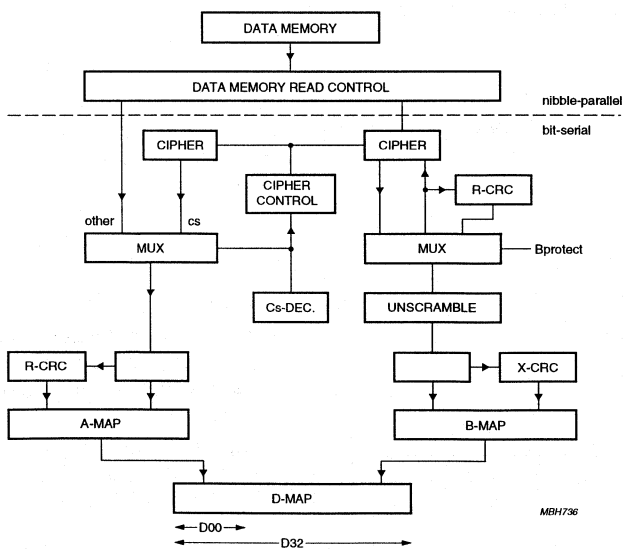

Fig.7 Serial transmitter structure.

6.5.3 SEAMLESS HANDOVER

Seamless handover guarantees that when speech information is switched from one slot to another, no speech samples are lost, added or displaced. Seamless handover is achieved in the RF interface by:

- Using a look-up table containing the correct start addresses of the B-fields in the data memory
- The RF receive and transmit blocks move data to/from the data memory block in 4-bit nibbles.

6.5.4 RF CONTROL SIGNALS

The timing of the control signals to the RF section is fixed, but such that an RF delay between 1.5 and 7 µs can be tolerated. Only the transmitter ramp signal and the synthesizer enable are programmable within certain limits.

6.5.5 SYNTHESIZER PROGRAMMING

To program a synthesizer, a 3-wire serial interface is used. The signals on this interface are:

- S_ENABLE (enable)
- S_CLK (clock)
- S_DATA (data).

To program various types of synthesizers, a 3-byte shift register is present. Three data formats are supported: 8, 16 or 24 bit words can be selected. The transfer of data from a frequency table in the common data memory to the shift register is under control of the PCC.

6.5.6 RSSI MEASUREMENT (see Fig.8)

The RSSI measurement in the PCD5041 RF-interface block is done in 3 parts: a peak/hold detector, a 6-bit A/D converter, and an RSSI control unit, which controls the peak/hold detector and the A/D converter. Once per slot time, a sample is fetched by the PCC and saved in the appropriate area of the common data memory.

If the radio receiver is active in a particular time slot, the RSSI value will automatically be measured in that slot. Adjustment to the RSSI_AN input level can be made with VREF.

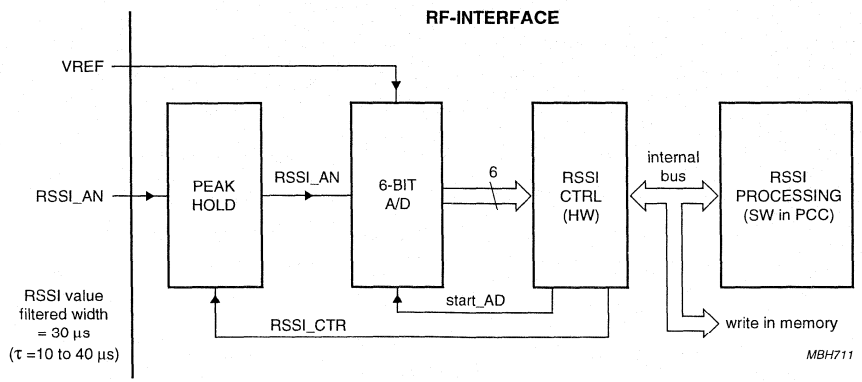

Fig.8 RSSI measurement path.

6.5.7 LOCAL CALL SWITCHING (see Fig.9)

The PCD5041 provides a local call switching function in the base station. It stores incoming speech nibbles in the common data memory, in the area reserved for that particular receive slot. Then, during the transmit phase, it passes the start pointer of the same data memory area to the transmit block. Thus, the speech data is echoed to the other user. To handle quality degradation for local calls, a mute can be performed at the RF side of the speech buffer.

6.5.8 DATA SYNCHRONIZATION (see Fig.10)

The data synchronization is done in 2 phases:

- Bit synchronization
- Sync word detection.

Bit synchronization is done using a Digital PLL (DPLL), with an oversampling factor of 12, i.e. the DPLL is running at 12 times the data rate. The output from the DPLL is a receive clock signal (RxC), which acts as the enable for a 20-bit shift register.

Sync word detection is achieved by checking the incoming data pattern with the expected synchronization field pattern, using a correlator.
The correlator has a programmable threshold, so it can accept bit errors in the sync field pattern up to the threshold level. Furthermore, the correlator window is programmable. This means that 'SlotSync', which indicates the slot synchronization event, can be detected only during a certain period (the time window).

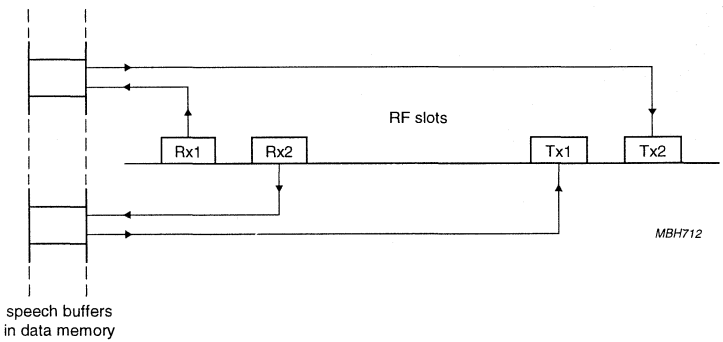

Fig.9 Local call switching on the RF-side.

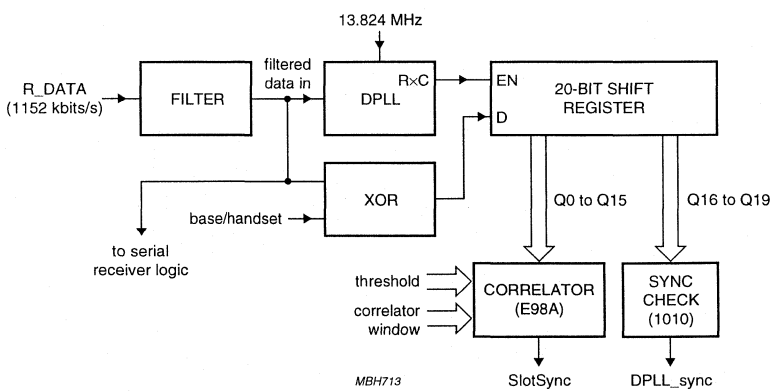

Fig.10 Schematic of the receiver synchronization part.

The 'DPLL_sync' indication should only be used, when 'SlotSync' is active. It indicates that the last 4 bits of the pre-amble field (the training sequence) are received correctly, and thus indicates that the DPLL was in lock (synchronized) in time. If the 'SlotSync' is active, and the 'DPLL_sync' is not, then a sliding interferer might have been detected.

If 'SlotSync' is not detected, effectively no data is received in that slot. This implies a 'fast mute' because speech data received in the previous frame is not destroyed.

6.5.9 CIPHERING MACHINE

The description of the cipher machine is subject to confidentiality. The specification of its algorithms are delivered by ETSI under the terms of a Non-Disclosure Agreement.

The cipher machine is under control of the TBC, which is implemented in the PCC. The cipher machine generates 2 fields of ciphering bits:

- A_cipher (40 bits) for A-field messages (ciphers tail only)
- B_cipher (320 bits) for speech in B-field.

The transmitted ciphered bits are then:

- A_ciphered: = A XOR A_cipher
- B_ciphered: = B XOR B_cipher.

On reception by the peer end point, deciphering consists of the same operation thanks to the synchronous generation of A_cipher and B_cipher.

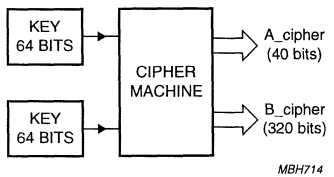

Fig.11 Cipher machine and its sources.

The cipher machine is time-multiplexed on a slot basis. Initially, the Initialisation Vector (IV) and the key must be loaded into the cipher machine. Transfer of the IV and key from the common data area to the cipher machine is done automatically by the cipher machine. The contents of the memory space where IV and key are found, are the responsibility of the PCC, and the external microprocessor.

6.5.10 COMPARATOR/DATA SLICER ON PCD5041HZ

The PCD5041HZ contains a comparator/data slicer. The comparator is a stand-alone circuit. No connections other than power supply are made internally. The comparator can be used as a data slicer for the receiver input. The delay requirements listed in Chapter 8 were derived from this application. Another use of the comparator is in a successive approximation A/D converter to indicate battery low-voltage condition, or in a power-on-reset circuit.

When the signal $\overline{\text{COMP\_NE}}$ is LOW the comparator is enabled. When $\overline{\text{COMP\_NE}}$ is HIGH the comparator is disabled, and the circuit consumes no power. If the comparator is used as a data slicer for the receiver input, the R_DATA is connected to COMP_OUT, the $\overline{\text{COMP\_NE}}$ is connected to $\overline{\text{R\_ENABLE}}$, both connection are done externally. The pin COMP_INP is connected to the RF mixer. A proper bias voltage (from the slicer time constant control circuit) is connected to COMP_INM. Another use of the comparator is in a successive approximation A/D converter for battery voltage detection.

The pins are protected against ESD damaging, with a protection diode to the positive and negative supply rail. The input pin $\overline{\text{COMP\_NE}}$ has a pull-up resistor which keeps the comparator in power-down mode by default.

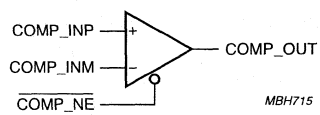

Fig.12 Circuit schematic of the comparator/data slicer.

6.6 Microcontroller Interface

6.6.1 Function of the microcontroller interface

The microcontroller interface will provide the following services.

- Direct interface to processors which have an INTEL-8051 compatible interface
- General interface to processors that can handle 'wait states' e.g. 68000-family; in this case glue logic is required
- Processor clock signal of which the frequency is programmable in order to adjust instantaneously processor performance to processor work load
- A programmable interrupt register
- A watchdog timer with time-out periods of 1.25 or 82 seconds, depending on the programming.

The microcontroller can address the PCD5041 as any other RAM memory connected to the microcontroller bus. By writing the 'Interface-Mode Register', the microcontroller can select the interface mode and its own clock frequency.

6.6.2 Microcontroller interrupts

The function of microcontroller Interrupts is to make optimal use of the microcontroller's processing power, and to achieve optimal cooperation between time-critical tasks and less time-critical tasks both executed in software. Three registers are available to handle interrupts. These are:

- Interrupt Event Register
- Interrupt Enable Register
- Interrupt Reset Register.

These registers are to be regarded together. Corresponding bits in these registers relate to one and the same event. Bits in the Interrupt Event Register are set by the PCC and are to be reset by the external processor by writing '1's in the corresponding bits in the Interrupt Reset Register. The mask in the Interrupt Enable Register enables the interrupt if corresponding events do occur.

6.6.3 Watchdog

The PCD5041 is equipped with a watchdog timer, which generates a reset towards an external device (e.g. a microcontroller) after time-out. Two (fixed) time-out periods can be programmed; 1.25 s and 82 s.
The watchdog function can be disabled by using the EN_WATCHDOG input pin.

6.6.4 Power-down

The PCC may switch off the 6.912 MHz internal clock, to enter a power saving mode. All blocks, running on this clock are then switched off (i.e. RF-interface, cipher block, speech interface, PCC). This is called the power-down state, and is only used in the handset mode.

The 13.824 MHz clock is never switched off. The Timing Control, microcontroller interface, and Bus Controller keep running, in order to remain synchronous with a base station, and to keep the wake-up circuitry active. During power-down the external microcontroller has still access to the common data area.

6.7 Survey of registers

For a survey of all addresses occupied refer to Tables 1 and 2. Some of the address locations are used differently for read and write. The addresses 000 to 7DF are occupied by RAM memory, while the upper 32 bytes are assigned to the hardware registers. A part of the RAM memory is allocated for use by the RF block, cipher block, and the speech interface.

Table 1 Hardware register addresses

ADDRESS	WRITE	READ
7E0	–	–
7E1	S-DATA1	–
7E2	S-DATA2	–
7E3	S-DATA3	RMT-STAT
7E4	–	RF-STATUS
7E5	B-field-shift	–
7E6	B-field-loc.	–
7E7	A-field-loc.	–
7E8	window-wide-off	–
7E9	window-wide-on	–
7EA	window-narrow-off	–
7EB	window-narrow-on	–
7EC	T-power-rmp-on	–
7ED	synth-off	–
7EE	RF-control-port	sync-status
7EF	slot-cnt-off	slot-counter-copy
7F0	frame-cnt-ref	RSSI
7F1	sync-ref-preset	bit-counter-copy 1
7F2	bit-counter-preset	bit-counter-copy 2
7F3	frame-counter	frame-counter
7F4	slot-counter	slot-counter
7F5	sync-control	sync-control
7F6	BMC-mode	BMC-mode
7F7	correlator-threshold	measure
7F8	watchdog-1	–
7F9	watchdog-2	–
7FA	–	–
7FB	–	–
7FC	interrupt-event	interrupt-event
7FD	interrupt-enable	interrupt-enable
7FE	interrupt-reset	–
7FF	controller mode	controller mode

Table 2 Fixed RAM locations

ADDRESS	ENTRY
740 to 747	cipher key vector #0
748 to 74F	cipher key vector #1
750 to 757	cipher key vector #2
758 to 75F	cipher key vector #3
760 to 767	cipher key vector #4
768 to 76F	cipher key vector #5
770 to 777	cipher key vector #6
778 to 77F	cipher key vector #7
780 to 787	cipher key vector #8
788 to 78F	cipher key vector #9
790 to 797	cipher key vector #10
798 to 79F	cipher key vector #11
7A0 to 7A7	cipher init vector
7A8 to 7AA	not used
7AB	XZ field buffer
7AC to 7AF	S-field buffer
7B0 to 7BB	cipher-slot-control-table
7BC to 7BF	not used
7C0 to 7DF	speech-slot-control-table

7 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	+6.5	V
V_I	all input voltages	−0.5	V_{DD} + 0.5	V
I_I	DC input current	−10	+10	mA
I_O	DC output current	−10	+10	mA
P_{tot}	total power dissipation	−	+500	mW
P_O	power dissipation per output	−	30	mW
I_{DD}	supply current	−100	+130	mA
I_{SS}	ground current	−100	+130	mA
T_{stg}	storage temperature range	−55	+100	°C
T_j	operating junction temperature	−	90	°C

8 CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
General						
T_{amb}	operating ambient temperature		−25	−	+70	°C
V_{DD}	supply voltage		2.7	−	5.5	V
$V_{DD(ret)}$	RAM retention voltage		1.0	−	V_{DD}	V
I_{DD}	operating supply current	note 1	−	6	12	mA
$I_{DD(stb)}$	standby supply current	note 2	−	1	3	mA
	clock input duty cycle	All inputs LOW except WRN; XTAL1 running at 14 MHz	45	−	55	%
Digital I/O						
V_{IL}	LOW level input voltage		0	−	$0.3V_{DD}$	V
V_{OL}	LOW level output voltage		0	−	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	−	V_{DD}	V
V_{OH}	HIGH level output voltage		$0.7V_{DD}$	−	V_{DD}	V
I_{LI}	input leakage current				1.0	µA
$I_{O(source)}$	output source current	V_{DD} = 3.6 V; 0.4 V ≤ V_O ≤ V_{DD} − 0.4 V	2.0	5.0	−	mA
$I_{O(sink)}$	output sink current	V_{DD} = 3.6 V; 0.4 V ≤ V_O ≤ V_{DD} − 0.4 V	2.0	5.0	−	mA
$I_{RDYN(sink)}$	RDYN output sink current	V_{DD} = 3.6 V; V_O = 0.4 V	2.0	5.0	−	mA
		V_{DD} = 5.0 V; V_O = 0.4 V	−	6.0	−	mA
f_{DCK}	DCK input frequency	n = 1 to 32	−	n × 64	−	kHz
f_{FS1}	FS1 input frequency		−	8	−	kHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Oscillator (inputs XTAL1 and XTAL2)						
g_m	transconductance	V_{DD} = 2.7 V	0.6	–	–	mS
		V_{DD} = 3.6 V	–	1.6	–	mS
R_F	feedback resistance		200	500	–	kΩ
RSSI Peak detector (6-bit linear A-D converter, for RSSI measurement on input RSSI_AN)						
$V_{i(RSSI\_AN)}$	input level		0	–	V_{DD}	V
$V_{conv(RSSI\_AN)}$	voltage conversion range		0	–	V_{REF}	V
$V_{i(VREF)}$	V_{REF} input voltage		1.0	3.0	V_{DD}	V
$Z_{i(VREF)}$	V_{REF} input impedance	during power-down high impedance	–	50	–	kΩ
t_{conv}	conversion time		18.4	–	–	µs
	integral non-linearity		–	–	4	LSB
	differential non-linearity	note 3	–	0.2	1.5	LSB
$Z_{i(RSSI\_AN)}$	input impedance RSSI_AN		–	1	–	MΩ
PCD5041HZ comparator characteristics						
$I_{DD(stb)(comp)}$	supply current (standby)	note 4	–	10	–	µA
$I_{DD(idle)(comp)}$	supply current (idle)	V_{DD} = 3.0 V; note 4	–	135	–	µA
$I_{DD(1MHz)}$	supply current (1 MHz)	V_{DD} = 3.0 V; note 4	–	350	–	µA
$I_{LI(comp)}$	input leakage current	note 5	–	–	1	µA
C_i	input capacitance	note 5	–	10	–	pF
R_{pu}	pullup resistance	note 6	–	200	–	kΩ
V_{cm}	input common mode range	note 7	1.0	–	V_{DD} – 0.5	V
V_{os}	max. input offset voltage	note 8	–	5	–	mV
t_{pd}	propagation delay	note 9	–	100	200	ns
Δt_{pd}	delay difference	note 8 and 9	–	10	–	ns
$V_{OL(comp)}$	output level LOW	I_O = 2 mA	–	–	0.4	V
$V_{OH(comp)}$	output level HIGH	I_O = 2 mA	V_{DD} – 0.4	–	–	V
t_r	output rise time	C_L = 50 pF	–	15	–	ns
t_f	output fall time	C_L = 50 pF	–	15	–	ns
t_{en}	enable time		–	–	8	µs

Notes to the characteristics

1. V_{DD} = 3.0 V; f_{clk} =13.824 MHz; no external load; one speech link active (under typical conditions).
2. V_{DD} = 3.0 V; f_{clk} =13.824 MHz; no external load; after reset.
3. Maximum differential non-linearity at supply voltage 5.5 V and V_{REF} = 1 V.
4. Supply current $I_{DD(stb)(comp)}$ flows when $\overline{COMP\_NE}$ is HIGH.
   Supply current $I_{DD(idle)(comp)}$ flows when the comparator is in active mode ($\overline{COMP\_NE}$ is LOW). It is the DC current of the comparator when it is not switching, and V(COMP_INP) < V(COMP_INM).
   The active mode supply current $I_{DD(1MHz)}$ includes the output pulse rate of 1 MHz.
5. For input pins COMP_INP, COMP_INM, $\overline{COMP\_NE}$.
6. For input pin $\overline{COMP\_NE}$.
7. The minimum input common mode voltage will be measured at DC levels with, COMP_INM at 1 V DC ±30 mV. The same goes for the maximum input common mode voltage at (V_{DD} – 0.5V).
8. These values are not tested in production, and are based upon theoretical estimates and laboratory tests.
9. The propagation delay t_{pd} is measured from the time the differential input voltage equals the offset voltage, to the 50% point of the output transition. The initial differential input voltage is 100 mV and the propagation delay is specified for an input overdrive of 30 mV, and a load capacitance of 50 pF. t_{pd} is valid for both the positive and negative going output transition. The maximum value is valid for the total ranges of temperature, supply voltage and common mode input voltage. The worst case operation conditions are at the minimum supply voltage, the lowest operating temperature and the minimum input common mode voltage. The delay difference Δt_{pd} gives the difference between t_{pd} for the rising output transition and t_{pd} for the falling output transition and is valid for all operating conditions. The test method to check the maximum delay difference is by measuring the RMS voltage of the output signal.

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DECT burst mode controller PCD5042

1 FEATURES

- On-chip pre-programmed Communication Controller with embedded firmware for implementation of Traffic Bearer Control (TBC), MAC message handling, scanning, and control of the device's other functional units.
- Fixed Part (FP) modes
- TDMA frame (de)multiplexing
- Encryption
- Scrambling
- CRC generation and checking
- Beacon transmission control (by P00 packets)
- On-chip comparator for receive data slicer function (only available in the LQFP80 package)
- Switches up to12 active speech channels from speech interface to 1 152 kbits/s. radio interface, and vice versa
- Dual channel speech/data capability
- RSSI measurement, with on-chip 6-bits peak/hold detector
- Local call switching for up to 6 internal calls on RF side/local call switching on speech side.
- Quality control report
- Digital Phase Locked Loop (DPLL)
- Synchronization (handset to active bearer, base station to cluster of RFPs)
- Seamless handover procedure
- Fast (hardware) and slow (software) mute function
- 1 kbyte extended RAM memory
- On-chip crystal oscillator (13.824 MHz)
- Programmable microcontroller clock frequency
- Programmable interrupts
- Watchdog with two programmable time-outs
- Low power consumption in standby mode
- Low supply voltage (2.7 to 5.5 V)
- SACMOS technology.

2 GENERAL DESCRIPTION

The PCD5042 DECT Burst Mode Controller (BMC) is a custom IC that performs the DECT Physical Layer and MAC Layer time-critical functions, for use in DECT base station products which comply with the following standards:

- DECT CI part 2: Physical layer (DE/RES 3001-2)
- DECT CI part 3 : Medium Access Control layer (DE/RES 3001-3)
- DECT CI part 7: Security features for DECT (DE/RES 3001-7)
- DECT CI part 9: Public Access Profile (DE/RES 3001-9).

The PCD5042 has interfaces to:

- Up to 4 ADPCM CODECs in a simple base station (with up to 4 analogue lines) without glue logic
- n x 64 kbits/s highway, where n = 1 to 32, for systems requiring more than 4 connections to the network
- A radio transceiver; the interface is fully decoded, and includes power-down signals
- An external microcontroller.

The PCD5042 is designed to be connected to an ADPCM CODEC (Philips' PCD5032, for example) and an 80C51-type microcontroller. Other microcontrollers (e.g. 68000) and CODECs can also be supported.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD5042H	QFP64	plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT319-2
PCD5042HZ	LQFP80	plastic low profile quad flat package; 80 leads; body 12 × 12 × 1.4 mm	SOT315-1

4 BLOCK DIAGRAM

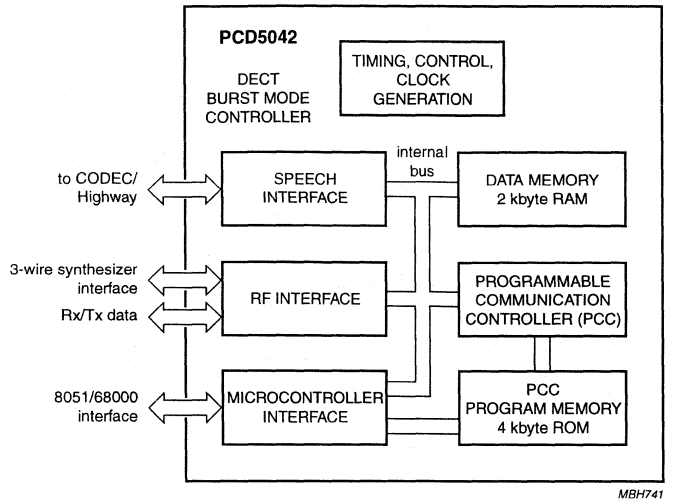

Fig.1 Block diagram.

5 PINNING (see Figs 2 and 3)

SYMBOL	PIN		TYPE(2)	DESCRIPTION
	QFP64	LQFP80(1)		
AD0 to AD7	1 to 8	80, 1, and 3 to 7	I/O	address/Data bus
ALE	9	9	I	address latch enable
$\overline{CS}$	10	11	I	chip select (active LOW)
A8 to A10	13 to 11	14 to 12	I	address bus
V_{DD1}	14	15	P	positive supply 1
PROC_CLK	15	16	O	microcontroller clock; programmable from $f_{CLK}/64$ to f_{CLK}, where f_{CLK} is the crystal oscillator frequency
V_{SS1}	16	17	P	negative supply 1
XTAL1	17	20	I	crystal oscillator input
XTAL2	18	21	O	crystal oscillator output
V_{SS2}	19	22	P	negative supply
RESET_OUT	20	23	O	watchdog timer output; intended to reset the external microcontroller when expired
$\overline{RD}$	21	24	I	read (active LOW)
$\overline{WR}$	22	25	I	write (active LOW)
$\overline{RDY}$	23	26	O	ready signal (active LOW), to initiate wait states in the microcontroller (open drain)

SYMBOL	PIN		TYPE[2]	DESCRIPTION
	QFP64	LQFP80[1]		
$\overline{INT}$	24	27	O	interrupt (active LOW)
CLK100	25	29	O	100 Hz frame timer
V_{SS3}	26	31	P	negative supply 3
DO	27	32	O	3-state data output on the speech interface
FS3	–	33	I/O	8 kHz framing signal to ADPCM CODEC 1 output, for simple base + handset, otherwise 8 kHz framing input
FS1	28	34	I/O	8 kHz framing signal to ADPCM CODEC 1 output, for simple base + handset, otherwise 8 kHz framing input
FS4	–	35	I/O	8 kHz framing signal to ADPCM CODEC 1 output, for simple base + handset, otherwise 8 kHz framing input
FS2	29	36	O	8 kHz framing signal to ADPCM CODEC 2 in the base station mode
DI	30	37	I	data input on the speech interface
DCK	31	38	O	simple base + handset; 1152 kHz data clock (output), otherwise 2048 kHz data clock (input) signal
CLK3	32	39	O	3.456 MHz clock (nominal value, used to adjust system timing)
ANT_SW	33	40	O	selects one of two antennas
$\overline{T\_ENABLE}$	34	41	O	Transmitter Enable (active LOW)
T_POWER_RMP	35	43	O	Transmitter Power Ramp control
RMT_STAT	36	44	I	serial 8-bit data can be read in for each slot; REMote radio
SYNTH_LOCK	37	45	I	lock indication from synthesizer
V_{SS4}	38	46	P	negative supply 4
REF_CLK	39	47	O	reference frequency for the synthesizer, i.e. the crystal oscillator clock f_{CLK}
V_{DD2}	40	48	P	positive supply 2
S_ENABLE	41	49	O	synthesizer enable
S_CLK	42	51	O	clock signal, to be used with S_DATA
S_DATA	43	52	O	serial data to the synthesizer
S_POWER_DWN	44	53	O	synthesizer power-down control
VCO_BND_SW	45	54	O	VCO bandswitch control signal
1200 HZ	46	55	O	control signal for dual synthesizer schemes
T_DATA	47	56	O	serial output data to transmitter
SET_OFF_IN	48	57	I	switches off the crystal oscillator, and prevents all RF signals from becoming active
TEST1	49	58	I	selects various test modes.; normal operation set to 0
RSSI_AN	50	60	I	analog signal (for basic DECT systems), peak signal strength measured after a lowpass filter
TEST2	51	–	I	selects various test modes; normal operation set to 0
TEST3	52	61	I	selects various test modes; normal operation set to 0
R_DATA	53	63	I	receive data

SYMBOL	PIN		TYPE[2]	DESCRIPTION
	QFP64	LQFP80[1]		
$\overline{R\_ENABLE}$	54	64	O	receiver enable (active LOW)
R_POWER_DWN	55	65	O	receiver power-down
$\overline{COMP\_NE}$	–	66	I	digital input comparator not_enable (active LOW)
SLICE_CTR	56	67	O	slice time constant control
COMP_OUT	–	68	O	digital comparator output
V_{DD3}	57	69	P	positive supply 3
V_{SS5}	58	70	P	negative supply 5
COMP_INM	–	71	I	analog comparator input negative
V_{REF}	59	72	I	reference input for the A/D converter
COMP_INP	–	73	I	analog input positive
$V_{DD(RAM)}$	60	74	P	power supply for data RAM
SYNCPORT	61	76	I/O	in the base station the signal is the SYNCPORT
RESET	62	77	I	BMC master reset signal
MEM_SEL	63	78	I	selects PCC program memory at microcontroller interface
EN_WATCHDOG	64	79	I	enable watchdog input; when HIGH, the watchdog timer of the BMC is enabled

Notes

1. Un-referenced pins for the LQFP80 package are not connected. FS3, FS4 and the comparator signals are only available in the LQFP80 package.
2. **All** signals which are input or I/O, and which can be floating, need to be pulled up to V_{DD} or down to V_{SS} in order to protect the device against cross-currents. Exceptions are VREF and RSSI_AN, which do not have to be protected.

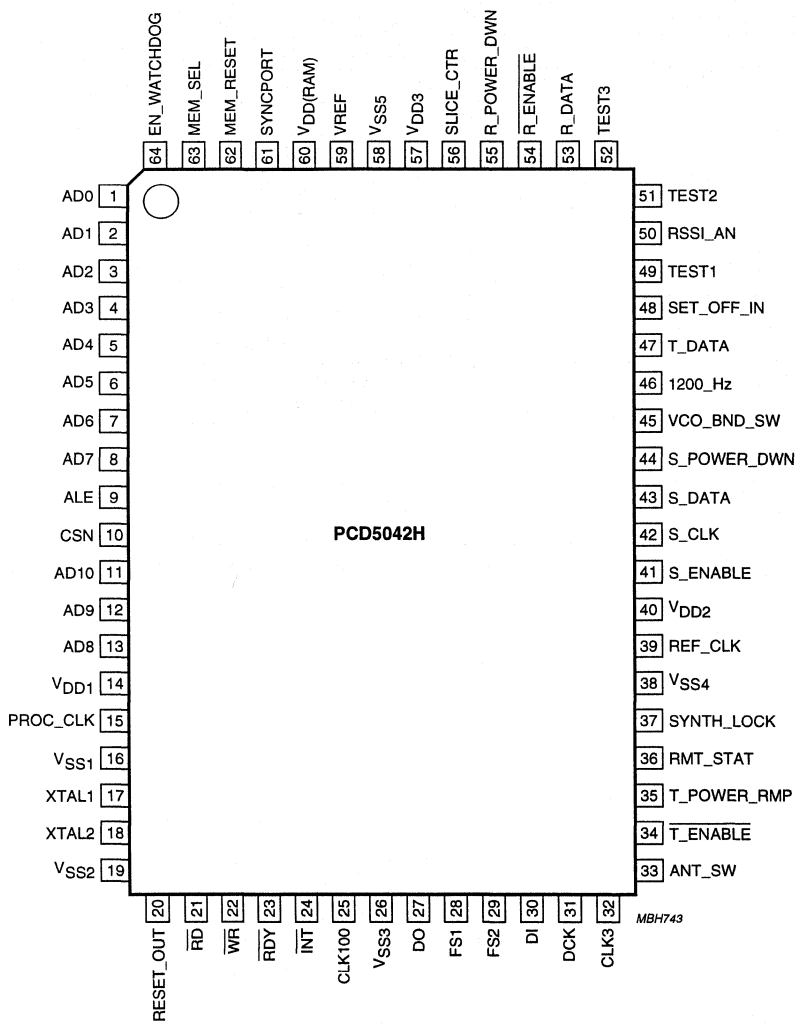

Fig.2 Pin configuration, PCD5042H (QFP64 package).

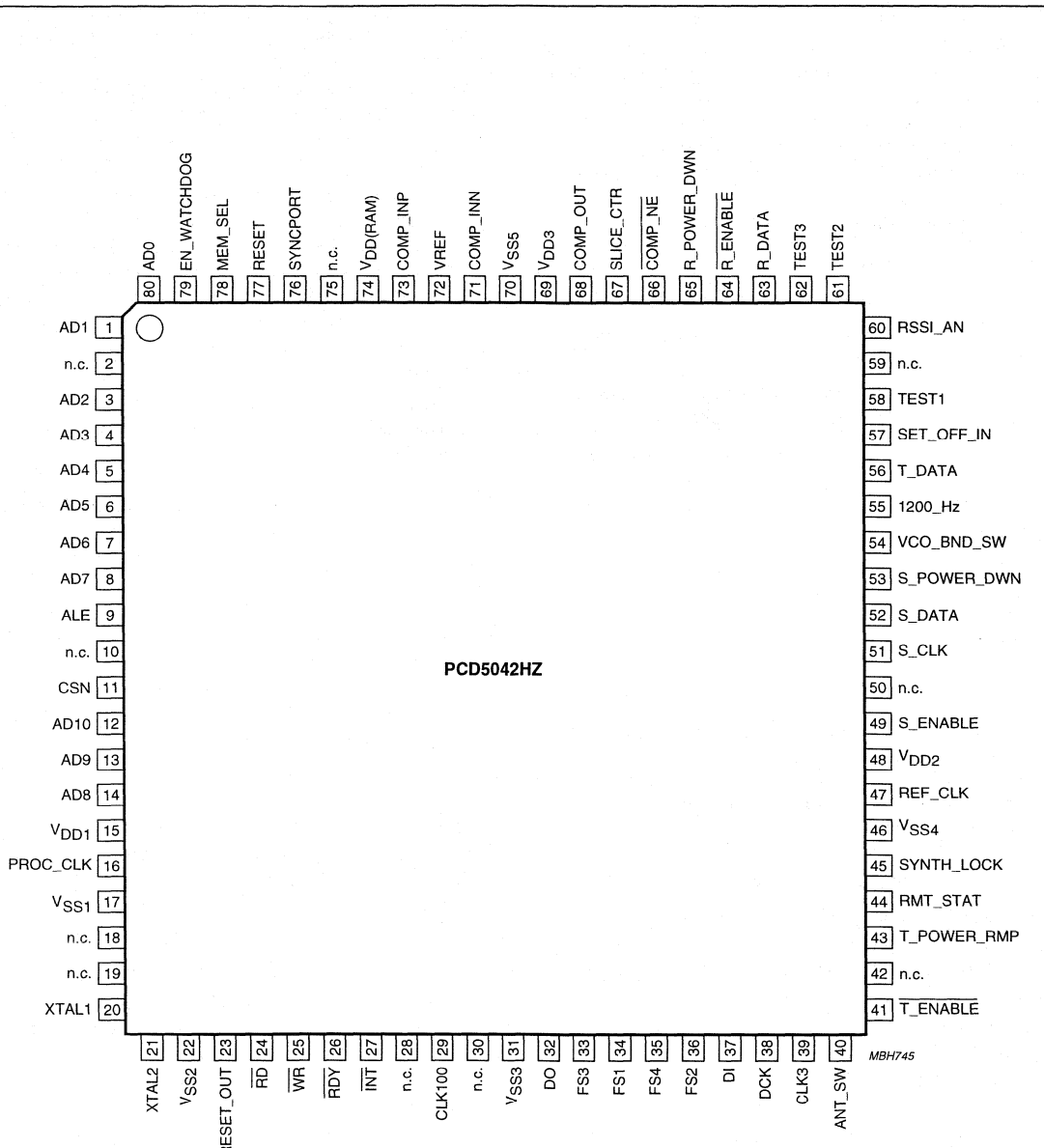

Fig.3 Pin configuration, PCD5042HZ (LQFP80 package).

6 FUNCTIONAL DESCRIPTION (see Fig.1)

The PCD5042 has dedicated hardware blocks containing logic for time-critical functions requiring bit or byte-time accuracy. Other functions requiring only slot-time accuracy are performed by software in the Preprogrammed Communication Controller (PCC). This approach offers maximum flexibility during prototyping.

6.1 Internal bus and data memory

6.1.1 INTERNAL BUS

The function of the internal bus is:

- To provide access for all functional blocks to the common data memory
- To provide access for the microcontroller-interface and the PCC to all other functional blocks.

All functional blocks (speech-interface, RF-interface, microcontroller-interface and PCC) can autonomously use the internal bus to communicate with the common data memory.

A bus controller is used to handle the bus priority mechanism. When several blocks request access simultaneously, the request with the highest priority is handled first.

6.1.2 DATA MEMORY

A large part of the data memory is used for the bit rate adaptation between the DECT radio interface and the speech interface. The data memory also acts as the main communication interface between the external microprocessor and the PCC.

6.2 Clock generation and correction (see Fig.4)

The device has an on-chip 13.824 MHz crystal oscillator. From this source, a few frequencies are derived for internal and external use. Frequencies generated for external use are:

- 13.824 MHz for the synthesizer reference (pin REF_CLK). This output is only provided if the synthesizer power-down control (output on pin S_POWER_DWN) is not selected.
- 0.144 to 13.824 MHz for the microcontroller clock (pin PROC_CLK)
- 3.456 MHz for the ADPCM CODEC (pin CLK3)
- 1200 Hz (pin 1200_HZ) for dual synthesizer switching
- 100 Hz (pin CLK100) indicates start of frame.

Nominally, the frequency on pin CLK3 is 3.456 MHz. This frequency is obtained by dividing the crystal frequency by 4. Sometimes, the crystal frequency will be divided by 3 or by 5, to synchronize the combination of the ADPCM CODEC and the device to an external source. External synchronization for base station applications is achieved as follows:

- **Master base station**. The master base station provides a 100 Hz signal to slave base stations on pin SYNCPORT. If the PCD5042 is connected to a digital interface (32-slot mode speech interface), the external synchronization will be done on the incoming 8 kHz signal. If it is connected to an analog line (12-slot mode speech interface), it will use its own crystal oscillator as reference.
- **Slave base station**. The slave base station will use the incoming SYNCPORT signal as synchronization reference.

6.3 Programmable communication controller and program memory

6.3.1 PCC

The PCC is a RISC-type controller and is used to control functions which are slot-time accurate. It is well suited for bit manipulation, and runs at a clock frequency of 6.912 MHz (equivalent to 3.4 Mips). After finishing a task, it switches to a power saving state, from which it returns after a pre-programmed time.

6.3.2 PCC FUNCTIONS

The most important functions of the PCC are to:

- Perform the appropriate actions on received messages: PMID and FMID checking, RFPI checking, TBC handling
- Prepare A-field messages for transmission
- Prepare the RF-interface for the coming slot
- Perform the procedures for RSSI and set-up scan, maintain scan counters and timers, assemble the RSSI field in the common data memory
- Filter events and indicate them to the microcontroller by interrupt.

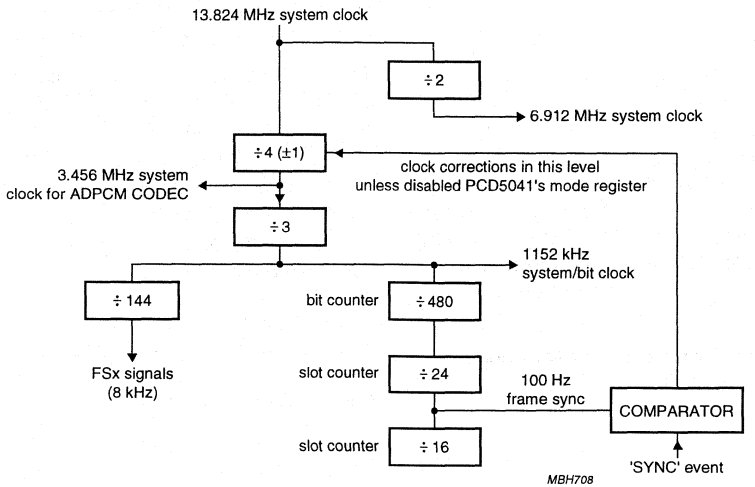

Fig.4 Internal clocking scheme of the PCD5042.

6.4 Speech interface

The speech interface block performs the following functions:

- Connection to a 1152 kbits/s interface in a handset and a simple base station in the so called '12 slot mode'
- Connection to a n x 64 kbits/s interface in base stations in the so called '32 slot mode'
- Autonomous storing/fetching of ADPCM speech data in/from the PCD5042's common data memory, using internal addressing logic
- Muting of speech data
- Local call.

6.4.1 12-SLOT MODE

The 12-slot mode is selected if up to 4 ADPCM CODECs are connected to the PCD5042, where the PCD5042 is the master of these CODECs. In a handset, or in a simple base stations which is connected with up to 4 analog lines to the public network, the PCD5042 is master of the CODECs. Each CODEC is connected with a separate framing reference signal (FS1 to FS4) to the PCD5042. In the QFP64 package, 2 framing signals FS1 and FS2 are available, whereas in the LQFP80 package 4 framing signals can be used (FS1 to FS4). When more CODECs are to be connected, the FS5 to FS12 signals have to be generated externally. When using the framing signals FS1 to FS4, no interface logic is required when using the PCD5032 ADPCM CODEC.

A speech-slot control table is used to determine where to store/fetch speech data for transmission and reception. The hardware speech-interface is capable of addressing the right speech buffer for the relevant speech slot, and will maintain a counter carrying the offset to the correct stored/fetched address.

6.4.2 32-SLOT MODE

The 32-slot mode is used to connect the PCD5042 to a digital interface with a data rate of n × 64 kbits/s; where n = 1 to 32 is the number of speech slots. This equates to data rates from 64 kbits/s to 2048 kbits/s.
Up to 12 of the 32 speech slots can be used simultaneously. The same kind of speech-slot control table used in the 12-slot mode is used for the 32-slot mode.

6.4.3 MUTING

Due to various reasons the quality of the incoming speech data may be degraded significantly. By muting the speech

data, these disturbances are not audible (or are less audible) to the user. The PCD5042 performs two types of muting:

- Fast muting
- Slow muting.

Fast muting, which is performed by the PCD5042 automatically, is nothing more than a repetition of the previously received frame (80 speech samples) to the ADPCM CODEC. It is issued if no Sync word was detected. Slow muting is issued by the microcontroller, after having detected a degradation of quality. A slow mute is implemented as a continuous '0000' nibble transmission to the ADPCM CODEC, until slow mute is released.

6.4.4 LOCAL CALL

A local call option is implemented, in order to loopback data from one CODEC to another CODEC, and vice versa, see Fig.5.

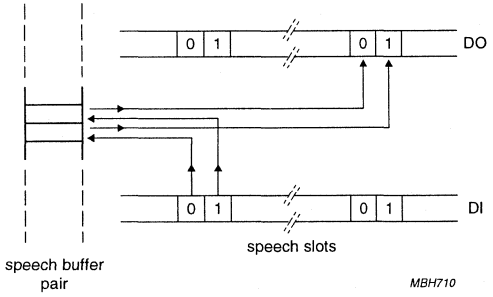

Fig.5 Local call switching on speech interface.

6.5 RF interface

Most of the functions performed by the RF interface are under control of the PCC. Specifically, the processing of non-speech data and the programming of functions and registers is done via the PCC.

6.5.1 SERIAL RECEIVER

The serial receiver processes the data, which comes from the RF section, and which is already filtered by the synchronization part. The data is latched, using the recovered data clock.

The serial receiver will collect the complete A-field and B-field and store it in the common data memory. Before the A-field is received, the A-field start address is programmed by the PCC. Upon reception of A-field nibbles, the address is updated by the serial receiver. Meanwhile, the PCC will program the B-field start address.

In Fig.6 the data flow in the serial receiver is shown. Note that almost no decoding of messages is required. Only the header of the A-field needs to be decoded to check if a ciphered message is being received or transmitted, which requires the ciphering to be switched on in the A-field also.

6.5.2 SERIAL TRANSMITTER

The serial transmitter performs the reverse of the receiver functions. Several blocks used in the receiver are also used in the transmitter. Amongst these are the CRC-generators, the scrambler, and the address registers. Figure 7 shows the serial transmitter structure.

By transmitting the X-CRC twice, the Z-field is transmitted. The handling of the address registers is the same for the transmitter. Transmission of the synchronization sequence (S-field) is done using the same method as the A-field and B-field. The S-field is stored in the common data memory and will be fetched by the transmitter, just before transmission.

Two additional functions are not shown in Fig.7:

- In the handset the data in the serial transmitter may be advanced by a programmable number of bit periods. This is done to compensate for the delay in the RF section
- The transmitted data can be inverted (using a switch in the PCD5042 mode register), in order to connect the PCD5042 to VCOs requiring negative modulation.

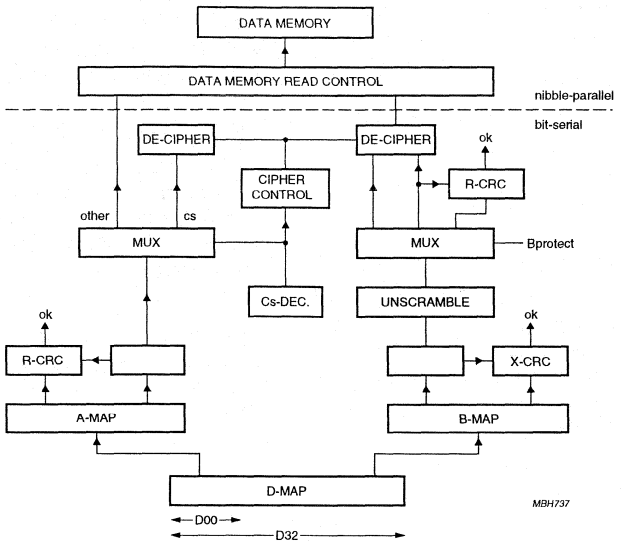

Fig.6 Serial receiver structure.

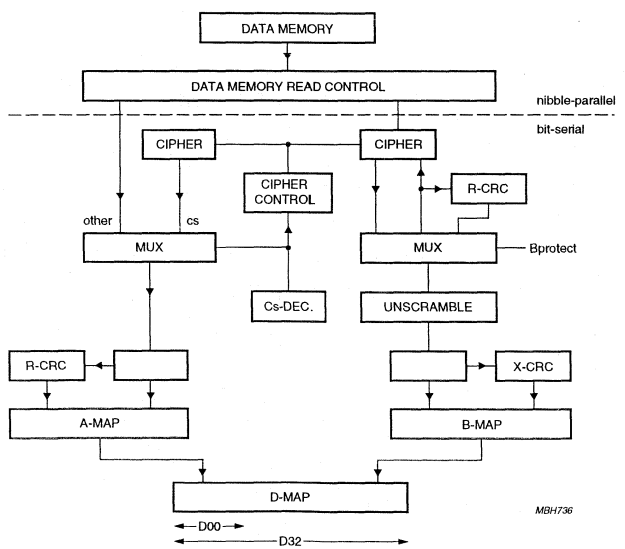

Fig.7 Serial transmitter structure.

6.5.3 SEAMLESS HANDOVER

Seamless handover guarantees that when speech information is switched from one slot to another, no speech samples are lost, added or displaced. Seamless handover is achieved in the RF interface by:

- Using a look-up table containing the correct start addresses of the B-fields in the data memory
- The RF receive and transmit blocks move data to/from the data memory block in 4-bit nibbles.

6.5.4 RF CONTROL SIGNALS

The timing of the control signals to the RF section is fixed, but such that an RF delay between 1.5 and 7 µs can be tolerated. Only the transmitter ramp signal and the synthesizer enable are programmable within certain limits.

6.5.5 SYNTHESIZER PROGRAMMING

To program a synthesizer, a 3-wire serial interface is used. The signals on this interface are:

- S_ENABLE (enable)
- S_CLK (clock)
- S_DATA (data).

To program various types of synthesizers, a 3-byte shift register is present. Three data formats are supported: 8, 16 or 24 bit words can be selected. The transfer of data from a frequency table in the common data memory to the shift register is under control of the PCC.

6.5.6 RSSI MEASUREMENT (see Fig.8)

The RSSI measurement in the PCD5042 RF-interface block is done in 3 parts: a peak/hold detector, a 6-bit A/D converter, and an RSSI control unit, which controls the peak/hold detector and the A/D converter. Once per slot time, a sample is fetched by the PCC and saved in the appropriate area of the common data memory.

If the radio receiver is active in a particular time slot, the RSSI value will automatically be measured in that slot. Adjustment to the RSSI_AN input level can be made with VREF.

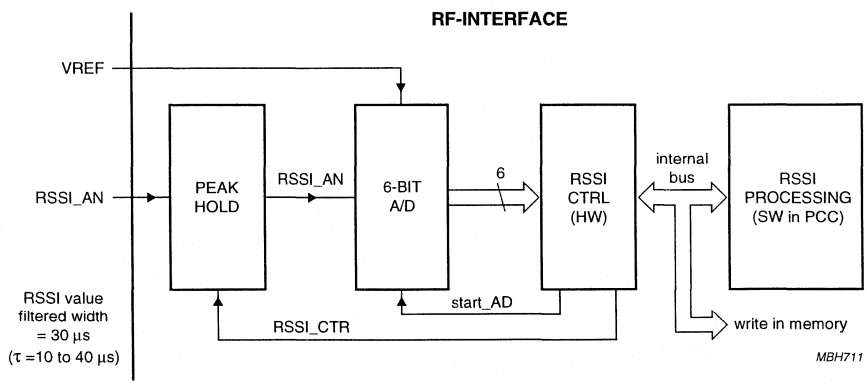

Fig.8 RSSI measurement path.

6.5.7 LOCAL CALL SWITCHING (see Fig.9)

The PCD5042 provides a local call switching function in the base station. It will store incoming speech nibbles in the common data memory, in the area reserved for that particular receive slot. Then, during the transmit phase, it passes the start pointer of the same data memory area to the transmit block. Thus, the speech data is echoed to the other user. To handle quality degradation for local calls, a mute can be performed at the RF side of the speech buffer.

6.5.8 DATA SYNCHRONIZATION (see Fig.10)

The data synchronization is done in 2 phases:

- Bit synchronization
- Sync word detection.

Bit synchronization is done using a Digital PLL (DPLL), with an oversampling factor of 12, i.e. the DPLL is running at 12 times the data rate. The output from the DPLL is a receive clock signal (RxC), which acts as the enable for a 20-bit shift register.

Sync word detection is achieved by checking the incoming data pattern with the expected synchronization field pattern, using a correlator.
The correlator has a programmable threshold, so it can accept bit errors in the sync field pattern up to the threshold level. Furthermore, the correlator window is programmable. This means that 'SlotSync', which indicates the slot synchronization event, can be detected only during a certain period (the time window).

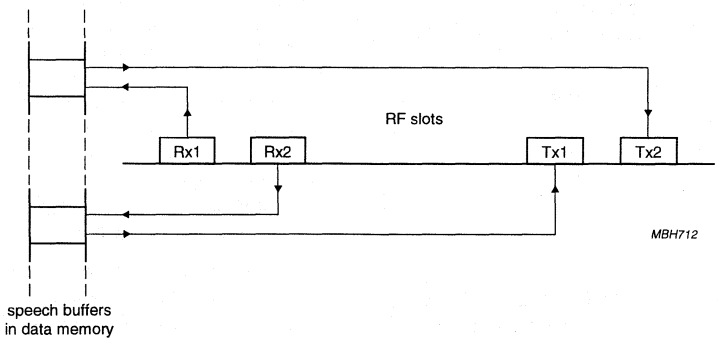

Fig.9 Local call switching on the RF-side.

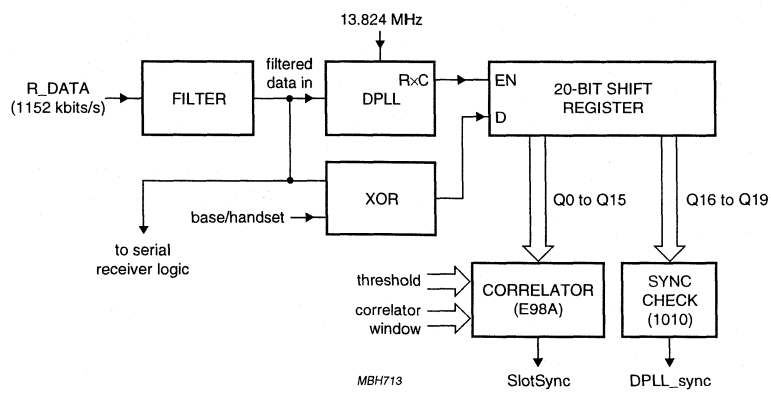

Fig.10 Schematic of the receiver synchronization part.

The 'DPLL_sync' indication should only be used, when 'SlotSync' is active. It indicates that the last 4 bits of the pre-amble field (the training sequence) are received correctly, and thus indicates that the DPLL was in lock (synchronized) in time. If the 'SlotSync' is active, and the 'DPLL_sync' is not, then a sliding interferer might have been detected.

If 'SlotSync' is not detected, effectively no data is received in that slot. This implies a 'fast mute' because speech data received in the previous frame is not destroyed.

6.5.9 CIPHERING MACHINE

The description of the cipher machine is subject to confidentiality. The specification of its algorithms are delivered by ETSI under the terms of a Non-Disclosure Agreement.

The cipher machine is under control of the TBC, which is implemented in the PCC. The cipher machine generates 2 fields of ciphering bits:

- A_cipher (40 bits) for A-field messages (ciphers tail only)
- B_cipher (320 bits) for speech in B-field.

The transmitted ciphered bits are then:

- A_ciphered: = A XOR A_cipher
- B_ciphered: = B XOR B_cipher.

On reception by the peer end point, deciphering consists of the same operation thanks to the synchronous generation of A_cipher and B_cipher.

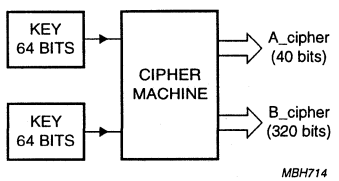

Fig.11 Cipher machine and its sources.

The cipher machine is time-multiplexed on a slot basis. Initially, the Initialisation Vector (IV) and the key must be loaded into the cipher machine. Transfer of the IV and key from the common data area to the cipher machine is done automatically by the cipher machine. The contents of the memory space where IV and key are found, are the responsibility of the PCC, and the external microprocessor.

6.5.10 COMPARATOR/DATA SLICER ON PCD5042HZ

The PCD5042HZ contains a comparator/data slicer. The comparator is a stand-alone circuit. No connections other than power supply are made internally.
The comparator can be used as a data slicer for the receiver input. The delay requirements listed in Chapter 8 were derived from this application. Another use of the comparator is in a successive approximation A/D converter to indicate battery low-voltage condition, or in a power-on-reset circuit.

When the signal $\overline{\text{COMP\_NE}}$ is LOW the comparator is enabled. When $\overline{\text{COMP\_NE}}$ is HIGH the comparator is disabled, and the circuit consumes no power. If the comparator is used as a data slicer for the receiver input, the R_DATA is connected to COMP_OUT, the $\overline{\text{COMP\_NE}}$ is connected to $\overline{\text{R\_ENABLE}}$, both connection are done externally. The pin COMP_INP is connected to the RF mixer. A proper bias voltage (from the slicer time constant control circuit) is connected to COMP_INM. Another use of the comparator is in a successive approximation A/D converter for battery voltage detection.

The pins are protected against ESD damaging, with a protection diode to the positive and negative supply rail. The input pin $\overline{\text{COMP\_NE}}$ has a pull-up resistor which keeps the comparator in power-down mode by default.

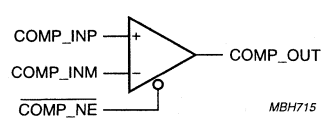

Fig.12 Circuit schematic of the comparator/data slicer.

6.6 Microcontroller Interface

6.6.1 Function of the microcontroller interface

The microcontroller Interface will provide the following services.

- Direct interface to processors which have an INTEL-8051 compatible interface
- General interface to processors that can handle 'wait states' e.g. 68000-family; in this case glue logic is required
- Processor clock signal of which the frequency is programmable in order to adjust instantaneously processor performance to processor work load
- A programmable interrupt register
- A watchdog timer with time-out periods of 1.25 or 82 seconds, depending on the programming.

The microcontroller can address the PCD5042 as any other RAM memory connected to the microcontroller bus. By writing the 'Interface-Mode Register', the microcontroller can select the interface mode and its own clock frequency.

6.6.2 Microcontroller interrupts

The function of microcontroller Interrupts is to make optimal use of the microcontroller's processing power, and to achieve optimal cooperation between time-critical tasks and less time-critical tasks both executed in software. Three registers are available to handle interrupts. These are:

- Interrupt Event Register
- Interrupt Enable Register
- Interrupt Reset Register.

These registers are to be regarded together. Corresponding bits in these registers relate to one and the same event. Bits in the Interrupt Event Register are set by the PCC and are to be reset by the external processor by writing '1's in the corresponding bits in the Interrupt Reset Register. The mask in the Interrupt Enable Register enables the interrupt if corresponding events do occur.

6.6.3 Watchdog

The PCD5042 is equipped with a watchdog timer, which generates a reset towards an external device (e.g. a µC) after time-out. Two (fixed) time-out periods can be programmed; 1.25 s and 82 s. The watchdog function can be disabled by using the EN_WATCHDOG input pin.

6.6.4 Power-down

The PCC may switch off the 6.912 MHz internal clock, to enter a power saving mode. All blocks, running on this clock are then switched off (i.e. RF-interface, cipher block, speech interface, PCC). This is called the power-down state, and is only used in the handset mode.

The 13.824 MHz clock is never switched off. The Timing Control, microcontroller interface, and Bus Controller keep running, in order to remain synchronous with a base station, and to keep the wake-up circuitry active. During power-down the external microcontroller has still access to the common data area.

6.7 Survey of registers

For a survey of all addresses occupied refer to Tables 1 and 2. Some of the address locations are used differently for read and write. The addresses 000 to 7DF are occupied by RAM memory, while the upper 32 bytes are assigned to the hardware registers. A part of the RAM memory is allocated for use by the RF block, cipher block, and the speech interface.

Table 1 Hardware register addresses

ADDRESS	WRITE	READ
7E0	–	–
7E1	S-DATA1	–
7E2	S-DATA2	–
7E3	S-DATA3	RMT-STAT
7E4	–	RF-STATUS
7E5	B-field-shift	–
7E6	B-field-loc.	–
7E7	A-field-loc.	–
7E8	window-wide-off	–
7E9	window-wide-on	–
7EA	window-narrow-off	–
7EB	window-narrow-on	–
7EC	T-power-rmp-on	–
7ED	synth-off	–
7EE	RF-control-port	sync-status
7EF	slot-cnt-off	slot-counter-copy
7F0	frame-cnt-ref	RSSI
7F1	sync-ref-preset	bit-counter-copy1
7F2	bit-counter-preset	bit-counter-copy2
7F3	frame-counter	frame-counter
7F4	slot-counter	slot-counter
7F5	sync-control	sync-control
7F6	BMC-mode	BMC-mode
7F7	correlator-threshold	measure
7F8	watchdog-1	–
7F9	watchdog-2	–
7FA	–	–
7FB	–	–
7FC	interrupt-event	interrupt-event
7FD	interrupt-enable	interrupt-enable
7FE	interrupt-reset	–
7FF	controller mode	controller mode

Table 2 Fixed RAM locations

ADDRESS	ENTRY
740 to 747	cipher key vector #0
748 to 74F	cipher key vector #1
750 to 757	cipher key vector #2
758 to 75F	cipher key vector #3
760 to 767	cipher key vector #4
768 to 76F	cipher key vector #5
770 to 777	cipher key vector #6
778 to 77F	cipher key vector #7
780 to 787	cipher key vector #8
788 to 78F	cipher key vector #9
790 to 797	cipher key vector #10
798 to 79F	cipher key vector #11
7A0 to 7A7	cipher init vector
7A8 to 7AA	not used
7AB	XZ field buffer
7AC to 7AF	S-field buffer
7B0 to 7BB	cipher-slot-control-table
7BC to 7BF	not used
7C0 to 7DF	speech-slot-control-table

7 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	+6.5	V
V_i	all input voltages	−0.5	V_{DD} + 0.5	V
I_I	DC input current	−10	+10	mA
I_O	DC output current	−10	+10	mA
P_{tot}	total power dissipation	−	+500	mW
P_O	power dissipation per output	−	30	mW
I_{DD}	supply current	−100	+130	mA
I_{SS}	ground current	−100	+130	mA
T_{stg}	storage temperature range	−55	+100	°C
T_j	operating junction temperature	−	90	°C

8 CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
General						
T_{amb}	operating ambient temperature		−25	−	+70	°C
V_{DD}	supply voltage		2.7	−	5.5	V
$V_{DD(ret)}$	RAM retention voltage		1.0	−	V_{DD}	V
I_{DD}	operating supply current	note 1	−	6	12	mA
$I_{DD(stb)}$	standby supply current	note 2	−	1	3	mA
	clock input duty cycle	All inputs LOW except WRN; XTAL1 running at 14 MHz	45	−	55	%
Digital I/O						
V_{IL}	LOW level input voltage		0	−	$0.3V_{DD}$	V
V_{OL}	LOW level output voltage		0	−	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	−	V_{DD}	V
V_{OH}	HIGH level output voltage		$0.7V_{DD}$	−	V_{DD}	V
I_{LI}	input leakage current				1.0	µA
$I_{O(source)}$	output source current	V_{DD} = 3.6 V; 0.4 V ≤ V_O ≤ V_{DD} − 0.4 V	2.0	5.0	−	mA
$I_{O(sink)}$	output sink current	V_{DD} = 3.6 V; 0.4 V ≤ V_O ≤ V_{DD} − 0.4 V	2.0	5.0	−	mA
$I_{RDYN(sink)}$	RDYN output sink current	V_{DD} = 3.6 V; V_O = 0.4 V	2.0	5.0	−	mA
		V_{DD} = 5.0 V; V_O = 0.4 V	−	6.0	−	mA
f_{DCK}	DCK input frequency	n = 1 to 32	−	n × 64	−	kHz
f_{FS1}	FS1 input frequency		−	8	−	kHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Oscillator (inputs XTAL1 and XTAL2)						
g_m	transconductance	V_{DD} = 2.7 V	0.6	–	–	mS
		V_{DD} = 3.6 V	–	1.6	–	mS
R_F	feedback resistance		200	500		kΩ
RSSI Peak detector (6-bit linear A-D converter, for RSSI measurement on input RSSI_AN)						
$V_{i(RSSI\_AN)}$	input level		0	–	V_{DD}	V
$V_{conv(RSSI\_AN)}$	voltage conversion range		0	–	V_{REF}	V
$V_{i(VREF)}$	V_{REF} input voltage		1.0	3.0	V_{DD}	V
$Z_{i(VREF)}$	V_{REF} input impedance	during power-down high impedance	–	50	–	kΩ
t_{conv}	conversion time		18.4	–	–	µs
	integral non-linearity		–	–	4	LSB
	differential non-linearity	note 3	–	0.2	1.5	LSB
$Z_{i(RSSI\_AN)}$	input impedance RSSI_AN		–	1	–	MΩ
PCD5042HZ comparator characteristics						
$I_{DD(stb)(comp)}$	supply current (standby)	note 4	–	10	–	µA
$I_{DD(idle)(comp)}$	supply current (idle)	V_{DD} = 3.0 V; note 4	–	135	–	µA
$I_{DD(1MHz)}$	supply current (1 MHz)	V_{DD} = 3.0 V; note 4	–	350	–	µA
$I_{LI(comp)}$	input leakage current	note 5	–	–	1	µA
C_i	input capacitance	note 5	–	10	–	pF
R_{pu}	pullup resistance	note 6	–	200	–	kΩ
V_{cm}	input common mode range	note 7	1.0	–	V_{DD} – 0.5	V
V_{os}	max. input offset voltage	note 8	–	5	–	mV
t_{pd}	propagation delay	note 9	–	100	200	ns
Δt_{pd}	delay difference	note 8 and 9	–	10	–	ns
$V_{OL(comp)}$	output level LOW	I_O = 2 mA	–	–	0.4	V
$V_{OH(comp)}$	output level HIGH	I_O = 2 mA	V_{DD} – 0.4	–	–	V
t_r	output rise time	C_L = 50 pF	–	15	–	ns
t_f	output fall time	C_L = 50 pF	–	15	–	ns
t_{en}	enable time		–	–	8	µs

Notes to the characteristics

1. V_{DD} = 3.0 V; f_{clk} =13.824 MHz; no external load; one speech link active (under typical conditions).
2. V_{DD} = 3.0 V; f_{clk} =13.824 MHz; no external load; after reset.
3. Maximum differential non-linearity at supply voltage 5.5 V and V_{REF} = 1 V.
4. Supply current $I_{DD(stb)(comp)}$ flows when $\overline{\text{COMP\_NE}}$ is HIGH.
   Supply current $I_{DD(idle)(comp)}$ flows when the comparator is in active mode ($\overline{\text{COMP\_NE}}$ is LOW). It is the DC current of the comparator when it is not switching, and V(COMP_INP) < V(COMP_INM).
   The active mode supply current $I_{DD(1MHz)}$ includes the output pulse rate of 1 MHz.
5. For input pins COMP_INP, COMP_INM, $\overline{\text{COMP\_NE}}$.
6. For input pin $\overline{\text{COMP\_NE}}$.
7. The minimum input common mode voltage will be measured at DC levels with, COMP_INM at 1 V DC ±30 mV. The same goes for the maximum input common mode voltage at (V_{DD} – 0.5V).
8. These values are not tested in production, and are based upon theoretical estimates and laboratory tests.
9. The propagation delay t_{pd} is measured from the time the differential input voltage equals the offset voltage, to the 50% point of the output transition. The initial differential input voltage is 100 mV and the propagation delay is specified for an input overdrive of 30 mV, and a load capacitance of 50 pF. t_{pd} is valid for both the positive and negative going output transition. The maximum value is valid for the total ranges of temperature, supply voltage and common mode input voltage. The worst case operation conditions are at the minimum supply voltage, the lowest operating temperature and the minimum input common mode voltage. The delay difference Δt_{pd} gives the difference between t_{pd} for the rising output transition and t_{pd} for the falling output transition and is valid for all operating conditions. The test method to check the maximum delay difference is by measuring the RMS voltage of the output signal.

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DECT burst mode controller PCD5043

1 FEATURES

- On-chip pre-programmed Communication Controller with embedded firmware for implementation of Traffic Bearer Control (TBC), MAC message handling, scanning, and control of the device's other functional units.
- Fixed Part (FP) modes
- TDMA frame (de)multiplexing
- Encryption
- Scrambling
- CRC generation and checking
- Beacon transmission control (by P00 packets)
- Switches up to12 active speech channels from speech interface to 1152 kbits/s. radio interface, and vice versa
- Dual channel speech/data capability
- RSSI measurement, with on-chip 6-bits peak/hold detector
- Local call switching for up to 6 internal calls on RF side/local call switching on speech side
- Quality control report
- Digital Phase Locked Loop (DPLL)
- Synchronization (handset to active bearer, base station to cluster of RFPs)
- Seamless handover procedure
- Fast (hardware) and slow (software) mute function
- 1 kbyte extended RAM memory
- On-chip crystal oscillator (13.824 MHz)
- Programmable microcontroller clock frequency
- Programmable interrupts
- Watchdog with two programmable time-outs
- Low power consumption in standby mode
- Low supply voltage (2.7 to 5.5 V)
- SACMOS technology.

2 GENERAL DESCRIPTION

The PCD5043 DECT Burst Mode Controller (BMC) is a custom IC that performs the DECT Physical Layer and MAC Layer time-critical functions, for use in DECT remote radio transceiver (PABX) products which comply with the following standards:

- DECT CI part 2: Physical layer (DE/RES 3001-2)
- DECT CI part 3 : Medium Access Control layer (DE/RES 3001-3)
- DECT CI part 7: Security features for DECT (DE/RES 3001-7)
- DECT CI part 9: Public Access Profile (DE/RES 3001-9).

The PCD5043 has interfaces to:

- Up to 4 ADPCM CODECs in a simple base station (with up to 4 analogue lines) without glue logic
- n x 64 kbits/s highway, where n = 1 to 32, for systems requiring more than 4 connections to the network
- A radio transceiver; the interface is fully decoded, and includes power-down signals
- An external microcontroller.

The PCD5043 is designed to be connected to an ADPCM CODEC (Philips' PCD5032, for example) and an 80C51-type microcontroller. Other microcontrollers (e.g. 68000) and CODECs can also be supported.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD5043H	QFP64	plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT319-2

4 BLOCK DIAGRAM

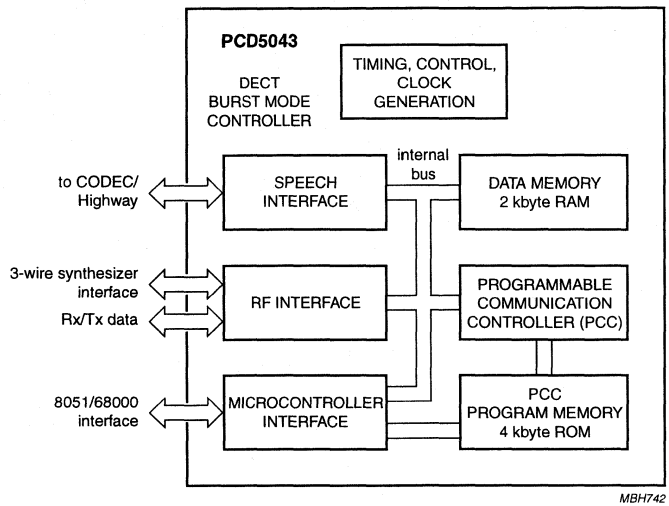

Fig.1 Block diagram.

5 PINNING (see Fig.2)

SYMBOL	PIN	TYPE(1)	DESCRIPTION
AD0 to AD7	1 to 8	I/O	address/Data bus
ALE	9	I	address latch enable
$\overline{CS}$	10	I	chip select (active LOW)
A8 to A10	13 to 11	I	address bus
V_{DD1}	14	P	positive supply 1
PROC_CLK	15	O	microcontroller clock; programmable from $f_{CLK}/64$ to f_{CLK}, where f_{CLK} is the crystal oscillator frequency
V_{SS1}	16	P	negative supply 1
XTAL1	17	I	crystal oscillator input
XTAL2	18	O	crystal oscillator output
V_{SS2}	19	P	negative supply
RESET_OUT	20	O	watchdog timer output; intended to reset the external microcontroller when expired
$\overline{RD}$	21	I	read (active LOW)
$\overline{WR}$	22	I	write (active LOW)
$\overline{RDY}$	23	O	ready signal (active LOW), to initiate wait states in the microcontroller (open drain)
$\overline{INT}$	24	O	interrupt (active LOW)
CLK100	25	O	100 Hz frame timer

SYMBOL	PIN	TYPE[1]	DESCRIPTION
V_{SS3}	26	P	negative supply 3
DO	27	O	3-state data output on the speech interface
FS1	28	I/O	8 kHz framing signal to ADPCM CODEC 1 output, for simple base + handset, otherwise 8 kHz framing input
FS2	29	O	8 kHz framing signal to ADPCM CODEC 2 in the base station mode
DI	30	I	data input on the speech interface
DCK	31	O	simple base + handset; 1152 kHz data clock (output), otherwise 2048 kHz data clock (input) signal
CLK3	32	O	3.456 MHz clock (nominal value, used to adjust system timing)
ANT_SW	33	O	selects one of two antennas
$\overline{\text{T\_ENABLE}}$	34	O	Transmitter Enable (active LOW)
T_POWER_RMP	35	O	Transmitter Power Ramp control
RMT_STAT	36	I	serial 8-bit data can be read in for each slot; REMote radio
SYNTH_LOCK	37	I	lock indication from synthesizer
V_{SS4}	38	P	negative supply 4
REF_CLK	39	O	reference frequency for the synthesizer, i.e. the crystal oscillator clock f_{CLK}
V_{DD2}	40	P	positive supply 2
S_ENABLE	41	O	synthesizer enable
S_CLK	42	O	clock signal, to be used with S_DATA
S_DATA	43	O	serial data to the synthesizer
S_POWER_DWN	44	O	synthesizer power-down control
VCO_BND_SW	45	O	VCO bandswitch control signal
1200 HZ	46	O	control signal for dual synthesizer schemes
T_DATA	47	O	serial output data to transmitter
SET_OFF_IN	48	I	switches off the crystal oscillator, and prevents all RF signals from becoming active
TEST1	49	I	selects various test modes.; normal operation set to 0
RSSI_AN	50	I	analog signal (for basic DECT systems), peak signal strength measured after a lowpass filter
TEST2	51	I	selects various test modes; normal operation set to 0
TEST3	52	I	selects various test modes; normal operation set to 0
R_DATA	53	I	receive data
$\overline{\text{R\_ENABLE}}$	54	O	receiver enable (active LOW)
R_POWER_DWN	55	O	receiver power-down
SLICE_CTR	56	O	slice time constant control
V_{DD3}	57	P	positive supply 3
V_{SS5}	58	P	negative supply 5
V_{REF}	59	I	reference input for the A/D converter
$V_{DD(RAM)}$	60	P	power supply for data RAM
SYNCPORT	61	I/O	in the base station the signal is the SYNCPORT

SYMBOL	PIN	TYPE[1]	DESCRIPTION
RESET	62	I	BMC master reset signal
MEM_SEL	63	I	selects PCC program memory at microcontroller interface
EN_WATCHDOG	64	I	enable watchdog input; when HIGH, the watchdog timer of the BMC is enabled

Note

1. **All** signals which are input or I/O, and which can be floating, need to be pulled up to V_{DD} or down to V_{SS} in order to protect the device against cross-currents. Exceptions are VREF and RSSI_AN, which do not have to be protected.

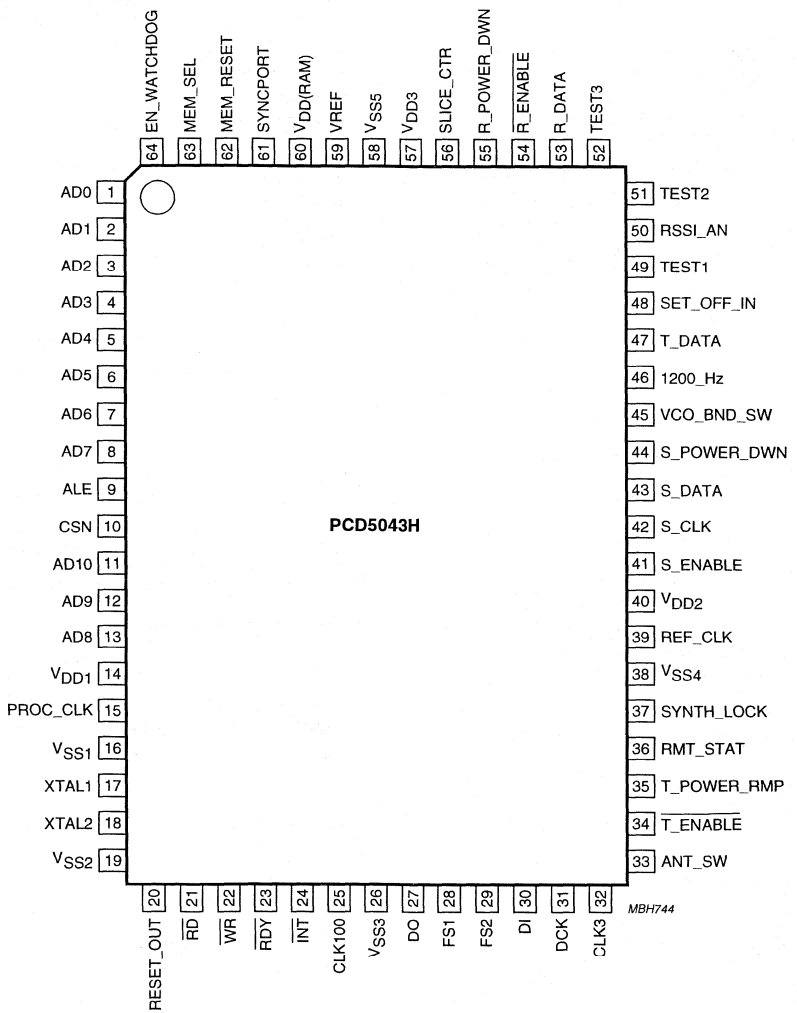

Fig.2 Pin configuration, PCD5043H.

6 FUNCTIONAL DESCRIPTION (see Fig.1)

The PCD5043 has dedicated hardware blocks containing logic for time-critical functions requiring bit or byte-time accuracy. Other functions requiring only slot-time accuracy are performed by software in the Preprogrammed Communication Controller (PCC). This approach offers maximum flexibility during prototyping.

6.1 Internal bus and data memory

6.1.1 INTERNAL BUS

The function of the internal bus is:

- To provide access for all functional blocks to the common data memory
- To provide access for the microcontroller-interface and the PCC to all other functional blocks.

All functional blocks (speech-interface, RF-interface, microcontroller-interface and PCC) can autonomously use the internal bus to communicate with the common data memory.

A bus controller is used to handle the bus priority mechanism. When several blocks request access simultaneously, the request with the highest priority is handled first.

6.1.2 DATA MEMORY

A large part of the data memory is used for the bit rate adaptation between the DECT radio interface and the speech interface. The data memory also acts as the main communication interface between the external microprocessor and the PCC.

6.2 Clock generation and correction (see Fig.3)

The device has an on-chip 13.824 MHz crystal oscillator. From this source, a few frequencies are derived for internal and external use. Frequencies generated for external use are:

- 13.824 MHz for the synthesizer reference (pin REF_CLK). This output is only provided if the synthesizer power-down control (output on pin S_POWER_DWN) is not selected.
- 0.144 to 13.824 MHz for the microcontroller clock (pin PROC_CLK)
- 3.456 MHz for the ADPCM codec (pin CLK3)
- 1200 Hz (pin 1200_HZ) for dual synthesizer switching
- 100 Hz (pin CLK100) indicates start of frame.

Nominally, the frequency on pin CLK3 is 3.456 MHz. This frequency is obtained by dividing the crystal frequency by 4. Sometimes, the crystal frequency will be divided by 3 or by 5, to synchronize the combination of the ADPCM codec and the device to an external source. External synchronization for base station applications is achieved as follows:

- **Master base station.** The master base station provides a 100 Hz signal to slave base stations on pin SYNCPORT. If the PCD5043 is connected to a digital interface (32-slot mode speech interface), the external synchronization will be done on the incoming 8 kHz signal. If it is connected to an analog line (12-slot mode speech interface), it will use its own crystal oscillator as reference.
- **Slave base station.** The slave base station will use the incoming SYNCPORT signal as synchronization reference.

6.3 Programmable communication controller and program memory

6.3.1 PCC

The PCC is a RISC-type controller and is used to control functions which are slot-time accurate. It is well suited for bit manipulation, and runs at a clock frequency of 6.912 MHz (equivalent to 3.4 Mips). After finishing a task, it switches to a power saving state, from which it returns after a pre-programmed time.

6.3.2 PCC FUNCTIONS

The most important functions of the PCC are to:

- Perform the appropriate actions on received messages: PMID and FMID checking, RFPI checking, TBC handling
- Prepare A-field messages for transmission
- Prepare the RF-interface for the coming slot
- Perform the procedures for RSSI and set-up scan, maintain scan counters and timers, assemble the RSSI field in the common data memory
- Filter events and indicate them to the microcontroller by interrupt.

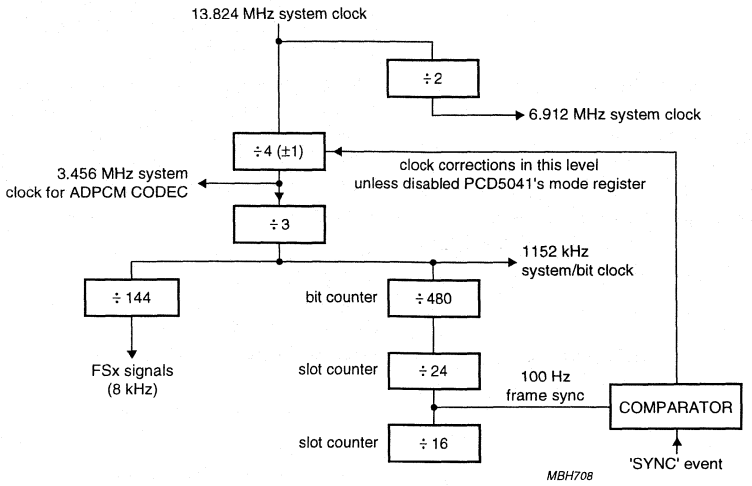

Fig.3 Internal clocking scheme of the PCD5043.

6.4 Speech interface

The speech interface block performs the following functions:

- Connection to a 1152 kbits/s interface in a handset and a simple base station in the so called '12 slot mode'
- Connection to a n x 64 kbits/s interface in base stations in the so called '32 slot mode'
- Autonomous storing/fetching of ADPCM speech data in/from the PCD5043's common data memory, using internal addressing logic
- Muting of speech data
- Local call.

6.4.1 12-SLOT MODE

The 12-slot mode is selected if up to 4 ADPCM codecs are connected to the PCD5043, where the PCD5043 is the master of these codecs. In a handset, or in a simple base stations which is connected with up to 4 analog lines to the public network, the PCD5043 is master of the codecs. Each codec is connected with a separate framing reference signal (FS1 to FS4) to the PCD5043. In the QFP64 package, 2 framing signals FS1 and FS2 are available, whereas in the LQFP80 package 4 framing signals can be used (FS1 to FS4). When more codecs are to be connected, the FS5 to FS12 signals have to be generated externally. When using the framing signals FS1 to FS4, no interface logic is required when using the PCD5032 ADPCM codec.

A speech-slot control table is used to determine where to store/fetch speech data for transmission and reception. The hardware speech-interface is capable of addressing the right speech buffer for the relevant speech slot, and will maintain a counter carrying the offset to the correct stored/fetched address.

6.4.2 32-SLOT MODE

The 32-slot mode is used to connect the PCD5043 to a digital interface with a data rate of n × 64 kbits/s; where n = 1 to 32 is the number of speech slots. This equates to data rates from 64 kbits/s to 2048 kbits/s.
Up to 12 of the 32 speech slots can be used simultaneously. The same kind of speech-slot control table used in the 12-slot mode is used for the 32-slot mode.

6.4.3 MUTING

Due to various reasons the quality of the incoming speech data may be degraded significantly. By muting the speech

data, these disturbances are not audible (or are less audible) to the user. The PCD5043 performs two types of muting:

- Fast muting
- Slow muting.

Fast muting, which is performed by the PCD5043 automatically, is nothing more than a repetition of the previously received frame (80 speech samples) to the ADPCM codec. It is issued if no Sync word was detected. Slow muting is issued by the microcontroller, after having detected a degradation of quality. A slow mute is implemented as a continuous '0000' nibble transmission to the ADPCM codec, until slow mute is released.

6.4.4 LOCAL CALL

A local call option is implemented, in order to loopback data from one codec to another codec, and vice versa, see Fig.4.

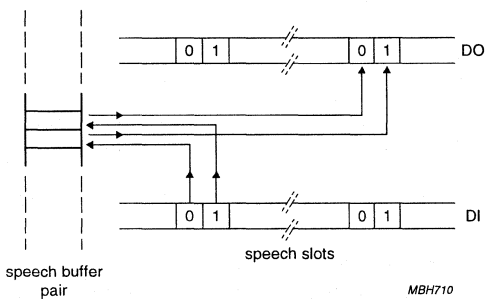

Fig.4 Local call switching on speech interface.

6.5 RF interface

Most of the functions performed by the RF interface are under control of the PCC. Specifically, the processing of non-speech data and the programming of functions and registers is done via the PCC.

6.5.1 SERIAL RECEIVER

The serial receiver processes the data, which comes from the RF section, and which is already filtered by the synchronization part. The data is latched, using the recovered data clock.

The serial receiver will collect the complete A-field and B-field and store it in the common data memory. Before the A-field is received, the A-field start address is programmed by the PCC. Upon reception of A-field nibbles, the address is updated by the serial receiver. Meanwhile, the PCC will program the B-field start address.

In Fig.5 the data flow in the serial receiver is shown. Note that almost no decoding of messages is required. Only the header of the A-field needs to be decoded to check if a ciphered message is being received or transmitted, which requires the ciphering to be switched on in the A-field also.

6.5.2 SERIAL TRANSMITTER

The serial transmitter performs the reverse of the receiver functions. Several blocks used in the receiver are also used in the transmitter. Amongst these are the CRC-generators, the scrambler, and the address registers. Figure 6 shows the serial transmitter structure.

By transmitting the X-CRC twice, the Z-field is transmitted. The handling of the address registers is the same for the transmitter. Transmission of the synchronization sequence (S-field) is done using the same method as the A-field and B-field. The S-field is stored in the common data memory and will be fetched by the transmitter, just before transmission.

Two additional functions are not shown in Fig.6:

- In the handset the data in the serial transmitter may be advanced by a programmable number of bit periods. This is done to compensate for the delay in the RF section
- The transmitted data can be inverted (using a switch in the PCD5043 mode register), in order to connect the PCD5043 to VCOs requiring negative modulation.

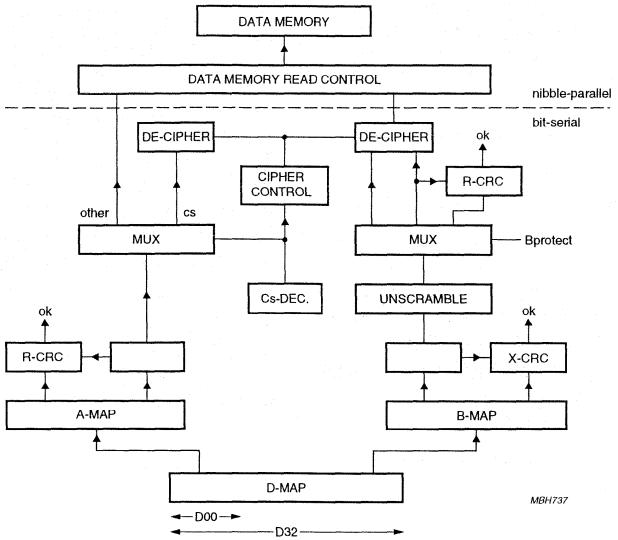

Fig.5 Serial receiver structure.

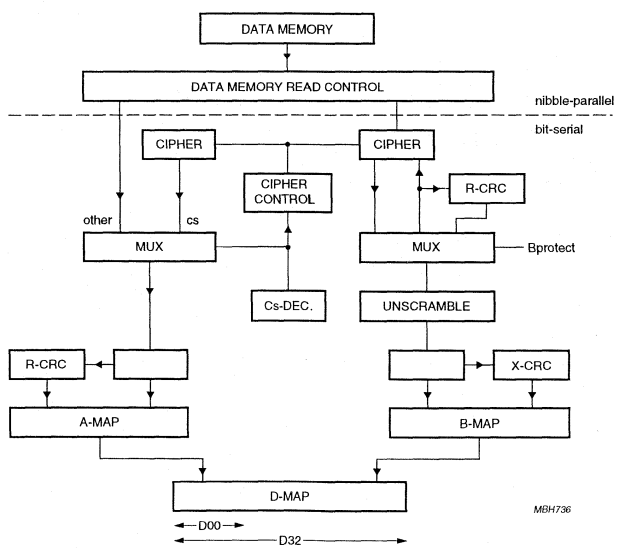

Fig.6 Serial transmitter structure.

6.5.3 SEAMLESS HANDOVER

Seamless handover guarantees that when speech information is switched from one slot to another, no speech samples are lost, added or displaced. Seamless handover is achieved in the RF interface by:

- Using a look-up table containing the correct start addresses of the B-fields in the data memory
- The RF receive and transmit blocks move data to/from the data memory block in 4-bit nibbles.

6.5.4 RF CONTROL SIGNALS

The timing of the control signals to the RF section is fixed, but such that an RF delay between 1.5 and 7 μs can be tolerated. Only the transmitter ramp signal and the synthesizer enable are programmable within certain limits.

6.5.5 SYNTHESIZER PROGRAMMING

To program a synthesizer, a 3-wire serial interface is used. The signals on this interface are:

- S_ENABLE (enable)
- S_CLK (clock)
- S_DATA (data).

To program various types of synthesizers, a 3-byte shift register is present. Three data formats are supported: 8, 16 or 24 bit words can be selected. The transfer of data from a frequency table in the common data memory to the shift register is under control of the PCC.

6.5.6 RSSI MEASUREMENT

The RSSI measurement in the PCD5043 RF-interface block is done in 3 parts: a peak/hold detector, a 6-bit A/D converter, and an RSSI control unit, which controls the peak/hold detector and the A/D converter. Once per slot time, a sample is fetched by the PCC and saved in the appropriate area of the common data memory.

If the radio receiver is active in a particular time slot, the RSSI value will automatically be measured in that slot. Adjustment to the RSSI_AN input level can be made with VREF.

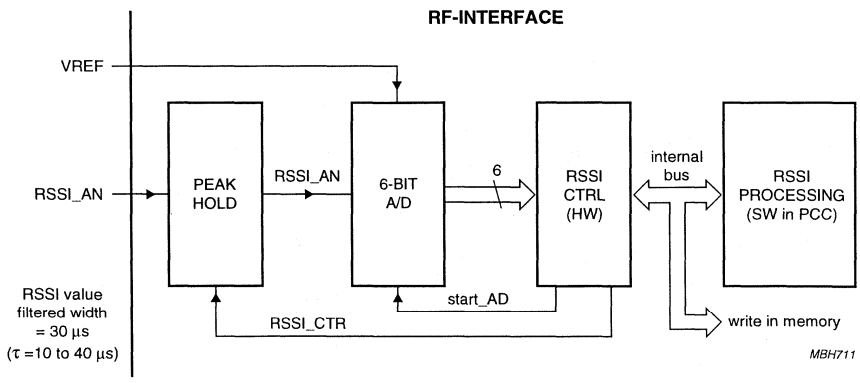

Fig.7 RSSI measurement path.

6.5.7 LOCAL CALL SWITCHING (see Fig.8)

The PCD5043 provides a local call switching function in the base station. It will store incoming speech nibbles in the common data memory, in the area reserved for that particular receive slot. Then, during the transmit phase, it passes the start pointer of the same data memory area to the transmit block. Thus, the speech data is echoed to the other user. To handle quality degradation for local calls, a mute can be performed at the RF side of the speech buffer.

6.5.8 DATA SYNCHRONIZATION (see Fig.9)

The data synchronization is done in 2 phases:

- Bit synchronization
- Sync word detection.

Bit synchronization is done using a Digital PLL (DPLL), with an oversampling factor of 12, i.e. the DPLL is running at 12 times the data rate. The output from the DPLL is a receive clock signal (RxC), which acts as the enable for a 20-bit shift register.

Sync word detection is achieved by checking the incoming data pattern with the expected synchronization field pattern, using a correlator.
The correlator has a programmable threshold, so it can accept bit errors in the sync field pattern up to the threshold level. Furthermore, the correlator window is programmable. This means that 'SlotSync', which indicates the slot synchronization event, can be detected only during a certain period (the time window).

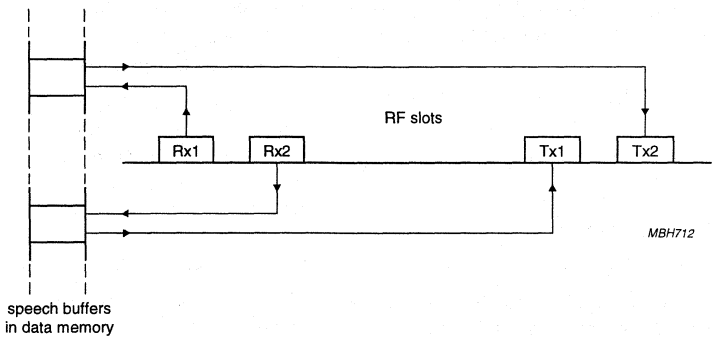

Fig.8 Local call switching on the RF-side.

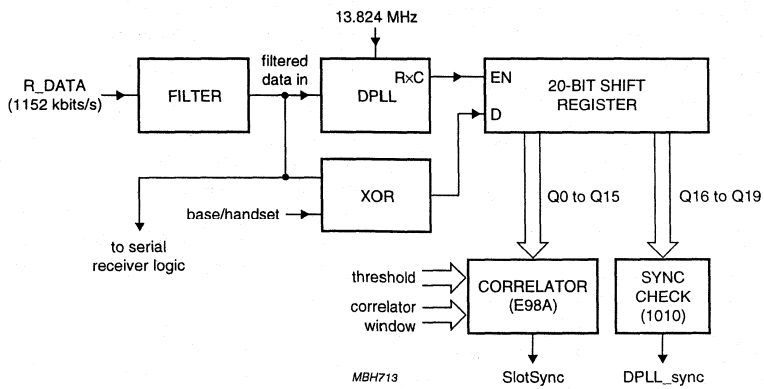

Fig.9 Schematic of the receiver synchronization part.

The 'DPLL_sync' indication should only be used, when 'SlotSync' is active. It indicates that the last 4 bits of the pre-amble field (the training sequence) are received correctly, and thus indicates that the DPLL was in lock (synchronized) in time. If the 'SlotSync' is active, and the 'DPLL_sync' is not, then a sliding interferer might have been detected.

If 'SlotSync' is not detected, effectively no data is received in that slot. This implies a 'fast mute' because speech data received in the previous frame is not destroyed.

6.5.9 CIPHERING MACHINE

The description of the cipher machine is subject to confidentiality. The specification of its algorithms are delivered by ETSI under the terms of a Non-Disclosure Agreement.

The cipher machine is under control of the TBC, which is implemented in the PCC. The cipher machine generates 2 fields of ciphering bits:

- A_cipher (40 bits) for A-field messages (ciphers tail only)
- B_cipher (320 bits) for speech in B-field.

The transmitted ciphered bits are then:

- A_ciphered: = A XOR A_cipher
- B_ciphered: = B XOR B_cipher.

On reception by the peer end point, deciphering consists of the same operation thanks to the synchronous generation of A_cipher and B_cipher.

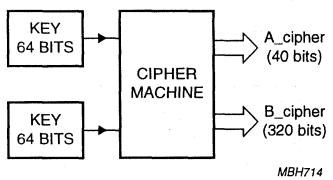

Fig.10 Cipher machine and its sources.

The cipher machine is time-multiplexed on a slot basis. Initially, the Initialisation Vector (IV) and the key must be loaded into the cipher machine. Transfer of the IV and key from the common data area to the cipher machine is done automatically by the cipher machine. The contents of the memory space where IV and key are found, are the responsibility of the PCC, and the external microprocessor.

6.6 Microcontroller Interface

6.6.1 FUNCTION OF THE MICROCONTROLLER INTERFACE

The microcontroller Interface will provide the following services.

- Direct interface to processors which have an INTEL-8051 compatible interface
- General interface to processors that can handle 'wait states' e.g. 68000-family; in this case glue logic is required
- Processor clock signal of which the frequency is programmable in order to adjust instantaneously processor performance to processor work load
- A programmable interrupt register
- A watchdog timer with time-out periods of 1.25 or 82 seconds, depending on the programming.

The microcontroller can address the PCD5043 as any other RAM memory connected to the microcontroller bus. By writing the 'Interface-Mode Register', the microcontroller can select the interface mode and its own clock frequency.

6.6.2 MICROCONTROLLER INTERRUPTS

The function of microcontroller Interrupts is to make optimal use of the microcontroller's processing power, and to achieve optimal cooperation between time-critical tasks and less time-critical tasks both executed in software. Three registers are available to handle interrupts. These are:

- Interrupt Event Register
- Interrupt Enable Register
- Interrupt Reset Register.

These registers are to be regarded together. Corresponding bits in these registers relate to one and the same event. Bits in the Interrupt Event Register are set by the PCC and are to be reset by the external processor by writing '1's in the corresponding bits in the Interrupt Reset Register. The mask in the Interrupt Enable Register enables the interrupt if corresponding events do occur.

6.6.3 WATCHDOG

The PCD5043 is equipped with a watchdog timer, which generates a reset towards an external device (e.g. a µC) after time-out. Two (fixed) time-out periods can be programmed; 1.25 s and 82 s. The watchdog function can be disabled by using the EN_WATCHDOG input pin.

6.6.4 POWER-DOWN

The PCC may switch off the 6.912 MHz internal clock, to enter a power saving mode. All blocks, running on this clock are then switched off (i.e. RF-interface, cipher block, speech interface, PCC). This is called the power-down state, and is only used in the handset mode.

The 13.824 MHz clock is never switched off. The Timing Control, microcontroller interface, and Bus Controller keep running, in order to remain synchronous with a base station, and to keep the wake-up circuitry active. During power-down the external microcontroller has still access to the common data area.

6.7 Survey of registers

For a survey of all addresses occupied refer to Tables 1 and 2. Some of the address locations are used differently for read and write. The addresses 000 to 7DF are occupied by RAM memory, while the upper 32 bytes are assigned to the hardware registers. A part of the RAM memory is allocated for use by the RF block, cipher block, and the speech interface.

Table 1 Hardware register addresses

ADDRESS	WRITE	READ
7E0	–	–
7E1	S-DATA1	–
7E2	S-DATA2	–
7E3	S-DATA3	RMT-STAT
7E4	–	RF-STATUS
7E5	B-field-shift	–
7E6	B-field-loc.	–
7E7	A-field-loc.	–
7E8	window-wide-off	–
7E9	window-wide-on	–
7EA	window-narrow-off	–
7EB	window-narrow-on	–
7EC	T-power-rmp-on	–
7ED	synth-off	–
7EE	RF-control-port	sync-status
7EF	slot-cnt-off	slot-counter-copy
7F0	frame-cnt-ref	RSSI
7F1	sync-ref-preset	bit-counter-copy1
7F2	bit-counter-preset	bit-counter-copy2
7F3	frame-counter	frame-counter
7F4	slot-counter	slot-counter
7F5	sync-control	sync-control
7F6	BMC-mode	BMC-mode
7F7	correlator-threshold	measure
7F8	watchdog-1	–
7F9	watchdog-2	–
7FA	–	–
7FB	–	–
7FC	interrupt-event	interrupt-event
7FD	interrupt-enable	interrupt-enable
7FE	interrupt-reset	–
7FF	controller mode	controller mode

Table 2 Fixed RAM locations

ADDRESS	ENTRY
740 to 747	cipher key vector #0
748 to 74F	cipher key vector #1
750 to 757	cipher key vector #2
758 to 75F	cipher key vector #3
760 to 767	cipher key vector #4
768 to 76F	cipher key vector #5
770 to 777	cipher key vector #6
778 to 77F	cipher key vector #7
780 to 787	cipher key vector #8
788 to 78F	cipher key vector #9
790 to 797	cipher key vector #10
798 to 79F	cipher key vector #11
7A0 to 7A7	cipher init vector
7A8 to 7AA	not used
7AB	XZ field buffer
7AC to 7AF	S-field buffer
7B0 to 7BB	cipher-slot-control-table
7BC to 7BF	not used
7C0 to 7DF	speech-slot-control-table

7 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	+6.5	V
V_i	all input voltages	−0.5	V_{DD} + 0.5	V
I_I	DC input current	−10	+10	mA
I_O	DC output current	−10	+10	mA
P_{tot}	total power dissipation	−	+500	mW
P_O	power dissipation per output	−	30	mW
I_{DD}	supply current	−100	+130	mA
I_{SS}	ground current	−100	+130	mA
T_{stg}	storage temperature range	−55	+100	°C
T_j	operating junction temperature	−	90	°C

8 CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
T_{amb}	operating ambient temperature		−25	−	+70	°C
V_{DD}	supply voltage		2.7	−	5.5	V
$V_{DD(ret)}$	RAM retention voltage		1.0	−	V_{DD}	V
I_{DD}	operating supply current	note 1	−	6	12	mA
$I_{DD(stb)}$	standby supply current	note 2	−	1	3	mA
	clock input duty cycle	All inputs LOW except WRN; XTAL1 running at 14 MHz	45	−	55	%
Digital I/O						
V_{IL}	LOW level input voltage		0	−	$0.3V_{DD}$	V
V_{OL}	LOW level output voltage		0	−	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	−	V_{DD}	V
V_{OH}	HIGH level output voltage		$0.7V_{DD}$	−	V_{DD}	V
I_{LI}	input leakage current				1.0	µA
$I_{O(source)}$	output source current	V_{DD} = 3.6 V; 0.4 V ≤ V_O ≤ V_{DD} − 0.4 V	2.0	5.0	−	mA
$I_{O(sink)}$	output sink current	V_{DD} = 3.6 V; 0.4 V ≤ V_O ≤ V_{DD} − 0.4 V	2.0	5.0	−	mA
$I_{RDYN(sink)}$	RDYN output sink current	V_{DD} = 3.6 V; V_O = 0.4 V	2.0	5.0	−	mA
		V_{DD} = 5.0 V; V_O = 0.4 V	−	6.0	−	mA
f_{DCK}	DCK input frequency	n = 1 to 32	−	n × 64	−	kHz
f_{FS1}	FS1 input frequency		−	8	−	kHz
Oscillator (inputs XTAL1 and XTAL2)						
g_m	transconductance	V_{DD} = 2.7 V	0.6	−	−	mS
		V_{DD} = 3.6 V	−	1.6	−	mS
R_F	feedback resistance		200	500		kΩ
RSSI Peak detector (6-bit linear A-D converter, for RSSI measurement on input RSSI_AN)						
$V_{i(RSSI\_AN)}$	input level		0	−	V_{DD}	V
$V_{conv(RSSI\_AN)}$	voltage conversion range		0	−	V_{REF}	V
$V_{i(VREF)}$	V_{REF} input voltage		1.0	3.0	V_{DD}	V
$Z_{i(VREF)}$	V_{REF} input impedance	during power-down high impedance	−	50	−	kΩ
t_{conv}	conversion time		18.4	−	−	µs
	integral non-linearity		−	−	4	LSB
	differential non-linearity	note 3	−	0.2	1.5	LSB
$Z_{i(RSSI\_AN)}$	input impedance RSSI_AN		−	1	−	MΩ

Notes to the characteristics

1. V_{DD} = 3.0 V; f_{clk} =13.824 MHz; no external load; one speech link active (under typical conditions).
2. V_{DD} = 3.0 V; f_{clk} =13.824 MHz; no external load; after reset.
3. Maximum differential non-linearity at supply voltage 5.5 V and V_{REF} = 1 V.

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1 FEATURES

- 80C51 ports P0, P1, P2 and P3 available for interfacing to display, keyboard, I^2C-bus, interrupt sources and/or external memory. Integrated 64 kbyte ROM, 3 kbytes of data memory and 1 kbyte SDR-RAM. External program memory is addressable up to 128 kbytes
- +2.7 to +5 V port (P0 to P3) interface
- TDMA frame (de)multiplexing. Transmission or reception can be programmed for any slot
- Ciphering, scrambling, CRC checking/generation and protected B-fields
- Speech and data buffering space for six handsets
- Local call and B-field loop-back
- Two interrupt lines for BML and DSP to interrupt 80C51
- On-chip, three-channel time-multiplexed 8-bit Analog-to-Digital Converter (ADC) for RSSI measurement, one for battery voltage measurement and one channel available for other purposes
- On-chip 8-bit Digital-to-Analog Converter (DAC) for electronic potentiometer function
- Phase error measurement and phase error correction by hardware
- DACs and ADCs for dynamic earpiece and dynamic or electret microphone
- On-chip reference voltage
- On-chip supply for electret microphone
- Very low ohmic buzzer output
- Serial interface to external ADPCM CODEC (PCD5032) or 8 kHz u-law samples
- Speech switch for Digital Telephone Answering Machine (DTAM) connected to SPI interface
- IOM-2 interface (Siemens registered trademark)
- Serial interface to synthesizer for frequency programming
- Programmable polarity and timing of radio-control signals
- GMSK pulse shaper
- Easy interfacing with radio circuits, operating at other supply voltage (RF supply pin with level shifter for RF signals)
- On-chip comparator for use as data-slicer
- Low power oscillator with integrated frequency adjustment
- QFP100 and LQFP100 packages
- Power-on-reset
- Programmable power-down modes
- Low supply voltage (2.7 to 3.6 V)
- CMOS technology.

1.1 DSP software features

- ADPCM encoding and decoding complying with G.721
- Volume control
- Speech filters
- Programmable gain in speech paths
- Side tone and soft mute
- Two tone (DTMF) generators
- Automatic gain control
- Hands-free operation

For each DSP software version a separate manual is available in which detailed information is provided on how parameters must be set. For further information please contact Philips Semiconductors.

2 GENERAL DESCRIPTION

The PCD5091 is designed for GAP-compliant handsets with speaker-phone option. It has an embedded 80C51 microcontroller with twice the performance of the classic architecture, 64 kbytes of PROM program memory and 3 kbytes of data memory on-chip. In addition there is 1 kbyte of on-chip data memory that is shared with on-chip Burst Mode Logic (BML) and DSP, the System Data RAM (SDR).

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD5091H	QFP100	plastic quad flat package; 100 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT317-2
PCD5091HZ	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1

4 BLOCK DIAGRAM

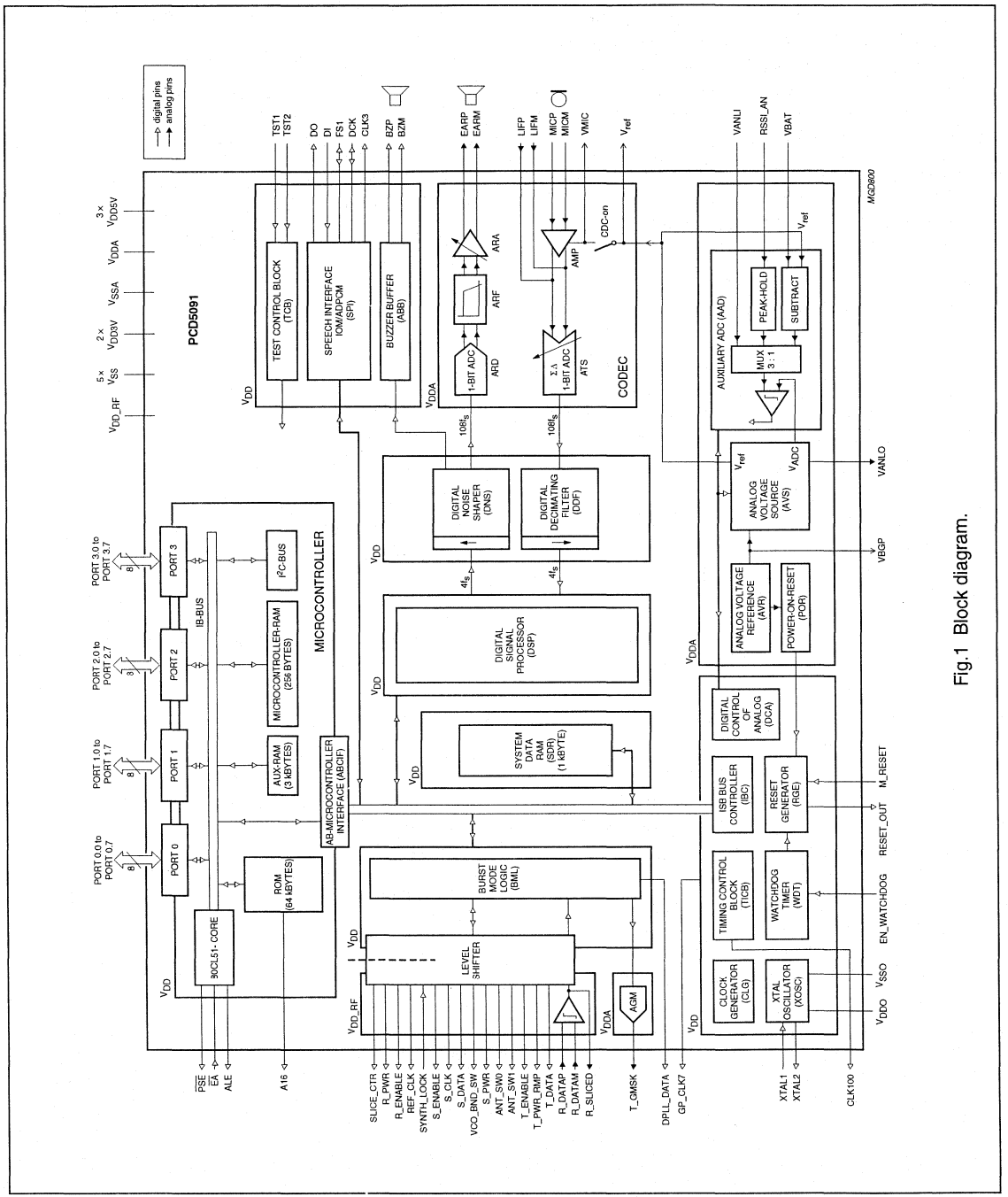


Fig.1 Block diagram.

5 PINNING INFORMATION

5.1 Pinning

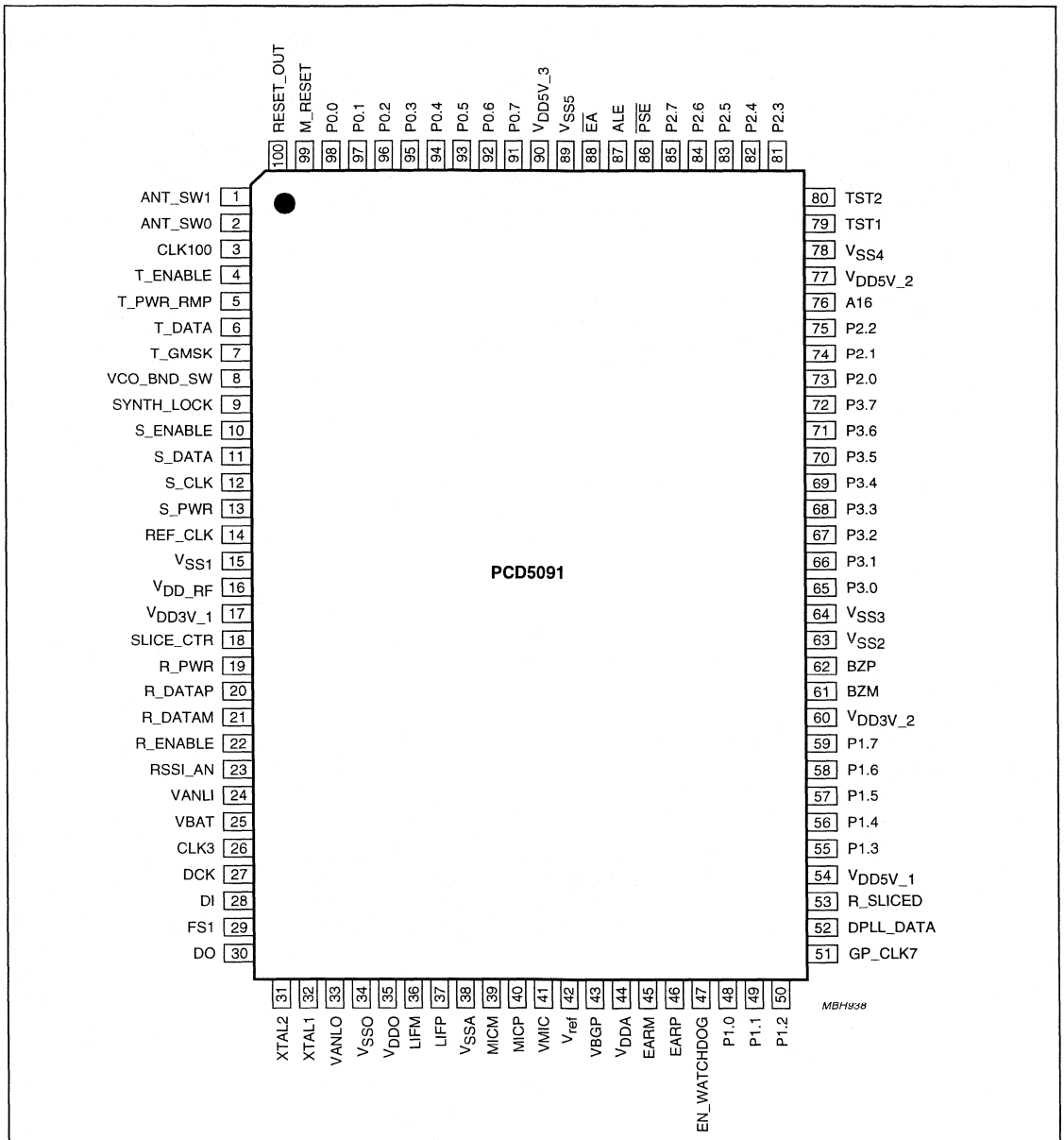


Fig.2 Pin configuration (QFP100).

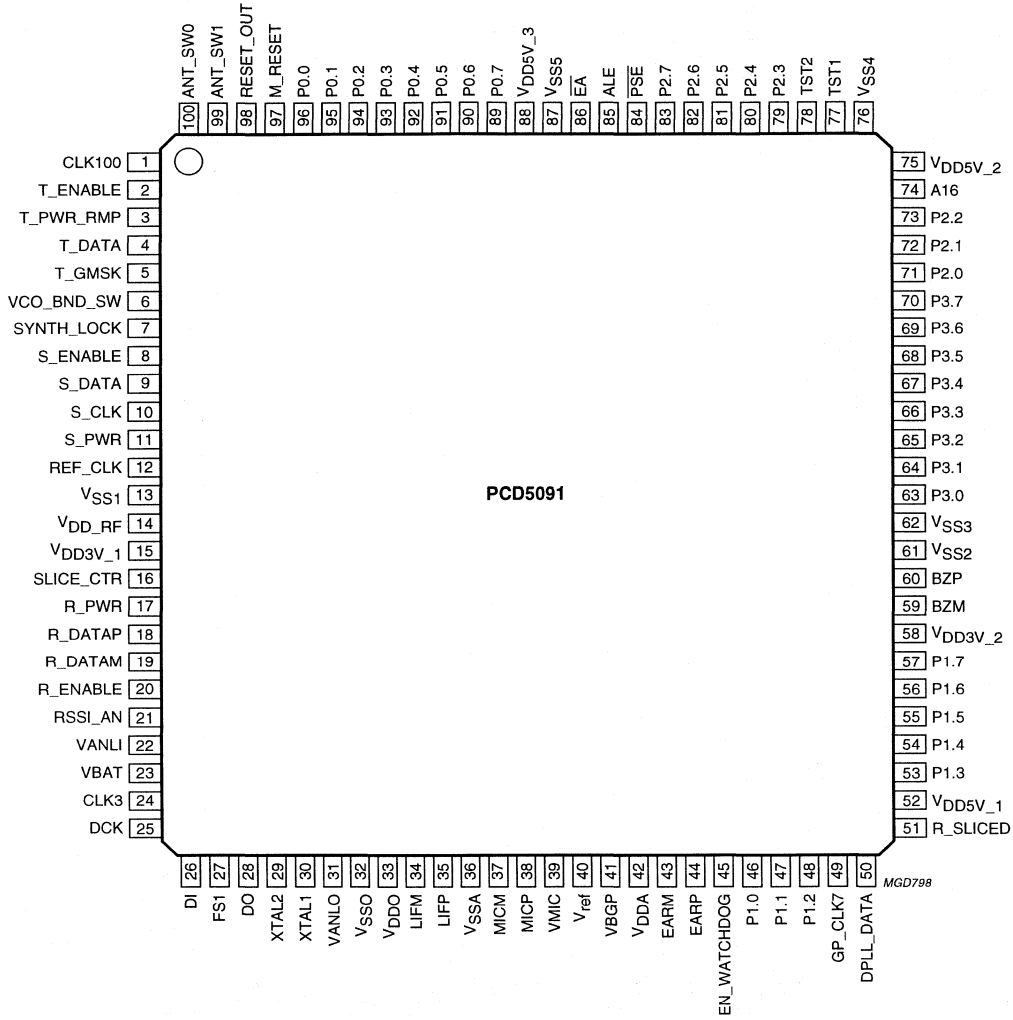


Fig.3 Pin configuration (LQFP100).

5.2 Pin description

Table 1 QFP100 and LQFP100 packages

SYMBOL	PIN		I/O	STATE AFTER RESET	PIN TYPE	PIN DESCRIPTION
	QFP100	LQFP100				
ANT_SW1	1	99	O	H	ISP2DRF3	antenna switch 1 output
ANT_SW0	2	100	O	H	ISP2DRF3	antenna switch 0 output
CLK100	3	1	O	H	ISP2DPES	100 Hz signal related to DECT frame timing output
T_ENABLE	4	2	O	H	ISP2DRF3	enable transmitter output
T_PWR_RMP	5	3	O	L	ISP2DRF3	switch transmitter power output
T_DATA	6	4	O	off	ISF2DRF3	unmodulated transmitter data output
T_GMSK	7	5	O	L	ANAIOD1	GMSK modulated transmitter data output
VCO_BND_SW	8	6	O	L	ISP2DRF3	VCO band switch output
SYNTH_LOCK	9	7	I	–	DIPP0RF3	synthesizer lock input
S_ENABLE	10	8	O	L	ISP2DRF3	synthesizer enable output
S_DATA	11	9	O	L	ISP2DRF3	serial synthesizer data output
S_CLK	12	10	O	L	ISP2DRF3	clock for serial synthesizer interface output
S_PWR	13	11	O	H	ISP2DRF3	switch synthesizer power output
REF_CLK	14	12	O	running	ISP4DRF3	13.824 MHz reference clock for synthesizer output
V_{SS1}	15	13	–	–	supply	negative supply voltage 1
V_{DD_RF}	16	14	–	–	supply	positive supply voltage for RF interface level shifters
V_{DD3V_1}	17	15	–	–	supply	positive supply voltage 1 (+3 V)
SLICE_CTR	18	16	O	L	ISP2DRF3	switch slicer time constant output
R_PWR	19	17	O	H	ISP2DRF3	switch receiver power output
R_DATAP	20	18	I	–	ANAIOD2	positive input for receiver data
R_DATAM	21	19	I	–	ANAIOD2	negative input for receiver data
R_ENABLE	22	20	O	H	ISP2DRF3	enable receiver output
RSSI_AN	23	21	I	–	ANAIOD1	analog input for RSSI measurement
VANLI	24	22	I	–	ANAIOD1	analog input to ADC
VBAT	25	23	I	–	ANAIOD1	analog input for battery voltage measurement
CLK3	26	24	O	L	ISP2DPES	3.456 MHz clock output for external ADPCM codec

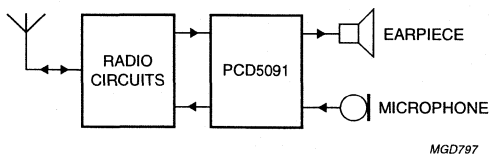
SYMBOL	PIN		I/O	STATE AFTER RESET	PIN TYPE	PIN DESCRIPTION
	QFP100	LQFP100				
DCK	27	25	I/O	input	ISF2DPES ISF2UPES	ADPCM output or IOM data clock input/output (ISF2UPES in PCD5090/xxx, PCA5097/xxx)
DI	28	26	I	–	DIPP0PES	ADPCM or IOM data input
FS1	29	27	I/O	input	ISF2DPES ISF2UPES	8 kHz framing input/output (ISF2UPES in PCD5090/xxx, PCA5097/xxx)
DO	30	28	O	off	ISI8DPES	ADPCM or IOM data output
XTAL2	31	29	O	running	ANAIOD1	crystal oscillator output
XTAL1	32	30	I	–	ANAIOD1	crystal oscillator input
VANLO	33	31	O	1.0 V	ANAIOD1	analog output from D/A converter
V_{SSO}	34	32	–	–	supply	negative supply voltage for the oscillator
V_{DDO}	35	33	–	–	supply	positive supply voltage for the oscillator
LIFM	36	34	I	0.7 V	ANAIOD1	negative input from line interface
LIFP	37	35	I	0.7 V	ANAIOD1	positive input from line interface
V_{SSA}	38	36	–	–	supply	negative supply voltage for analog circuits
MICM	39	37	I	0.7 V	ANAIOR1	negative input from microphone
MICP	40	38	I	0.7 V	ANAIOR1	positive input from microphone
VMIC	41	39	O	off	ANAIOD1	positive microphone supply voltage (+2 V)
V_{ref}	42	40	O	2.0 V	ANAIOD1	reference voltage (+2 V)
VBGP	43	41	O	1.25 V	ANAIOR1	bandgap output voltage (+1.25 V)
V_{DDA}	44	42	–	–	supply	positive supply voltage for analog circuits
EARM	45	43	O	1.4 V	ANAIOD1	negative output to earpiece
EARP	46	44	O	1.4 V	ANAIOD1	positive output to earpiece
EN_WATCHDOG	47	45	I	–	DIUP0PES	watchdog enable input
P1.0	48	46	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P1.1	49	47	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P1.2	50	48	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
GP_CLK7	51	49	O	L	ISP2DPES	general purpose 6.912 MHz output
DPLL_DATA	52	50	O	L	ISP2DPES	data after clock recovery network
R_SLICED	53	51	O	L	ISP2DPES	R_DATA comparator output
V_{DD5V_1}	54	52	–	–	supply	positive supply voltage 1 for the +5 V interface
P1.3	55	53	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P1.4	56	54	I/O	H	ISQ2CPES	bidirectional 80C51 port pin

SYMBOL	PIN		I/O	STATE AFTER RESET	PIN TYPE	PIN DESCRIPTION
	QFP100	LQFP100				
P1.5	57	55	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P1.6	58	56	I/O	off	ISI8DPES	bidirectional 80C51 port pin
P1.7	59	57	I/O	off	ISI8DPES	bidirectional 80C51 port pin
V_{DD3V_2}	60	58	–	–	supply	positive supply voltage 2 (+3 V)
BZM	61	59	O	L	ANAIOD2	negative buzzer output
BZP	62	60	O	L	ANAIOD2	positive buzzer output
V_{SS2}	63	61	–	–	supply	negative supply voltage 2
V_{SS3}	64	62	–	–	supply	negative supply voltage 3
P3.0	65	63	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.1	66	64	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.2	67	65	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.3	68	66	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.4	69	67	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.5	70	68	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.6	71	69	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.7	72	70	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.0	73	71	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.1	74	72	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.2	75	73	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
A16	76	74	O	L	ISP4DPES	address bit 16 for 128 kbytes external program memory
V_{DD5V_2}	77	75	–	–	supply	positive supply voltage 2 for the +5 V interface
V_{SS4}	78	76	–	–	supply	negative supply voltage 4
TST1	79	77	I	–	DIDP0PES	test input 1
TST2	80	78	I	–	DIDP0PES	test input 2
P2.3	81	79	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.4	82	80	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.5	83	81	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.6	84	82	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.7	85	83	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
$\overline{PSE}$	86	84	O	H	ISQ2CPES	program store enable (80C51); active LOW
ALE	87	85	O	H	ISQ4CPES	address latch enable (80C51)

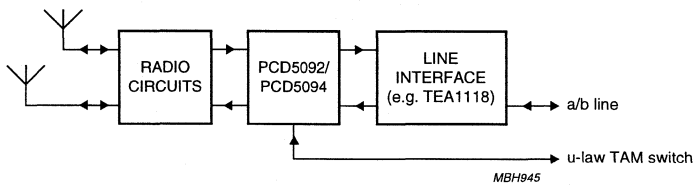
SYMBOL	PIN		I/O	STATE AFTER RESET	PIN TYPE	PIN DESCRIPTION
	QFP100	LQFP100				
$\overline{EA}$	88	86	I	–	ISF2DPES	external access enable (80C51); active LOW
V_{SS5}	89	87	–	–	supply	negative supply voltage 5
V_{DD5V_3}	90	88	–	–	supply	positive supply voltage 3 for the +5 V interface
P0.7	91	89	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.6	92	90	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.5	93	91	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.4	94	92	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.3	95	93	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.2	96	94	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.1	97	95	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.0	98	96	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
M_RESET	99	97	I	–	DIDP0PES	master reset input (Schmitt trigger)
RESET_OUT	100	98	O	H	ISF2DPES	reset output

6 FUNCTIONAL DESCRIPTION

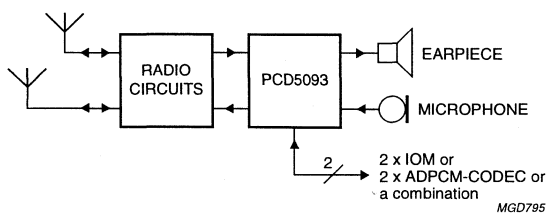
The PCD509x is a family of single-chip controllers, designed for use in Digital Enhanced Cordless Telecommunications systems (DECT). The family is designed for minimum component-count and minimum power consumption. All controllers include an embedded 80C51 microcontroller with on-chip memory and I²C-bus. The Philips DECT RF interface is implemented. The Burst Mode Logic (BML) performs the time-critical MAC layer functions for applications in DECT handsets and base stations. The ADPCM transcoding is in compliance with the CCITT recommendation G.721 and includes receive and transmit filters.



a. Handset.



b. Base with analog interface and echo cancellation; up to 6 portables can be handled.



c. Base with digital interface and analog handset connected; up to 6 portables can be handled.

Fig.4 Block diagrams of DECT systems with PCX509x.

CONTENTS

1 FEATURES
1.1 DSP software features
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1 FEATURES

- 80C51 ports P0, P1, P2 and P3 available for interfacing to display, keyboard, I²C-bus, interrupt sources and/or external memory. Integrated 64 kbyte ROM, 3 kbytes of data memory and 1 kbyte SDR-RAM. External program memory is addressable up to 128 kbytes
- +2.7 to +5 V port (P0 to P3) interface
- TDMA frame (de)multiplexing. Transmission or reception can be programmed for any slot.
- Ciphering, scrambling, CRC checking/generation and protected B-fields
- Speech and data buffering space for six handsets
- Local call and B-field loop-back
- Two interrupt lines for BML and DSP to interrupt 80C51
- On-chip, three-channel time-multiplexed 8-bit Analog-to-Digital Converter (ADC) for RSSI measurement, one for battery voltage measurement and one channel available for other purposes
- On-chip 8-bit Digital-to-Analog Converter (DAC) for electronic potentiometer function
- Phase error measurement and phase error correction by hardware
- DACs and ADCs for dynamic earpiece and dynamic or electret microphone
- On-chip reference voltage
- On-chip supply for electret microphone
- Very low ohmic buzzer output
- Serial interface to external ADPCM CODEC (PCD5032) or 8 kHz u-law samples
- Speech switch for Digital Telephone Answering Machine (DTAM) connected to SPI interface
- IOM-2 interface (Siemens registered trademark)
- Serial interface to synthesizer for frequency programming
- Programmable polarity and timing of radio-control signals
- GMSK pulse shaper
- Easy interfacing with radio circuits, operating at other supply voltage (RF supply pin with level shifter for RF signals)
- On-chip comparator for use as data-slicer
- Low power oscillator with integrated frequency adjustment
- QFP100 package
- Power-on-reset
- Programmable power-down modes
- Low supply voltage (2.7 to 3.6 V)
- CMOS technology.

1.1 DSP software features

- ADPCM encoding and decoding complying with G.721
- u-law encoding and decoding complying with G.711
- Echo cancellation and network echo suppressor
- Speech filters
- Programmable gain in speech paths
- Side tone and soft mute
- Ringer and tone (DTMF) generator
- Automatic gain control
- Telephone Answering Machine (TAM) switch.

For each DSP software version a separate manual is available in which detailed information is provided on how parameters must be set. For further information please contact Philips Semiconductors.

2 GENERAL DESCRIPTION

The PCD5092 is designed for GAP-compliant single a/b line basestations with answering machine switch. It has an embedded 80C51 microcontroller with twice the performance of the classic architecture, 64 kbytes of PROM program memory and 3 kbytes of data memory on-chip. In addition there is 1 kbyte of on-chip data memory that is shared with on-chip Burst Mode Logic (BML) and DSP, the System Data RAM (SDR).

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD5092H	QFP100	plastic quad flat package; 100 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT317-2

4 BLOCK DIAGRAM

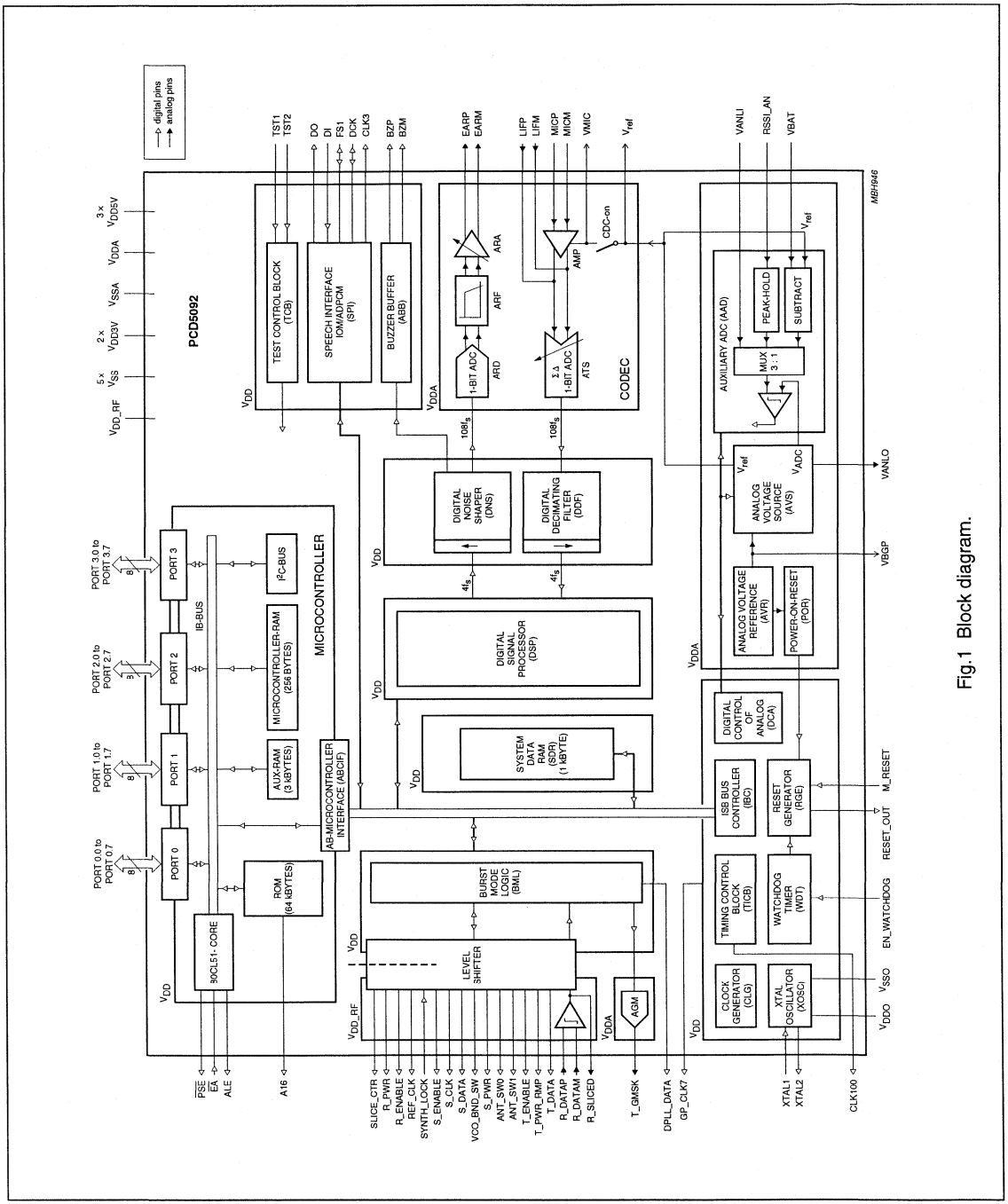


Fig.1 Block diagram.

5 PINNING INFORMATION

5.1 Pinning

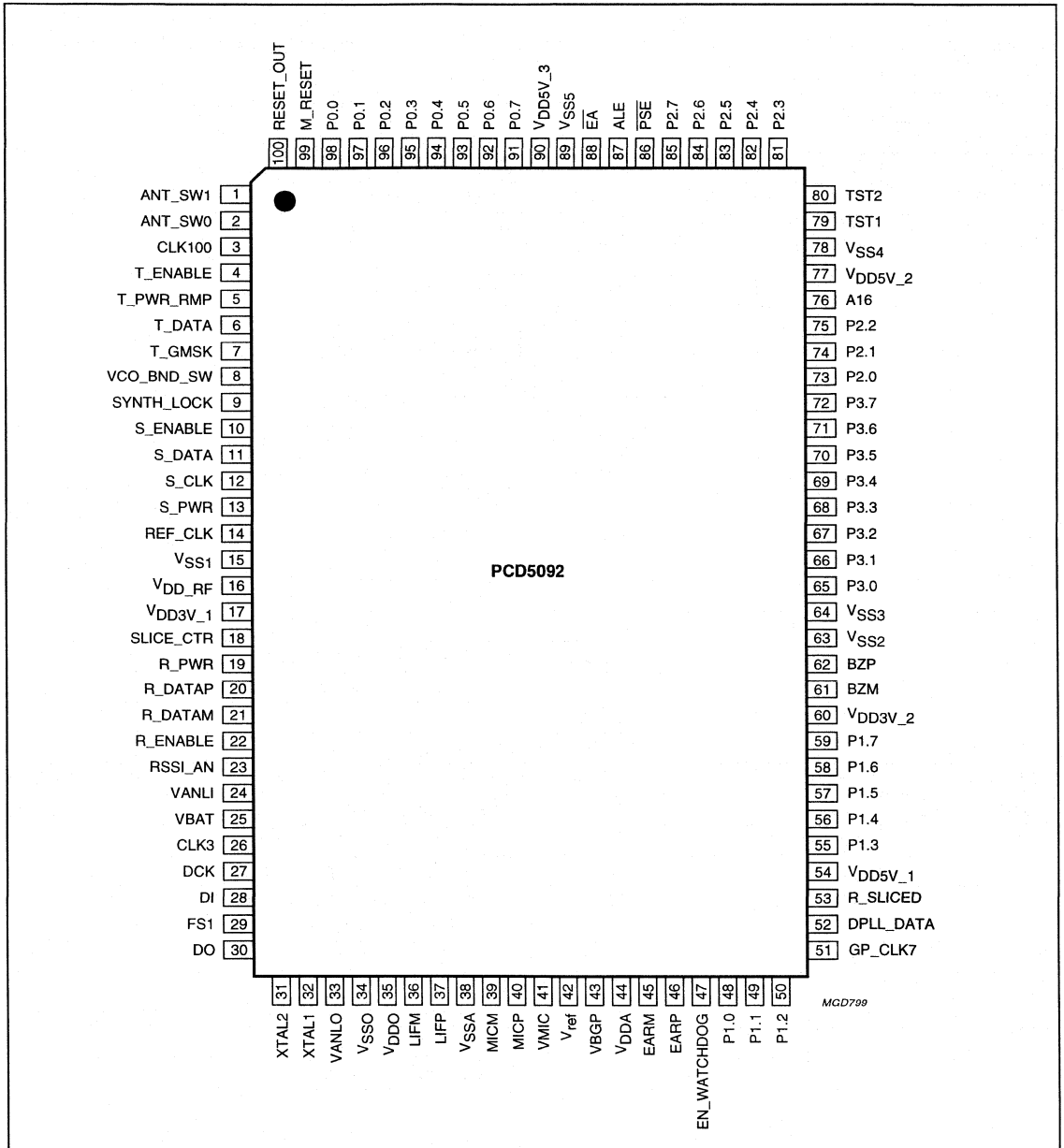


Fig.2 Pin configuration (QFP100).

5.2 Pin description

Table 1 QFP100 package

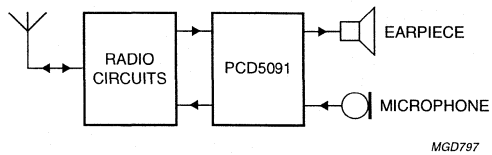
SYMBOL	PIN	I/O	STATE AFTER RESET	PIN TYPE	PIN DESCRIPTION
ANT_SW1	1	O	H	ISP2DRF3	antenna switch 1 output
ANT_SW0	2	O	H	ISP2DRF3	antenna switch 0 output
CLK100	3	O	H	ISP2DPES	100 Hz signal related to DECT frame timing output
T_ENABLE	4	O	H	ISP2DRF3	enable transmitter output
T_PWR_RMP	5	O	L	ISP2DRF3	switch transmitter power output
T_DATA	6	O	off	ISF2DRF3	unmodulated transmitter data output
T_GMSK	7	O	L	ANAIOD1	GMSK modulated transmitter data output
VCO_BND_SW	8	O	L	ISP2DRF3	VCO band switch output
SYNTH_LOCK	9	I	–	DIPP0RF3	synthesizer lock input
S_ENABLE	10	O	L	ISP2DRF3	synthesizer enable output
S_DATA	11	O	L	ISP2DRF3	serial synthesizer data output
S_CLK	12	O	L	ISP2DRF3	clock for serial synthesizer interface output
S_PWR	13	O	H	ISP2DRF3	switch synthesizer power output
REF_CLK	14	O	running	ISP4DRF3	13.824 MHz reference clock for synthesizer output
V_{SS1}	15	–	–	supply	negative supply voltage 1
V_{DD_RF}	16	–	–	supply	positive supply voltage for RF interface level shifters
V_{DD3V_1}	17	–	–	supply	positive supply voltage 1 (+3 V)
SLICE_CTR	18	O	L	ISP2DRF3	switch slicer time constant output
R_PWR	19	O	H	ISP2DRF3	switch receiver power output
R_DATAP	20	I	–	ANAIOD2	positive input for receiver data
R_DATAM	21	I	–	ANAIOD2	negative input for receiver data
R_ENABLE	22	O	H	ISP2DRF3	enable receiver output
RSSI_AN	23	I	–	ANAIOD1	analog input for RSSI measurement
VANLI	24	I	–	ANAIOD1	analog input to ADC
VBAT	25	I	–	ANAIOD1	analog input for battery voltage measurement
CLK3	26	O	L	ISP2DPES	3.456 MHz clock output for external ADPCM codec
DCK	27	I/O	input	ISF2DPES ISF2UPES	ADPCM output or IOM data clock input/output (ISF2UPES in PCD5090/xxx, PCA5097/xxx)
DI	28	I	–	DIPP0PES	ADPCM or IOM data input
FS1	29	I/O	input	ISF2DPES ISF2UPES	8 kHz framing input/output (ISF2UPES in PCD5090/xxx, PCA5097/xxx)
DO	30	O	off	ISI8DPES	ADPCM or IOM data output
XTAL2	31	O	running	ANAIOD1	crystal oscillator output
XTAL1	32	I	–	ANAIOD1	crystal oscillator input
VANLO	33	O	1.0 V	ANAIOD1	analog output from D/A converter

SYMBOL	PIN	I/O	STATE AFTER RESET	PIN TYPE	PIN DESCRIPTION
V_{SSO}	34	–	–	supply	negative supply voltage for the oscillator
V_{DDO}	35	–	–	supply	positive supply voltage for the oscillator
LIFM	36	I	0.7 V	ANAIOD1	negative input from line interface
LIFP	37	I	0.7 V	ANAIOD1	positive input from line interface
V_{SSA}	38	–	–	supply	negative supply voltage for analog circuits
MICM	39	I	0.7 V	ANAIOR1	negative input from microphone
MICP	40	I	0.7 V	ANAIOR1	positive input from microphone
VMIC	41	O	off	ANAIOD1	positive microphone supply voltage (+2 V)
V_{ref}	42	O	2.0 V	ANAIOD1	reference voltage (+2 V)
VBGP	43	O	1.25 V	ANAIOR1	bandgap output voltage (+1.25 V)
V_{DDA}	44	–	–	supply	positive supply voltage for analog circuits
EARM	45	O	1.4 V	ANAIOD1	negative output to earpiece
EARP	46	O	1.4 V	ANAIOD1	positive output to earpiece
EN_WATCHDOG	47	I	–	DIUP0PES	watchdog enable input
P1.0	48	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P1.1	49	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P1.2	50	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
GP_CLK7	51	O	L	ISP2DPES	general purpose 6.912 MHz output
DPLL_DATA	52	O	L	ISP2DPES	data after clock recovery network
R_SLICED	53	O	L	ISP2DPES	R_DATA comparator output
V_{DD5V_1}	54	–	–	supply	positive supply voltage 1 for the +5 V interface
P1.3	55	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P1.4	56	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P1.5	57	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P1.6	58	I/O	off	ISI8DPES	bidirectional 80C51 port pin
P1.7	59	I/O	off	ISI8DPES	bidirectional 80C51 port pin
V_{DD3V_2}	60	–	–	supply	positive supply voltage 2 (+3 V)
BZM	61	O	L	ANAIOD2	negative buzzer output
BZP	62	O	L	ANAIOD2	positive buzzer output
V_{SS2}	63	–	–	supply	negative supply voltage 2
V_{SS3}	64	–	–	supply	negative supply voltage 3
P3.0	65	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.1	66	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.2	67	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.3	68	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.4	69	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.5	70	I/O	H	ISQ2CPES	bidirectional 80C51 port pin

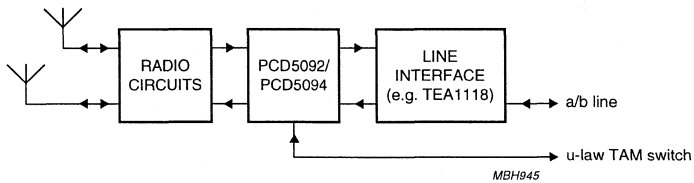
SYMBOL	PIN	I/O	STATE AFTER RESET	PIN TYPE	PIN DESCRIPTION
P3.6	71	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.7	72	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.0	73	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.1	74	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.2	75	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
A16	76	O	L	ISP4DPES	address bit 16 for 128 kbytes external program memory
V_{DD5V_2}	77	–	–	supply	positive supply voltage 2 for the +5 V interface
V_{SS4}	78	–	–	supply	negative supply voltage 4
TST1	79	I	–	DIDP0PES	test input 1
TST2	80	I	–	DIDP0PES	test input 2
P2.3	81	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.4	82	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.5	83	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.6	84	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.7	85	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
$\overline{PSE}$	86	O	H	ISQ2CPES	program store enable (80C51); active LOW
ALE	87	O	H	ISQ4CPES	address latch enable (80C51)
$\overline{EA}$	88	I	–	ISF2DPES	external access enable (80C51); active LOW
V_{SS5}	89	–	–	supply	negative supply voltage 5
V_{DD5V_3}	90	–	–	supply	positive supply voltage 3 for the +5 V interface
P0.7	91	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.6	92	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.5	93	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.4	94	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.3	95	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.2	96	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.1	97	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.0	98	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
M_RESET	99	I	–	DIDP0PES	master reset input (Schmitt trigger)
RESET_OUT	100	O	H	ISF2DPES	reset output

6 FUNCTIONAL DESCRIPTION

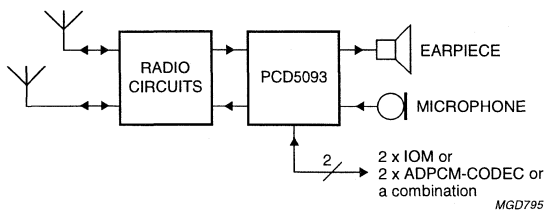
The PCD509x is a family of single-chip controllers, designed for use in Digital Enhanced Cordless Telecommunications systems (DECT). The family is designed for minimum component-count and minimum power consumption. All controllers include an embedded 80C51 microcontroller with on-chip memory and I²C-bus. The Philips DECT RF interface is implemented. The Burst Mode Logic (BML) performs the time-critical MAC layer functions for applications in DECT handsets and base stations. The ADPCM transcoding is in compliance with the CCITT recommendation G.721 and includes receive and transmit filters.



a. Handset.



b. Basestation (PCD5092) with analog interface and echo cancellation; up to 6 portables can be handled.



c. Base with digital interface and analog handset connected; up to 6 portables can be handled.

Fig.3 Block diagrams of DECT systems with PCX509x.

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1 FEATURES

- 80C51 ports P0, P1, P2 and P3 available for interfacing to display, keyboard, I²C-bus, interrupt sources and/or external memory. Integrated 64 kbyte ROM, 3 kbytes of data memory and 1 kbyte SDR-RAM. External program memory is addressable up to 128 kbytes
- +2.7 to +5 V port (P0 to P3) interface
- TDMA frame (de)multiplexing. Transmission or reception can be programmed for any slot
- Ciphering, scrambling, CRC checking/generation and protected B-fields
- Speech and data buffering space for six handsets
- Local call and B-field loop-back
- Two interrupt lines for BML and DSP to interrupt 80C51
- On-chip, three-channel time-multiplexed 8-bit Analog-to-Digital Converter (ADC) for RSSI measurement, one for battery voltage measurement and one channel available for other purposes
- On-chip 8-bit Digital-to-Analog Converter (DAC) for electronic potentiometer function
- Phase error measurement and phase error correction by hardware
- DACs and ADCs for dynamic earpiece and dynamic or electret microphone
- On-chip reference voltage
- On-chip supply for electret microphone
- Very low ohmic buzzer output
- Serial interface to external ADPCM CODEC (PCD5032) or 8 kHz u-law samples
- Speech switch for Digital Telephone Answering Machine (DTAM) connected to SPI interface
- IOM-2 interface (Siemens registered trademark)
- Serial interface to synthesizer for frequency programming
- Programmable polarity and timing of radio-control signals
- GMSK pulse shaper
- Easy interfacing with radio circuits, operating at other supply voltages (RF supply pin with level shifter for RF signals)
- On-chip comparator for use as data-slicer
- Low power oscillator with integrated frequency adjustment
- QFP100 package
- Power-on-reset
- Low supply voltage (2.7 to 3.6 V)
- CMOS technology.

1.1 DSP software features

- ADPCM encoding and decoding complying with G.721
- Up to two A-law channels
- Network echo suppressor
- Support of local corded handset with handsfree feature
- Speech filters
- Programmable gain in speech paths
- Side tone and soft mute
- Ringer and tone (DTMF) generator
- Automatic gain control
- Direct connection to universal codec PCD5096
- Conference between IOM-2 buffer(s) and two handsets.

For each DSP software version a separate manual is available in which detailed information is provided on how parameters must be set. For further information please contact Philips Semiconductors.

2 GENERAL DESCRIPTION

The PCD5093 is designed as GAP-compliant basestation chip for ISDN or n lines (PCD5096) business systems. It has an embedded 80C51 microcontroller with twice the performance of the classic architecture, 64 kbytes of PROM program memory and 3 kbytes of data memory on chip. In addition there is 1 kbyte of on-chip data memory that is shared with on-chip Burst Mode Logic (BML) and DSP, the System Data RAM (SDR).

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD5093H	QFP100	plastic quad flat package; 100 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT317-2

4 BLOCK DIAGRAM

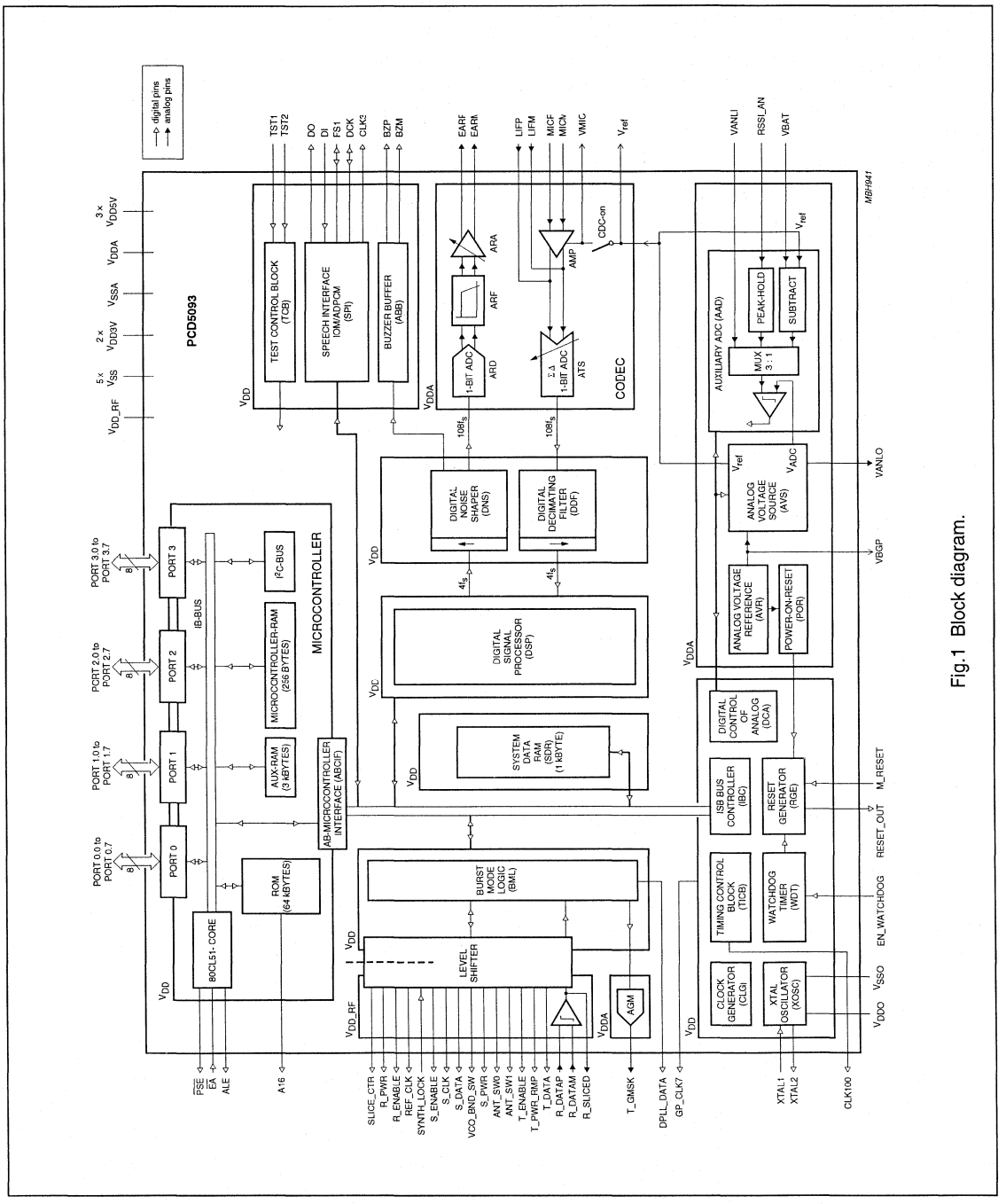


Fig.1 Block diagram.

5 PINNING INFORMATION

5.1 Pinning

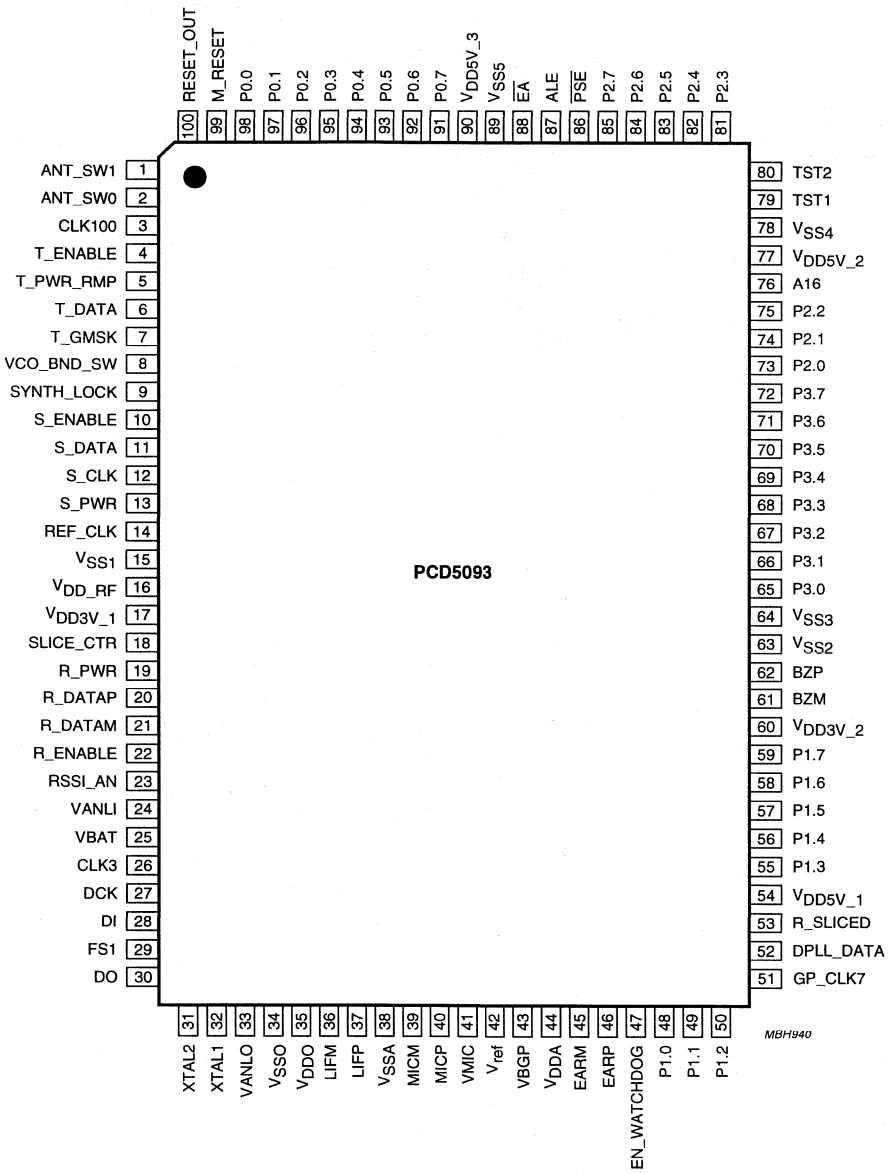


Fig.2 Pin configuration (QFP100).

5.2 Pin description

Table 1 QFP100 package

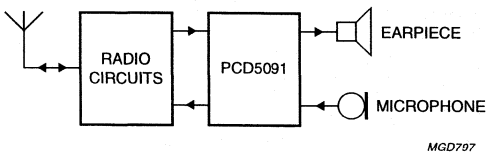
SYMBOL	PIN	I/O	STATE AFTER RESET	PIN TYPE	PIN DESCRIPTION
ANT_SW1	1	O	H	ISP2DRF3	antenna switch 1 output
ANT_SW0	2	O	H	ISP2DRF3	antenna switch 0 output
CLK100	3	O	H	ISP2DPES	100 Hz signal related to DECT frame timing output
T_ENABLE	4	O	H	ISP2DRF3	enable transmitter output
T_PWR_RMP	5	O	L	ISP2DRF3	switch transmitter power output
T_DATA	6	O	off	ISF2DRF3	unmodulated transmitter data output
T_GMSK	7	O	L	ANAIOD1	GMSK modulated transmitter data output
VCO_BND_SW	8	O	L	ISP2DRF3	VCO band switch output
SYNTH_LOCK	9	I	–	DIPP0RF3	synthesizer lock input
S_ENABLE	10	O	L	ISP2DRF3	synthesizer enable output
S_DATA	11	O	L	ISP2DRF3	serial synthesizer data output
S_CLK	12	O	L	ISP2DRF3	clock for serial synthesizer interface output
S_PWR	13	O	H	ISP2DRF3	switch synthesizer power output
REF_CLK	14	O	running	ISP4DRF3	13.824 MHz reference clock for synthesizer output
V_{SS1}	15	–	–	supply	negative supply voltage 1
V_{DD_RF}	16	–	–	supply	positive supply voltage for RF interface level shifters
V_{DD3V_1}	17	–	–	supply	positive supply voltage 1 (+3 V)
SLICE_CTR	18	O	L	ISP2DRF3	switch slicer time constant output
R_PWR	19	O	H	ISP2DRF3	switch receiver power output
R_DATAP	20	I	–	ANAIOD2	positive input for receiver data
R_DATAM	21	I	–	ANAIOD2	negative input for receiver data
R_ENABLE	22	O	H	ISP2DRF3	enable receiver output
RSSI_AN	23	I	–	ANAIOD1	analog input for RSSI measurement
VANLI	24	I	–	ANAIOD1	analog input to ADC
VBAT	25	I	–	ANAIOD1	analog input for battery voltage measurement
CLK3	26	O	L	ISP2DPES	3.456 MHz clock output for external ADPCM codec
DCK	27	I/O	input	ISF2DPES ISF2UPES	ADPCM output or IOM data clock input/output (ISF2UPES in PCD5090/xxx, PCA5097/xxx)
DI	28	I	–	DIPP0PES	ADPCM or IOM data input
FS1	29	I/O	input	ISF2DPES ISF2UPES	8 kHz framing input/output (ISF2UPES in PCD5090/xxx, PCA5097/xxx)
DO	30	O	off	ISI8DPES	ADPCM or IOM data output
XTAL2	31	O	running	ANAIOD1	crystal oscillator output
XTAL1	32	I	–	ANAIOD1	crystal oscillator input
VANLO	33	O	1.0 V	ANAIOD1	analog output from D/A converter

SYMBOL	PIN	I/O	STATE AFTER RESET	PIN TYPE	PIN DESCRIPTION
V_{SSO}	34	–	–	supply	negative supply voltage for the oscillator
V_{DDO}	35	–	–	supply	positive supply voltage for the oscillator
LIFM	36	I	0.7 V	ANAIOD1	negative input from line interface
LIFP	37	I	0.7 V	ANAIOD1	positive input from line interface
V_{SSA}	38	–	–	supply	negative supply voltage for analog circuits
MICM	39	I	0.7 V	ANAIOR1	negative input from microphone
MICP	40	I	0.7 V	ANAIOR1	positive input from microphone
VMIC	41	O	off	ANAIOD1	positive microphone supply voltage (+2 V)
V_{ref}	42	O	2.0 V	ANAIOD1	reference voltage (+2 V)
VBGP	43	O	1.25 V	ANAIOR1	bandgap output voltage (+1.25 V)
V_{DDA}	44	–	–	supply	positive supply voltage for analog circuits
EARM	45	O	1.4 V	ANAIOD1	negative output to earpiece
EARP	46	O	1.4 V	ANAIOD1	positive output to earpiece
EN_WATCHDOG	47	I	–	DIUP0PES	watchdog enable input
P1.0	48	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P1.1	49	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P1.2	50	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
GP_CLK7	51	O	L	ISP2DPES	general purpose 6.912 MHz output
DPLL_DATA	52	O	L	ISP2DPES	data after clock recovery network
R_SLICED	53	O	L	ISP2DPES	R_DATA comparator output
V_{DD5V_1}	54	–	–	supply	positive supply voltage 1 for the +5 V interface
P1.3	55	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P1.4	56	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P1.5	57	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P1.6	58	I/O	off	ISI8DPES	bidirectional 80C51 port pin
P1.7	59	I/O	off	ISI8DPES	bidirectional 80C51 port pin
V_{DD3V_2}	60	–	–	supply	positive supply voltage 2 (+3 V)
BZM	61	O	L	ANAIOD2	negative buzzer output
BZP	62	O	L	ANAIOD2	positive buzzer output
V_{SS2}	63	–	–	supply	negative supply voltage 2
V_{SS3}	64	–	–	supply	negative supply voltage 3
P3.0	65	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.1	66	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.2	67	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.3	68	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.4	69	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.5	70	I/O	H	ISQ2CPES	bidirectional 80C51 port pin

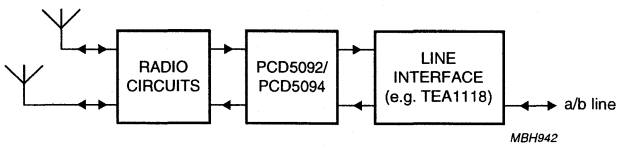
SYMBOL	PIN	I/O	STATE AFTER RESET	PIN TYPE	PIN DESCRIPTION
P3.6	71	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.7	72	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.0	73	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.1	74	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.2	75	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
A16	76	O	L	ISP4DPES	address bit 16 for 128 kbytes external program memory
V_{DD5V_2}	77	–	–	supply	positive supply voltage 2 for the +5 V interface
V_{SS4}	78	–	–	supply	negative supply voltage 4
TST1	79	I	–	DIDP0PES	test input 1
TST2	80	I	–	DIDP0PES	test input 2
P2.3	81	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.4	82	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.5	83	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.6	84	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.7	85	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
$\overline{PSE}$	86	O	H	ISQ2CPES	program store enable (80C51); active LOW
ALE	87	O	H	ISQ4CPES	address latch enable (80C51)
$\overline{EA}$	88	I	–	ISF2DPES	external access enable (80C51); active LOW
V_{SS5}	89	–	–	supply	negative supply voltage 5
V_{DD5V_3}	90	–	–	supply	positive supply voltage 3 for the +5 V interface
P0.7	91	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.6	92	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.5	93	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.4	94	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.3	95	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.2	96	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.1	97	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.0	98	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
M_RESET	99	I	–	DIDP0PES	master reset input (Schmitt trigger)
RESET_OUT	100	O	H	ISF2DPES	reset output

6 FUNCTIONAL DESCRIPTION

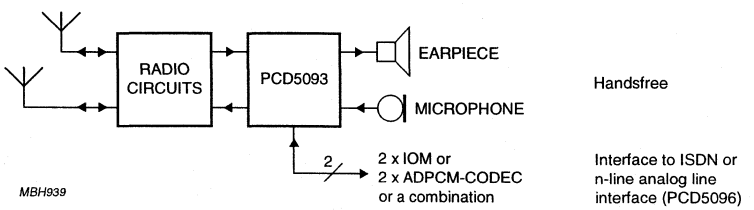
The PCD509x is a family of single-chip controllers, designed for use in Digital Enhanced Cordless Telecommunications systems (DECT). The family is designed for minimum component-count and minimum power consumption. All controllers include an embedded 80C51 microcontroller with on-chip memory and I²C-bus. The Philips DECT RF interface is implemented. The Burst Mode Logic (BML) performs the time-critical MAC layer functions for applications in DECT handsets and base stations. The ADPCM transcoding is in compliance with the CCITT recommendation G.721 and includes receive and transmit filters.



a. Handset.



b. Basestation with analog interface and echo cancellation; up to 6 portables can be handled.



c. Base(PCD5093) with digital interface and analog handset connected; up to 6 portables can be handled.

Fig.3 Block diagrams of DECT systems with PCX509x.

DECT baseband controller PCD5094

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1 FEATURES

- 80C51 ports P0, P1, P2 and P3 available for interfacing to display, keyboard, I²C-bus, interrupt sources and/or external memory. External program memory is addressable up to 128 kbytes
- +2.7 to 5 V port (P0 to P3) interface
- TDMA frame (de)multiplexing. Transmission or reception can be programmed for any slot
- Ciphering, scrambling, CRC checking/generation and protected B-fields
- Speech and data buffering space for six handsets
- Local call and B-field loop-back
- Two interrupt lines for BML and DSP to interrupt 80C51
- On-chip, three-channel time-multiplexed 8-bit Analog-to-Digital Converter (ADC) for RSSI measurement, one for battery voltage measurement and one channel available for other purposes
- On-chip 8-bit Digital-to-Analog Converter (DAC) for electronic potentiometer function
- Phase error measurement and phase error correction by hardware
- DACs and ADCs for dynamic earpiece and dynamic or electret microphone
- On-chip reference voltage
- On-chip supply for electret microphone
- Very low ohmic buzzer output
- Serial interface to external ADPCM CODEC (PCD5032) or 8 kHz u-law samples
- Speech switch for Digital Telephone Answering Machine (DTAM) connected to SPI interface
- IOM-2 interface (Siemens registered trademark)
- Serial interface to synthesizer for frequency programming
- Programmable polarity and timing of radio-control signals
- GMSK pulse shaper
- On-chip comparator for use as data-slicer
- Easy interfacing with radio circuits, operating at other supply voltage (RF supply pin with level shifter for RF signals)
- QFP100 package
- Power-on-reset
- Low power oscillator with integrated frequency adjustment
- Low supply voltage (2.7 to 3.6 V)
- CMOS technology.

1.1 DSP software features

- ADPCM encoding and decoding complying with G.721
- u-law encoding and decoding complying with G.711
- Echo cancellation and network echo suppressor
- Speech filters
- Programmable gain in speech paths
- Side tone and soft mute
- Ringer and tone (DTMF) generator
- Automatic gain control
- Telephone Answering Machine (TAM) switch
- TAM switch volume control
- Conference between a/b line and two handsets.

For each DSP software version a separate manual is available in which detailed information is provided on how parameters must be set. For further information please contact Philips Semiconductors.

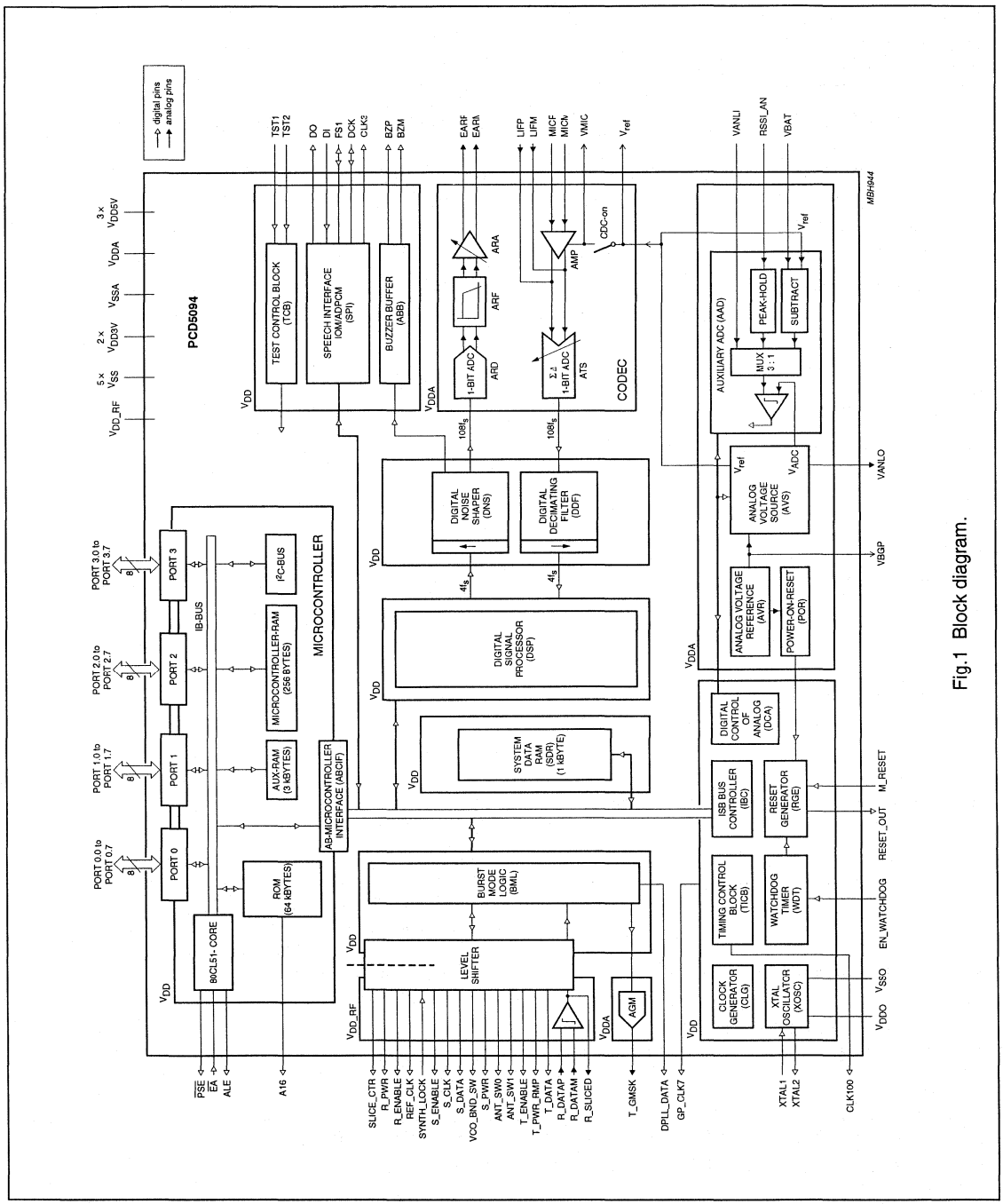
2 GENERAL DESCRIPTION

The PCD5094 is designed for GAP-compliant basestations offering conference call between the a/b line and two handsets and answering machine switch. It has an embedded 80C51 microcontroller with twice the performance of the classic architecture, 64 kbytes of PROM program memory and 3 kbytes of data memory on chip. In addition there is 1 kbyte of on-chip data memory that is shared with on-chip Burst Mode Logic (BML) and DSP, the System Data RAM (SDR).

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD5094H	QFP100	plastic quad flat package; 100 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT317-2

4 BLOCK DIAGRAM



5 PINNING INFORMATION

5.1 Pinning

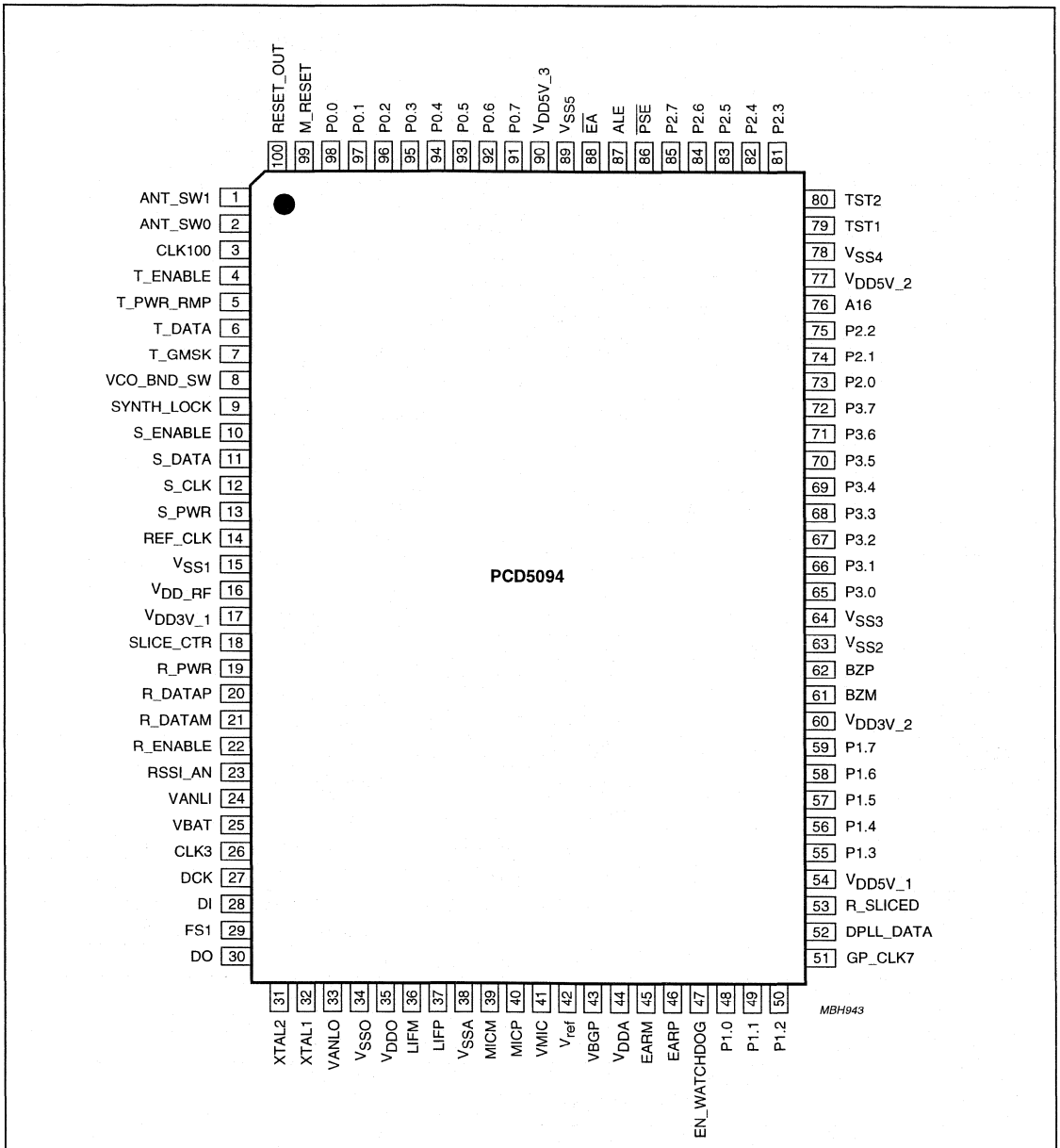


Fig.2 Pin configuration (QFP100).

5.2 Pin description

Table 1 QFP100 package

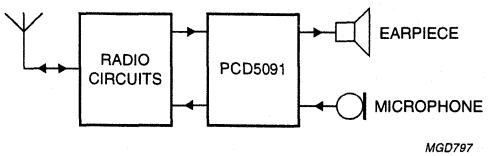
SYMBOL	PIN	I/O	STATE AFTER RESET	PIN TYPE	PIN DESCRIPTION
ANT_SW1	1	O	H	ISP2DRF3	antenna switch 1 output
ANT_SW0	2	O	H	ISP2DRF3	antenna switch 0 output
CLK100	3	O	H	ISP2DPES	100 Hz signal related to DECT frame timing output
T_ENABLE	4	O	H	ISP2DRF3	enable transmitter output
T_PWR_RMP	5	O	L	ISP2DRF3	switch transmitter power output
T_DATA	6	O	off	ISF2DRF3	unmodulated transmitter data output
T_GMSK	7	O	L	ANAIOD1	GMSK modulated transmitter data output
VCO_BND_SW	8	O	L	ISP2DRF3	VCO band switch output
SYNTH_LOCK	9	I	–	DIPP0RF3	synthesizer lock input
S_ENABLE	10	O	L	ISP2DRF3	synthesizer enable output
S_DATA	11	O	L	ISP2DRF3	serial synthesizer data output
S_CLK	12	O	L	ISP2DRF3	clock for serial synthesizer interface output
S_PWR	13	O	H	ISP2DRF3	switch synthesizer power output
REF_CLK	14	O	running	ISP4DRF3	13.824 MHz reference clock for synthesizer output
V_{SS1}	15	–	–	supply	negative supply voltage 1
V_{DD_RF}	16	–	–	supply	positive supply voltage for RF interface level shifters
V_{DD3V_1}	17	–	–	supply	positive supply voltage 1 (+3 V)
SLICE_CTR	18	O	L	ISP2DRF3	switch slicer time constant output
R_PWR	19	O	H	ISP2DRF3	switch receiver power output
R_DATAP	20	I	–	ANAIOD2	positive input for receiver data
R_DATAM	21	I	–	ANAIOD2	negative input for receiver data
R_ENABLE	22	O	H	ISP2DRF3	enable receiver output
RSSI_AN	23	I	–	ANAIOD1	analog input for RSSI measurement
VANLI	24	I	–	ANAIOD1	analog input to ADC
VBAT	25	I	–	ANAIOD1	analog input for battery voltage measurement
CLK3	26	O	L	ISP2DPES	3.456 MHz clock output for external ADPCM codec
DCK	27	I/O	input	ISF2DPES ISF2UPES	ADPCM output or IOM data clock input/output (ISF2UPES in PCD5090/xxx, PCA5097/xxx)
DI	28	I	–	DIPP0PES	ADPCM or IOM data input
FS1	29	I/O	input	ISF2DPES ISF2UPES	8 kHz framing input/output (ISF2UPES in PCD5090/xxx, PCA5097/xxx)
DO	30	O	off	ISI8DPES	ADPCM or IOM data output
XTAL2	31	O	running	ANAIOD1	crystal oscillator output
XTAL1	32	I	–	ANAIOD1	crystal oscillator input
VANLO	33	O	1.0 V	ANAIOD1	analog output from D/A converter
V_{SSO}	34	–	–	supply	negative supply voltage for the oscillator
V_{DDO}	35	–	–	supply	positive supply voltage for the oscillator

SYMBOL	PIN	I/O	STATE AFTER RESET	PIN TYPE	PIN DESCRIPTION
LIFM	36	I	0.7 V	ANAIOD1	negative input from line interface
LIFP	37	I	0.7 V	ANAIOD1	positive input from line interface
V_{SSA}	38	–	–	supply	negative supply voltage for analog circuits
MICM	39	I	0.7 V	ANAIOR1	negative input from microphone
MICP	40	I	0.7 V	ANAIOR1	positive input from microphone
VMIC	41	O	off	ANAIOD1	positive microphone supply voltage (+2 V)
V_{ref}	42	O	2.0 V	ANAIOD1	reference voltage (+2 V)
VBGP	43	O	1.25 V	ANAIOR1	bandgap output voltage (+1.25 V)
V_{DDA}	44	–	–	supply	positive supply voltage for analog circuits
EARM	45	O	1.4 V	ANAIOD1	negative output to earpiece
EARP	46	O	1.4 V	ANAIOD1	positive output to earpiece
EN_WATCHDOG	47	I	–	DIUP0PES	watchdog enable input
P1.0	48	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P1.1	49	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P1.2	50	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
GP_CLK7	51	O	L	ISP2DPES	general purpose 6.912 MHz output
DPLL_DATA	52	O	L	ISP2DPES	data after clock recovery network
R_SLICED	53	O	L	ISP2DPES	R_DATA comparator output
V_{DD5V_1}	54	–	–	supply	positive supply voltage 1 for the +5 V interface
P1.3	55	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P1.4	56	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P1.5	57	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P1.6	58	I/O	off	ISI8DPES	bidirectional 80C51 port pin
P1.7	59	I/O	off	ISI8DPES	bidirectional 80C51 port pin
V_{DD3V_2}	60	–	–	supply	positive supply voltage 2 (+3 V)
BZM	61	O	L	ANAIOD2	negative buzzer output
BZP	62	O	L	ANAIOD2	positive buzzer output
V_{SS2}	63	–	–	supply	negative supply voltage 2
V_{SS3}	64	–	–	supply	negative supply voltage 3
P3.0	65	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.1	66	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.2	67	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.3	68	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.4	69	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.5	70	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.6	71	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.7	72	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.0	73	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.1	74	I/O	H	ISQ2CPES	bidirectional 80C51 port pin

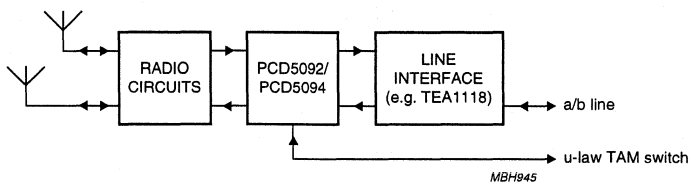
SYMBOL	PIN	I/O	STATE AFTER RESET	PIN TYPE	PIN DESCRIPTION
P2.2	75	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
A16	76	O	L	ISP4DPES	address bit 16 for 128 kbytes external program memory
V_{DD5V_2}	77	–	–	supply	positive supply voltage 2 for the +5 V interface
V_{SS4}	78	–	–	supply	negative supply voltage 4
TST1	79	I	–	DIDP0PES	test input 1
TST2	80	I	–	DIDP0PES	test input 2
P2.3	81	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.4	82	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.5	83	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.6	84	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.7	85	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
$\overline{PSE}$	86	O	H	ISQ2CPES	program store enable (80C51); active LOW
ALE	87	O	H	ISQ4CPES	address latch enable (80C51)
$\overline{EA}$	88	I	–	ISF2DPES	external access enable (80C51); active LOW
V_{SS5}	89	–	–	supply	negative supply voltage 5
V_{DD5V_3}	90	–	–	supply	positive supply voltage 3 for the +5 V interface
P0.7	91	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.6	92	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.5	93	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.4	94	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.3	95	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.2	96	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.1	97	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.0	98	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
M_RESET	99	I	–	DIDP0PES	master reset input (Schmitt trigger)
RESET_OUT	100	O	H	ISF2DPES	reset output

6 FUNCTIONAL DESCRIPTION

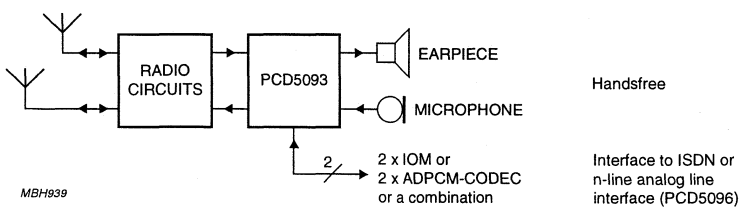
The PCD509x is a family of single-chip controllers, designed for use in Digital Enhanced Cordless Telecommunications systems (DECT). The family is designed for minimum component-count and minimum power consumption. All controllers include an embedded 80C51 microcontroller with on-chip memory and I²C-bus. The Philips DECT RF interface is implemented. The Burst Mode Logic (BML) performs the time-critical MAC layer functions for applications in DECT handsets and base stations. The ADPCM transcoding is in compliance with the CCITT recommendation G.721 and includes receive and transmit filters.



a. Handset.



b. Basestation (PCD5094) with analog interface and echo cancellation; up to 6 portables can be handled.



c. Base with digital interface and analog corded handset connected; up to 6 portables can be handled.

Fig.3 Block diagrams of DECT systems with PCX509x.

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1 FEATURES

- 80C51 ports P0, P1, P2 and P3 available for interfacing to display, keyboard, I²C-bus, interrupt sources and/or external memory. Integrated 64 kbyte ROM, 3 kbytes of data memory and 1kbyte System Data RAM. External program memory is addressable up to 128 kbytes
- +2.7 to 5 V port (P0 to P3) interface
- TDMA frame (de)multiplexing, transmission or reception can be programmed for any slot
- Ciphering, scrambling, CRC checking/generation and protected B-fields
- Speech and data buffering space for six handsets
- Local call and B-field loop-back
- Two interrupt lines for BML and DSP to interrupt 80C51
- On-chip, three channel time-multiplexed 8-bit Analog-to-Digital Converter (ADC) for RSSI measurement, one for battery voltage measurement and one channel available for other purposes
- On-chip 8-bit Digital-to-Analog Converter (DAC) for electronic potentiometer function
- Phase error measurement and phase error correction by hardware
- DACs and ADCs for dynamic earpiece and dynamic or electret microphone
- On-chip reference voltage
- On-chip supply for electret microphone
- Very low ohmic buzzer output
- Serial interface to external ADPCM CODEC (PCD5032) or 8 kHz u-law samples
- Speech switch for Digital Telephone Answering Machine (DTAM) connected to SPI interface
- IOM®-2 interface (Siemens registered trademark)
- Serial interface to synthesizer for frequency programming
- Programmable polarity and timing of radio-control signals
- GMSK pulse shaper
- On-chip comparator for use as data-slicer
- Easy interfacing with radio circuits, operating at other supply voltage (RF supply pin with level shifter for RF signals)
- Low-power oscillator with integrated frequency adjustment
- QFP100 package
- Power-on-reset
- Programmable power-down modes
- Low supply voltage (2.7 to 3.6 V)
- CMOS technology.

1.1 DSP software features

- 3x ADPCM transcoding complying with G.726
- A-Law encoding and decoding complying with G.711
- 4 Channel bidirectional ADPCM interface to the IOM®-2 and radio interface
- Programmable channel switching and buffers
- Channel mute.

For each DSP software version a separate manual is available in which detailed information is provided on how parameters must be set. For further information please contact Philips Semiconductors.

2 GENERAL DESCRIPTION

The PCD5095 is designed for GAP-compliant business systems, PABX and WLL. Two modes can be selected: three channel ADPCM CODEC with conversion of ADPCM samples to linear PCM format and vice versa, the second mode copies four ADPCM samples into two IOM data buffers and vice versa. In both modes the DSP controls the bidirectional data flow from the radio interface and the IOM®-2 interface. The 80C51 controls the DECT protocol and the IOM®-2 interface. The performance of the embedded 80C51 microcontroller is twice the performance of the classic architecture. The PCD5095 has 64 kbytes of PROM program memory and 3 kbytes of data memory on-chip. In addition there is 1 kbyte of on-chip data memory that is shared with the Burst Mode Logic (BML), the DSP and the System Data RAM (SDR).

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD5095H	QFP100	plastic quad flat package; 100 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT317-2

4 BLOCK DIAGRAM

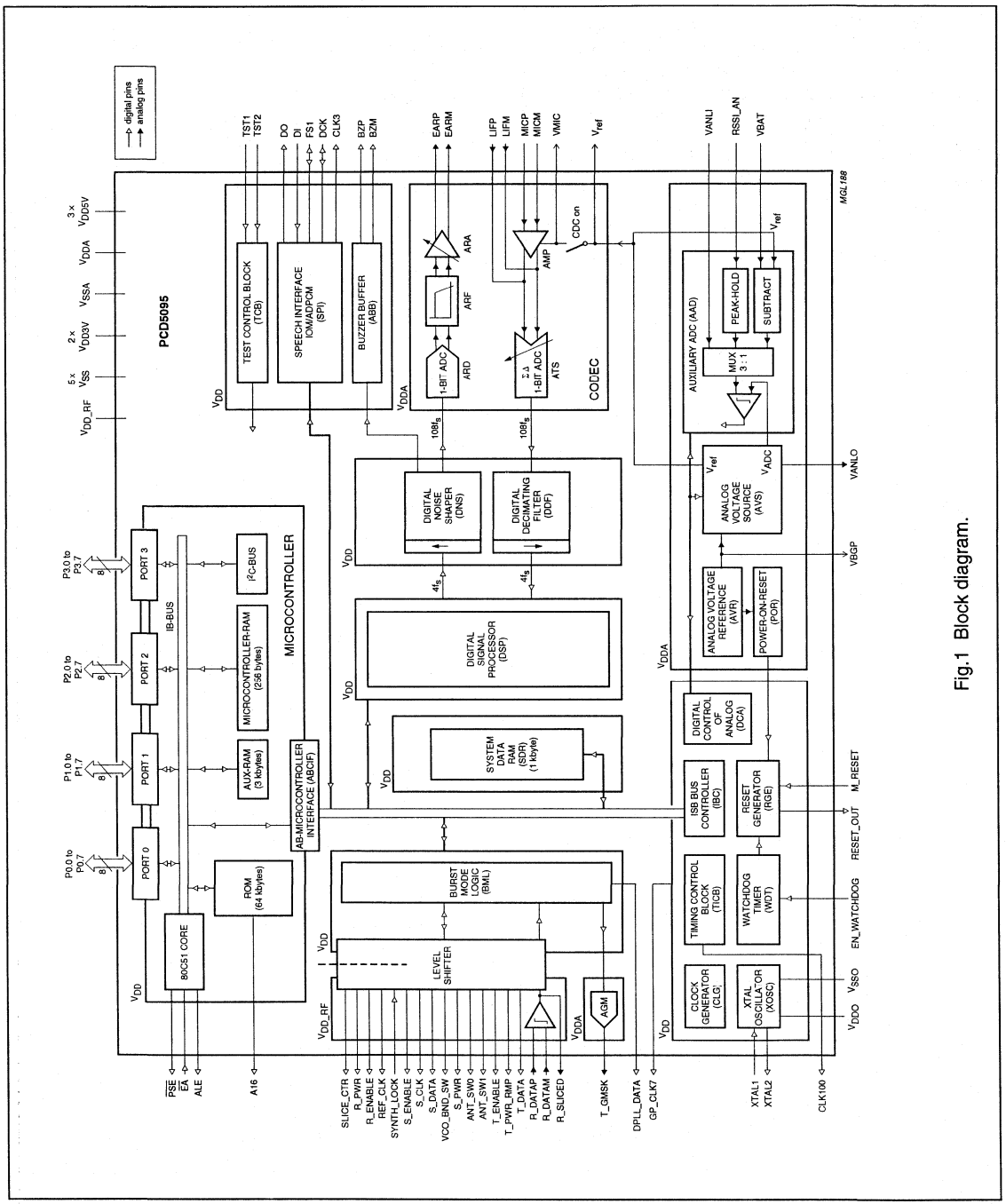

Fig.1 Block diagram.

5 PINNING INFORMATION

5.1 Pinning

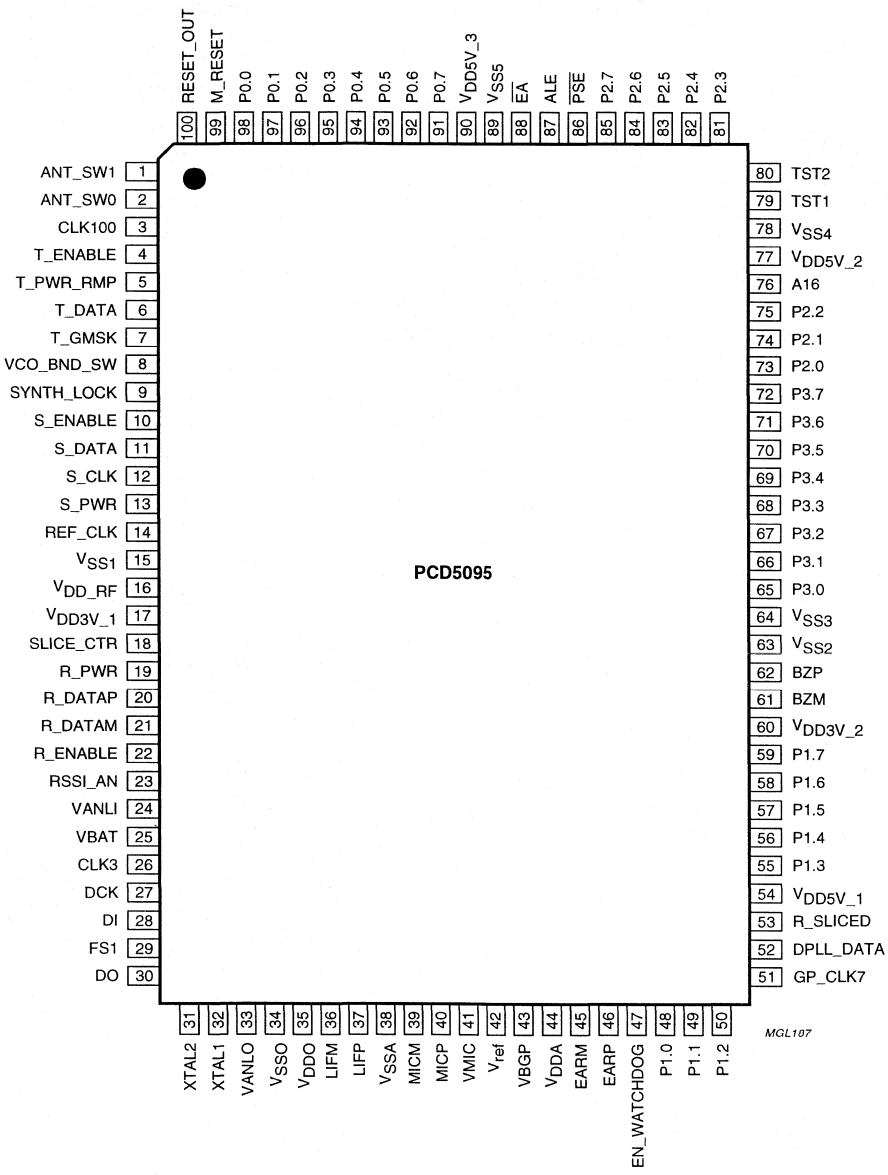

Fig.2 Pin configuration (QFP100).

5.2 Pin description

Table 1 QFP100 package

SYMBOL	PIN	I/O	STATE AFTER RESET	PIN TYPE	PIN DESCRIPTION
ANT_SW1	1	O	H	ISP2DRF3	antenna switch 1 output
ANT_SW0	2	O	H	ISP2DRF3	antenna switch 0 output
CLK100	3	O	H	ISP2DPES	100 Hz signal related to DECT frame timing output
T_ENABLE	4	O	H	ISP2DRF3	enable transmitter output
T_PWR_RMP	5	O	L	ISP2DRF3	switch transmitter power output
T_DATA	6	O	off	ISF2DRF3	unmodulated transmitter data output
T_GMSK	7	O	L	ANAIOD1	GMSK modulated transmitter data output
VCO_BND_SW	8	O	L	ISP2DRF3	VCO band switch output
SYNTH_LOCK	9	I	–	DIPP0RF3	synthesizer lock input
S_ENABLE	10	O	L	ISP2DRF3	synthesizer enable output
S_DATA	11	O	L	ISP2DRF3	serial synthesizer data output
S_CLK	12	O	L	ISP2DRF3	clock for serial synthesizer interface output
S_PWR	13	O	H	ISP2DRF3	switch synthesizer power output
REF_CLK	14	O	running	ISP4DRF3	13.824 MHz reference clock for synthesizer output
V_{SS1}	15	–	–	supply	negative supply voltage 1
V_{DD_RF}	16	–	–	supply	positive supply voltage for RF interface level shifters
V_{DD3V_1}	17	–	–	supply	positive supply voltage 1 (+3 V)
SLICE_CTR	18	O	L	ISP2DRF3	switch slicer time constant output
R_PWR	19	O	H	ISP2DRF3	switch receiver power output
R_DATAP	20	I	–	ANAIOD2	positive input for receiver data
R_DATAM	21	I	–	ANAIOD2	negative input for receiver data
R_ENABLE	22	O	H	ISP2DRF3	enable receiver output
RSSI_AN	23	I	–	ANAIOD1	analog input for RSSI measurement
VANLI	24	I	–	ANAIOD1	analog input to ADC
VBAT	25	I	–	ANAIOD1	analog input for battery voltage measurement
CLK3	26	O	L	ISP2DPES	3.456 MHz clock output for external ADPCM codec
DCK	27	I/O	input	ISF2DPES ISF2UPES	ADPCM output or IOM®-2 data clock input/output (ISF2UPES in PCD5090/xxx, PCA5097/xxx)
DI	28	I	–	DIPP0PES	ADPCM or IOM®-2 data input
FS1	29	I/O	input	ISF2DPES ISF2UPES	8 kHz framing input/output (ISF2UPES in PCD5090/xxx, PCA5097/xxx)
DO	30	O	off	ISI8DPES	ADPCM or IOM®-2 data output
XTAL2	31	O	running	ANAIOD1	crystal oscillator output
XTAL1	32	I	–	ANAIOD1	crystal oscillator input
VANLO	33	O	1.0 V	ANAIOD1	analog output from DAC
V_{SSO}	34	–	–	supply	negative supply voltage for the oscillator
V_{DDO}	35	–	–	supply	positive supply voltage for the oscillator

SYMBOL	PIN	I/O	STATE AFTER RESET	PIN TYPE	PIN DESCRIPTION
LIFM	36	I	0.7 V	ANAIOD1	negative input from line interface
LIFP	37	I	0.7 V	ANAIOD1	positive input from line interface
V_{SSA}	38	–	–	supply	negative supply voltage for analog circuits
MICM	39	I	0.7 V	ANAIOR1	negative input from microphone
MICP	40	I	0.7 V	ANAIOR1	positive input from microphone
VMIC	41	O	off	ANAIOD1	positive microphone supply voltage (+2 V)
V_{ref}	42	O	2.0 V	ANAIOD1	reference voltage (+2 V)
VBGP	43	O	1.25 V	ANAIOR1	bandgap output voltage (+1.25 V)
V_{DDA}	44	–	–	supply	positive supply voltage for analog circuits
EARM	45	O	1.4 V	ANAIOD1	negative output to earpiece
EARP	46	O	1.4 V	ANAIOD1	positive output to earpiece
EN_WATCHDOG	47	I	–	DIUP0PES	Watchdog Timer enable input
P1.0	48	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P1.1	49	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P1.2	50	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
GP_CLK7	51	O	L	ISP2DPES	general purpose 6.912 MHz output
DPLL_DATA	52	O	L	ISP2DPES	data after clock recovery network
R_SLICED	53	O	L	ISP2DPES	R_DATA comparator output
V_{DD5V_1}	54	–	–	supply	positive supply voltage 1 for the +5 V interface
P1.3	55	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P1.4	56	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P1.5	57	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P1.6	58	I/O	off	ISI8DPES	bidirectional 80C51 port pin
P1.7	59	I/O	off	ISI8DPES	bidirectional 80C51 port pin
V_{DD3V_2}	60	–	–	supply	positive supply voltage 2 (+3 V)
BZM	61	O	L	ANAIOD2	negative buzzer output
BZP	62	O	L	ANAIOD2	positive buzzer output
V_{SS2}	63	–	–	supply	negative supply voltage 2
V_{SS3}	64	–	–	supply	negative supply voltage 3
P3.0	65	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.1	66	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.2	67	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.3	68	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.4	69	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.5	70	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.6	71	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.7	72	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.0	73	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.1	74	I/O	H	ISQ2CPES	bidirectional 80C51 port pin

SYMBOL	PIN	I/O	STATE AFTER RESET	PIN TYPE	PIN DESCRIPTION
P2.2	75	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
A16	76	O	L	ISP4DPES	address bit 16 for 128 kbytes external program memory
V_{DD5V_2}	77	–	–	supply	positive supply voltage 2 for the +5 V interface
V_{SS4}	78	–	–	supply	negative supply voltage 4
TST1	79	I	–	DIDP0PES	test input 1
TST2	80	I	–	DIDP0PES	test input 2
P2.3	81	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.4	82	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.5	83	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.6	84	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.7	85	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
$\overline{PSE}$	86	O	H	ISQ2CPES	program store enable (80C51); active LOW
ALE	87	O	H	ISQ4CPES	address latch enable (80C51)
$\overline{EA}$	88	I	–	ISF2DPES	external access enable (80C51); active LOW
V_{SS5}	89	–	–	supply	negative supply voltage 5
V_{DD5V_3}	90	–	–	supply	positive supply voltage 3 for the +5 V interface
P0.7	91	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.6	92	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.5	93	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.4	94	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.3	95	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.2	96	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.1	97	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.0	98	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
M_RESET	99	I	–	DIDP0PES	master reset input (Schmitt trigger)
RESET_OUT	100	O	H	ISF2DPES	reset output

6 FUNCTIONAL DESCRIPTION

The PCD509x is a family of single-chip controllers, designed for use in Digital Enhanced Cordless Telecommunications systems (DECT). The family is designed for minimum component-count and minimum power consumption. All controllers include an embedded 80C51 microcontroller with on-chip memory and I^2C-bus interface. The Philips DECT RF interface is implemented. The Burst Mode Logic (BML) performs the time-critical MAC layer functions for applications in DECT handsets and base stations. The ADPCM transcoding is in compliance with the CCITT recommendation G.721 and includes receive and transmit filters.

The PCD5095 is designed for business systems, PABX and WLL. Two modes can be selected: bidirectional conversion of three ADPCM channels based on linear PCM format, the second mode copies four ADPCM samples, without data processing, into two IOM®-2 data buffers and vice versa. In both modes the DSP controls the bidirectional data flow from the radio interface and the IOM®-2 interface. The 80C51 controls the DECT protocol and the IOM®-2 interface.

The data flow between radio, DSP and IOM®-2 is described in the *"PCD5095 DSP user manual"*. Basically the System Data RAM (SDR), the shared memory with inbound and outbound speech buffers, is the interface to the DSP and to the radio. Depending on the selected mode the DSP processes the data stored in the SDR. The speech buffers are 40 bytes long and each buffer can hold 80 ADPCM-coded speech samples.

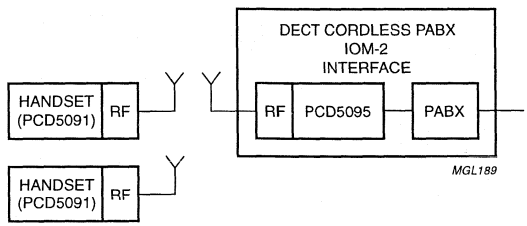

Fig.3 PCD5095 for PABX.

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1 FEATURES

- Applications in digital terminal equipment featuring line interface and/or voice functions
- Digital signal processor performing echo cancellation, codec functions and dial tone detection
- Two independent receive and transmit channels
- Independent programmable gain for all analog inputs and outputs
- Programmable filter correction functions
- Flexible configuration of all functions
- IOM-2 serial data interface (slave mode only)
- Serial data interface to DTAM speech compression ICs
- 400 kHz I²C-bus slave interface (four I²C-bus subaddresses)
- Codec compatible with G.714 CCITT specification
- PCM A-Law/u-Law (G.711 CCITT) and 16-bit linear data
- Dual differential inputs and outputs performing the following functions:
  - Line interface connection
  - Loudspeaker, speaker phone (hands-free)
  - Earpiece, microphone (handset)
- Peripheral interface: two I/O pins
- Separate ringer function
- Tone and ringer generator
- Conference call
- QFP44 package
- Low voltage (2.7 to 3.6 V)
- Low power consumption.

2 GENERAL DESCRIPTION

The universal codec combines two high resolution bidirectional analog channels with a DSP in a single chip. Besides the analog interfaces the PCD5096 includes two digital interfaces: an I²C-bus interface allowing an external microcontroller to program the chip, and a 4-wire serial interface compatible with IOM-2 and with DTAM speech compression ICs. This programmable serial interface offers up to 14 channels and is capable of handling 8-bit (A-law) or 16-bit (linear PCM) data packages, or any combination of them. It opens the scope for a wide application area, for example in combination with the PCD5093H DECT baseband chip for digital cordless business applications.

Several PCD5096s can be connected together for small switching systems (PABX) offering a combination of corded and cordless functionality. Besides the basic functions like echo cancellation for two channels the on-chip DSP provides all necessary functions such as conference call and DTMF.

3 APPLICATIONS

The PCD5096 is designed for the telecommunications market and is targeting small business and residential systems offering a two-line interface or a one-line interface combined with hands-free speaker phone. Specific applications are detailed in Chapter 12.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD5096H	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2

5 BLOCK DIAGRAM

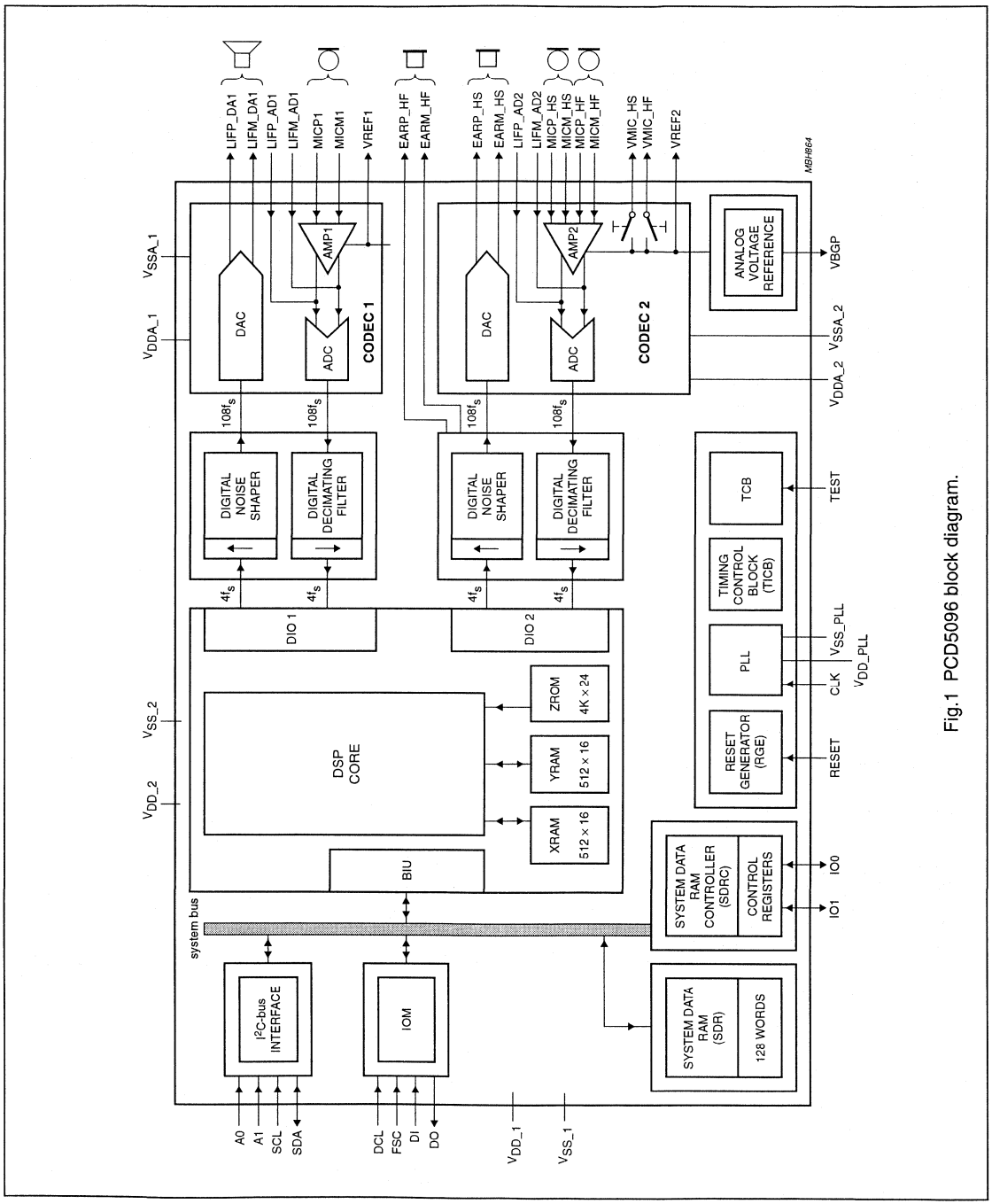


Fig.1 PCD5096 block diagram.

6 PINNING INFORMATION

6.1 Pin description

Table 1 QFP44 package

SYMBOL	PIN	I/O[1]	DESCRIPTION
IO0	1	I/O	programmable I/O pin 0 (Schmitt trigger input, pull-up output)
IO1	2	I/O	programmable I/O pin 1 (Schmitt trigger input, pull-up output)
CLK	3	I	clock input
V_{DD_PLL}	4	P	3 V analog supply for PLL
V_{SS_PLL}	5	P	analog ground supply for PLL
V_{SS_1}	6	P	peripheral ground supply
V_{DD_1}	7	P	3 to 5 V peripheral supply
SCL	8	I	I²C-bus clock signal input (Schmitt trigger)
SDA	9	I/O	I²C-bus data signal
A0	10	I	I²C-bus subaddress
A1	11	I	I²C-bus subaddress
LIFM_DA1	12	O	negative analog output from Codec 1 to line interface
LIFP_DA1	13	O	positive analog output from Codec 1 to line interface
V_{DDA_1}	14	P	3 V analog supply for Codec 1
LIFM_AD1	15	I	negative analog input to Codec 1 from line interface
LIFP_AD1	16	I	positive analog input to Codec 1 from line interface
V_{SSA_1}	17	P	analog ground supply for Codec 1
MICM1	18	I	negative analog input to Codec 1 from microphone
MICP1	19	I	positive analog input to Codec 1 from microphone
VREF1	20	O	Codec 1 analog reference voltage
VBGP	21	O	bandgap analog output voltage
VREF2	22	O	Codec 2 analog reference voltage
VMIC_HS	23	O	positive analog supply voltage from Codec 2 for handset microphone
MICP_HS	24	I	positive analog input to Codec 2 from handset microphone
MICM_HS	25	I	negative analog input to Codec 2 from handset microphone
VMIC_HF	26	O	positive analog supply voltage from Codec 2 for hands-free microphone
MICP_HF	27	I	positive analog input to Codec 2 from hands-free microphone
MICM_HF	28	I	negative analog input to Codec 2 from hands-free microphone
V_{SSA_2}	29	P	analog ground supply for Codec 2
LIFP_AD2	30	I	positive analog input to Codec 2 from line interface
LIFM_AD2	31	I	negative analog input to Codec 2 from line interface
V_{DDA_2}	32	P	3 V analog supply for Codec 2
EARP_HS	33	O	positive analog output from Codec 2 to handset earpiece
EARM_HS	34	O	negative analog output from Codec 2 to handset earpiece
EARP_HF	35	O	positive output to hands-free earpiece
EARM_HF	36	O	negative output to hands-free earpiece
TEST	37	I	test input; pull-down

SYMBOL	PIN	I/O[1]	DESCRIPTION
RESET	38	I	reset input (Schmitt trigger)
V_{SS_2}	39	P	digital core ground supply
V_{DD_2}	40	P	3 V digital core supply
DI	41	I	IOM-2 interface serial data input
DO	42	O	IOM-2 interface serial data output (open-drain)
FSC	43	I/O	IOM-2 interface 8 kHz frame synchronization clock (Schmitt trigger input); note 2
DCL	44	I/O	IOM-2 interface data clock (Schmitt trigger input); note 2

Note

1. 'P' denotes power line.
2. FSC and DCL are outputs only in test modes.

6.2 Pinning

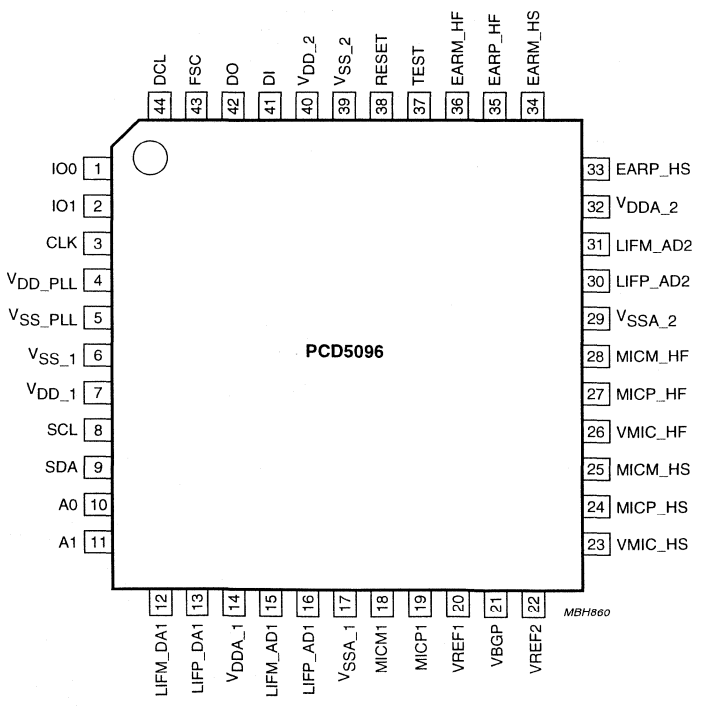


Fig.2 Pin configuration.

6.3 Supply concept

The universal codec is designed for 3 V systems with a voltage range of 2.7 to 3.6 V. To allow connection to 5 V systems the digital I/Os include level shifters. The core must run on 3.3 V and the peripheral supply on 5 V.

The five power supplies are listed in Table 2. Codec 1 and Codec 2 have their own power supplies: V_{DDA_1} and V_{DDA_2} respectively. V_{DD_PLL} is the power supply dedicated to the PLL. The digital core and the memories are powered by V_{DD_2} and the digital peripherals by V_{DD_1}. All digital pins (EARP_HF, EARM_HF, TEST, RESET, DI, DO, FSC, DCL, IO0, IO1, CLK, SCL, SDA, A0 and A1) have internal level shifters, allowing the chip to be used in a 3 to 5 V environment.

Table 2 PCD5096 power supply

SUPPLY PAIR	ASSOCIATED DEVICE
V_{DD_1} and V_{SS_1}	3 to 5 V peripheral supply
V_{DD_2} and V_{SS_2}	3 V digital core supply
V_{DD_PLL} and V_{SS_PLL}	3 V PLL supply
V_{DDA_1} and V_{SSA_1}	3 V Codec 1 supply
V_{DDA_2} and V_{SSA_2}	3 V Codec 2 supply

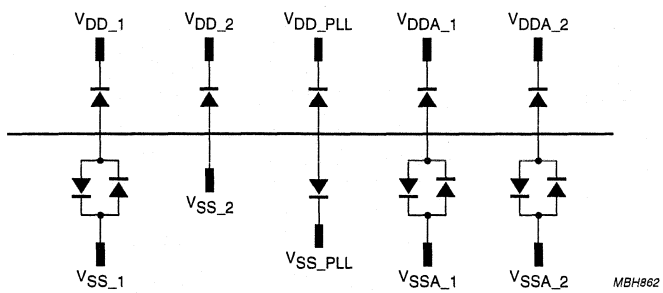


Fig.3 PCx5096 supply rails with protection diodes.

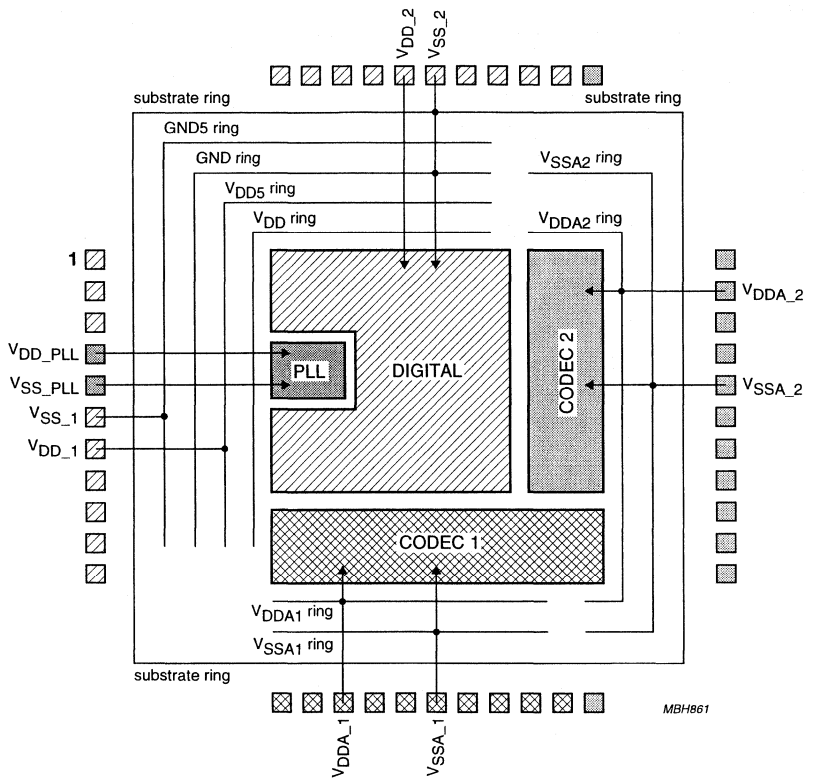


Fig.4 PCD5096 power supply.

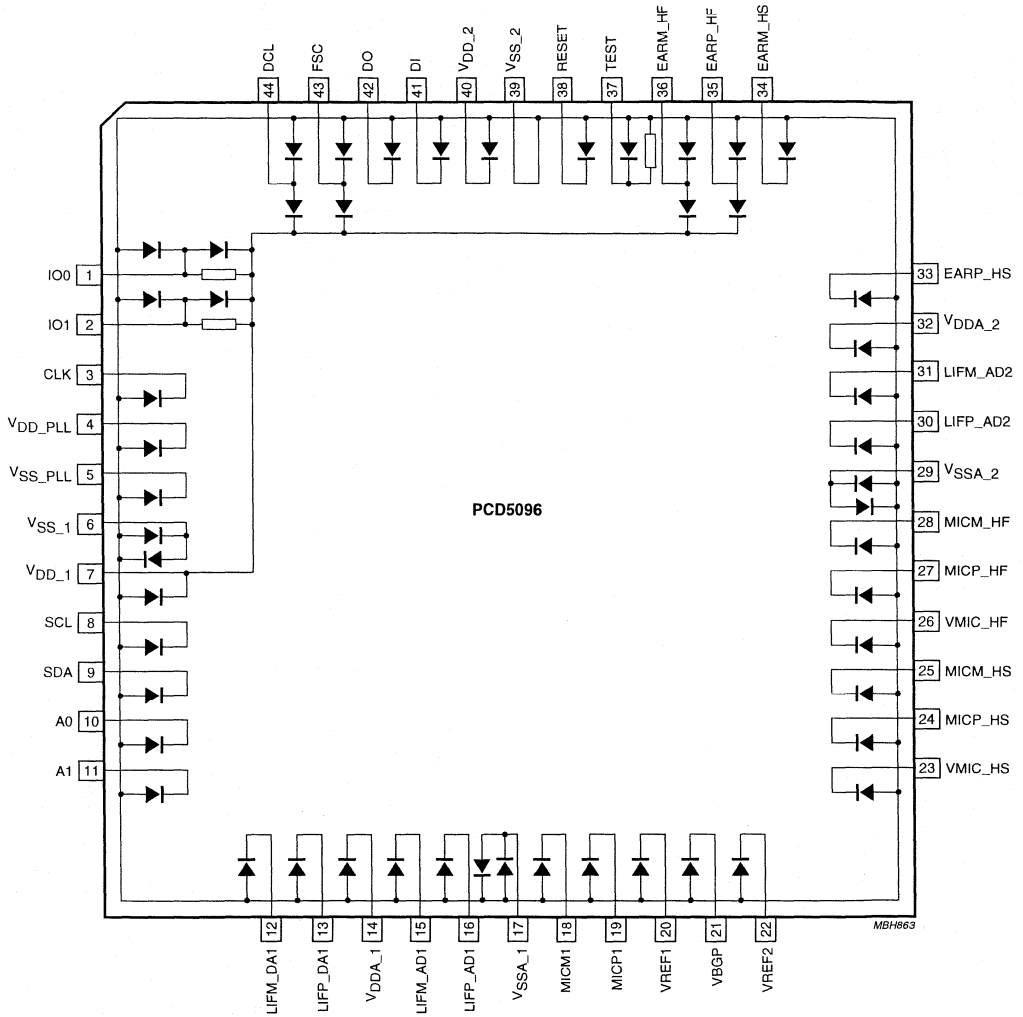


Fig.5 Open/short diagram.

7 FUNCTIONAL DESCRIPTION

7.1 General

The PCD5096 is a universal codec designed for use in digital terminal equipment. It connects two PSTN lines to a digital interface (IOM-2), thus covering a wide application area. Echo cancellation is performed on both PSTN lines by an on-chip DSP. Hands-free speaker phone functionality is also provided by sacrificing one PSTN line connection. The chip is controlled by an external microcontroller via a high bit rate I²C-bus interface.

Figure 1 shows the block diagram of the PCD5096. The different functional blocks operate more or less autonomously and communicate with each other via the System Data RAM (SDR). Each block has access to the SDR via an internal system bus. Access to this bus is controlled by the System Data RAM Controller (SDRC).

The IOM block connects to a n × 256 kbits/s digital interface (IOM-2 interface) and also supports interfacing to DTAM speech compression ICs. The IOM block stores and fetches speech data into/from the SDR using internal addressing logic.

The DSP block is the link between the data in the SDR stored/fetched by the IOM block on one hand, and the analog front-end on the other hand. The basic functions of the DSP are data filtering, local echo cancelling, network echo suppressing, A-law coding and decoding according to the G.711 CCITT recommendations, dial tone detection and generation, DTMF generation, side-tone, automatic volume control, automatic gain control, double talk detection and conference call.

Data processed by the DSP goes to and comes from two independent codecs interfacing to the PSTN lines. The codecs comply with the G.714 specifications and handle the PCM coding and decoding of speech signals. They perform the analog and high speed digital speech processing functions: analog bitstream A/D and D/A conversion, analog filtering and amplification, digital decimation filtering and noise shaping. Both codecs should be connected to a local line or to a PSTN line, but one codec also supports a corded handset and hands-free speaker and microphone.

The control of the entire chip is done via the I²C-bus block by writing to the SDR or to special control registers. In this way the DSP and the IOM operation modes can be set, as well as some analog parameters in the two codecs.

The PCD5096 has two general purpose programmable I/O pins controlled by two special registers (direction and state). These two special registers are accessible via the I²C-bus interface or by the on-chip DSP. A typical application is the generation of interrupts by the DSP, indicating that DTMF tones were detected.

The timing for the whole chip is generated in the Timing Control Block (TICB). The system clock (20.736 MHz) is delivered by a PLL which triples the input clock frequency.

7.2 Clocking

The universal codec is designed to operate in a digital cordless telephone system, for example together with a PCD5093 baseband controller. To save the expense of having to provide each universal codec with a separate crystal, a common clock is provided by the master controller. In the current generation of the Philips DECT baseband controllers this clock is GP_CLK7, a 6.912 MHz clock output derived from the 13.824 MHz crystal oscillator. GP_CLK7 must therefore be used as the input clock for the universal codec. GP_CLK7 is enabled during a reset of the PCD5093 and when either the Burst Mode Logic or codec are turned on (see PCD5093 data sheet).

In order to meet the DSP processing requirements for the various applications an on-chip PLL is used to generate a system clock which is triple the input clock frequency (20.736 MHz).

7.3 Reset and power-down strategy

The universal codec must be reset at power-up. The RESET input must remain HIGH until the CLK input is active (toggling) and stable. After releasing the RESET input, an additional 1024 CLK periods (≈150 μs at 6.912 MHz) must elapse before starting to program the chip via the I²C-bus interface. This must be done after every RESET pulse. The minimum duration of a RESET pulse is one CLK period. During reset, the I²C-bus and the IOM-2 interface are inactive.

Entering the Power-down mode is achieved by resetting the chip and holding the RESET input HIGH. This resets the on-chip PLL and stops the system clock. The user must ensure that the IOM-2 interface is deactivated and the I²C-bus idle before resetting the chip in order not to interrupt any transaction on these two interfaces. Note that stopping the CLK input is only allowed while the RESET input is HIGH. To exit the Power-down mode the RESET input is set LOW and after 1024 CLK periods (≈150 μs at 6.912 MHz) have elapsed normal operation can be resumed.

After reset, all the flip-flops are in a defined state, and the IOM, DSP and codecs are in inactive mode. In typical applications the universal codec is used with the PCD5093, which provides a clock (GP_CLK7) and a reset signal to the universal codec. The reset signal must be generated by a microcontroller port bit. The RESET_OUT pin of the PCD5093 cannot be used for this purpose, because GP_CLK7 is stopped while RESET_OUT is LOW after a Power-on-reset.

8 MEMORY AND CONTROL REGISTERS

8.1 DSP memories

The DSP in the PCD5096 has access to a 4k × 24-bit DSP program ROM, a 512 × 16-bit XRAM and a 512 × 16-bit YRAM.

8.2 Data memory and control register map

The PCD5096 contains a 128 word (128 × 16-bit) System Data RAM (SDR) and a group of 7 control registers mapped onto the upper addresses of the SDR.
The registers and the SDR are byte and word accessible externally, via the I^2C-bus interface and internally via the internal system bus.

The memory map is shown in Fig.6. The lower 32 words contain the DSP parameter table. The next 32 words are reserved for the IOM control table, which is used to control the activity on the IOM-2 interface (maximum 32 slots per 8 kHz speech frame). The rest of the SDR addressable space (40H to 77H) is free RAM and can be used to store up to 14 IOM data buffer pairs. In cases where not all 14 IOM buffer pairs are needed this memory space can be used for other applications via the I^2C-bus. The same holds for the unused part of the IOM control table.

The upper addresses of the SDR (78H to 7EH) are mapped onto 7 control registers (CR0 to CR6) that control the entire chip (DSP mode, data rate on the IOM-2 interface, control of the two codecs).

Note that the uppermost address of the SDR (7FH) is not mapped to any hardware register and is addressable as a normal RAM word.

The contents of the IOM control table and the IOM data buffers are described in Chapter 9. For further details about the DSP parameter table, see the *"PCD5096 DSP user manual"*.

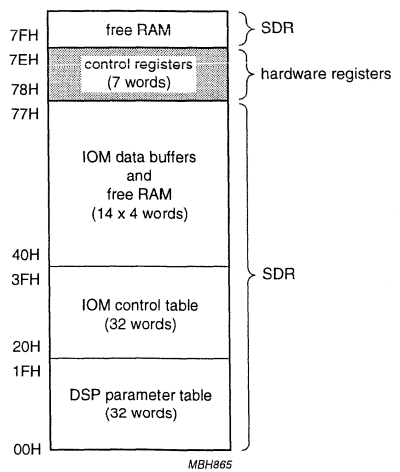


Fig.6 PCD5096 Memory map.

8.3 Control registers organization

8.3.1 CONTROL REGISTER ASSIGNMENT

The control register address assignment in the PCD5096 is shown in Table 3.

Table 3 Control register map

REGISTER	REGISTER MNEMONIC	SIZE (BITS)	ADDRESS (HEX)	RESET STATE (HEX)	FUNCTION
Control Register 0	CR0	16	78	0000	control signals for codecs, codec test modes, Power-down control and disable phase correction
Control Register 1	CR1	3	79	00	IOM control
Control Register 2	CR2	16	7A	0000	gain setting of analog-to-digital (A/D) and digital-to-analog (D/A) paths
Control Register 3	CR3	16	7B	A0A0	reference voltage setting of Codec 1 and Codec 2
Control Register 4	CR4	16	7C	0000	selection of the DSP modes
Control Register 5	CR5	2	7D	02	control of I/O pin IO0
Control Register 6	CR6	2	7E	02	control of I/O pin IO1

8.3.2 Control Register 0 (CR0)

Table 4 Control Register 0 (address 78H)

15	14	13	12	11	10	9	8
–	DISPC	CDC2TM2	CDC2TM1	CDC2TM0	CDC1TM2	CDC1TM1	CDC1TM0

Table 5 Control Register 0 (continued)

7	6	5	4	3	2	1	0
HFMICON	HSMICON	LHFEN	EHSEN	CDC2ON	ADD_DC	LIF1_EN	CDC1ON

Table 6 Description of CR0 bits

BIT	SYMBOL	DESCRIPTION
15	–	reserved, not used
14	DISPC	**Disable Phase Correction.** If DISPC = 1, phase correction is disabled.
13	CDC2TM2	**Functional test modes of Codec 2.** These 3 bits select the functional test modes of Codec 2; see Table 7.
12	CDC2TM1	
11	CDC2TM0	
10	CDC1TM2	**Functional test modes of Codec 1.** These 3 bits select the functional test modes of Codec 1; see Table 7.
9	CDC1TM1	
8	CDC1TM0	
7	HFMICON	**Hands-free Microphone ON in Codec 2.** When this bit is set the internal microphone reference voltage VREFMIC is connected to pad VMIC_HF (supply pad for the external hands-free microphone).
6	HSMICON	**Handset Microphone ON in Codec 2.** When this bit is set the internal microphone reference voltage VREFMIC is connected to pad VMIC_HS (supply pad for the external handset microphone).
5	LHFEN	**Loudspeaker Enable for hands-free.** This bit enables the Noise Shaper data in Codec 2 to the hands-free pads EARP_HF and EARM_HF.
4	EHSEN	**Earpiece Enable for Handset.** This bit enables the Noise Shaper data to the DAC in Codec 2.
3	CDC2ON	**Codec 2 ON.** When CDC2ON = 1, Codec 2 is ON.
2	ADD_DAC	**Add a DC offset in the microphone amplifier of Codec 1.**
1	LIF1_EN	**Line Interface Enable for Codec 1.** This bit enables the Noise Shaper data to the DAC in Codec 1.
0	CDC1ON	**Codec 1 ON.** When CDC1ON = 1, Codec 1 is ON.

Table 7 Selection of functional test modes for Codec 1 and Codec 2

CDC2TM2	CDC2TM1	CDC2TM0	FUNCTIONAL TEST MODE
CDC1TM2	CDC1TM1	CDC1TM0	
0	0	0	normal operation
0	0	1	1 bit analog
0	1	0	1 bit digital
0	1	1	1 bit closed loop
1	0	0	$4f_s$ codec
1	0	1	$4f_s$ DSP
1	1	0	$4f_s$ closed loop
1	1	1	PCM probe

8.3.3 CONTROL REGISTER 1 (CR1)

Table 8 Control Register 1 (address 79H)

2	1	0
IOM2	IOM1	IOM0

Table 9 Description of CR1 bits

BIT	SYMBOL	DESCRIPTION
2	IOM2	These 3 bits select the IOM mode; see Table 10.
1	IOM1	
0	IOM0	

Table 10 Selection of IOM mode

IOM2	IOM1	IOM0	IOM MODE
0	0	0	inactive
0	0	1	not used
0	1	0	IOM slave 256 kbits/s in 4 speech-slots/speech-frame
0	1	1	IOM slave 512 kbits/s in 8 speech-slots/speech-frame
1	0	0	IOM slave 768 kbits/s in 12 speech-slots/speech-frame
1	0	1	IOM slave 1024 kbits/s in 16 speech-slots/speech-frame
1	1	0	SpeechPro slave 2048 kbits/s in 32 speech-slots/speech-frame; note 1
1	1	1	IOM slave 2048 kbits/s in 32 speech-slots/speech-frame

Note

1. The SpeechPro mode is similar to the IOM slave 32 slots mode, but with a non-doubled data clock DCL.

8.3.4 Control Register 2 (CR2)

CR2 contains the gain setting values of the analog Codec 1 and Codec 2 section. The state of CR2 after reset is 0000H. This sets the A/D path and the D/A path gain to their minimum values of +9 dB and −13 dB respectively.

The D/A path gain is defined as the relationship between the level of the analog output signal, differentially seen at EARP_HS - EARM_HS or LIFP_DA1 - LIFM_DA1, expressed in dBm (0 dBm0 is 1 mW in 600 Ω), and the level of the digital input signal at the PCM interface, expressed in dBm0 according to CCITT Recommendation G.711. This D/A path gain definition assumes that the volume control in the DSP is set to the default value of 0 dB.

The A/D path gain is defined as the relationship between the level of the digital output signal at the PCM interface, expressed in dBm0, and the level of the analog input signal at the LIF interface, differentially seen at LIFP_AD2 - LIFM_AD2 or LIFP_AD1 - LIFM_AD1, expressed in dBm.

Table 11 Control Register 2 (address 7AH)

15	14	13	12	11	10	9	8
DA2.3	DA2.2	DA2.1	DA2.0	AD2.3	AD2.2	AD2.1	AD2.0

Table 12 Control Register 2 (continued)

7	6	5	4	3	2	1	0
DA1.3	DA1.2	DA1.1	DA1.0	AD1.3	AD1.2	AD1.1	AD1.0

Table 13 Description of CR2 bits

BIT	SYMBOL	DESCRIPTION
15	DA2.3	These 4 bits select the D/A path gain for Codec 2; see Table 14.
14	DA2.2	
13	DA2.1	
12	DA2.0	
11	AD2.3	These 4 bits select the A/D path gain for Codec 2; see Table 15.
10	AD2.2	
9	AD2.1	
8	AD2.0	
7	DA1.3	These 4 bits select the D/A path gain for Codec 1; see Table 14.
6	DA1.2	
5	DA1.1	
4	DA1.0	
3	AD1.3	These 4 bits select the A/D path gain for Codec 1; see Table 15.
2	AD1.2	
1	AD1.1	
0	AD1.0	

Table 14 Selection of D/A path gain for Codec 1 and Codec 2

DA1.3	DA1.2	DA1.1	DA1.0	D/A PATH GAIN (dB)
DA2.3	DA2.2	DA2.1	DA2.0	
0	0	0	0	−13
0	0	0	1	−12
0	0	1	0	−11
0	0	1	1	−10
0	1	0	0	−9
0	1	0	1	−8
0	1	1	0	−7
0	1	1	1	−6
1	0	0	0	−5
1	0	0	1	−4
1	0	1	0	−3
1	0	1	1	−2
1	1	0	0	−1
1	1	0	1	0
1	1	1	0	+1
1	1	1	1	+2

Table 15 Selection of A/D path gain for Codec 1 and Codec 2

AD1.3	AD1.2	AD1.1	AD1.0	A/D PATH GAIN (FROM LIF TO PCM) (dB)
AD2.3	AD2.2	AD2.1	AD2.0	
0	0	0	0	+9
0	0	0	1	+10
0	0	1	0	+11
0	0	1	1	+12
0	1	0	0	+13
0	1	0	1	+14
0	1	1	0	+15
0	1	1	1	+16
1	0	0	0	+17
1	0	0	1	+18
1	0	1	0	+19
1	0	1	1	+20
1	1	0	0	+21
1	1	0	1	+22
1	1	1	0	+23
1	1	1	1	+24

8.3.5 Control Register 3 (CR3)

This 16-bit register is used to adjust the reference voltage of Codec 1 and Codec 2 to 2000 mV. An accuracy of 12 mV is guaranteed. The equation for determining the reference voltage (VREFn) for each codec is given below:

$$VREFn = \frac{256 \times VBGP}{RVnREF}$$

Where 'n' is the codec number and can take a value of '1' or '2'. The default value for VBGP is 1.25 V but this may vary due to process spread (see Chapter 16). Note that increasing RVnREF reduces VREFn.

For correct function of the analog blocks, care must be taken to have sensible values in CR3. For example, bits (15:14), as well as (7:6) must be '10'. The state of this register after reset is A0A0H.

Table 16 Control Register 3 (address 78H)

15	14	13	12	11	10	9	8
1	0	RV2REF5	RV2REF4	RV2REF3	RV2REF2	RV2REF1	RV2REF0

Table 17 Control Register 3 (continued)

7	6	5	4	3	2	1	0
1	0	RV1REF5	RV1REF4	RV1REF3	RV1REF2	RV1REF1	RV1REF0

Table 18 Description of CR2 bits

BIT	SYMBOL	DESCRIPTION
15	–	This bit must be set to a logic 1.
14	–	This bit must be set to a logic 0.
13	RV2REF5	These 5 bits are used to select the reference voltage of Codec 2.
12	RV2REF4	
11	RV2REF3	
10	RV2REF2	
9	RV2REF1	
8	RV2REF0	
7	–	This bit must be set to a logic 1.
6	–	This bit must be set to a logic 0.
5	RV1REF5	These 5 bits are used to select the reference voltage of Codec 1.
4	RV1REF4	
3	RV1REF3	
2	RV1REF2	
1	RV1REF1	
0	RV1REF0	

8.3.6 Control Register 4 (CR4)

CR4 is used to select the DSP modes. For further information see the *"PCD5096 DSP user manual"*. Its state after reset is 0000H.

Table 19 Control Register 4 (address 7CH)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	–	LLb2	LLb1	LLb0	LLa2	LLa1	LLa0	OPM1	OPM0

Table 20 Description of CR4 bits

BIT	SYMBOL	DESCRIPTION
15 to 8	–	These 8 bits are not used.
7	LLb2	These 3 bits select the connection mode for channel LLb; see Table 21.
6	LLb1	
5	LLb0	
4	LLa2	These 3 bits select the connection mode for channel LLa; see Table 21.
3	LLa1	
2	LLa0	
1	OPM1	These 2 bits select the operation mode, see Table 22.
0	OPM0	

Table 21 Selection of the connection mode for channels LLb and LLa

LLb2	LLb1	LLb0	CONNECTION MODES
LLa2	LLa1	LLa0	
0	0	0	Idle mode with reset of LEC coefficients
0	0	1	Idle mode without reset of LEC coefficients
0	1	0	speech and tone
0	1	1	tone generation
1	0	0	dial tone detection
1	0	1	not allowed
1	1	0	not allowed
1	1	1	not allowed

Table 22 Selection of the operation mode

OPM1	OPM0	OPERATION MODE
0	0	connection mode
0	1	read/write RAM mode
1	0	software reset
1	1	not allowed

8.3.7 Control Register 5 (CR5)

CR5 controls the general purpose I/O pin IO0.

Table 23 Control Register 5 (address 7DH)

1	0
IODIR0	IO0

Table 24 Description of CR5 bits

BIT	SYMBOL	DESCRIPTION
1	IODIR0	Direction control for IO0. If IODIR0 = 1, then IO0 is an input. If IODIR0 = 0, then IO0 is an output. Input during and after reset; see note 1.
0	IO0	State of IO0

Note

1. Depending on the DSP program, the contents of CR5 might be overwritten by the DSP as soon as the reset is inactive.

8.3.8 Control Register 6 (CR6)

CR6 controls the general purpose I/O pin IO1.

Table 25 Control Register 6 (address 7EH)

1	0
IODIR1	IO1

Table 26 Description of CR6 bits

BIT	SYMBOL	DESCRIPTION
1	IODIR1	Direction control for IO1. If IODIR1 = 1, then IO1 is an input. If IODIR1 = 0, then IO1 is an output. Input during and after reset; see note 1.
0	IO1	State of IO1

Note

1. Depending on the DSP program, the contents CR6 might be overwritten by the DSP as soon as the reset is inactive.

9 IOM

9.1 Features

The IOM block in the PCD5096 is a 4-wire serial interface performing the following functions:

- Digital interface with up to fourteen 64 kbits/s channels at a bit rate of n × 256 kbits/s (n = 1, 2, 3, 4 or 8), complying with the IOM-2 specifications (IOM-2 is a registered trademark of Siemens AG)
- Digital interface with 32 slots/frame and non-doubled data clock, compatible with the digital interface of some DTAM speech compression ICs
- Autonomous storing/fetching of data to/from the system data memory (SDR) using internal addressing logic
- Byte or word (16 bits) transfer
- 14 data buffers (byte or word)
- Muting of speech data
- Local call.

9.2 Pin description

The following pins are used by the IOM-2 interface:

- **DI**: serial data input with a bit rate of n × 256 kbits/s (n = 1, 2, 3, 4 or 8)
- **DO**: serial data output with a bit rate of n × 256 kbits/s (n = 1, 2, 3, 4 or 8). DO is an open-drain pin, as many devices must be able to write on the same data line in a time-multiplexed mode. Therefore, DO must be externally pulled-up.
- **FSC**: 8 kHz frame synchronization input
- **DCL**: data clock input. Twice the data transmission frequency on DI and DO, except in the non-doubled data clock mode (see Section 9.3).

9.3 Functional description

The digital interface of the PCD5096 can work at several bit rates; these are specified Table 27. The bit rate is selected by writing the appropriate 3 bit code, given in Table 27, into Control Register 1 (address 79H).

The PCD5096 is always a slave on the IOM interface, which means that both FSC and DCL are inputs. This is valid for both the IOM modes and the Speech mode.

FSC is an 8 kHz framing signal for synchronizing data transmission on DI and DO. The rising edge of FSC gives the time reference for the first bit transmitted in the first slot of a speech frame. The number of slots per speech frame depends on the selected data rate. Each slot contains 8 data bits.

DCL is a data clock. Its frequency is twice the selected data rate in IOM mode. In Speech mode, the DCL frequency is equal to the data rate (2048 kHz for 2048 kbits/s).

DI is the serial data input. Data coming on DI in packets of 8 bits (A-law PCM encoded data) or 16 bits (linear PCM data) is stored temporarily in an IOM data buffer, from where it is processed by the on-chip DSP. On the other hand, data written into the IOM data buffers by the DSP is shifted out on pin DO.

There are 14 IOM data buffers, allowing the use of 14 different channels. One channel is 64 kbits/s for A-law PCM encoded data and 128 kbits/s if linear PCM data is transferred, in which case two consecutive slots are used.

The Speech mode was implemented to support the codec interface of some speech compression ICs. This mode is very similar to the IOM 32 slots mode, the main difference being the non-doubled data clock. See Section 9.4 for timing information.

Table 27 IOM modes

IOM2	IOM1	IOM0	MODE
0	0	0	These codes deactivate the IOM-2 interface and stop all the transactions on the IOM bus. This is the default state after reset.
0	0	1	
0	1	0	IOM slave mode, 256 kbits/s in 4 slots/speech-frame
0	1	1	IOM slave mode, 512 kbits/s in 8 slots/speech-frame
1	0	0	IOM slave mode, 768 kbits/s in 12 slots/speech-frame
1	0	1	IOM slave mode, 1024 kbits/s in 16 slots/speech-frame
1	1	0	Speech mode, 2048 kbits/s in 32 slots/speech-frame. The Speech mode is similar to the IOM slave 32 slots mode, but with a non-doubled data clock DCL.
1	1	1	IOM slave mode, 2048 kbits/s in 32 slots/speech-frame

9.4 Timing

The timing on the 4-wire interface for the IOM mode is shown in Fig.7 and specified in Table 28. The timing for the Speech mode is shown Fig.8 and specified in Table 29.

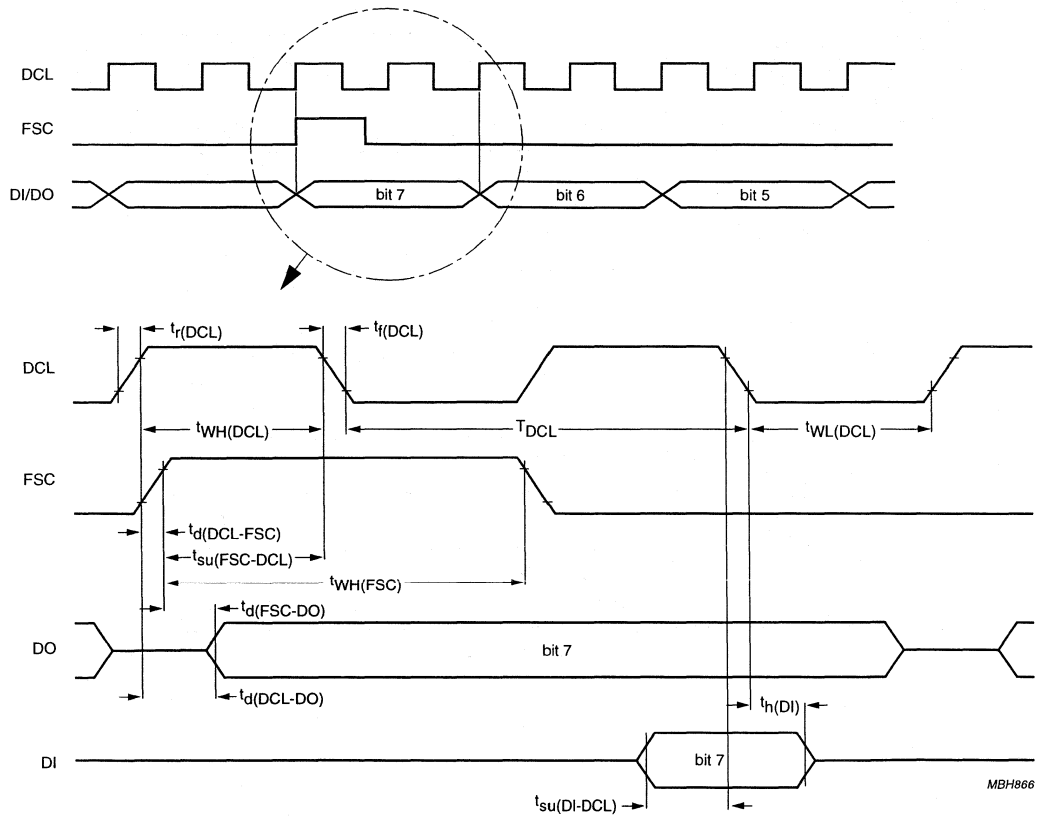


Fig.7 4-wire interface timing in IOM mode.

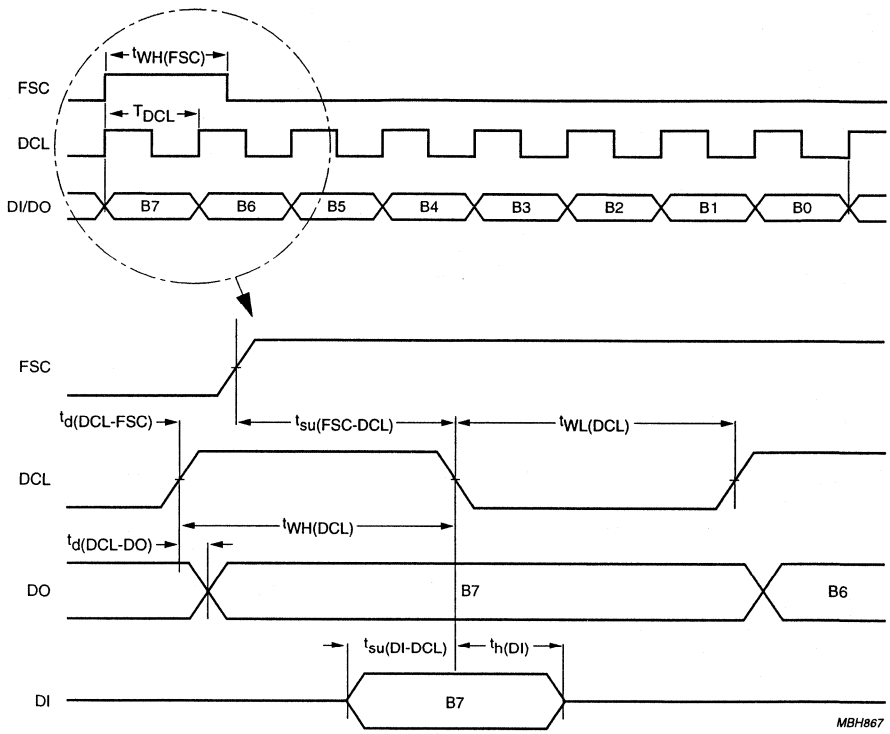


Fig.8 4-wire interface timing in Speech mode.

Table 28 Timing parameters in IOM mode; see Fig.7

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$t_{r(DCL)}$	data clock rise time	–	60	ns
$t_{f(DCL)}$	data clock fall time	–	60	ns
T_{DCL}	data clock period	220[1]	–	ns
$t_{WH(DCL)}$	data clock pulse width HIGH	80	–	ns
$t_{WL(DCL)}$	data clock pulse width LOW	80	–	ns
$t_{r(FSC)}$	frame sync rise time	–	60	ns
$t_{f(FSC)}$	frame sync fall time	–	60	ns
$t_{d(DCL-FSC)}$	frame delay DCL to FSC	$-t_{WL(DCL)}$	60	ns
$t_{su(FSC-DCL)}$	frame set-up time FSC to DCL	60	–	ns
$t_{WH(FSC)}$	frame width HIGH	130	–	ns
$t_{d(DLC-DO)}$	data delay from data clock	–	100[2]	ns
$t_{d(FSC-DO)}$	data delay from frame	–	150[2]	ns
$t_{su(DI-DCL)}$	set-up time DI to DCL	$t_{WH(DCL)}$	–	ns
$t_{h(DI)}$	data hold time	50	–	ns

Notes

1. Corresponds to the highest DCL frequency allowed (4.096 MHz) with a 10% margin.
2. C_L = 150 pF.

Table 29 Timing parameters in Speech mode; see Fig.8

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$t_{d(DCL-FSC)}$	frame delay time DCL to FSC	$-t_{wL(DCL)}$	100	ns
$t_{su(FSC-DCL)}$	frame set-up time FSC to DCL	60	–	ns
$t_{WH(FSC)}$	frame width HIGH	130	–	ns
T_{DCL}	data clock period	440[1]	–	ns
$t_{WL(DCL)}$	data clock pulse width LOW	150	–	ns
$t_{WH(DCL)}$	data clock pulse width HIGH	150	–	ns
$t_{d(DCL-DO)}$	data delay from clock	–	100[2]	ns
$t_{su(DI-DCL))}$	set-up time DI to DCL	60	–	ns
$t_{h(DI)}$	data hold time	60	–	ns

Notes

1. Corresponds to the DCL frequency (2.048 MHz) with a 10% margin.
2. C_L = 150 pF.

9.5 IOM control table

The selection of active slots in the IOM-2 interface and the logic connection between an IOM slot and an IOM data buffer is defined in the IOM control table located at addresses 20H to 3FH of the SDR. The IOM control table is 'n' words long. The number 'n' is the number of slots resulting from the IOM mode selection in Control Register 1. Speech slot 0 is defined by word 0 (address 20H) in the IOM control table, and speech slot 'n' by word 'n' (address 20H + n). The IOM interface block reads all words in the IOM control table once every speech frame (125 µs). In every IOM slot in a speech frame the IOM-2 interface block reads the corresponding word in the IOM control table. The function of the bits within each word is shown in Table 30. Depending on the IOM mode selected, only part of the IOM control table address space is used. The unused space is free for extra IOM data buffers or for other applications.

Table 30 Word definition in the IOM control table

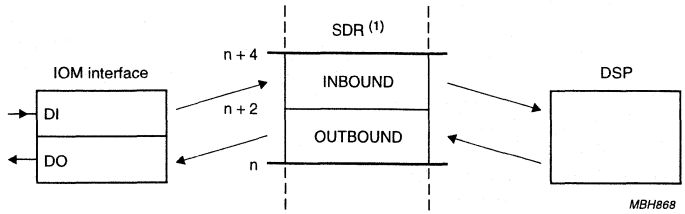
BIT	FUNCTION
B15 to B10	not used
B9	**Mute.** If B9 = 1, data on the DO output is forced to zero regardless of the contents of the IOM data buffer. The input data on DI is not affected. If B9 = 0, then normal operation is selected.
B8	**Local.** If B8 = 1, swap in/out buffers. If B8 = 0, then normal operation is selected. See Section 9.7.
B7	**Select byte.** When byte transfer is selected (B6 = 1); B7 = 1, selects the high byte and B7 = 0 selects the low byte.
B6	**Byte/word transfer.** If B6 = 1, then byte transfer is selected. If B6 = 0, then word transfer is selected and two consecutive slots are activated.
B5	**Active slot.** If B5 = 1, the slot is active. If B5 = 0, the slot is idle.
B4 to B0	**IOM data buffer assigned to the slot.** These 4 bits select the locations in SDR where the IOM data buffer will reside. The allowed values are 10000 to 11101; see Table 31.

Table 31 IOM data buffers location in SDR

IOM BUFFER CODE					ADDRESS IN SDR (HEX)
B4	B3	B2	B1	B0	
1	0	0	0	0	40 to 43
1	0	0	0	1	44 to 47
1	0	0	1	0	48 to 4B
1	0	0	1	1	4C to 4F
1	0	1	0	0	50 to 53
1	0	1	0	1	54 to 57
1	0	1	1	0	58 to 5B
1	0	1	1	1	5C to 5F
1	1	0	0	0	60 to 63
1	1	0	0	1	64 to 67
1	1	0	1	0	68 to 6B
1	1	0	1	1	6C to 6F
1	1	1	0	0	70 to 73
1	1	1	0	1	74 to 77

9.6 IOM data buffers

The address space 40H to 77H in the SDR is reserved for up to 14 IOM data buffers. These buffers are used to exchange data between the IOM-2 interface and the on-chip DSP. Each IOM data buffer consists of four 16-bit words: two words for storing inbound data and two words for outbound data; this is shown in Fig.9



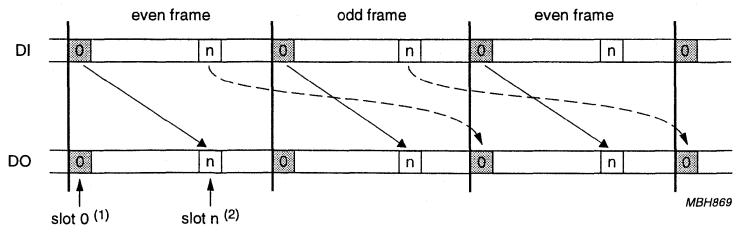
(1) IOM data buffers location is SDR: n = S × 4 with S = B4 to B0 of the corresponding word in the IOM control table.

Fig.9 Data flow between the IOM-2 interface and the DSP.

9.7 Local loop

A local call is implemented in order to loop-back data from one codec to another codec and vice-versa, as illustrated in Fig.10. The inbound and outbound buffer are simply swapped. This is done by setting bit 8 in the correct IOM control table word (see Section 9.5).

A local call is created by assigning one IOM data buffer to 2 codecs, whereby in one IOM control word bit 8 is set, and in the other IOM control word bit 8 is reset.



(1) Bit 8 is set in slot 0 control word.
(2) Bit 8 is reset in slot n control word.

Fig.10 Local call switching on the IOM interface.

10 I²C-BUS INTERFACE

The PCD5096 is programmed by writing to the control registers (CR0 to CR6) and loading the SDR using the I²C-bus interface. The master on the I²C-bus is either a PCD509x DECT processor or an external microcontroller.

The memory map of the PCD5096 is given in Chapter 8. It consists of 128 words (16 bits wide) of system data IOM buffers, IOM control data and DSP parameters) and 7 words (16 bits wide) of control registers mapped at addresses 78H to 7EH.

The I²C-bus interface uses word and byte access to the RAM and to the control registers. For byte access the address is not incremented automatically. For word access the address is incremented after two data bytes (low, high byte) in order to be able to fill the memory without a full I²C-bus protocol (start, slave address, stop bits).

The protocol is shown in Figs 12 to 15. I2C_BYTE = 1, for byte access and I2C_BYTE = 0, for word access. I2C_BSEL = 1 for selecting the high byte and I2C_BSEL = 0 for selecting the low byte. For control registers with less than 8 bits, there is no difference between word access, high byte access and low byte access.

The PCD5096 has two pins (A1 and A0) for programming the slave address. This means that a maximum of four devices can be located on a board without glue logic. The I²C-bus slave address allocated for the PCD5096 is shown in Fig.11.

A6	A5	A4	A3	A2	A1	A0	R/$\overline{W}$
0	0	1	1	0	A1	A0	

MBH870

Fig.11 PCD5096 I²C-bus slave address.

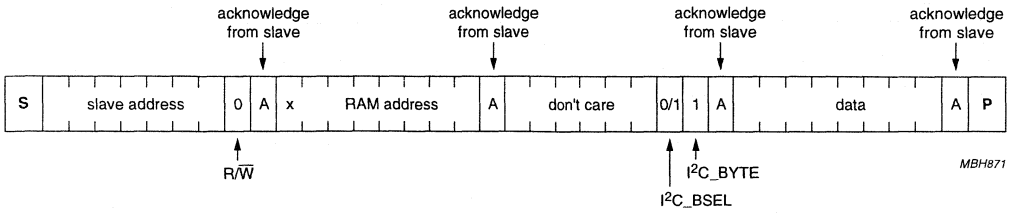


Fig.12 I²C-bus write byte.

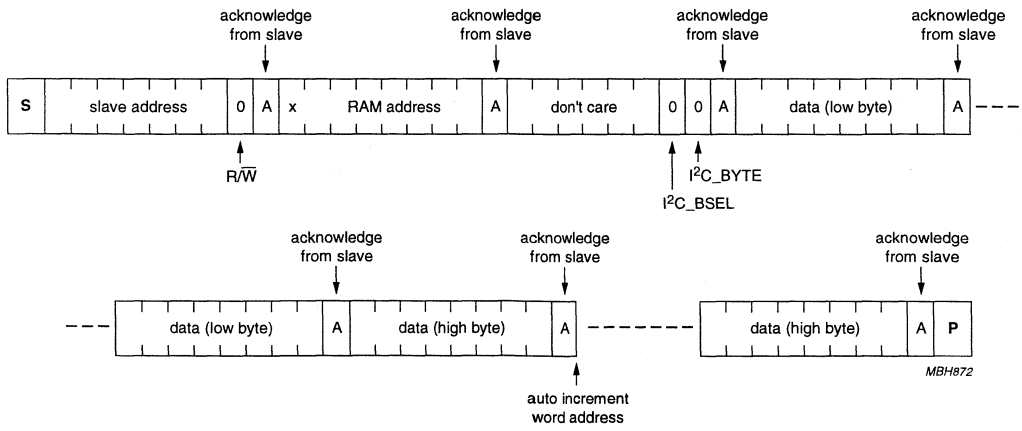


Fig.13 I²C-bus write word.

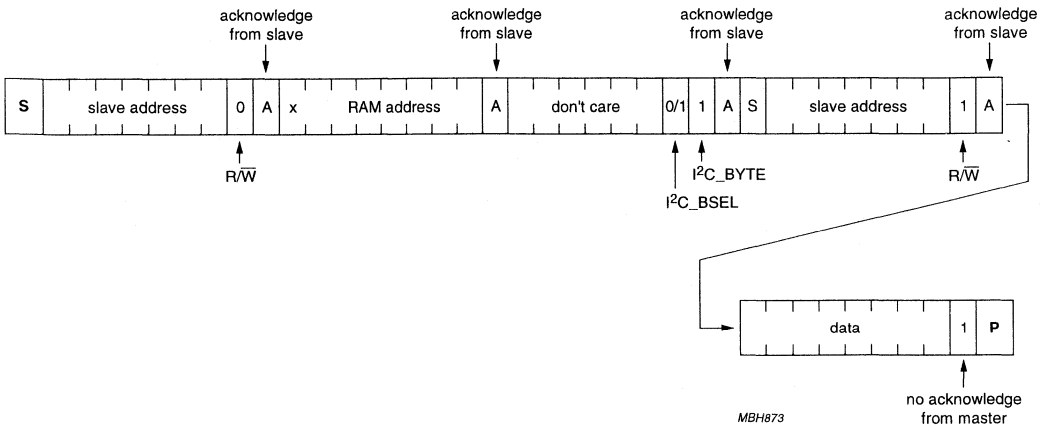


Fig.14 I²C-bus read byte.

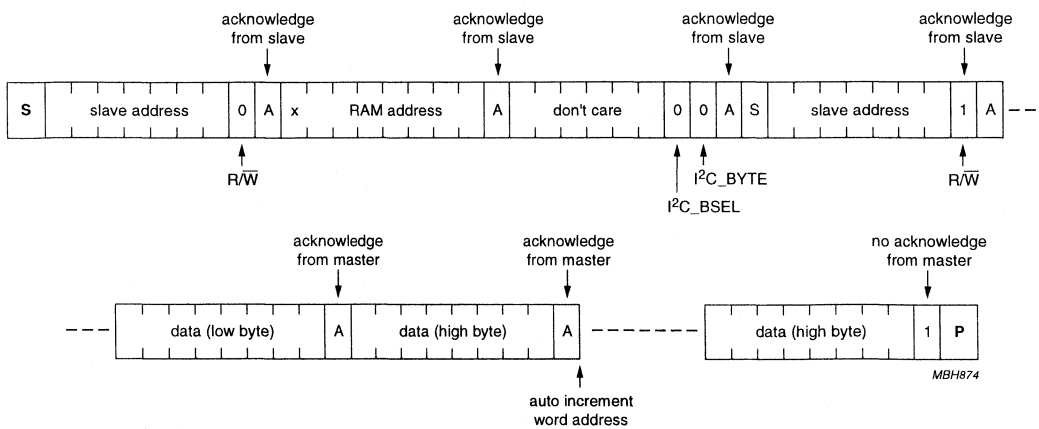


Fig.15 I²C-bus read word.

11 CODEC TEST LOOPS

11.1 Test modes definition

For debug and evaluation purposes some test loops are implemented in the speech codecs. These test loops are activated by setting bits 13 to 8 in Control Register 0; see Table 32. The signal flow in the test loops is shown in Fig.16 and is described as follows:

- **Normal operation**: the codec is not in any of its test loop modes; used for a normal application.
- **1 bit analog**: this loop is intended for a separate evaluation of the analog parts of the codec. A bitstream interface ($108f_s$) is available. Via TEST_INPUT bitstream data is fed to the DAC and bitstream data from the ADC is present on TEST_OUTPUT.
- **1 bit digital**: this loop allows the evaluation of DDF and DNS at the $108f_s$ interface. Bitstream data from TEST_INPUT is led to DDF and bitstream data from DNS is available on TEST_OUTPUT.
- **1 bit closed loop**: a connection between the bitstream output of the ADC and the bitstream input of the DAC is made. The bitstream data is also made available on TEST_OUTPUT.
- **$4f_s$ codec**: the $4f_s$ codec loop gives access to the $4f_s$ interface for evaluation of DDF and DNS. 16-bit input data is serially shifted in (two's complement, MSB first) on TEST_INPUT and the 14 MSBs are used by DNS. On the other side 16 bits DDF output data is serially shifted out on TEST_OUTPUT.
- **$4f_s$ DSP**: this loop allows evaluation of the DSP software. On TEST_INPUT and TEST_OUTPUT, data can be exchanged with the DSP (16 bits serially, 2's complement, MSB first).
- **$4f_s$ closed loop**: a connection between the parallel output of DDF and the input of DNS is made. The loop data at $4f_s$ can be monitored by shifting out bits serially via TEST_OUTPUT.
- **PCM probe**: this special test loop allows the evaluation of DSP software. The DSP software however, must include a test mode in which any 16-bit data at a sample rate of f_s or 8 kHz (normally only present as numbers within the DSP algorithm) is written to the output line that is connected to DNS. While normally the data on this line has a $4f_s$ (32 kHz) sample rate, up to four (interleaved) PCM signals can be monitored via TEST_OUTPUT.

Next to these hardware codec test loops there also may be software DSP test loops, depending on the DSP software version. For more information about the DSP software the DSP manuals must be consulted.

In all codec test loop modes (except the normal operation mode) the signals lines TEST_INPUT_x and TEST_OUTPUT_x (x = 1 for Codec 1, x = 2 for Codec 2) are mapped onto pins that normally have a different function. Next to these data signals some timing signals (FS4 and CLK3) are presented on pins. Table 33 shows which pins are used in the codec test loop modes.

Table 32 Selection of functional test modes for Codec 1 and Codec 2

CDC1TM2	CDC1TM1	CDC1TM0	FUNCTIONAL TEST MODE
CDC2TM2	CDC2TM1	CDC2TM0	
0	0	0	normal operation
0	0	1	1 bit analog
0	1	0	1 bit digital
0	1	1	1 bit closed loop
1	0	0	$4f_s$ codec
1	0	1	$4f_s$ DSP
1	1	0	$4f_s$ closed loop
1	1	1	PCM probe

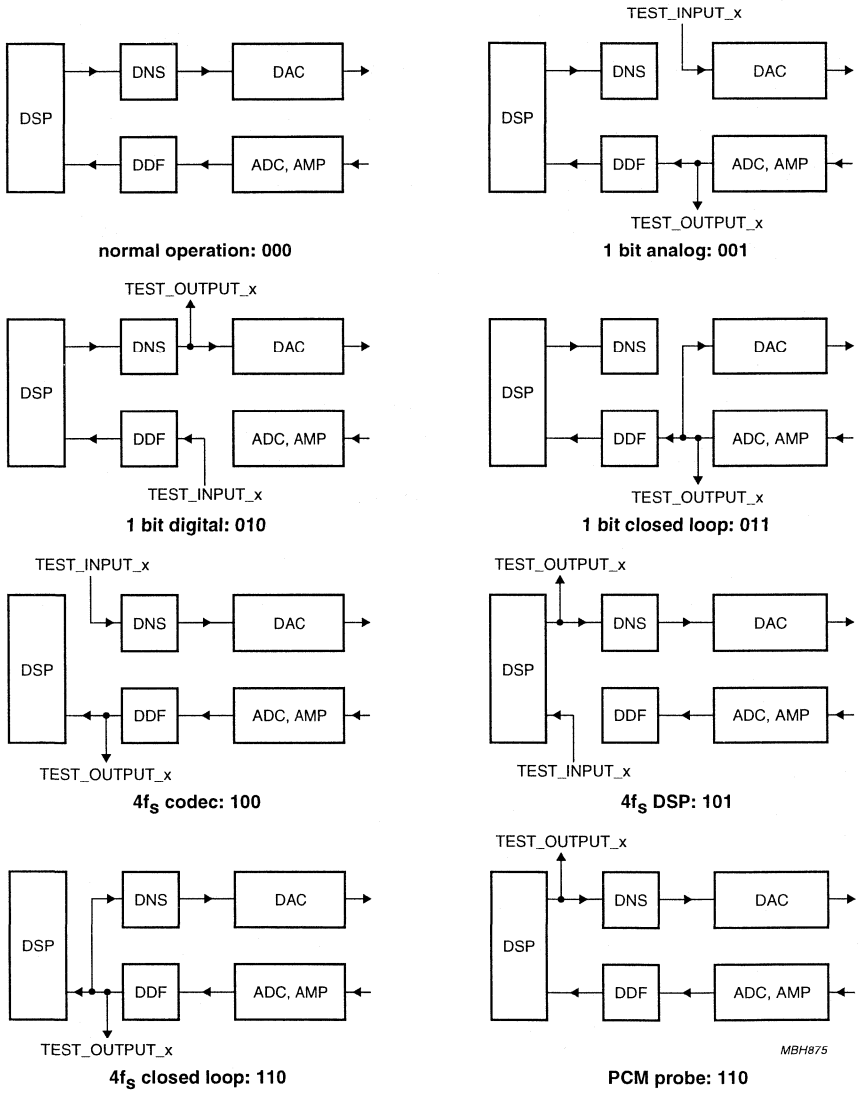


Fig.16 Speech codec test loops.

Table 33 Pin redefinition in Codec test loop mode

NORMAL MODE	CODEC TEST LOOP MODE		
PIN NAME	**SIGNAL NAME**	**I/O**	**DESCRIPTION**
DI	TEST_INPUT_1	I	$108f_s$ bitstream or $4f_s$ serial data input to Codec 1
DO	TEST_OUTPUT_1	O	$108f_s$ bitstream or $4f_s$ serial data output from Codec 1
A1	TEST_INPUT_2	I	$108f_s$ bitstream or $4f_s$ serial data input to Codec 2
IO1	TEST_OUTPUT_2	O	$108f_s$ bitstream or $4f_s$ serial data output from Codec 2
DCL	CLK3	O	3456 kHz bit clock signal ($4 \times 108f_s$) with 50% duty cycle
IO0	FS4	O	32 kHz word synchronization signal ($4f_s$), duty cycle = 12/108

11.2 Codec test loop signal timing

The TEST_OUTPUT_x signal changes at the falling edge of CLK3, and the signal presented on TEST_INPUT_x is sampled just before the falling edge of CLK3. Note that the $4f_s$ serial PCM data shifted in via TEST_INPUT_x is only used during the next FS4 HIGH period.

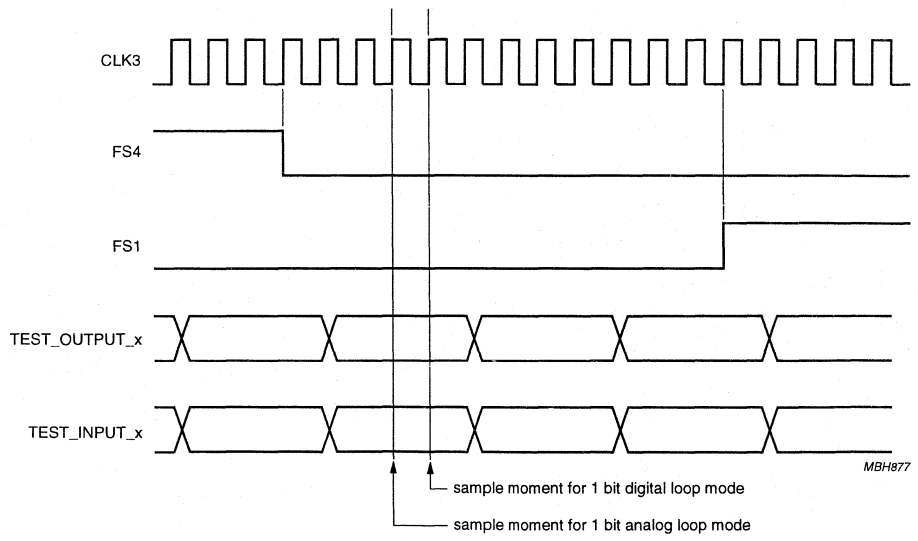


Fig.17 Codec test loop signal timing for $108f_s$ 1-bit bitstream signals.

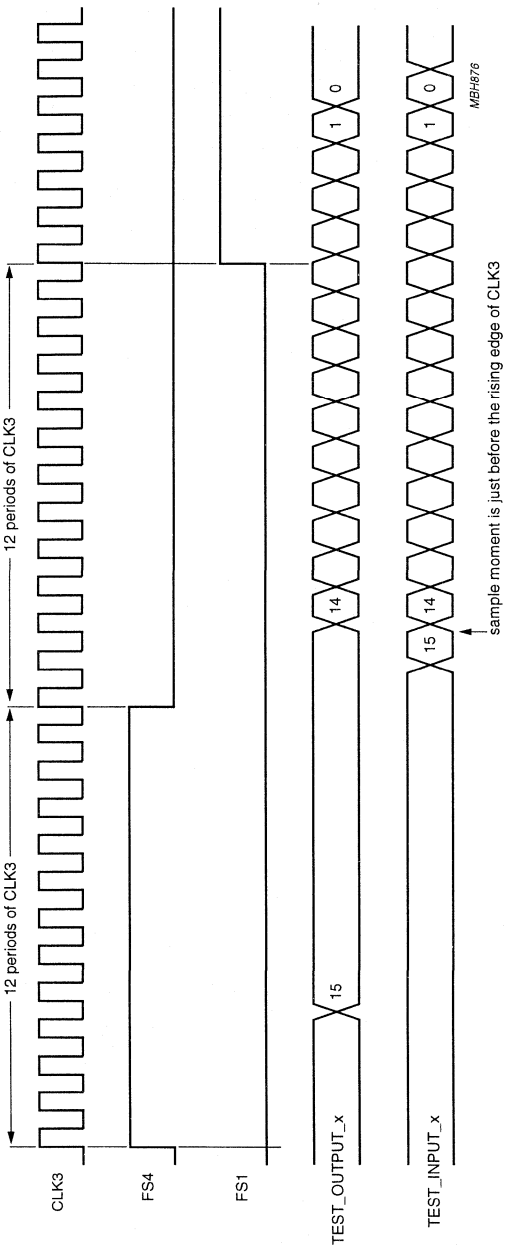


Fig.18 Codec test loop signal timing for $4f_s$ 16-bit serial signals.

12 APPLICATION INFORMATION

12.1 Small business systems

The PCD5096 is designed for business and residential phone systems. In combination with a processor like the PCD5093, two simultaneous calls on 2 PSTN lines (Ba, Bb) can be processed. To realize single line systems with hands-free functionality one analog interface port can be connected to a speaker phone and the other to the line interface. A typical small business system consists of a PCD5093 DECT processor with radio interface and a single universal codec (see Fig.19).

The possible configurations for speech connections in the universal codec are listed in Table 34.

A real hands-free solution can also be implemented by using one PSTN line port and connecting a corded handset, a hands-free microphone and a loudspeaker to the second analog interface port of the universal codec.

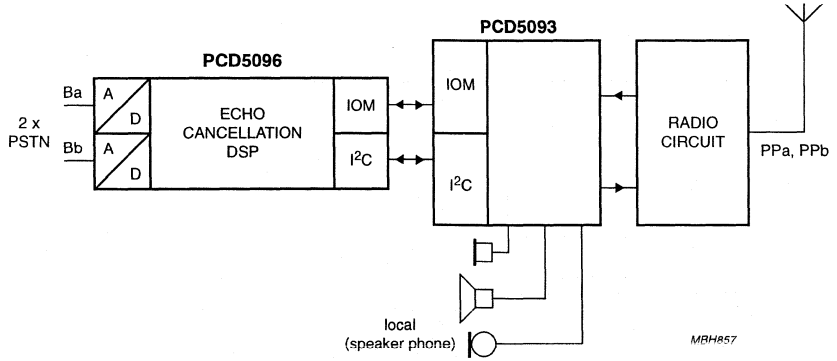


Fig.19 Small business system.

Table 34 Possible speech connections in a small business system

SINGLE CONNECTIONS	DUAL CONNECTIONS	
LOCAL ↔ Ba	(LOCAL ↔ Ba) + (Bb ↔ PPa)	(LOCAL ↔ Ba) + (Bb ↔ PPb)
LOCAL ↔ Bb	(LOCAL ↔ Bb) + (Ba ↔ PPa)	(LOCAL ↔ Bb) + (Ba ↔ PPb)
LOCAL ↔ PPa	(LOCAL ↔ PPa) + (Ba ↔ PPb)	(LOCAL ↔ PPa) + (Bb ↔ PPb)
LOCAL ↔ PPb	(LOCAL ↔ PPb) + (Ba ↔ PPa)	(LOCAL ↔ PPb) + (Bb ↔ PPa)
Ba ↔ PPa	(Ba ↔ PPa) + (Bb ↔ PPb)	–
Ba ↔ PPb	(Ba ↔ PPb) + (Bb ↔ PPa)	–
Bb ↔ PPa	–	–
Bb ↔ PPb	–	–

12.2 Large business systems

For large business systems, local loop and public access systems, several PCD5096 codecs can be connected together utilizing the serial bus system. A digital cordless base station for large business systems typically consists of a baseband processor, radio interface and a number of universal codecs interfacing to local lines, PSTN lines and to the local corded handset/hands-free interface. A diagram of this configuration is shown in Fig.20.

The universal codec can connect to different applications in a typical large business system. They are as follows:

1. PSTN Line Interface
2. Speaker phone with hands-free feature
3. Local Line Interface.

In these applications the additional processing required for conference calling is performed either in the host baseband processor, or in the universal codecs.

For further details about these three applications consult the *"PCD5096 DSP user manual"*.

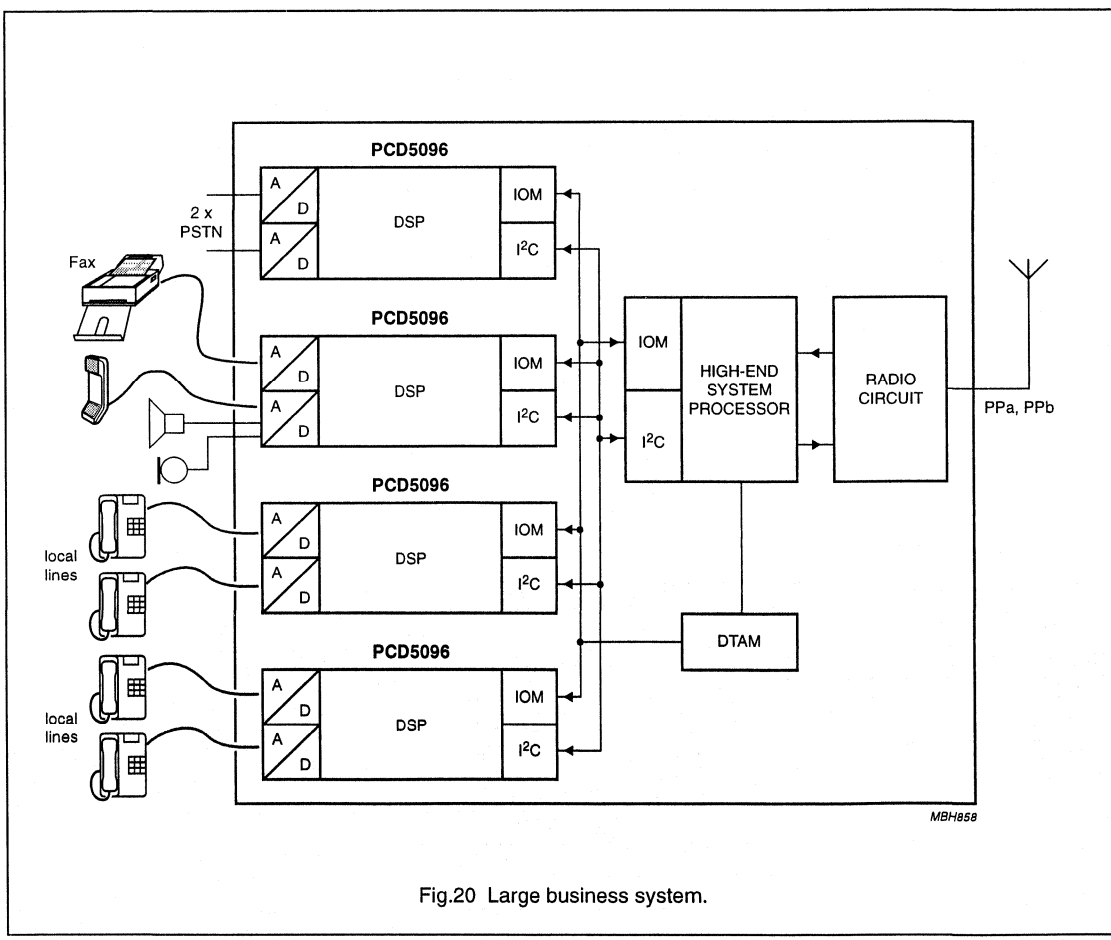


Fig.20 Large business system.

12.3 DECT and ISDN

The PCD5096 is perfectly suited to extend an ISDN-based DECT base station with analog extension lines. The IOM-2 interface communicates with the S0 interface chip. The host controller can connect via IOM-2 or I^2C-bus to the PCD5096. The two analog interfaces of the PCD5096 can either be used to connect to analog phones/Fax machines, or combine hands-free and one analog extension.

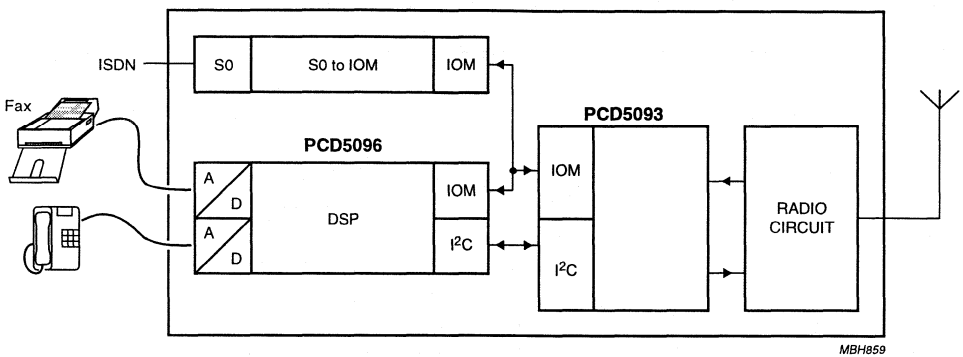


Fig.21 DECT and ISDN.

13 APPLICATION EXAMPLES

In this chapter some application examples are given to assist users with the programming of the PCD5096 (DSP parameter settings, control register settings and IOM-2 interface programming). Three examples are considered: a two channel application, a conference call application between one PSTN line and two IOM buffers, and a conference call application between two PSTN lines and one IOM buffer.

13.1 PCD5096 with two active channels

A typical application for the PCD5096 is depicted in Fig.22. Two handsets (PPa and PPb) are connected through a PCD5093 and a PCD5096 to two PSTN lines. Tables 35, 36 and 37 show possible settings for the DSP parameters, the IOM control table and the control registers in the PCD5096.

Note that the chosen values for the IOM pointers, the volume parameters and the frequency parameters depend on the application. This means that they can differ from the values that are given in this example.

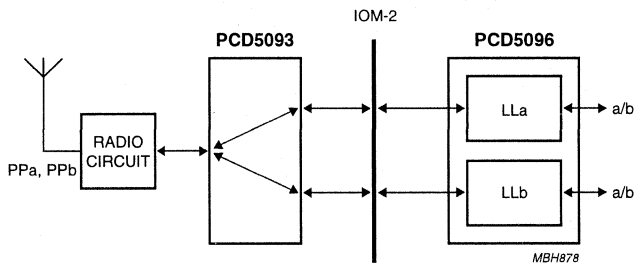


Fig.22 Typical PCD5096 application with two channels.

Table 35 DSP parameters for two active channels

SDR ADDRESS (HEX)	PARAMETER NAME		VALUE (HEX)	FUNCTION
00	LLa_IOM1	LLb_IOM1	484C	not used
01	LLa_LSW	LLb_LSW	FFFF	2 × analog line interface (LLx_IOM1 not used)
02	LLa_LEC	LLb_LEC	FFFF	2 × Local Echo Canceller ON
03	LLa_NES	LLb_NES	2D2D	2 × Network Echo Suppressor (9 dB attenuation)
04	LLa_AGC	LLb_AGC	FFFF	2 × Automatic Gain Control ON
05	LLa_TXV	LLb_TXV	2020	2 × Transmit Volume set to 0 dB
06	LLa_ISW	LLb_ISW	0000	2 × 8-bit A-law PCM data
07	LLa_IOM2	LLb_IOM2	4044	Codec 1 uses IOM buffer at address 40H
				Codec 2 uses IOM buffer at address 44H
08	LLa_SMU2	LLb_SMU2	0000	2 × Soft Mute OFF
09	LLa_AVR	LLb_AVR	0000	2 × Automatic Volume Control OFF
0A	LLa_RXV	LLb_RXV	2020	2 × Receive Volume set to 0 dB
0B	LLa_PST	LLb_PST	0000	2 × Site Tone OFF
0C	LLa_TST	LLb_TST	0000	2 × Tone Site Tone OFF (LLx_TOGx and LLx_TOVx not used)
0D	LLa_TOV1	LLb_TOV1	4040	2 × Tone Volume for Tone 1 set to 0 dB
0E	LLa_TOV2	LLb_TOV2	4040	2 × Tone Volume for Tone 2 set to 0 dB
0F	LLa_TOG1		7ECE	Tone 1 to Codec 1
10	LLa_TOG2		7E8A	Tone 2 to Codec 1
11	LLb_TOG1		7E37	Tone 1 to Codec 2
12	LLb_TOG2		7DD2	Tone 2 to Codec 2
13	CCa_CNC	reserved	0000	no conference call (CCa_IOMx not used)
14	CCa_IOM3	CCa_IOM4	5054	not used
15	CCa_SMU3	CCa_SMU4	0000	not used

Table 36 IOM control table for two active channels

SDR ADDRESS (HEX)	PARAMETER NAME	VALUE (HEX)	FUNCTION
20	slot 0 control	0070	IOM slot 0 uses buffer at address 40H
21	slot 1 control	0071	IOM slot 1 uses buffer at address 44H
22 to 3F	slot 2-slot 32	0000	slots 2 to 32 inactive

Table 37 Control registers for two active channels

SDR ADDRESS (HEX)	PARAMETER NAME	VALUE (HEX)	FUNCTION
78	codec control	005B	Codec 1 ON, Codec 2 ON
79	IOM control	0004	IOM slave mode, 768 kbits/s
7A	gain settings A/D and D/A paths	D0D0	A/D gain = +9 dB, D/A gain = 0 dB for both channels
7B	VREF1, VREF2 settings	A0A0	default setting for VREF1 and VREF2
7C	DSP modes	0048	both channels run in speech and tone mode

13.2 Conference call between one PSTN line and two IOM buffers

The PCD5096 is able to perform a 3 party conference call. Figure 23 shows a typical configuration, with two handsets in conference call with an PSTN line. Tables 38, 39 and 40 show possible settings for the DSP parameters, the IOM control table and the control registers in the PCD5096.

Note that the LLb block of the PCD5096 could be used in parallel to connect a second PSTN line to another IOM buffer. This is not covered in this example.

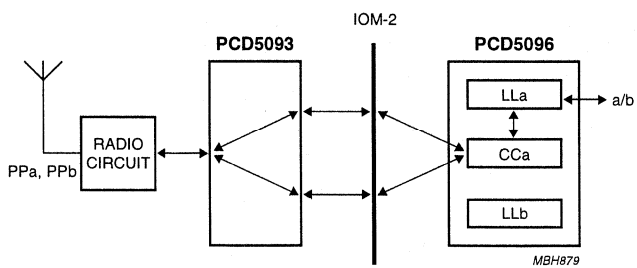


Fig.23 Conference call between one PSTN line and two IOM buffers.

Table 38 DSP parameters for conference call between one PSTN line and two IOM buffers

SDR ADDRESS (HEX)	PARAMETER NAME		VALUE (HEX)	FUNCTION
00	LLa_IOM1	LLb_IOM1	5054	not used
01	LLa_LSW	LLb_LSW	FF00	LLa analog line interface (LLx_IOM1 not used)
02	LLa_LEC	LLb_LEC	FF00	Local Echo Canceller ON in Codec 1
03	LLa_NES	LLb_NES	2D00	Network Echo Suppressor (9 dB attenuation) in Codec 1
04	LLa_AGC	LLb_AGC	FF00	Automatic Gain Control ON in Codec 1
05	LLa_TXV	LLb_TXV	2000	Transmit Volume set to 0 dB in Codec 1
06	LLa_ISW	LLb_ISW	0000	8-bit A-law PCM data
07	LLa_IOM2	LLb_IOM2	484C	not used
08	LLa_SMU2	LLb_SMU2	0000	Soft Mute OFF
09	LLa_AVR	LLb_AVR	0000	Automatic Volume Control OFF
0A	LLa_RXV	LLb_RXV	2000	Receive Volume set to 0 dB in Codec 1
0B	LLa_PST	LLb_PST	0000	Site Tone OFF
0C	LLa_TST	LLb_TST	0000	Tone Site Tone OFF (LLx_TOGx and LLx_TOVx not used)
0D	LLa_TOV1	LLb_TOV1	4040	Tone Volume for Tone 1 set to 0 dB
0E	LLa_TOV2	LLb_TOV2	4040	Tone Volume for Tone 2 set to 0 dB
0F	LLa_TOG1		7ECE	Tone 1 to Codec 1
10	LLa_TOG2		7E8A	Tone 2 to Codec 1
11	LLb_TOG1		7E37	Tone 1 to Codec 2
12	LLb_TOG2		7DD2	Tone 2 to Codec 2
13	CCa_CNC	reserved	0900	conference call between Codec 1 and Codec 2 IOM buffers (8 bit A-law PCM data)
14	CCa_IOM3	CCa_IOM4	4044	conference call IOM buffer 1 at address 40H
				conference call IOM buffer 2 at address 44H
15	CCa_SMU3	CCa_SMU4	0000	soft mute off

Table 39 IOM control table for conference call between one PSTN line and two IOM buffers

SDR ADDRESS (HEX)	PARAMETER NAME	VALUE (HEX)	FUNCTION
20	slot 0 control	0070	IOM slot 0 uses buffer at address 40H
21	slot 1 control	0071	IOM slot 1 uses buffer at address 44H
22 to 3F	slot 2 to slot 32	0000	slots 2 to 32 inactive

Table 40 Control registers for conference call between one PSTN line and two IOM buffers

SDR ADDRESS (HEX)	PARAMETER NAME	VALUE (HEX)	FUNCTION
78	codec control	0003	Codec 1 ON, Codec 2 OFF
79	IOM control	0004	IOM slave mode, 768 kbits/s
7A	gain settings A/D and D/A paths	00D0	A/D gain = +9 dB, D/A gain = 0 dB in Codec 1
7B	VREF1, VREF2 settings	A0A0	default setting for VREF1 and VREF2
7C	DSP modes	0008	channel a in speech and tone mode

13.3 Conference call between two PSTN lines and one IOM buffer

Another configuration for conference call is between two PSTN lines and one IOM buffer, as shown in Fig.24. Tables 41, 42 and 43 show possible settings for the DSP parameters, the IOM control table and the control registers in the PCD5096.

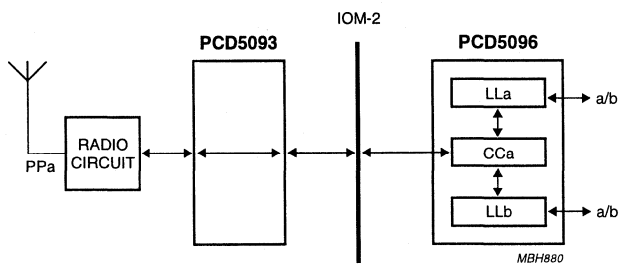


Fig.24 Conference call between two PSTN lines and one IOM buffer.

Table 41 DSP parameters for conference call between one IOM buffer and two PSTN lines

SDR ADDRESS (HEX)	PARAMETER NAME		VALUE (HEX)	FUNCTION
00	LLa_IOM1	LLb_IOM1	5054	not used
01	LLa_LSW	LLb_LSW	FFFF	2 × analog line interface (LLx_IOM1 not used)
02	LLa_LEC	LLb_LEC	FFFF	2 × Local Echo Canceller ON
03	LLa_NES	LLb_NES	2D2D	2 × Network Echo Suppressor (9 dB attenuation)
04	LLa_AGC	LLb_AGC	FFFF	2 × Automatic Gain Control ON
05	LLa_TXV	LLb_TXV	2020	2 × Transmit Volume set to 0 dB
06	LLa_ISW	LLb_ISW	0000	2 × 8-bit A-law PCM data
07	LLa_IOM2	LLb_IOM2	484C	not used
08	LLa_SMU2	LLb_SMU2	0000	2 × Soft Mute OFF
09	LLa_AVR	LLb_AVR	0000	2 × Automatic Volume Control OFF
0A	LLa_RXV	LLb_RXV	2020	2 × Receive Volume set to 0 dB
0B	LLa_PST	LLb_PST	0000	2 × Site Tone OFF
0C	LLa_TST	LLb_TST	0000	2 × Tone Site Tone OFF (LLx_TOGx and LLx_TOVx not used)
0D	LLa_TOV1	LLb_TOV1	4040	2 × Tone Volume for Tone 1 set to 0 dB
0E	LLa_TOV2	LLb_TOV2	4040	2 × Tone Volume for Tone 2 set to 0 dB
0F	LLa_TOG1		7ECE	Tone 1 to Codec 1
10	LLa_TOG2		7E8A	Tone 2 to Codec 1
11	LLb_TOG1		7E37	Tone 1 to Codec 2
12	LLb_TOG2		7DD2	Tone 2 to Codec 2
13	CCa_CNC	reserved	0100	conference call between Codec 1, Codec 2 and one IOM buffer (8 bit A-law PCM data)
14	CCa_IOM3	CCa_IOM4	4044	conference call with IOM buffer at address 40H CCa_IOM4 not used
15	CCa_SMU3	CCa_SMU4	0000	soft mute off

Table 42 IOM control table for conference call between one IOM buffer and two PSTN lines

SDR ADDRESS (HEX)	PARAMETER NAME	VALUE (HEX)	FUNCTION
20	slot 0 control	0070	IOM slot 0 uses buffer at address 40H
21 to 3F	slot 1 to slot 32	0000	slots 1 to 32 inactive

Table 43 Control registers for conference call between one IOM buffer and two PSTN lines

SDR ADDRESS (HEX)	PARAMETER NAME	VALUE (HEX)	FUNCTION
78	codec control	00FB	Codec 1 ON, Codec 2 ON with hands-free
79	IOM control	0004	IOM slave mode, 768 kbits/s
7A	gain settings A/D and D/A paths	D0D0	A/D gain = +9 dB, D/A gain = 0 dB for both channels
7B	VREF1, VREF2 settings	A0A0	default setting for VREF1 and VREF2
7C	DSP modes	0048	both channels run in speech and tone mode

14 LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD_1}	supply voltage V_{DD_1} with respect to V_{SS_1}	−0.5	+6.0	V
V_{DD_2}	supply voltage V_{DD_2} with respect to V_{SS_2}	−0.5	+5.0	V
V_{DDA_1}	analog supply voltage V_{DDA_1} with respect to V_{SSA_1}	−0.5	+5.0	V
V_{DDA_2}	analog supply voltage V_{DDA_2} with respect to V_{SSA_2}	−0.5	+5.0	V
V_{DD_PLL}	supply voltage V_{DD_PLL} with respect to V_{SS_PLL}	−0.5	+5.0	V
I_{DC}	DC current through pins			
	supply pins	−	150	mA
	other pins	−	10	mA
P_{tot}	total power dissipation	−	500	mW
T_{amb}	operating ambient temperature	−25	+70	°C
T_{stg}	storage temperature	−65	+150	°C

15 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. ESD protection according to Human Body Model is guaranteed up to 2 kV. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see *"Handling MOS Devices"*).

16 ELECTRICAL SPECIFICATIONS

Table 44 General parameters

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{clk}	clock frequency		–	6.912	–	MHz
T_{amb}	ambient temperature		–25	+25	+70	°C
V_{DD_1}	supply voltage	note 1	2.7	3.3	5.5	V
$I_{DD\_1(act)}$	active supply current	note 2	–	–	–	mA
$I_{DD\_1(off)}$	power off supply current	note 3	–	0.1	–	µA
V_{DD_2}	supply voltage	note 4	2.7	3.3	3.6	V
$I_{DD\_2(act)}$	active supply current	note 5	–	18	28	mA
$I_{DD\_2(off)}$	power off supply current	note 3	–	4	–	µA
V_{DDA_1}	analog supply voltage	note 4	2.7	3.3	3.6	V
$I_{DDA\_1(act)}$	active analog supply current	no load; notes 5 and 6	–	1.5	3	mA
$I_{DDA\_1(off)}$	power off supply current	note 3	–	33	–	µA
V_{DDA_2}	analog supply voltage	note 4	2.7	3.3	3.6	V
$I_{DDA\_2(act)}$	active analog supply current	no load; notes 5 and 6	–	1.5	3	mA
$I_{DDA\_2(off)}$	power off supply current	note 3	–	2	–	µA
V_{DD_PLL}	supply voltage	note 4	2.7	3.3	3.6	V
$I_{DD\_PLL(act)}$	active supply current	note 5	–	0.1	1	mA
$I_{DD\_PLL(off)}$	power off supply current	note 3	–	1	–	µA
$I_{DD(tot)(off)}$	total power off supply current	note 3	–	40	70	µA

Notes

1. V_{DD_1} supplies all digital I/Os to ensure 5 V interfacing. V_{DD_1} may vary over its range independent of the value of V_{DD_2}, V_{DDA_1}, V_{DDA_2} and V_{DD_PLL}. If V_{DD_1} is 5.5 V, V_{DD_2} cannot be lower than 3.0 V.
2. $I_{DD\_1(act)}$ is application dependent.
3. Power off at 25 °C and 3.3 V, RESET pin HIGH, clock not running. The pins IO0 and IO1 are then inputs and must be kept HIGH (internal pull-ups).
4. V_{DD_2}, V_{DDA_1}, V_{DDA_2} and V_{DD_PLL} will have the same value. Internally they are NOT connected.
5. Active mode at 25 °C and 3.3 V, clock running. DSP parameter table, IOM control table and control registers set according to Section 13.1 (application example with two active channels). A sine wave signal (1031.25 Hz) at a level of –25 dBm is applied to the microphone input of both codecs. DI is tied to DO to simulate activity on the IOM-2 interface.
6. No load on LIFM_DA1, LIFP_DA1, EARM_HS, EARP_HS, VBGP, VREF1, VREF2, VMIC_HS and VMIC_HF.

Table 45 Digital I/Os

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{LI}	leakage current input pins		–	–	1	µA
V_{IH}	HIGH-level input voltage		$0.7V_{DD\_1}$	–	–	V
V_{IL}	LOW-level input voltage		–	–	$0.3V_{DD\_1}$	V
V_{OH}	HIGH-level output voltage	note 1	$0.8V_{DD\_1}$	–	–	V
V_{OL}	LOW-level output voltage	notes 2 and 4	–	–	0.4	V
R_{pd}	equivalent pull-down resistor	note 3	–	50	–	kΩ
R_{pu}	equivalent pull-up resistor	note 3	–	100	–	kΩ
$t_{o(f)}$	SDA output fall time	notes 4 and 5	–	–	250	ns

Notes

1. I_{OH} = –8 mA for pins EARM_HF and EARP_HF. I_{OH} = –2 mA for pins IO0 and IO1.
2. I_{OL} = 8 mA for pins EARM_HF, EARP_HF and DO. I_{OL} = 2 mA for pins IO0 and IO1.
3. Pull-down resistor present at pin TEST. Pull-up resistor present at pins IO0 and IO1.
4. For SDA pin, I_{OL} = 3 mA at 5 V, 1 mA at 3.3 V and 0.7 mA at 2.7 V.
5. Output fall time of SDA measured from $V_{IH(min)}$ to $V_{IL(max)}$.

Table 46 Analog supplies

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{bgp}	bandgap voltage	note 1	1	1.2	1.5	V
V_{ref}	reference voltage	notes 2 and 3	1.975	2.000	2.025	V
R_{vmic}	microphone supply output resistance	note 4	–	75	150	Ω

Notes

1. VBGP output current is zero. Decoupling capacitance between pins VBGP and V_{SSA_1} is 100 nF at 25 °C. The bandgap has a temperature coefficient between –0.2 and +0.2 mV/°C.
2. V_{ref} stands for VREF1 or VREF2. V_{ref} output current is zero. Decoupling capacitance between VREF1 and V_{SSA_1}, or between VREF2 and V_{SSA_2} is between 1 µF and 100 µF, with a 100 nF capacitance in parallel. The voltage is programmed by setting the appropriate value (80H to BFH) for each codec, in Control Register 3. VMIC_HS and VMIC_HF output current is zero (e.g. by setting bits 6 and 7 in Control Register 3 to a logic 0. The output can only source current (i.e. not sink).
3. Pins VMIC_HS and VMIC_HF (called VMIC below) are internally connected to VREF2 via two switches. The VMIC_HS switch is closed by setting the HSMICON bit in Control Register 0 to a logic 1. The VMIC_HF switch is closed by setting the HFMICON bit in Control Register 0 to a logic 1. The VMIC DC output current is 400 µA maximum, and VREF2 must be programmed to its typical value. Use a low pass filter (resistor + capacitor) between VMIC and V_{SSA_2} of 100 Ω + 10 µF, with a 100 nF capacitance in parallel. VMIC adjustment can only be done by adjusting VREF2.
4. Valid for both VMIC_HS and VMIC_HF pins.

Table 47 Speech codec

V_{ref1} and V_{ref2} are tuned to 2.0 V. Typical values for the A/D and D/A filter characteristics conform to the G.712 specification.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{i(MIC1)}$	MIC input level (Codec 1)	note 1	–	–	–22	dBm
$V_{i(MIC\_HS)}$	handset MIC input level (Codec 2)	note 1	–	–	–22	dBm
$V_{i(MIC\_HF)}$	hands-free MIC input level (Codec 2)	note 1	–	–	–22	dBm
$R_{i(MIC1)(dm)}$	MIC input resistance differential mode seen across MICP1 and MICM1		–	200	–	kΩ
$R_{i(MIC\_HS)(dm)}$	handset MIC input resistance differential mode seen across MICP_HS and MICM_HS		–	200	–	kΩ
$R_{i(MIC\_HF)(dm)}$	hands-free MIC input resistance differential mode seen across MICP_HF and MICM_HF		–	200	–	kΩ
$R_{i(MIC1)(cm)}$	MIC input resistance common mode seen between MICP1 (or MICM1) and V_{SSA_1}		–	500	–	kΩ
$R_{i(MIC\_HS)(cm)}$	handset MIC input resistance common mode seen between MICP_HS (or MICM_HS) and V_{SSA_2}		–	500	–	kΩ
$R_{i(MIC\text{-}HF)(cm)}$	hands-free MIC input resistance common mode seen between MICP_HF (or MICM_HF) and V_{SSA_2}		–	500	–	kΩ
$V_{i(LIF\_AD1)}$	LIF input level (Codec 1)	note 2	–	–	–6	dBm
$V_{i(LIF\_AD2)}$	LIF input level (Codec 2)	note 2	–	–	–6	dBm
$R_{i(LIF\_AD1)(dm)}$	LIF input resistance differential mode seen across LIFP_AD1 and LIFM_AD1		–	30	–	kΩ
$R_{i(LIF\_AD2)(dm)}$	LIF input resistance differential mode seen across LIFP_AD2 and LIFM_AD2		–	30	–	kΩ
$R_{i(LIF\_AD1)(cm)}$	LIF input resistance common mode seen between LIFP_AD1 (or LIFM_AD1) and V_{SSA_1}		–	15	–	kΩ
$R_{i(LIF\_AD2)(cm)}$	input resistance common mode seen between LIFP_AD2 (or LIFM_AD2) and V_{SSA_2}		–	15	–	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$F_{(A/D)(idle)}$	A/D idle channel noise	note 3	–	–85	–72	dBm0p
$S/(N + THD)_{(A/D)(65)}$	A/D signal-to-noise plus total harmonic distortion ratio (–65 dBm input level)	note 4	32	40	–	dBp
$S/(N + THD)_{(A/D)(25)}$	A/D signal-to-noise plus total harmonic distortion ratio (–25 dBm input level)	note 4	40	60	–	dBp
$t_{d(g)(A/D)}$	A/D path group delay		–	500	–	µs
$G_{(MIC1)}$	Codec 1 MIC gain from MICP1 - MICM1 to LIFP_AD1 - LIFM_AD1		12	15	18	dB
$G_{(MIC\_HS)}$	Codec 2 handset MIC gain from MICP_HS - MICM_HS to LIFP_AD2 - LIFM_AD2		12	15	18	dB
$G_{(MIC\_HF)}$	Codec 2 hands-free MIC gain from MICP_HF - MICM_HF to LIFP_AD2 - LIFM_AD2		12	15	18	dB
$G_{(A/D)}$	gain A/D path from LIF to PCM	note 5	$G_{AD} - 1.5$	G_{AD}	$G_{AD} + 1.5$	dB
$G_{step(A/D)}$	gain difference between adjacent steps (A/D path)	note 6	+0.1	+1.0	+1.9	dB
$G_{(D/A)}$	gain D/A path from PCM to LIF	note 7	$G_{DA} - 1$	G_{DA}	$G_{DA} + 1$	dB
$G_{step(D/A)}$	gain difference between adjacent steps (D/A path)	note 6	+0.5	+1.0	+1.5	dB
$V_{o(D/A)}$	D/A path output level	note 8	–	1350	–	mV
$R_{o(D/A\_1)}$	D/A path output resistance seen between LIFP_DA1 and LIFM_DA1		–	10	20	Ω
$R_{o(D/A\_2)}$	D/A path output resistance seen between EARP_HS and EARM_HS		–	10	20	Ω
$F_{(D/A)(idle)}$	D/A idle channel noise	note 9	–	–85	–72	dBmp
$S/(N + THD)_{(D/A)(40)}$	D/A signal-to-noise plus total harmonic distortion ratio (–40 dBm0 input level)	note 10	32	40	–	dBp
$S/(N + THD)_{(D/A)(0)}$	D/A signal-to-noise plus total harmonic distortion ratio (0 dBm0 input level)	notes 10 and 11	40	70	–	dBp
$t_{d(g)(D/A)}$	D/A-path group delay		–	500	–	µs

Notes

1. A sine wave rms level applied differentially between the microphone pins. The A/D path gain in Control Register 2 is set to +9 dB. For larger input levels the output signal will saturate.
2. A sine wave rms level applied differentially between pins LIFP_ADn and LIFM_ADn (n = 1 for Codec 1; n = 2 for Codec 2). The A/D path gain is set to +9 dB using Control Register 2. For larger input levels the output signal will saturate.
3. Valid for Codec 1 and Codec 2. Control Register 0 = 0003H (Codec 1) or 0018H (Codec 2) and the A/D path gain in Control Register 2 is set to +9 dB. The microphone pins are shorted together. The value is psophometrically weighted.
4. Valid for Codec 1 and Codec 2. Control Register 0 = 0003H (Codec 1) or 0018H (Codec 2) and the A/D path gain in Control Register 2 is set to +9 dB. A sine wave of 1030 Hz is applied between the microphone input pins. The value is psophometrically weighted and includes harmonic distortion.
5. Valid for Codec 1 and Codec 2. G_{AD} is the A/D gain value selected in Control Register 2. The gain is measured at 1030 Hz from the LIF interface (pins LIFP_ADn and LIFM_ADn, where n = 1 for Codec 1 and n = 2 for Codec 2) to the PCM interface.
6. The difference between two adjacent gain settings as specified in Control Register 2. Valid for Codec 1 and Codec 2.
7. Valid for Codec 1 and Codec 2. G_{DA} is the D/A gain value selected in Control Register 2. The gain is measured at 970 Hz, from the PCM interface to the LIF interface (pins LIFP_DA1 and LIFM_DA1, for Codec 1 and pins EARP_HS and EARM_HS for Codec 2).
8. Valid for Codec 1 and Codec 2. Sine wave rms level differentially seen between pins LIFP_DA1 and LIFM_DA1 (Codec 1) or EARP_HS and EARM_HS (Codec 2), with an input signal of 970 Hz and a level of +3.14 dBm0 at the PCM interface. Load resistance is larger than 120 Ω. The D/A path gain in Control Register 2 is set to +2 dB.
9. Valid for Codec 1 and Codec 2. Control Register 0 = 0003H (Codec 1) or 0018H (Codec 2). The D/A path gain in Control Register 2 is set to 0 dB and the DSP is set to idle mode. The value is psophometrically weighted.
10. Valid for Codec 1 and Codec 2. Control Register 0 = 0003H (Codec 1) or 0018H (Codec 2).The D/A path gain in Control Register 2 is set to 0 dB. A sine wave of 970 Hz is applied. The value is psophometrically weighted and includes harmonic distortion.
11. The D/A path is loaded with (150 Ω + 800 μF)//100 pF.

Threshold detector and reset generator PCF1252-X family

FEATURES

- Very low current consumption, typically 10 μA
- 10 factory programmed threshold voltages available covering trip voltages from 4.75 to 2.55 V
- ±50 mV trip point accuracy over full temperature range
- Variable RESET delay
- RESET pulse polarity selection
- Defined outputs at 0.6 V (typ.)
- Comparator for second level detection (e.g. overvoltage detection)
- Advance warning of power fail
- Operating temperature range –40 to +85 °C.

GENERAL DESCRIPTION

The PCF1252-Xs are low-power CMOS voltage threshold detectors designed especially for supervision of microcontroller/microprocessor systems for detection of power-on/off conditions and generation of a system reset pulse. The PCF1252-X also provides a $\overline{\text{POWF}}$ (power fail) output which is activated at a precise factory-programmed trip point. A system RESET output has a built-in delay with duration determined by an external capacitor (C_{CT}).

A second comparator (comparator 2) has been included to enable the possibility of a second monitoring point in the system.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF1252-XP[1]	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
PCF1252-XT[1]	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

Note

1. X = 0 to 9; depending on threshold voltage.

BLOCK DIAGRAM

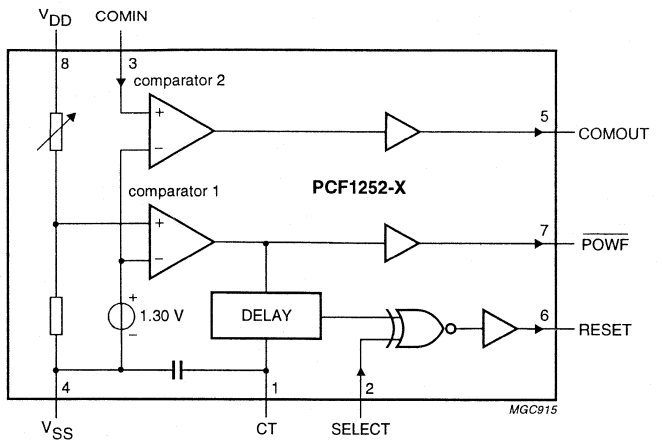


Fig.25 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
CT	1	connection for the external capacitor
SELECT	2	select polarity or external reset input
COMIN	3	comparator input
V_{SS}	4	ground (0 V)
COMOUT	5	comparator output
RESET	6	reset output
$\overline{POWF}$	7	power failure signal output
V_{DD}	8	supply voltage

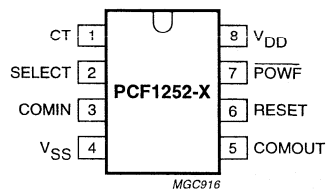


Fig.26 Pinning diagram.

LCD controller/driver PCF2104x

FEATURES

- Single chip LCD controller/driver
- 1 or 2-line display of up to 24 characters per line, or 2 or 4 lines of up to 12 characters per line
- 5 × 7 character format plus cursor; 5 × 8 for kana (Japanese syllabary) and user-defined symbols
- On-chip:
  - generation of intermediate LCD bias voltages
  - oscillator requires no external components (external clock also possible)
- Display data RAM: 80 characters
- Character generator ROM: 240 characters
- Character generator RAM: 16 characters
- 4 or 8-bit parallel bus or 2-wire I²C-bus interface
- CMOS/TTL compatible
- 32 row, 60 column outputs
- MUX rates 1 : 32 and 1 : 16
- Uses common 11 code instruction set
- Logic supply voltage range, $V_{DD} - V_{SS}$: 2.5 to 6 V
- Display supply voltage range, $V_{DD} - V_{LCD}$: 3.5 to 9 V
- Low power consumption.
- I²C-bus address: 011101 SA0.

APPLICATIONS

- Telecom equipment
- Portable instruments
- Point-of-sale terminals.

GENERAL DESCRIPTION

The PCF2104x integrated circuit is similar to the PCF2114x (described in the *"PCF2116 family"* data sheet) but does not contain the high voltage generator of that device.

The PCF2104x is optimized for chip-on-glass applications. The 'x' in 'PCF2104x' represents a specific letter code for a character set in the character generator ROM (CGROM).

Two standard character sets are currently available, specified by the letters 'C' and 'L'. Other character sets are available on request.

The PCF2104x is a low-power CMOS LCD controller and driver, designed to drive a split screen dot matrix LCD display of 1 or 2 lines by 24 characters or 2 or 4 lines by 12 characters with a 5 × 8 dot format. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD bias voltages which results in a minimum of external components and lower system power consumption. To allow partial V_{DD} shutdown the ESD protection system of the SCL and SDA pins does not use a diode connected to V_{DD}.

The chip contains a character generator and displays alphanumeric and kana characters. The PCF2104x interfaces to most microcontrollers via a 4 or 8-bit bus, or via the 2-wire I²C-bus.

Packages

- PCF2104xU/2; chip with bumps in tray.

Available types

- PCF2104CU/2: character set 'C' in CGROM
- PCF2104LU/2: character set 'L' in CGROM.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF2104CU/2	–	chip with bumps in tray	–
PCF2104LU/2	–	chip with bumps in tray	–

Full Data Sheet: on CD-ROM/WWW (Internet) or FOD-system (details in front Section/back of this HB), or updated Loose leaf or Parent HB

BLOCK DIAGRAM

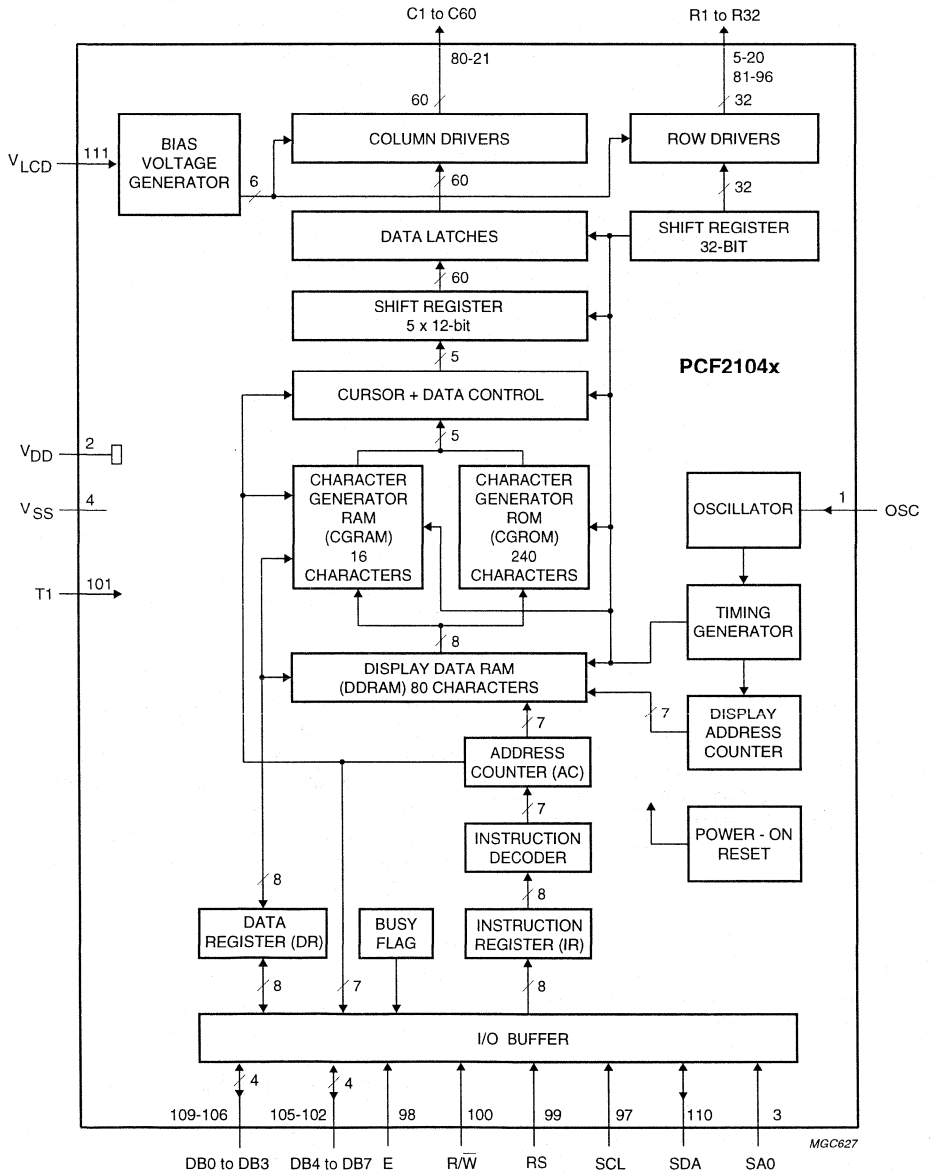


Fig.27 Block diagram.

PINNING

SYMBOL	FFC PAD	TYPE	DESCRIPTION
OSC	1	I	oscillator/external clock input
V_{DD}	2	P	logic supply voltage
SA0	3	I	I²C-bus address pin input
V_{SS}	4	P	ground
R8 to R5	5 to 8	O	LCD row driver outputs
R32 to R29	9 to12	O	LCD row driver outputs
R24 to R17	13 to 20	O	LCD row driver outputs
C60 to C1	21 to 80	O	LCD column driver outputs
R9 to R16	81 to 88	O	LCD row driver outputs
R25 to R28	89 to 92	O	LCD row driver outputs
R1 to R4	93 to 96	O	LCD row driver outputs
SCL	97	I	I²C-bus serial clock input
E	98	I	data bus clock input
RS	99	I	register select input
R/$\overline{W}$	100	I	read/write input
T1	101	I	test pad input
DB7 to DB0	102 to 109	I/O	8-bit bidirectional data bus input/output
SDA	110	I/O	I²C-bus serial data input/output
V_{LCD}	111	I	LCD supply voltage input

PIN FUNCTIONS

RS: register select (parallel control)

RS selects the register to be accessed for read and write when the device is controlled by the parallel interface. RS = logic 0 selects the instruction register for write and the Busy Flag and Address Counter for read. RS = logic 1 selects the data register for both read and write. There is an internal pull-up on pin RS.

R/$\overline{W}$: read/write (parallel control)

R/$\overline{W}$ selects either the read (R/$\overline{W}$ = logic 1) or write (R/$\overline{W}$ = logic 0) operation when control is by the parallel interface. There is an internal pull-up on this pin.

E: data bus clock (parallel control)

The E pin is set HIGH to signal the start of a read or write operation when the device is controlled by the parallel interface. Data is clocked in or out of the chip on the negative edge of the clock. Note that this pin must be tied to logic 0 (V_{SS}) when I²C-bus control is used.

DB0 to DB7: data bus (parallel control)

The bidirectional, 3-state data bus transfers data between the system controller and the PCF2104x. DB7 may be used as the Busy Flag, signalling that internal operations are not yet completed. In 4-bit operations the 4 higher order lines DB4 to DB7 are used; DB0 to DB3 must be left open circuit. There is an internal pull-up on each of the data lines. Note that these pins must be left open circuit when I²C-bus control is used.

C1 to C60: column driver outputs

These pins output the data for pairs of columns. This arrangement permits optimized chip-on-glass (COG) layout for 4-line by 12 characters.

R1 to R32: row driver outputs

These pins output the row select waveforms to the left and right halves of the display.

V_{LCD}: LCD power supply

Negative power supply for the liquid crystal display.

OSC: oscillator

When the on-chip oscillator is used, this pin must be connected to V_{DD}. An external clock signal, if used, is input at this pin.

SCL: serial clock line

Input for the I^2C-bus clock signal.

SDA: serial data line

Input/output for the I^2C-bus data line.

SA0: address pin

The hardware sub-address line is used to program the device sub-address for 2 different PCF2104xs on the same I^2C-bus.

T1: test pad

Must be connected to V_{SS}. Not user accessible.

LCD controller/driver PCF2113x

FEATURES

- Single-chip LCD controller/driver
- 2-line display of up to 12 characters + 120 icons, or 1-line display of up to 24 characters + 120 icons
- 5 × 7 character format plus cursor; 5 × 8 for kana (Japanese syllabary) and user defined symbols
- Icon mode: reduced current consumption while displaying icons only(1)
- Icon blink function
- On-chip:
  - generation of LCD supply voltage, programmable by instruction (external supply also possible)
  - temperature compensation of on-chip generated V_{LCD}: –8 to –12 mV/K at 5.0 V (programmable by instruction)
  - generation of intermediate LCD bias voltages
  - oscillator requires no external components (external clock also possible)
- Display data RAM: 80 characters
- Character generator ROM: 240, 5 × 8 characters
- Character generator RAM: 16, 5 × 8 characters; 3 characters used to drive 120 icons, 6 characters used if icon-blink feature is used in application
- 4 or 8-bit parallel bus and 2-wire I²C-bus interface
- CMOS compatible
- 18 row, 60 column outputs
- MUX rates 1 : 18 (for normal operation) and 1 : 2 (for icon-only mode)
- Uses common 11 code instruction set (extended)
- Logic supply voltage range, $V_{DD} - V_{SS}$ = 1.8 to 4.0 V (up to 5.5 V if external V_{LCD} is used); chip may be driven with two battery cells
- Display supply voltage range, $V_{LCD} - V_{SS}$ = 2.2 to 6.5 V
- Very low current consumption (20 to 200 μA):
  - icon mode: <25 μA
  - power-down mode: <2.5 μA.

APPLICATIONS

- Telecom equipment
- Portable instruments
- Point-of-sale terminals.

GENERAL DESCRIPTION

The PCF2113x is a low power CMOS LCD controller and driver, designed to drive a dot matrix LCD display of 2 line by 12 and 1 line by 24 characters with 5 × 8 dot format. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD bias voltages, resulting in a minimum of external components and lower system current consumption. The PCF2113x interfaces to most microcontrollers via a 4 or 8-bit bus or via the 2-wire I²C-bus. The chip co cter sets (A, D and E) are currently available. Various other character sets can be manufactured on request.

(1) Icon mode is used to save current. When only icons are displayed, a much lower operating voltage V_{LCD} can be used and the switching frequency of the LCD outputs is reduced. In most applications it is possible to use V_{DD} as V_{LCD}. Never use the voltage generator in icon mode.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF2113AU/10/F2	–	chip on flexible film carrier	–
PCF2113DU/10/F2	–	chip on flexible film carrier	–
PCF2113DU/F2	–	chip in tray	–
PCF2113DH/F2	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
PCF2113EU/2/F2	–	chip with bumps in tray	–

BLOCK DIAGRAM

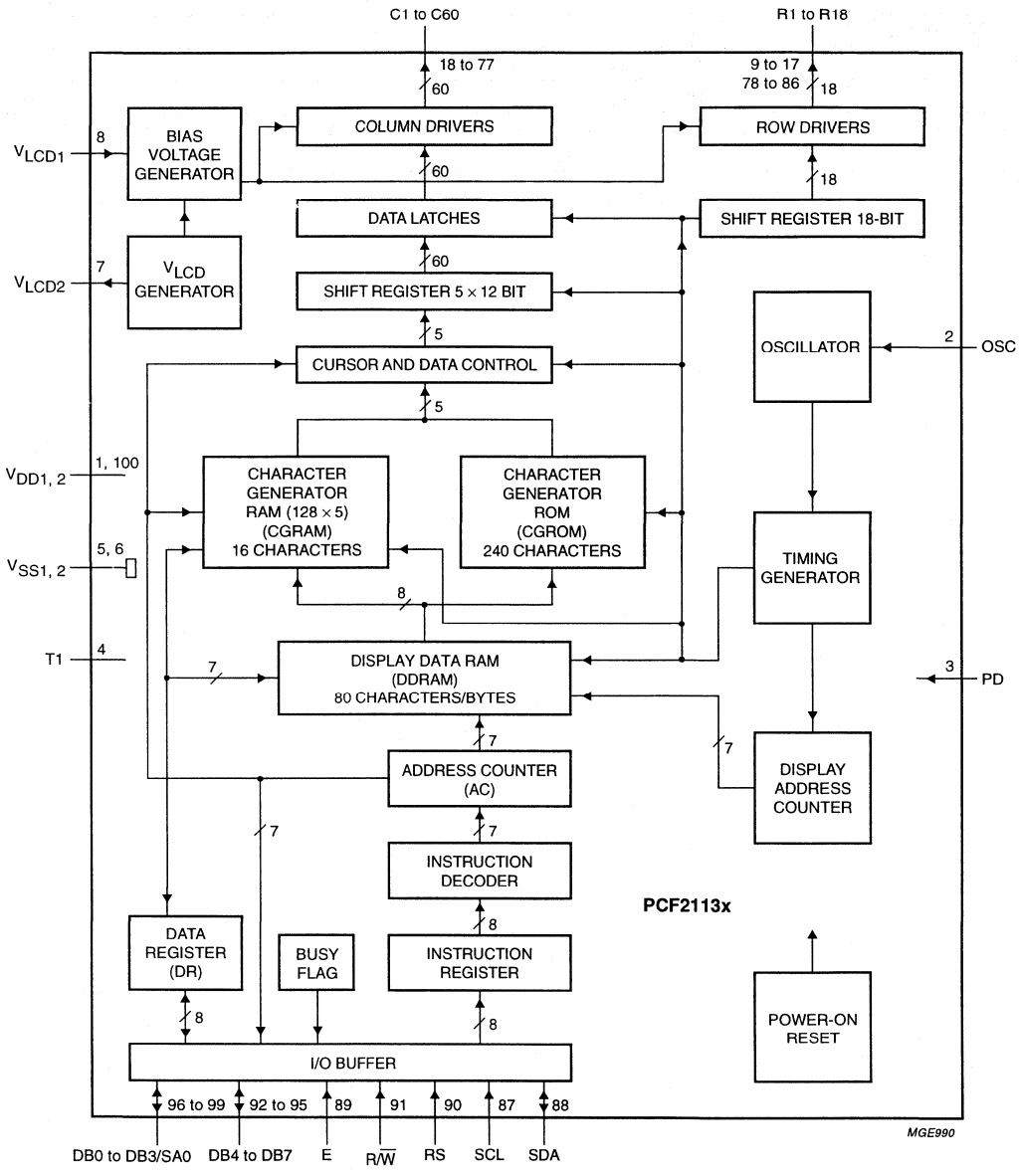


Fig.28 Block diagram.

PINNING

SYMBOL	PIN	TYPE	DESCRIPTION
V_{DD1}	1	P	supply voltage for all except high voltage generator
OSC	2	I	oscillator/external clock input
PD	3	I	power-down pad input
T1	4	I	test pad (connected to V_{SS})
V_{SS1}	5	P	ground for all except high voltage generator
V_{SS2}	6	P	ground for high voltage generator
V_{LCD2}	7	O	V_{LCD} output; note 1
V_{LCD1}	8	I	V_{LCD} input; note 2
R9 to R16	9 to 16	O	LCD row driver outputs 9 to 16
R18	17	O	LCD row driver output 18
C60 to C1	18 to 77	O	LCD column driver outputs 60 to 1
R8 to R1	78 to 85	O	LCD row driver outputs 8 to 1
R17	86	O	LCD row driver output 17
SCL	87	I	I^2C serial clock input
SDA	88	I/O	I^2C serial data input/output
E	89	I	data bus clock input
RS	90	I	register select input
R/$\overline{W}$	91	I	read/write input
DB7	92	I/O	1 bit of 8-bit bidirectional data bus
DB6	93	I/O	1 bit of 8-bit bidirectional data bus
DB5	94	I/O	1 bit of 8-bit bidirectional data bus
DB4	95	I/O	1 bit of 8-bit bidirectional data bus
DB3/SA0	96	I/O	1 bit of 8-bit bi-directional data bus/I^2C address pin
DB2	97	I/O	1 bit of 8-bit bidirectional data bus
DB1	98	I/O	1 bit of 8-bit bidirectional data bus
DB0	99	I/O	1 bit of 8-bit bidirectional data bus
V_{DD2}	100	P	supply voltage for high voltage generator; note 3

Notes

1. This is the V_{LCD} output pin, if V_{LCD} is generated internally and has to be connected to V_{LCD1}. If V_{LCD1} is generated externally, V_{LCD2} has to be left open or connected to ground.
2. This is the voltage used for the generation of LCD bias levels.
3. This is the supply for the high voltage generator. If V_{LCD} is generated externally, connect V_{DD2} to V_{SS}.

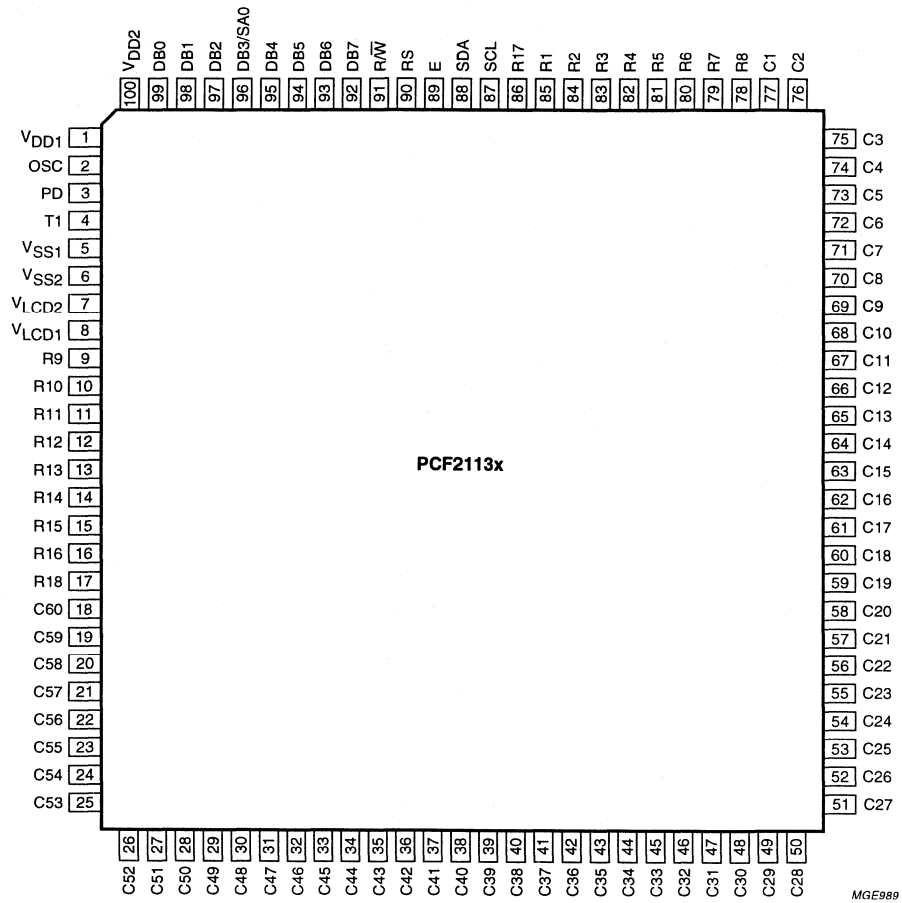


Fig.29 Pin configuration (LQFP100).

PIN FUNCTIONS

NAME	FUNCTION	DESCRIPTION
RS	register select	RS selects the register to be accessed for read and write when the device is controlled by the parallel interface. There is an internal pull-up on this pin. RS = logic 0 selects the instruction register for write and the Busy Flag and Address Counter for read. RS = logic 1 selects the data register for both read and write.
R/$\overline{W}$	read/write	R/$\overline{W}$ selects either the read (R/$\overline{W}$ = logic 1) or write (R/$\overline{W}$ = logic 0) operation when the device is controlled by the parallel interface. There is an internal pull-up on this pin.
E	data bus clock	The E pin is set HIGH to signal the start of a read or write operation when the device is controlled by the parallel interface. Data is clocked in or out of the chip on the negative edge of the clock. Note that this pin must be tied to logic 0 (V_{SS}) when I^2C-bus control is used.
DB7 to DB0	data bus	The parallel interface of the device. This bi-directional, 3-state data bus transfers data between the system controller and the PCF2113x. There is an internal pull-up on each of the data lines. DB7 to DB0 must be connected to V_{DD} or left open circuit when I^2C-bus control is used. Note that DB3 shares the same pin as SA0. In 4-bit operations only DB7 to DB4 are used, and DB3 to DB0 must be left open circuit. See note 1. DB7 may be used as the Busy Flag, signalling that internal operations are not yet completed.
C1 to C60	column driver outputs	These pins output the data for columns.
R1 to R18	row driver outputs	These pins output the row select waveforms to the display. R17 and R18 drive the icons.
V_{LCD}	LCD power supply	Positive power supply for the liquid crystal display. This may be generated on-chip or supplied externally.
OSC	oscillator	When the on-chip oscillator is used this pin must be connected to V_{DD}. An external clock signal, if used, is input at this pin.
SCL	serial clock line	Input for the I^2C-bus clock signal. SCL must be connected to V_{SS} or V_{DD} when the parallel interface is used.
SDA	serial data line	I/O for the I^2C-bus data line. SDA must be connected to V_{SS} or V_{DD} when the parallel interface is used.
SA0	address pin	The hardware sub-address line is used to program the device sub-address for two different PCF2113xs on the same I^2C bus. Note that SA0 shares the same pin as DB3.
T1	test pad	T1 must be connected to V_{SS} and is not user accessible.
PD	power-down pad	PD selects chip power-down mode. For normal operation PD = logic 0.

Note

1. If the 4-bit interface is used without reading out from the PCF2113x (i.e. R/$\overline{W}$ is set permanently to logic 0), the unused ports DB0 to DB3 can either be set to V_{SS} or V_{DD} instead of leaving them open.

LCD controller/drivers PCF2116 family

FEATURES

- Single chip LCD controller/driver
- 1 or 2-line display of up to 24 characters per line, or 2 or 4 lines of up to 12 characters per line
- 5 × 7 character format plus cursor; 5 × 8 for kana (Japanese syllabary) and user defined symbols
- On-chip:
  - generation of LCD supply voltage (external supply also possible)
  - generation of intermediate LCD bias voltages
  - oscillator requires no external components (external clock also possible)
- Display data RAM: 80 characters
- Character generator ROM: 240 characters
- Character generator RAM: 16 characters
- 4 or 8-bit parallel bus or 2-wire I²C-bus interface
- CMOS/TTL compatible
- 32 row, 60 column outputs
- MUX rates 1 : 32 and 1 : 16
- Uses common 11 code instruction set
- Logic supply voltage range, $V_{DD} - V_{SS}$: 2.5 to 6 V
- Display supply voltage range, $V_{DD} - V_{LCD}$: 3.5 to 9 V
- Low power consumption
- I²C-bus address: 011101 SA0.

APPLICATIONS

- Telecom equipment
- Portable instruments
- Point-of-sale terminals.

GENERAL DESCRIPTION

The PCF2116 family of LCD controller/drivers consists of the PCF2116x, the PCF2114x and the PCF2116K. The term 'PCF2116' is used to refer to all devices for common information. Specific information is given in separate paragraphs.

The 'x' in 'PCF2116x' and 'PCF2114x' represents a specific letter code for a character set in the character generator ROM (CGROM). The different character sets currently available are specified by the letters A, C, and G. Other character sets are available on request.

The PCF2116 is a low-power CMOS LCD controller and driver, designed to drive a split screen dot matrix LCD display of 1 or 2 lines by 24 characters or 2 or 4 lines by 12 characters with 5 × 8 dot format. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD bias voltages, resulting in a minimum of external components and lower system power consumption. The chip contains a character generator and displays alphanumeric and kana (Japanese) characters. The PCF2116 interfaces to most microcontrollers via a 4 or 8-bit bus or via the 2-wire I²C-bus. To allow partial V_{DD} shutdown the ESD protection system of the SCL and SDA pins does not use a diode connected to V_{DD}.

The PCF2116K differs from the other members of the family in that:

- V_{LCD}/V_{OP} generation is different
- It is available with character set C only.

Full Data Sheet: on CD-ROM/WWW (Internet) or FOD-system (details in front Section/back of this HB), or updated Loose leaf or Parent HB

ORDERING INFORMATION

TYPE NUMBER[1]	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF2116xU/10	–	chip on flexible film carrier	–
PCF2114xU/10	–	chip on flexible film carrier	–
PCF2116xU/12	–	chip with bumps on flexible film carrier	–
PCF2114xU/12	–	chip with bumps on flexible film carrier	–
PCF2116xHZ	LQFP128	plastic low profile quad flat package; 128 leads; body 14 × 20 × 1.4 mm	SOT425-1

Note

1. The letter 'x' in the type number represents the letter of the required built-in character set: A, C or G.

BLOCK DIAGRAM

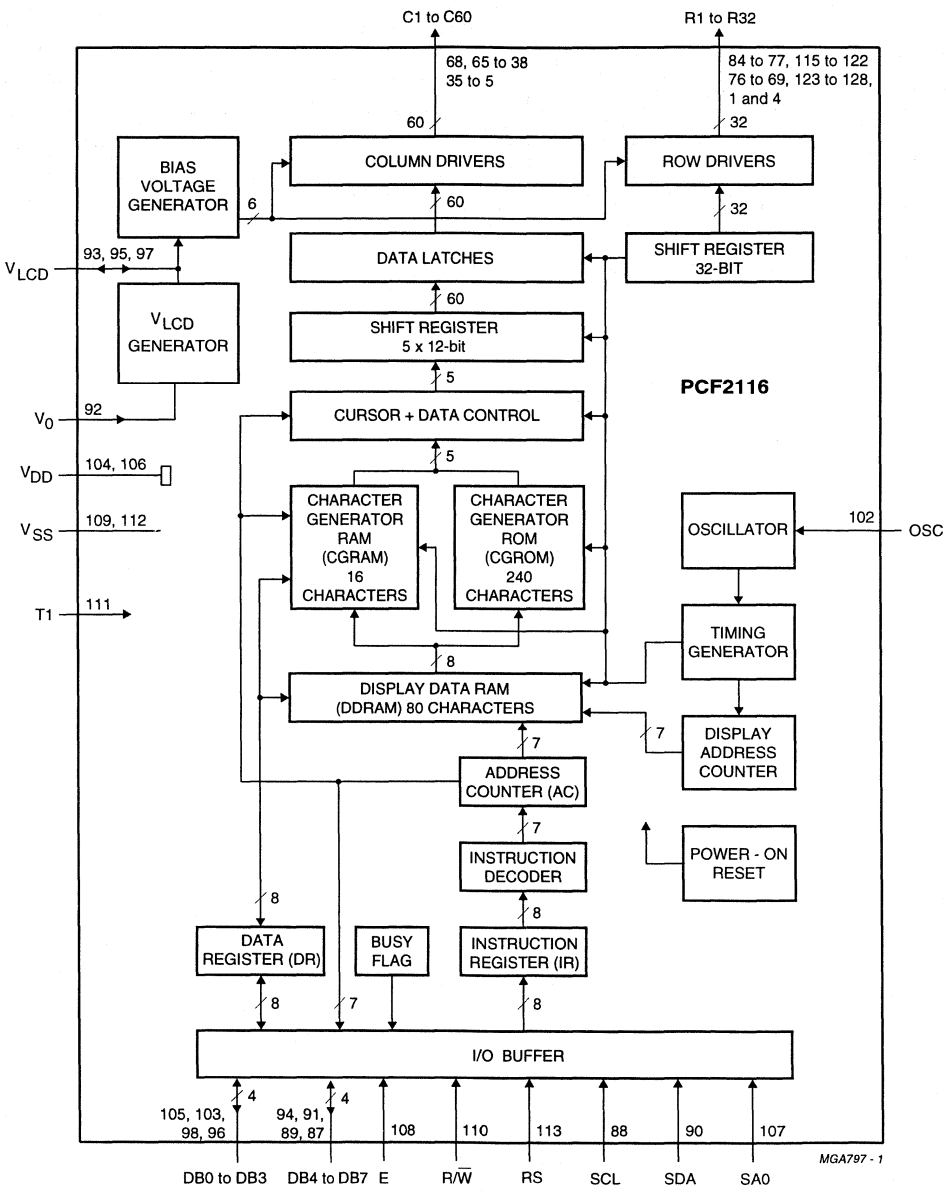


Fig.30 Block diagram (pin numbers for LQFP128 package).

PINNING

SYMBOL	LQFP128	FFC PAD	TYPE	DESCRIPTION
R31	1	27	O	LCD row driver output
n.c.	2 and 3	–	–	not connected
R32	4	28	O	LCD row driver output
C60 to C30	5 to 35	29 to 59	O	LCD column driver outputs 60 to 30
n.c.	36 and 37	–	–	not connected
C29 to C2	38 to 65	60 to 87	O	LCD column driver outputs 29 to 2
n.c.	66 and 67	–	–	not connected
C1	68	88	O	LCD column driver output 1
R24 to R17	69 to 76	89 to 96	O	LCD row driver outputs
R8 to R1	77 to 84	97 to 104	O	LCD row driver outputs
n.c.	85 and 86	–	–	not connected
DB7	87	105	I/O	1 bit of 8-bit bidirectional data bus
SCL	88	106	I	I^2C-bus serial clock input
DB6	89	107	I/O	1 bit of 8-bit bidirectional data bus
SDA	90	108	I/O	I^2C-bus serial data input/output
DB5	91	109	I/O	1 bit of 8-bit bidirectional data bus
V_0	92	110	I	control input for V_{LCD}
V_{LCD1}	93	111	I/O	LCD supply voltage input/output 1
DB4	94	112	I/O	1 bit of 8-bit bidirectional data bus
V_{LCD2}	95	113	I/O	LCD supply voltage input/output 2
DB3	96	114	I/O	1 bit of 8-bit bidirectional data bus
V_{LCD3}	97	115	I/O	LCD supply voltage input/output 3
DB2	98	116	I/O	1 bit of 8-bit bidirectional data bus
n.c.	99 to 101	–	–	not connected
OSC	102	1	I	oscillator/external clock input
DB1	103	2	I/O	1 bit of 8-bit bidirectional data bus
V_{DD2}	104	3	P	supply voltage 2
DB0	105	4	I/O	1 bit of 8-bit bidirectional data bus
V_{DD1}	106	5	P	supply voltage 1
SA0	107	6	I	I^2C-bus address pin
E	108	7	I	data bus clock input (parallel control)
V_{SS1}	109	8	P	ground (logic) 1
$R/\overline{W}$	110	9	I	read/write input (parallel control)
T1	111	10	I	test pad (connect to V_{SS})
V_{SS2}	112	11	P	ground (logic) 2
RS	113	12	I	register select input (parallel control)
n.c.	114	–	–	not connected
R9 to R16	115 to 122	13 to 20	O	LCD row driver outputs
R25 to R30	123 to 128	21 to 26	O	LCD row driver outputs

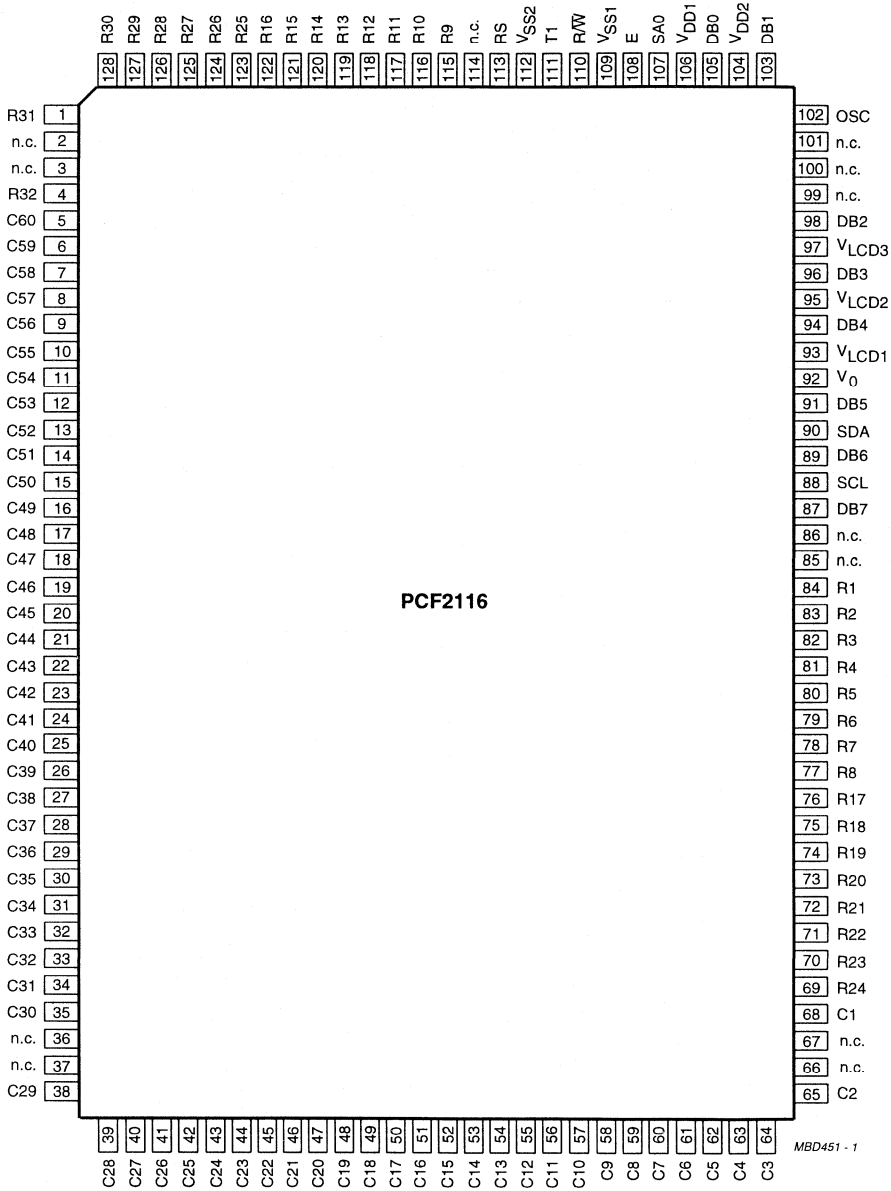


Fig.31 Pin configuration (LQFP128).

PIN FUNCTIONS

RS: register select (parallel control)

RS selects the register to be accessed for read and write when the device is controlled by the parallel interface. RS = logic 0 selects the instruction register for write and the Busy Flag and Address Counter for read. RS = logic 1 selects the data register for both read and write. There is an internal pull-up on pin RS.

R/$\overline{W}$: read/write (parallel control)

R/$\overline{W}$ selects either the read (R/$\overline{W}$ = logic 1) or write (R/$\overline{W}$ = logic 0) operation when control is by the parallel interface. There is an internal pull-up on this pin.

E: data bus clock

The E pin is set HIGH to signal the start of a read or write operation when the device is controlled by the parallel interface. Data is clocked in or out of the chip on the negative edge of the clock. Note that this pin must be tied to logic 0 (V_{SS}) when I^2C-bus control is used.

DB0 to DB7: data bus

The bidirectional, 3-state data bus transfers data between the system controller and the PCF2116. DB7 may be used as the Busy Flag, signalling that internal operations are not yet completed. In 4-bit operations the 4 higher order lines DB4 to DB7 are used; DB0 to DB3 must be left open circuit. There is an internal pull-up on each of the data lines. Note that these pins must be left open circuit when I^2C-bus control is used.

C1 to C60: column driver outputs

These pins output the data for pairs of columns. This arrangement permits optimized chip-on-glass (COG) layout for 4-line by 12 characters.

R1 to R32: row driver outputs

These pins output the row select waveforms to the left and right halves of the display.

V_{LCD}: LCD power supply

Negative power supply for the liquid crystal display. This may be generated on-chip or supplied externally.

V_0: V_{LCD} control input

The input level at this pin determines the generated V_{LCD} output voltage.

OSC: oscillator

When the on-chip oscillator is used this pin must be connected to V_{DD}. An external clock signal, if used, is input at this pin.

SCL: serial clock line

Input for the I^2C-bus clock signal.

SDA: serial data line

Input/output for the I^2C-bus data line.

SA0: address pin

The hardware sub-address line is used to program the device sub-address for 2 different PCF2116s on the same I^2C-bus.

T1: test pad

Must be connected to V_{SS}. Not user accessible.

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1 FEATURES

- Single-chip LCD controller/driver
- 2-line display of up to 16 characters + 160 icons, or 1-line display of up to 32 characters + 160 icons
- 5 × 7 character format plus cursor; 5 × 8 for kana (Japanese) and user defined symbols
- Icon mode: reduced current consumption while displaying icons only
- Icon blink function
- On-chip:
  - generation of LCD supply voltage, independent of V_{DD}, programmable by instruction (external supply also possible)
  - temperature compensation of on-chip generated V_{LCD}: –8 to –12 mV/K at 5.0 V (programmable by instruction)
  - generation of intermediate LCD bias voltages
  - oscillator requires no external components (external clock also possible)
- Display Data RAM: 80 characters
- Character Generator ROM: 240, 5 × 8 characters
- Character Generator RAM: 16, 5 × 8 characters; 4 characters used to drive 160 icons, 8 characters used if icon-blink feature is used in application
- 4 or 8-bit parallel bus and 2-wire I²C-bus interface
- CMOS compatible
- 18 row, 80 column outputs
- Multiplex rates 1 : 18 (for normal operation), 1 : 9 (for single line operation) and 1 : 2 (for icon-only mode)
- Uses common 11 code instruction set (extended)
- Logic supply voltage range, $V_{DD} - V_{SS}$ = 1.5 to 4.0 V (up to 5.5 V if external V_{LCD} is used); chip may be driven with two battery cells
- Display supply voltage range, $V_{LCD} - V_{SS}$ = 2.2 to 6.5 V
- Very low current consumption (20 to 200 µA):
  - icon mode: <25 µA
  - power-down mode: <2 µA
- Power control mode automatically reduces power when $V_{LCD} \approx V_{DD}$.

1.1 Note

Icon mode is used to save current. When only icons are displayed, a much lower operating voltage V_{LCD} can be used and the switching frequency of the LCD outputs is reduced. In most applications it is possible to use V_{DD} as V_{LCD}.

2 APPLICATIONS

- Telecom equipment
- Portable instruments
- Point-of-sale terminals.

3 GENERAL DESCRIPTION

The PCF2119x is a low power CMOS LCD controller and driver, designed to drive a dot matrix LCD display of 2-line by 16 and 1-line by 32 characters with 5 × 8 dot format. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD bias voltages, resulting in a minimum of external components and lower system current consumption. The PCF2119x interfaces to most microcontrollers via a 4 or 8-bit bus or via the 2-wire I²C-bus. The chip contains a character generator and displays alphanumeric and kana (Japanese) characters. The letter 'x' in PCF2119x characterizes the built-in character set. Various character sets can be manufactured on request.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PC2119RU/2	–	chip with bumps in tray	–

5 BLOCK DIAGRAM

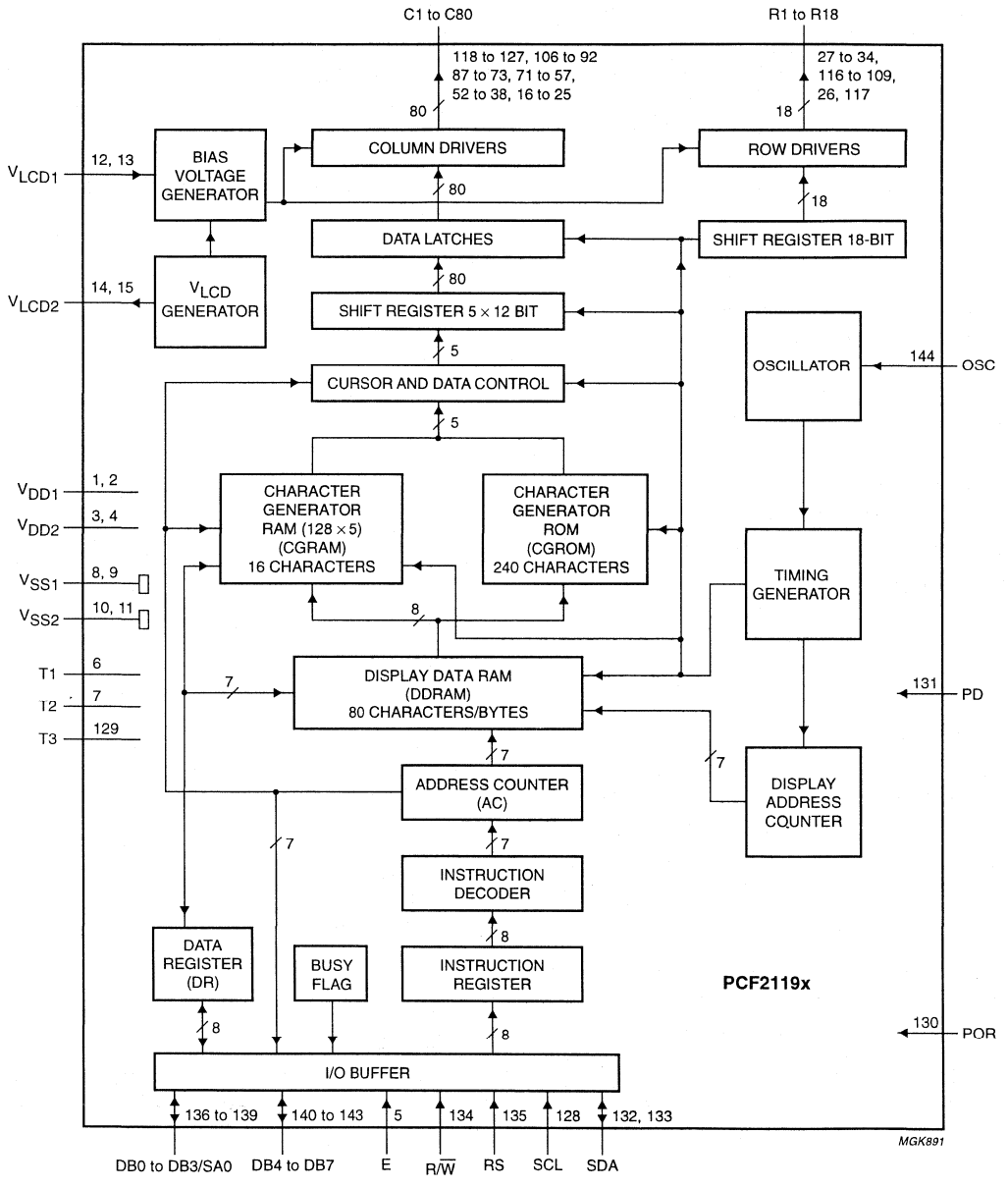


Fig.1 Block diagram.

6 PAD INFORMATION

The identification of each pad and its location is given in Chapter 17.

6.1 Pad functions

Table 1 Pad function description

SYMBOL	DESCRIPTION
V_{DD1}	Supply voltage for all except the high voltage generator.
V_{DD2}	Supply voltage for the high voltage generator.
V_{SS1}	This is the ground pad for all except the high voltage generator.
V_{SS2}	This is the ground pad for the high voltage generator.
V_{LCD1}	This input is used for the generation of the LCD bias levels.
V_{LCD2}	This is the V_{LCD} output pad if V_{LCD} is generated internally. This pad must be connected to V_{LCD1}.
E	The data bus clock input is set HIGH to signal the start of a read or write operation; data is clocked in or out of the chip on the negative edge of the clock; note 1.
T1	These are three test pads. T1 and T2 must be connected to V_{SS1}; T3 is left open and is not user accessible.
T2	
T3	
R1 to R18; R17DUP	LCD row driver outputs R1 to R18; these pins output the row select waveforms to the display; R17 and R18 drive the icons. R17 has two pads R17 and R17DUP.
C1 to C80	LCD column driver outputs C1 to C80.
SCL	I²C-bus serial clock input; note 1.
POR	External power-on reset input.
PD	PD selects the chip power-down mode; for normal operation PD = 0.
SDA	I²C-bus serial data input/output; note 1.
R/$\overline{W}$	This is the read/write input. R/$\overline{W}$ selects either the read (R/$\overline{W}$ = 1) or write (R/$\overline{W}$ = 0) operation. This pad has internal pull-up.
RS	The RS input selects the register to be accessed for read and write. RS = 0, selects the instruction register for write and the busy flag and address counter for read. RS = 1, selects the data register for both read and write. This pad has an internal pull-up.
DB0 to DB7	The 8-bit bidirectional data bus (3-state) transfers data between the system controller and the PCF2119x. DB7 may be used as the busy flag, signalling that internal operations are not yet completed. In 4-bit operations the 4 higher order lines DB7 to DB4 are used; DB3 to DB0 must be left open-circuit. Data bus line DB3 has an alternative function (SA0), when selected this is the I²C-bus address pad. Each data line has its own internal pull-up resistor; note 1.
OSC	Oscillator or external clock input. When the on-chip oscillator is used this pin must be connected to V_{DD1}.

Note

1. When the I²C-bus is used, the parallel interface pin E must be a logic 0. In the I²C-bus read mode DB7 to DB0 should be connected to V_{DD1} or left open.
   a) When the parallel bus is used, pins SCL and SDA must be connected to V_{SS1} or V_{DD1}; they must not be left open.
   b) If the 4-bit interface is used without reading out from the PCF2119x (i.e. R/$\overline{W}$ is set permanently to a logic 0), the unused ports DB0 to DB4 can either be set to V_{SS1} or V_{DD1} instead of leaving them open.

7 FUNCTIONAL DESCRIPTION

7.1 LCD supply voltage generator

The LCD supply voltage may be generated on-chip. The voltage generator is controlled by two internal 6-bit registers: V_A and V_B. The nominal LCD operating voltage at room temperature is given by the relationship:

$$V_{OP(nom)} = (\text{integer value of register} \times 0.08) + 1.82$$

7.2 Programming ranges

Programmed value: 1 to 63. Voltage: 1.90 to 6.84 V. T_{ref} = 27 °C.

Values producing more than 6.5 V at operating temperature are not allowed. Operation above this voltage may damage the device. When programming the operating voltage the V_{LCD} temperature coefficient must be taken into account.

Values below 2.2 V are below the specified operating range of the chip and are therefore not allowed.

Value 0 for V_A and V_B switches the generator off (i.e. V_A = 0 in character mode, V_B = 0 in icon mode, $V_A = V_B = 0$ in power control mode switches the generator off).

Usually register V_A is programmed with the voltage for character mode and register V_B with the voltage for icon mode.

When V_{LCD} is generated on-chip the V_{LCD} pins should be decoupled to V_{SS} with a suitable capacitor. The generated V_{LCD} is independent of V_{DD} and is temperature compensated. When the generator is switched off an external voltage may be supplied at connected pins $V_{LCD1,2}$. $V_{LCD1,2}$ may be higher or lower than V_{DD}.

The LCD supply voltage generator ensures that, as long as V_{DD} is in the valid range (1.8 to 4 V), the required peak voltage V_{OP} = 5.2 V can be generated at any time.

7.3 LCD bias voltage generator

The intermediate bias voltages for the LCD display are also generated on-chip. This removes the need for an external resistive bias chain and significantly reduces the system current consumption. The optimum value of V_{LCD} depends on the multiplex rate, the LCD threshold voltage (V_{th}) and the number of bias levels and is given by the relationships given in Tables 2 and 3. Using a 5-level bias scheme for 1 : 18 maximum rate allows V_{LCD} <5 V for most LCD liquids.

Table 2 Optimum/maximum values for V_{OP} (off pixels start darkening; $V_{off} = V_{th}$)

MULTIPLEX RATE	NUMBER OF LEVELS	V_{on}/V_{th}	V_{OP}/V_{th}	V_{OP} (typical; for V_{th} = 1.4 V)
1 : 18	5	1.272	3.7	5.2 V
1 : 2	4	2.236	2.283	3.9 V

Table 3 Minimum values for V_{OP} (on pixels clearly visible; $V_{on} > V_{th}$)

MULTIPLEX RATE	NUMBER OF LEVELS	V_{on}/V_{th}	V_{OP}/V_{th}	V_{OP} (typical; for V_{th} = 1.4 V)
1 : 18	5	1.12	3.2	4.6 V
1 : 2	4	1.2	1.5	2.1 V

7.4 Oscillator

The on-chip oscillator provides the clock signal for the display system. No external components are required and the OSC pin must be connected to V_{DD}.

7.5 External clock

If an external clock is to be used this is input at the OSC pin. The resulting display frame frequency is given by:

$$f_{frame} = \frac{f_{OSC}}{3072}$$

Only in the power-down state is the clock allowed to be stopped (OSC connected to V_{SS}), otherwise the LCD is frozen in a DC state.

7.6 Power-on reset

The PC2119 must be reset externally. This is internally a synchronous reset and requires 3 OSC cycles to be executed after release of the external reset signal. If no external reset is done, the chip might start up in an unwanted state.

7.7 Power-down mode

The chip can be put into power-down mode where all static currents are switched off (no internal oscillator, no bias level generation, all LCD outputs are internally connected to V_{SS}) when PD = 1.

During power-down, information in the RAMs and the chip state are preserved. Instruction execution during power-down is possible when externally clocking pad OSC.

7.8 Registers

The PCF2119x has two 8-bit registers, an Instruction Register (IR) and a Data Register (DR). The Register Select signal (RS) determines which register will be accessed. The instruction register stores instruction codes such as 'display clear' and 'cursor shift', and address information for the Display Data RAM (DDRAM) and Character Generator RAM (CGRAM).

The instruction register can be written from but not read by the system controller. The data register temporarily stores data to be read from the DDRAM and CGRAM. When reading, data from the DDRAM or CGRAM corresponding to the address in the instruction register is written to the data register prior to being read by the 'read data' instruction.

7.9 Busy flag

The busy flag indicates the internal status of the PCF2119x. A logic 1 indicates that the chip is busy and further instructions will not be accepted. The busy flag is output to pad DB7 when RS = 0 and R/$\overline{W}$ = 1. Instructions should only be written after checking that the busy flag is a logic 0 or waiting for the required number of cycles.

7.10 Address Counter (AC)

The address counter assigns addresses to the DDRAM and CGRAM for reading and writing and is set by the commands 'set CGRAM address' and 'set DDRAM address'. After a read/write operation the address counter is automatically incremented or decremented by 1.
The address counter contents are output to the bus (DB6 to DB0) when RS = 0 and R/$\overline{W}$ = 1.

7.11 Display Data RAM (DDRAM)

The DDRAM stores up to 80 characters of display data represented by 8-bit character codes. RAM locations which are not used for storing display data can be used as general purpose RAM. The basic RAM to display addressing scheme is shown in Fig.2. With no display shift the characters represented by the codes in the first 32 RAM locations starting at address 00H in line 1 are displayed. Figures 3 and 4 show the display mapping for right and left shift respectively.

When data is written to or read from the DDRAM wrap-around occurs from the end of one line to the start of the next line. When the display is shifted each line wraps around within itself, independently of the others. Thus all lines are shifted and wrapped around together.
The address ranges and wrap-around operations for the various modes are shown in Table 4.

Table 4 Address space and wrap-around operation

MODE	1 × 32	2 × 16
Address space	00 to 4F	00 to 27; 40 to 67
Read/write wrap-around (moves to next line)	4F to 00	27 to 40; 67 to 00
Display shift wrap-around (stays within line)	4F to 00	27 to 00; 67 to 40

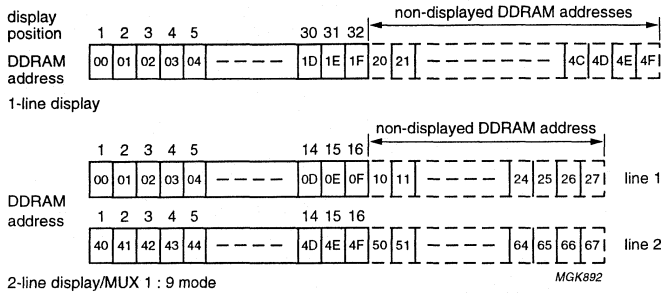


Fig.2 DDRAM to display mapping: no shift.

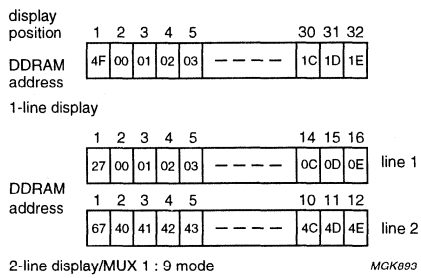


Fig.3 DDRAM to display mapping: right shift.

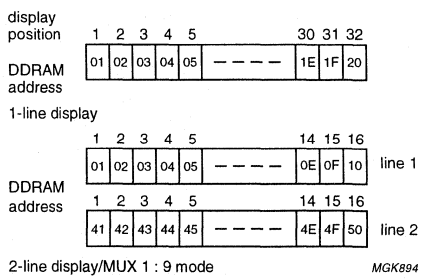


Fig.4 DDRAM to display mapping: left shift.

7.12 Character Generator ROM (CGROM)

The Character Generator ROM generates 240 character patterns in 5 × 8 dot format from 8-bit character codes. Figure 6 shows the character set that is currently implemented.

7.13 Character Generator RAM (CGRAM)

Up to 16 user defined characters may be stored in the Character Generator RAM. Some CGRAM characters (see Fig.15) are also used to drive icons (6 if icons blink and both icon rows are used in the application; 3 if no blink but both icon rows are used in the application; 0 if no icons are driven by the icon rows). The CGROM and CGRAM use a common address space, of which the first column is reserved for the CGRAM (see Fig.6). Figure 7 shows the addressing principle for the CGRAM.

7.14 Cursor control circuit

The cursor control circuit generates the cursor (underline and/or cursor blink as shown in Fig.5) at the DDRAM address contained in the address counter.

When the address counter contains the CGRAM address the cursor will be inhibited.

7.15 Timing generator

The timing generator produces the various signals required to drive the internal circuitry. Internal chip operation is not disturbed by operations on the data buses.

7.16 LCD row and column drivers

The PCF2119x contains 18 row and 80 column drivers, which connect the appropriate LCD bias voltages in sequence to the display in accordance with the data to be displayed. R17 and R18 drive the icon rows.

The bias voltages and the timing are selected automatically when the number of lines in the display is selected. Figures 8 to 11 show typical waveforms. Unused outputs should be left unconnected.

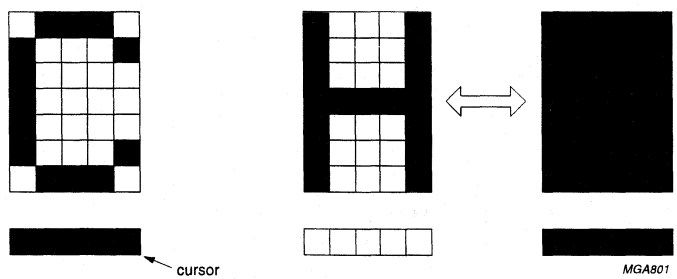
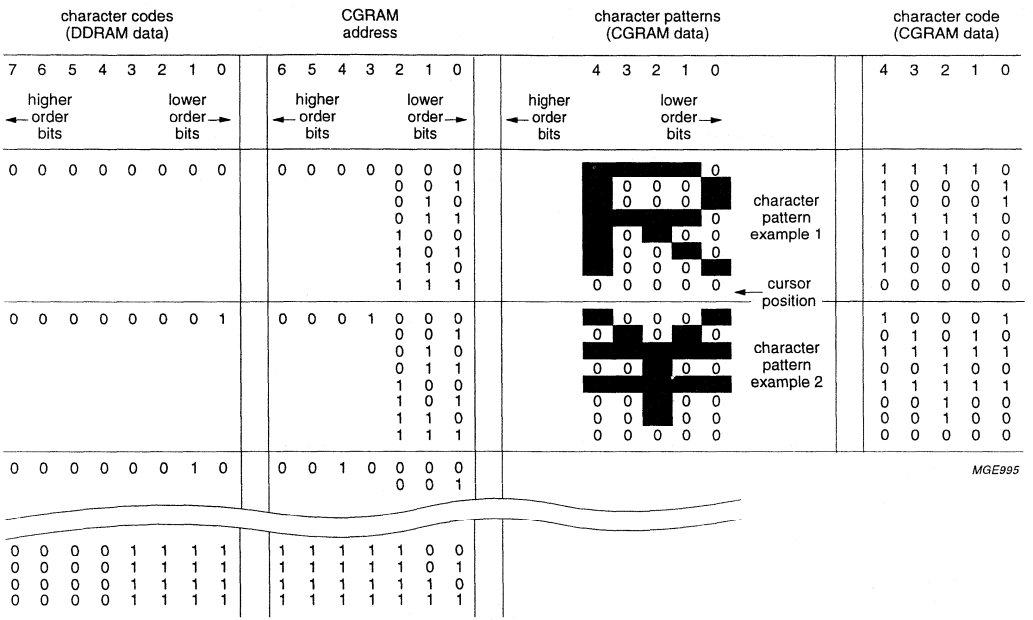


Fig.5 Cursor and blink display examples.

lower 4 bits \ upper 4 bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx 0000	1															
xxxx 0001	2															
xxxx 0010	3															
xxxx 0011	4															
xxxx 0100	5															
xxxx 0101	6															
xxxx 0110	7															
xxxx 0111	8															
xxxx 1000	9															
xxxx 1001	10															
xxxx 1010	11															
xxxx 1011	12															
xxxx 1100	13															
xxxx 1101	14															
xxxx 1110	15															
xxxx 1111	16															

MGM276

Fig.6 Character set 'R' in CGROM.



Character code bits 0 to 3 correspond to CGRAM address bits 3 to 6.

CGRAM address bits 0 to 2 designate the character pattern line position. The 8th line is the cursor position and display is performed by logical OR with the cursor. Data in the 8th position will appear in the cursor position.

Character pattern column positions correspond to CGRAM data bits 0 to 4, as shown in Fig.6.

As shown in Figs 6 and 7, CGRAM character patterns are selected when character code bits 4 to 7 are all logic 0. CGRAM data = logic 1 corresponds to selection for display.

Only bits 0 to 5 of the CGRAM address are set by the 'set CGRAM address' command. Bit 6 can be set using the 'set DDRAM address' command in the valid address range or by using the auto-increment feature during CGRAM write. All bits 0 to 6 can be read using the 'read busy flag and address counter' command.

Fig.7 Relationship between CGRAM addresses, data and display patterns.

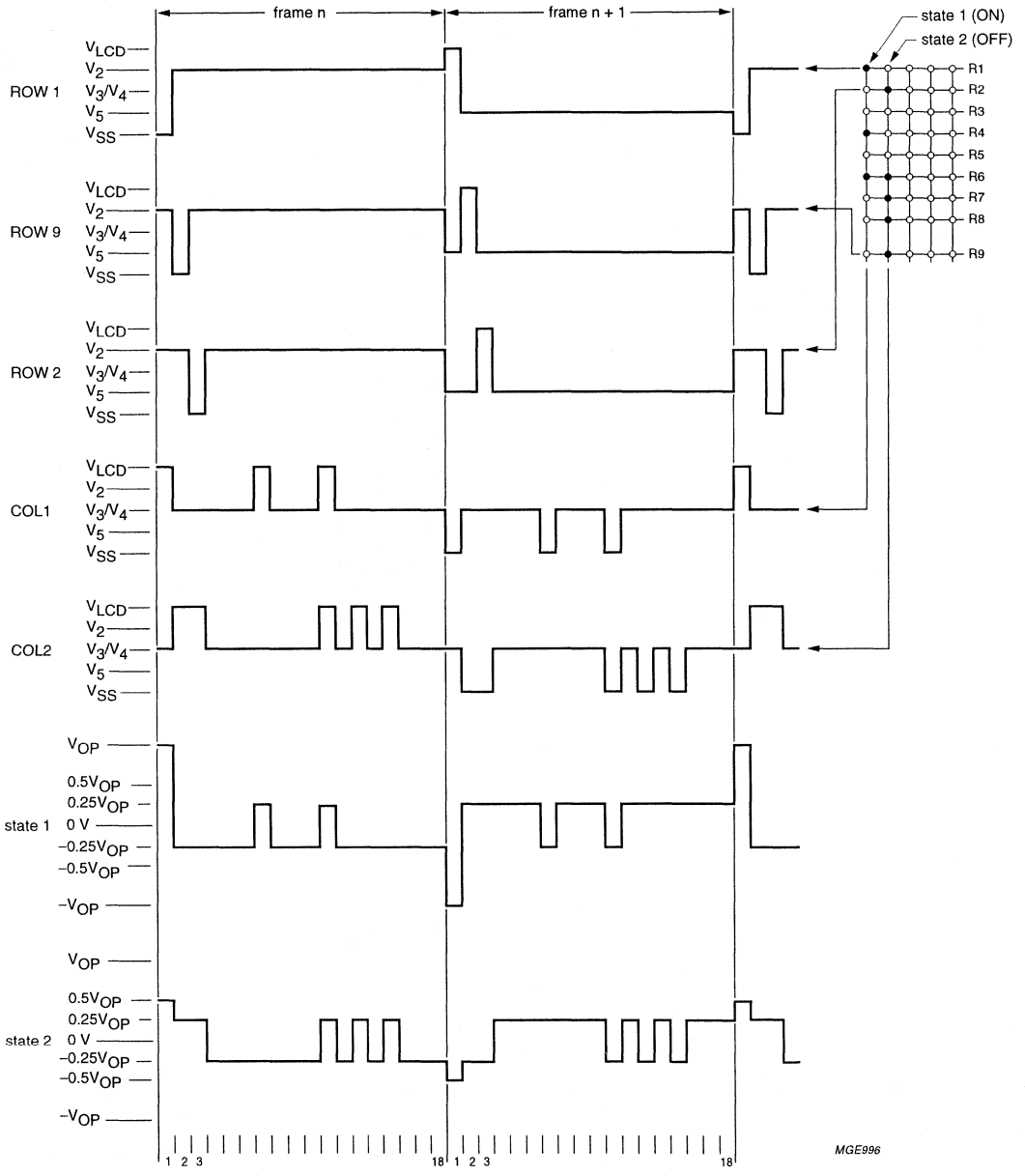


Fig.8 MUX 1 : 18 LCD waveforms; character mode.

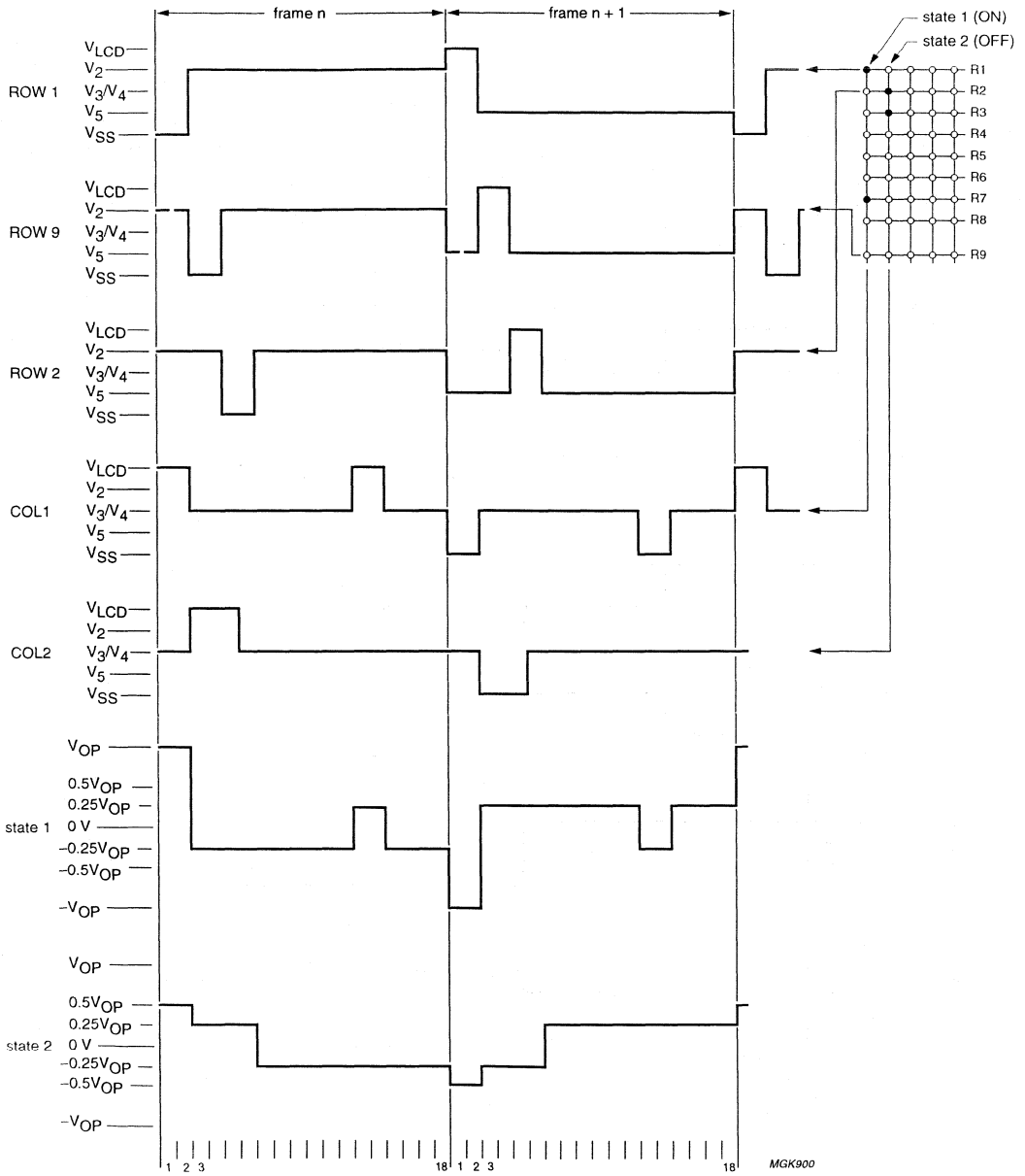


Fig.9 MUX 1 : 9 LCD waveforms; character mode. R10 to 18 to be left open.

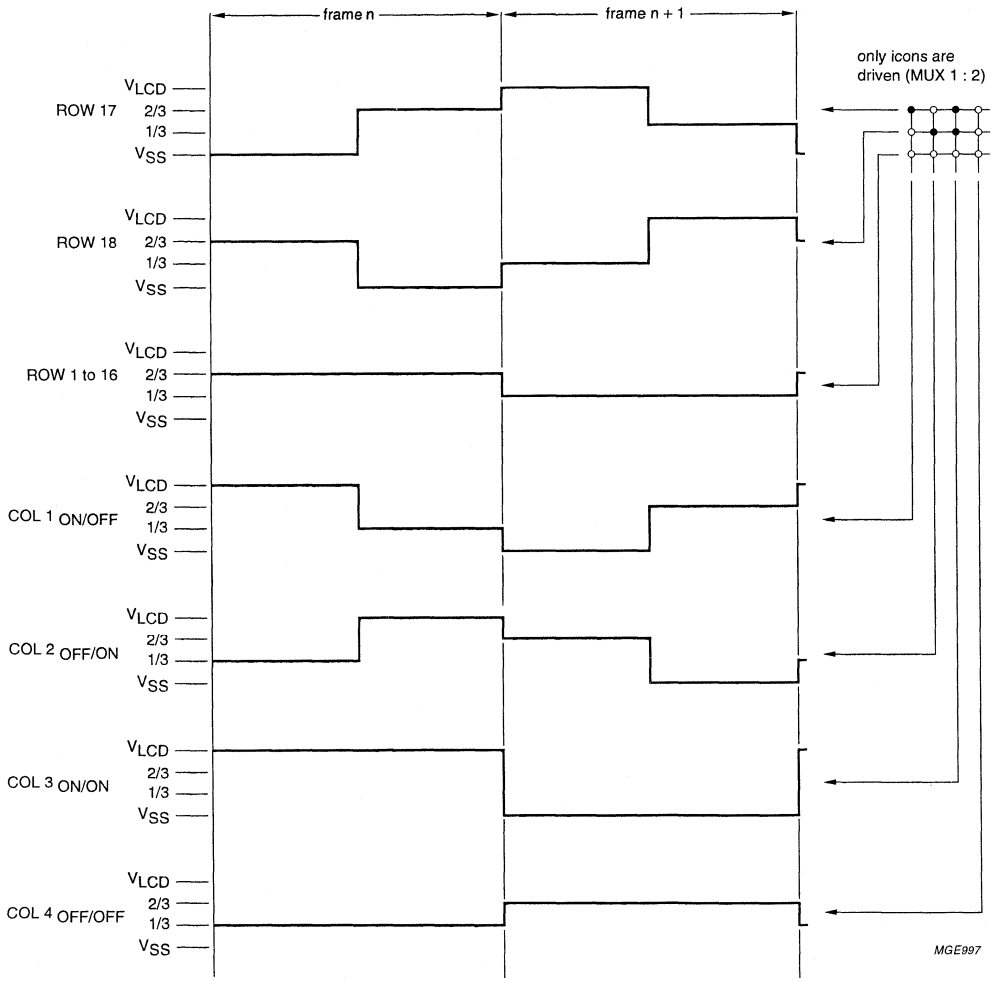
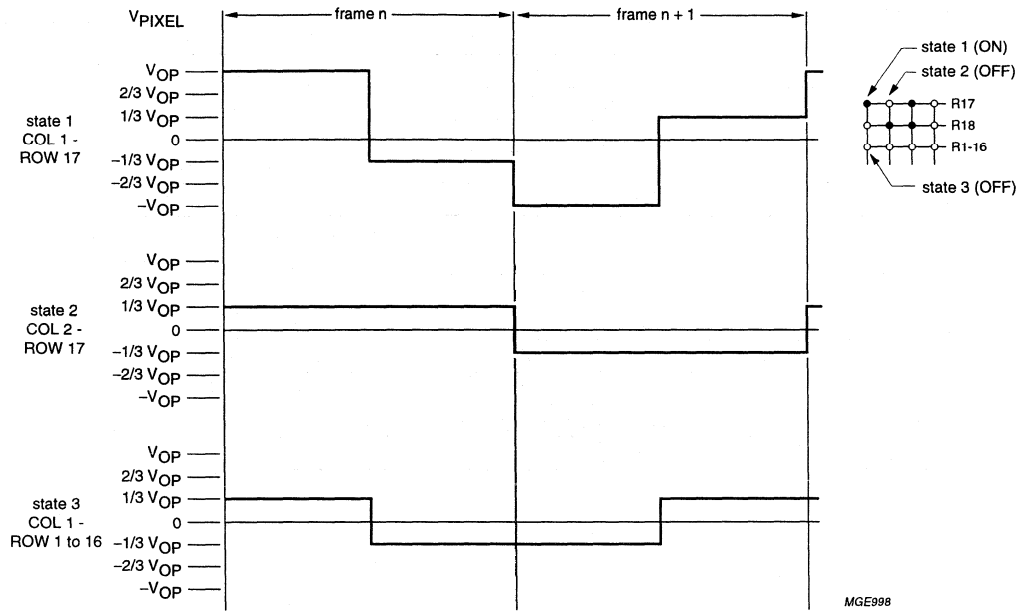


Fig.10 MUX 1 : 2 LCD waveforms; icon-mode.



$V_{ON(rms)} = 0.745V_{OP}$

$V_{OFF(rms)} = 0.333V_{OP}$

$$D = \frac{V_{ON}}{V_{OFF}} = 2.23$$

Fig.11 MUX 1 : 2 LCD waveforms; icon-mode.

7.17 Reset function

The PCF2119x must be reset externally when power is turned on. The reset executes a 'clear display', requiring 165 oscillator cycles. After the reset the chip has the state shown in Table 5.

Table 5 State after reset

STEP	FUNCTION	CONTROL BIT STATE	CONDITION
1	clear display		
2	entry mode set	I/D = 1	+1 (increment)
		S = 0	no shift
3	display control	D = 0	display off
		C = 0	cursor off
		B = 0	cursor character blink off
4	function set	DL = 1	8-bit interface
		M = 0	1-line display
		H = 0	normal instruction set
		SL = 0	MUX 1 : 18 mode
5	default address pointer to DDRAM; the Busy Flag (BF) indicates the busy state (BF = 1) until initialization ends; the busy state lasts 2 ms; the chip may also be initialized by software; see Tables 18 and 19		
6	icon control	IM, IB = 00	icons/icon blink disabled
7	power control	PC = 0	power control off
8	display/screen configuration	L, P and Q = 000	default configurations
9	V_{LCD} temperature coefficient	TC1 and TC2 = 00	default temperature coefficient
10	set V_{LCD}	V_A and V_B = 0 (V_{LCD} generator off)	
11	I^2C-bus interface reset		

8 INSTRUCTIONS

Only two PCF2119x registers, the Instruction Register (IR) and the Data Register (DR) can be directly controlled by the MPU. Before internal operation, control information is stored temporarily in these registers, to allow interfacing to various types of MPUs which operate at different speeds or to allow interface to peripheral control ICs.
The PCF2119x operation is controlled by the instructions shown in Table 7 together with their execution time. Details are explained in subsequent sections.

Instructions are of 4 types, those that:

1. Designate PCF2119x functions such as display format, data length, etc.
2. Set internal RAM addresses
3. Perform data transfer with internal RAM
4. Others.

In normal use, category 3 instructions are used most frequently. However, automatic incrementing by 1 (or decrementing by 1) of internal RAM addresses after each data write lessens the MPU program load.
The display shift in particular can be performed concurrently with display data write, enabling the designer to develop systems in minimum time with maximum programming efficiency.

During internal operation, no instructions other than the 'read busy flag' and 'read address' instructions will be executed. Because the busy flag is set to a logic 1 while an instruction is being executed, check to ensure it is a logic 0 before sending the next instruction or wait for the maximum instruction execution time, as given in Table 7. An instruction sent while the busy flag is logic 1 will not be executed.

Table 6 Instruction set for I²C-bus commands

CONTROL BYTE								COMMAND BYTE								I²C-BUS COMMANDS
Co	RS	0	0	0	0	0	0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	note 1

Note

1. R/$\overline{W}$ is set together with the slave address.

Table 7 Instruction set with parallel bus commands; note 1

INSTRUCTION	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DESCRIPTION	REQUIRED CLOCK CYCLES
H = 0 or 1												
NOP	0	0	0	0	0	0	0	0	0	0	no operation	3
Function set	0	0	0	0	1	DL	0	M	SL	H	sets interface Data Length (DL) and number of display lines (M); single line/MUX 1 : 9 (SL), extended instruction set control (H)	3
Read busy flag and address counter	0	1	BF	A_C							reads the Busy Flag (BF) indicating internal operating is being performed and reads address counter contents	0
Read data	1	1	read data								reads data from CGRAM or DDRAM	3
Write data	1	0	write data								writes data from CGRAM or DDRAM	3
H = 0												
Clear display	0	0	0	0	0	0	0	0	0	1	clears entire display and sets DDRAM address 0 in address counter	165
Return home	0	0	0	0	0	0	0	0	1	0	sets DDRAM address 0 in address counter; also returns shifted display to original position; DDRAM contents remain unchanged	3
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	sets cursor move direction and specifies shift of display; these operations are performed during data write and read	3
Display control	0	0	0	0	0	0	1	D	C	B	sets entire display on/off (D), cursor on/off (C) and blink of cursor position character (B); D = 0 (display off) puts chip into the power-down mode	3
Cursor/display shift	0	0	0	0	0	1	S/C	R/L	0	0	moves cursor and shifts display without changing DDRAM contents	3
Set CGRAM address	0	0	0	1	A_{CG}						sets CGRAM address; bit 6 is to be set by the command 'set DDRAM address'; look at the description of the commands	3
Set DDRAM address	0	0	1	A_{DD}							sets DDRAM address	3

INSTRUCTION	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DESCRIPTION	REQUIRED CLOCK CYCLES
H = 1												
Reserved	0	0	0	0	0	0	0	0	0	1	do not use	–
Screen configuration	0	0	0	0	0	0	0	0	1	L	set screen configuration	3
Display configuration	0	0	0	0	0	0	0	1	P	Q	set display configuration	3
Icon/power control	0	0	0	0	0	0	1	IM	IB	PC	set icon mode (IM), icon blink (IB), power control (PC)	3
Temperature control	0	0	0	0	0	1	0	0	TC1	TC2	set temperature coefficient (TCx)	3
Reserved	0	0	0	1	X	X	X	X	X	X	do not use	–
Set V_{LCD}	0	0	1	V	voltage						store V_{LCD} in register V_A or V_B (V)	3

Note

1. X = don't care.

Table 8 Explanations of symbols used in Table 7

BIT	STATE	
	LOGIC 0	LOGIC 1
I/D	decrement	increment
S	display freeze	display shift
D	display off	display on
C	cursor off	cursor on
B	cursor character blink off: character at cursor position does not blink	cursor character blink on: character at cursor position blinks
S/C	cursor move	display shift
R/L	left shift	right shift
DL	4 bits	8 bits
H	use basic instruction set	use extended instruction set
L (no impact, if M = 1 or SL = 1)	left/right screen: standard connection (as in PCF2114); 1st 16 characters of 32: columns are from 1 to 80 2nd 16 characters of 32: columns are from 1 to 80	left/right screen: mirrored connection (as in PCF2116); 1st 16 characters of 32: columns are from 1 to 80 2nd 16 characters of 32: columns are from 80 to 1
P	column data: left to right (as in PCF2116); column data is displayed from 1 to 80	column data: right to left; column data is displayed from 80 to 1
Q	row data: top to bottom (as in PCF2116); row data is displayed from 1 to 16 and icon row data is in 17 and 18	row data: bottom to top; row data is displayed from 16 to 1 and icon row data is in 18 and 17
IM	character mode; full display	icon mode; only icons displayed
IB	icon blink disabled	icon blink enabled
PC	power control off; V_{LCD} = programmed value	power control on; voltage generator is switched off and V_{DD} is used for V_{LCD} if $V_B < V_{DD} < V_A$
V	set V_A	set V_B
M (no impact, if SL = 1)	1-line by 32 display	2-line by 16 display
SL	MUX 1 : 18 (1 × 32 or 2 × 16 character display)	MUX 1 : 9 (1 × 16 character display)
C_0	last control byte; see Table 6	another control byte follows after data/command

Table 9 Explanation of TC1 and TC2 used in Table 7

TC1	TC2	DESCRIPTION
0	0	V_{LCD} temperature coefficient 0
1	0	V_{LCD} temperature coefficient 1
0	1	V_{LCD} temperature coefficient 2
1	1	V_{LCD} temperature coefficient 3; for ranges for TC see Chapter 13

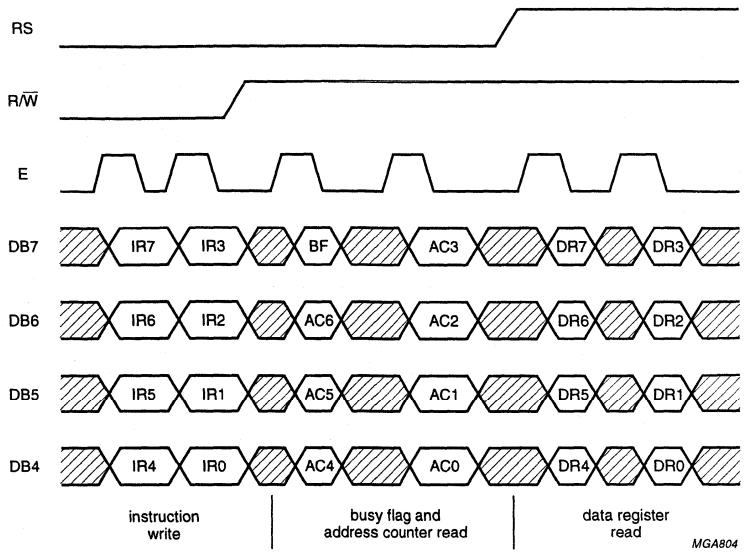
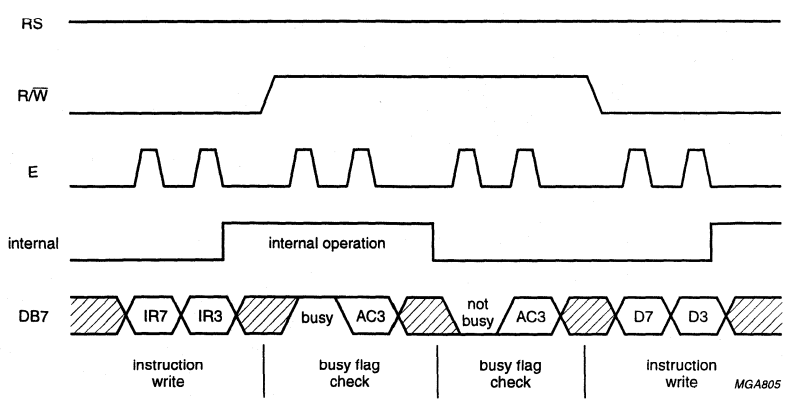


Fig.12 4-bit transfer example.



IR7, IR3: instruction 7th, 3rd bit.
AC3: address counter 3rd bit.
D7, D3: data 7th, 3rd bit.

Fig.13 An example of 4-bit data transfer timing sequence.

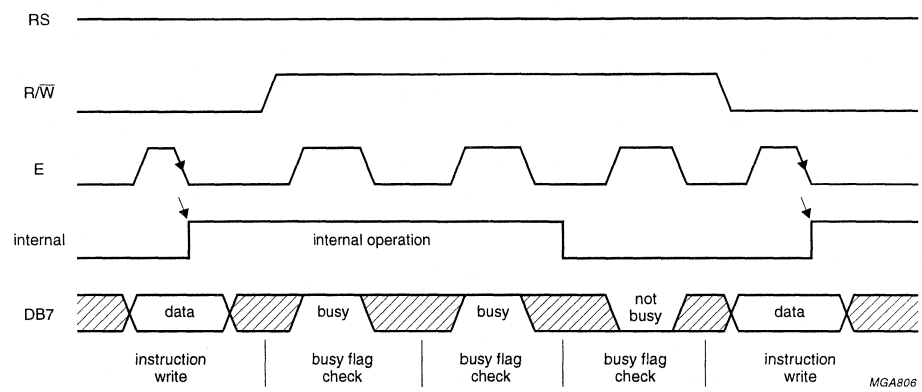


Fig.14 Example of busy flag checking timing sequence.

8.1 Clear display

'Clear display' writes character code 20H into all DDRAM addresses (the character pattern for character code 20H must be a blank pattern), sets the DDRAM address counter to logic 0 and returns the display to its original position, if it was shifted. Thus, the display disappears and the cursor or blink position goes to the left edge of the display. Sets entry mode I/D = 1 (increment mode). S of entry mode does not change.

The instruction 'clear display' requires extra execution time. This may be allowed by checking the Busy Flag (BF) or by waiting until the 165 clock cycles have elapsed. The latter must be applied where no read-back options are foreseen, as in some Chip-On-Glass (COG) applications.

8.2 Return home

'Return home' sets the DDRAM address counter to a logic 0 and returns display to its original position if it was shifted. DDRAM contents do not change. The cursor or blink position goes to the left of the first display line. I/D and S of entry mode do not change.

8.3 Entry mode set

8.3.1 I/D

When I/D = 1 (0) the DDRAM or CGRAM address increments (decrements) by 1 when data is written into or read from the DDRAM or CGRAM. The cursor or blink position moves to the right when incremented and to the left when decremented. The cursor underline and cursor character blink are inhibited when the CGRAM is accessed.

8.3.2 S

When S = 1, the entire display shifts either to the right (I/D = 0) or to the left (I/D = 1) during a DDRAM write. Thus it appears as if the cursor stands still and the display moves. The display does not shift when reading from the DDRAM, or when writing into or reading out of the CGRAM. When S = 0, the display does not shift.

8.4 Display control (and partial power-down mode)

8.4.1 D

The display is on when D = 1 and off when D = 0. Display data in the DDRAM are not affected and can be displayed immediately by setting D to a logic 1.

When the display is off (D = 0) the chip is in partial power-down mode:

- The LCD outputs are connected to V_{SS}
- The LCD generator and bias generator are turned off.

3 oscillator cycles are required after sending the 'display off' instruction to ensure all outputs are at V_{SS}, afterwards OSC can be stopped. If the oscillator is running during partial power-down mode ('display off') the chip can still execute instructions. Even lower current consumption is obtained by inhibiting the oscillator (OSC = V_{SS}).

To ensure I_{DD} <1 μA, the parallel bus pins DB7 to DB0 should be connected to V_{DD}; RS and R/$\overline{W}$ to V_{DD} or left open and PD to V_{DD}. Recovery from power-down mode: PD back to logic 0, if necessary OSC back to V_{DD} and send a 'display control' instruction with D = 1.

8.4.2 C

The cursor is displayed when C = 1 and inhibited when C = 0. Even if the cursor disappears, the display functions I/D, etc. remain in operation during display data write. The cursor is displayed using 5 dots in the 8th line (see Fig.5).

8.4.3 B

The character indicated by the cursor blinks when B = 1. The cursor character blink is displayed by switching between display characters and all dots on with a period of approximately 1 second, with $f_{BLINK} = \frac{f_{OSC}}{52\,224}$

The cursor underline and the cursor character blink can be set to display simultaneously.

8.5 Cursor or display shift

'Cursor/display shift' moves the cursor position or the display to the right or left without writing or reading display data. This function is used to correct a character or move the cursor through the display. In 2-line displays, the cursor moves to the next line when it passes the last position (40) of the line. When the displayed data is shifted repeatedly all lines shift at the same time; displayed characters do not shift into the next line. The Address Counter (AC) content does not change if the only action performed is shift display, but increments or decrements with the 'cursor shift'.

8.6 Function set

8.6.1 DL (PARALLEL MODE ONLY)

Sets interface data width. Data is sent or received in bytes (DB7 to DB0) when DL = 1 or in two nibbles (DB7 to DB4) when DL = 0. When 4-bit width is selected, data is transmitted in two cycles using the parallel bus. In a 4-bit application DB3 to DB0 should be left open (internal pull-ups). Hence in the first 'function set' instruction after power-on, N and H are set to logic 1. A second 'function set' must then be sent (2 nibbles) to set N and H to their required values.

'Function set' from I^2C-bus interface sets the DL bit to logic 1.

8.6.2 M

Chooses either 1-line by 32 display (M = 0) or 2-line by 16 display (M = 1).

8.6.3 SL

Chooses MUX 1 : 9, 1-line by 16 display (independent of M and L). Only rows 1 to 8 and 17 are to be used. All other rows must be left open. The DDRAM map is the same as in the 2-line by 16 display mode, however, the second line is not displayable.

8.6.4 H

When H = 0 the chip can be programmed via the standard 11 instruction codes used in the PCF2116 and other LCD controllers.

When H = 1 the extended range of instructions will be used. These are mainly for controlling the display configuration and the icons.

8.7 Set CGRAM address

'Set CGRAM address' sets bits 5 to 0 of the CGRAM address A_{CG} into the address counter (binary A[5] to A[0]). Data can then be written to or read from the CGRAM.

Attention: the CGRAM address uses the same address register as the DDRAM address and consists of 7 bits (binary A[6] to A[0]). With the 'set CGRAM address' command, only bits 5 down to 0 are set. Bit 6 can be set using the 'set DDRAM address' command first, or by using the auto-increment feature during CGRAM write. All bits 6 to 0 can be read using the 'read busy flag' and 'read address' command.

When writing to the lower part of the CGRAM, ensure that bit 6 of the address is not set (e.g. by an earlier DDRAM write or read action).

8.8 Set DDRAM address

'Set DDRAM address' sets the DDRAM address A_{DD} into the address counter (binary A[6] to A[0]). Data can then be written to or read from the DDRAM.

8.9 Read busy flag and read address

'Read busy flag' and 'read address' read the Busy Flag (BF) and Address Counter (AC). BF = 1 indicates that an internal operation is in progress. The next instruction will not be executed until BF = 0. It is recommended that the BF status is checked before the next write operation is executed.

At the same time, the value of the address counter expressed in binary A[6] to A[0] is read out. The address counter is used by both CGRAM and DDRAM, and its value is determined by the previous instruction.

8.10 Write data to CGRAM or DDRAM

'Write data' writes binary 8-bit data D[7] to D[0] to the CGRAM or the DDRAM.

Whether the CGRAM or DDRAM is to be written into is determined by the previous 'set CGRAM address' or 'set DDRAM address' command. After writing, the address automatically increments or decrements by 1, in accordance with the entry mode. Only bits D[4] to D[0] of CGRAM data are valid, bits D[7] to D[5] are 'don't care'.

8.11 Read data from CGRAM or DDRAM

'Read data' reads binary 8-bit data D[7] to D[0] from the CGRAM or DDRAM.

The most recent 'set address' command determines whether the CGRAM or DDRAM is to be read.

The 'read data' instruction gates the content of the Data Register (DR) to the bus while E is HIGH. After E goes LOW again, internal operation increments (or decrements) the AC and stores RAM data corresponding to the new AC into the DR.

There are only three instructions that update the data register:

- 'set CGRAM address'
- 'set DDRAM address'
- 'read data' from CGRAM or DDRAM.

Other instructions (e.g. 'write data', 'cursor/display shift', 'clear display' and 'return home') do not modify the data register content.

9 EXTENDED FUNCTION SET INSTRUCTIONS AND FEATURES

9.1 New instructions

H = 1, sets the chip into alternate instruction set mode.

9.2 Icon control

The PCF2119x can drive up to 160 icons. See Fig.15 for CGRAM to icon mapping.

9.3 IM

When IM = 0, the chip is in character mode. In character mode characters and icons are driven (MUX 1 : 18). The V_{LCD} generator, if used, produces the V_{LCD} voltage programmed in register V_A.

When IM = 1, the chip is in icon mode. In icon mode only the icons are driven (MUX 1 : 2) and the V_{LCD} voltage generator, if used, produces the V_{LCD} voltage as programmed in register V_B.

Power control (see Section 9.5) can be used in both icon and character mode to save current. In this case, when $V_B < V_{DD} < V_A$ the V_{LCD} voltage generator is switched off and V_{DD} is used as V_{LCD}.

9.4 IB

Icon blink control is independent of the cursor/character blink function.

When IB = 0, icon blink is disabled. Icon data is stored in CGRAM character 0 to 3 ($4 \times 8 \times 5 = 160$ bits for 160 icons).

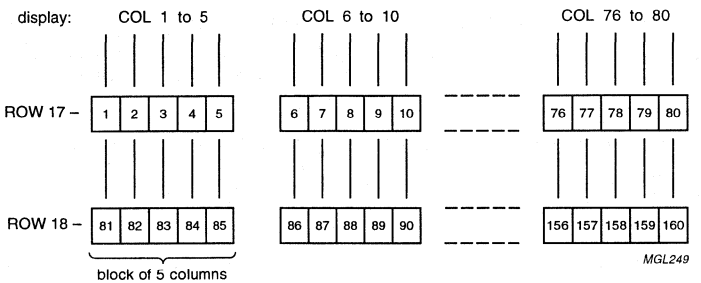
When IB = 1, icon blink is enabled. In this case each icon is controlled by two bits. Blink consists of two half phases (corresponding to the cursor on and off phases called even and odd phases hereafter).

Icon states for the even phase are stored in CGRAM characters 0 to 3 ($4 \times 8 \times 5 = 160$ bits for 160 icons). These bits also define icon state when icon blink is not used.

Icon states for the odd phase are stored in CGRAM character 4 to 7 (another 160 bits for the 160 icons). When icon blink is disabled CGRAM characters 4 to 6 may be used as normal CGRAM characters.

Table 10 Blink effect for icons and cursor character blink

PARAMETER	EVEN PHASE	ODD PHASE
Cursor underline	on	off
Cursor character blink	block (all on)	normal (display character)
Icons	state 1: CGRAM character 0 to 2	state 2: CGRAM character 4 to 6



icon no.	phase	ROW/COL	character codes	CGRAM address	CGRAM data	icon view
			7 6 5 4 3 2 1 0 MSB LSB	6 5 4 3 2 1 0 MSB LSB	4 3 2 1 0 MSB LSB	
1-5	even	17/1-5	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0	1 0 1 0 1	
6-10	even	17/6-10	0 0 0 0 0 0 0 0	0 0 0 0 0 0 1	0 1 0 1 0	
11-15	even	17/11-15	0 0 0 0 0 0 0 0	0 0 0 0 0 1 0	0 1 1 1 0	
⋮	⋮	⋮	⋮	⋮	⋮	⋮
76-80	even	17/76-80	0 0 0 0 0 0 0 1	0 0 0 1 1 1 1	1 1 1 1 1	
81-85	even	18/1-5	0 0 0 0 0 0 1 0	0 0 1 0 0 0 0	1 1 0 0 0	
⋮	⋮	⋮	⋮	⋮	⋮	⋮
156-160	even	18/76-80	0 0 0 0 0 0 1 1	0 0 1 1 1 1 1	1 1 1 0 1	
1-5	odd (blink)	17/1-5	0 0 0 0 0 1 0 0	0 1 0 0 0 0 0	0 0 0 0 0	
⋮	⋮	⋮	⋮	⋮	⋮	⋮
156-160	odd (blink)	18/76-80	0 0 0 0 0 1 1 1	0 1 1 1 1 1 1	0 0 1 1 0	

MGK999

CGRAM data bit = logic 1 turns the icon on, data bit = logic 0 turns the icon off.
Data in character codes 0 to 2 define the icon state when icon blink is disabled or during the even phase when icon blink is enabled.
Data in character codes 4 to 6 define the icon state during the odd phase when icon blink is enabled (not used for icons when icon blink is disabled).

Fig.15 CGRAM to icon mapping.

9.5 PC

PC = 1, enables power control. If V_{DD} lies above both programmed V_{LCD} values, V_A and V_B, V_A is generated. If V_{DD} lies below both programmed values, V_B is generated. If $V_B < V_{DD} < V_A$ the V_{LCD} generator is switched off and V_{DD} is used as V_{LCD}, thus reducing current consumption. This can be useful in many cases (e.g. battery operation in icon mode). Current consumption is reduced by about a factor 4 compared to character mode MUX 1 : 18.

To disable power control send the 'icon/power control' instruction with PC = 0.

9.6 Power control operation

IM	PC	CONDITION	V_{LCD}
Power control off			
0	0	character mode	generates V_A
1	0	icon mode	generates V_B
Power control on (character or icon mode)			
X[1]	1	$V_{DD} > V_A$	generates V_A
		$V_B < V_{DD} < V_A$	use V_{DD}
		$V_{DD} < V_A$ and $< V_B$	generates V_B

Note

1. X = don't care.

9.7 Screen configuration

L: default is L = 0.

L = 0: the two halves of a split screen are connected in a standard way i.e. column 1/81, 2/82 to 80/160.

L = 1: the two halves of a split screen are connected in a mirrored way i.e. column 1/160, 2/159 to 80/81. This allows single layer PCB or glass layout.

9.8 Display configuration

P, Q: default is P, Q = 0.

P = 1: mirrors the column data.

Q = 1: mirrors the row data.

9.9 TC1 and TC2

Default is TC1 and TC2 = 0. This selects the default temperature coefficient for the internally generated V_{LCD}. TC1 and TC2 = 10, 01 and 11 selects alternative temperature coefficients 1, 2 and 3 respectively.

9.10 Set V_{LCD}

The V_{LCD} value is programmed by instruction. Two on-chip registers hold V_{LCD} values for character mode and icon mode respectively (V_A and V_B). The generated V_{LCD} value is independent of V_{DD}, allowing battery operation of the chip.

V_{LCD} programming:

1. Send 'function set' instruction with H = 1
2. Send 'set V_{LCD}' instruction to write to voltage register:
   a) DB7, DB6 = 10: DB5 to DB0 are V_{LCD} of character mode (V_A)
   b) DB7, DB6 = 11: DB5 to DB0 are V_{LCD} of icon mode (V_B)
   c) DB5 to DB0 = 000000 switches V_{LCD} generator off (when selected)
   d) During 'display off' and power-down the V_{LCD} generator is also disabled
3. Send 'function set' instruction with H = 0 to resume normal programming.

V_{LCD} with power control: V_{DD} is used instead of generating V_{LCD} when $V_B < V_{DD} < V_A$ (see Section 9.2). Power control is controlled by the 'icon/power control' instruction.

9.11 Reducing current consumption

Reducing current consumption can be achieved by one of the options mentioned in Table 11.

When V_{LCD} lies outside the V_{DD} range and must be generated, it is usually more efficient to use the on-chip generator than an external regulator.

Table 11 Reducing current consumption

ORIGINAL MODE	ALTERNATIVE MODE
Character mode	icon mode (control bit IM)
Display on	display off (control bit D)
Any mode	power-down (PD pin)
V_{LCD} generation	power control (control bit PC) V_{DD} used for V_{LCD} when $V_B < V_{DD} < V_A$ (V_{LCD} generator switched off)

Table 12 Use of the V_A and V_B registers

MODE	V_A	V_B
Normal operation	V_{LCD} character mode	V_{LCD} icon mode
Power control	V_{LCD} upper limit	V_{LCD} lower limit

10 INTERFACES TO MPU

10.1 Parallel interface

The PCF2119x can send data in either two 4-bit operations or one 8-bit operation and can thus interface to 4-bit or 8-bit microcontrollers.

In 8-bit mode data is transferred as 8-bit bytes using the 8 data lines DB7 to DB0. Three further control lines E, RS and R/$\overline{W}$ are required; see Section 6.1.

In 4-bit mode data is transferred in two cycles of 4 bits each using pins DB7 to DB4 for the transaction. The higher order bits (corresponding to DB7 to DB4 in 8-bit mode) are sent in the first cycle and the lower order bits (DB3 to DB0 in 8-bit mode) in the second. Data transfer is complete after two 4-bit data transfers. Note that two cycles are also required for the busy flag check. 4-bit operation is selected by instruction. See Figs 12 to 14 for examples of bus protocol.

In 4-bit mode pins DB3 to DB0 must be left open-circuit. They are pulled up to V_{DD} internally.

10.2 I²C-bus interface

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are the Serial Data line (SDA) and the Serial Clock line (SCL). Both lines must be connected to a positive supply via pull-up resistors. Data transfer may be initiated only when the bus is not busy.

Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte.

Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

10.2.1 I²C-BUS PROTOCOL

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the START procedure. The I²C-bus configuration for the different PCF2119x read and write cycles is shown in Figs 20 to 22. The slow down feature of the I²C-bus protocol (receiver holds SCL LOW during internal operations) is not used in the PCF2119x.

10.2.2 DEFINITIONS

- Transmitter: the device which sends the data to the bus
- Receiver: the device which receives the data from the bus
- Master: the device which initiates a transfer, generates clock signals and terminates a transfer
- Slave: the device addressed by a master
- Multi-master: more than one master can attempt to control the bus at the same time without corrupting the message
- Arbitration: procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted
- Synchronization: procedure to synchronize the clock signals of two or more devices.

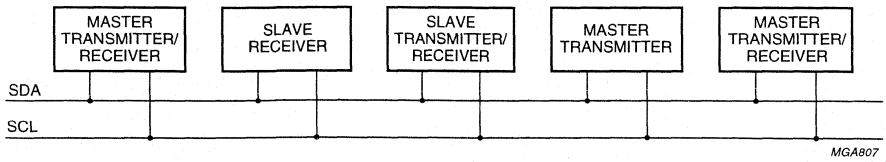


Fig.16 System configuration.

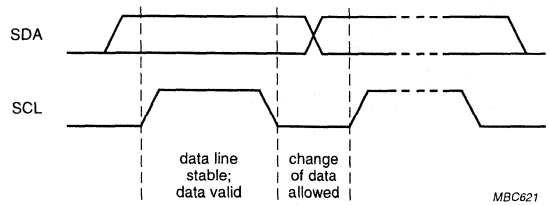


Fig.17 Bit transfer.

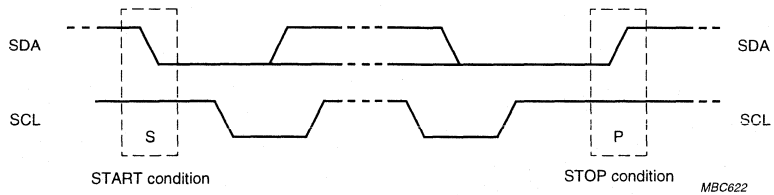


Fig.18 Definition of START and STOP conditions.

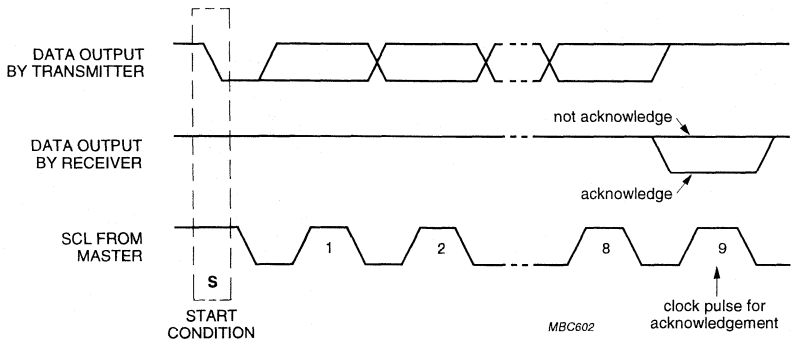


Fig.19 Acknowledgement on the I²C-bus.

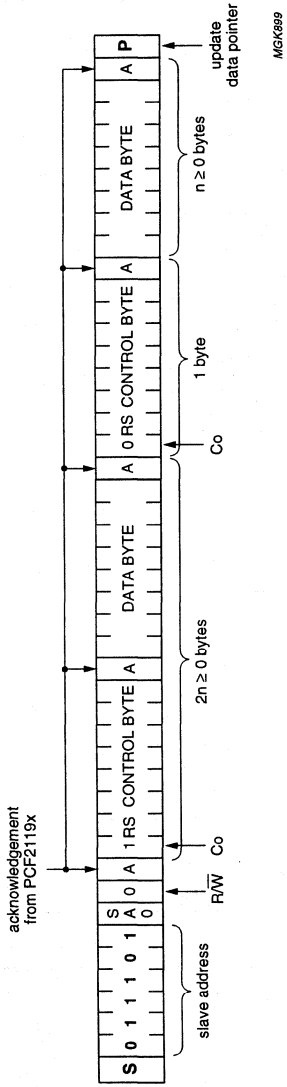
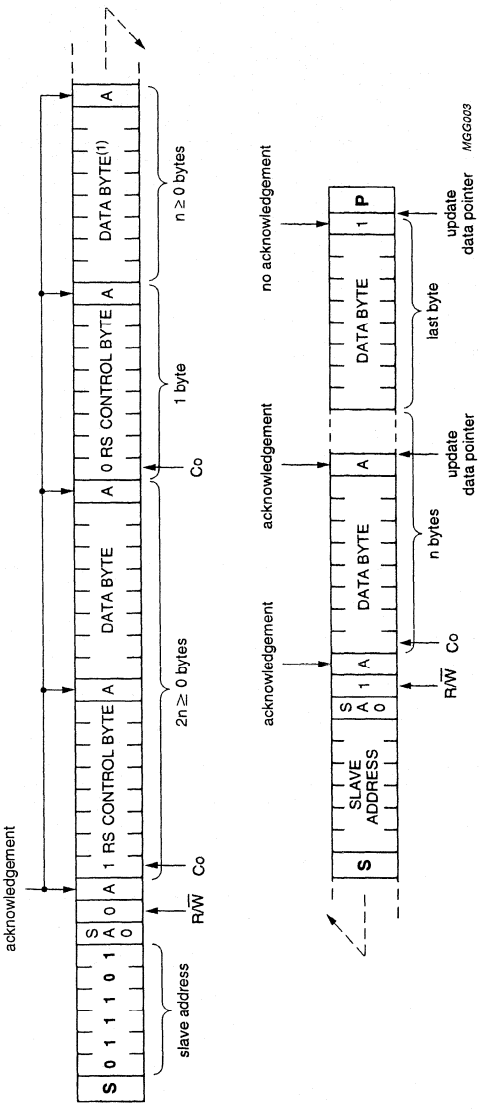


Fig.20 Master transmits to slave receiver; write mode.



(1) Last data byte is a dummy byte (may be omitted).

Fig.21 Master reads after setting word address; writes word address, set RS; 'read data'.

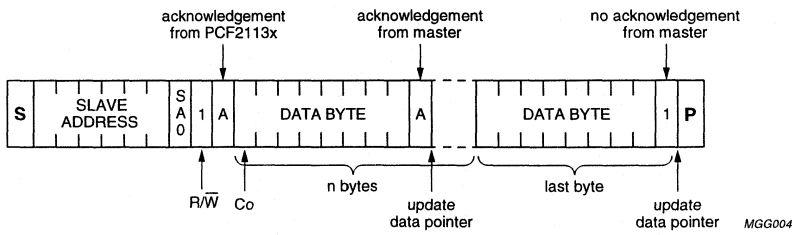


Fig.22 Master reads slave immediately after first byte; read mode (RS previously defined).

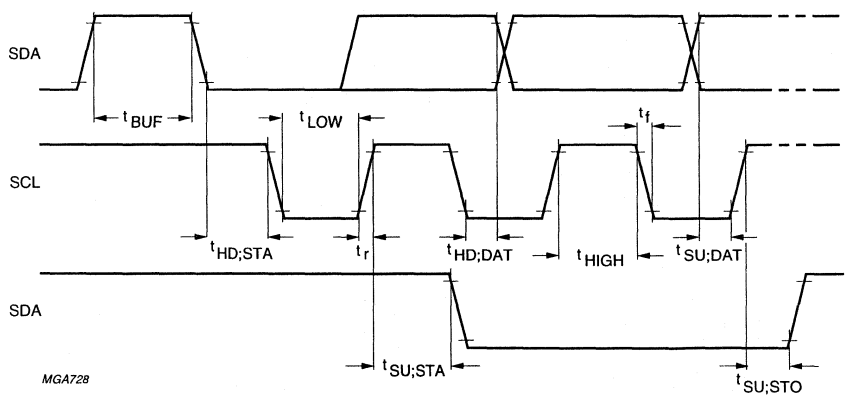


Fig.23 I²C-bus timing diagram.

11 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	+6.5	V
V_{LCD}	LCD supply voltage	−0.5	+7.5	V
V_I	input voltages: OSC, RS, R/$\overline{W}$, E and DB7 to DB0	−0.5	V_{DD} + 0.5	V
V_O	output voltages: R1 to R18, C1 to C80 and V_{LCD}	−0.5	V_{LCD} + 0.5	V
I_I	DC input current	−10	+10	mA
I_O	DC output current	−10	+10	mA
I_{DD}, I_{SS} and I_{LCD}	V_{DD}, V_{SS} or V_{LCD} current	−50	+50	mA
P_{tot}	total power dissipation	−	400	mW
P_O	power dissipation per output	−	100	mW
T_{stg}	storage temperature	−65	+150	°C

12 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see *"Handling MOS Devices"*).

13 DC CHARACTERISTICS

V_{DD} = 1.8 to 4.0 V (external V_{LCD}: V_{DD} = 1.8 to 5.5 V); V_{SS} = 0 V; V_{LCD} = 2.2 to 6.5 V; T_{amb} = −30 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD1}	supply voltage	internal V_{LCD} generation	1.5	–	4.0	V
V_{DD2}	high voltage generator supply voltage	internal V_{LCD} generation	2.2	–	4.0	
V_{DD1}	supply voltage	external V_{LCD}	1.5	–	5.5	V
V_{LCD}	LCD supply voltage		2.2	–	6.5	V
I_{SS}	ground supply current (external V_{LCD})	note 1				
I_{SS1}	ground supply current 1		–	tbf	tbf	µA
I_{SS3}	ground supply current 3	V_{DD} = 3 V; V_{LCD} = 5 V; note 2	–	45	80	µA
I_{SS4}	ground supply current 4 (icon mode)	V_{DD} = 3 V; V_{LCD} = 2.5 V; note 2	–	25	45	µA
I_{SS5}	ground supply current 5 (power-down mode)	V_{DD} = 3 V; V_{LCD} = 2.5 V; DB7 to DB0, RS and R/$\overline{W}$ = 1; OSC = 0; PD = 1	–	2	5	µA
I_{SS}	ground supply current (internal V_{LCD})	notes 1 and 3				
I_{SS6}	ground supply current 6		–	tbf	tbf	µA
I_{SS8}	ground supply current 8	V_{DD} = 3 V; V_{LCD} = 5 V; note 2	–	150	tbf	µA
I_{SS9}	ground supply current 9 (icon mode)	V_{DD} = 3 V; V_{LCD} = 2.5 V; note 2	–	100	–	µA
Logic						
V_{IL1}	LOW-level input voltage T1, E, RS, R/$\overline{W}$, DB[7 to 0] and SA0		0	–	$0.3V_{DD}$	V
V_{IH1}	HIGH-level input voltage T1, E, RS, R/$\overline{W}$, DB[7 to 0] and SA0		$0.7V_{DD}$	–	V_{DD}	V
$V_{IL(PD)}$	LOW-level input voltage PD		0	–	$0.2V_{DD}$	V
$V_{IH(PD)}$	HIGH-level input voltage PD		$0.8V_{DD}$	–	V_{DD}	V
$V_{IL(osc)}$	LOW-level input voltage OSC		0	–	V_{DD} − 1.5	V
$V_{IH(osc)}$	HIGH-level voltage OSC		V_{DD} − 0.1	–	V_{DD}	V
$I_{OL(DB)}$	LOW-level output current DB[7 to 0]	V_{OL} = 0.4 V; V_{DD} = 5 V	1.6	4	–	mA
$I_{OH(DB)}$	HIGH-level output current DB[7 to 0]	V_{OH} = 4 V; V_{DD} = 5 V	−1	−8	–	mA
I_{pu}	pull-up current DB[7 to 0]	$V_I = V_{SS}$	0.04	0.15	1	µA
I_L	leakage current OSC, E, RS, R/$\overline{W}$, DB[7 to 0] and SA0	$V_I = V_{DD}$ or V_{SS}	−1	–	+1	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I²C-bus						
SDA AND SCL						
V_{IL2}	LOW-level input voltage		0	–	$0.3V_{DD}$	V
V_{IH2}	HIGH-level input voltage		$0.7V_{DD}$	–	5.5	V
I_{LI}	input leakage current	$V_I = V_{DD}$ or V_{SS}	−1	–	+1	μA
C_i	input capacitance	note 4	–	–	10	pF
$I_{OL(SDA)}$	LOW-level output current SDA	V_{OL} = 0.4 V; V_{DD} = 5 V	3	–	–	mA
LCD outputs						
R_{ROW}	row output resistance R1 to R18	note 5	–	10	30	kΩ
R_{COL}	column output resistance C1 to C80	note 5	–	15	40	kΩ
V_{tol1}	bias tolerance R1 to R18 and C1 to C80	note 6	–	20	130	mV
$V_{LCD(tol)}$	V_{LCD} tolerance	T_{amb} = 25 °C; note 3	–	200	250	mV
TC0	V_{LCD} temperature coefficient 0	note 7	–	−7.6	–	mV/K
TC1	V_{LCD} temperature coefficient 1	note 7	–	−8.4	–	mV/K
TC2	V_{LCD} temperature coefficient 2	note 7	–	−10.4	–	mV/K
TC3	V_{LCD} temperature coefficient 3	note 7	–	−12.4	–	mV/K

Notes

1. LCD outputs are open-circuit; inputs at V_{DD} or V_{SS}; bus inactive.
2. T_{amb} = 25 °C; f_{OSC} = 200 kHz.
3. LCD outputs are open-circuit; HV generator is on; load current I_{VLCD} (at V_{LCD}) = 5 μA.
4. Tested on sample basis.
5. Resistance of output terminals (R1 to R18 and C1 to C80) with a load current of 20 μA; outputs measured one at a time; external V_{LCD}.
6. LCD outputs open-circuit; external V_{LCD}.
7. Temperature coefficient at V_{OP} = 5.0 V. Typical range ±2 mV/K.

14 AC CHARACTERISTICS

V_{DD} = 1.8 to 5.5 V; V_{SS} = 0 V; V_{LCD} = 2.2 to 6.5 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{FR}	LCD frame frequency (internal clock)	V_{DD} = 5.0 V	45	81	147	Hz
f_{OSC}	oscillator frequency (not available at any pin)		140	250	450	kHz
$f_{OSC(ext)}$	external clock frequency		tbf	–	450	kHz
t_{OSCST}	oscillator start-up time after power-down		–	200	300	µs
Bus timing characteristics: parallel interface; note 1						
WRITE OPERATION (WRITING DATA FROM MPU TO PCF2119x)						
$T_{cy(en)}$	enable cycle time		500	–	–	ns
$t_{W(en)}$	enable pulse width		220	–	–	ns
$t_{su(A)}$	address set-up time		50	–	–	ns
$t_{h(A)}$	address hold time		25	–	–	ns
$t_{su(D)}$	data set-up time		60	–	–	ns
$t_{h(D)}$	data hold time		25	–	–	ns
READ OPERATION (READING DATA FROM PCF2119x TO MPU)						
$T_{cy(en)}$	enable cycle time		500	–	–	ns
$t_{W(en)}$	enable pulse width		220	–	–	ns
$t_{su(A)}$	address set-up time		50	–	–	ns
$t_{h(A)}$	address hold time		25	–	–	ns
$t_{d(D)}$	data delay time		–	–	150	ns
$t_{h(D)}$	data hold time		20	–	100	ns
Timing characteristics: I^2C-bus interface; note 1						
f_{SCL}	SCL clock frequency		–	–	400	kHz
t_{LOW}	SCL clock low period		1.3	–	–	µs
t_{HIGH}	SCL clock high period		0.6	–	–	µs
$t_{SU;DAT}$	data set-up time		100	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	–	ns
t_r	SCL, SDA rise time		–	–	300	ns
t_f	SCL, SDA fall time		–	–	300	ns
C_B	capacitive bus line load		–	–	400	pF
$t_{SU;STA}$	set-up time for a repeated START condition		0.6	–	–	µs
$t_{HD;STA}$	START condition hold time		0.6	–	–	µs
$t_{SU;STO}$	set-up time for STOP condition		0.6	–	–	µs
t_{SW}	tolerable spike width on bus		–	–	50	ns

Note

1. All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

15 TIMING CHARACTERISTICS

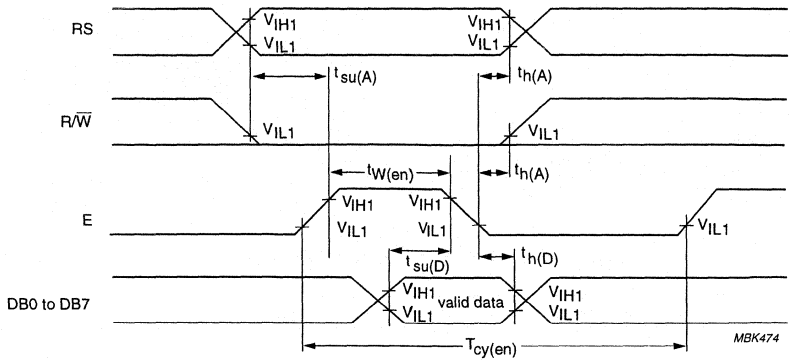


Fig.24 Parallel bus write operation sequence; writing data from MPU to PCF2119x.

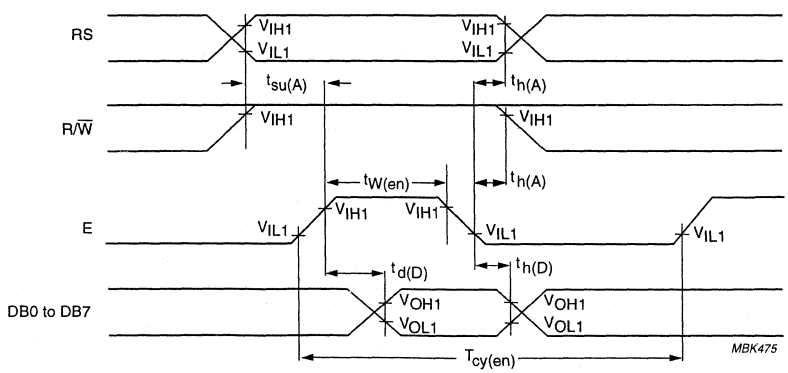


Fig.25 Parallel bus read operation sequence; reading data from PCF2119x to MPU.

16 APPLICATION INFORMATION

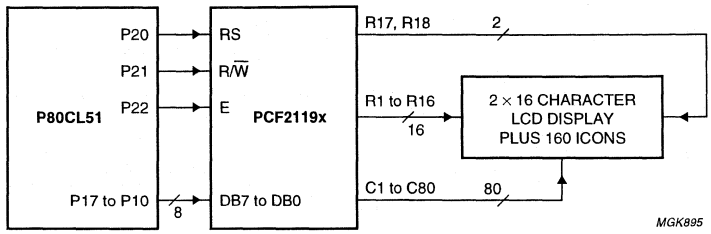


Fig.26 Direct connection to 8-bit MPU; 8-bit bus.

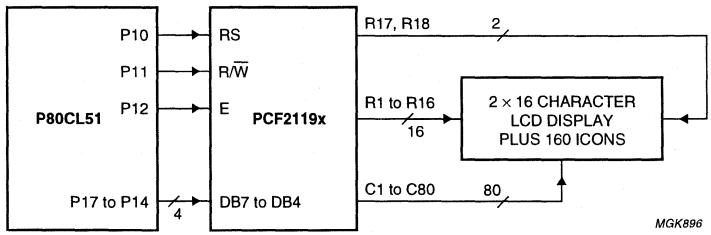


Fig.27 Direct connection to 8-bit MPU; 4-bit bus.

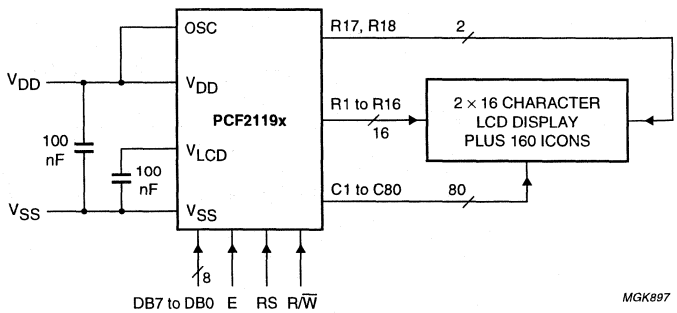


Fig.28 Typical application using parallel interface.

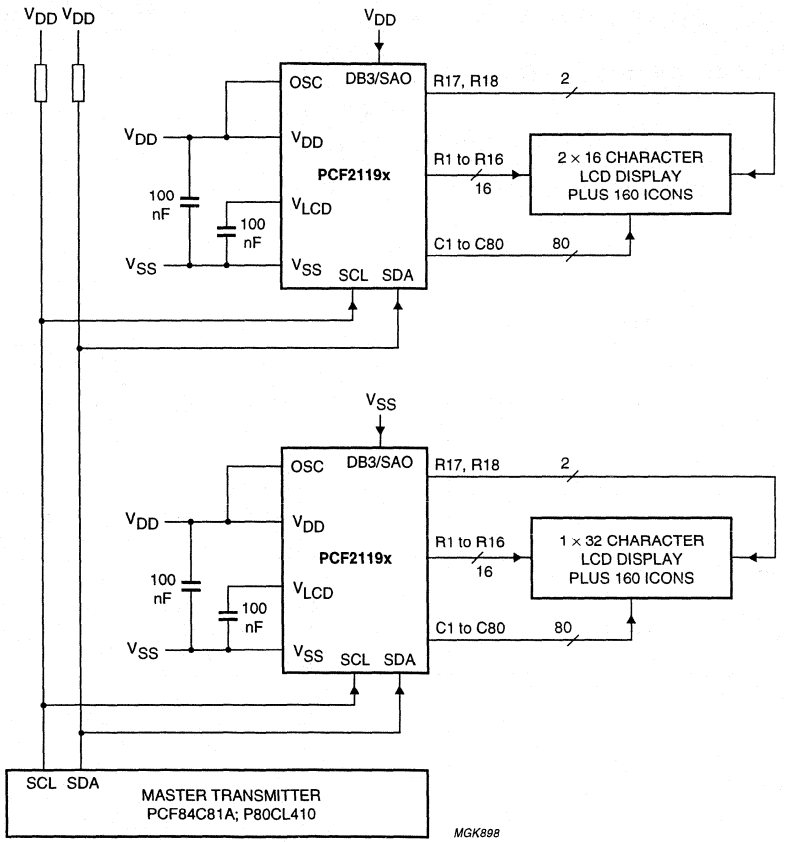


Fig.29 Application using I²C-bus interface.

16.1 8-bit operation, 1-line display using external reset

Table 14 shows an example of a 1-line display in 8-bit operation. The PCF2119x functions must be set by the 'function set' instruction prior to display. Since the DDRAM can store data for 80 characters, the RAM can be used for advertising displays when combined with display shift operation. Since the display shift operation changes display position only and the DDRAM contents remain unchanged, display data entered first can be displayed when the 'return home' operation is performed.

16.2 4-bit operation, 1-line display using external reset

The program must set functions prior to 4-bit operation. Table 13 shows an example. When power is turned on, 8-bit operation is automatically selected and the PCF2119x attempts to perform the first write as an 8-bit operation. Since nothing is connected to DB0 to DB3, a rewrite is then required. However, since one operation is completed in two accesses of 4-bit operation, a rewrite is required to set the functions (see Table 13 step 3).

Thus, DB4 to DB7 of the 'function set' are written twice.

16.3 8-bit operation, 2-line display

For a 2-line display, the cursor automatically moves from the first to the second line after the 40th digit of the first line has been written. Thus, if there are only 8 characters in the first line, the DDRAM address must be set after the 8th character is completed (see Table 7). Note that both lines of the display are always shifted together; data does not shift from one line to the other.

16.4 I²C-bus operation, 1-line display

A control byte is required with most commands (see Table 17).

Table 13 4-bit operation, 1-line display example; using external reset

STEP	INSTRUCTION						DISPLAY	OPERATION
1	power supply on (PCF2119x is initialized by the external reset)							initialized; no display appears
2	function set							
	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4		sets to 4-bit operation; in this instance operation is handled as 8-bits by initialization and only this instruction completes with one write
	0	0	0	0	1	0		
3	function set							
	0	0	0	0	1	0		sets to 4-bit operation, selects 1-line display and $V_{LCD} = V_0$; 4-bit operation starts from this point and resetting is needed
	0	0	0	0	0	0		
4	display on/off control							
	0	0	0	0	0	0	_	turns on display and cursor; entire display is blank after initialization
	0	0	1	1	1	0		
5	entry mode set							
	0	0	0	0	0	0	_	sets mode to increment the address by 1 and to shift the cursor to the right at the time of write to the DD/CGRAM; display is not shifted
	0	0	0	1	1	0		
6	'write data' to CGRAM/DDRAM							
	1	0	0	1	0	1	P_	writes 'P'; the DDRAM has already been selected by initialization at power-on; the cursor is incremented by 1 and shifted to the right
	1	0	0	0	0	0		

Table 14 8-bit operation, 1-line display example; using external reset (character set 'A')

STEP	INSTRUCTION	DISPLAY	OPERATION
1	power supply on (PCF2119x is initialized by the external reset)		initialized; no display appears
2	function set RS R/$\overline{W}$ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 1 1 0 0 0 0		sets to 8-bit operation, selects 1-line display and $V_{LCD} = V_0$
3	display mode on/off control 0 0 0 0 0 0 1 1 1 0	_	turns on display and cursor; entire display is blank after initialization
4	entry mode set 0 0 0 0 0 0 0 1 1 0	_	sets mode to increment the address by 1 and to shift the cursor to the right at the time of the write to the DD/CGRAM; display is not shifted
5	'write data' to CGRAM/DDRAM 1 0 0 1 0 1 0 0 0 0	**P**_	writes 'P'; the DDRAM has already been selected by initialization at power-on; the cursor is incremented by 1 and shifted to the right
6	'write data' to CGRAM/DDRAM 1 0 0 1 0 0 1 0 0 0	**PH**_	writes 'H'
7 to 11			
12	'write data' to CGRAM/DDRAM 1 0 0 1 0 1 0 0 1 1	**PHILIPS**_	writes 'S'
13	entry mode set 0 0 0 0 0 0 0 1 1 1	**PHILIPS**_	sets mode for display shift at the time of write
14	'write data' to CGRAM/DDRAM 1 0 0 0 1 0 0 0 0 0	**HILIPS** _	writes space
15	'write data' to CGRAM/DDRAM 1 0 0 1 0 0 1 1 0 1	**ILIPS M**_	writes 'M'
16			

STEP	INSTRUCTION	DISPLAY	OPERATION
17	'write data' to CGRAM/DDRAM 1 0 0 1 0 0 1 1 1 1	**MICROKO_**	writes 'O'
18	cursor/display shift 0 0 0 0 0 1 0 0 0 0	**MICROKO**	shifts only the cursor position to the left
19	cursor/display shift 0 0 0 0 0 1 0 0 0 0	**MICROKO**	shifts only the cursor position to the left
20	'write data' to CGRAM/DDRAM 1 0 0 1 0 0 0 0 1 1	**ICROCO**	writes 'C' correction; the display moves to the left
21	cursor/display shift 0 0 0 0 0 1 1 1 0 0	**MICROCO**	shifts the display and cursor to the right
22	cursor/display shift 0 0 0 0 0 1 0 1 0 0	**MICROCO_**	shifts only the cursor to the right
23	'write data' to CGRAM/DDRAM 1 0 0 1 0 0 1 1 0 1	**ICROCOM_**	writes 'M'
24			
25	return home 0 0 0 0 0 0 0 0 1 0	**PHILIPS M**	returns both display and cursor to the original position (address 0)

Table 15 8-bit operation, 1-line display and icon example; using external reset (character set 'A')

STEP	INTRODUCTION	DISPLAY	OPERATION
1	power supply on (PCF2119x is initialized by the external reset)		initialized; no display appears
2	function set RS R/$\overline{W}$ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 1 1 0 0 0 0		sets to 8-bit operation, selects 1-line display and $V_{LCD} = V_0$
3	display mode on/off control 0 0 0 0 0 0 1 1 1 0	_	turns on display and cursor; entire display is blank after initialization
4	entry mode set 0 0 0 0 0 0 0 1 1 0	_	sets mode to increment the address by 1 and to shift the cursor to the right at the time of the write to the DD/CGRAM; display is not shifted
5	set CGRAM address 0 0 0 1 0 0 0 0 0 0	_	sets the CGRAM address to position of character 0; the CGRAM is selected
6	'write data' to CGRAM/DDRAM 1 0 0 0 0 0 1 0 1 0	_	writes data to CGRAM for icon even phase; icons appears
7			
8	set CGRAM address 0 0 0 1 1 1 0 0 0 0	_	sets the CGRAM address to position of character 4; the CGRAM is selected
9	'write data' to CGRAM/DDRAM 1 0 0 0 0 0 1 0 1 0	_	writes data to CGRAM for icon odd phase
10			
11	function set 0 0 0 0 1 1 0 0 0 1	_	sets H = 1
12	icon/power control 0 0 0 0 0 0 1 0 1 0	_	icons blink
13	function set 0 0 0 0 1 1 0 0 0 1	_	sets H = 0

STEP	INTRODUCTION	DISPLAY	OPERATION
14	set DDRAM address 0 0 1 0 0 0 0 0 0 0		sets the DDRAM address to the first position; DDRAM is selected
15	'write data' to CGRAM/DDRAM 1 0 0 1 0 1 0 0 0 0	**P_**	writes 'P'; the cursor is incremented by 1 and shifted to the right
16	'write data' to CGRAM/DDRAM 1 0 0 1 0 0 1 0 0 0	**PH_**	writes 'H'
17 to 20			
21	return home 0 0 0 0 0 0 0 0 1 0	**PHILIPS**	returns both display and cursor to the original position (address 0)

Table 16 8-bit operation, 2-line display example; using external reset

STEP	INTRODUCTION	DISPLAY	OPERATION
1	power supply on (PCF2119x is initialized by the external reset)		initialized; no display appears
2	function set RS R/$\overline{W}$ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 1 1 1 0 0 0		sets to 8-bit operation; selects 2-line display and voltage generator off
3	display on/off control 0 0 0 0 0 0 1 1 1 0	_	turns on display and cursor; entire display is blank after initialization
4	entry mode set 0 0 0 0 0 0 0 1 1 0	_	sets mode to increment the address by 1 and to shift the cursor to the right at the time of write to the CG/DDRAM; display is not shifted
5	'write data' to CGRAM/DDRAM 1 0 0 1 0 1 0 0 0 0	**P_**	writes 'P'; the DDRAM has already been selected by initialization at power-on; the cursor is incremented by 1 and shifted to the right
6 to 10			
11	'write data' to CGRAM/DDRAM 1 0 0 1 0 1 0 0 1 1	**PHILIPS_**	writes 'S'
12	set DDRAM address 0 0 1 1 0 0 0 0 0 0	**PHILIPS** **_**	sets DDRAM address to position the cursor at the head of the 2nd line
13	'write data' to CGRAM/ DDRAM 1 0 0 1 0 0 1 1 0 1	**PHILIPS** **M_**	writes 'M'
14 to 19			

STEP	INTRODUCTION	DISPLAY	OPERATION
20	'write data' to CGRAM/DDRAM 1 0 0 1 0 0 1 1 1 1	**PHILIPS MICROCO_**	writes 'O'
21	'write data' to CGRAM/DDRAM 0 0 0 0 0 0 0 1 1 1	**PHILIPS MICROCO_**	sets mode for display shift at the time of write
22	'write data' to CGRAM/DDRAM 1 0 0 1 0 0 1 1 0 1	**HILIPS ICROCOM_**	writes 'M'; display is shifted to the left; the first and second lines shift together
23			
24	return home 0 0 0 0 0 0 0 0 1 0	**PHILIPS MICROCOM**	returns both display and cursor to the original position (address 0)

Table 17 Example of I²C-bus operation; 1-line display (using external reset, assuming SA0 = V_{SS}; note 1)

STEP	I²C BYTE	DISPLAY	OPERATION
1	I²C-bus start		initialized; no display appears
2	slave address for write SA6 SA5 SA4 SA3 SA2 SA1 SA0 R/$\overline{W}$ Ack 0 1 1 1 0 1 0 0 1		during the acknowledge cycle SDA will be pulled-down by the PCF2119x
3	send a control byte for 'function set' Co RS 0 0 0 0 0 0 Ack 0 0 0 0 0 0 0 0 1		control byte sets RS for following data bytes
4	function set DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 0 1 X 0 0 0 0 1		selects 1-line display and $V_{LCD} = V_0$; SCL pulse during acknowledge cycle starts execution of instruction
5	display on/off control DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 0 0 0 1 1 1 0 1	_	turns on display and cursor; entire display shows character 20H (blank in ASCII-like character sets)
6	entry mode set DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 0 0 0 0 1 1 0 1	_	sets mode to increment the address by 1 and to shift the cursor to the right at the time of write to the DDRAM or CGRAM; display is not shifted
7	I²C start	_	for writing data to DDRAM, RS must be set to 1; therefore a control byte is needed
8	slave address for write SA6 SA5 SA4 SA3 SA2 SA1 SA0 R/$\overline{W}$ Ack 0 1 1 1 0 1 0 0 1	_	
9	send a control byte for 'write data' Co RS 0 0 0 0 0 0 Ack 0 1 0 0 0 0 0 0 1	_	
10	'write data' to DDRAM DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 1 0 0 0 0 1	**P**_	writes 'P'; the DDRAM has been selected at power-up; the cursor is incremented by 1 and shifted to the right
11	'write data' to DDRAM DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 0 1 0 0 0 1	**PH**_	writes 'H'

STEP	I²C BYTE	DISPLAY	OPERATION
12 to 15			
16	'write data' to DDRAM DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 1 0 0 1 1 1	**PHILIPS_**	writes 'S'
17	(optional I²C stop) I²C start + slave address for write (as step 8)	**PHILIPS_**	
18	control byte Co RS 0 0 0 0 0 0 Ack 1 0 0 0 0 0 0 0 1	**PHILIPS_**	
19	return home DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 0 0 0 0 0 1 0 1	**PHILIPS**	sets DDRAM address 0 in address counter (also returns shifted display to original position; DDRAM contents unchanged); this instruction does not update the Data Register (DR)
20	I²C start	**PHILIPS**	
21	slave address for read SA6 SA5 SA4 SA3 SA2 SA1 SA0 R/$\overline{W}$ Ack 0 1 1 1 0 1 0 1 1	**PHILIPS**	during the acknowledge cycle the content of the DR is loaded into the internal I²C-bus interface to be shifted out; in the previous instruction neither a 'set address' nor a 'read data' has been performed; therefore the content of the DR was unknown; the R/W has to be set to 1 while still in I²C-write mode
22	control byte for read Co RS 0 0 0 0 0 0 Ack 0 1 1 0 0 0 0 0 1	**PHILIPS**	DDRAM content will be read from following instructions
23	'read data': 8 × SCL + master acknowledge; note 2 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack X X X X X X X X 0	**PHILIPS**	8 × SCL; content loaded into interface during previous acknowledge cycle is shifted out over SDA; MSB is DB7; during master acknowledge content of DDRAM address 01 is loaded into the I²C-bus interface

STEP	I²C BYTE	DISPLAY	OPERATION
24	'read data': 8 × SCL + master acknowledge; note 2 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 0 1 0 0 0 0	PHILIPS	8 × SCL; code of letter 'H' is read first; during master acknowledge code of 'I' is loaded into the I²C interface
25	'read data': 8 × SCL + no master acknowledge; note 2 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 0 1 0 0 1 1	PHILIPS	no master acknowledge; after the content of the I²C-bus interface register is shifted out no internal action is performed; no new data is loaded to the interface register, data register is not updated, address counter is not incremented and cursor is not shifted
26	I²C stop	PHILIPS	

Notes

1. X = don't care.
2. SDA is left at high-impedance by the microcontroller during the read acknowledge.

Table 18 Initialization by instruction, 8-bit interface (note 1)

STEP										DESCRIPTION
power-on or unknown state										
					↓					
wait 2 ms after external reset has been applied										
					↓					
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	BF cannot be checked before this instruction
0	0	0	0	1	1	X	X	X	X	function set (interface is 8 bits long)
					↓					
wait 2 ms										
					↓					
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	BF cannot be checked before this instruction
0	0	0	0	1	1	X	X	X	X	function set (interface is 8 bits long)
					↓					
wait more than 40 μs										
					↓					
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	BF cannot be checked before this instruction
0	0	0	0	1	1	X	X	X	X	function set (interface is 8 bits long)
					↓					BF can be checked after the following instructions; when BF is not checked, the waiting time between instructions is the specified instruction time (see Table 4)
					↓					
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	function set (interface is 8 bits long); specify the number of display lines
0	0	0	0	1	1	0	M	0	H	
0	0	0	0	0	0	1	0	0	0	display off
0	0	0	0	0	0	0	0	0	1	clear display
0	0	0	0	0	0	0	1	I/D	S	entry mode set
					↓					
Initialization ends										

Note

1. X = don't care.

Table 19 Initialization by instruction, 4-bit interface; not applicable for I²C-bus operation

STEP						DESCRIPTION
power-on or unknown state						
Wait 2 ms after external reset has been applied						
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	BF cannot be checked before this instruction
0	0	0	0	1	1	function set (interface is 8 bits long)
Wait 2 ms						
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	BF cannot be checked before this instruction
0	0	0	0	1	1	function set (interface is 8 bits long)
Wait 40 µs						
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	BF cannot be checked before this instruction
0	0	0	0	1	1	function set (interface is 8 bits long)
						BF can be checked after the following instructions; when BF is not checked, the waiting time between instructions is the specified instruction time (see Table 4)
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	function set (set interface to 4 bits long)
0	0	0	0	1	0	interface is 8 bits long
0	0	0	0	1	0	function set (interface is 4 bits long)
0	0	0	M	0	H	specify number of display lines
0	0	0	0	0	0	
0	0	1	0	0	0	display off
0	0	0	0	0	0	clear display
0	0	0	0	0	1	
0	0	0	0	0	0	entry mode set
0	0	0	1	I/D	S	
Initialization ends						

17 BONDING PAD LOCATIONS

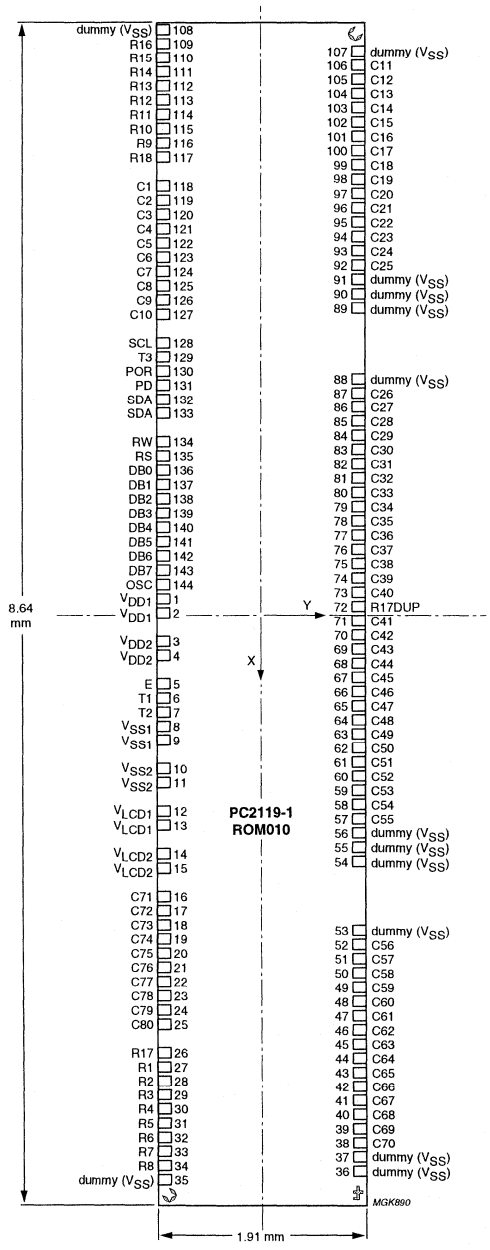


Fig.30 Bonding pad locations.

Table 20 Bonding pad locations

Dimensions in μm; all x/y coordinates are referenced to centre of chip; see Fig.30

SYMBOL	PAD	X	Y
V_{DD1}	1	−117	−779
V_{DD1}	2	−16	−779
V_{DD2}	3	+185	−779
V_{DD2}	4	+286	−779
E	5	+486	−779
T1	6	+587	−779
T2	7	+688	−779
V_{SS1}	8	+789	−779
V_{SS1}	9	+889	−779
V_{SS2}	10	+1090	−779
V_{SS2}	11	+1191	−779
V_{LCD1}	12	+1393	−779
V_{LCD1}	13	+1493	−779
V_{LCD2}	14	+1695	−779
V_{LCD2}	15	+1795	−779
C71	16	+1996	−779
C72	17	+2097	−779
C73	18	+2198	−779
C74	19	+2298	−779
C75	20	+2399	−779
C76	21	+2499	−779
C77	22	+2600	−779
C78	23	+2701	−779
C79	24	+2801	−779
C80	25	+2902	−779
R17	26	+3103	−779
R1	27	+3204	−779
R2	28	+3304	−779
R3	29	+3405	−779
R4	30	+3505	−779
R5	31	+3606	−779
R6	32	+3707	−779
R7	33	+3807	−779
R8	34	+3908	−779
Dummy (V_{SS1})	35	+4008	−779
Dummy (V_{SS1})	36	3957	779
Dummy (V_{SS1})	37	3856	779
C70	38	3756	779
C69	39	3655	779
C68	40	3555	779
C67	41	3454	779
C66	42	3353	779
C65	43	3253	779
C64	44	3152	779
C63	45	3052	779
C62	46	2951	779
C61	47	2850	779
C60	48	2750	779
C59	49	2649	779
C58	50	2549	779
C57	51	2448	779
C56	52	2347	779
Dummy (V_{SS1})	53	2247	779
Dummy (V_{SS1})	54	1744	779
Dummy (V_{SS1})	55	1643	779
Dummy (V_{SS1})	56	1543	779
C55	57	1442	779
C54	58	1341	779
C53	59	1241	779
C52	60	1140	779
C51	61	1040	779
C50	62	939	779
C49	63	838	779
C48	64	738	779
C47	65	637	779
C46	66	537	779
C45	67	436	779
C44	68	335	779
C43	69	235	779
C42	70	134	779
C41	71	34	779
R17DUP	72	−67	+779
C40	73	−168	+779
C39	74	−268	+779
C38	75	−369	+779
C37	76	−469	+779

SYMBOL	PAD	X	Y
C36	77	–570	+779
C35	78	–671	+779
C34	79	–771	+779
C33	80	–872	+779
C32	81	–972	+779
C31	82	–1073	+779
C30	83	–1174	+779
C29	84	–1274	+779
C28	85	–1375	+779
C27	86	–1475	+779
C26	87	–1576	+779
Dummy (V_{SS1})	88	–1677	+779
Dummy (V_{SS1})	89	–2180	+779
Dummy (V_{SS1})	90	–2280	+779
Dummy (V_{SS1})	91	–2381	+779
C25	92	–2481	+779
C24	93	–2582	+779
C23	94	–2683	+779
C22	95	–2783	+779
C21	96	–2884	+779
C20	97	–2984	+779
C19	98	–3085	+779
C18	99	–3186	+779
C17	100	–3286	+779
C16	101	–3387	+779
C15	102	–3487	+779
C14	103	–3588	+779
C13	104	–3689	+779
C12	105	–3789	+779
C11	106	–3890	+779
Dummy (V_{SS1})	107	–3990	+779
Dummy (V_{SS1})	108	–4141	–779
R16	109	–4041	–779
R15	110	–3940	–779
R14	111	–3840	–779
R13	112	–3739	–779

SYMBOL	PAD	X	Y
R12	113	–3638	–779
R11	114	–3538	–779
R10	115	–3437	–779
R9	116	–3337	–779
R18	117	–3236	–779
C1	118	–3035	–779
C2	119	–2934	–779
C3	120	–2834	–779
C4	121	–2733	–779
C5	122	–2633	–779
C6	123	–2532	–779
C7	124	–2431	–779
C8	125	–2331	–779
C9	126	–2230	–779
C10	127	–2129	–779
SCL	128	–1928	–779
T3	129	–1827	–779
POR	130	–1726	–779
PD	131	–1626	–779
SDA	132	–1525	–779
SDA	133	–1425	–779
R/$\overline{W}$	134	–1223	–779
RS	135	–1123	–779
DB0/SA0	136	–1022	–779
DB1	137	–922	–779
DB2	138	–821	–779
DB3	139	–720	–779
DB4	140	–620	–779
DB5	141	–519	–779
DB6	142	–419	–779
DB7	143	–318	–779
OSC	144	–217	–779
Rec. Pat. C1	–	+4125	–762
Rec. Pat. C2	–	–4125	+762
Rec. Pat. +	–	4095	762

Table 21 Bump size

PARAMETER	VALUE	UNIT
Type	galvanic pure Au	–
Bump width	70 ±6	μm
Bump length	90 ±6	μm
Bump height	17.5 ±5	μm
Height difference in one die	<2	μm
Convex deformation	<5	μm
Pad size, aluminium	85 × 100	μm
Passivation opening CBB	58 × 78	μm
Wafer thickness	380 ±25	μm

POCSAG Paging Decoder PCF5001

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POCSAG Paging Decoder PCF5001

1 FEATURES

- Wide operating supply voltage range (1.5 to 6.0 V)
- Extended temperature range: –40 to +85 °C (between –40 to –10 °C, minimum supply voltage restricted to 1.8 V)
- Very low supply current (60 μA typ. with 76.8 kHz crystal)
- *"CCIR radio paging Code No 1"* (POCSAG) compatible
- Programmable call termination conditions
- 512 and 1200 bits/s data rates (2400 bits/s with some restrictions), see Section 7.4
- Improved ACCESS® synchronization algorithm
- Supports 4 user addresses (RICs) in two independent frames
- Eight different alert cadences
- Directly drives magnetic or piezo ceramic beeper
- High level alert requires only a single external transistor
- Optional vibrator type alerting
- Silent call storage, up to eight different calls
- Repeat alarm facility
- Programmable duplicate call suppression
- Interfaces directly to UAA2050T, UAA2080 and UAA2082 digital paging receivers
- Programmable receiver power control for battery economy
- On-chip non-volatile EEPROM storage
- On-chip voltage converter with improved drive capability
- Serial microcontroller interface for display pager applications
- Optional visual indication of received call data using a modified RS232 format
- Level shifted microcontroller interface signals
- Alert on low battery
- Optional out-of-range indication.

2 APPLICATIONS

- Alert-only pagers, display pagers
- Telepoint
- Telemetry/data receivers.

3 GENERAL DESCRIPTION

The PCF5001 is a fully integrated low-power decoder and pager controller. It decodes the CCIR radio paging Code No.1 (POCSAG-Code) at 512 and 1200 bits/s data rates. The PCF5001 is fabricated in SACMOS technology to ensure low power consumption at low supply voltages.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF5001T	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
PCF5001H	LQFP32[1]	plastic low profile quad flat package; 32 leads; body 7 × 7 × 1.4 mm	SOT358-1

Note

1. When using IR reflow soldering it is recommended that the Drypack instructions in the *"Quality Reference Handbook"* (order number 9397 750 00192) are followed.

5 BLOCK DIAGRAMS

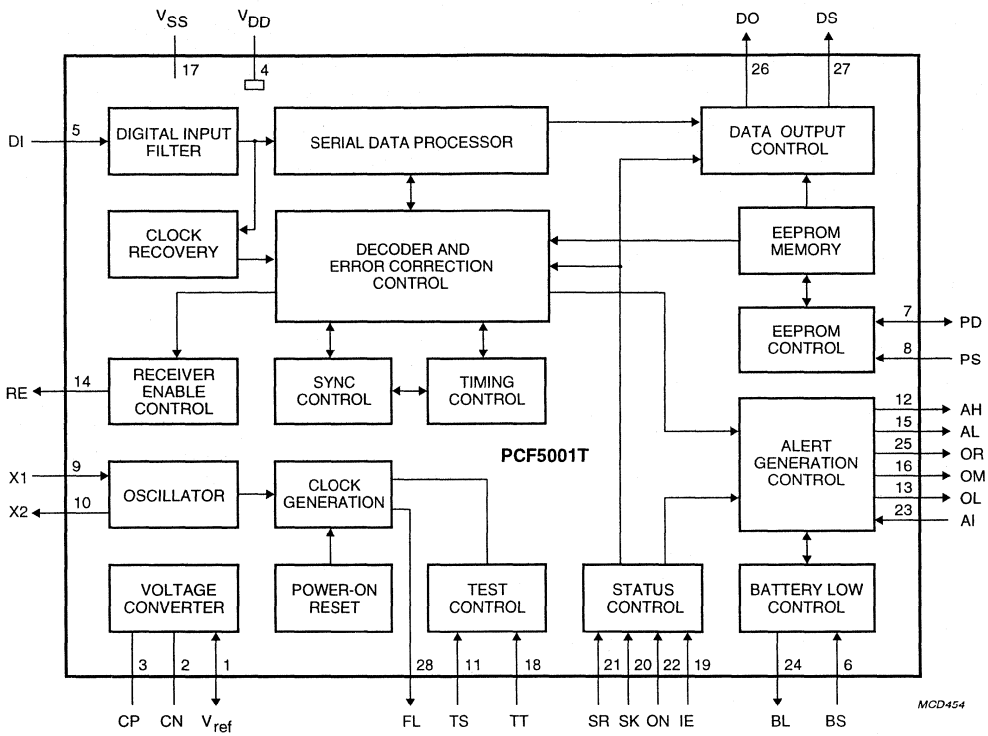


Fig.1 Block diagram (SO28; SOT136-1).

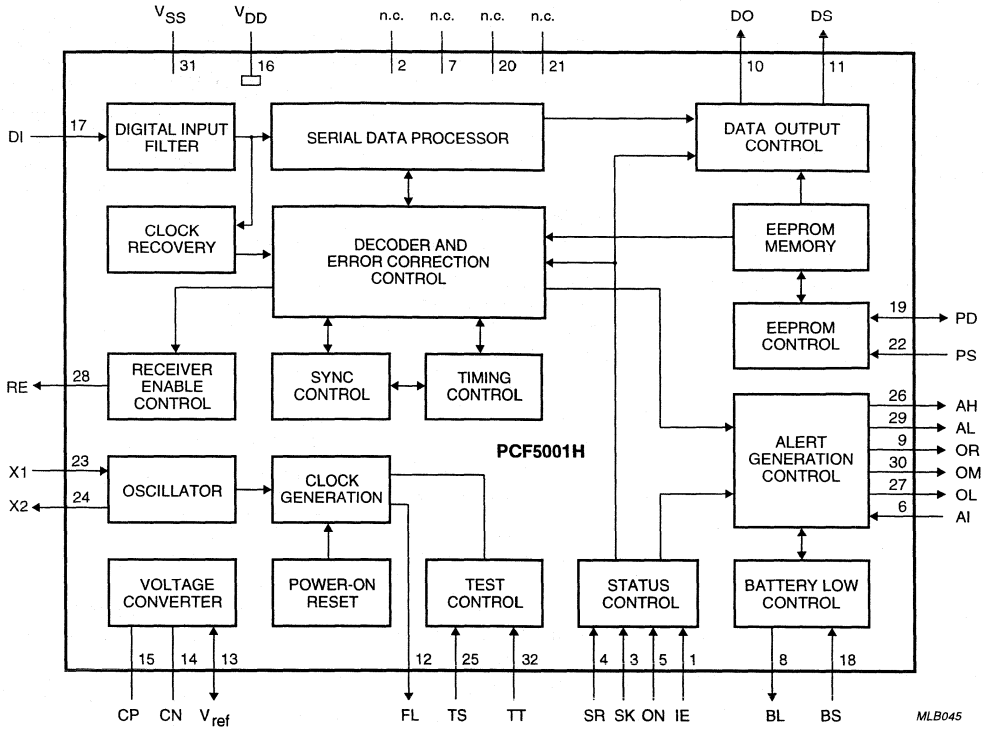


Fig.2 Block diagram (LQFP32; SOT358-1).

6 PINNING

SYMBOL	PIN		DESCRIPTION
	PCF5001T (SOT136-1)	PCF5001H (SOT358-1)	
V_{ref}	1	13	Microcontroller interface reference voltage input/output. The LOW level of pins FL, DS, DO, OR, BL, AI, ON, SK, SR and IE is related to the voltage on V_{ref}. May be driven from an external negative voltage source or must be connected to V_{SS}, if pins CN and CP are left open-circuit. When the on-chip voltage converter is used, this pin provides a doubled negative output voltage.
CN	2	14	Voltage converter external shunt capacitance, negative side. Connect the negative side of the shunt capacitor to this pin, if the on-chip voltage converter function is used.
CP	3	15	Voltage converter external shunt capacitor, positive side. Connect the positive side of the shunt capacitor to this pin, if the on-chip voltage converter function is used.
V_{DD}	4	16	Main positive power supply. This pin is common to all supply voltages and is referred to as 0 V (common).
DI	5	17	Serial data input (POCSAG code). The serial data signal train applied to this pin is processed by the decoder. Pulled LOW by an on-chip pull-down when the receiver is disabled (RE = LOW).
BS	6	18	Battery-low indication input. The decoder samples this input during synchronization scan, when it is in ON or SILENT status and the receiver is enabled (RE = HIGH). A battery-low condition is assumed, if the decoder detects four consecutive samples HIGH. An audible battery-low indication is made by the decoder, when operating in ON status. Normally LOW by the operation of an on-chip pull-down.
PD	7	19	EEPROM programming data input and output. Normally HIGH by the operation of an on-chip pull-up. During programming of the on-chip EEPROM, PD is a bidirectional data and control signal.
PS	8	22	EEPROM programming strobe input. Normally LOW by the operation of an on-chip pull-down. During programming of the on-chip EEPROM, PS is a unidirectional control input.
X1	9	23	Crystal oscillator input. Connect a 32768 Hz or 76800 Hz crystal and a biasing resistor between this pin and X2. In addition, provide a load capacitance to V_{DD}, which may also be used for frequency tuning.
X2	10	24	Crystal oscillator output. Return connection for the external crystal and resistor at X1.
TS	11	25	Scan test mode enable input. Always LOW by operation of an on-chip pull-down.
AH	12	26	Alert HIGH-level output. This output can directly drive an external bipolar transistor to control HIGH-level alerting in conjunction with AL, by means of an alerter or beeper.
OL	13	27	LED indication output. This output can directly drive an external bipolar transistor to control the visual alert function by means of an LED. It may also be used for visual indication of received call data during call reception.

SYMBOL	PIN		DESCRIPTION
	PCF5001T (SOT136-1)	PCF5001H (SOT358-1)	
RE	14	28	Receiver enable output. May be used to control the paging receiver power control input, to minimize power consumption. The decoder provides a HIGH-level at this pin, when receiver operation is requested. Each time the decoder does not require any input data at DI the receiver enable output is LOW.
AL	15	29	Alert LOW-level output. Open drain alert output in anti-phase to AH, to provide LOW-level alerting. HIGH-level alerting is generated in conjunction with AH.
OM	16	30	Vibrator output. This output can directly drive an external bipolar transistor to control a vibrator type alerter.
V_{SS}	17	31	Main negative supply voltage.
TT	18	32	Test mode enable input. Always LOW by operation of an on-chip pull-down.
IE	19	1	Interface enable input. While the interface enable input is active HIGH, operation of the ON, SK, SR, AI, BL and OR inputs and outputs is possible. When IE is LOW the inputs do not respond to applied signals and the outputs are made high-impedance. In **alert-only pager** mode the interface enable input does not have any effect on the operation of inputs ON, SK and SR, but IE must be referenced to LOW or HIGH.
SK	20	3	SILENT state control input. The SILENT control input selects the decoder ON status (LOW-level) or SILENT status (HIGH-level), if the ON input is active HIGH. An on-chip pull-up is provided, if the decoder has been programmed for 'alert-only pager' mode, whereby the pull-up is disabled for **display pager** mode. In 'display pager' mode status change is possible if the interface enable input (IE) is HIGH and the status is latched on the falling edge of IE.
SR	21	4	Status request and reset input. A HIGH-going pulse on this input causes (a) status indication cadence to be generated, if the decoder is not alerting or (b) resetting of a call alert, repeated call alert or battery-low alert, if active or (c) triggers the call store re-alert facility, if **repeat** mode is active. In 'display pager' mode operation of SR is possible only if the interface control input is active. Normally LOW by the operation of an on-chip pull-down.
ON	22	5	On/off control input. The on/off control input selects the decoder ON status (HIGH-level) or OFF status (LOW-level). An on-chip pull-up resistor is provided, if the decoder has been programmed for 'alert-only pager' mode, but the pull-up resistor is disabled for 'display pager' mode. In 'display pager' mode, status change is possible if the interface enable input (IE) is HIGH and the status is latched on the falling edge of IE.
AI	23	6	Alarm input. A HIGH-level on this input causes generation of a continuous HIGH-level alert via AH and AL outputs, if the decoder operates in ON status or OFF status. In addition, the LED output is active independent from the decoder status, but in accordance with AI. Pulsing the input may be used to modulate the alert and LED indication. Normally LOW in 'alert-only pager' mode by operation of an on-chip pull-down.

SYMBOL	PIN		DESCRIPTION
	PCF5001T (SOT136-1)	PCF5001H (SOT358-1)	
BL	24	8	Battery-low indication output. If the decoder encounters a battery-low condition a battery-low output latch is set HIGH. The battery-low output latch may be tested for a battery-low condition, whenever the interface enable input (IE) is active (HIGH), otherwise the battery-low output is made high-impedance. The battery-low output latch is reset only, by switching the decoder to OFF status.
OR	25	9	Out-of-range indication output. Whenever the decoder detects an out-of-range condition an out-of-range output latch is set HIGH after expiry of the programmed out-of-range hold-off time selected by means of special programming (SPF06 and SPF07) of the EEPROM. The out-of-range latch may be tested for an out-of-range condition, whenever the interface enable input (IE) is active (HIGH), otherwise the out-of-range output is made high-impedance. The out-of- range output is reset by detection of a valid data transmission or by switching the decoder to OFF status.
DO	26	10	Serial interface data output. During normal decoder operation, accepted calls and possibly subsequent message data are serially output via this pin in conjunction with the data strobe output (DS). This pin is also used to output the EEPROM contents upon special command, if the decoder is programmed for display pager.
DS	27	11	Serial interface data strobe output. Provides a clock signal for the received call data and EEPROM data appearing at the data output (DO). Each time this output is LOW the data at DO is valid. Additional start and stop conditions allow easy identification of data sequence start and end.
FL	28	12	Frequency reference output. When programmed for 'display pager' mode, this output provides a clock reference with 16384 or 32768 Hz per second, selected by SPF32. See Chapter 7.
n.c.	–	2, 7, 20, 21	Not connected.

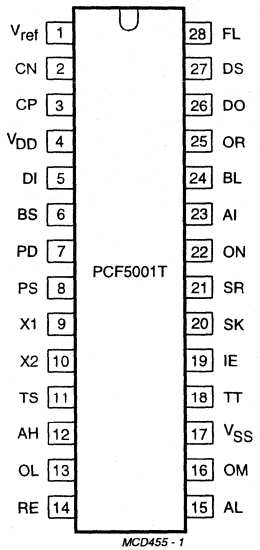


Fig.3 Pin configuration PCF5001T (SOT136-1).

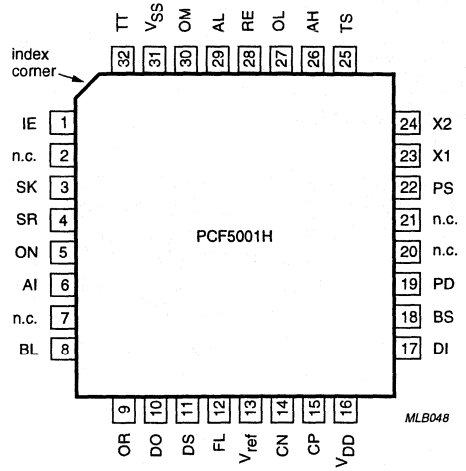


Fig.4 Pin configuration PCF5001H (SOT358-1).

7 FUNCTIONAL DESCRIPTION

The PCF5001 is a very low power Decoder and Pager Controller specifically designed for use in new generation radio pagers. The architecture of the PCF5001 allows for flexible application in a wide variety of radio pager designs.

The PCF5001 is fully compatible with *"CCIR radio paging Code Number 1"* (also known as the POCSAG code) operating at the originally specified 512 bits/s data rate, and also at the newly specified 1200 bits/s data rate (2400 bits/s operation is also possible). The PCF5001 also offers features which extend the basic flexibility and efficiency of this code standard.

7.1 The PCF5001 supports two basic modes of operation

In **alert-only pager** mode only a minimum number of external components are required to build a complete tone-only pager. Selection of operating states ON, OFF or SILENT is achieved using a slider switch interface.

In **display pager** mode the state input logic is switched to a bus interface structure. Received calls and messages are transferred to an external microcontroller via the serial microcontroller interface. A built-in voltage converter with increased drive capabilities can supply doubled supply voltage output, and appropriate logic level shifting on microcontroller interface signals is provided.

Upon reception of valid calls one of eight different call cadences is generated; upon status interrogation status indication tones make the current status of the decoder available to the user.

On-chip non-volatile 114-bit EEPROM storage is provided to hold up to four user addresses, two frame numbers and the programmed decoder configuration.

Synchronization to the input data stream is achieved using the improved ACCESS® algorithm, which allows for data synchronization and re-synchronization without preamble detection while minimizing battery power consumption by receiver power control. One of four error correction algorithms is applied to the received data to optimize the call success rate.

7.2 The POCSAG paging code

A transmission using the *"CCIR Radio paging Code No. 1"* (POCSAG code) is constructed in accordance with the following rules (see Fig.5).

The transmission is started by sending a **preamble**, consisting of at least 576 continuously alternating bits (10101010...). The preamble is followed by an arbitrary number of batch blocks. Only complete batches are transmitted.

Each **batch** comprises 17 codewords of 32 bits each. The first codeword is a synchronization codeword with a fixed pattern. The **sync** word is followed by 8 frames (0 to 7) of 2 codewords each, containing message information. A codeword in a frame can either be an address, message or idle codeword.

Idle codewords also have a fixed pattern and are used to fill empty frames or to separate messages.

Address codewords are identified by an MSB at logic 0 and are coded as shown in Fig.5. A user address or RIC consists of 21 bits. Only the upper 18 bits are encoded in the address codeword (bits 2 to 19). The lower 3 bits designate the frame number (0 to 7) in which the address is transmitted.

Four different call types ('numeric', 'alphanumeric' and two 'alert only' types) can be distinguished. The call type is determined by two function bits in the address codeword (bits 20 and 21).

Alert-only calls consist only of a single address codeword. Numeric and alphanumeric calls have message codewords following the address. A message causes the frame structure to be temporarily suspended. Message codewords are sent until the message is completed, with only the sync words being transmitted in their expected positions.

Message codewords are identified by an MSB at logic 1 and are coded as shown in Fig.5. The message information is stored in a 20-bit field (bits 2 to 21).

The standard data format is determined by the call type: 4 bits per digit for numeric messages and 7 bits per (ASCII) character for alphanumeric messages.

Each codeword is protected against transmission errors by 10 CRC check bits (bits 22 to 31) and an even-parity bit (bit 32). This permits correction of a maximum of 2 random errors or up to 3 errors in a burst of 4 bits (a 4-bit burst error) per codeword.

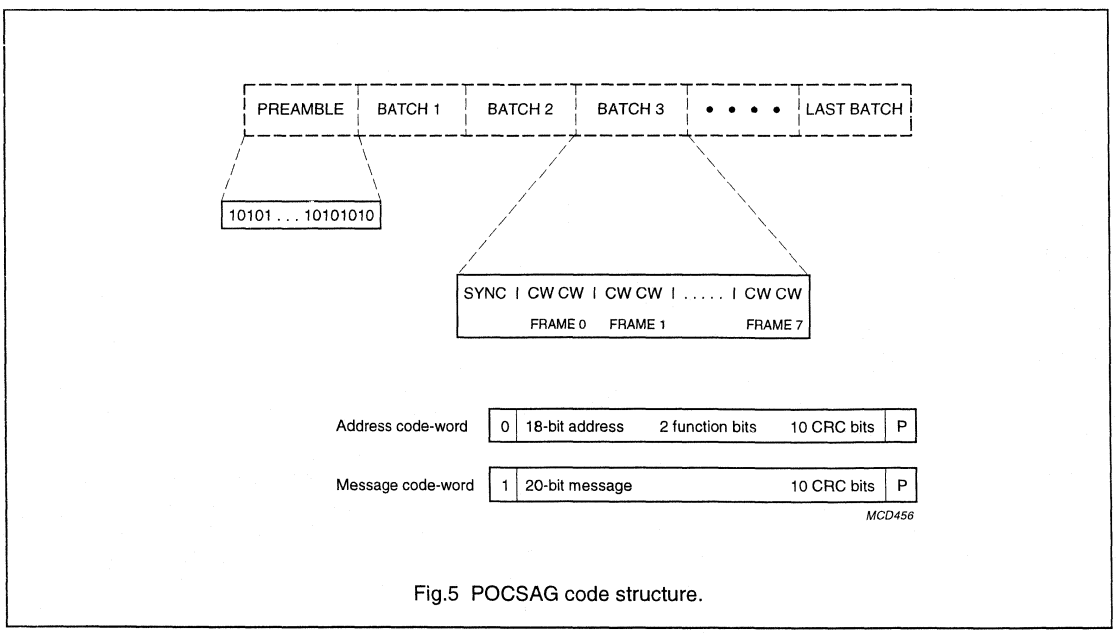


Fig.5 POCSAG code structure.

7.3 Modes and states of the decoder

The PCF5001 supports two basic operating modes:

- 'Alert-only pager' mode
- 'Display pager' mode.

Two further modes, the **programming** mode and the **test** mode, are implemented to program and verify the EEPROM contents and to support pager production and approval tests, respectively.

In 'alert-only pager' mode no external microcontroller is required, see Fig.22. A three position slider switch interface is provided to select the internal state of the decoder. The decoder performs regular scanning of the switch inputs to detect a status change. A push-button interface is provided on the SR input, which is used as input for user acknowledgment actions and status interrogation. Upon reception of valid calls, tone alert cadences are generated. A call storage is provided to store calls received while operating in SILENT status and to recall cadences upon 'repeat' mode operation.
The voltage doubler and the frequency reference output are disabled in this mode.

In 'display pager' mode the PCF5001 operates as decoder and pager controller in combination with an external microcontroller (see Fig.23). The internal states of the decoder are determined by appropriate logic levels on the status inputs. A bus type interface structure is used to interface the decoder to the microcontroller. The decoder's on-chip voltage converter provides doubled supply voltage output to provide a higher supply voltage to the microcontroller and any additional hardware. The logic levels of the interface's input and output signals are level shifted to allow for direct coupling between microcontroller and the decoder. Upon detection of a valid call, address and message information are transferred to the external microcontroller using the serial microcontroller interface. In addition, appropriate call alert cadences are generated.

If the decoder is in one of the two operating modes, it is always in one of the following three internal states:

- OFF status. This is the power saving, inactive status of the PCF5001. The paging receiver is disabled, no decoding of input data takes place. However, the crystal oscillator is kept running to ensure that scanning of the status inputs/status switch is maintained to allow changing into one of the following two active states.
- ON status. This is the normal active status of the decoder. Incoming calls are compared with the user addresses stored in the internal EEPROM. Upon detection of valid calls, alert cadences and LED indication are generated and data is shifted out at the serial microcontroller interface.
- SILENT status. The SILENT status is the same as the ON status with the exception that valid calls no longer cause generation of call alert cadences. Instead, if programmed as 'alert-only pager', the decoder stores up to eight different calls and generates appropriate alert cadences after the decoder has been put back into the ON status. However, special SILENT override calls will cause generation of alert cadences, if enabled.

The decoder operating status is selected as indicated in Table 1.

When programmed for 'alert-only pager' a switch debounce period is applied to the status inputs. For status change and status interrogation in 'display pager' mode, see Figs 6 and 7.

Table 1 Truth table for decoder operating status

ON INPUT	SK INPUT	OPERATING STATUS
0	0	OFF
0	1	OFF (EEPROM transfer mode; note 1)
1	0	ON
1	1	SILENT

Note

1. The EEPROM transfer mode applies to 'display pager' mode only.

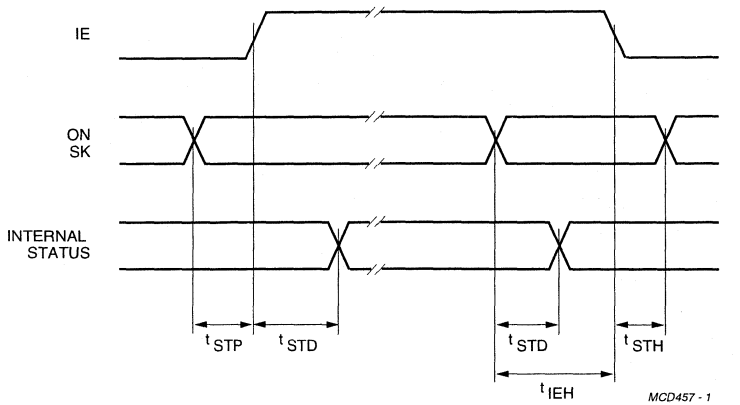


Fig.6 Status change in display pager mode.

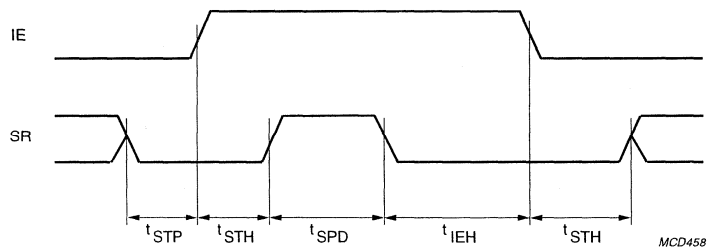


Fig.7 Status interrogation in display pager mode.

7.4 Decoding of the POCSAG data stream

The POCSAG coded input data stream is first noise filtered by a digital filter. From the filtered data a sampling clock synchronous to the data rate is derived. The PCF5001 supports 512 bits/s and 1200 bits/s data rates. This results in a 512 Hz or 1200 Hz sampling clock frequency, respectively. Synchronization on the POCSAG code structure is performed using the improved Philips ACCESS® algorithm, which employs a state machine with six internal states.

A data rate of 2400 bits/s is possible if an external clock generator of 153.6 kHz is connected to X1. The minimum supply voltage is then −1.8 V.

The receiver enable output is activated a period equal to t_{RXON} before the input data is actually needed. The decoder has first to achieve bit and word synchronization before it can receive calls. The algorithm searches first for the preamble and then for synchronization codeword patterns.

This is carried out for the duration of 3 batches in **power-on** mode or 1 batch (=preamble duration) in **preamble receive** mode. Error correction algorithms are applied to the data before it is compared with preamble and synchronization codeword patterns.
The synchronization process is terminated and thus **data receive** mode is entered as soon as synchronization codewords are seen at the beginning of each batch.

The decoder handles loss of synchronization in three steps:

1. If the decoder fails to detect the synchronization pattern at the beginning of the current batch it continues data reception as normal. This **data fail** mode is signalled in the message output when an address codeword was received, as shown in Table 4.
2. If also at the beginning of the next batch no synchronization codeword can be detected, the algorithm assumes a small bit shift in the **fade recovery** mode and performs more synchronization codeword checks around the expected position for the following 15 batches. Call reception is suspended.
3. If it fails to re-synchronize in the 'fade recovery' mode, the **carrier off** mode is selected, in which the decoder attempts to regain synchronization by bit-wise shifting its synchronization scan window. Using this technique re-synchronization is obtained within a continuous data stream of at least 18 batches without preamble detection.

In 'data receive' mode, the input data stream is sampled at the synchronization codeword position and the programmed frame positions. The received codewords are error corrected and then, if address codewords, compared with the stored user addresses related to that frame.

On detection of a valid call, the decoder performs the following three operations:

1. Set a store for call alert cadence generation according to the combination of the function bits in the accepted address codeword. The call alert cadence will not be generated before the call has been terminated.
2. Keep the receiver enable output (RE) active and receive subsequent message codewords, until any of the call termination criteria are fulfilled.
3. Trigger the serial message transfer by sending a start condition and transfer deformatted message codewords as attached to the address codeword via the serial microcontroller interface to an external microcontroller, followed by a stop condition.

Normally call termination is assumed, when a valid idle or address codeword is received. On reception of uncorrectable codewords, call termination takes place in accordance with conditions shown in Table 2.

Table 2 Call termination on error

SPF12	SPF13	CALL TERMINATION EVENT
0	X[1]	Any two consecutive codewords or the codeword directly following the address codeword uncorrectable.
1	0	Any single codeword uncorrectable.
1	1	Any two consecutive codewords uncorrectable.

Note

1. X = don't care.

7.5 Generation of output signals

The PCF5001 provides output indications for call alert, repeat mode alert, out of range alert, battery-low alert, status indication alert and start-up alert. Some of the alert functions may be freely configured by programming of SPF bits within the EEPROM.

Table 3 shows the outputs which are used for special output indications, if the decoder operates in ON status.

Remark: reception of special SILENT override calls causes the decoder to generate call alert indication via AL and AH even if it operates in SILENT status.

Table 3 Output signals

ALERT FUNCTION	OUTPUT ACTIVE(1)					
	AL	AH	OL	OM	OR	BL
Start-up	(yes)	–	yes	yes	–	–
Status indication	yes	–	–	–	–	–
Call reception	(yes)	(yes)	yes	SPF11	–	–
Repeat mode	(SPF16)	(SPF16)	SPF16	–	–	–
Out-of-range	–	–	SPF15	–	yes	–
Battery-low	(yes)	(yes)	–	–	–	yes
Alarm input	(yes)	(yes)	yes	–	–	–

Note

1. Entries in parenthesis are not valid, if the decoder operates in SILENT status.

7.6 Alerter

The PCF5001 provides the AL and AH outputs for acoustical LOW-level and HIGH-level signalling. LOW-level alerting is provided by the AL output only. For HIGH-level alerting both, AL and AH are active in anti-phase. The square-wave output signals produce tone alert cadences by means of a magnetic or piezo ceramic beeper. The alert frequency, 2048 Hz or 2731 Hz square-wave, is selected by programming of SPF31.

When valid calls are received while operating in ON status, the PCF5001 generates call alert cadences. The first four seconds are generated at LOW-level, a further twelve seconds are generated at HIGH-level. Alert tone generation and LED indication automatically terminate after sixteen seconds unless terminated by pulsing the status request and reset input (SR). Call alert generation is inhibited until completion of message codeword reception and the termination word is sent by the decoder. Call alert generation commences after an alert delay period, t_{ALD}, at the earliest, see Fig.8. Call alert deletion is possible during the alert delay period.

The call alert cadence is modulated according to the two function bits (FC) in the received address codeword, see Fig.9.

Valid calls received on RIC B or RIC D cause the alerter frequency to be warbled by means of an additional 16 Hz and 1024 Hz signal (respective 1365 Hz for SPF31 = 1) as opposed to RIC A and RIC C where no alert frequency warble takes place. Thus, eight different call cadences are distinguishable.

ON status interrogation by the status request and reset input (SR) the PCF5001 generates a status cadence at LOW-level, in accordance with the present internal decoder status (see Fig.10).

When detecting a battery-low condition the PCF5001 provides a battery-low indication. Operating in ON status causes generation of a battery-low alert at HIGH-level for sixteen seconds or until terminated by pulsing SR. Operating in SILENT status or 'repeat' mode the battery-low alert is stored and inhibited until switching to ON status.

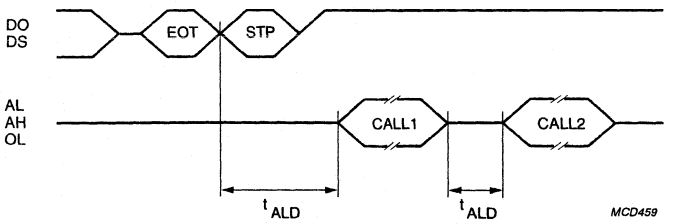


Fig.8 Call alert delay.

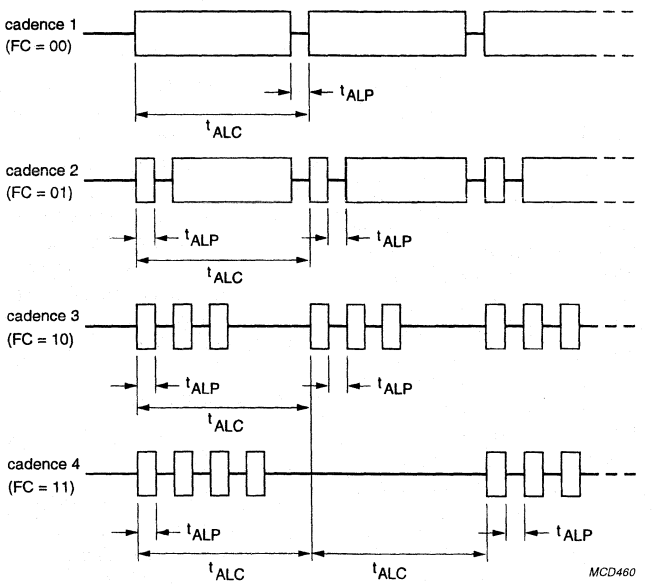


Fig.9 Call alert cadences.

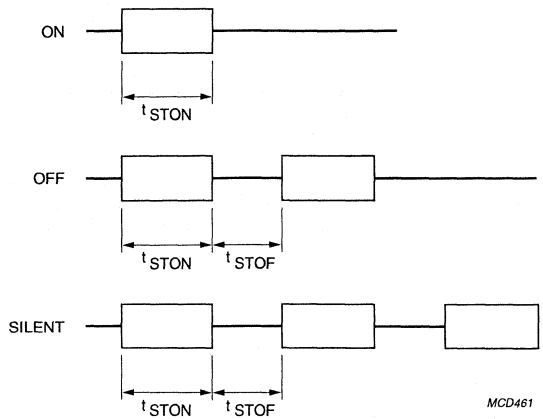


Fig.10 Status indication cadences.

7.7 Silent call storage and repeat mode

When programmed for alert only pager the PCF5001 provides a call alert storage for storing of call alerts received during SILENT status or for call alerts which caused the decoder to enter **repeat** mode. Call alert is not stored, when call indication is terminated by action of the status request and reset input (SR).

Allowing the call indication to time-out by expiration of a sixteen second alert operation causes the 'repeat' mode to be entered, while operating in ON status or SILENT status. Such call alerts are stored for later repeated call alert on interrogation by the user. When 'repeat' mode has been entered and the decoder operates in ON status, the repeat call store is interrogated by pulsing the status request and reset input (SR) or on switching to ON status if the decoder operates in SILENT status. When SILENT override calls are received, which entered the 'repeat' mode, interrogation of repeat call store operates as in decoder ON status. After interrogation of repeat call store and subsequent generation of all stored call alerts the call store is cleared and the 'repeat' mode is terminated.

When programmed by means of SPF16, a repeat alert cadence is generated periodically, whenever 'repeat' mode has been entered. Operating in ON status causes the repeat alert cadence to be generated at HIGH-level and warbled by means of an additional 16 Hz and 1024 Hz signal (respective 1365 Hz for SPF31 = 1) as shown in Fig.11. The LED output indicates the same alert cadence and alert warble. In SILENT status only the LED output is active.

No call alert storage occurs when the decoder is programmed for 'display pager' mode.

7.8 Duplicate Call Suppression

The PCF5001 provides a Duplicate Call Suppression with time-out facility, to identify duplicate call reception. When selected by programming of SPF14, the PCF5001 inhibits any duplicate call alert in 'alert-only pager' mode.
In 'display pager' mode, duplicate call indication is achieved only via the serial microcontroller interface. A call is assumed to be duplicate if its address and function bit setting is equal to the latest received call, which initialized the call address and function bit reference. The Duplicate Call Suppression time-out is selectable by programming of SPF06 and SPF07.

7.9 LED indicator

The PCF5001 provides for visual signalling using a LED via output OL.

Call alert indication is provided by the LED with the same cadence and warble modulation as for the alerter outputs AL and AH. Call alert indication occurs in ON and SILENT status and automatically terminates after sixteen seconds time-out unless terminated by pulsing the status request and reset input (SR).

When detecting an out-of-range condition and enabled by programming of SPF15, the LED output provides an out-of-range indication as shown in Fig.12.

The LED output can be made to provide message data by programming SPF17. Alert signals are inhibited during message data transfer.

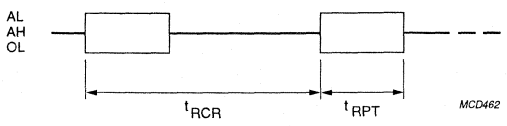


Fig.11 Repeat alert cadence.

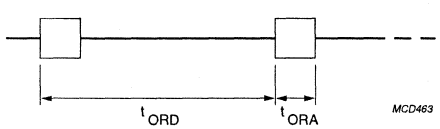


Fig.12 Out-of-range indication.

7.10 Vibrator output

The PCF5001 provides the OM output for activating a vibrator-type alerter for call alert indication. The vibrator output is enabled by programming of SPF11.

Calls received while operating in SILENT status cause activation of the vibrator output for the normal call alert cadence or until terminated by operation of the status request and reset input (SR). SILENT override calls, calls received in decoder ON status and repeated call alerts are alerted normally by the AL and AH outputs.

7.11 Start-up alert

To indicate the establishment of operational condition whenever the decoder status has been changed from OFF to ON or SILENT status, the PCF5001 provides a start-up alert indication. Switching from OFF to ON status causes generation of a start-up alert cadence at LOW-level and on the LED output OL (see Fig.13).

When changing from OFF to SILENT status, the start-up alert will be indicated on the LED output and the vibrator output OM.

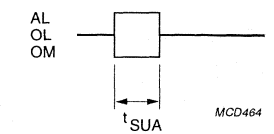


Fig.13 Start-up alert.

7.12 Serial communication interface

To transmit any call message data received to an external microcontroller for post-processing, a serial communication interface has been provided by a serial data output signal DO and a data strobe signal DS as shown in Fig.14.

Upon interrogation the PCF5001 is also able to transfer EEPROM contents via the serial communication interface, see Section 7.21.

7.13 Message data transfer

The transfer of message data via DO and DS is organized in 8-bit words providing additional start and stop conditions as shown in Fig.15.

On reception of a valid call address the PCF5001 generates a start condition and outputs an address word as shown in Fig.15a.

The address word indicates call address, function bit setting and decoder flags as shown in Table 4.

Message codewords received and concatenated to a valid call address are transferred after completion of the address word. The message bits received in the message codewords are split into blocks and are converted to obtain the message words. The message words comprise an error flag to indicate message words, which are derived from uncorrectable message codewords as shown in Table 5.

Message data is output at a rate of 2048 bits/s with a minimum delay of 2 bits between consecutive message words.

Termination of call reception causes a termination word to be transferred, which indicates successful or unsuccessful call termination as shown in Table 6.

Serial data transfer for a received call ends with a stop condition as shown in Fig.15c.

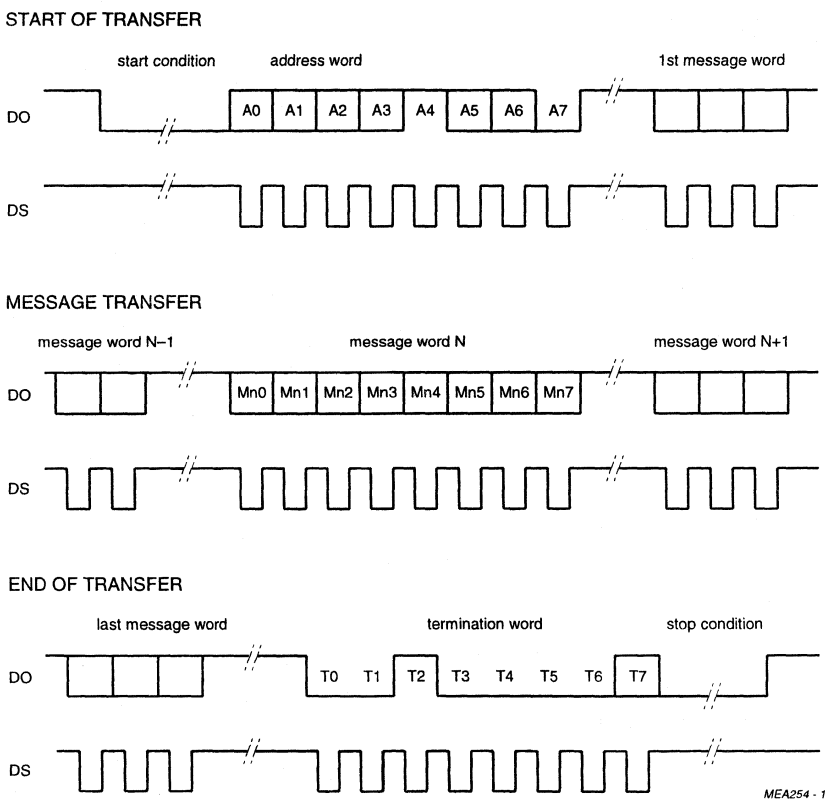
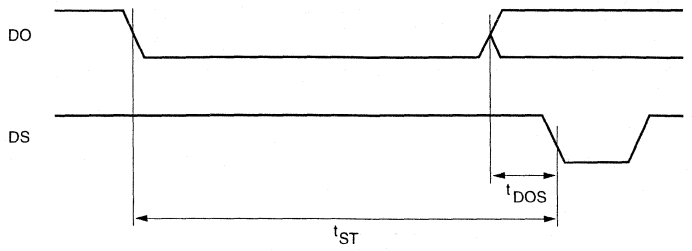
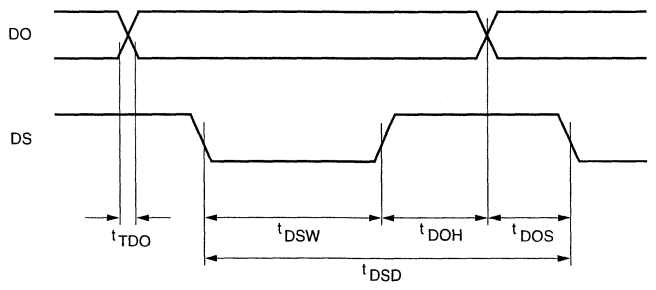


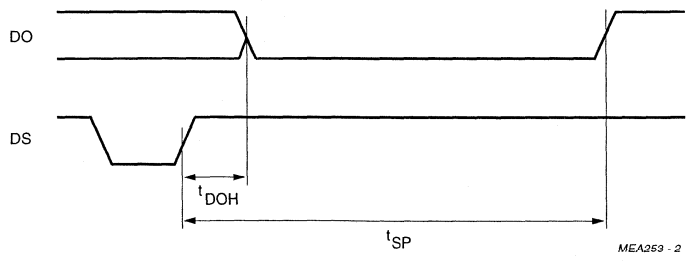
Fig.14 Call data transfer on the serial communication interface.



a.



b.



c.

a. Start condition.
b. Data bit.
c. Stop condition.

Fig.15 Serial communication interface timing.

7.14 Call Data output on LED

When enabled by programming of SPF17 = 1, message data will appear on the LED output OL. The data format and timing are equal to the signal on DO, except that the start/stop conditions are replaced with start/stop bits (respectively 1 and 0). The data format is shown in Fig.16. No alert signals will appear on OL during message data transfer. Consecutive message words have a minimum separation of 1 start bit and 1 stop bit.

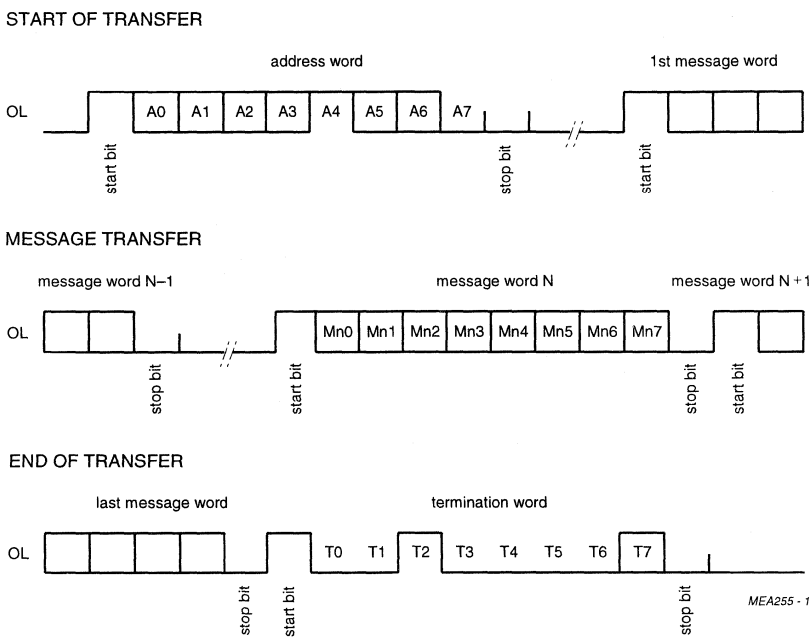


Fig.16 Call data transfer on the LED output.

7.15 Serial communication call data format

Table 4 Address word format

FUNCTION CODE		CALL ADDRESS			BIT 4	SYNC STATUS	DUPLEX CALL	BIT 7
BIT 0 (LSB)	BIT 1 (MSB)	BIT 2	BIT 3	RIC		BIT 5	BIT 6	
Bit 21 of address codeword	bit 20 of address codeword	0	0	A	1	0 = Data Receive; 1 = Data fail	1 = Duplex Call time-out active	0
		0	1	B				
		1	0	C				
		1	1	D				

Table 5 Message word format

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7[1]
LSB			message bits			MSB	error flag

Note

1. Bit 7 = 1, if message codeword could not be corrected.

Table 6 Termination word format

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7[1]
0	0	1	0	0	0	0	error flag

Note

1. Bit 7 = 1, if call termination on error.

7.16 Data conversion

The PCF5001 automatically converts message codewords received in numeric or alphanumeric format into ASCII format. Depending on SPF13 and the function bit setting in the received address codeword a conversion takes place as shown in Table 7.

When a conversion from alphanumeric format to ASCII takes place, the received message codewords are split into message blocks, seven bits in length. After adding the error flag they are transferred as message words.

When a conversion from numeric format to ASCII takes place, the received message codewords are split into blocks, four bits in length. Each four bit block is converted to a seven bit block as shown in Table 8. After adding the error flag they are transferred as message words.

Table 7 Message data conversion

SPF13	FUNCTION BITS		MESSAGE FORMAT
	BIT 20 (MSB)	BIT 21 (LSB)	
0	X[1]	X[1]	numeric
1	0	0	numeric
1	X[1]	1	alphanumeric
1	1	X[1]	alphanumeric

Note

1. X = don't care.

Table 8 Numeric format to ASCII conversion

4-BIT BLOCK				CHARACTER	7-BIT BLOCK						
LSB			MSB		LSB						MSB
0	0	0	0	'0'	0	0	0	0	1	1	0
1	0	0	0	'1'	1	0	0	0	1	1	0
0	1	0	0	'2'	0	1	0	0	1	1	0
1	1	0	0	'3'	1	1	0	0	1	1	0
0	0	1	0	'4'	0	0	1	0	1	1	0
1	0	1	0	'5'	1	0	1	0	1	1	0
0	1	1	0	'6'	0	1	1	0	1	1	0
1	1	1	0	'7'	1	1	1	0	1	1	0
0	0	0	1	'8'	0	0	0	1	1	1	0
1	0	0	1	'9'	1	0	0	1	1	1	0
0	1	0	1	'*'	0	1	0	1	0	1	0
1	1	0	1	'U'	1	0	1	0	1	0	1
0	0	1	1	' '	0	0	0	0	0	1	0
1	0	1	1	'–'	1	0	1	1	0	1	0
0	1	1	1	']'	1	0	1	1	1	0	1
1	1	1	1	'['	1	1	0	1	1	0	0

7.17 Memory Organization

The PCF5001 POCSAG decoder contains non-volatile EEPROM memory to store four user addresses, two frame numbers and specially programmed function bits (SPF01 to SPF32) for decoder application configuration.
The EEPROM is organized as three arrays of 38 bits each as shown in Fig.17.

A user address (or RIC) in POCSAG code comprises of 21 bits, but the three least significant bits are coded in the frame number and therefore not explicitly transmitted. In the PCF5001, addresses A/B and C/D must share the same frame number: addresses A and B reside in frame FR1 (FR10, FR11 and FR12), addresses C and D reside in frame FR2 (FR20, FR21 and FR22). Figure 18 shows an example of decimal address to EEPROM content conversion. Each address must be explicitly enabled by resetting of the associated enable bit.

EEPROM ARRAY 1

BIT18	BIT17	BIT16	BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
A17	A16	A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00	$\overline{ENA}$

BIT37	BIT36	BIT35	BIT34	BIT33	BIT32	BIT31	BIT30	BIT29	BIT28	BIT27	BIT26	BIT25	BIT24	BIT23	BIT22	BIT21	BIT20	BIT19
B17	B16	B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00	$\overline{ENB}$

EEPROM ARRAY 2

BIT18	BIT17	BIT16	BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
C17	C16	C15	C14	C13	C12	C11	C10	C09	C08	C07	C06	C05	C04	C03	C02	C01	C00	$\overline{ENC}$

BIT37	BIT36	BIT35	BIT34	BIT33	BIT32	BIT31	BIT30	BIT29	BIT28	BIT27	BIT26	BIT25	BIT24	BIT23	BIT22	BIT21	BIT20	BIT19
D17	D16	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00	$\overline{END}$

EEPROM ARRAY 3

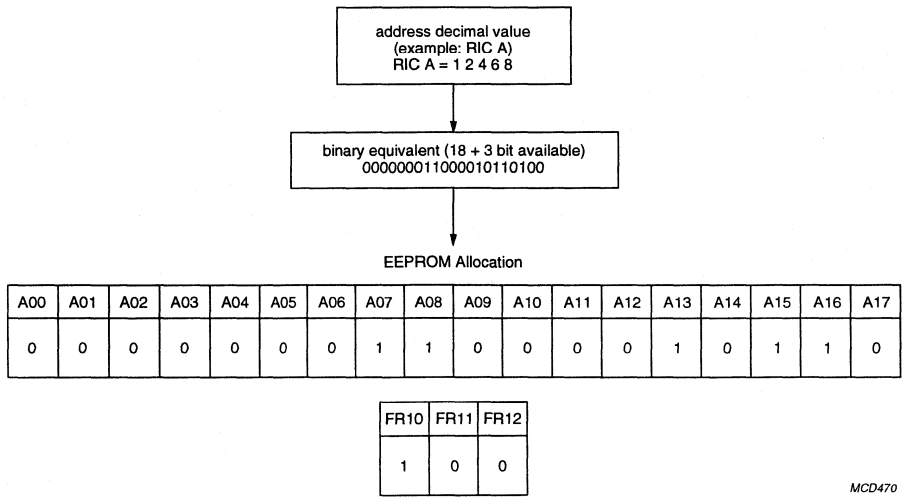
BIT18	BIT17	BIT16	BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
SPF13	SPF12	SPF11	SPF10	SPF09	SPF08	SPF07	SPF06	SPF05	SPF04	SPF03	SPF02	SPF01	FR20	FR21	FR22	FR10	FR11	FR12

BIT37	BIT36	BIT35	BIT34	BIT33	BIT32	BIT31	BIT30	BIT29	BIT28	BIT27	BIT26	BIT25	BIT24	BIT23	BIT22	BIT21	BIT20	BIT19
SPF32	SPF31	SPF30	SPF29	SPF28	SPF27	SPF26	SPF25	SPF24	SPF23	SPF22	SPF21	SPF20	SPF19	SPF18	SPF17	SPF16	SPF15	SPF14

MCD469

A00 represents the MSB of RIC A, B00 is the MSB of RIC C, etc.
FR10 represents the MSB of Frame 1 (valid for RICs A and B), FR20 is the MSB of Frame 2 (RICs C and D).

Fig.17 EEPROM memory organization.



A00 is the MSB of RIC A, FR10 is the MSB of Frame 1.

Fig.18 Decimal address to memory contents conversion example.

7.18 Description of the Special Programmed Function (SPF) bits

The following features can be selected by appropriate programming of the special programmed function bits as shown in Table 9.

Table 9 Special Programmed Function (SPF) bits

SPF	BIT	FUNCTION
SPF01	0	Alert-only pager mode.
	1	Display pager mode.
SPF02	0	512 bits/s data rate.
	1	1200 bits/s data rate, possible with 76.8 kHz crystal only.
SPF03	0	32768 Hz crystal configuration.
	1	76800 Hz crystal configuration.
SPF04, SPF05		Receiver establishment time (depending on data rate).
	00	7.8 ms/512 bits/s; 53.3 ms/1200 bits/s.
	01	15.6 ms/512 bits/s; 6.7 ms/1200 bits/s.
	10	31.3 ms/512 bits/s; 13.3 ms/1200 bits/s.
	11	62.5 ms/512 bits/s; 26.7 ms/1200 bits/s.

SPF	BIT	FUNCTION
SPF06, SPF07		Duplicate call suppression time-out and out-of-range hold-off time-out.
	00	30 s.
	01	60 s.
	10	120 s.
	11	240 s.
SPF08	0	Voltage converter disabled, if SPF01 = 1 ('display pager' mode).
	1	Voltage converter enabled, if SPF01 = 1 ('display pager' mode).
SPF09	0	SILENT override on address C disabled.
	1	SILENT override on address C enabled.
SPF10	0	SILENT override on address D disabled.
	1	SILENT override on address D enabled.
SPF11	0	Vibrator output disabled.
	1	Vibrator output enabled.
SPF12	0	Call termination criteria combination method (note 1).
	1	Call termination criteria defined by SPF13.
SPF13	0	Numeric data deformatting, call termination on first uncorrectable codeword.
	1	Numeric data deformatting on function code 00 only, call termination on two uncorrectable codewords.
SPF14	0	Duplicate call suppression disabled.
	1	Duplicate call suppression enabled.
SPF15	0	Out of range indication at OL output disabled, hold-off period is zero regardless of SPF06 and SPF07 setting.
	1	Out of range indication at OL output enabled, hold-off period is according to SPF06 and SPF07 setting.
SPF16	0	Repeat alert disabled.
	1	Repeat alert enabled.
SPF17	0	Call data output on OL disabled.
	1	Call data output on OL enabled.
SPF18	–	Spare.
SPF19	–	Program always 0.
SPF20 to SPF30	–	Spares.
SPF31	0	Alerter frequency 2048 Hz.
	1	Alerter frequency 2731 Hz.
SPF32	0	Frequency reference output 16384 Hz if SPF01 = 1 ('display pager' mode).
	1	Frequency reference output 32768 Hz if SPF01 = 1 ('display pager' mode).

Note

1. Call termination on:
   a) First codeword immediately following address codeword uncorrectable.
   b) Two consecutive codewords uncorrectable.

7.19 EEPROM Write operation

The **program** mode is entered in OFF status by setting the PD input LOW and the PS input HIGH at any time. The 'program' mode is left and normal operation resumed by either removing the power supply or setting the PD input HIGH after the 38th data bit while continuing to clock the PS input. The three EEPROM arrays can be programmed in any order. Selection of array is made during the second and third pulse on the PS input. The 'program' mode has to be left after programming of each array.

After entering the 'program' mode, keeping input PD LOW during the first pulse on PS selects Memory Write operation. After selection of the current array an erase cycle of duration t_{PEW} has to be carried out, during which the supply voltage at V_{SS} input must be at least V_{PG}. Program data for the selected array is entered bit by bit using PD as data input and the rising edge on PS as data strobe pulse. See Fig.19 for timing during an EEPROM write operation.

After the last bit a special write cycle of duration t_{PEW} has to be carried out again, during which the supply voltage at V_{SS} input must be V_{PG}. During conditions when the supply voltage is increased to V_{PG} the maximum DC ratings at V_{ref} must not be exceeded. When the on-chip voltage converter is enabled a voltage regulator diode or a damping resistor of sufficiently low impedance has to be connected between V_{ref} and V_{SS} to limit the voltage level at V_{ref} during program operation.

7.20 EEPROM Read operation

After entrance to the 'program' mode, keeping input PD HIGH during the first pulse on PS selects Memory Read operation. After selection of the current array the programmed data is output bit-by-bit using PD as data output. A positive edge on PS input switches to the next bit. See Fig.19 for timing during an EEPROM read operation.

7.21 Read-back operation via Microcontroller Interface

In 'display pager' mode, the PCF5001 is capable of delivering the EEPROM contents to an external microcontroller using the serial interface outputs DO and DS. The EEPROM data transfer mode is selected by applying a LOW to input ON and a HIGH to input SK while pulsing the SR input, and the interface is enabled (IE is HIGH). The data transfer is started by a logic HIGH level on SR. The HIGH level on SR must be removed before the end of the tenth output byte, otherwise the transfer is aborted and restarted. The minimum pulse duration corresponds with t_{SPD} in the status interrogation timing (see Fig.7). The transfer is organized as 15-byte transfers. The contents of each array are extended to 40 bits by trailing zeros. The EEPROM data transfer starts with array 1, bit 0. A valid data bit at DO is indicated by a LOW-level on DS as shown in Fig.20.

During EEPROM Read-back operation, the PCF5001 configuration and the outputs FL, OL are undefined. After completion of the Read-Back operation, the PCF5001 will re-enter the programmed configuration.

7.22 Voltage converter

The PCF5001 contains a switched capacitor-type on-chip voltage converter, which can provide doubled supply voltage to the external microcontroller and display control devices. The microcontroller interface signals are level shifted accordingly.

A capacitor of 100 nF (C_S) must be connected between pins CP and CN while a load capacitor of 10 μF is connected to V_{ref} as shown in Fig.23. The voltage converter operates in 'display pager' mode only, when enabled by programming SPF08 (see Table 9).

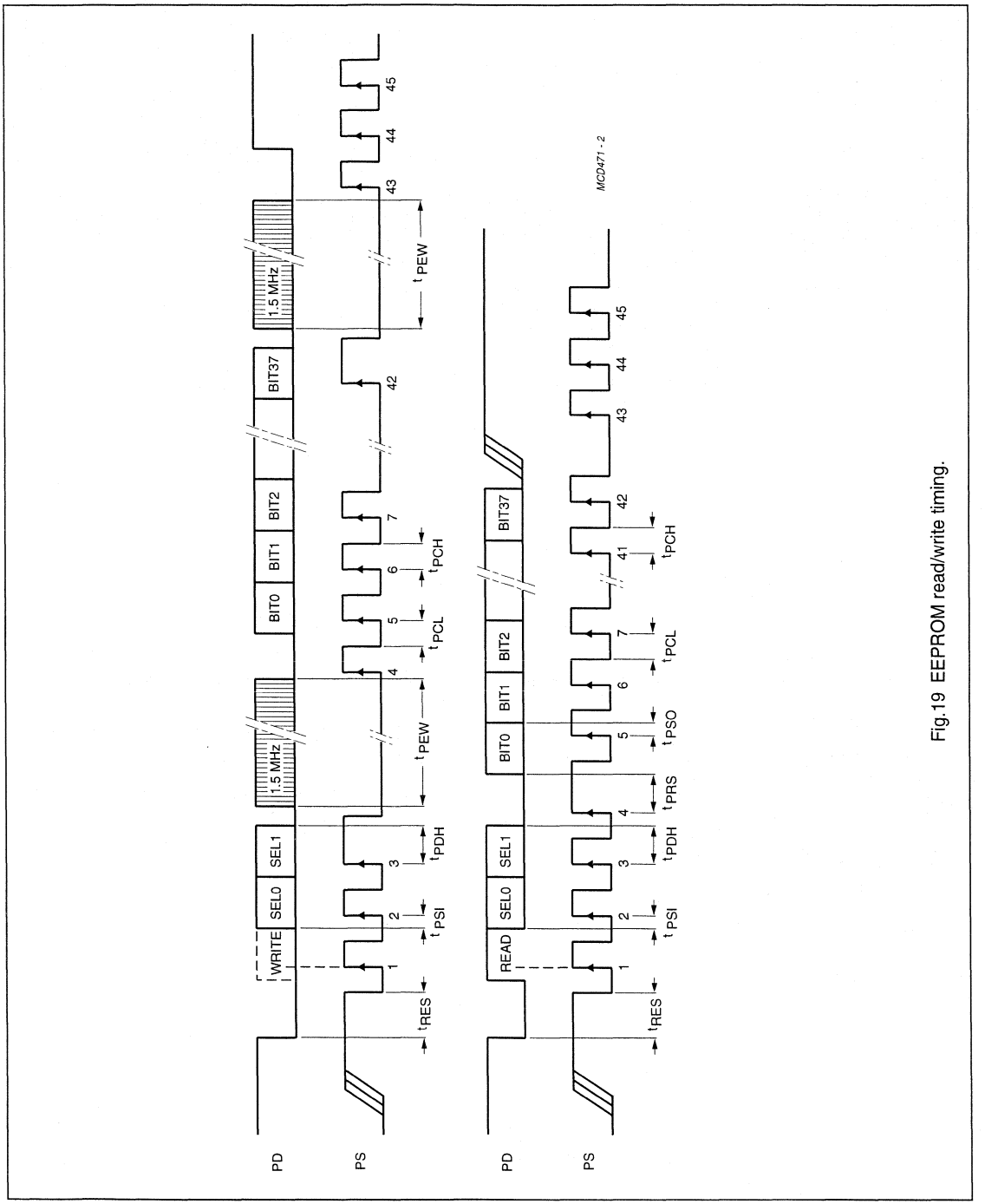


Fig.19 EEPROM read/write timing.

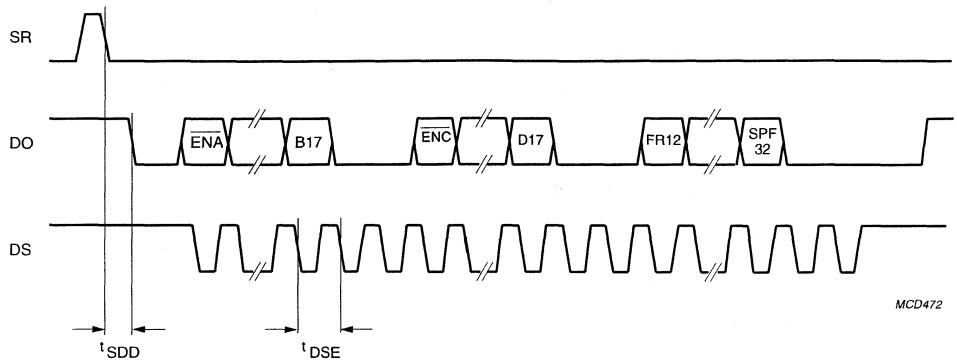


Fig.20 EEPROM data transfer to microcontroller timing.

7.23 Test modes of the decoder

The decoder supports two test modes, which are intended for use during pager production and type approval tests.

7.23.1 Board test mode

'Board test' mode is selected by setting the PD input LOW at any time. In this test mode the following features are provided:

1. Receiver enable output is set constantly HIGH
2. Output AL is activated by a LOW-level on ON input
3. Output AH is activated by a HIGH-level on SR input
4. Outputs OL and OM are activated by a HIGH-level on SK input.

Exit from 'board test' mode is achieved by setting input PD HIGH.

7.23.2 Pager Test Mode (Type Approval Mode)

'Pager test' mode is entered by reception of a valid call while 'board test' mode is active, see above. In 'pager test' mode:

1. Call alert cadences are terminated after 2 seconds
2. Duplicate call suppression is disabled.

Exit from 'pager test' mode is achieved by disconnecting the power supply from the decoder.

8 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{SS}	supply voltage	note 1	+0.5	−8.0	V
V_{PG}	programming supply voltage		−5.5	−	V
V_n	voltage on pins FL, DS, DO, OR, BL, AI, ON, SK, SR and IE		+0.8	V_{ref} − 0.8	V
V_{n1}	input voltage on any other pin		+0.8	V_{SS} − 0.8	V
P_{tot}	total power dissipation		−	250	mW
P_O	power dissipation per output		−	100	mW
$I_{I(max)}$	maximum input current (any input)		−	10	mA
$I_{O(max)}$	maximum output current				
	any output except AL		−	20	mA
	output AL		−	70	mA
T_{amb}	operating ambient temperature		−40	+85	°C
T_{stg}	storage temperature		−55	+125	°C

Note

1. V_{DD} is connected to the substrate (see Fig.1), and is referred to as common, 0 V.

9 DC CHARACTERISTICS

V_{DD} = 0 V; V_{SS} = −2.7 V; V_{ref} = 2.7 V; T_{amb} = 25 °C; unless otherwise specified.
Quartz crystal parameters: f = 76800 Hz; $R_{S(max)}$ = 40 kΩ; C_L = 12 pF.
Decoder Mode programmed as Alert-only (SPF01 = 0).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{SS}	supply voltage	voltage converter disabled; all outputs open-circuit				
		T_{amb} = −10 to +85 °C	−1.5	−2.7	−6.0	V
		T_{amb} = −40 to +85 °C	−1.8	−2.7	−6.0	V
I_{SS}	supply current	note 1	−	−60	−100	µA
V_{PG}	programming supply voltage	note 2	−4.5	−5.0	−5.5	V
I_{PG}	programming supply current		−	−500	−	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs						
V_{IL1}	LOW level input voltage PD, PS, DI, BS, TS, TT and X1		$0.7V_{SS}$	–	–	V
V_{IL2}	LOW level input voltage AI, ON, SR, SK and IE		$0.7V_{ref}$	–	–	V
V_{IH1}	HIGH level input voltage PD, PS, DI, BS, TS, TT and X1		–	–	$0.3V_{SS}$	V
V_{IH2}	HIGH level input voltage AI, ON, SR, SK and IE		–	–	$0.3V_{ref}$	V
I_I	input current					
	BS, PS, TS and TT	$V_I = V_{DD}$	7.0	–	20.0	µA
	PD	$V_I = V_{SS}$	–9.0	–	–24.0	µA
	DI	$V_I = V_{DD}$; RE = 0	7.0	–	20.0	µA
	DI	$V_I = V_{DD}$; RE = 1	0	–	0.5	µA
	ON and SK	$V_I = V_{SS}$	–0.5	–0.8	–1.1	µA
	AI and SR	$V_I = V_{DD}$	7.0	–	20.0	µA
C_i	input capacitance BS, DI, PD, PS, TS, TT, AI, ON, SR, SK, IE and X1		2	–	–	pF
Outputs						
I_{OL}	LOW level output current					
	OL, OM and AH	V_{OL} = –1.35 V	100	–	–	µA
	DO, DS, BL, FL and OR	V_{OL} = –1.35 V	100	–	–	µA
	AL	V_{OL} = –1.5 V	17.5	–	–	mA
	RE	V_{OL} = 2.2 V	200	–	–	µA
I_{OH}	HIGH level output current					
	OL, OM and AH	V_{OH} = –1.35 V	–0.8	–	–1.8	mA
	DO, DS, BL, FL and OR	V_{OH} = –1.35 V	–100	–	–	µA
	AL	AL high-impedance	–	–	–0.2	µA
	RE	V_{OH} = –0.5 V	–1.0	–	–	mA
Oscillator						
C_{XO}	output capacitance X2		–	40	–	pF
g_m	oscillator transconductance	V_{SS} = –1.5 V	15	29	43	µS
		V_{SS} = –6.0 V	25	39	55	µS
V_{PU}	power-up reset threshold voltage		–	–1.2	–	V

Notes

1. All inputs = V_{SS}; voltage converter off; all outputs open-circuit.
2. See Section 7.19 and Chapter 8 for limitations of V_{ref} when programming while the voltage converter is enabled.

10 DC CHARACTERISTICS (WITH VOLTAGE CONVERTER)

V_{DD} = 0 V; V_{SS} = –3.0 V; V_{ref} = –6.0 V; T_{amb} = 25 °C.
Quartz crystal parameters: f = 76800 Hz; $R_{S(max)}$ = 40 kΩ; C_L = 12 pF.
Decoder Mode programmed as Display Pager (SPF01 = 1).
Voltage converter enabled (SPF08 = 1); C_S = 100 nF.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{SS}	supply voltage		–1.5	–	–3.0	V
Voltage converter						
$V_{ref(0)}$	output voltage; no load	V_{SS} = –3.0 V	–5.8	–	–6.0	V
V_{ref}	output voltage	V_{SS} = –2.0 V; I_{ref} = 250 µA	–3.0	–3.5	–	V
I_{ref}	output current	V_{SS} = –2.0 V; V_{ref} = –2.7 V	400	600	–	µA
		V_{SS} = –3.0 V; V_{ref} = –4.5 V	600	900	–	µA
Inputs						
I_I	input current					
	AI, ON, SR and SK	$V_I = V_{ref}$	–	0	–0.5	µA
	ON and SK	$V_I = V_{DD}$	–	0	±0.5	µA
	SR	$V_I = V_{DD}$; V_{ref} = –6.0 V	–	17	–	µA

11 AC CHARACTERISTICS

V_{DD} = 0 V; V_{SS} = –2.7 V; T_{amb} = 25 °C.
Quartz crystal parameters: f = 32768 or 76800 Hz; $R_{S(max)}$ = 40 kΩ; C_L = 12 pF.
Decoder Mode programmed as Display or Alert-only Pager (SPF01 = 1 or 0).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Alert frequency						
f_{AL}	alert frequency	SPF31 = 0	–	2048	–	Hz
f_{AWH}	high alert warble frequency		–	1024	–	Hz
f_{AWL}	low alert warble frequency		–	16	–	Hz
f_{AL}	alert frequency	SPF31 = 1	–	2731	–	Hz
f_{AWH}	high alert warble frequency		–	1365	–	Hz
f_{AWL}	low alert warble frequency		–	16	–	Hz
f_{FL}	output frequency reference at FL	SPF32 = 0	–	16384	–	Hz
		SPF32 = 1	–	32768	–	Hz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Call alert duration						
t_{ALT}	time-out period		–	16	–	s
t_{ALL}	alert time LOW (AL output only)		–	4	–	s
t_{ALH}	alert time HIGH (AH and AL outputs)		–	12	–	s
t_{ALC}	call alert cycle time	see Fig.9	–	1	–	s
t_{ALP}	call alert pulse duration	see Fig.9	–	125	–	ms
t_{ALD}	call alert hold off period	see Fig.8	52	–	–	ms
t_{RPT}	repeat alert duration	see Fig.11	–	–	4	s
t_{RCR}	repeat alert recurrence time	see Fig.11	–	–	15	s
t_{RCP}	repeat alert cycle time		–	–	500	ms
t_{RPD}	repeat alert pulse duration		–	–	250	ms
t_{STON}	status alert time	see Fig.10	–	–	62.5	ms
t_{STOF}	status alert delay	see Fig.10	–	–	62.5	ms
t_{SUA}	start-up alert time	SPF02 = 0; see Fig.13	–	–	500	ms
		SPF02 = 1; see Fig.13	–	–	453	ms
t_{ORA}	out-of-range alert pulse width	see Fig.12	–	–	62.5	ms
t_{ORD}	out-of-range alert time	see Fig.12	–	–	2	s
t_{BLAL}	battery LOW-level alert time		–	–	16	s
Receiver control						
t_{RXT}	RE transition time	C_L = 5 pF	–	–	100	ns
t_{RXON}	RE establishment time	SPF04 = 0; SPF05 = 1	–	7.8	62.5	ms
Data output						
f_{DO}	data output rate		–	2048	–	bits/s
t_{DSD}	strobe period call data	see Fig.15	480	–	495	µs
t_{DSE}	strobe period EEPROM data	see Fig.20	200	488	1150	µs
t_{DSW}	data strobe pulse width	see Fig.15	230	–	250	µs
t_{TDO}	data output transition time	C_L = 10 pF; see Fig.15	–	–	100	ns
t_{DOS}	data output set-up time	see Fig.15	–	–	135	µs
t_{DOH}	data output hold time	see Fig.15	115	–	–	µs
t_{BYD}	consecutive byte delay		1210	–	1225	µs
t_{CWD}	inter-codeword delay	1200 bits/s numeric message	3420	–	–	µs
t_{ST}	start condition set-up time	see Fig.15	4750	–	–	µs
t_{SP}	stop condition set-up time	see Fig.15	595	–	615	µs
t_{STL}	start bit period OL output		480	–	495	µs
t_{SPL}	stop bit period OL output		480	488	495	µs
t_{SDD}	SPF output delay	see Fig.20	1	–	10	ms

12 TIMING CHARACTERISTICS

V_{DD} = 0 V; V_{SS} = −2.7 V; T_{amb} = 25 °C.
Quartz crystal parameters: f = 32768 or 76800 Hz; $R_{S(max)}$ = 40 kΩ; C_L = 12 pF.
Decoder Mode programmed as Display or Alert-only Pager (SPF01 = 1 or 0).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operating frequency dependent						
f_{osc}	oscillator frequency	SPF03 = 0	–	32768	–	Hz
		SPF03 = 1	–	76800	–	Hz
t_{TDI}	data input transition time	see Fig.21	–	–	100	µs
t_{DI1}	data input logic 1	see Fig.21	t_{BIT}	–	∞	
t_{DI0}	data input logic 0	see Fig.21	t_{BIT}	–	∞	
f_{DI}	data input rate	SPF02 = 0	–	512	–	bits/s
t_{BIT}	bit period		–	1.9531	–	ms
t_{CW}	codeword duration		–	62.5	–	ms
t_{PA}	preamble duration		1125	–	–	ms
t_{BAT}	batch duration		–	1062.5	–	ms
f_{DI}	data input rate	SPF02 = 1; f_{osc} = 76800 Hz	–	1200	–	bits/s
t_{BIT}	bit period		–	833.3	–	ms
t_{CW}	codeword duration		–	26.7	–	ms
t_{PA}	preamble duration		480	–	–	ms
t_{BAT}	batch duration		–	453.3	–	ms
Alert only mode (SPF01 = 0)						
t_{SDB}	switch debounce period		–	62.5	–	ms
Display pager mode (SPF01 = 1); see Figs 6 and 7						
t_{STP}	status set-up time	f_{osc} = 32768 Hz	35	–	–	µs
t_{STD}	status change delay		–	–	35	µs
t_{IEH}	interface enable hold time		35	–	–	µs
t_{STH}	status hold time		35	–	–	µs
t_{SPD}	status pulse duration		35	–	–	µs
t_{STP}	status set-up time	f_{osc} = 76800 Hz	15	–	–	µs
t_{STD}	status change delay		–	–	15	µs
t_{IEH}	interface enable hold time		15	–	–	µs
t_{STH}	status hold time		15	–	–	µs
t_{SPD}	status pulse duration		15	–	–	µs

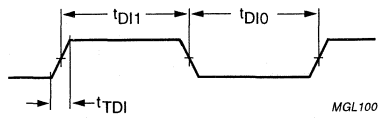


Fig.21 Data input timing.

13 PROGRAMMING CHARACTERISTICS

V_{DD} = 0 V; V_{SS} = V_{PG} = −5.0 V (see notes 1, 2 and 3); V_{ref} = V_{SS}; pins 2 and 3 open-circuit; T_{amb} = 25 °C.
Quartz crystal parameters: f = 32768 Hz; $R_{S(max)}$ = 40 kΩ; C_L = 12 pF.
Decoder in OFF status.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Programming; see Fig.19						
t_{RES}	power-up reset pulse width	note 4	35	–	–	µs
t_{PEW}	erase/write time		10	–	–	ms
f_{EW}	erase/write frequency		1.0	1.5	2.0	MHz
t_{EW}	erase/write cycles		1000	10000	–	–
t_{DR}	data retention time	T_{amb} = 85 °C	10	–	–	years
t_{PCH}	data clock HIGH time	note 4	65	–	–	µs
t_{PCL}	data clock LOW time	note 4	65	–	–	µs
t_{PRS}	read set-up time	note 4	–	–	35	µs
t_{PSI}	data set-up time on input	note 4	35	–	–	µs
t_{PSO}	data set-up time on output	note 4	–	–	35	µs
t_{PDH}	data hold time	note 4	35	–	–	µs

Notes

1. V_{SS} = V_{PG} only required during erase/write (t_{PEW} in Fig.19), otherwise $V_{SS(min)}$ = −1.5 V.
2. Maximum voltage for programming (V_{PG}) is −5.5 V.
3. See Section 7.19 and Chapter 8 for limitations of V_{ref} when programming while the voltage converter is enabled.
4. EEPROM programming is also possible at higher frequencies (76.8 kHz or 153.6 kHz). The timings shown then become proportionally smaller.

14 APPLICATION INFORMATION

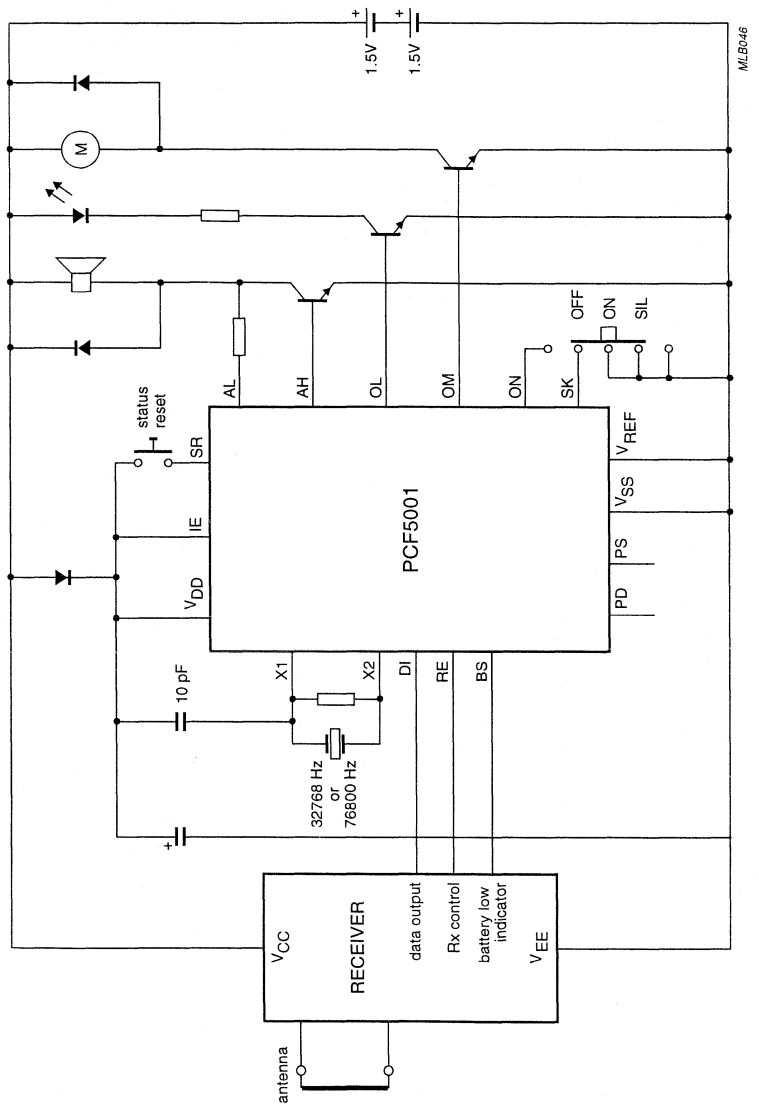


Fig.22 Alert-only pager application example.

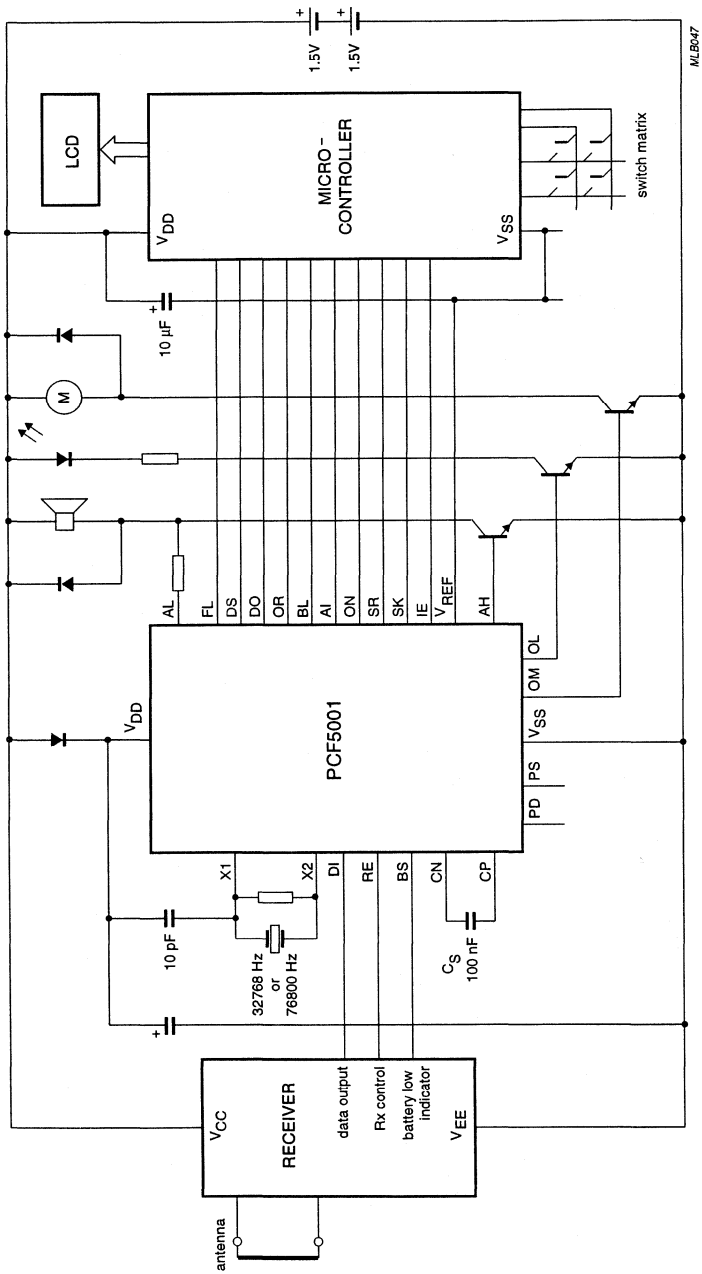


Fig.23 Display-pager application example.

GSM Baseband and Audio Interface (BAI) PCF5073

FEATURES

- Low power device in 0.5 micron CMOS technology for 3.0 V typical power supply
- Compatible with GSM phase 2 and DCS1800 recommendations
- Complete in-phase and quadrature component interface paths between digital signal processor and IF circuitry (e.g. Philips SA1638)
- Complete linear PCM CODEC for audio signal conversion between earphone/microphone and digital signal processor
- Four auxiliary analog inputs for measurement purposes (e.g. battery monitoring)
- Three auxiliary analog outputs for control purposes (e.g. AFC, AGC and power ramping control)
- Separate baseband, audio and control serial interfaces
- JTAG interface for boundary scan test.

APPLICATIONS

The CMOS integrated circuit PCF5073 is dedicated to wireless telephone handsets following the GSM recommendations phases 1 and 2 and DCS1800.

GENERAL DESCRIPTION

The baseband CODEC is a complete interface circuit between the RF part in a mobile communication handset and the digital signal processor. It consists of three parts:

1. The **receive path**, which transforms the quadrature signals from the RF (I/Q) to digital signals.
2. The **transmit path**, which transforms a bitstream to analog quadrature signals for the RF devices.
3. The digital **baseband serial interface**, which exchanges baseband data between the PCF5073 and the digital signal processor. The interface also includes signals to power the transmit path and the receive path up and down.

The voice band CODEC in the PCF5073 is a complete analog front-end circuit. It consists of three parts:

1. The **receive path**, which converts a digital signal to an analog signal for an earpiece, an external loudspeaker or a buzzer.
2. The **transmit path**, which receives the analog external signal from a microphone and converts it into a digital signal.
3. The digital **audio serial interface**, which connects the digital linear PCM signals of the receive and transmit paths to an external digital signal processor. The voice band data is coded in 16-bit linear PCM twos complement words.

The **auxiliary ADC** section consists of four input channels specified for battery management applications.

The **auxiliary DAC** section consists of three digital-to-analog converters for automatic gain control, for automatic frequency control and for power ramping.

The **control serial interface** is used to program a set of control registers, to store the power amplifier ramping characteristics into the dedicated RAM and to transmit auxiliary ADC values to the digital signal processor.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF5073H	LQFP64	plastic low profile quad flat package; 64 leads; body 7 × 7 × 1.4 mm	SOT414-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage (digital)	2.7 (2.5)	3.0	3.6	V
I_{DD}	supply current	–	15	–	mA
$I_{stb(tot)}$	total standby current	–	10	–	µA
f_{clk}	master clock frequency	–	13.0	–	MHz
T_{amb}	operating ambient temperature	–40	+27	+85	°C

BLOCK DIAGRAM

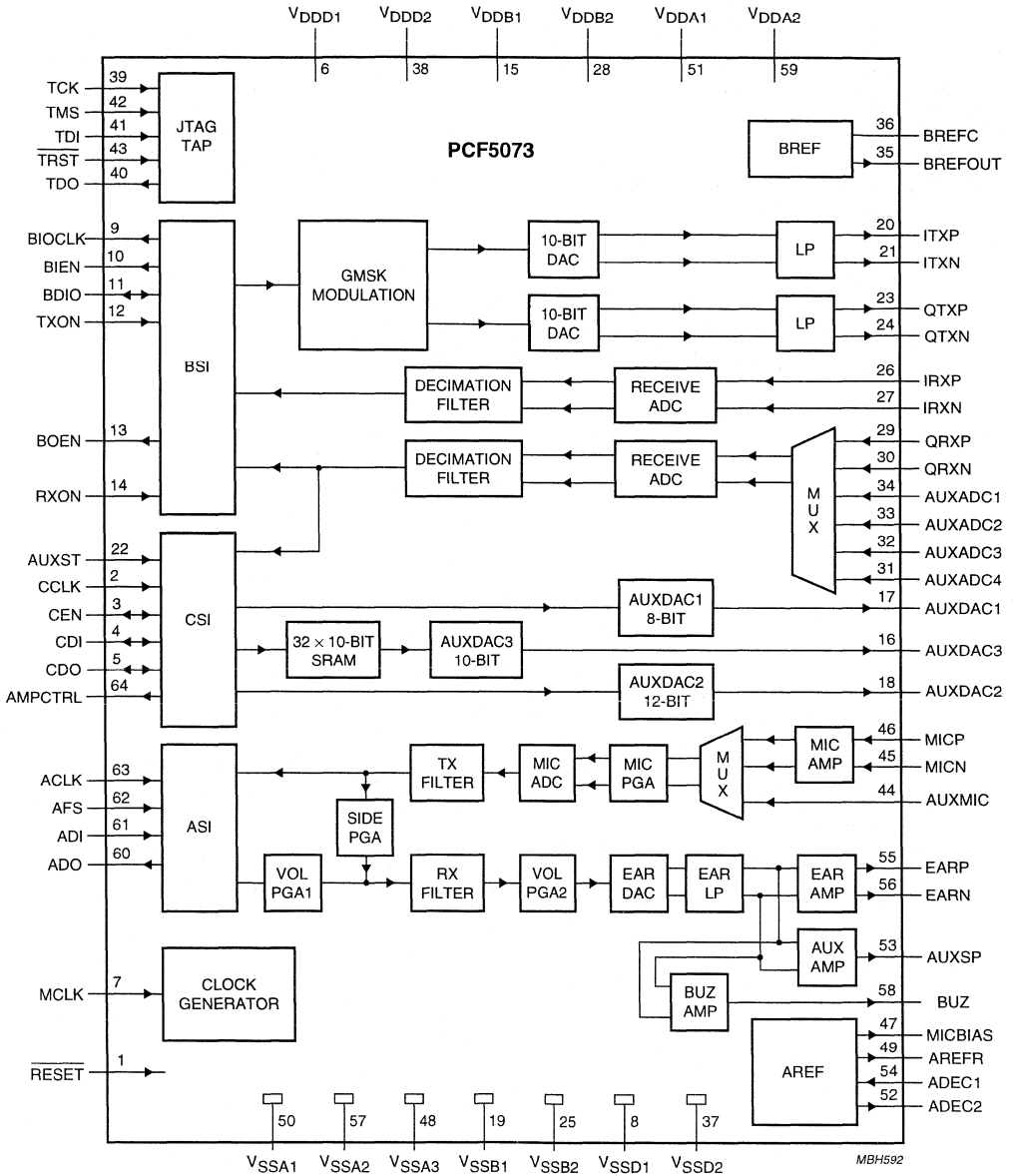


Fig.1 Block diagram.

PINNING

SYMBOL	PIN			DESCRIPTION
	PIN	TYPE	ACTIVE LEVEL/I_{DD}	
$\overline{RESET}$	1	I	LOW	asynchronous reset input
CCLK	2	I	falling	control bus clock input from DSP or UART (f_{max} = 3.25 MHz)
CEN	3	I/O[1]	LOW	control bus data enable from DSP
CDI	4	I/O[1]		control bus data input from DSP (fixed to V_{SS} in UART mode)
CDO	5	I/O	1.5 mA	control bus data output to DSP (data I/O in UART control mode)
V_{DDD1}	6	P		digital power supply 1
MCLK	7	I	rising	low-swing master clock input; f =13 MHz; integrated capacitive coupling
V_{SSD1}	8	G		digital ground 1
BIOCLK	9	O/TS[2]	3 mA	baseband interface data clock (TX: f = 270.833 kHz; RX: f = 13.0 MHz)
BIEN	10	O	LOW/1.5 mA	baseband transmit interface data enable signal
BDIO	11	I/O	1.5 mA	baseband interface data I/O from/to DSP
TXON	12	I	HIGH	baseband transmit path activation signal
BOEN	13	O	LOW/1.5 mA	baseband receive interface data enable signal
RXON	14	I	HIGH	baseband receive path activation signal
V_{DDB1}	15	P		baseband transmit path power supply 1
AUXDAC3	16	O		auxiliary DAC output for power ramping; maximum load 50 pF//2 kΩ
AUXDAC1	17	O		auxiliary DAC output for AGC; maximum load 50 pF//2 kΩ
AUXDAC2	18	O		auxiliary DAC output for AFC; maximum load 50 pF//10 kΩ
V_{SSB1}	19	G		baseband transmit path ground 1
ITXP	20	O		(I) baseband transmit differential positive output to IF circuit
ITXN	21	O		(I) baseband transmit differential negative output to IF circuit
AUXST	22	I	HIGH	status control signal for activation of AUXDAC2 and MCLK input
QTXP	23	O		(Q) baseband transmit differential positive output to IF circuit
QTXN	24	O		(Q) baseband transmit differential negative output to IF circuit
V_{SSB2}	25	G		baseband receive interface ground 2
IRXP	26	I		(I) baseband receive differential positive input from IF circuit
IRXN	27	I		(I) baseband receive differential negative input from IF circuit
V_{DDB2}	28	P		baseband receive interface power supply 2
QRXP	29	I		(Q) baseband receive differential positive input from IF circuit
QRXN	30	I		(Q) baseband receive differential negative input from IF circuit
AUXADC4	31	I		auxiliary ADC input 4
AUXADC3	32	I		auxiliary ADC input 3
AUXADC2	33	I		auxiliary ADC input 2
AUXADC1	34	I		auxiliary ADC input 1 for battery voltage measurement
BREFOUT	35	O	0.2 mA[3]	baseband receive reference voltage noise decoupling pin
BREFC	36	I/O		band gap reference voltage noise decoupling pin
V_{SSD2}	37	G		digital ground 2
V_{DDD2}	38	P		digital power supply 2

SYMBOL	PIN			DESCRIPTION
	PIN	TYPE	ACTIVE LEVEL/I_{DD}	
TCK	39	I		JTAG clock input
TDO	40	O/TS[2]	3 mA	JTAG data output
TDI	41	I		JTAG data input
TMS	42	I		JTAG mode selection input
$\overline{TRST}$	43	I	LOW	JTAG reset input
AUXMIC	44	I		auxiliary microphone single-ended input
MICN	45	I		microphone differential negative input
MICP	46	I		microphone differential positive input
MICBIAS	47	O	0.5 mA	microphone bias voltage
V_{SSA3}	48	G		analog ground 3; shielding substrate contact
AREFR	49	O	12 μA	reference current external resistor to analog ground
V_{SSA1}	50	G		analog ground; audio analog ground 1
V_{DDA1}	51	P		analog power supply; audio analog power supply 1
ADEC2	52	O		audio CODEC buffered DC reference; for noise decoupling
AUXSP	53	O		auxiliary speaker output
ADEC1	54	I		mid-reference non-buffered decoupling connection; $\frac{1}{2}V_{DD}$
EARP	55	O		earphone differential positive output
EARN	56	O		earphone differential negative output
V_{SSA2}	57	G		analog ground, audio analog ground 2
BUZ	58	O		buzzer output
V_{DDA2}	59	P		analog power supply; audio analog power supply 2
ADO	60	O/TS	1.5 mA	audio digital interface PCM data output to DSP
ADI	61	I/O[1]		audio digital interface PCM data input from DSP
AFS	62	I	HIGH	audio digital interface PCM frame synchronisation signal from DSP
ACLK	63	I	rising	audio digital interface PCM clock signal from DSP
AMPCTRL	64	O[4]	1.5 mA	auxiliary speaker external amplifier control signal

Notes

1. Bidirectional for testing only.
2. 3-state (TS) output.
3. Only during start-up time.
4. Active level selectable.

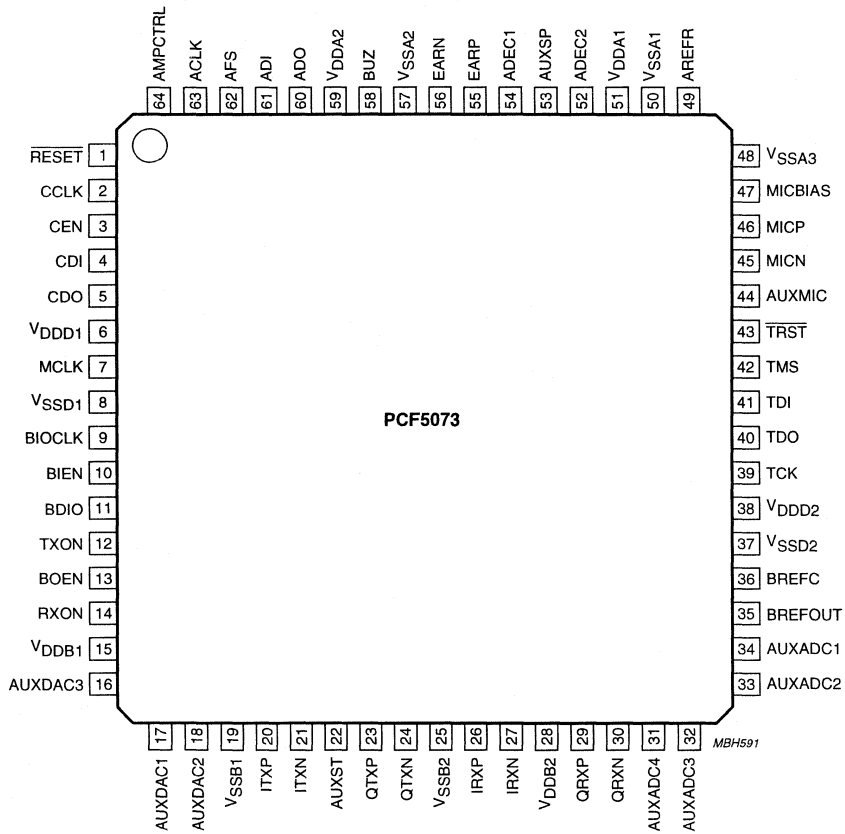


Fig.2 Pin configuration, LQFP64 package.

Power amplifier controller for GSM and PCN systems

PCF5077T

FEATURES

- CMOS low-voltage, low-power
- Can be used in burst mode with power-down
- 3-wire serial bus interface with the bus available in Power-down mode
- On-chip ramp generator for 256 different power levels with two dynamic ranges
- Two programmable regulator start conditions (V_{KICK} and V_{HOME})
- Programmable analog output voltage limitation
- Ramping speed depending on the 13 MHz system frequency clock for Global System for Mobile communications (GSM) and Personal Communications Network (PCN)
- Low swing input buffer for the 13 MHz master clock
- Compatible to a large number of different RF power modules
- Programmable temperature matching
- Dual supply concept for analog and digital part
- No external filter for suppression of clock pulse feed through
- Direct power control with ramping function (control loop can be switched off)
- On-chip Power-on reset for all registers
- Serial bus is compatible to bus systems independent of additional clock pulse after rising edge of strobe signal
- Low operating current consumption
- TTL compatible interface
- Programmable gain factor for sensor signal at OP1
- Two different voltages for 1 LSB of the burst power Digital-to-Analog Converter (DAC) are programmable.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage	note 1	2.7	3.0	6.0	V
V_{DDA1}	analog supply voltage 1	note 1	2.7	3.0	6.0	V
V_{DDA2}	analog supply voltage 2 (for OP4)		2.7	5.0	6.0	V
$I_{DD(oper)(tot)}$	total operating current on the V_{DD} pins	note 2	–	9	18	mA
T_{amb}	operating ambient temperature		−40	–	+85	°C

Notes

1. The voltages V_{DDA1} and V_{DDD} must be equal and V_{DDA2} must be either equal or greater than $V_{DDA1} = V_{DDD}$.
2. $V_{DDA1} = V_{DDD} = 3$ V and $V_{DDA2} = 5$ V. The V_{DD} pins are: V_{DDA1}, V_{DDA2} and V_{DDD}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF5077T	SSOP16	plastic shrink small outline package; 16 leads; body width 4.4 mm	SOT369-1

BLOCK DIAGRAM

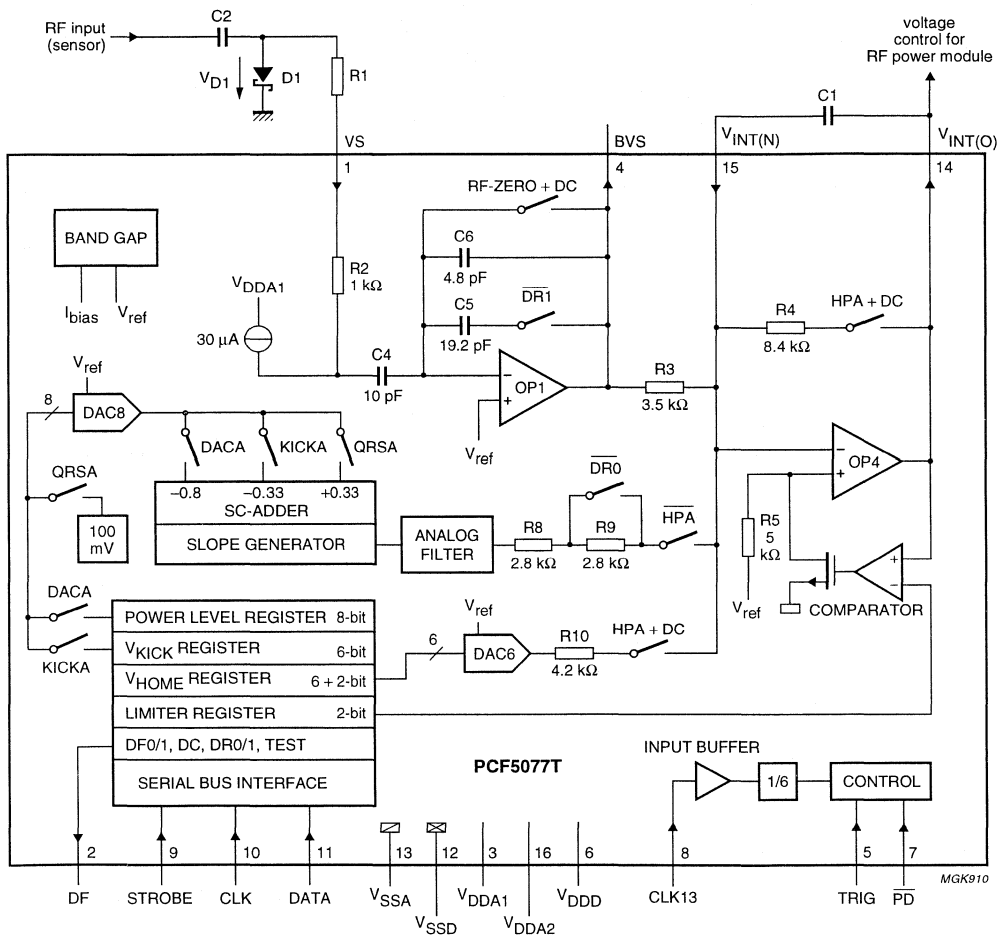


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
VS	1	sensor signal input
DF	2	programmable 3-state output
V_{DDA1}	3	analog supply voltage 1
BVS	4	buffered sensor signal output
TRIG	5	trigger signal input
V_{DDD}	6	digital supply voltage
$\overline{PD}$	7	power-down input (active LOW)
CLK13	8	13 MHz master clock input (low-swing)
STROBE	9	serial bus strobe signal input
CLK	10	serial bus clock signal input
DATA	11	serial bus data signal input
V_{SSD}	12	digital ground
V_{SSA}	13	analog ground
$V_{INT(O)}$	14	integrator output
$V_{INT(N)}$	15	integrator inverting input
V_{DDA2}	16	analog supply voltage 2 (for OP4)

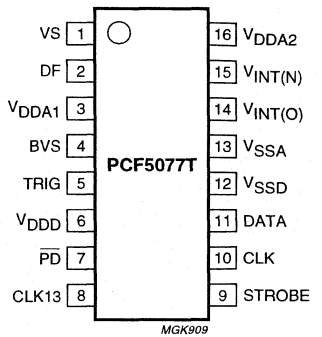


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

General

This CMOS device integrates operational amplifiers, two digital-to-analog converters and a serial bus interface to implement an 'Integrating-Controller' (see Fig.1). It is designed to control both the power level and the up- and down-ramping of GSM/PCN transmit bursts.

The GSM/PCN power-up and power-down ramping curves are generated on-chip, using an internal clock frequency of 2.166 MHz $\left(T_{cy} = \frac{1}{f_{clk}}\right)$, that is generated internally by dividing the external 13 MHz clock signal by six.

Generally, the power amplifier is ramped-up after a rising edge on pin TRIG and ramped-down after a falling edge.

The content of the power level register (bits PL7 to PL0) determines which of the 2×256 possible values the top of the burst will have.

To match the controller to different power modules and sensors several parameters must be adapted.
The following parameters influence the performance of the transmission system:

- The external capacitor C1 in Fig.1 determines the maximum bandwidth of the power control loop, depending on the highest steepness of the control curve of the power module and on the sensor attenuation.
- The maximum output voltage at pin $V_{INT(O)}$ to protect the power module: the limiting value of $V_{INT(O)}$ can be set to 4, 3.3 or 2.55 V, depending on the contents of the limiter register (bits Lim1 and Lim0). This limiting results in a ringing at $V_{INT(O)}$ (typ. 200 mV peak-to-peak value) but it will not be transferred to the antenna because the power module is in saturation. The limiter register bits Lim1 and Lim0 can be used to switch off the limiter option (see Table 5).
- The home position at $V_{INT(O)}$: the integrator output voltage at home position ($\overline{PD}$ = HIGH and TRIG = LOW) is programmed by means of the V_{HOME} register. Bits Vh5 to Vh0 are fed into a 6-bit DAC that generates a part of V_{HOME}.
- The temperature behaviour of the home position: bits DVh1 and DVh0 can be used to compensate temperature dependencies (–2 or –4 mV/K) of the control curves of the power module. This completes the setting of V_{HOME}.
- The KICK voltage: the 6 bits of the V_{KICK} register (Vk5 to Vk0) determine the differential integrator input voltage just after a ramp-up starting signal is detected.

The register information is written via a 3-wire serial bus (see Sections "Serial bus programming" and "Data format").

The output of pin DF is for general purpose which can have three different states (LOW, HIGH and 3-state), depending on the values of bits DF0 and DF1 in the serial register.

Dual supply pins are provided for the analog and digital blocks.

Reset function

After switching on the power supply, the on-chip reset is active for maximal 50 µs when the rising slope of V_{DDD} has reached 1.5 ±0.4 V. During this reset, all controllers are set to the home position and the registers are set to their default values. If the supply voltage drops below the reset threshold a constant reset will appear.

Operating conditions

$\overline{PD}$ = LOW

The serial bus interface is operating, e.g. all registers can be programmed but no effect will be seen on any pin. The contents of the registers are passed to the rest of the circuit only during power-up and with the 13 MHz master clock applied.

If the low-swing input buffer at pin CLK13 is switched off, neither the SC-adder nor the slope generator will function. This means that after the chip is powered-up, the outputs have to settle again to the programmed register values. The settling time is dominated by the slow power-up of the band gap of typically 50 µs.

When the chip is used in the burst mode, it is important to switch on the PCF5077T before the power module or the RF power. Otherwise it is possible that a positive spike at $V_{INT(O)}$ will open the power module.

A safe value is t_{ON} = 200 µs between the switching on of the PCF5077T and the switching on of the power module respectively the next TRIG (see Fig.3).

$\overline{PD}$ = HIGH

The whole chip is active. CLK13 clocks the internal state machine as well as the SC-adder and slope generator. Every change at TRIG is recognized if the master clock is running. The contents of the serial bus registers are processed. If the master clock is switched off during power-up, the state machine is stopped and the output of the SC-adder and slope generator becomes undefined. Nevertheless, by reactivating the master clock, the output of the SC-adder and slope generator will settle to the old values again.

The analog integrating controller

The analog integrating controller consists of two operational amplifiers (OP1 and OP4) and a comparator. OP1 amplifies the sensor signal and OP4 is used to form a differential integrator. The comparator is used to limit the integrator output voltage to the value selected by bits Lim1 and Lim0 in the limiter register.

A (Schottky) diode D1 as external rectifier is connected to pin VS. The SC-adder block generates the voltage for the ramping of the power module.The differential integrator integrates the difference of this voltage and the voltage detected at the diode. The integrator output voltage $V_{INT(O)}$ is used to control the power amplifier module.

Table 1 Definition of some voltages used in Figs 1 and 3

SYMBOL	DESCRIPTION
V_{ref}	reference voltage, typically 1.25 V
V_{D1}	voltage over the sensor diode D1
V_{PL}	voltage determining the power level; it is generated in the Switched Capacitor (SC)-adder block if switch DACA is closed (i.e. if the signal DACA is HIGH)
V_{VS}	voltage at pin VS when RF is rectified by the sensor diode D1
V_{BVS}	amplified voltage from pin VS
V_{KICK}	voltage determining the kick level; it is generated in the SC-adder block if switch KICKA is closed (i.e. if the signal KICKA is HIGH)
V_{HOME}	voltage determining the home position voltage; if HPA signal is active, the output of DAC6 plus temperature compensation is amplified and appears at the output of OP4 (pin $V_{INT(O)}$)
V_{QRS}	low voltage at the output of the SC-adder block which causes a ramp-down with a shortened tail if switch QRSA is closed (i.e. if the signal QRSA is HIGH)
V_{RFIN}	input signal to the power amplifier

Ramp generation (see Fig.3)

The circuit is activated with the $\overline{PD}$ signal going HIGH before time mask AS and deactivated after ramping down, e.g. at time GS to HS. For this usual 'power-down burst mode' application in GSM/PCN mobile stations, the RF input power at the power module must be activated between time AS and BS (when the home position at $V_{INT(O)}$ has already reached its stable value) and deactivated between time GS and HS. This is necessary for many types of power modules to meet the –70 dB margin.

A ramp-up is started by a rising edge of the TRIG signal. The TRIG signal and all other internal signals are delayed by two clock periods ($2T_{cy}$) with respect to the signal at pin TRIG.

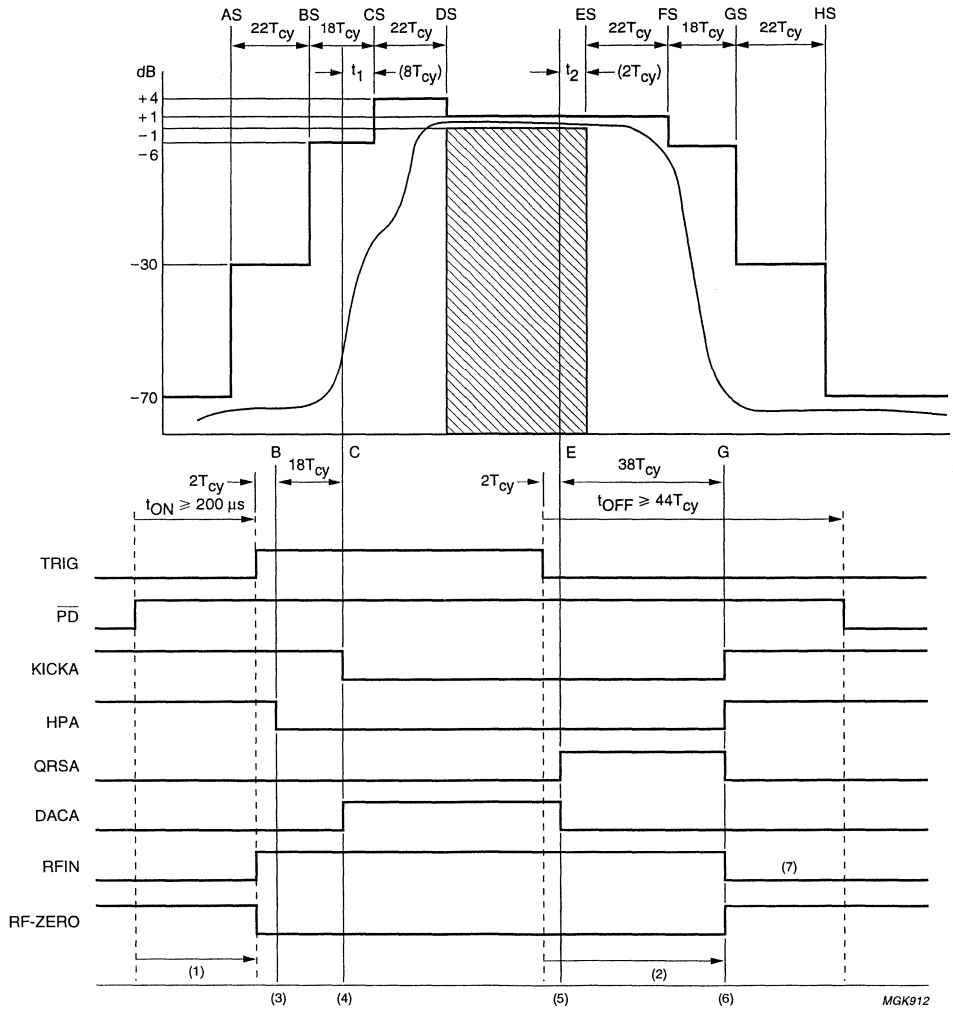
The timing diagram shows a possible relationship between the chip timing (time B to G) relative to the GSM-mask (AS to HS). However, the user is free to choose the rising and falling edge of TRIG independently so that the mask is not violated.

DESCRIPTION OF THE SIGNALS STARTING AT A STABLE HOME POSITION OF $V_{INT(O)}$ AT TIME B – $2T_{cy}$

The integrator output voltage is regulated to the value defined in the V_{HOME} register. The output of the slope generator is connected to the negative input $V_{INT(N)}$ of operational amplifier OP4 (V_{KICK} is defined by bits Vk5 to Vk0 in the V_{KICK} register). Two clock periods after a rising edge on pin TRIG, the integrator start condition circuitry is turned off and OP4 is switched into an integrator configuration (time B). The HPA switches will open (HPA + DC is either HPA switch or DC bit). Switch $\overline{HPA}$ is closed when there is no home position. Due to the negative differential input voltage V_{KICK}, the integrator output will start to rise. After $18T_{cy}$ (time C) the output of DAC8 is connected to the SC-adder and slope generator block. The input of the 8-bit DAC comes from bits PL7 to PL0 in the power level register. The slope generator will generate a smooth curve between the former and the new output value of the SC-adder block. The power amplifier is ramped-up via the integrator in approximately $22T_{cy}$.

This condition is stable as long as TRIG remains HIGH. Two clock periods after a falling edge at TRIG the ramp-down is started (time E). The SC-adder output voltage will change to V_{QRS} (–100 mV), because DACA becomes inactive and QRSA active. This causes a ramp-down with a shortened tail. The slope generator again generates a smooth curve between the new SC-adder output voltage and the old SC-adder output voltage.

The slope generator must have reached its final value at $38T_{cy}$ after the recognized falling edge of TRIG because the HPA signal is activated again and by that turning the integrator into its 'home position' (time G). The integrator output voltage will be regulated once more to the value defined in the V_{HOME} register.



(1) $t_{RFON} = t_{ON} - 12T_{cy}$ to $t_{ON} + 2T_{cy}$.
(2) $t_{RFOFF} = 44T_{cy}$ to $66T_{cy}$.
(3) V_{KICK} (start integrator) applied to integrator.
(4) V_{PL} applied to integrator.
(5) V_{QRS} applied to integrator.
(6) V_{HOME} at output of OP4.
(7) This timing of the RF input power (from the power module) ensures that the −70 dB margin is met, even if the isolation of the power module is bad.

Fig.3 Timing diagram of a typical ramp-up/ramp-down curve.

Serial bus programming

A simple 3-wire unidirectional serial bus is used to program the circuit. The 3 wires are DATA, CLK and STROBE. The data sent to the device is loaded in bursts framed by STROBE. Programming clock edges and their appropriate data bits are ignored until STROBE goes active LOW.

The last four address bits are decoded on the active STROBE edge. This produces an internal load pulse to store the data in one of the addressed registers. To avoid erroneous circuit operation, the STROBE pulse is not allowed during internal data reads by the rest of the circuit. This condition is guaranteed by respecting a minimum STROBE pulse width after data transfer.

Only the last 16 bits serially clocked into the device are retained within the programming register. Additional leading bits are ignored, and no check is made on the number of clock pulses. The fully static CMOS design uses virtually no current when the bus is inactive. The bus is also programmable during power-down.

Data format

Data is entered with the most significant bit (MSB) first. The leading 10 bits p15 to p6 are the data field, the following bits p5 and p4 form the subaddress, while the last 4 bits p3 to p0 are the device address field. The PCF5077T uses only one of the available addresses. The format is given in Table 2.

The correspondence between data and address fields is given in Table 3 and the description in Table 4.

All three registers in Table 3 are set to 00H during reset.

Table 2 Programming register format

DATA BITS				SUBADDRESS		DEVICE ADDRESS			
MSB			LSB						
p15	p14 to p8	p7	p6	p5	p4	p3	p2	p1	p0
data9	data8 to data2	data1	data0	Sadd1	Sadd0	add3	add2	add1	add0

Table 3 Register bit allocation

DATA FIELD (D9 TO D0)										SUBADDRESS		DEVICE ADDRESS			
MSB									LSB						
p15	p14	p13	p12	p11	p10	p9	p8	p7	p6	p5	p4	p3	p2	p1	p0
Vk5	Vk4	Vk3	Vk2	Vk1	Vk0	Lim1	Lim0	DC	Test	0	0	1	0	1	0
Vh5	Vh4	Vh3	Vh2	Vh1	Vh0	DVh1	DVh0	DR1	DR0	0	1	1	0	1	0
PL7	PL6	PL5	PL4	PL3	PL2	PL1	PL0	DF1	DF0	1	1	1	0	1	0

Table 4 Description of bits used in Table 3

BITS	DESCRIPTION
Vk5 to Vk0	6 bits to control the kick voltage in 64 steps
Vh5 to Vh0	6 bits to control the home position voltage in 64 steps
PL7 to PL0	8 bits to control the power level in 256 steps
Lim1 and Lim0	2 bits to control the limiter voltage (see Table 5)
DC	direct control with ramping function (control loop is switched off when DC = 1)
Test	test mode (Test = 1); **must always be set to logic 0 in application**
DVh1 and DVh0	2 bits to set the temperature coefficient of V_{HOME} (see Table 6)
DR1	gain factor of OP1
DR0	gain factor for slope generator output
DF1	enable of the 3-state output on pin DF (for DF1 = 0, pin DF is in 3-state mode)
DF0	data output on pin DF

Table 5 Limiter voltage

Lim1	Lim0	LIMITER VOLTAGE (V)	TOLERANCE AT T_{amb} = 27 °C (mV)	TOLERANCE AT T_{amb} = 85 °C (mV)
0	0	limiter off	–	–
0	1	4.00	±250	±350
1	0	3.30	±250	±350
1	1	2.55	±250	±350

Table 6 Programmable temperature coefficient of V_{HOME}

DVh1	DVh0	V_{HOME}[1]
0	0	Vh ±0.4 mV/K
0	1	Vh – 2 mV/K ±20%
1	0	Vh – 4 mV/K ±20%
1	1	V_{SS}

Note

1. Vh = voltage programmed in V_{HOME} register bits Vh5 to Vh0 and generated by DAC6.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDA1}	analog supply voltage 1	–0.5	+6.0[1]	V
V_{DDA2}	analog supply voltage 2	–0.5	+6.0[1]	V
V_{DDD}	digital supply voltage	–0.5	+6.0[1]	V
V_I	DC input voltage on all pins (except pin VS)	–0.5	V_{DD} + 0.5	V
$V_{I(VS)}$	DC input voltage on pin VS	–3.0	V_{DD} + 0.5	V
$I_{I(n)}$	DC input current on any signal pin	–10	+10	mA
P_{tot}	total power dissipation	–	83	mW
T_{stg}	storage temperature	–65	+150	°C
T_{amb}	operating ambient temperature	–40	+85	°C

Note

1. Pulses of 7 V are allowed for less than 100 ms.

OPERATING CHARACTERISTICS

V_{DDA1}, V_{DDA2} and $V_{DDD} = V_{DD}$ = 2.7 to 6.0 V; $V_{DDD} = V_{DDA1} \leq V_{DDA2}$; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operational amplifier (OP1)						
V_{DDA1}	analog supply voltage 1		2.7	3.0	6.0	V
GB	gain bandwidth product	V_{DDA1} = 3.0 V	2.0	–	–	MHz
G_{min}	minimum gain	DR1 = 0	−8.1	−7.6	−7.1	dB
G_{max}	maximum gain	DR1 = 1	5.9	6.4	6.9	dB
V_{offset}	offset voltage	no load at output	−20	0	+20	mV
Operational amplifier (OP4)						
V_{DDA2}	analog supply voltage 2		2.7	5.0	6(1)	V
GB	gain bandwidth product	C_L = 120 pF; V_{DDA2} = 5 V; note 2	4	–	–	MHz
PSRR	power supply rejection ratio	V_{DDA2} = 5 V, at 217 Hz	50(3)	55	–	dB
SR_{pos}	positive slew rate	V_{DDA2} = 5 V; note 4	3.5	15	–	V/µs
SR_{neg}	negative slew rate	V_{DDA2} = 5 V; note 4	3.5	6	–	V/µs
V_{offset}	voltage offset	no load at output	−20	0	+20	mV
$V_{o(min)}$	minimum output voltage		–	–	0.3	V
$V_{o(max)}$	maximum output voltage		0.85V_{DDA2}	–	–	V
I_o	output current	note 5	4.5	–	–	mA
Programmability and accuracy of V_{PL} (DAC8) at $V_{INT(O)}$						
INL	integral non-linearity		–	±1.5	±10	LSB
DNL	differential non-linearity		–	±0.2	±1	LSB
$V_{o(min)}$	minimum output voltage	DC = 1; DR0 = 1; note 6	−30	–	+60	mV
$V_{o(max)}$	maximum output voltage	DC = 1; DR0 = 0; note 6	2.72	–	3.15	V
STS	step size	DC = 1; DR0 = 1	–	6	–	mV
		DC = 1; DR0 = 0	–	11.7	–	mV
Programmability and accuracy of V_{KICK} (DAC8) at $V_{INT(O)}$						
$V_{o(min)}$	minimum output voltage	DC = 1; DR0 = 1; note 6	−50	–	+50	mV
$V_{o(max)}$	maximum output voltage	DC = 1; DR0 = 0; note 6	270	–	400	mV
STS	step size	DC = 1; DR0 = 1	–	2.6	–	mV
		DC = 1; DR0 = 0	–	5.0	–	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Programmability and accuracy of V_{HOME} (DAC6) at $V_{INT(O)}$						
INL	integral non-linearity	note 7	–	±1.0	±3	LSB
DNL	differential non-linearity	note 7	–	±0.2	±1	LSB
$V_{o(min)}$	minimum output voltage	DVh1 = 0; DVh0 = 0	50	–	170	mV
$V_{o(max)}$	maximum output voltage	DVh1 = 0; DVh0 = 0	1.95	–	2.25	V
STS	step size		–	33	–	mV

Notes

1. Pulses of 7 V are allowed for less than 100 ms.
2. Minimum specified frequency at T_{amb} = 27 °C. For T_{amb} = 85 °C a typical value of 4 MHz is specified.
3. Not tested. Guaranteed by design.
4. Slew rates are measured between 10% and 90% of output voltage with a load of approximately 40 pF to ground.
5. Measured with R_L = 1.2 kΩ, C_L = 80 pF and V_{DDA2} = 5 V. The voltage drop at the output is less than 20 mV.
6. Referred to V_{HOME}; nominal operating condition, direct control (DC = 1), V_{HOME} programmed to 40.
7. The parameter is measured starting from code 4, due to a saturation effect for the first four codes.

DC CHARACTERISTICS

V_{DDA1}, V_{DDA2} and V_{DDD} = V_{DD} = 2.7 to 6.0 V; V_{DDD} = V_{DDA1} ≤ V_{DDA2}; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage		2.7	3.0	6.0	V
V_{DDA1}	analog supply voltage 1		2.7	3.0	6.0	V
V_{DDA2}	analog supply voltage 2		2.7	5.0	6.0	V
$I_{DD(oper)(tot)}$	total operating current on the V_{DD} pins	f_{CLK13} = 13 MHz; see Fig.5	–	9	18	mA
$I_{DD(idle)(tot)}$	total idle current on the V_{DD} pins	$\overline{PD}$ = LOW	–	4	20	µA
Logic inputs (pins TRIG, STROBE, CLK and DATA)						
I_{LIL}	LOW-level input leakage current	V_{IL} = 0 V	−5	–	+5	µA
I_{LIH}	HIGH-level input leakage current	V_{IH} = 6 V	−5	–	+5	µA
C_i	input capacitance		–	10	–	pF
V_{IL}	LOW-level input voltage		0	–	$0.2V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.5V_{DD}$	–	V_{DD}	V
3-state output (pin DF)						
V_{OL}	LOW-state output voltage	I_{OL} = I_{OH} = 3 mA	–	–	0.4	V
V_{OH}	HIGH-state output voltage	I_{OL} = I_{OH} = 3 mA	$0.7V_{DD}$	–	–	V
I_{LO}	3-state output leakage current	V_{DF} = 0 to V_{DD}	−5	–	+5	µA
Low-swing master clock input (pin CLK13)						
I_{LI}	input leakage current		−5	–	+5	µA
C_i	input capacitance		–	10	–	pF
$\|Z_i\|$	input impedance	f_{CLK13} = 13 MHz; note 1	–	5	–	kΩ
$V_{i(p-p)}$	input voltage (peak-to-peak value)	note 2	0.35	–	V_{DD}	V
Sensor input voltage (pin VS)						
$V_{i(VS)}$	input voltage at pin VS		−3.0	–	V_{DD}	V
Band gap						
I_{bias}	bias current (source for D1)	V_{VS} = 0 V; T_{amb} = 25 °C; TC = −0.08 µA/K	21	28	35	µA
V_{ref}	reference voltage	T_{amb} = 25 °C	1.18	1.25	1.32	V
TC	temperature coefficient for V_{ref}		–	±170	–	ppm/K
t_{pu}	power-up time for V_{ref}	note 3	–	5	50	µs
Power-on reset, threshold voltage V_{th}; see Fig.4						
V_{th}	threshold voltage	T_{amb} = 25 °C; TC = −4 mV/K	1.2	1.5	1.8	V
t_{rst}	reset time		–	–	50	µs

Notes

1. An AC coupling with 33 pF is recommended.
2. Tested at nominal working condition (V_{DDD} = V_{DDA1} = 3 V; V_{DDA2} = 5 V). AC coupling = 33 pF.
3. The necessary start-up time t_{ON} = 200 µs (see Fig.3) between $\overline{PD}$ and TRIG is more than t_{pu}.

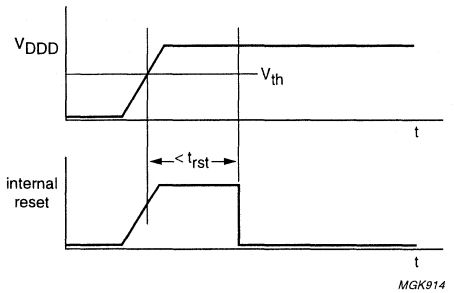
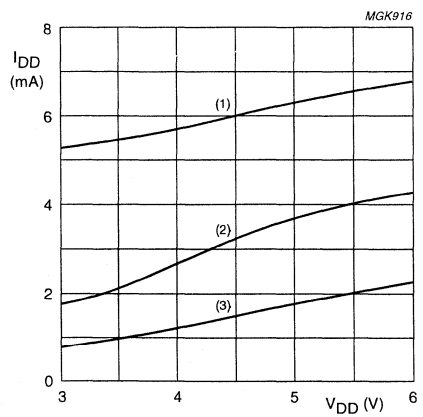


Fig.4 Timing diagram for on-chip reset function.



(1) I_{DDA1}. (2) I_{DDA2}. (3) I_{DDD}.

Fig.5 Operating current I_{DD} as a function of V_{DD}.

TIMING CHARACTERISTICS

V_{DDA1}, V_{DDA2} and V_{DDD} = 2.7 to 6.0 V; $V_{DDD} = V_{DDA1} \leq V_{DDA2}$; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	UNIT
Controller timing; see Fig.3				
$t_{d(TRIG-B)}$	delay from positive TRIG edge to time B = $^{13}/_{6}T_{cy}$	–	1.0	µs
$t_{d(B-C)}$	delay from time B to time C = $18T_{cy}$	–	8.31	µs
$t_{d(TRIG-E)}$	delay from negative TRIG edge to time E = $^{13}/_{6}T_{cy}$	–	1.0	µs
$t_{d(E-G)}$	delay from time E to time G = $38T_{cy}$	–	17.54	µs
Serial bus timing; see Fig.6				
SERIAL PROGRAMMING CLOCK (PIN CLK)				
t_r	rise time	–	10	ns
t_f	fall time	–	10	ns
T_{cy}	clock period	100	–	ns
ENABLE PROGRAMMING (PIN STROBE)				
t_{start}	strobe start time to first clock edge	0	–	ns
t_{end}	strobe end time after last clock edge	40	–	ns
REGISTER SERIAL INPUT DATA (PIN DATA)				
t_{su}	input data to CLK set-up time	20	–	ns
t_h	input data to CLK hold time	20	–	ns

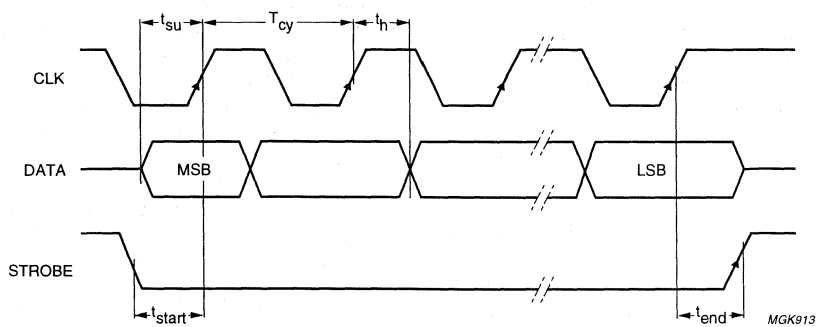


Fig.6 Serial bus timing diagram.

APPLICATION INFORMATION

Direct power control with ramping function (DC = 1)

The circuit offers a useful feature to control power levels close to the saturation region of the external power module.

This flexibility consists in the direct control on the power level by setting bit DC to logic 1.

In this condition, the external control loop is switched off by disabling the gain path from OP1. The ramping shape of the signal to be transmitted as well as its final level are driven only by the internally generated control signal from the slope generator. In this way transient effects to recover active components from deep saturation are avoided. The relative error on the absolute value of output power is quite limited, as a power amplifier is less sensitive to temperature variation in its saturated region. However, this way of operating may increase the phase error.

Increased dynamic range

The PCF5077T is able to control a dynamic range of 30 dBm by switching the gain factor of the sensor amplifier and the resolution of DAC8. This range corresponds to a maximum peak-to-peak voltage of 3 V measured at the sensor diode. Figure 7 shows the voltage at the sensor diode (V_S) versus the output power (P) of the Power Amplifier (PA) with a directional coupler of 20 dB attenuation. The maximum voltage of 3 V is reached when the output power is 35 dBm.

The sensor voltage for power level lower than 13 dBm, as necessary for GSM Phase 2 and DCS1800, is lower than 200 mV. An 8-bit DAC would not be sufficient to cover the complete dynamic range. Therefore bits DR0 and DR1 are used to switch the power range that can be controlled with the controller (see Table 7).

Reduced voltage steps of power level DAC8 (DR0 = 1)

The DR0 bit is used to switch resistor R9 (switch $\overline{DR0}$ is closed) at the integrator input (OP4). The ratio of the DAC8 range to the sensor signal voltage is therefore halved and the power corresponding to one LSB of DAC8 is reduced by 3 dB. With this setting the power module can be controlled more accurately for low output power levels.

Gain factor of OP1 (DR1)

Bit DR1 switches (switch $\overline{DR1}$ is closed) the ratio of the capacitances at OP1. The gain factor for the sensor amplifier is five times higher when DR1 is in high state.

When DR1 = 1, the control loop regulates the output power of the PA to a lower power level. A dynamic range of about 10 dBm can be switched by this manner.

$V_s : V_{peak}$ is the ratio of sensor signal to slope generator output voltage effective at the integrator output (OP4).

Table 7 Gain factors

DR1	DR0	$V_S : V_{peak}$
0	0	1 : 1
0	1	2 : 1
1	0	5 : 1
1	1	10 : 1

Additional application information

Evaluation kits with software and demonstration board are available for the PCF5077T together with Philips power modules BGY206, CGY2010, CGY2020 and CGY2021 for GSM and PCN, which will provide help for applications.

Very little bus traffic is required for the PCF5077T because the ramping curves are generated on-chip. V_{KICK} and V_{HOME} define the start conditions for up-ramping. V_{PL} determines the power levels. TRIG is the trigger for up and down-ramping.

The non-linear behaviour of the control curves of the power modules have a big influence on the loop. Start conditions in the flat area of the control curve are critical and need some attention. Initially $V_{INT(O)}$ will be at the home position. The HPA switches release the regulator. The integrator is moved into the active part of the control curve. This is achieved by integrating V_{KICK}. When $V_{INT(O)}$ has reached the active region of the control curve the loop is closed and the circuit is able to follow the ramping function generated by a voltage step to the slope generator. The step height V_{PL} determines the power of the transmit burst. Down-ramping is started at the slope generator input by a voltage step from V_{PL} back to V_{QRS}. The loop follows the leading function for down-ramping until the RF sensor measures zero. The reason for V_{QRS} is to shorten the tail of the slope.

Figures 8 and 9 show the results of measurements on the up and down-ramping where REF is the reference level of the power in the time slot, ATTEN is the attenuation of the input instrument for not to destroy the instrument itself, RES BW is the resolution bandwidth, VBW is the video bandwidth, CENTER is the carrier frequency for the burst that has been measured and SWP is the sweep time used for the measurement.

ADJUSTMENT OF THE HOME POSITION

The 6-bit DAC for V_{HOME} determines the start point of the burst in the time template. Curve 2 in Fig.8 shows what happens when V_{HOME} is too low. The burst starts too late and the up-ramping of the power is too steep. The steep up-ramping results in a wide transient spectra. The RF input power shall be switched off when the TRIG signal is LOW to keep the −70 dB margin before the burst.

The home position has to be adjusted for each mobile phone because of DAC tolerances and individual PA characteristics.

The temperature coefficients for V_{HOME} (−2 and −4 mV/K) are used to compensate the temperature shift of the PA control curve. Therefore the PA and the controller shall be placed nearby on the printed-circuit board. Additionally it has to be considered that the temperature of the PA and PCF5077T are different because the PA heats up itself. Software may help to adapt V_{HOME} to different temperatures.

ADJUSTMENT OF V_{KICK}

After the falling edge of HPA the integrator starts to increase the control voltage up to the position of V_{KICK} where the PA should have reached its active region. Increasing V_{KICK} at high power level makes the up ramping of the burst smoother and improves the transient spectra.

V_{KICK} must be reduced for low level of V_{PL} to avoid that both voltages become equal. Setting V_{KICK} to minimum value for the lowest power level can be sufficient.

At low power level the burst will start later because of the bend sensor curve (see Fig.7). The trigger pulse has to be started up to 3 bits earlier for the lowest power level to avoid that the power is ramped up too late for the first data bits of the burst.

LIMIT FOR CORRECT DOWN-RAMPING

The maximum RF power that the power module in saturation is able to deliver depends on RF input power, transmit frequency, supply voltage, temperature and load impedance. The maximum V_{PL} must be matched to the worst case output power and then reduced by 1 dB when the PCF5077T is used in closed loop mode.

Curve 2 in Fig.9 shows what happens when the PA is driven into saturation. The down-ramping of the power is getting too steep and therefore the transient spectra will be too wide. The 1 dB margin is necessary because of the flat PA control curve at high power level. The loop needs more time to reduce the power during the down-ramping and the control voltage increases. The high control voltage forces the power quickly down when the steep region of the control curve is achieved. The steep down-ramping results in a wide transient spectra.

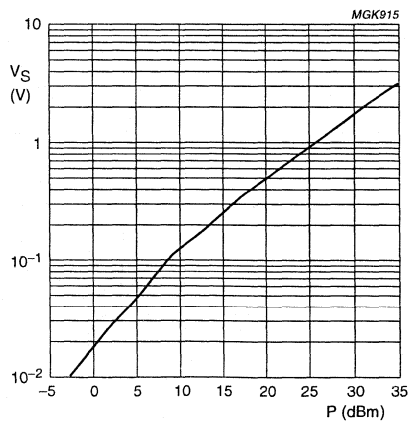
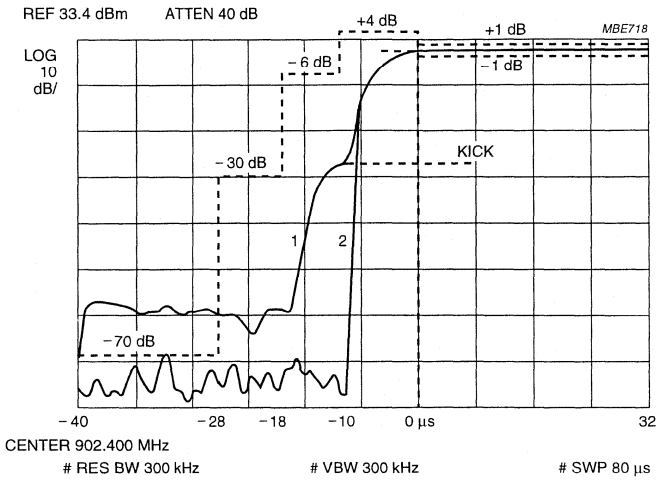
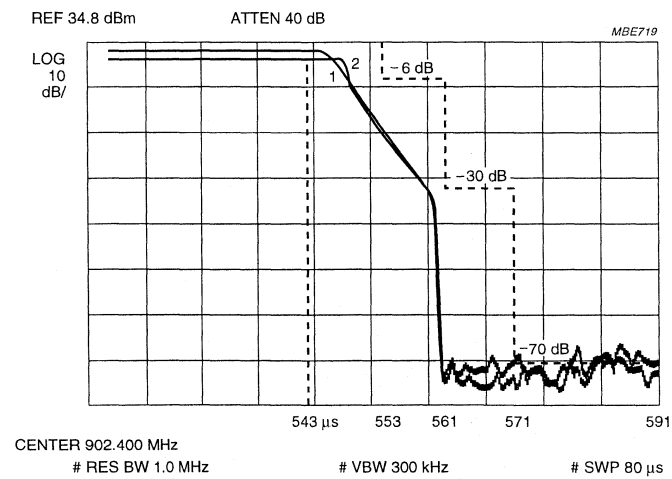


Fig.7 Sensor voltage as a function of output power (diode BAT62).



(1) Highest usable value.
(2) Lowest usable value.

Fig.8 Power as a function of time; rising edge (behaviour at different worst case home positions of $V_{INT(O)}$).



(1) Correct behaviour.
(2) Unusable behaviour with wrong V_{PL} value.

Fig.9 Power as a function of time; falling edge.

Application in mobile stations

Using a directional coupler with 16.5 dB attenuation produces a sensor signal between 100 mV and 3 V below the diode forward voltage at pin VS for the PA output power range of 8 to 36 dBm.

The sensor voltage of 3 V at pin VS corresponds to the maximum DAC output voltage. The power range that can be controlled is therefore not limited by the sensor voltage input VS and higher power levels can be controlled with the control loop switched on.

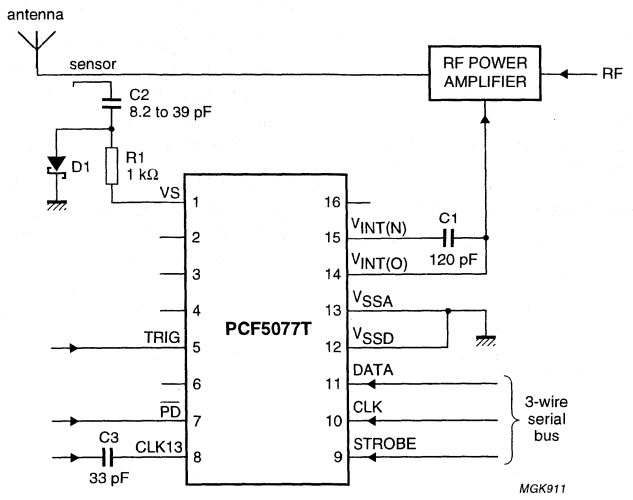


Fig.10 Application diagram for mobile stations.

GSM signal processing IC PCF5083

FEATURES

- Fabricated in a 0.5 μm/0.4 μm CMOS process with 3-layer metal
- LQFP128 package
- 3.3 V operation
- Low power
- Embedded DSP core for all GSM specific signal processing tasks:
  - 16-bit fixed point DSP
  - 19.5 MHz or external clock operation
  - Flexible power-down modes
  - 5 kbytes on-chip program or data RAM
  - 2 kbytes on-chip data ROM
  - 16 kbytes on-chip program ROM
  - Fully pre-programmed modules for GSM baseband tasks including all data channels
  - Dedicated GSM signal processor with application specific hardware for: equalisation, channel encoding/decoding for all traffic and control channels and encryption/decryption (A5/1 and A5/2 algorithms)
  - Tone and side-tone generation
- GSM Hardware Timer and Interface core:
  - Power saving Sleep mode for GSM mobiles
  - Programmable TDMA timing and power-down signals with 0.25 bit resolution
  - Three wire serial control bus for fast programming of RF ICs and synthesizers
  - IOM®-2 interface for external accessories, host software download and support of the Digital Audio Interface (DAI)
  - RS232 interface for the man machine interface controller
  - Man machine interface power-down control
  - Power supply control logic with Watchdog Timer
  - Real time clock and calendar running on 32.768 kHz
  - 6-bit general purpose I/O port
- Reduced swing 13 MHz main clock input
- On-chip PLL to derive the DSP and microcontroller clock
- 8-bit, 68000 compatible host interface with three interrupt lines
- Boundary scan interface in accordance with *"IEEE Standard 1149.1-1990"*.

GENERAL DESCRIPTION

The PCF5083 GSM Signal Processing IC is a dedicated VLSI circuit; fabricated in a 0.5 μm/0.4 μm CMOS process. It has been designed for baseband signal processing tasks for the Pan European Global System for Mobile telecommunication (GSM). The PCF5083 is part of the second generation Philips Semiconductors GSM chip set.

The PCF5083 consists of an embedded 16-bit DSP core for all GSM specific signal processing tasks and a Timer and Interface core which contains many peripheral functions to simplify the system design.

APPLICATIONS

The PCF5083 is suitable for use in GSM mobile stations or hand-helds.

ORDERING INFORMATION

TYPE NUMBER[1]	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF5083H/F2	LQFP128	plastic low profile quad flat package; 128 leads; body 14 × 14 × 1.4 mm	SOT420-1
PCF5083H/001/F2			
PCF5083H/5V2/F3			
PCF5083H/6V2/F4			

Note

1. Version references in the data sheet PCF5083H/F2: PCF5083-2B; PCF5083H/001/F2: PCF5083-2C; PCF5083H/5V2/F3: PCF5083-3A and PCF5083H/6V2/F4: PCF5083-4C.

BLOCK DIAGRAM

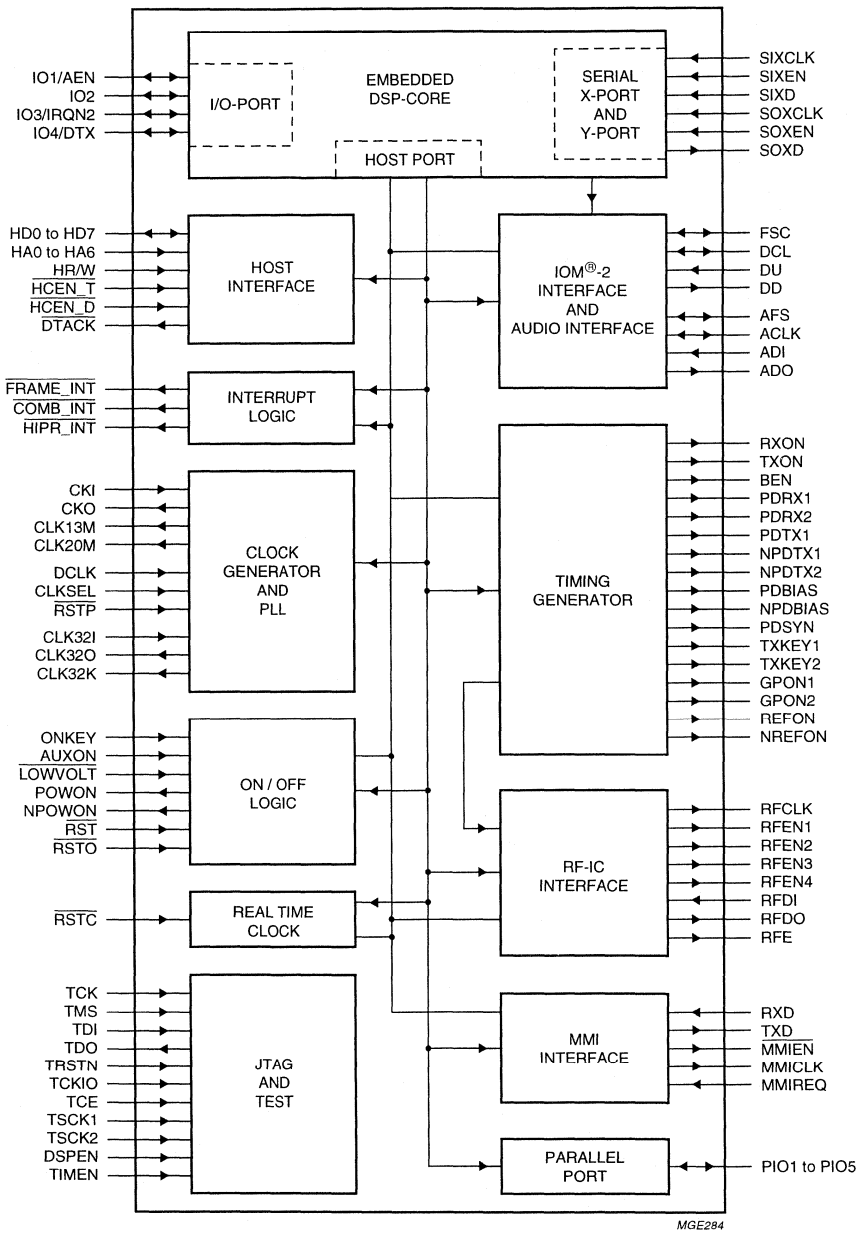


Fig.1 Block diagram.

PINNING INFORMATION

Pinning

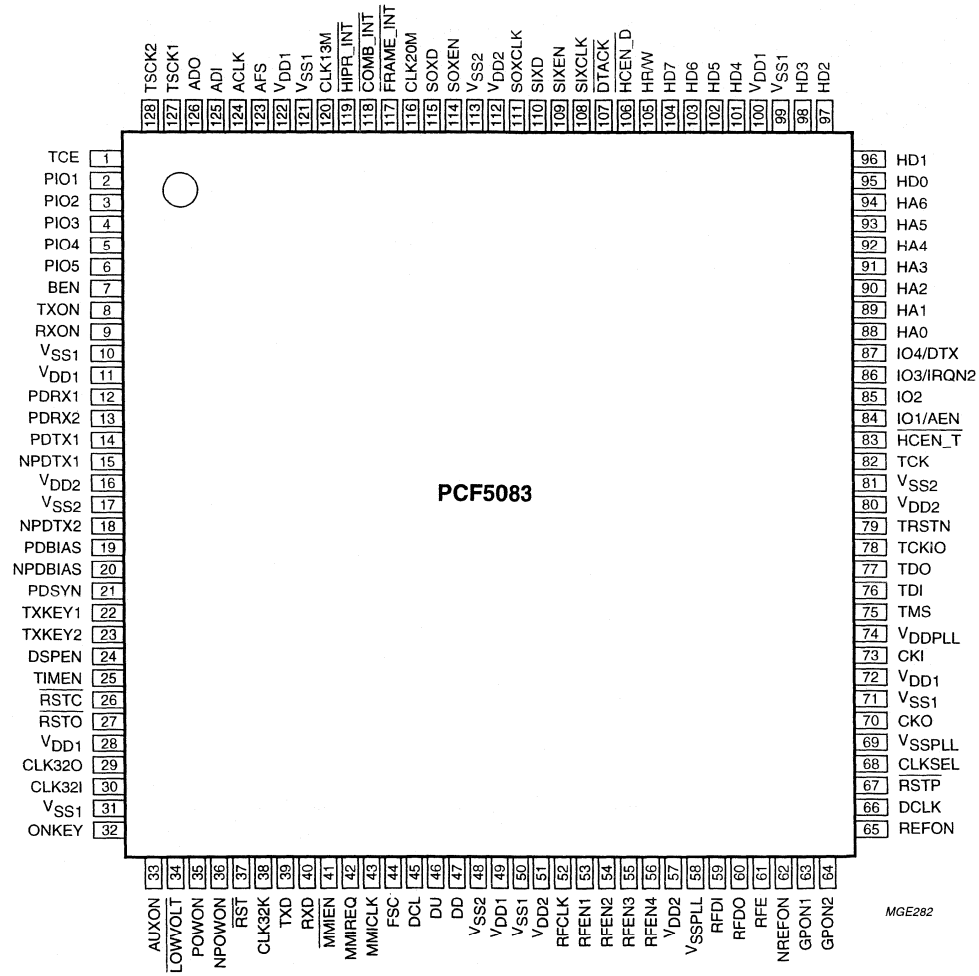


Fig.2 Pin configuration for PCF5083-2B and PCF5083-2C.

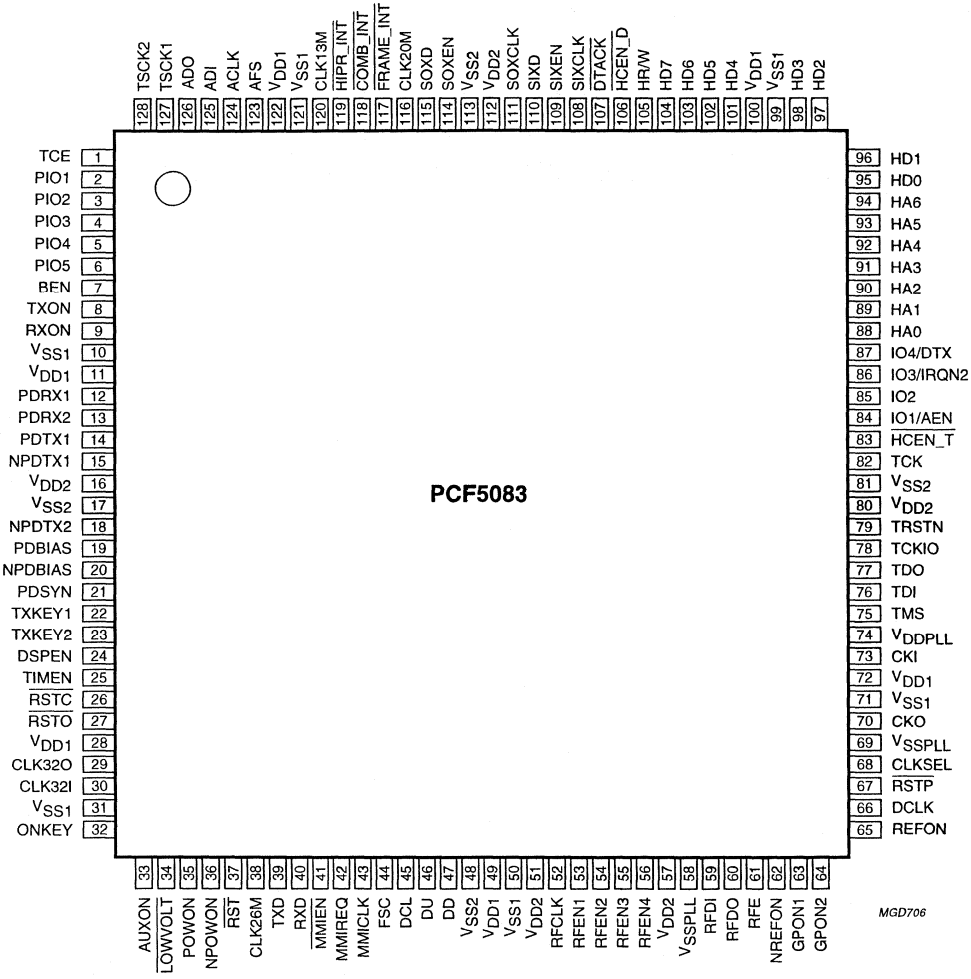


Fig.3 Pin configuration for PCF5083-3A.

Pinning description

SYMBOL	PIN	I/O	DESCRIPTION
TCE	1	I	Test Clock Enable (active HIGH); tied to V_{SS} during normal operation.
PIO1 to PIO5	2 to 6	I/O	General purpose parallel port (3-state output).
BEN	7	O	Baseband Port Enable (active HIGH, 3-state).
TXON	8	O	Modulator window enable (active HIGH, 3-state).
RXON	9	O	Receiver window enable (active HIGH, 3-state).
V_{SS1}	10	–	I/O ground.
V_{DD1}	11	–	I/O power supply.
PDRX1	12	O	Receiver Power-down 1 (active HIGH, 3-state).
PDRX2	13	O	Receiver Power-down 2 (active HIGH, 3-state).
PDTX1	14	O	Transmitter Power-down 1 (active HIGH, 3-state).
NPDTX1	15	O	Inverted output of PDTX1 (active LOW, 3-state).
V_{DD2}	16	–	Core power supply.
V_{SS2}	17	–	Core ground.
NPDTX2	18	O	Transmitter Power-down 2 (active LOW, 3-state, open-drain).
PDBIAS	19	O	Transmitter power supply Power-down (active HIGH, 3-state).
NPDBIAS	20	O	Inverted output of PDBIAS (active LOW, 3-state).
PDSYN	21	O	Synthesizer Power-down (active HIGH, 3-state).
TXKEY1	22	O	Power ramping control (active HIGH, 3-state).
TXKEY2	23	O	Power module control (active HIGH, 3-state).
DSPEN	24	I	DSP Test Mode Enable (active HIGH). PCF5083-2B includes an internal pull-down resistor. PCF5083-2C does not include an internal pull-down resistor.
TIMEN	25	I	Timer Test Mode Enable (active HIGH). PCF5083-2B includes an internal pull-down resistor. PCF5083-2C does not include an internal pull-down resistor.
$\overline{RSTC}$	26	I	Asynchronous Reset - real time clock (active LOW, CMOS level Schmitt trigger input).
$\overline{RSTO}$	27	I	Asynchronous Reset - ON/OFF logic (active LOW, CMOS level Schmitt trigger input).
V_{DD1}	28	–	I/O power supply.
CLK32O	29	O	32.768 kHz crystal oscillator output.
CLK32I	30	I	32.768 kHz crystal oscillator input.
V_{SS1}	31	–	I/O ground.
ONKEY	32	I	ON/OFF Key input (active HIGH, CMOS level Schmitt trigger input with internal pull-down resistor).

SYMBOL	PIN	I/O	DESCRIPTION
AUXON	33	I	Auxiliary Switch-on input (active HIGH, CMOS level Schmitt trigger input).
$\overline{\text{LOWVOLT}}$	34	I	Low battery indication (active LOW, CMOS level Schmitt trigger input).
POWON	35	O	Power Regulator On (active HIGH).
NPOWON	36	O	Power Regulator On (active LOW).
$\overline{\text{RST}}$	37	I	Asynchronous Reset for timer section (active LOW, CMOS level Schmitt trigger input).
CLK32K	38	O	The 32.768 kHz CMOS level output for PCF5083-2B and PCF5083-2C.
CLK26M			The 26 MHz CMOS level output for PCF5083-3A.
TXD	39	O	RS232 transmit data output (open-drain output).
RXD	40	I	RS232 receive data input.
$\overline{\text{MMIEN}}$	41	O	RS232 input buffer full indication (active LOW, open-drain output).
MMIREQ	42	I	MMI clock request (active HIGH, CMOS level Schmitt trigger input).
MMICLK	43	O	MMI clock 13 MHz.
FSC	44	I/O	IOM®-2 frame pulse (3-state).
DCL	45	I/O	IOM®-2 clock (3-state).
DU	46	I	IOM®-2 data input (CMOS level Schmitt trigger input).
DD	47	O	IOM®-2 data output (open-drain output).
V_{SS2}	48	–	Core ground.
V_{DD1}	49	–	I/O power supply.
V_{SS1}	50	–	I/O ground.
V_{DD2}	51	–	Core power supply.
RFCLK	52	O	RF–IC Interface shift clock (3-state).
RFEN1	53	O	RF–IC Interface Enable 1(active LOW, 3-state, open-drain).
RFEN2	54	O	RF–IC Interface Enable 2 (active LOW, 3-state, open-drain).
RFEN3	55	O	RF–IC Interface Enable 3 (active LOW, 3-state, open-drain).
RFEN4	56	O	RF–IC Interface Enable 4 (active LOW, 3-state, open-drain).
V_{DD2}	57	–	Core power supply.
V_{SSPLL}	58	–	PLL ground.
RFDI	59	I	RF–IC Interface Data In.
RFDO	60	O	RF–IC Interface Data Out (3-state).
RFE	61	O	RF–IC Interface Enable (active HIGH, 3-state).
NREFON	62	O	Reference oscillator power-down (active LOW, 3-state).

SYMBOL	PIN	I/O	DESCRIPTION
GPON1	63	O	Sleep mode power-down 1 (active HIGH, 3-state).
GPON2	64	O	Sleep mode power-down 2 (active HIGH, open-drain output).
REFON	65	O	Sleep mode power-down 3 (active HIGH, 3-state).
DCLK	66	I	External DSP clock input.
$\overline{RSTP}$	67	I	PLL reset (active LOW with internal pull-down resistor).
CLKSEL	68	I	Timer clock source select.
V_{SSPLL}	69	–	PLL ground.
CKO	70	O	Low swing input buffer output.
V_{SS1}	71	–	I/O ground.
V_{DD1}	72	–	I/O power supply.
CKI	73	I	Reference clock input, low swing input 13 kHz.
V_{DDPLL}	74	–	PLL power supply.
TMS	75	I	JTAG port mode select (with internal pull-down resistor).
TDI	76	I	JTAG port data input (with internal pull-down resistor).
TDO	77	O	JTAG port data output.
TCKIO	78	I	Auxiliary test signal - tied to V_{SS} during operation.
TRSTN	79	I	JTAG port reset (with internal pull-down resistor).
V_{DD2}	80	–	Core power supply.
V_{SS2}	81	–	Core ground.
TCK	82	I	JTAG port clock input (with internal pull-down resistor).
$\overline{HCEN\_T}$	83	I	Host Interface Enable - Timer core (active LOW).
IO1/AEN	84	I/O	DSP general purpose I/O used for Voice Port control (CMOS level I/O). The PCF5083-3A has its own internal pull-up resistor, however both the PCF5083-2B and PCF5083-2C require a pull-up resistor.
IO2	85	I/O	DSP general purpose I/O used for Voice Port control (CMOS level I/O). The PCF5083-3A has its own internal pull-up resistor, however both the PCF5083-2B and PCF5083-2C require a pull-up resistor.
IO3/IRQN2	86	I/O	DSP general purpose I/O or Interrupt Request Input 2 (CMOS level I/O). The PCF5083-3A has its own internal pull-up resistor, however both the PCF5083-2B and PCF5083-2C require a pull-up resistor.
IO4/DTX	87	I/O	DSP general purpose I/O (CMOS level I/O, external pull-up resistor required).
HA0 to HA6	88 to 94	I	Host Interface Address.
HD0 to HD3	95 to 98	I/O	Host Interface Data (3-state).

SYMBOL	PIN	I/O	DESCRIPTION
V_{SS1}	99	–	I/O ground.
V_{DD1}	100	–	I/O power supply.
HD4 to HD7	101 to 104	I/O	Host Interface Data (3-state).
HR/W	105	I	Host Interface Write Enable.
$\overline{\text{HCEN\_D}}$	106	I	Host Interface Enable - DSP core (active LOW).
$\overline{\text{DTACK}}$	107	O	Host port acknowledge - used as DTACK from DSP core (active LOW, open-drain output).
SIXCLK	108	I	DSP serial input port X clock (CMOS level Schmitt trigger input).
SIXEN	109	I	DSP serial input port X enable.
SIXD	110	I	DSP serial input port X data.
SOXCLK	111	I	DSP serial output port X clock (CMOS level Schmitt trigger input).
V_{DD2}	112	–	Core power supply.
V_{SS2}	113	–	Core ground.
SOXEN	114	I	DSP serial output port X enable.
SOXD	115	O	DSP serial output port X data (3-state).
CLK20M	116	O	19.5 MHz CMOS level output.
$\overline{\text{FRAME\_INT}}$	117	O	TDMA frame interrupt (active LOW, open-drain output).
$\overline{\text{COMB\_INT}}$	118	O	Combined interrupt (active LOW, open-drain output).
$\overline{\text{HIPR\_INT}}$	119	O	High Priority Interrupt (active LOW, open-drain output).
CLK13M	120	O	13 MHz CMOS level output.
V_{SS1}	121	–	I/O ground.
V_{DD1}	122	–	I/O power supply.
AFS	123	I/O	Audio Interface Frame Sync signal (3-state).
ACLK	124	I/O	Audio Interface Clock (3-state).
ADI	125	I	Audio Interface Data In, RS232 clock if enabled.
ADO	126	O	Audio Interface Data Out (3-state).
TSCK1	127	I	Test Clock 1 - tied to V_{SS} during normal operation.
TSCK2	128	I	Test Clock 2 - tied to V_{DD2} during normal operation.

65 × 102 pixels matrix LCD driver PCF8549

FEATURES

- Single chip LCD controller/driver
- 65 row and 102 column outputs
- Display data RAM 65 × 102 bits
- On-chip:
  - Generation of LCD supply voltage
  - Generation of intermediate LCD bias voltages
  - Oscillator requires no external components (external clock also possible)
- 400 kHz Fast I²C Interface
- CMOS compatible inputs
- Mux rate: 65
- Logic supply voltage range $V_{DD1} - V_{SS}$: 1.5 to 6 V
- Voltage generator voltage range $V_{DD2/2\_HV} - V_{SS}$: 2.4 to 5 V
- Display supply voltage range $V_{LCD} - V_{SS}$: 7.0 to 16 V
- Low power consumption, suitable for battery operated systems
- Temperature compensation of V_{LCD}
- Interlacing for better display quality
- Slim chip layout, suited for chip-on-glass applications.

APPLICATIONS

- Telecom equipment
- Portable instruments
- Point of sale terminals.

GENERAL DESCRIPTION

The PCF8549 is a low power CMOS LCD controller driver, designed to drive a graphic display of 65 rows and 102 columns. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD supply and bias voltages, resulting in a minimum of external components and low power consumption. The PCF8549 interfaces to most microcontrollers via an I²C interface.

Packages

The PCF8549U/2 is available as bumped die. Sawn wafer as chip sorted in chip tray. For further details see Section "Bonding pads".

Customized TCP upon request.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8549U/2/F1	TRAY	chip with bumps in tray	

BLOCK DIAGRAM

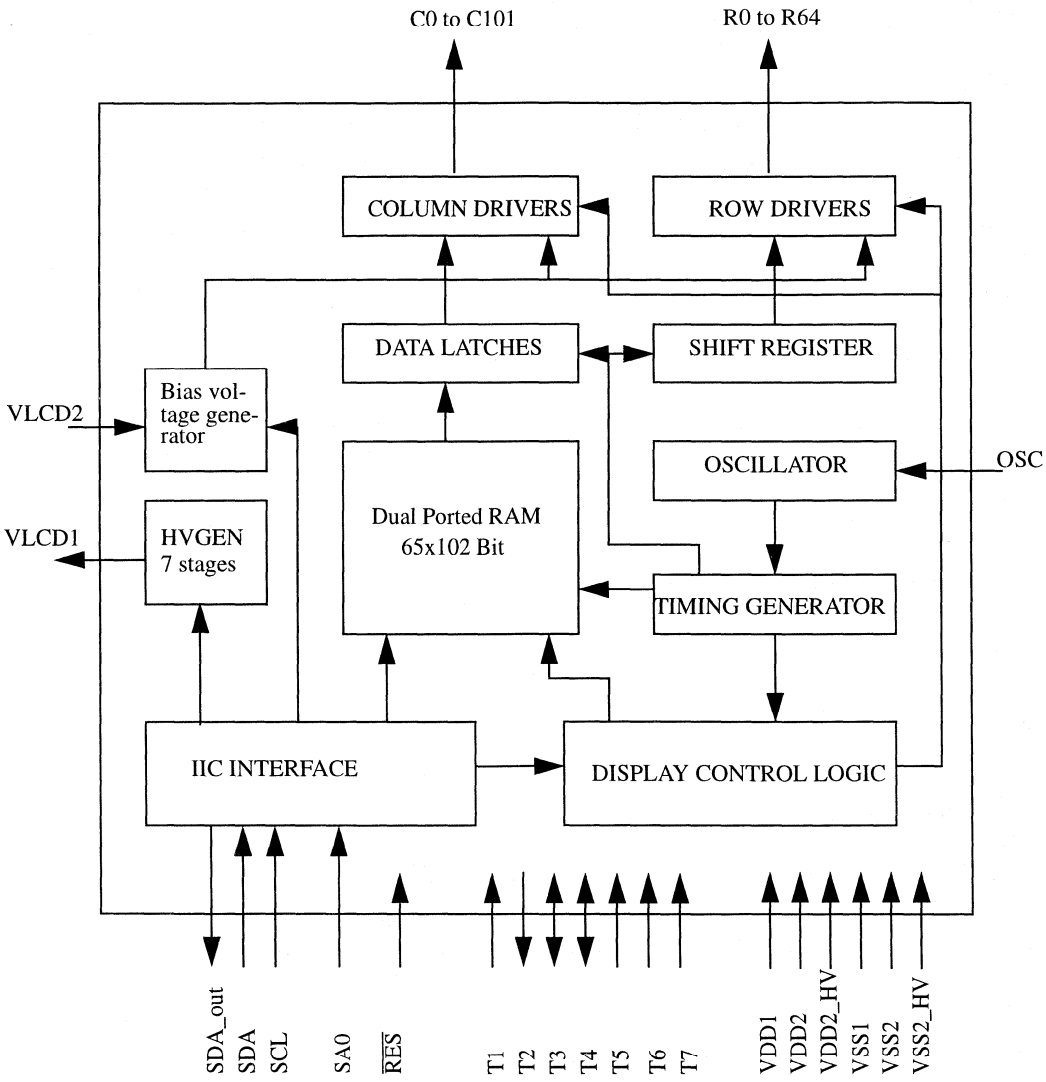


Fig.1 Block diagram.

PINNING

SYMBOL	DESCRIPTION
R0 to R64	LCD row driver outputs
C0 to C101	LCD column driver outputs
$V_{SS1,2,2\_HV}$	negative power supply
$V_{DD1,2,2\_HV}$	supply voltage
$V_{LCD1,2}$	LCD supply voltage
T1	test 1 input
T2	test 2 output
T3	test 3 I/O
T4	test 4 I/O
T5	test 5 input
T6	test 6 input
T7	test 7 input
SDA	I^2C data input
SCL	I^2C clock line
SDA_OUT	I^2C output
SA0	least significant bit of slave address
OSC	oscillator
$\overline{RES}$	external reset input, low active

Pin functions

R0 TO R64: ROW DRIVER OUTPUTS

These pads output the row signals.

C0 TO C101: COLUMN DRIVER OUTPUTS

These pads output the column signals.

$V_{SS1,2,2\_HV}$: NEGATIVE POWER SUPPLY RAILS

Negative power supplies.

$V_{DD1,2,2\_HV}$: POSITIVE POWER SUPPLY RAILS

V_{DD2} and V_{DD2_HV} are the supply voltages for the internal voltage generator. Both have to be on the same voltage and may be connected together outside of the chip. If the internal voltage generator is not used, they should be both connected to ground. V_{DD1} is used as power supply for the rest of the chip. This voltage can be a different voltage than V_{DD2} and V_{DD2_HV}.

$V_{LCD1,2}$: LCD POWER SUPPLY

Positive power supply for the liquid crystal display. If the internal voltage generator is used, the two supply rails V_{LCD1} and V_{LCD2} must be connected together. An external LCD supply voltage can be supplied using the V pad. In this case, V_{LCD1} has to be connected to ground, and the internal voltage generator has to be programmed to zero. If the PCF8549 is in power-down mode, the external LCD supply voltage has to be switched off.

T1, T2, T3, T4, T5, T6 AND T7: TEST PADS

T1, T3, T4, T5, T6 and T7 must be connected to V_{SS1}, T2 is to be left open. Not accessible to user.

SDA/SDA_OUT: I^2C DATA LINES

Output and input are separated. If both pads are connected together they behave like a standard I^2C pad.

SCL: I^2C CLOCK SIGNAL

Input for the I^2C-bus clock signal.

SA0: SLAVE ADDRESS

With the SA0 pin two different slave addresses can be selected. That allows to connect two PCF8549 LCD drivers to the same I^2C-bus.

OSC: OSCILLATOR

When the on-chip oscillator is used this input must be connected to V_{DD1}. An external clock signal, if used, is connected to this input.

$\overline{RES}$: RESET

This signal will reset the device. Signal is active low.

FUNCTIONAL DESCRIPTION

Block diagram functions

OSCILLATOR

The on-chip oscillator provides the clock signal for the display system. No external components are required and the OSC input must be connected to V_{DD1}. An external clock signal, if used, is connected to this input.

I^2C INTERFACE

The I^2C interface receives and executes the commands sent via the I^2C-bus. It also receives RAM-data and sends them to the RAM. During read access the 8-bit parallel data or the status register content is converted to a serial data stream and output via the I^2C-bus.

DISPLAY CONTROL LOGIC

The display control logic generates the control signals to read out the RAM via the 101 bit parallel port. It also generates the control signals for the row, and column drivers.

DISPLAY DATA RAM (DDRAM)

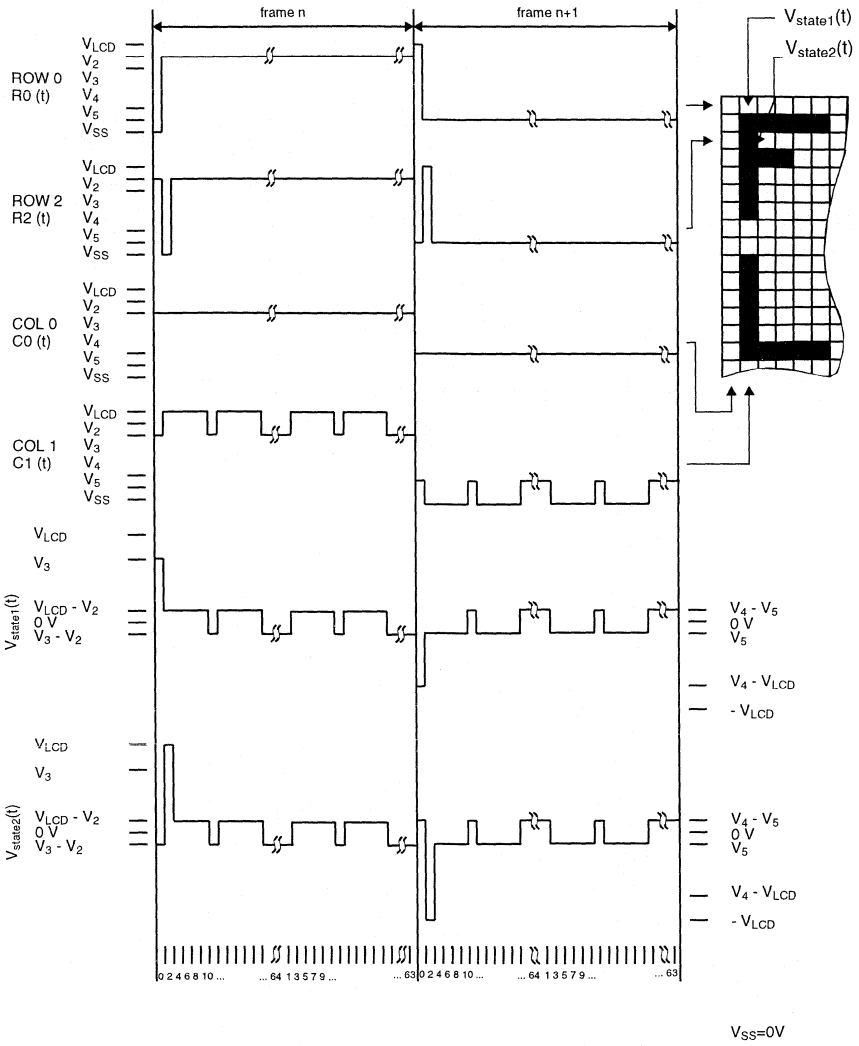
The PCF8549 contains a 65 × 102 bit static RAM which stores the display data. The RAM is divided into 8 banks of 102 bytes and one bank of 102 bits ((8 × 8 + 1) × 102 bits). During RAM access, data is transferred to the RAM via the I^2C interface. There is a direct correspondence between X-address and column output number.

TIMING GENERATOR

The timing generator produces the various signals required to drive the internal circuitry. Internal chip operation is not disturbed by operations on the I^2C-bus.

LCD ROW AND COLUMN DRIVERS

The PCF8549 contains 65 row and 102 column drivers, which connect the appropriate LCD bias voltages to the display in accordance with the data to be displayed. Figure 2 shows typical waveforms. Unused outputs should be left unconnected.



$V_{state1}(t) = C1(t) - R0(t)$
$V_{state2}(t) = C1(t) - R2(t)$

Fig.2 Typical LCD driver waveforms.

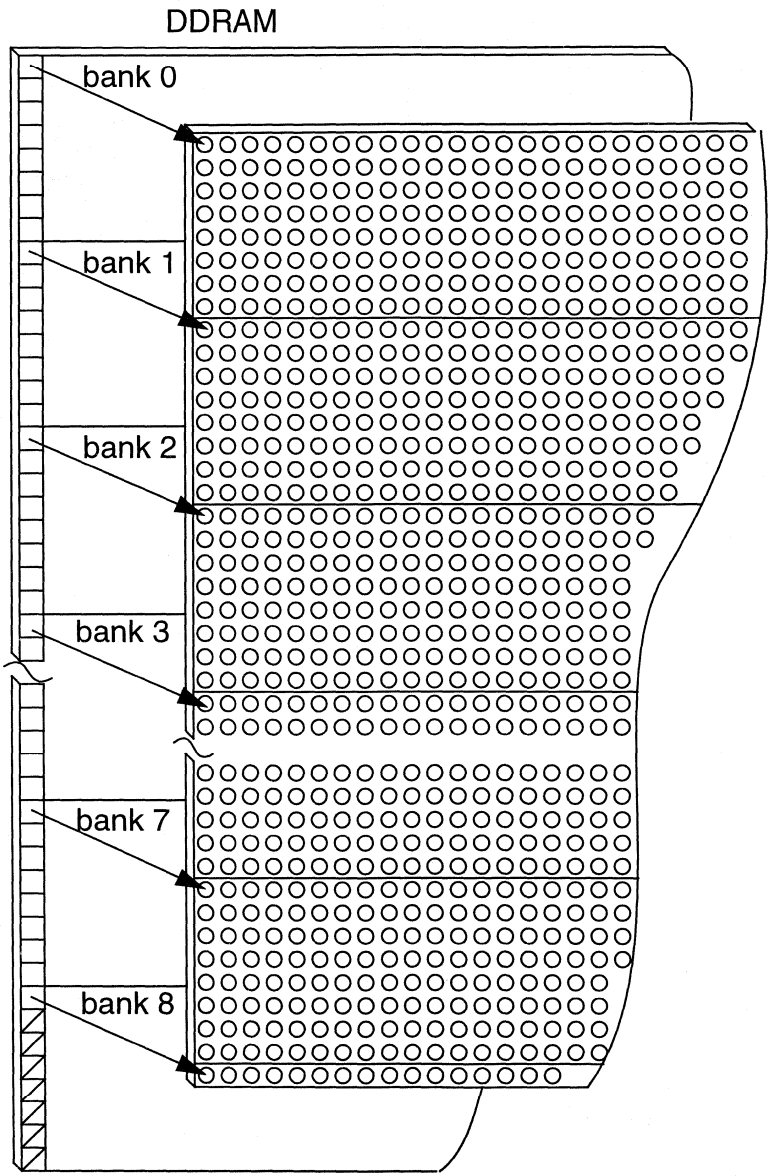


Fig.3 DDRAM to display mapping.

Addressing

The Display data RAM of the PCF8549 is accessed as indicated in Figs 3, 4, 4, 6 and 7. The display RAM has a matrix of 65 × 102 bits. The columns are addressed by the address pointer. The address ranges are:
X 0 to 101 (1100101b) and Y 0 to 8 (1000b). Addresses outside these ranges are not allowed. In vertical addressing mode (V = 1) the Y address increments (see Fig.7) after each byte. After the last Y address (Y = 8) Y wraps around to 0 and X increments to address the next column. In horizontal addressing mode (V = 0) the X address increments (see Fig.6) after each byte. After the last X address (X = 101) X wraps around to 0 and Y increments to address the next row. After the very last address (X = 101 and Y = 8) the address pointers wrap around to address (X = 0 and Y = 0).

The MX bit allows a horizontal mirroring: When MX = 1, the X address space is mirrored: The address X = 0 is then located at the right side (column 101) of the display (see Fig.4). When MX = 0 the mirroring is disabled and the address X = 0 is located at the left side (column 0) of the display (see Fig.4).

If the RM-bit (read-modify-write mode) is set, the address is only incremented after a write, otherwise the address is incremented after both read and write access to the display data RAM.

DISPLAY DATA RAM STRUCTURE

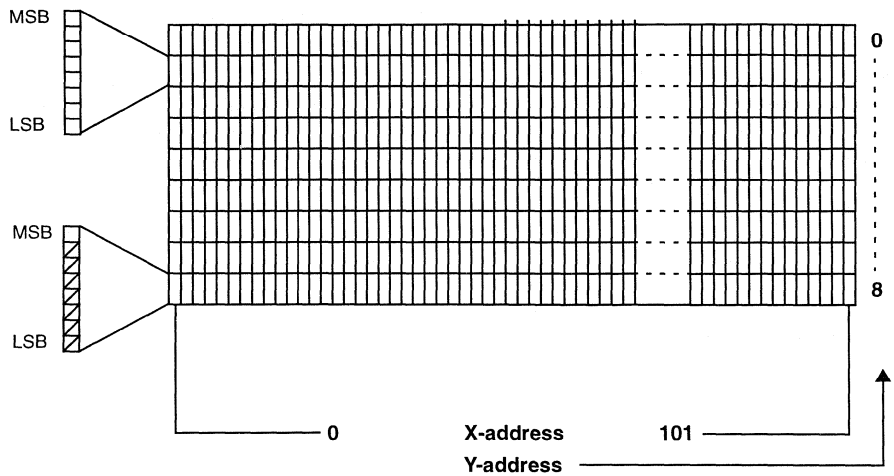


Fig.4 RAM format, addressing (MX = 0).

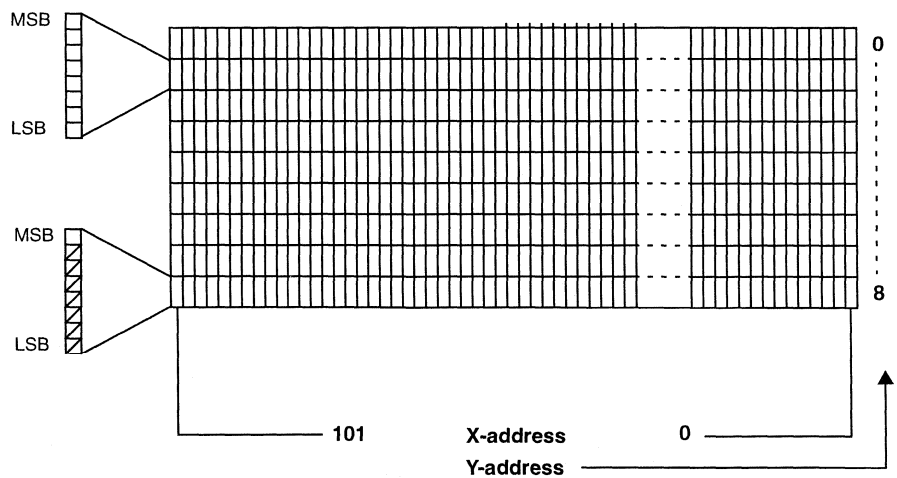


Fig.5 RAM format, addressing (MX = 1).

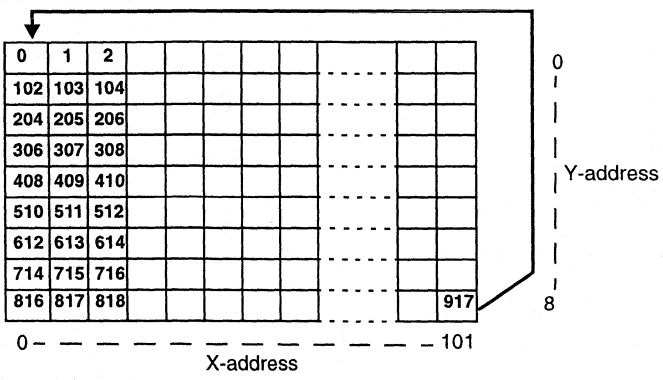


Fig.6 Sequence of writing data bytes into RAM with horizontal addressing (V = 0).

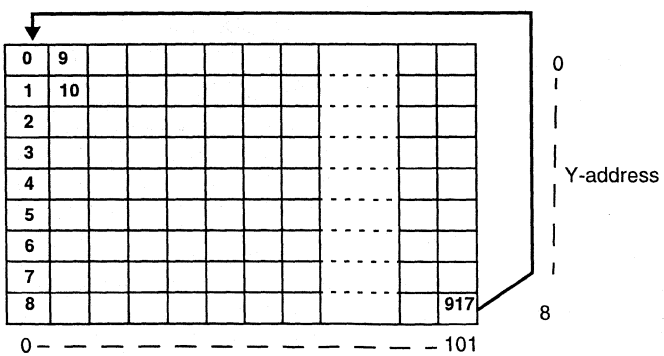


Fig.7 Sequence of writing data bytes into RAM with vertical addressing (V = 1).

RAM access

If the D/$\overline{C}$ bit is 1 the RAM can be accessed in both read and write access mode, depending on the R/$\overline{W}$ bit. The data is written to the RAM during the acknowledge cycle.

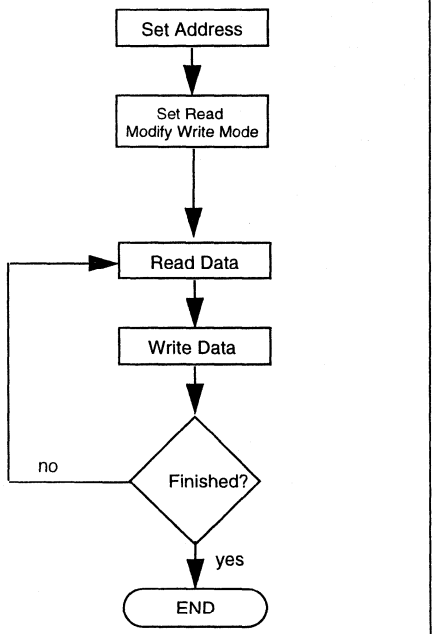


Fig.8 Read modify write access.

I²C-BUS INTERFACE

Characteristics of the I²C-bus

The I²C-bus is for bi-directional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

BIT TRANSFER (see Fig.9)

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

START AND STOP CONDITIONS (see Fig.10)

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P).

SYSTEM CONFIGURATION (see Fig.11)

- Transmitter: The device which sends the data to the bus
- Receiver: The device which receives the data from the bus
- Master: The device which initiates a transfer, generates clock signals and terminates a transfer
- Slave: The device addressed by a master
- Multi-Master: More than one master can attempt to control the bus at the same time without corrupting the message
- Arbitration: Procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted
- Synchronisation: Procedure to synchronize the clock signals of two or more devices.

ACKNOWLEDGE (see Fig.12)

Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

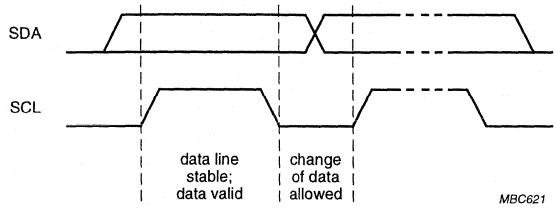


Fig.9 Bit transfer.

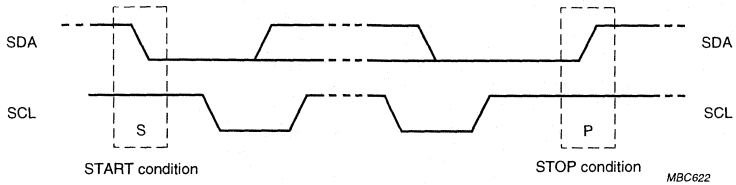


Fig.10 Definition of start and stop conditions.

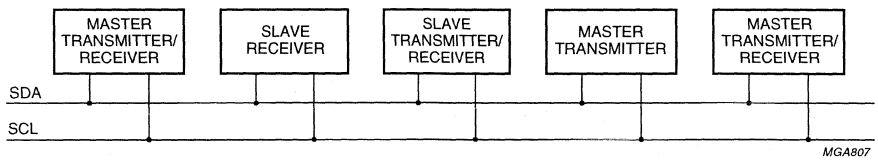


Fig.11 System configuration.

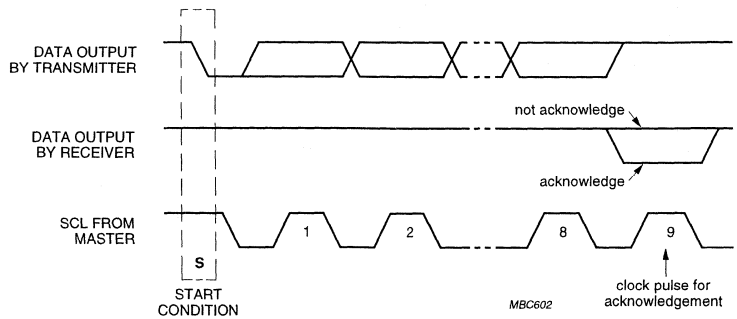


Fig.12 Acknowledgement on the I²C-bus.

I²C-bus protocol

The PCF8549 supports both read and write access. The R/$\overline{W}$ bit is part of the slave address.

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. Two 7-bit slave addresses (0111100 and 0111101) are reserved for the PCF8549. The least significant bit of the slave address is set by connecting the input SA0 to either logic 0 (V_{SS1}) or 1 (V_{DD1}).

The I²C-bus protocol is illustrated in Fig.13.

The sequence is initiated with a START condition (S) from the I²C-bus master which is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I²C-bus transfer. After acknowledgement, one or more command words follow which define the status of the addressed slaves. A command word consists of a control byte, which defines Co and D/$\overline{C}$, plus a data byte (see Fig.13 and Table 1).

The last control byte is tagged with a cleared most significant bit, the continuation bit Co. After a control byte with a cleared Co-bit, only data bytes will follow. The state of the D/$\overline{C}$-bit defines whether the data-byte is interpreted as a command or as RAM-data.The control and data bytes are also acknowledged by all addressed slaves on the bus.

After the last control byte, depending on the D/$\overline{C}$ bit setting, either a series of display data bytes or command data bytes may follow. If the D/$\overline{C}$ bit was set to '1', these display bytes are stored in the display RAM at the address specified by the data pointer. The data pointer is automatically updated and the data is directed to the intended PCF8549 device. If the D/$\overline{C}$ bit of the last control byte was set to '0', these command bytes will be decoded and the setting of the device will be changed according to the received commands. The acknowledgement after each byte is made only by the addressed slave. At the end of the transmission the I²C-bus master issues a stop condition (P).

If the R/$\overline{W}$ bit is set to one in the slave-address, the chip will output data immediately after the slave-address according to the D/$\overline{C}$ bit, which was sent during the last write access. If no acknowledge is generated by the master after a byte, the driver stops transferring data to the master.

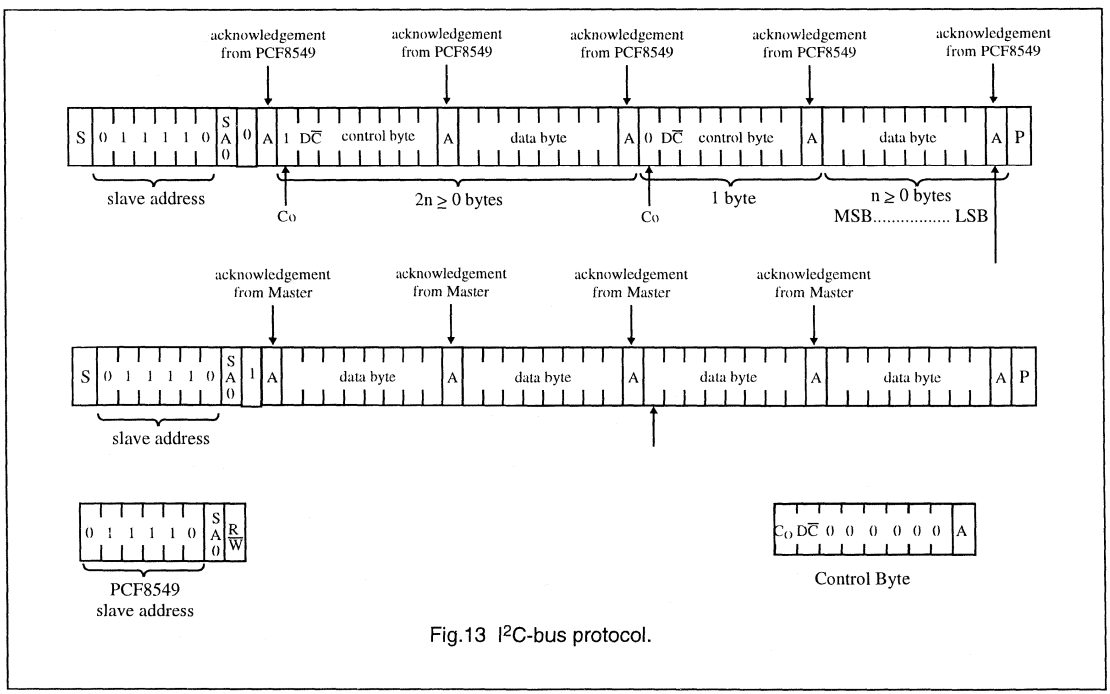


Fig.13 I²C-bus protocol.

INSTRUCTIONS

The instruction format is divided into two modes: If D/$\overline{C}$ is set low, the status byte can be read or commands can be sent to the chip, depending on the R/$\overline{W}$ signal. If D/$\overline{C}$ is set high, the DDRAM will be accessed. Every instruction can be sent in any order to the PCF8549.

Table 1 Instruction set

INSTRUCTION	D/$\overline{C}$	R/$\overline{W}$	COMMAND BYTE								DESCRIPTION
			DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
H = 0 or 1											
NOP	0	0	0	0	0	0	0	0	0	0	no operation
Function Set	0	0	0	0	1	MX	MY	PD	V	H	power down control; entry mode; Extended Instruction Set control (H)
Read Status Byte	0	1	PD	X	X	D	E	MX	MY	X	reads status byte
Write Data	1	0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	writes data to RAM
Read Data	1	1	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	reads data from RAM
H = 0											
Set Read Modify Write	0	0	0	0	0	0	0	0	1	RM	sets the read-modify-write mode
Reserved	0	0	0	0	0	0	0	1	X	X	do not use
Display Control	0	0	0	0	0	0	1	D	0	E	sets display configuration
Reserved	0	0	0	0	0	1	X	X	X	X	do not use
Set Y address of RAM	0	0	0	1	0	0	Y_3	Y_2	Y_1	Y_0	sets Y-address of RAM: $0 \leq Y \leq 8$
Set X address of RAM.	0	0	1	X_6	X_5	X_4	X_3	X_2	X_1	X_0	sets X-address of RAM: $0 \leq X \leq 101$
H = 1											
Reserved	0	0	0	0	0	0	0	0	0	1	do not use
Reserved	0	0	0	0	0	0	0	0	1	X	do not use
Temperature Control	0	0	0	0	0	0	0	1	TC_1	TC_0	set temperature coefficient (TCx)
Reserved	0	0	0	0	0	0	1	X	X	X	do not use
Bias System	0	0	0	0	0	1	0	BS_2	BS_1	BS_0	Set Bias System(BSx)
Reserved	0	0	0	1	X	X	X	X	X	X	do not use (reserved for test...)
Set V_{OP}	0	0	1	V_{OP6}	V_{OP5}	V_{OP4}	V_{OP3}	V_{OP2}	V_{OP1}	V_{OP0}	write V_{OP} to register

Table 2 Explanations for symbols in Table 1

BIT		0	1	RESET STATE
PD		chip is active	chip is in power down mode	1
V		horizontal addressing	vertical addressing	0
H		use basic instruction set	use extended instruction set	0
MX		normal X-addressing	X-address is mirrored	0
MY		display is not vertically mirrored	display is vertically mirrored	0
RM		read-modify-write mode is disabled	read-modify-write mode is enabled	0
D and E	00	display blank		D = 0 E = 0
	10	normal mode		
	01	all display segments on		
	11	inverse video mode		
TC[1 : 0]	00	V_{LCD} temperature coefficient 0		TC[1 : 0] = 00
	01	V_{LCD} temperature coefficient 1		
	10	V_{LCD} temperature coefficient 2		
	11	V_{LCD} temperature coefficient 3		
BS[2 : 0]		bias system		BS[2 : 0] = 000

External reset ($\overline{RES}$)

After power-on a reset pulse has to be applied immediately to the chip, as it is in an undefined state. A reset of the chip can be achieved with the external reset pin. After the reset the LCD driver is set to the following status:

- Power down mode (PD = 1)
- All LCD-outputs at V_{SS} (display off)
- Read-modify-write mode is disabled (RM = 0)
- Horizontal addressing (V = 0)
- Normal instruction set (H = 0)
- Normal display (MX = MY = 0)
- Display blank (E = D = 0)
- Address counter X[6 : 0] = 0 and Y[3 : 0] = 0
- Temperature coefficient (TC[1 : 0] = 0)
- Bias system (BS[2 : 0] = 0)
- Read-modify-write mode disabled (RM = 0)
- V_{LCD} is equal to 0, the HV generator is switched off (V_{OP}[6 : 0] = 0)
- After power-on, RAM data are undefined; The reset signal does not change the content of the RAM.

Set read-modify-write

When RM = 0, the read-modify-write mode is disabled. The X/Y-address counter is incremented after every read or write access to the display data RAM.

When RM = 1, the read-modify-write mode is enabled. In this mode the X/Y-address is incremented only after a write access to the display data RAM. The X/Y-address will not be incremented after a read access to the RAM.

Function Set

PD (POWER DOWN)

- All LCD outputs at V_{SS} (display off)
- Bias generator and V_{LCD} generator off
- Oscillator off (external clock possible)
- V_{LCD} can be disconnected
- Parallel bus, command, etc. function
- RAM contents not cleared; RAM data can be written.

V

When V = 0, the horizontal addressing is selected. The data is written into the RAM as shown in Fig.6. When V = 1, the vertical addressing is selected. The data is written into the RAM as shown in Fig.7.

H

When H = 0 the commands 'display control', 'set Y address' and 'set X address' can be performed, when H = 1 the other commands can be executed. The commands 'write data' and 'function set' can be executed in both cases.

MX

When MX = 0, the display is written from left to right (X = 0 is on the left side, X = 100 is on the right side of the display). When MX = 1 the display is written from right to left (X = 0 is on the right side, X = 100 is on the left side of the display).

MY

When MY = 1, the display is mirrored vertically.

Display Control

D AND E

The bits D and E select the display mode (see Table 2).

Set Y address of RAM

Y[3 : 0] defines the Y address vector address of the RAM.

Table 3 X-/Y-Address range

Y Y Y Y 3 2 1 0	CONTENT	ALLOWED X-RANGE
0 0 0 0	bank 0 (display RAM)	0 to 101
0 0 0 1	bank 1 (display RAM)	0 to 101
0 0 1 0	bank 2 (display RAM)	0 to 101
0 0 1 1	bank 3 (display RAM)	0 to 101
0 1 0 0	bank 4 (display RAM)	0 to 101
0 1 0 1	bank 5 (display RAM)	0 to 101
0 1 1 0	bank 6 (display RAM)	0 to 101
0 1 1 1	bank 7 (display RAM)	0 to 101
1 0 0 0	bank 8 (display RAM)	0 to 101

In bank 8 only the MSB is accessed.

Set X address of RAM

The X address points to the columns. The range of X is 0 to 101(65 hex).

Temperature Control

Due to the temperature dependency of the liquid crystals viscosity the LCD controlling voltage V_{LCD} must be increased with lower temperature to maintain optimal contrast. There are 4 different temperature coefficients available in the

PCF8549 (see Fig.14). The coefficients are selected by the two bits TC[1 : 0]. Table 6 shows the typical values of the different temperature coefficients. The coefficients are proportional to the programmed V_{LCD}.

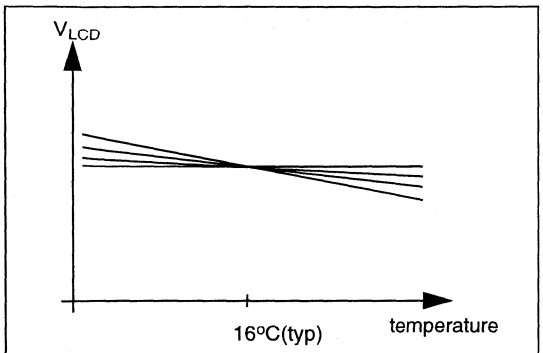


Fig.14 Temperature coefficients.

Bias value:

The bias voltage levels are set in the ratio of R – R – nR – R – R giving a $\frac{1}{n+4}$ bias system. The resulting bias levels are shown in table 5.

Different multiplex rates require different factors n (see Table 4). This is programmed by BS[2 : 0]. For MUX 1 : 65 the optimum bias value n is given by: $n = \sqrt{m} - 3 = \sqrt{65} - 3 = 5.06 = 5$

resulting in ⅛bias.

Table 4 Programming the required Bias system

BS[2]	BS[1]	BS[0]	n	b (RES. COUNT)	MUX RATE
0	0	0	7	11	1 : 100
0	0	1	6	10	1 : 81
0	1	0	5	9	1 : 64
0	1	1	4	8	1 : 49
1	0	0	3	7	1 : 36

BS[2]	BS[1]	BS[0]	n	b (RES. COUNT)	MUX RATE
1	0	1	2	6	1 : 24
1	1	0	1	5	1 : 16
1	1	1	0	4	1 : 9

Table 5 LCD bias voltage

SYMBOL	BIAS VOLTAGES
V1	V_{LCD}
V2	$(b-1)/b \times V_{LCD}$
V3	$(b-2)/b \times V_{LCD}$
V4	$2/b \times V_{LCD}$
V5	$1/b \times V_{LCD}$
V6	V_{SS}

Set V_{OP} value:

The operation voltage V_{LCD} can be set by software. The generated voltage is dependent of the temperature, the programmed temperature coefficient (TC), and the programmed voltage at reference temperature (T_{CUT}).

(1)

$$V_{LCD} = (a + VOP \cdot b) + (T - T_{CUT}) \cdot TC$$

The voltage at reference temperature ($V_{LCD}(T=T_{CUT})$) can be calculated as:

(2)

$$V_{LCD} = (a + VOP \cdot b)$$

The parameters are explained in table 6.

The maximum voltage that can be generated is depending on the $V_{DD2/2\_HV}$ Voltage and the display load current. The relation ship is shown in Fig.16.

The charge pump is turned off if Vop[6 : 0] is set to zero.

For Mux 1 : 65 the optimum operation voltage of the liquid can be calculated as:

$$V_{LCD} = \frac{1 + \sqrt{65}}{\sqrt{2 \cdot \left(1 - \frac{1}{\sqrt{65}}\right)}} \cdot V_{th} = 6.85 \cdot V_{th}$$

where V_{th} is the threshold voltage of the liquid crystal material used.

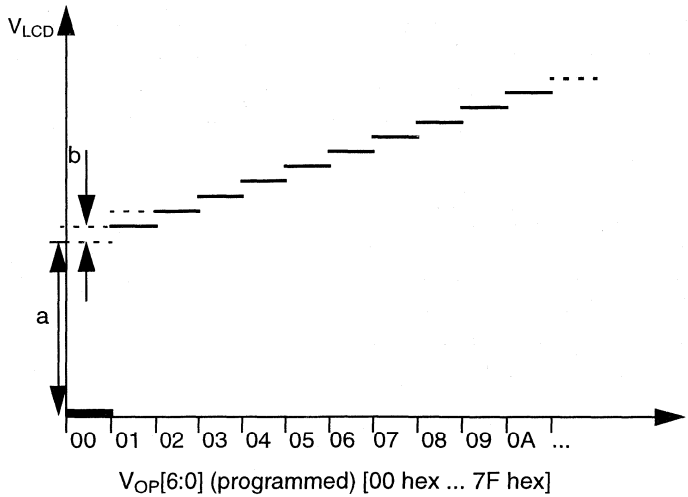


Fig.15 V_{OP} programming of PCF8549.

Table 6 Typical values for parameters for the HV-Generator programming

SYMBOL		VALUE	UNIT
a		7.06	V
b		0.06	V
T_{CUT}		16	°C
TC	00	$-0.142 \cdot 10^{-3} \cdot V_{LCD}\,(T = T_{CUT})$	V/°C
	01	$-1.3 \cdot 10^{-3} \cdot V_{LCD}\,(T = T_{CUT})$	V/°C
	10	$-2.467 \cdot 10^{-3} \cdot V_{LCD}\,(T = T_{CUT})$	V/°C
	11	$-3.483 \cdot 10^{-3} \cdot V_{LCD}\,(T = T_{CUT})$	V/°C

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134); all voltages referred to V_{SS} = 0V unless otherwise specified.

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{DD}	supply voltage range	-0.5	+7	V
V_{LCD}	supply voltage range LCD	-0.5	+17	V
I_{SS}	supply current	-50	50	mA
V_I/V_O	input/output voltage range	-0.5	V_{DD}+0.5	V
V_{OLCD}	LCD output voltage range	-0.5	V_{LCD}+0.5	V
I_I	DC input current	-10	10	mA
I_O	DC output current	-10	10	mA
P_{TOT}	power dissipation per package	-	300	mW
P_O	power dissipation per output	-	50	mW
T_{AMB}	operating ambient temperature. range	-40	+85	℃
T_{STG}	storage temperature range	-65	+150	°C

Notes

1. Stresses above those listed under Limiting Values may cause permanent damage to the device.
2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.
3. with external LCD supply voltage external supplied **(voltage generator disabled)**. V_{DDmax} (V_{DD2},V_{DD2_HV}) is **5V** if LCD supply voltage is internally generated (voltage generator enabled).

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS Devices"). The PCF8549 withstands the following stress:

- approximately 1.0kV Human Body Model
- approximately 150V Machine Model

DC CHARACTERISTICS

Table 7 V_{DD1} = 1.5 to 6 V; $V_{DD2/2\_HV}$ = 2.4 to 5.0 V; V_{DD2} = V_{DD2_HV}; V_{SS1} = V_{SS2} = V_{SS2_HV} = 0 V; V_{LCD} = 7 to 16 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD1}	Logic supply voltage range		1.5	3	6	V
V_{DD2}, V_{DD2_HV}	HV Generator supply range		2.4		5	V
I_{VDD1}	supply current internal V_{LCD}	V_{LCD} = 10.0V; f_{scl} = 0; display load = 0;		30	80	µA
$I_{VDD2/2\_HV}$	supply current internal V_{LCD}	V_{LCD} = 10.0V; f_{scl} = 0; display load = 0; (1)(5)		600	1200	µA
I_{VDD1}	supply current external V_{LCD}	V_{LCD} = 10.0V; f_{scl} = 0; display load = 0;		30	80	µA
$I_{VDD2/2\_HV}$	supply current external V_{LCD}	V_{LCD} = 10.0V; f_{scl} = 0; display load = 0; (2)(5)		0	10	µA
I_{VDD1}	supply current	power-down mode; V_{LCD} = 0V; f_{scl} = 0; display load = 0		0.5	10	µA
I_{LCD}	supply current external V_{LCD}	V_{LCD} = 10 V; f_{SCL}= 0, display load = 0; (2)		50	130	µA
$V_{LCD(tol)}$	V_{LCD} tolerance internal generated	V_{DD} = 2.7V; V_{LCD} = 10V; f_{SCL} = 0; display load = 0;(3)(4)(6)			+/- 500	mV
V_{IL}	LOW level input voltage		V_{SS}		0.3V_{DD}	V
V_{IH}	HIGH level input voltage		0.7 V_{DD}		V_{DD}	V
I_{OL}	LOW level output current (SDA)	V_{OL} = 0.4V; V_{DD1} = 5 V		3.0		mA
I_L	leakage current	V_I = V_{DD1} or V_{SS1}	-1		+1	µA
R_{ROW}	Row output resistance R0 to R64			12	20	kOhm
R_{COL}	Column output resistance C0 to C101			12	20	kOhm

Note

1. When a display is connected the I_{VDD2_HV} increases with 7 x display load current due to 7 stage charge pump.
2. With external V_{LCD}, the display load current does not translate into increased I_{VDD2_HV}.
3. For TC1, TC2 and TC3
4. The maximum possible VLCD voltage that may be generated is dependent on voltage ($V_{DD2/2\_HV}$), temperature and (display) load.
5. V_{DD2} V_{DD2_HV} connected together
6. Difference to the theoretical value given by equation 1

AC CHARACTERISTICS

Table 8 V_{DD1} = 1.5 to 6 V; $V_{DD2/2\_HV}$ = 2.4 to 5.0 V; $V_{DD2} = V_{DD2\_HV}$; $V_{SS1} = V_{SS2} = V_{SS2\_HV}$ = 0 V; V_{LCD} = 7 to 16 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{OSC}	oscillator frequency		19	32	64	kHz
f_{EXT}	external clock frequency	(2)	10	32	64	kHz
t_{start}	oscillator start up time	(5)	–	450	1600	us
f_{FRAME}	frame frequency	f_{EXT} = 32 kHz;(1)	–	62	–	Hz
t_{VHRL}	VDD to $\overline{RES}$ Low	(5)			1	ms
t_{PWRES}	reset low pulse width		400	–	–	ns
I²C timing characteristics						
f_{SCLK}	SCL clock frequency	(6)	DC	–	400	kHz
t_{LOW}	SCL clock low period		1.3	–	–	us
t_{HIGH}	SCL clock high period		0.6	–	–	us
$t_{SU;Data}$	Data set-up time		100	–	–	ns
$t_{HD;Data}$	Data hold time		0	–	0.9	us
t_R	SCL and SDA rise time	(3)	20 + 0.1 Cb	–	300	ns
t_F	SCL and SDA fall time	(3)	20 + 0.1 Cb	–	300	ns
C_b	Capacitive load represented by each bus line		–	–	400	pF
$t_{SU;STA}$	setup time for a repeated START condition		0.6	–	–	us
$t_{HD;STA}$	start condition hold time		0.6	–	–	us
$t_{SU;DAT}$	data set-up time		100	–	–	ns
$t_{HD;DAT}$	data hold-time		0	–	–	ns
$t_{SU;STO}$	setup time for STOP condition		0.6	–	–	us
t_{SW}	tolerable spike width on bus	(4)	–	–	50	ns
t_{BUF}	BUS free time between a STOP and START condition		1.3	–	–	us

Note

1. $f_{FRAME} = \frac{f_{EXT}}{520}$
2. Duty cycle of 50 +/-5%.
3. The rise and fall times specified here refer to the driver device (i.e. not PCF8549) and are part of the general fast I²C-bus specification. When PCF8549 asserts an acknowledge on SDA, the minimum fall time is 10ns. C_b= capacitive load per bus line.
4. The device inputs SDA and SCL are filtered and will reject spikes on the bus lines of width < $t_{SW(max)}$.
5. Not tested in production
6. Only for VDD1= 2V to 6V

TYPICAL CHARACTERISTICS

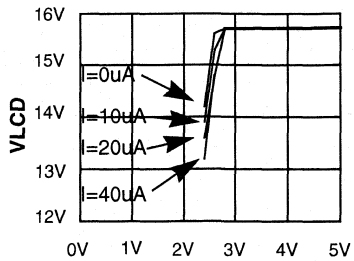


Fig.16 VLCD dependency of VDD2, VDD2_HV and load current. Programmed VLCD=15.8V (@ Room Temperature in special Test mode)

RESET

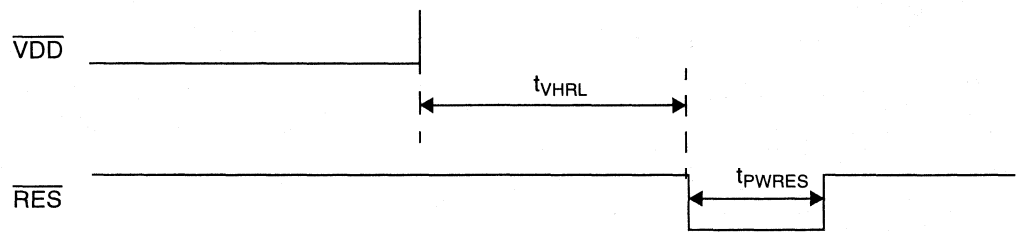
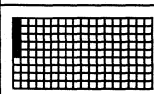
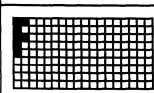
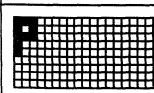
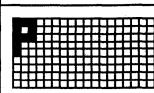
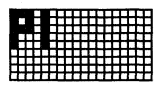
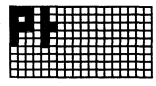
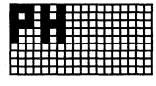


Fig.17 Reset timing.

APPLICATION INFORMATION

Table 9 programming example for PCF8549

STEP	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DISPLAY	OPERATION
1	I^2C start									
2	0	1	1	1	1	0	0	0		Slave address for write
3	0	0	0	0	0	0	0	0		Control byte with cleared C_O bit and D/$\overline{C}$ set to 0.
4	0	0	1	0	0	0	0	1		Function Set PD = 0; V = 0; select extended instruction set (H = 1 mode)
5	0	0	0	1	0	0	1	0		Set Bias System 2. This is the recommended Bias System for a multiplex rate 1:65
6	1	1	1	0	1	0	1	0		set V_{OP} V_{OP} is set to a +16 × b [V]. Please note: The required voltage is depending on the liquid.
7	0	0	1	0	0	0	0	0		Function Set PD = 0; V = 0; select normal instruction set (H = 0 mode)
8	0	0	0	0	1	1	0	0		Display Control set normal mode (D = 1 and E = 0)
9	I^2C start									Restart: To write into the Display RAM the D/$\overline{C}$ must be set to 1; therefore a control byte is needed.
10	0	1	1	1	1	0	0	0		Slave address for write
11	0	1	0	0	0	0	0	0		Control byte with cleared C_O bit and D/$\overline{C}$ set to 1.
12	1	1	1	1	1	0	0	0		Data Write Y and X are initialized to 0 by default, so they aren't set here
13	1	0	1	0	0	0	0	0		Data Write
14	1	1	1	0	0	0	0	0		Data Write

STEP	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DISPLAY	OPERATION
15	0	0	0	0	0	0	0	0		Data Write
16	1	1	1	1	1	0	0	0		Data Write
17	0	0	1	0	0	0	0	0		Data Write
18	1	1	1	1	1	0	0	0		Data Write
19	I^2C start									Restart
20	0	1	1	1	1	0	0	0		Slave address for write
21	1	0	0	0	0	0	0	0		Control byte with set C_O bit and D/$\overline{C}$ set to 0.
22	0	0	0	0	1	1	0	1		Display Control Set inverse video mode (D = 1 and E = 1)
23	1	0	0	0	0	0	0	0		Control byte with set C_O bit and D/$\overline{C}$ set to 0.
24	1	0	0	0	0	0	0	0		Set X address of RAM set address to '0000000'
25	1	1	0	0	0	0	0	0		Control byte with set C_O bit and D/$\overline{C}$ set to 1.
26	0	0	0	0	0	0	0	0		Data Write
27	0	0	0	0	0	0	0	0		Control byte with cleared C_O bit and D/$\overline{C}$ set to 0.
28	1	0	0	0	0	0	0	0		Set X address of RAM Set address to '0000000'
29	0	0	0	0	0	0	0	1		Set Read Modify Write Mode

STEP	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DISPLAY	OPERATION
30	I²C start									Restart
31	0	1	1	1	1	0	0	0		Slave address for write
32	1	1	0	0	0	0	0	0		Control byte with set C_O bit and D/$\overline{C}$ set to 1.
33	I²C start									Restart
34	0	1	1	1	1	0	0	1		Slave address for read
35	1	0	0	0	0	0	0	0		Read Data From Address '0000000'
36	1	0	0	0	0	0	0	0		Read Data From Address '0000000' again. Master does not send an acknowledge to stop the read access.
37	I²C start									Restart
38	0	1	1	1	1	0	0	0		Slave address for write
39	1	1	0	0	0	0	0	0		Control byte with set C_O bit and D/$\overline{C}$ set to 1.
40	1	1	1	1	1	0	0	0		Write Data
41	1	0	0	0	0	0	0	0		Control byte with set C_O bit and D/$\overline{C}$ set to 0.
42	I²C start									Restart
43	0	1	1	1	1	0	0	1		Slave address for read
44	1	0	0	0	0	0	0	0		Read Status Byte

APPLICATION INFORMATION

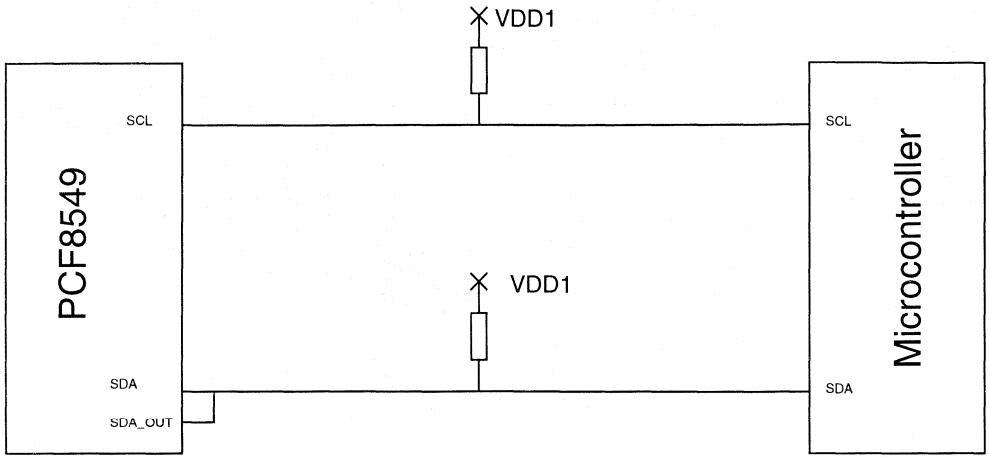


Fig.18 Application diagram: Connecting the I2C Interface

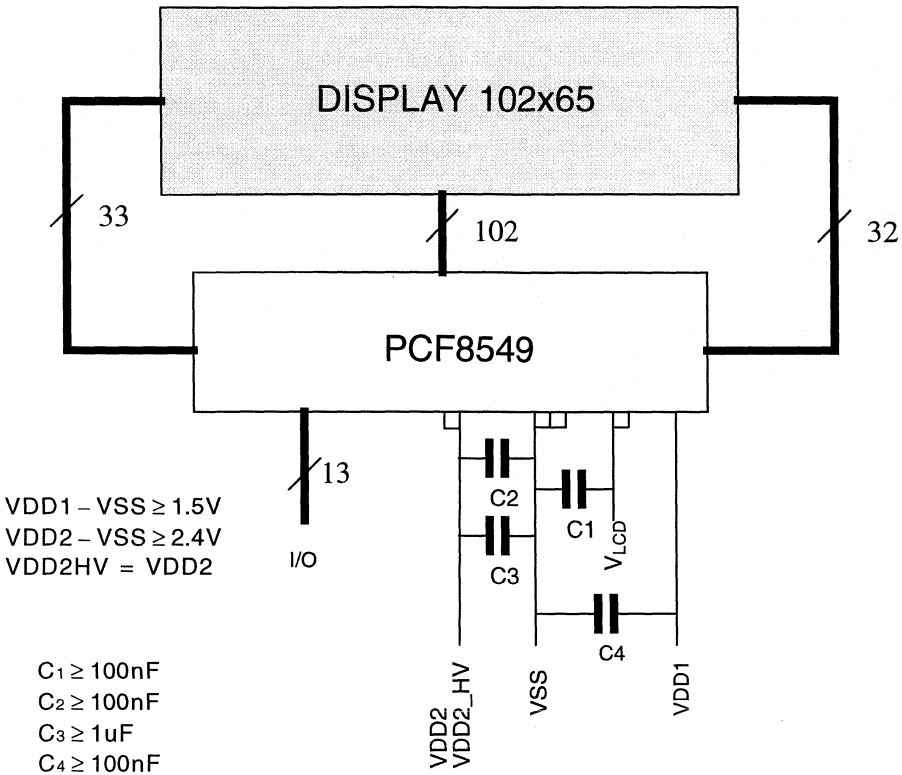


Fig.19 Application diagram: Connecting the power supplies

The pinning of the PCF8549 is optimized for single plane wiring e.g. for chip-on-glass display modules. Display size: 65 × 102 pixels.

CHIP INFORMATION

The PCF8549 is manufactured in n-well CMOS technology.

The substrate is on V_{SS} potential.

BONDING PADS

	VALUE	UNIT
Pad pitch	min. 100	µm
Pad size, alumin.	80 × 100	µm
Passivation.	48 × 78	µm
Bumps	60 (±6) × 90 (±6) × 17.5 (±5)	µm
Wafer thickness	380 (±25)	µm

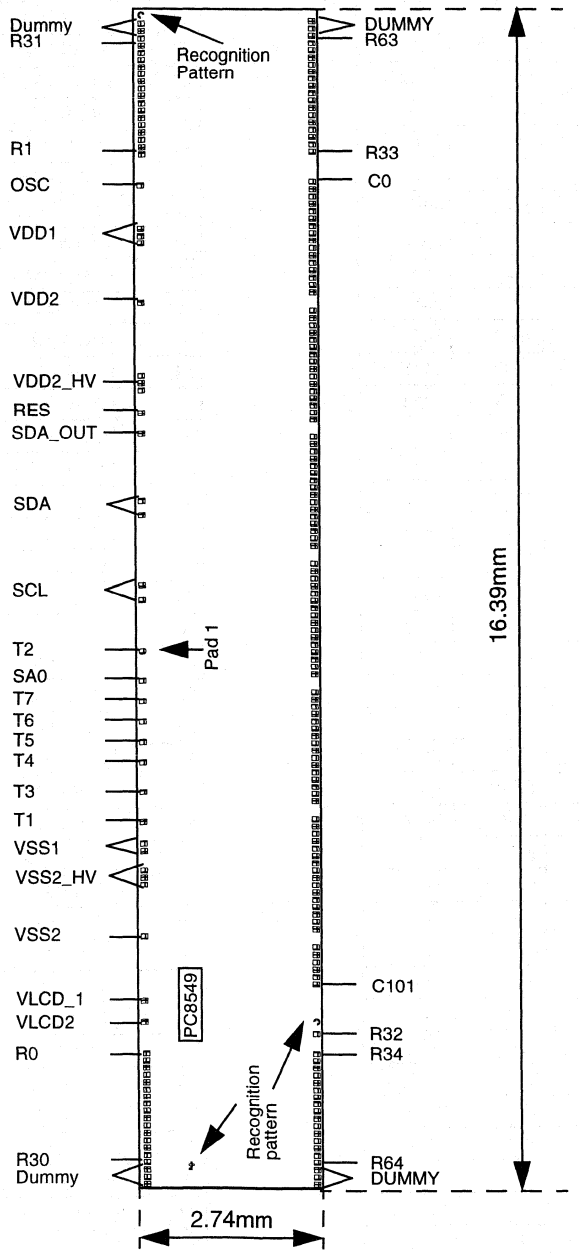

Dummy
R31
Recognition
Pattern
DUMMY
R63
R1
R33
OSC
C0
VDD1
VDD2
VDD2_HV
RES
SDA_OUT
SDA
SCL
T2
Pad 1
SA0
T7
T6
T5
T4
T3
T1
VSS1
VSS2_HV
VSS2
PC8549
C101
VLCD_1
VLCD2
R32
R0
R34
Recognition
pattern
R30
Dummy
R64
DUMMY
16.39mm
2.74mm

Fig.20 Pads.

Table 10 Bonding pad locations (dimensions in um).

Pad	Pad name	X	Y
1	T2	7359.5	2462
2	SA0	6958	2462
3	T7	6679	2462
4	T6	6400	2462
5	T5	6121	2462
6	T4	5841.5	2462
7	T3	5431.5	2462
8	T1	5022	2462
9	VSS1	4724	2458
10	VSS1	4624	2458
11	VSS2_HV	4359	2458
12	VSS2_HV	4259	2458
13	VSS2_HV	4159	2458
14	VSS2	3458.5	2458
15	VLCD1	2580	2462
16	VLCD2	2294	2462
17	ROW<0>	1870	2437
18	ROW<2>	1770	2437
19	ROW<4>	1670	2437
20	ROW<6>	1570	2437
21	ROW<8>	1470	2437
22	ROW<10>	1370	2437
23	ROW<12>	1270	2437
24	ROW<14>	1170	2437
25	ROW<16>	1070	2437
26	ROW<18>	970	2437
27	ROW<20>	870	2437
28	ROW<22>	770	2437
29	ROW<24>	670	2437
30	ROW<26>	570	2437
31	ROW<28>	470	2437
32	ROW<30>	370	2437
33	Dummy 4	270	2437
34	Dummy 5	170	2437
35	Dummy 6	70	2437
36	Dummy 3	70	84
37	Dummy 2	170	84
38	Dummy 1	270	84
39	ROW<64>	370	84
40	ROW<62>	470	84
41	ROW<60>	570	84
42	ROW<58>	670	84
43	ROW<56>	770	84
44	ROW<54>	870	84
45	ROW<52>	970	84
46	ROW<50>	1070	84
47	ROW<48>	1170	84
48	ROW<46>	1270	84
49	ROW<44>	1370	84
50	ROW<42>	1470	84
51	ROW<40>	1570	84
52	ROW<38>	1670	84
53	ROW<36>	1770	84
54	ROW<34>	1870	84
55	ROW<32>	2137	84
56	COL<101>	2812	84
57	COL<100>	2914	84
58	COL<99>	3014	84
59	COL<98>	3114	84
60	COL<97>	3214	84
61	COL<96>	3314	84
62	COL<95>	3560	84
63	COL<94>	3660	84
64	COL<93>	3760	84
65	COL<92>	3860	84
66	COL<91>	3960	84
67	COL<90>	4060	84
68	COL<89>	4160	84
69	COL<88>	4260	84
70	COL<87>	4360	84
71	COL<86>	4460	84
72	COL<85>	4560	84
73	COL<84>	4660	84
74	COL<83>	4760	84
75	COL<82>	4860	84
76	COL<81>	4960	84
77	COL<80>	5060	84
78	COL<79>	5306	84
79	COL<78>	5406	84
80	COL<77>	5506	84

Pad	Pad name	X	Y
81	COL<76>	5606	84
82	COL<75>	5706	84
83	COL<74>	5806	84
84	COL<73>	5906	84
85	COL<72>	6006	84
86	COL<71>	6106	84
87	COL<70>	6206	84
88	COL<69>	6306	84
89	COL<68>	6406	84
90	COL<67>	6506	84
91	COL<66>	6606	84
92	COL<65>	6706	84
93	COL<64>	6806	84
94	COL<63>	7052	84
95	COL<62>	7152	84
96	COL<61>	7252	84
97	COL<60>	7352	84
98	COL<59>	7452	84
99	COL<58>	7552	84
100	COL<57>	7652	84
101	COL<56>	7752	84
102	COL<55>	7852	84
103	COL<54>	7952	84
104	COL<53>	8052	84
105	COL<52>	8152	84
106	COL<51>	8252	84
107	COL<50>	8352	84
108	COL<49>	8452	84
109	COL<48>	8552	84
110	COL<47>	8798	84
111	COL<46>	8898	84
112	COL<45>	8998	84
113	COL<44>	9098	84
114	COL<43>	9198	84
115	COL<42>	9298	84
116	COL<41>	9398	84
117	COL<40>	9498	84
118	COL<39>	9598	84
119	COL<38>	9698	84
120	COL<37>	9798	84

Pad	Pad name	X	Y
121	COL<36>	9898	84
122	COL<35>	9998	84
123	COL<34>	10098	84
124	COL<33>	10198	84
125	COL<32>	10298	84
126	COL<31>	10544	84
127	COL<30>	10644	84
128	COL<29>	10744	84
129	COL<28>	10844	84
130	COL<27>	10944	84
131	COL<26>	11044	84
132	COL<25>	11144	84
133	COL<24>	11244	84
134	COL<23>	11344	84
135	COL<22>	11444	84
136	COL<21>	11544	84
137	COL<20>	11644	84
138	COL<19>	11744	84
139	COL<18>	11844	84
140	COL<17>	11944	84
141	COL<16>	12044	84
142	COL<15>	12290	84
143	COL<14>	12390	84
144	COL<13>	12490	84
145	COL<12>	12590	84
146	COL<11>	12690	84
147	COL<10>	12790	84
148	COL<9>	12890	84
149	COL<8>	12990	84
150	COL<7>	13090	84
151	COL<6>	13190	84
152	COL<5>	13290	84
153	COL<4>	13390	84
154	COL<3>	13490	84
155	COL<2>	13590	84
156	COL<1>	13690	84
157	COL<0>	13790	84
158	ROW<33>	14204	84
159	ROW<35>	14304	84
160	ROW<37>	14404	84

Pad	Pad name	X	Y
161	ROW<39>	14504	84
162	ROW<41>	14604	84
163	ROW<43>	14704	84
164	ROW<45>	14804	84
165	ROW<47>	14904	84
166	ROW<49>	15004	84
167	ROW<51>	15104	84
168	ROW<53>	15204	84
169	ROW<55>	15304	84
170	ROW<57>	15404	84
171	ROW<59>	15504	84
172	ROW<61>	15604	84
173	ROW<63>	15704	84
174	Dummy 7	15804	84
175	Dummy 8	15904	84
176	Dummy 9	16004	84
177	Dummy 12	15961	2437
178	Dummy 11	15861	2437
179	Dummy 10	15761	2437
180	ROW<31>	15661	2437
181	ROW<29>	15561	2437
182	ROW<27>	15461	2437
183	ROW<25>	15361	2437
184	ROW<23>	15261	2437
185	ROW<21>	15161	2437
186	ROW<19>	15061	2437
187	ROW<17>	14961	2437
188	ROW<15>	14861	2437
189	ROW<13>	14761	2437
190	ROW<11>	14661	2437
191	ROW<9>	14561	2437
192	ROW<7>	14461	2437
193	ROW<5>	14361	2437
194	ROW<3>	14261	2437
195	ROW<1>	14161	2437
196	OSC	13738	2462
197	VDD1	13147	2461
198	VDD1	13047	2461
199	VDD1	12947	2461
200	VDD2	12145	2461

Pad	Pad name	X	Y
201	VDD2_HV_IN	11145	2461
202	VDD2_HV_IN	11045	2461
203	VDD2_HV_IN	10945	2461
204	RES_B_IN	10627	2462
205	SDA_OUT	10333.55	2462
206	SDA_IN	9412.4	2462
207	SDA_IN	9212.4	2462
208	SCL_IN	8256.8	2462
209	SCL_IN	8056.8	2462
	Recpat C1	16275	2437
	Recpat C2	2301	80
	Recpat F	304	1824

Universal LCD driver for small graphic panels

PCF8558

FEATURES

- Single chip LCD controller/driver
- 40 row and 101 column outputs
- Display data RAM
  40 × 101 bits = 505 bytes = 4040 bits
- On-chip:
  - Generation of intermediate LCD bias voltages
  - Oscillator requires no external components (external clock also possible)
- 400 kHz fast I²C-bus interface
- CMOS compatible
- MUX rate 1 : 40
- Logic supply voltage range $V_{DD} - V_{SS}$ = 2.5 to 6 V
- Display supply voltage range $V_{DD} - V_{LCD}$ = 3.5 to 9 V
- Low power consumption, suitable for battery operated systems.

APPLICATIONS

- Telecom equipment
- Portable instruments
- Point of sale terminals
- Alarm systems.

GENERAL DESCRIPTION

The PCF8558 is a low power CMOS LCD controller driver, designed to drive a graphic display of 40 rows and 101 columns. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD bias voltages, resulting in a minimum of external components and lower power consumption.

The PCF8558 interfaces to most microcontrollers via a I²C-bus interface.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8558U/10	–	chip on FFC	–
PCF8558U/12	–	chip with bumps on FFC	–

Full Data Sheet: on CD-ROM/WWW (Internet) or FOD-system (details in front Section/back of this HB), or updated Loose leaf or Parent HB

BLOCK DIAGRAM

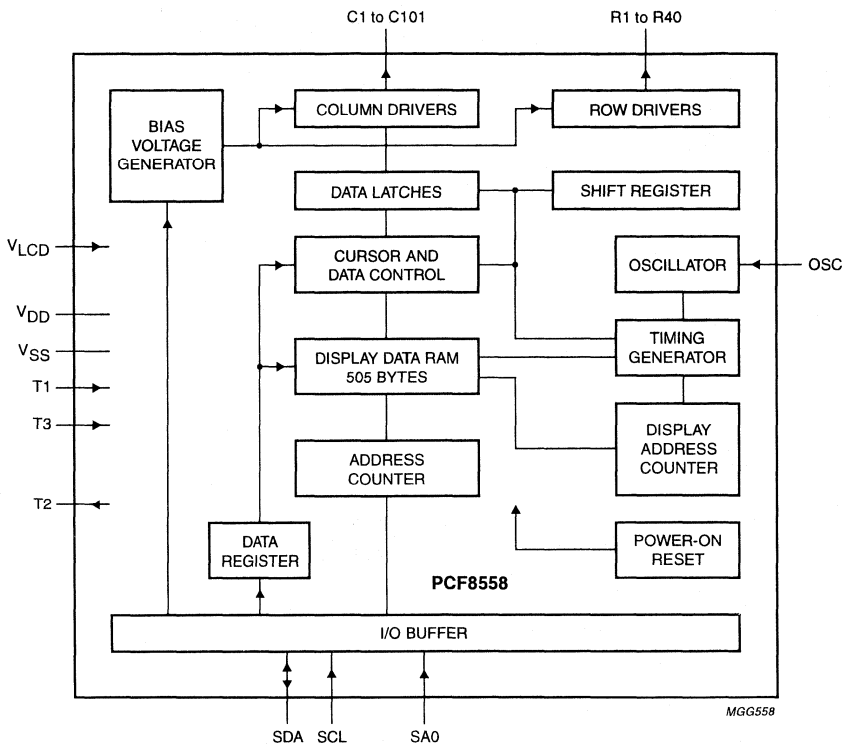


Fig.1 Block diagram.

PINNING

SYMBOL	PAD	DESCRIPTION
SCL	1	I^2C-bus serial clock input
R20 to R1	2 to 21	LCD row driver data outputs
C101 to C1	22 to 122	LCD column driver data outputs
R21 to R40	123 to 142	LCD row driver data outputs
T2	143	test pad output, must be left unconnected (not user accessible)
SDA	144	I^2C-bus serial data input/output
V_{SS}	145	ground
T1	146	test pad input, must be connected to V_{SS} (not user accessible)
V_{LCD}	147	negative supply voltage input for the LCD
SA0	148	the LSB bit of the I^2C-bus slave address input is set by connecting this pin to either 0 (V_{SS}) or 1 (V_{DD})
T3	149	test pad input, must be connected to V_{DD} (not user accessible)
OSC	150	when the on-chip oscillator is used this pin must be connected to V_{DD}; an external clock signal, if used, is input at this pin
V_{DD}	151	positive supply voltage

Universal LCD driver for low multiplex rates

PCF8566

FEATURES

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2, 3 or 4 backplane multiplexing
- Selectable display bias configuration: static, ½ or ⅓
- Internal LCD bias generation with voltage-follower buffers
- 24 segment drives: up to twelve 8-segment numeric characters; up to six 15-segment alphanumeric characters; or any graphics of up to 96 elements
- 24 × 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- 2.5 to 6 V power supply range
- Low power consumption
- Power saving mode for extremely low power consumption in battery-operated and telephone applications
- I²C-bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 1536 segments possible)
- Cascadable with the 40 segment LCD driver PCF8576C
- Optimized pinning for single plane wiring in both single and multiple PCF8566 applications
- Space-saving 40 lead plastic very small outline package (VSO40; SOT158-1)
- No external components required (even in multiple device applications)
- Manufactured in silicon gate CMOS process.

GENERAL DESCRIPTION

The PCF8566 is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD) having low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 24 segments and can easily be cascaded for larger LCD applications. The PCF8566 is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional I²C-bus. Communication overheads are minimized by a display RAgmM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8566P	DIP40	plastic dual in-line package; 40 leads (600 mil)	SOT129-1
PCF8566T	VSO40	plastic very small outline package; 40 leads	SOT158-1

Full Data Sheet: on CD-ROM/WWW (Internet) or FOD-system (details in front Section/back of this HB), or updated Loose leaf or Parent HB

BLOCK DIAGRAM

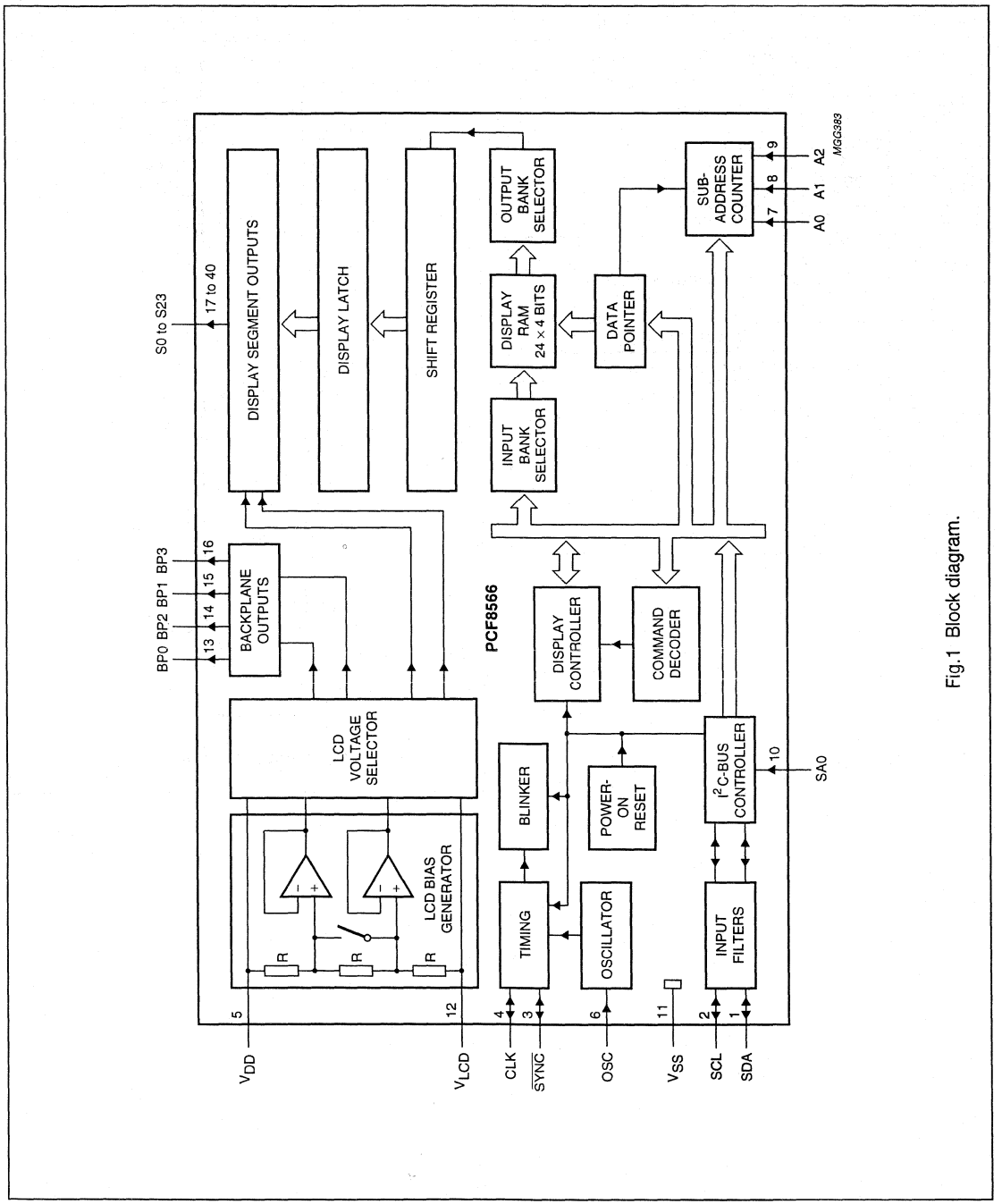


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SDA	1	I²C-bus data input/output
SCL	2	I²C-bus clock input/output
$\overline{SYNC}$	3	cascade synchronization input/output
CLK	4	external clock input/output
V_{DD}	5	positive supply voltage
OSC	6	oscillator input
A0	7	I²C-bus subaddress inputs
A1	8	
A2	9	
SA0	10	I²C-bus slave address bit 0 input
V_{SS}	11	logic ground
V_{LCD}	12	LCD supply voltage
BP0	13	LCD backplane outputs
BP2	14	
BP1	15	
BP3	16	
S0 to S23	17 to 40	LCD segment outputs

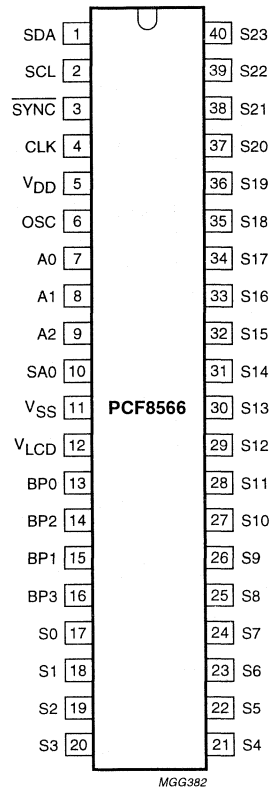


Fig.2 Pin configuration.

Universal LCD driver for low multiplex rates

PCF8576

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Universal LCD driver for low multiplex rates

PCF8576

1 FEATURES

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
- Selectable display bias configuration: static, ½ or ⅓
- Internal LCD bias generation with voltage-follower buffers
- 40 segment drives: up to twenty 8-segment numeric characters; up to ten 15-segment alphanumeric characters; or any graphics of up to 160 elements
- 40 × 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- Wide power supply range: from 2 V for low-threshold LCDs and up to 6 V for guest-host LCDs and high-threshold (automobile) twisted nematic LCDs
- Low power consumption
- Power-saving mode for extremely low power consumption in battery-operated and telephone applications
- I²C-bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 2560 segments possible)
- Cascadable with 24-segment LCD driver PCF8566
- Optimized pinning for plane wiring in both single and multiple PCF8576 applications
- Space-saving 56-lead plastic very small outline package (VSO56)
- Very low external component count (at most one resistor, even in multiple device applications)
- Compatible with chip-on-glass technology
- Manufactured in silicon gate CMOS process.

2 GENERAL DESCRIPTION

The PCF8576 is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD) with low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 40 segments and can easily be cascaded for larger LCD applications. The PCF8576 is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional I²C-bus. Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8576T	VSO56	plastic very small outline package; 56 leads	SOT190-1
PCF8576U	–	chip in tray	–
PCF8576U/2	–	chip with bumps in tray	–
PCF8576U/5	–	unsawn wafer	–
PCF8576U/7	–	chip with bumps on tape	–
PCF8576U/10	FFC	chip on film frame carrier (FFC)	–
PCF8576U/12	FFC	chip with bumps on film frame carrier (FFC)	–

4 BLOCK DIAGRAM

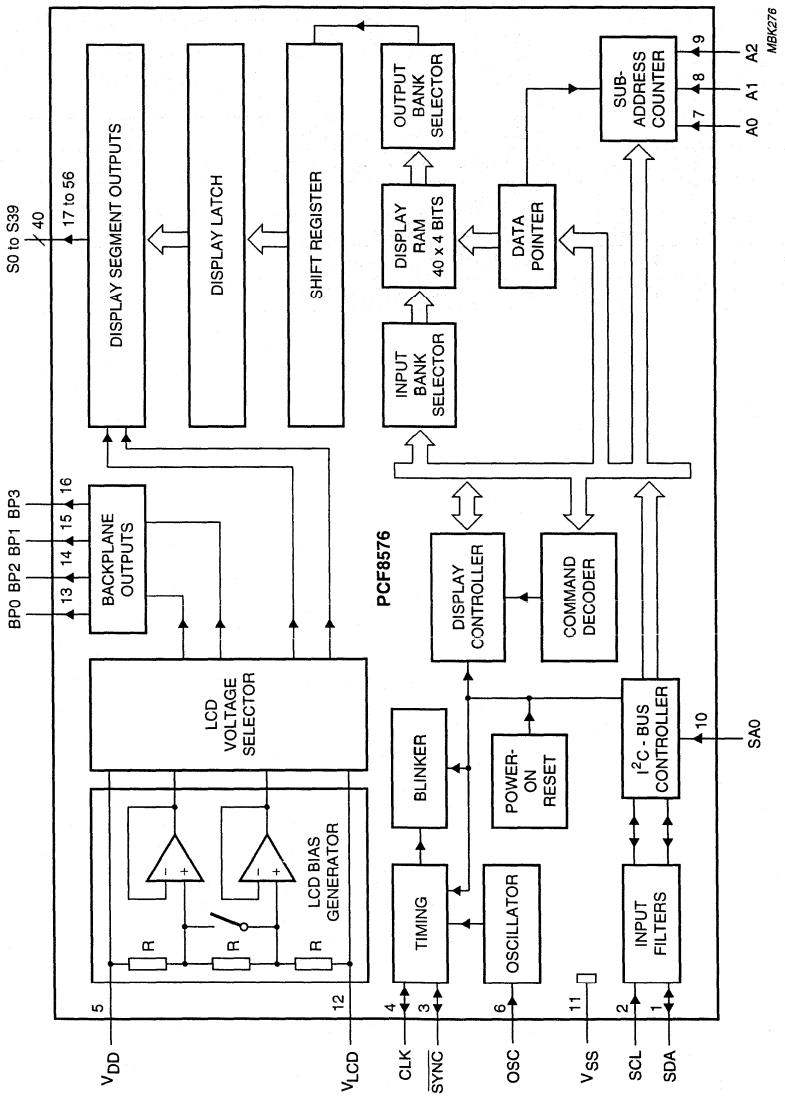


Fig.1 Block diagram (for VSO56 package; SOT190-1).

5 PINNING

SYMBOL	PIN	DESCRIPTION
SDA	1	I²C-bus serial data input/output
SCL	2	I²C-bus serial clock input
$\overline{SYNC}$	3	cascade synchronization input/output
CLK	4	external clock input/output
V_{DD}	5	supply voltage
OSC	6	oscillator input
A0 to A2	7 to 9	I²C-bus subaddress inputs
SA0	10	I²C-bus slave address input; bit 0
V_{SS}	11	logic ground
V_{LCD}	12	LCD supply voltage
BP0, BP2, BP1 and BP3	13 to 16	LCD backplane outputs
S0 to S39	17 to 56	LCD segment outputs

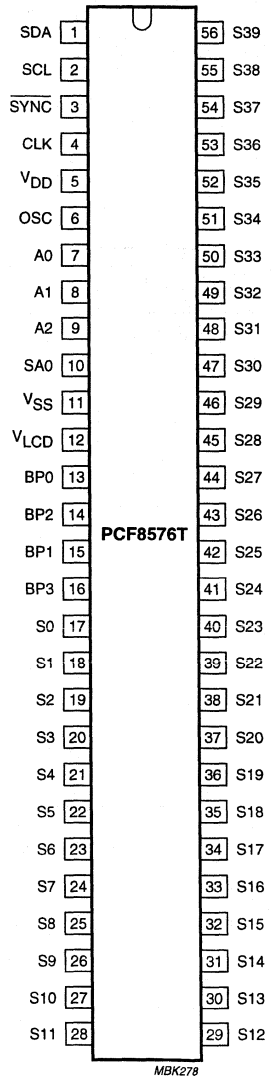


Fig.2 Pin configuration; SOT190-1.

6 FUNCTIONAL DESCRIPTION

The PCF8576 is a versatile peripheral device designed to interface to any microprocessor/microcontroller to a wide variety of LCDs. It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 40 segments. The display configurations possible with the PCF8576 depend on the number of active backplane outputs required; a selection of display configurations is given in Table 1.

All of the display configurations given in Table 1 can be implemented in the typical system shown in Fig.3.

The host microprocessor/microcontroller maintains the 2-line I^2C-bus communication channel with the PCF8576. The internal oscillator is selected by connecting pin OSC to pin V_{SS}. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are to the power supplies (V_{DD}, V_{SS} and V_{LCD}) and the LCD panel chosen for the application.

Table 1 Selection of display configurations

NUMBER OF		7-SEGMENTS NUMERIC		14-SEGMENTS ALPHANUMERIC		DOT MATRIX
BACKPLANES	SEGMENTS	DIGITS	INDICATOR SYMBOLS	CHARACTERS	INDICATOR SYMBOLS	
4	160	20	20	10	20	160 dots (4 × 40)
3	120	15	15	8	8	120 dots (3 × 40)
2	80	10	10	5	10	80 dots (2 × 40)
1	40	5	5	2	12	40 dots (1 × 40)

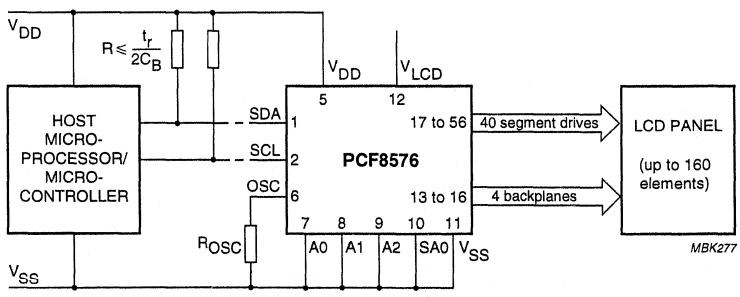


Fig.3 Typical system configuration.

6.1 Power-on reset

At power-on the PCF8576 resets to a starting condition as follows:

1. All backplane outputs are set to V_{DD}.
2. All segment outputs are set to V_{DD}.
3. The drive mode '1 : 4 multiplex with ⅓bias' is selected.
4. Blinking is switched off.
5. Input and output bank selectors are reset (as defined in Table 5).
6. The I²C-bus interface is initialized.
7. The data pointer and the subaddress counter are cleared.

Data transfers on the I²C-bus should be avoided for 1 ms following power-on to allow completion of the reset action.

6.2 LCD bias generator

The full-scale LCD voltage (V_{op}) is obtained from $V_{DD} - V_{LCD}$. The LCD voltage may be temperature compensated externally through the V_{LCD} supply to pin 12. Fractional LCD biasing voltages are obtained from an internal voltage divider of the three series resistors connected between V_{DD} and V_{LCD}. The centre resistor can be switched out of the circuit to provide a ½bias voltage level for the 1 : 2 multiplex configuration.

6.3 LCD voltage selector

The LCD voltage selector co-ordinates the multiplexing of the LCD in accordance with the selected LCD drive configuration. The operation of the voltage selector is controlled by MODE SET commands from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of $V_{op} = V_{DD} - V_{LCD}$ and the resulting discrimination ratios (D), are given in Table 2.

A practical value for V_{op} is determined by equating $V_{off(rms)}$ with a defined LCD threshold voltage (V_{th}), typically when the LCD exhibits approximately 10% contrast. In the static drive mode a suitable choice is $V_{op} > 3V_{th}$ approximately.

Multiplex drive ratios of 1 : 3 and 1 : 4 with ½bias are possible but the discrimination and hence the contrast ratios are smaller ($\sqrt{3} = 1.732$ for 1 : 3 multiplex or $\frac{\sqrt{21}}{3} = 1.528$ for 1 : 4 multiplex).

The advantage of these modes is a reduction of the LCD full-scale voltage V_{op} as follows:

- 1 : 3 multiplex (½bias):

  $V_{op} = \sqrt{6} \times V_{off(rms)} = 2.449\ V_{off(rms)}$

- 1 : 4 multiplex (½bias):

  $V_{op} = \left[\frac{(4 \times \sqrt{3})}{3}\right] = 2.309\ V_{off(rms)}$

These compare with $V_{op} = 3\ V_{off(rms)}$ when ⅓bias is used.

Table 2 Preferred LCD drive modes: summary of characteristics

LCD DRIVE MODE	NUMBER OF		LCD BIAS CONFIGURATION	$\frac{V_{off(rms)}}{V_{op}}$	$\frac{V_{on(rms)}}{V_{op}}$	$D = \frac{V_{on(rms)}}{V_{off(rms)}}$
	BACKPLANES	LEVELS				
static	1	2	static	0	1	∞
1 : 2	2	3	½	0.354	0.791	2.236
1 : 2	2	4	⅓	0.333	0.745	2.236
1 : 3	3	4	⅓	0.333	0.638	1.915
1 : 4	4	4	⅓	0.333	0.577	1.732

6.4 LCD drive mode waveforms

6.4.1 STATIC DRIVE MODE

The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and segment drive waveforms for this mode are shown in Fig.4.

6.4.2 1 : 2 MULTIPLEX DRIVE MODE

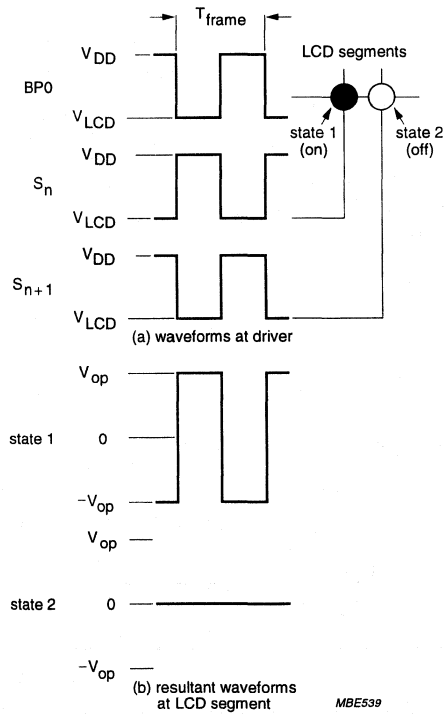
When two backplanes are provided in the LCD, the 1 : 2 multiplex mode applies. The PCF8576 allows use of ½bias or ⅓bias in this mode as shown in Figs 5 and 6.

6.4.3 1 : 3 MULTIPLEX DRIVE MODE

When three backplanes are provided in the LCD, the 1 : 3 multiplex drive mode applies, as shown in Fig.7.

6.4.4 1 : 4 MULTIPLEX DRIVE MODE

When four backplanes are provided in the LCD, the 1 : 4 multiplex drive mode applies, as shown in Fig.8.



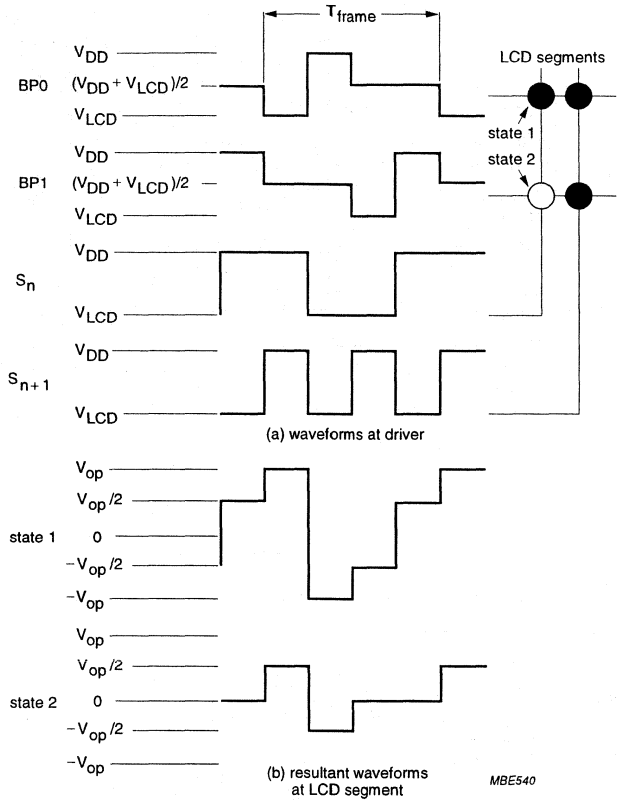
$V_{state1}(t) = V_{S_n}(t) - V_{BP0}(t)$

$V_{on(rms)} = V_{op}$

$V_{state2}(t) = V_{S_{n+1}}(t) - V_{BP0}(t)$

$V_{off(rms)} = 0\ V$

Fig.4 Static drive mode waveforms ($V_{op} = V_{DD} - V_{LCD}$).



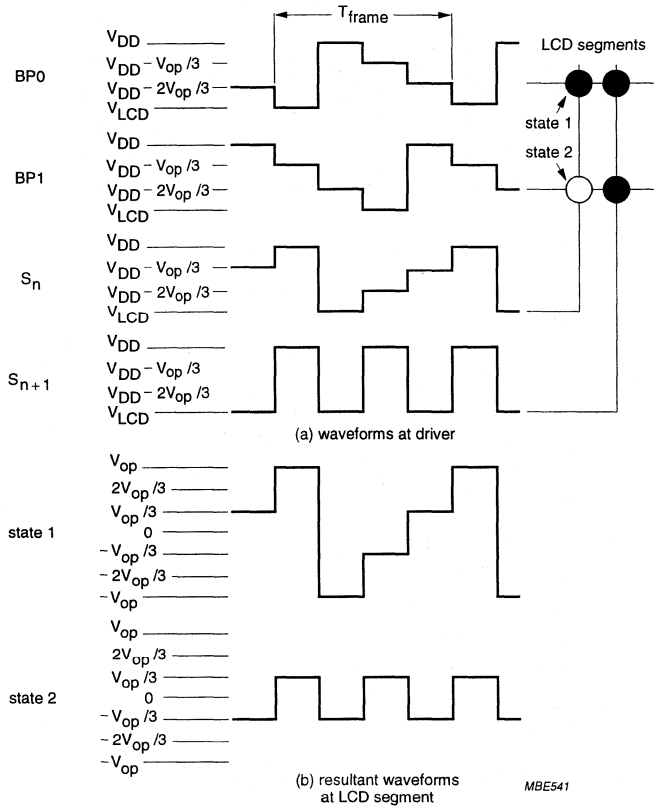
$V_{state1}(t) = V_{S_n}(t) - V_{BP0}(t)$

$V_{on(rms)} = 0.791V_{op}$

$V_{state2}(t) = V_{S_n}(t) - V_{BP1}(t)$

$V_{off(rms)} = 0.354V_{op}$

Fig.5 Waveforms for the 1 : 2 multiplex drive mode with ½bias ($V_{op} = V_{DD} - V_{LCD}$).



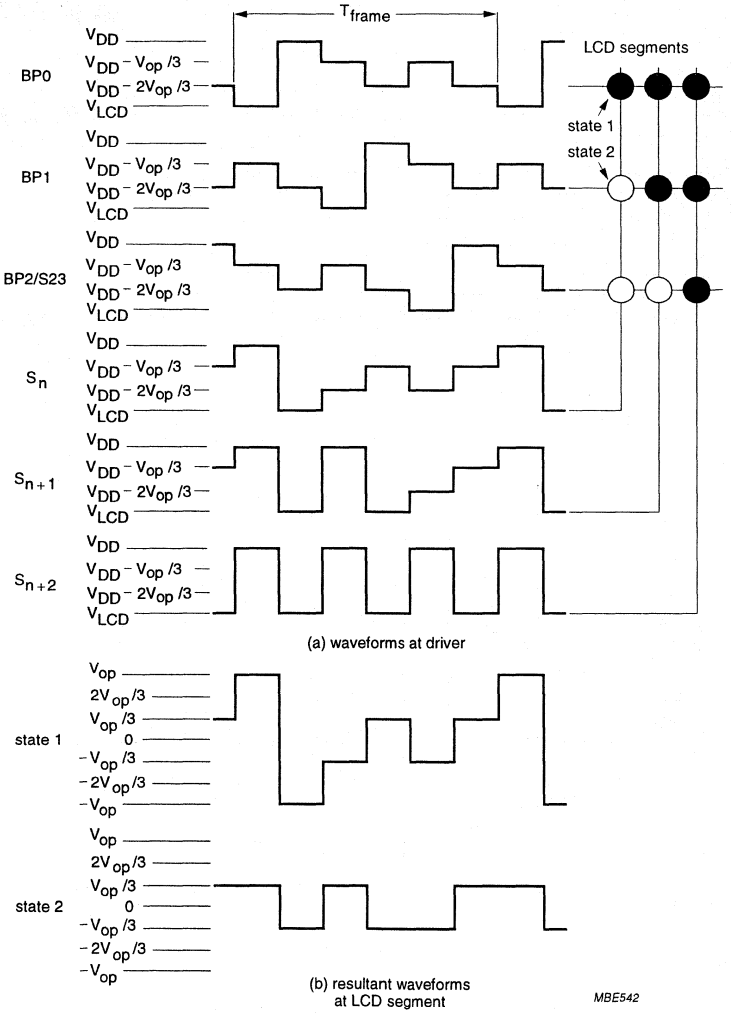
$V_{state1}(t) = V_{S_n}(t) - V_{BP0}(t)$

$V_{on(rms)} = 0.745V_{op}$

$V_{state2}(t) = V_{S_n}(t) - V_{BP1}(t)$

$V_{off(rms)} = 0.333V_{op}$

Fig.6 Waveforms for the 1 : 2 multiplex drive mode with ⅓bias ($V_{op} = V_{DD} - V_{LCD}$).



$V_{state1}(t) = V_{S_n}(t) - V_{BP0}(t)$

$V_{on(rms)} = 0.638V_{op}$

$V_{state2}(t) = V_{S_n}(t) - V_{BP1}(t)$

$V_{off(rms)} = 0.333V_{op}$

Fig.7 Waveforms for the 1 : 3 multiplex drive mode ($V_{op} = V_{DD} - V_{LCD}$).

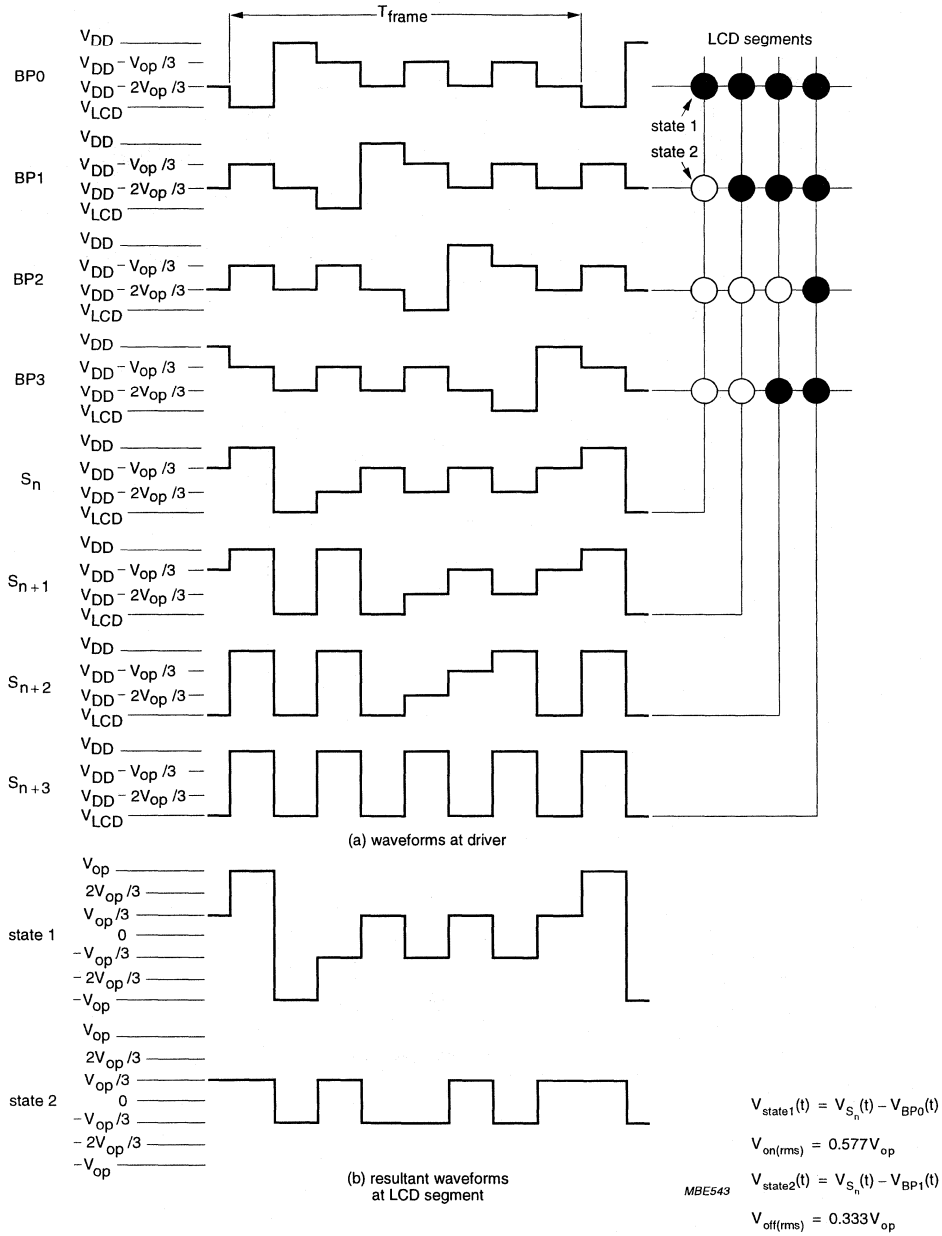


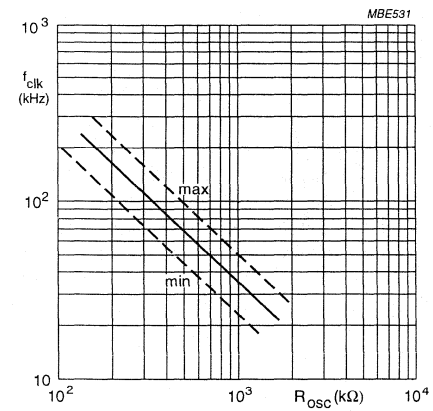
Fig.8 Waveforms for the 1 : 4 multiplex drive mode ($V_{op} = V_{DD} - V_{LCD}$).

6.5 Oscillator

6.5.1 INTERNAL CLOCK

The internal logic and the LCD drive signals of the PCF8576 are timed either by the internal oscillator or from an external clock. When the internal oscillator is used, pin OSC should be connected to pin V_{SS}. In this event, the output from pin CLK provides the clock signal for cascaded PCF8566s in the system.

Where resistor R_{osc} to V_{SS} is present, the internal oscillator is selected. The relationship between the oscillator frequency on pin CLK (f_{clk}) and R_{osc} is shown in Fig.9.



$$f_{clk} \approx \left(\frac{3.4 \times 10^7}{R_{osc}}\right) (kHz)$$

Fig.9 Oscillator frequency as a function of R_{osc}.

6.5.2 EXTERNAL CLOCK

The condition for external clock is made by connecting pin OSC to pin V_{DD}; pin CLK then becomes the external clock input.

The clock frequency (f_{clk}) determines the LCD frame frequency and the maximum rate for data reception from the I²C-bus. To allow I²C-bus transmissions at their maximum data rate of 100 kHz, f_{clk} should be chosen to be above 125 kHz.

A clock signal must always be supplied to the device; removing the clock may freeze the LCD in a DC state.

6.6 Timing

The timing of the PCF8576 organizes the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the synchronization signal $\overline{SYNC}$ maintains the correct timing relationship between the PCF8576s in the system. The timing also generates the LCD frame frequency which it derives as an integer multiple of the clock frequency (see Table 3). The frame frequency is set by the MODE SET commands when internal clock is used, or by the frequency applied to pin CLK when external clock is used.

The ratio between the clock frequency and the LCD frame frequency depends on the mode in which the device is operating. In the power-saving mode the reduction ratio is six times smaller; this allows the clock frequency to be reduced by a factor of six. The reduced clock frequency results in a significant reduction in power dissipation. The lower clock frequency has the disadvantage of increasing the response time when large amounts of display data are transmitted on the I²C-bus.

When a device is unable to digest a display data byte before the next one arrives, it holds the SCL line LOW until the first display data byte is stored. This slows down the transmission rate of the I²C-bus but no data loss occurs.

Table 3 LCD frame frequencies

PCF8576 MODE	FRAME FREQUENCY	NOMINAL FRAME FREQUENCY (Hz)
Normal mode	$\frac{f_{clk}}{2880}$	64
Power-saving mode	$\frac{f_{clk}}{480}$	64

6.7 Display latch

The display latch holds the display data while the corresponding multiplex signals are generated. There is a one-to-one relationship between the data in the display latch, the LCD segment outputs and one column of the display RAM.

6.8 Shift register

The shift register serves to transfer display information from the display RAM to the display latch while previous data is displayed.

6.9 Segment outputs

The LCD drive section includes 40 segment outputs pins S0 to S39 which should be connected directly to the LCD. The segment output signals are generated in accordance with the multiplexed backplane signals and with data resident in the display latch. When less than 40 segment outputs are required the unused segment outputs should be left open-circuit.

6.10 Backplane outputs

The LCD drive section includes four backplane outputs BP0 to BP3 which should be connected directly to the LCD. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than four backplane outputs are required the unused outputs can be left open-circuit. In the 1 : 3 multiplex drive mode BP3 carries the same signal as BP1, therefore these two adjacent outputs can be connected together to give enhanced drive capabilities. In the 1 : 2 multiplex drive mode BP0 and BP2, BP1 and BP3 respectively carry the same signals and may also be paired to increase the drive capabilities. In the static drive mode the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

6.11 Display RAM

The display RAM is a static 40 × 4-bit RAM which stores LCD data. A logic 1 in the RAM bit-map indicates the on state of the corresponding LCD segment; similarly, a logic 0 indicates the off state. There is a one-to-one correspondence between the RAM addresses and the segment outputs, and between the individual bits of a RAM word and the backplane outputs. The first RAM column corresponds to the 40 segments operated with respect to backplane BP0 (see Fig.10). In multiplexed LCD applications the segment data of the second, third and fourth column of the display RAM are time-multiplexed with BP1, BP2 and BP3 respectively.

When display data is transmitted to the PCF8576 the display bytes received are stored in the display RAM in accordance with the selected LCD drive mode.
To illustrate the filling order, an example of a 7-segment numeric display showing all drive modes is given in Fig.11; the RAM filling organization depicted applies equally to other LCD types.

With reference to Fig.11, in the static drive mode the eight transmitted data bits are placed in bit 0 of eight successive display RAM addresses. In the 1 : 2 multiplex drive mode the eight transmitted data bits are placed in bits 0 and 1 of four successive display RAM addresses. In the 1 : 3 multiplex drive mode these bits are placed in bits 0, 1 and 2 of three successive addresses, with bit 2 of the third address left unchanged. This last bit may, if necessary, be controlled by an additional transfer to this address but care should be taken to avoid overriding adjacent data because full bytes are always transmitted. In the 1 : 4 multiplex drive mode the eight transmitted data bits are placed in bits 0, 1, 2 and 3 of two successive display RAM addresses.

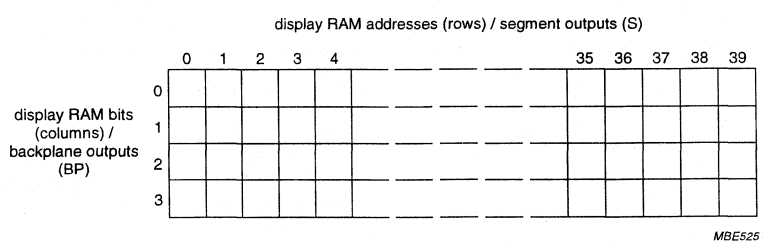


Fig.10 Display RAM bit-map showing direct relationship between display RAM addresses and segment outputs, and between bits in a RAM word and backplane outputs.

6.12 Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the LOAD DATA POINTER command. Following this, an arriving data byte is stored starting at the display RAM address indicated by the data pointer thereby observing the filling order shown in Fig.11. The data pointer is automatically incremented in accordance with the chosen LCD configuration. That is, after each byte is stored, the contents of the data pointer are incremented by eight (static drive mode), by four (1 : 2 multiplex drive mode) or by two (1 : 4 multiplex drive mode).

6.13 Subaddress counter

The storage of display data is conditioned by the contents of the subaddress counter. Storage is allowed to take place only when the contents of the subaddress counter agree with the hardware subaddress applied to A0, A1 and A2. The subaddress counter value is defined by the DEVICE SELECT command. If the contents of the subaddress counter and the hardware subaddress do not agree then data storage is inhibited but the data pointer is incremented as if data storage had taken place.
The subaddress counter is also incremented when the data pointer overflows.

The storage arrangements described lead to extremely efficient data loading in cascaded applications. When a series of display bytes are sent to the display RAM, automatic wrap-over to the next PCF8576 occurs when the last RAM address is exceeded. Subaddressing across device boundaries is successful even if the change to the next device in the cascade occurs within a transmitted character (such as during the 14th display data byte transmitted in 1 : 3 multiplex mode).

6.14 Output bank selector

This selects one of the four bits per display RAM address for transfer to the display latch. The actual bit chosen depends on the particular LCD drive mode in operation and on the instant in the multiplex sequence. In 1 : 4 multiplex, all RAM addresses of bit 0 are the first to be selected, these are followed by the contents of bit 1, bit 2 and then bit 3. Similarly in 1 : 3 multiplex, bits 0, 1 and 2 are selected sequentially. In 1 : 2 multiplex, bits 0 and 1 are selected and, in the static mode, bit 0 is selected.

The PCF8576 includes a RAM bank switching feature in the static and 1 : 2 multiplex drive modes. In the static drive mode, the BANK SELECT command may request the contents of bit 2 to be selected for display instead of bit 0 contents. In the 1 : 2 drive mode, the contents of bits 2 and 3 may be selected instead of bits 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

6.15 Input bank selector

The input bank selector loads display data into the display RAM in accordance with the selected LCD drive configuration. Display data can be loaded in bit 2 in static drive mode or in bits 2 and 3 in 1 : 2 drive mode by using the BANK SELECT command. The input bank selector functions independent of the output bank selector.

6.16 Blinker

The display blinking capabilities of the PCF8576 are very versatile. The whole display can be blinked at frequencies selected by the BLINK command. The blinking frequencies are integer multiples of the clock frequency; the ratios between the clock and blinking frequencies depend on the mode in which the device is operating, as shown in Table 4.

An additional feature is for an arbitrary selection of LCD segments to be blinked. This applies to the static and 1 : 2 LCD drive modes and can be implemented without any communication overheads. By means of the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blinking frequency. This mode can also be specified by the BLINK command.

In the 1 : 3 and 1 : 4 multiplex modes, where no alternate RAM bank is available, groups of LCD segments can be blinked by selectively changing the display RAM data at fixed time intervals.

If the entire display is to be blinked at a frequency other than the nominal blinking frequency, this can be effectively performed by resetting and setting the display enable bit E at the required rate using the MODE SET command.

Table 4 Blinking frequencies

BLINKING MODE	NORMAL OPERATING MODE RATIO	POWER-SAVING MODE RATIO	NOMINAL BLINKING FREQUENCY
Off	–	–	blinking off
2 Hz	$\frac{f_{clk}}{92160}$	$\frac{f_{clk}}{15360}$	2 Hz
1 Hz	$\frac{f_{clk}}{184320}$	$\frac{f_{clk}}{30720}$	1 Hz
0.5 Hz	$\frac{f_{clk}}{368640}$	$\frac{f_{clk}}{61440}$	0.5 Hz

x = data bit unchanged.

Fig.11 Relationships between LCD layout, drive mode, display RAM filling order and display data transmitted over the I²C-bus.

7 CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

7.1 Bit transfer (see Fig.12)

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

7.2 START and STOP conditions (see Fig.13)

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P).

7.3 System configuration (see Fig.14)

A device generating a message is a 'transmitter', a device receiving a message is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves'.

7.4 Acknowledge (see Fig.15)

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

7.5 PCF8576 I²C-bus controller

The PCF8576 acts as an I²C-bus slave receiver. It does not initiate I²C-bus transfers or transmit data to an I²C-bus master receiver. The only data output from the PCF8576 are the acknowledge signals of the selected devices. Device selection depends on the I²C-bus slave address, on the transferred command data and on the hardware subaddress.

In single device application, the hardware subaddress inputs A0, A1 and A2 are normally connected to V_{SS} which defines the hardware subaddress 0. In multiple device applications A0, A1 and A2 are connected to V_{SS} or V_{DD} in accordance with a binary coding scheme such that no two devices with a common I²C-bus slave address have the same hardware subaddress.

In the power-saving mode it is possible that the PCF8576 is not able to keep up with the highest transmission rates when large amounts of display data are transmitted. If this situation occurs, the PCF8576 forces the SCL line to LOW until its internal operations are completed. This is known as the 'clock synchronization feature' of the I²C-bus and serves to slow down fast transmitters. Data loss does not occur.

7.6 Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

7.7 I²C-bus protocol

Two I²C-bus slave addresses (0111000 and 0111001) are reserved for the PCF8576. The least significant bit of the slave address that a PCF8576 will respond to is defined by the level connected at its input pin SA0. Therefore, two types of PCF8576 can be distinguished on the same I²C-bus which allows:

- Up to 16 PCF8576s on the same I²C-bus for very large LCD applications
- The use of two types of LCD multiplex on the same I²C-bus.

The I²C-bus protocol is shown in Fig.16. The sequence is initiated with a START condition (S) from the I²C-bus master which is followed by one of the two PCF8576 slave addresses available. All PCF8576s with the corresponding SA0 level acknowledge in parallel with the slave address but all PCF8576s with the alternative SA0 level ignore the whole I²C-bus transfer.

After acknowledgement, one or more command bytes (m) follow which define the status of the addressed PCF8576s.

The last command byte is tagged with a cleared most significant bit, the continuation bit C. The command bytes are also acknowledged by all addressed PCF8576s on the bus.

After the last command byte, a series of display data bytes (n) may follow. These display bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated and the data is directed to the intended PCF8576 device. The acknowledgement after each byte is made only by the (A0, A1 and A2) addressed PCF8576. After the last display byte, the I²C-bus master issues a STOP condition (P).

7.8 Command decoder

The command decoder identifies command bytes that arrive on the I²C-bus. All available commands carry a continuation bit C in their most significant bit position (Fig.17). When this bit is set, it indicates that the next byte of the transfer to arrive will also represent a command. If this bit is reset, it indicates the last command byte of the transfer. Further bytes will be regarded as display data.

The five commands available to the PCF8576 are defined in Table 5.

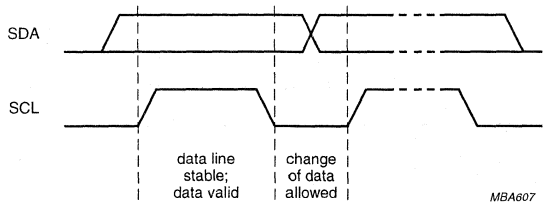


Fig.12 Bit transfer.

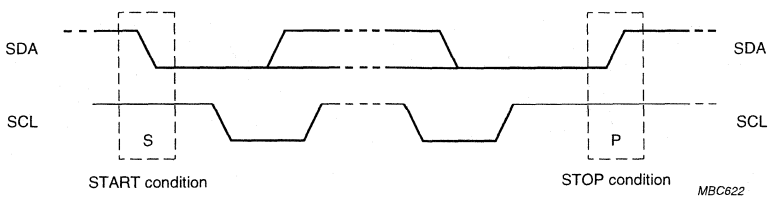


Fig.13 Definition of START and STOP conditions.

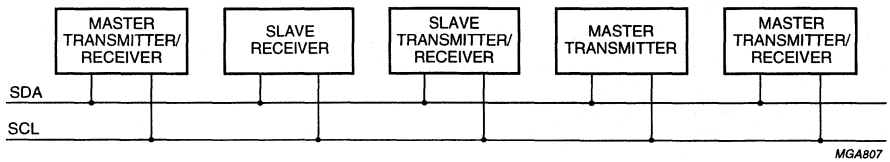


Fig.14 System configuration.

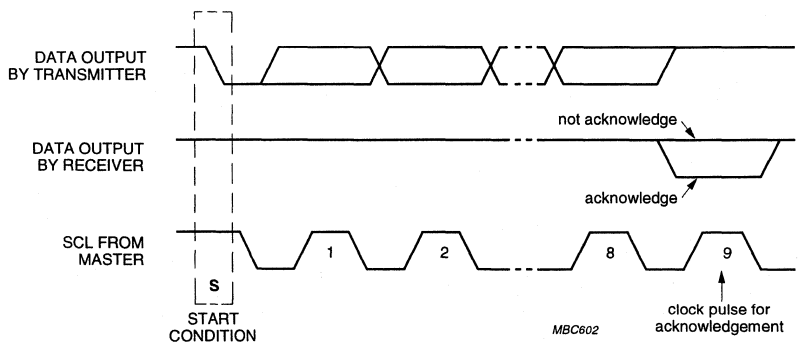


Fig.15 Acknowledgement on the I²C-bus.

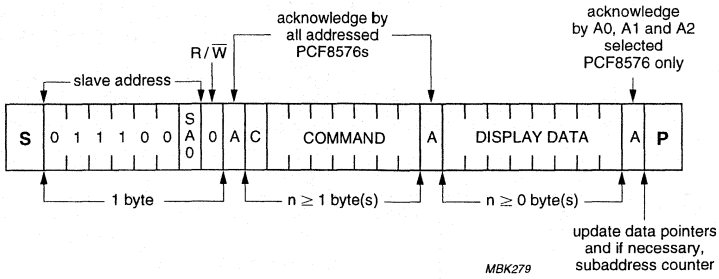
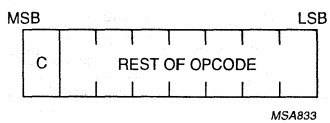


Fig.16 I²C-bus protocol.



C = 0; last command.
C = 1; commands continue.

Fig.17 General format of command byte.

Table 5 Definition of PCF8576 commands

COMMAND	OPCODE	OPTIONS	DESCRIPTION
MODE SET	C 1 0 LP E B M1 M0	Table 6	Defines LCD drive mode.
		Table 7	Defines LCD bias configuration.
		Table 8	Defines display status. The possibility to disable the display allows implementation of blinking under external control.
		Table 9	Defines power dissipation mode.
LOAD DATA POINTER	C 0 P5 P4 P3 P2 P1 P0	Table 10	Six bits of immediate data, bits P5 to P0, are transferred to the data pointer to define one of forty display RAM addresses.
DEVICE SELECT	C 1 1 0 0 A2 A1 A0	Table 11	Three bits of immediate data, bits A2 to A0, are transferred to the subaddress counter to define one of eight hardware subaddresses.
BANK SELECT	C 1 1 1 1 0 I O	Table 12	Defines input bank selection (storage of arriving display data).
		Table 13	Defines output bank selection (retrieval of LCD display data). The BANK SELECT command has no effect in 1 : 3 and 1 : 4 multiplex drive modes.
BLINK	C 1 1 1 0 A BF1 BF0	Table 14	Defines the blinking frequency.
		Table 15	Selects the blinking mode; normal operation with frequency set by BF1, BF0 or blinking by alternation of display RAM banks. Alternation blinking does not apply in 1 : 3 and 1 : 4 multiplex drive modes.

Table 6 MODE SET option 1

LCD DRIVE MODE		BITS	
DRIVE MODE	BACKPLANE	M1	M0
Static	1 BP	0	1
1 : 2	MUX (2 BP)	1	0
1 : 3	MUX (3 BP)	1	1
1 : 4	MUX (4 BP)	0	0

Table 7 MODE SET option 2

LCD BIAS	BIT B
1/3 bias	0
1/2 bias	1

Table 8 MODE SET option 3

DISPLAY STATUS	BIT E
Disabled (blank)	0
Enabled	1

Table 9 MODE SET option 4

MODE	BIT LP
Normal mode	0
Power-saving mode	1

Table 10 LOAD DATA POINTER option 1

DESCRIPTION	BITS					
6-bit binary value of 0 to 39	P5	P4	P3	P2	P1	P0

Table 11 DEVICE SELECT option 1

DESCRIPTION	BITS		
3-bit binary value of 0 to 7	A2	A1	A0

Table 12 BANK SELECT option 1

STATIC	1 : 2 MUX	BIT I
RAM bit 0	RAM bits 0 and 1	0
RAM bit 2	RAM bits 2 and 3	1

Table 13 BANK SELECT option 2

STATIC	1 : 2 MUX	BIT O
RAM bit 0	RAM bits 0 and 1	0
RAM bit 2	RAM bits 2 and 3	1

Table 14 BLINK option 1

BLINK FREQUENCY	BITS	
	BF1	BF0
Off	0	0
2 Hz	0	1
1 Hz	1	0
0.5 Hz	1	1

Table 15 BLINK option 2

BLINK MODE	BIT A
Normal blinking	0
Alternation blinking	1

7.9 Display controller

The display controller executes the commands identified by the command decoder. It contains the status registers of the PCF8576 and co-ordinates their effects.
The controller is also responsible for loading display data into the display RAM as required by the filling order.

7.10 Cascaded operation

In large display configurations, up to 16 PCF8576s can be distinguished on the same I^2C-bus by using the 3-bit hardware subaddress (A0, A1 and A2) and the programmable I^2C-bus slave address (SA0). When cascaded PCF8576s are synchronized so that they can share the backplane signals from one of the devices in the cascade. Such an arrangement is cost-effective in large LCD applications since the backplane outputs of only one device need to be through-plated to the backplane electrodes of the display. The other PCF8576s of the cascade contribute additional segment outputs but their backplane outputs are left open-circuit (see Fig.18).

The $\overline{SYNC}$ line is provided to maintain the correct synchronization between all cascaded PCF8576s. This synchronization is guaranteed after the Power-on reset. The only time that $\overline{SYNC}$ is likely to be needed is if synchronization is accidentally lost (e.g. by noise in adverse electrical environments; or by the definition of a multiplex mode when PCF8576s with differing SA0 levels are cascaded). $\overline{SYNC}$ is organized as an input/output pin; the output selection being realized as an open-drain driver with an internal pull-up resistor. A PCF8576 asserts the $\overline{SYNC}$ line at the onset of its last active backplane signal and monitors the $\overline{SYNC}$ line at all other times. Should synchronization in the cascade be lost, it will be restored by the first PCF8576 to assert $\overline{SYNC}$. The timing relationship between the backplane waveforms and the $\overline{SYNC}$ signal for the various drive modes of the PCF8576 are shown in Fig.19.

For single plane wiring of packaged PCF8576s and chip-on-glass cascading, see Chapter 12.

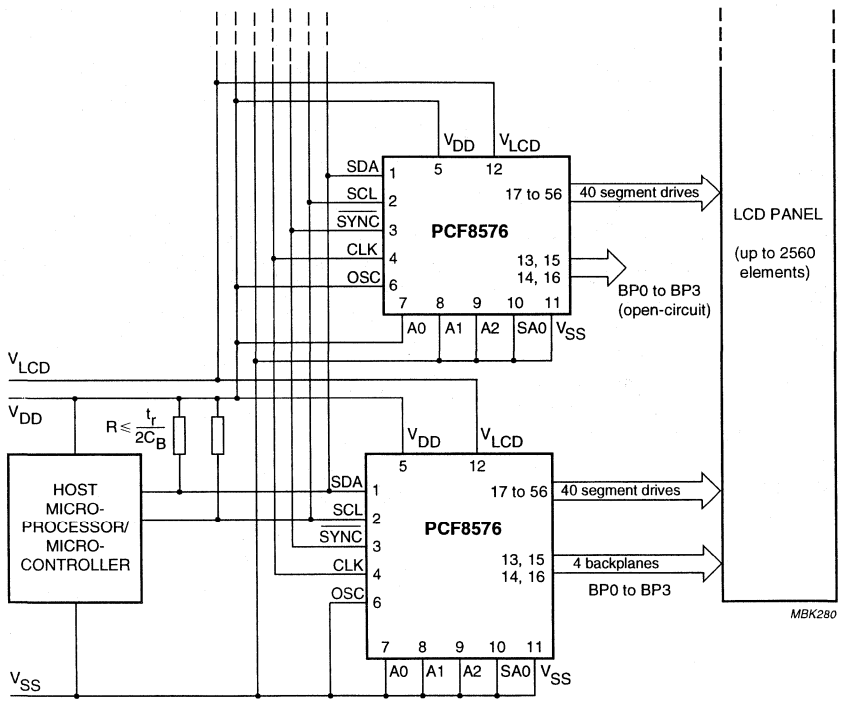
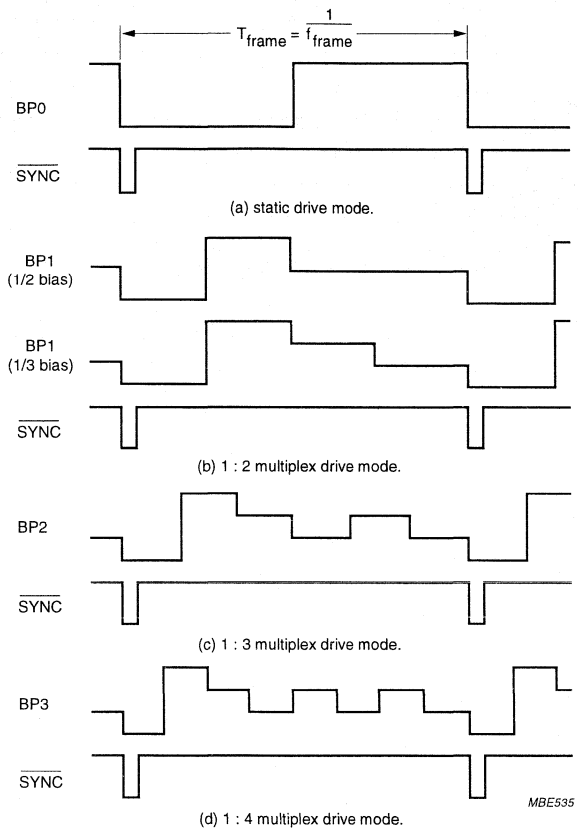


Fig.18 Cascaded PCF8576 configuration.



Excessive capacitive coupling between SCL or CLK and $\overline{SYNC}$ may cause erroneous synchronization. If this proves to be a problem, the capacitance of the $\overline{SYNC}$ line should be increased (e.g. by an external capacitor between $\overline{SYNC}$ and V_{DD}). Degradation of the positive edge of the $\overline{SYNC}$ pulse may be countered by an external pull-up resistor.

Fig.19 Synchronization of the cascade for the various PCF8576 drive modes.

8 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	+11.0	V
V_{LCD}	LCD supply voltage	V_{DD} − 11.0	V_{DD}	V
V_I	input voltage SDA, SCL, CLK, $\overline{SYNC}$, SA0, OSC, A0 to A2	V_{SS} − 0.5	V_{DD} + 0.5	V
V_O	output voltage S0 to S39, BP0 to BP3	V_{LCD} − 0.5	V_{DD} + 0.5	V
I_I	DC input current	−	20	mA
I_O	DC output current	−	25	mA
I_{DD}, I_{SS}, I_{LCD}	V_{DD}, V_{SS} or V_{LCD} current	−	50	mA
P_{tot}	total power dissipation	−	400	mW
P_O	power dissipation per output	−	100	mW
T_{stg}	storage temperature	−65	+150	°C

9 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see *"Handling MOS Devices"*).

10 DC CHARACTERISTICS

V_{DD} = 2 to 9 V; V_{SS} = 0 V; V_{LCD} = V_{DD} − 2 V to V_{DD} − 9 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage		2	–	9	V
V_{LCD}	LCD supply voltage	note 1	V_{DD} − 9	–	V_{DD} − 2	V
I_{DD}	supply current	note 2				
	normal mode	f_{clk} = 200 kHz	–	–	180	µA
	power-saving mode	f_{clk} = 35 kHz; V_{DD} = 3.5 V; V_{LCD} = 0 V; A0, A1 and A2 connected to V_{SS}	–	–	60	µA
Logic						
V_{IL}	LOW-level input voltage		V_{SS}	–	0.3V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7V_{DD}	–	V_{DD}	V
V_{OL}	LOW-level output voltage	I_{OL} = 0 mA	–	–	0.05	V
V_{OH}	HIGH-level output voltage	I_{OH} = 0 mA	V_{DD} − 0.05	–	–	V
I_{OL1}	LOW-level output current CLK, $\overline{SYNC}$	V_{OL} = 1 V; V_{DD} = 5 V	1	–	–	mA
I_{OH1}	HIGH-level output current CLK	V_{OH} = 4 V; V_{DD} = 5 V	1	–	–	mA
I_{OL2}	LOW-level output current SDA and SCL	V_{OL} = 0.4 V; V_{DD} = 5 V	3	–	–	mA
I_{L1}	leakage current SA0, A0 to A2, CLK, SDA and SCL	V_I = V_{DD} or V_{SS}	–	–	1	µA
I_{L2}	leakage current OSC	V_I = V_{DD}	–	–	1	µA
I_{pd}	A0, A1, A2 and OSC pull-down current	V_I = 1 V; V_{DD} = 5 V	20	50	150	µA
R_{SYNC}	pull-up resistor ($\overline{SYNC}$)		20	50	150	kΩ
V_{POR}	Power-on reset voltage level	note 3	–	1.0	1.6	V
C_I	input capacitance	note 4	–	–	7	pF
LCD outputs						
V_{BP}	DC voltage component BP0 to BP3	C_{BP} = 35 nF	–	20	–	mV
V_S	DC voltage component S0 to S39	C_S = 5 nF	–	20	–	mV
R_{BP}	output resistance BP0 to BP3	note 5; V_{LCD} = V_{DD} − 5 V	–	–	5	kΩ
R_S	output resistance S0 to S39	note 5; V_{LCD} = V_{DD} − 5 V	–	–	7.5	kΩ

Notes

1. $V_{LCD} \leq V_{DD} - 3$ V for ⅓bias.
2. LCD outputs are open-circuit; inputs at V_{SS} or V_{DD}; external clock with 50% duty factor; I^2C-bus inactive.
3. Resets all logic when $V_{DD} < V_{POR}$.
4. Periodically sampled, not 100% tested.
5. Outputs measured one at a time.

11 AC CHARACTERISTICS

V_{DD} = 2 to 9 V; V_{SS} = 0 V; V_{LCD} = V_{DD} − 2 V to V_{DD} − 9 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{clk}	oscillator frequency on pin CLK					
	normal mode	V_{DD} = 5 V; note 1	125	200	288	kHz
	power-saving mode	V_{DD} = 3.5 V	21	31	48	kHz
t_{clkH}	CLK HIGH time	see Fig.21	1	–	–	µs
t_{clkL}	CLK LOW time		1	–	–	µs
$t_{P\overline{SYNC}}$	$\overline{SYNC}$ propagation delay time		–	–	400	ns
$t_{\overline{SYNC}L}$	$\overline{SYNC}$ LOW time		1	–	–	µs
t_{PLCD}	driver delays with test loads	V_{LCD} = V_{DD} − 5 V; see Fig.20	–	–	30	µs
Timing characteristics: I²C-bus; note 2; see Fig.22						
t_{SW}	tolerable spike width on bus		–	–	100	ns
t_{BUF}	bus free time		4.7	–	–	µs
$t_{HD;STA}$	START condition hold time		4.0	–	–	µs
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	–	–	µs
t_{LOW}	SCL LOW time		4.7	–	–	µs
t_{HIGH}	SCL HIGH time		4.0	–	–	µs
t_r	SCL and SDA rise time		–	–	1	µs
t_f	SCL and SDA fall time		–	–	0.3	µs
C_B	capacitive bus line load		–	–	400	pF
$t_{SU;DAT}$	data set-up time		250	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	–	ns
$t_{SU;STO}$	set-up time for STOP condition		4.0	–	–	µs

Notes

1. At f_{clk} < 125 kHz, I²C-bus maximum transmission speed is derated.
2. All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

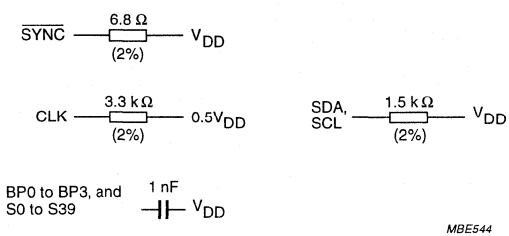


Fig.20 Test loads.

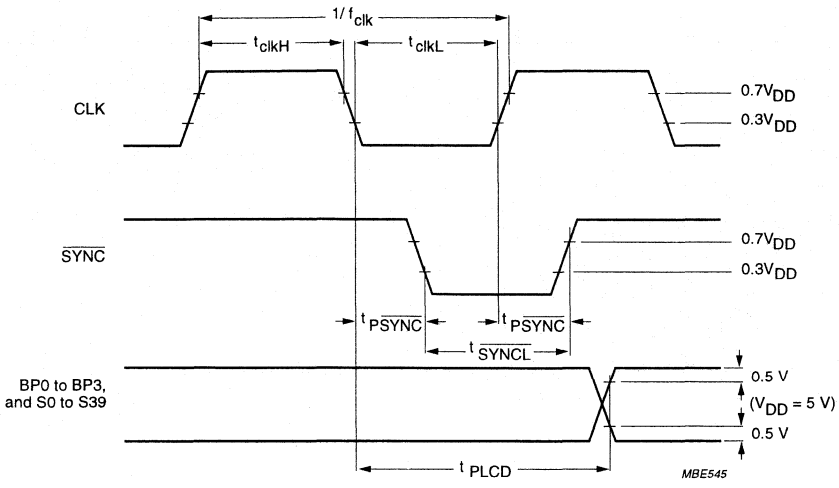


Fig.21 Driver timing waveforms.

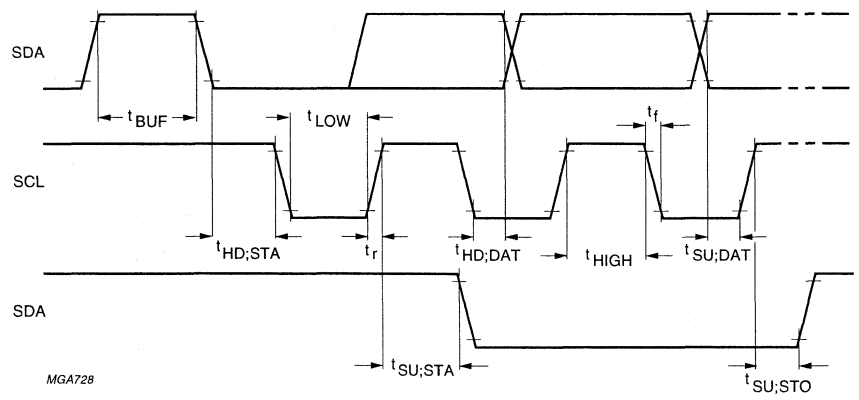
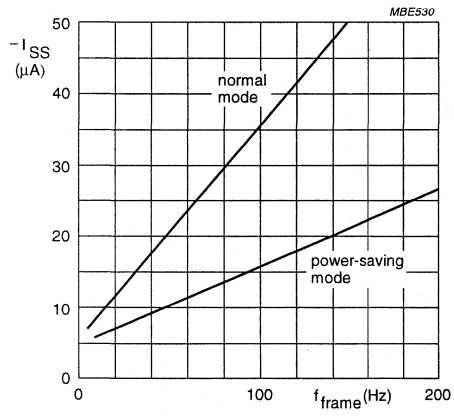


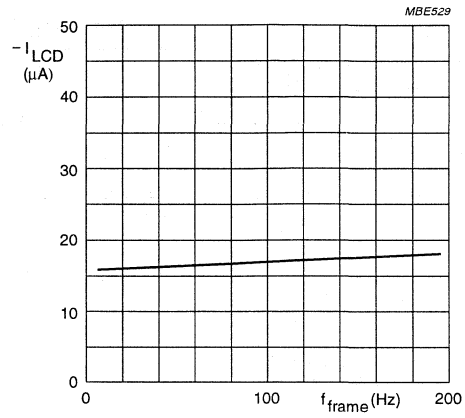
Fig.22 I²C-bus timing waveforms.

11.1 Typical supply current characteristics



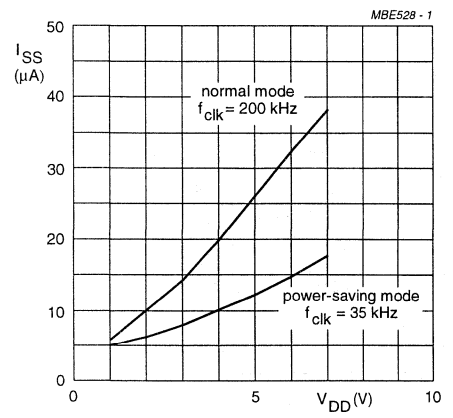
V_{DD} = 5 V; V_{LCD} = 0 V; T_{amb} = 25 °C.

Fig.23 $-I_{SS}$ as a function of f_{frame}.



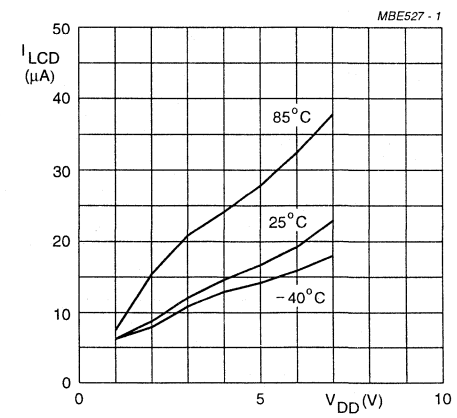
V_{DD} = 5 V; V_{LCD} = 0 V; T_{amb} = 25 °C.

Fig.24 $-I_{LCD}$ as a function of f_{frame}.



V_{LCD} = 0 V; external clock; T_{amb} = 25 °C.

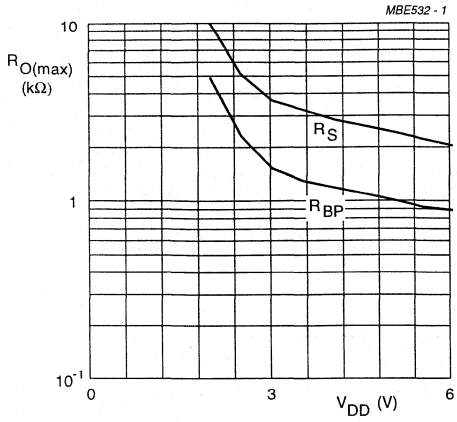
Fig.25 I_{SS} as a function of V_{DD}.



V_{LCD} = 0 V; external clock; f_{clk} = nominal frequency.

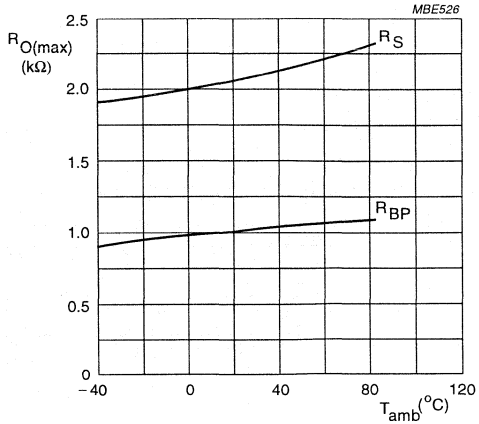
Fig.26 I_{LCD} as a function of V_{DD}.

11.2 Typical characteristics of LCD outputs



V_{LCD} = 0 V; T_{amb} = 25 °C.

Fig.27 $R_{O(max)}$ as a function of V_{DD}.



V_{DD} = 5 V; V_{LCD} = 0 V.

Fig.28 $R_{O(max)}$ as a function of T_{amb}.

12 APPLICATION INFORMATION

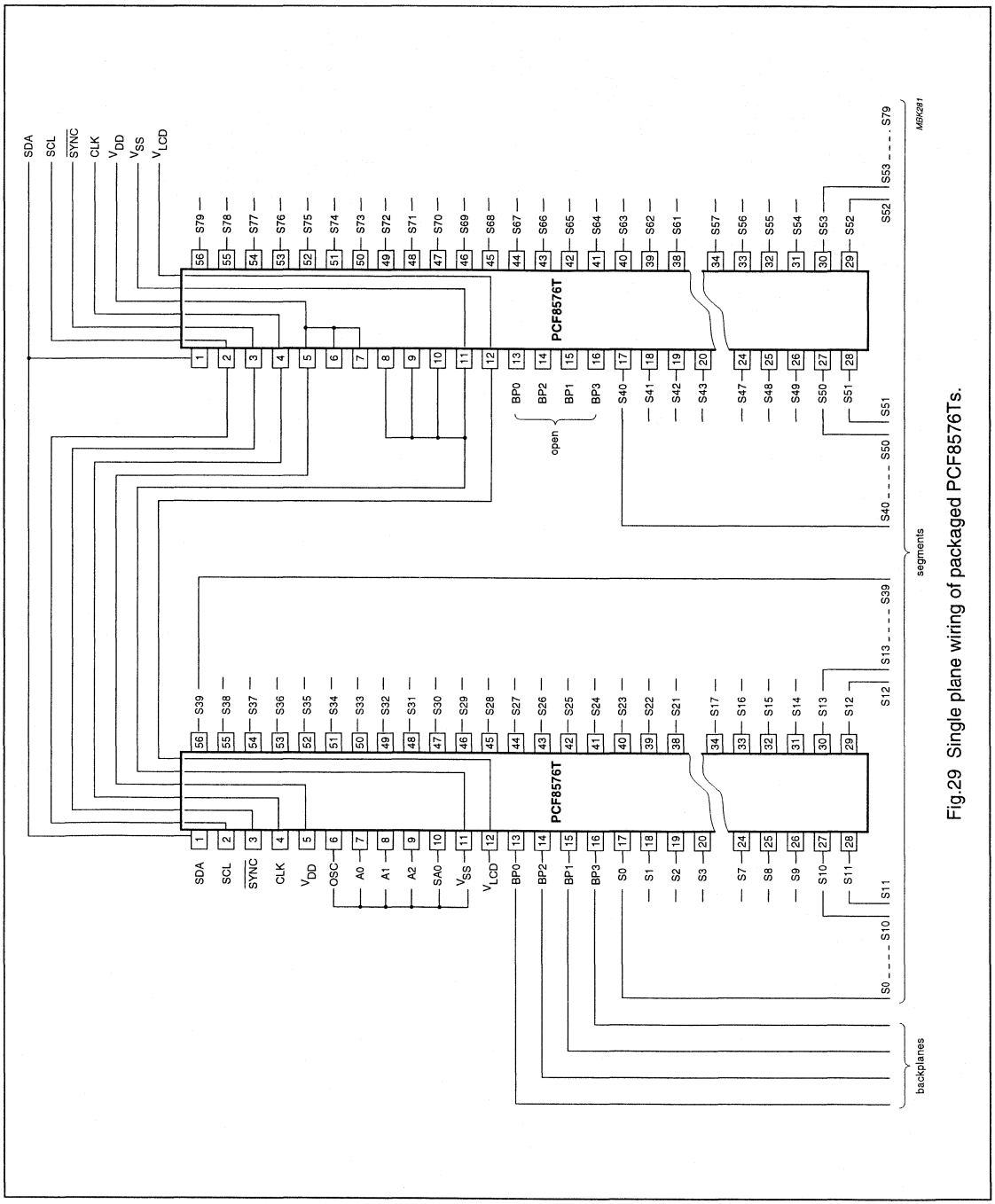


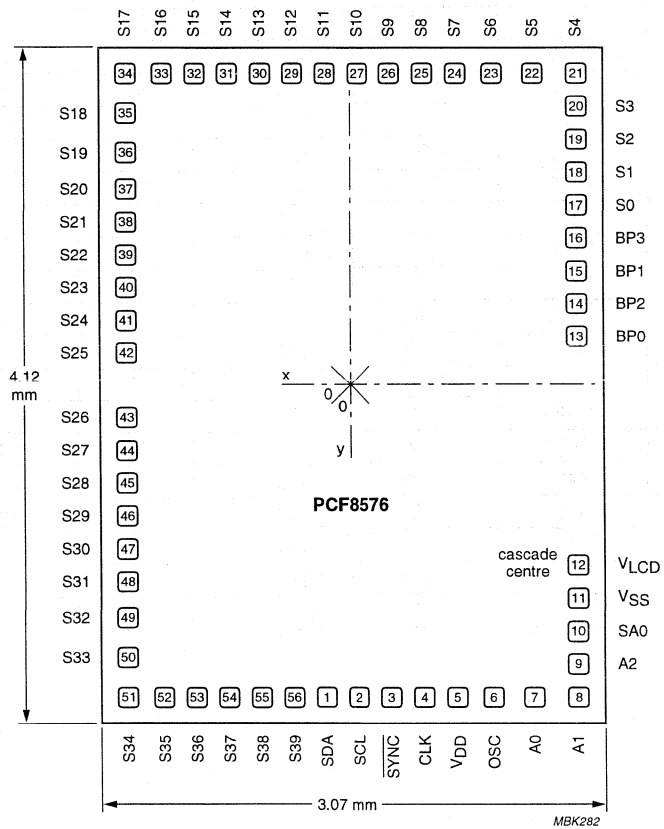
Fig.29 Single plane wiring of packaged PCF8576Ts.

12.1 Chip-on-glass cascadability in single plane

In chip-on-glass technology, where driver devices are bonded directly onto glass of the LCD, it is important that the devices may be cascaded without the crossing of conductors, but the paths of conductors can be continued on the glass under the chip. All of this is facilitated by the PCF8576 bonding pad layout (see Fig.30). Pads needing bus interconnection between all PCF8576s of the cascade are V_{DD}, V_{SS}, V_{LCD}, CLK, SCL, SDA and $\overline{SYNC}$. These lines may be led to the corresponding pads of the next PCF8576 through the wide opening between V_{LCD} pad and the backplane output pads. The only bus line that does not require a second opening to lead through to the next PCF8576 is V_{LCD}, being the cascade centre. The placing of V_{LCD} adjacent to V_{SS} allows the two supplies to be connected together.

When an external clocking source is to be used, OSC of all devices should be connected to V_{DD}.
The pads OSC, A0, A1, A2 and SA0 have been placed between V_{SS} and V_{DD} to facilitate wiring of oscillator, hardware subaddress and slave address.

13 BONDING PAD LOCATIONS



Bonding pad dimensions: 120 × 120 µm.

Fig.30 Bonding pad locations.

Table 16 Bonding pad locations (dimensions in μm)
All x/y coordinates are referenced to centre of chip (see Fig.30).

SYMBOL	PAD	x	y
SDA	1	−155	−1900
SCL	2	45	−1900
$\overline{SYNC}$	3	245	−1900
CLK	4	445	−1900
V_{DD}	5	645	−1900
OSC	6	865	−1900
A0	7	1105	−1900
A1	8	1375	−1900
A2	9	1375	−1700
SA0	10	1375	−1500
V_{SS}	11	1375	−1300
V_{LCD}	12	1375	−1100
BP0	13	1375	300
BP2	14	1375	500
BP1	15	1375	700
BP3	16	1375	900
S0	17	1375	1100
S1	18	1375	1300
S2	19	1375	1500
S3	20	1375	1700
S4	21	1375	1900
S5	22	1105	1900
S6	23	865	1900
S7	24	645	1900
S8	25	445	1900
S9	26	245	1900
S10	27	45	1900
S11	28	−155	1900

SYMBOL	PAD	x	y
S12	29	−355	1900
S13	30	−555	1900
S14	31	−755	1900
S15	32	−955	1900
S16	33	−1155	1900
S17	34	−1375	1900
S18	35	−1375	1660
S19	36	−1375	1420
S20	37	−1375	1200
S21	38	−1375	1000
S22	39	−1375	800
S23	40	−1375	600
S24	41	−1375	400
S25	42	−1375	200
S26	43	−1375	−200
S27	44	−1375	−400
S28	45	−1375	−600
S29	46	−1375	−800
S30	47	−1375	−1000
S31	48	−1375	−1200
S32	49	−1375	−1420
S33	50	−1375	−1660
S34	51	−1375	−1900
S35	52	−1155	−1900
S36	53	−955	−1900
S37	54	−755	−1900
S38	55	−555	−1900
S39	56	−355	−900

Universal LCD driver for low multiplex rates

PCF8576C

FEATURES

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
- Selectable display bias configuration: static, 1/2 or 1/3
- Internal LCD bias generation with voltage-follower buffers
- 40 segment drives: up to twenty 8-segment numeric characters; up to ten 15-segment alphanumeric characters; or any graphics of up to 160 elements
- 40 × 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- Wide power supply range: from 2 V for low-threshold LCDs and up to 6 V for guest-host LCDs and high-threshold (automobile) twisted nematic LCDs.

  A 9 V version is also available on request.
- Low power consumption
- Power-saving mode for extremely low power consumption in battery-operated and telephone applications
- I²C-bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 2560 segments possible)
- Cascadable with 24-segment LCD driver PCF8566
- Optimized pinning for plane wiring in both and multiple PCF8576C applications
- Space-saving 56-lead plastic very small outline package (VSO56) or 64-lead low profile quad flat package (LQFP64)
- No external components
- Compatible with chip-on-glass technology
- Manufactured in silicon gate CMOS process.

GENERAL DESCRIPTION

The PCF8576C is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD) with low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 40 segments and can easily be cascaded for larger LCD applications. The PCF8576C is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional I²C-bus. Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8576CT	VSO56	plastic very small outline package; 56 leads	SOT190-1
PCF8576CU	–	chip in tray	–
PCF8576CU/2	–	chip with bumps in tray	–
PCF8576CU/7	–	chip with bumps on tape	–
PCF8576CU/10	FFC	chip-on-film frame carrier	–
PCF8576CU/12	FFC	chip with bumps on film frame carrier	–
PCF8576CH	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2

Full Data Sheet: on CD-ROM/WWW (Internet) or FOD-system (details in front Section/back of this HB), or updated Loose leaf or Parent HB

BLOCK DIAGRAM

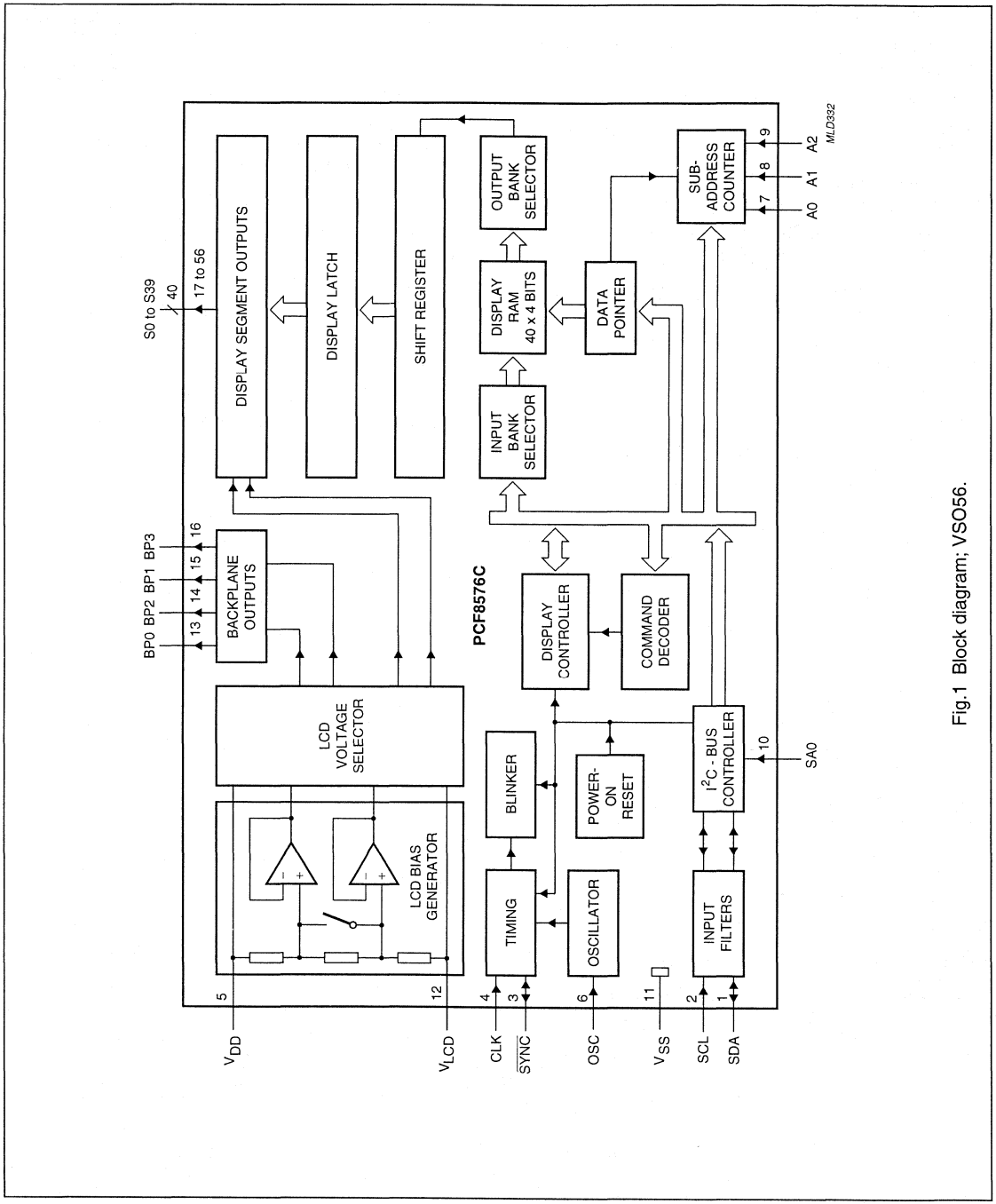


Fig.1 Block diagram; VSO56.

PINNING

SYMBOL	PIN		DESCRIPTION
	SOT190	SOT314	
SDA	1	10	I²C-bus serial data input/output
SCL	2	11	I²C-bus serial clock input
$\overline{SYNC}$	3	12	cascade synchronization input/output
CLK	4	13	external clock input
V_{DD}	5	14	supply voltage
OSC	6	15	oscillator input
A0 to A2	7 to 9	16 to 18	I²C-bus subaddress inputs
SA0	10	19	I²C-bus slave address input; bit 0
V_{SS}	11	20	logic ground
V_{LCD}	12	21	LCD supply voltage
BP0, BP2, BP1, BP3	13 to 16	25 to 28	LCD backplane outputs
S0 to S39	17 to 56	29 to 32, 34 to 47, 49 to 64, 2 to 7	LCD segment outputs
n.c.	–	1, 8, 9, 22 to 24, 33 and 48	not connected

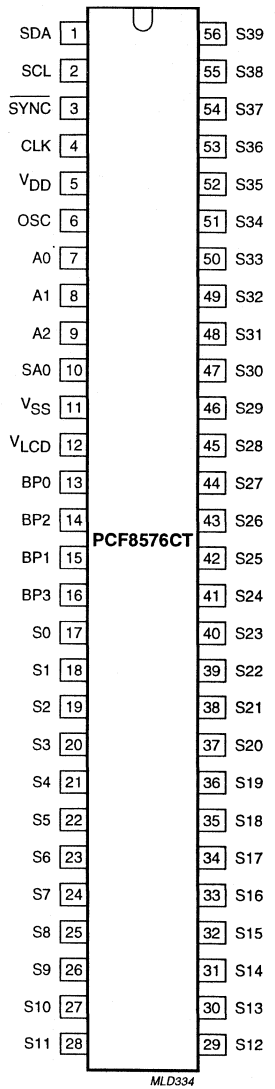


Fig.2 Pin configuration; VSO56.

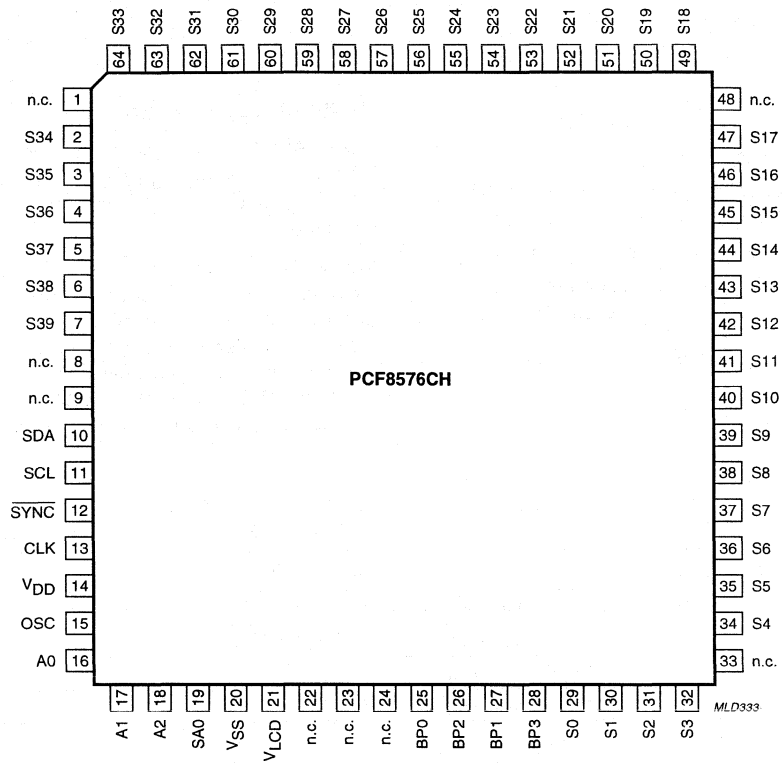


Fig.3 Pin configuration; LQFP64.

LCD direct/duplex driver with I²C-bus interface

PCF8577C

FEATURES

- Direct/duplex drive modes with up to 32/64 LCD-segment drive capability per device
- Operating supply voltage: 2.5 to 6 V
- Low power consumption
- I²C-bus interface
- Optimized pinning for single plane wiring
- Single-pin built-in oscillator
- Auto-incremented loading across device subaddress boundaries
- Display memory switching in direct drive mode
- May be used as I²C-bus output expander
- System expansion up to 256 segments
- Power-on reset blanks display
- I²C-bus address: 0111 0100.

GENERAL DESCRIPTION

The PCF8577C is a single chip, silicon gate CMOS circuit. It is designed to drive liquid crystal displays with up to 32 segments directly, or 64 segments in a duplex configuration.

The two-line I²C-bus interface substantially reduces wiring overheads in remote display applications. I²C-bus traffic is minimized in multiple IC applications by automatic address incrementing, hardware subaddressing and display memory switching (direct drive mode).To allow partial V_{DD} shutdown the ESD protection system of the SCL and SDA pins does not use a diode connected to V_{DD}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8577CP	DIP40	plastic dual in-line package; 40 leads (600 mil)	SOT129-1
PCF8577CT	VSO40	plastic very small outline package; 40 leads	SOT158A
PCF8577CT	–	VS040 in blister tape	–
PCF8577CU/10	–	chip on film-frame-carrier (FFC)	–

BLOCK DIAGRAM

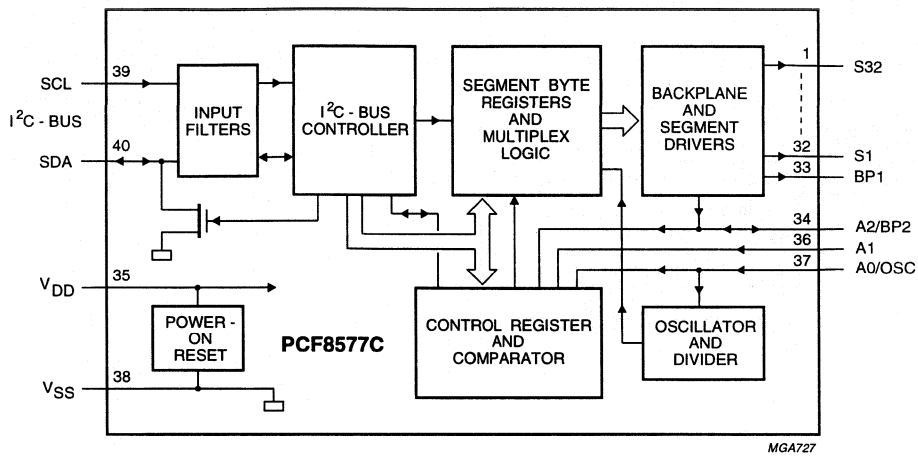


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
S32 to S1	1 to 32	segments outputs
BP1	33	cascade sync input/backplane output
A2/BP2	34	hardware address line and cascade sync input/backplane output
V_{DD}	35	positive supply voltage
A1	36	hardware address line input
A0/OSC	37	hardware address line and oscillator pin input
V_{SS}	38	negative supply voltage
SCL	39	I²C-bus clock line input
SDA	40	I²C-bus data line input/output

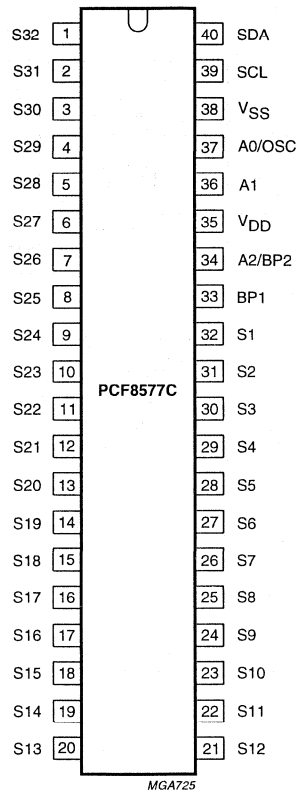


Fig.2 Pin configuration.

LCD row/column driver for dot matrix graphic displays

PCF8578

FEATURES

- Single chip LCD controller/driver
- Stand-alone or may be used with up to 32 PCF8579s (40960 dots possible)
- 40 driver outputs, configurable as $^{32}/_{8}$, $^{24}/_{16}$, $^{16}/_{24}$ or $^{8}/_{32}$ rows/columns
- Selectable multiplex rates; 1 : 8, 1 : 16, 1 : 24 or 1 : 32
- Externally selectable bias configuration, 5 or 6 levels
- 1280-bit RAM for display data storage and scratch pad
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries (with PCF8579)
- Provides display synchronization for PCF8579
- On-chip oscillator, requires only 1 external resistor
- Power-on reset blanks display
- Logic voltage supply range 2.5 to 6 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I²C-bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications (with PCF8579)
- Space saving 56-lead plastic mini-pack and 64 pin quad flat pack
- Compatible with chip-on-glass technology.

APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Computer terminals
- Instrumentation.

GENERAL DESCRIPTION

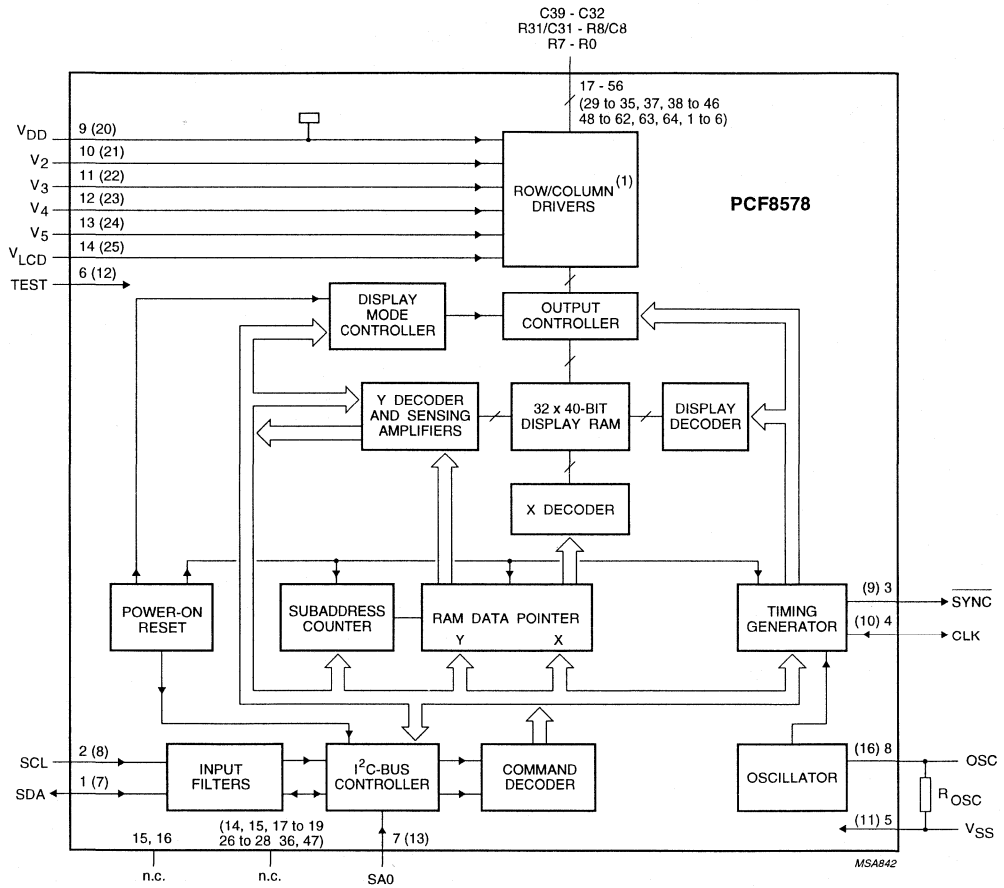
The PCF8578 is a low power CMOS LCD row/column driver, designed to drive dot matrix graphic displays at multiplex rates of 1 : 8, 1 : 16, 1 : 24 or 1 : 32. The device has 40 outputs, of which 24 are programmable, configurable as $^{32}/_{8}$, $^{24}/_{16}$, $^{16}/_{24}$ or $^{8}/_{32}$ rows/columns. The PCF8578 can function as a stand-alone LCD controller/driver for use in small systems, or for larger systems can be used in conjunction with up to 32 PCF8579s for which it has been optimized. Together these two devices form a general purpose LCD dot matrix driver chip set, capable of driving displays of up to 40960 dots. The PCF8578 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I²C-bus). Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8578T	VSO56	plastic very small outline package; 56 leads	SOT190-1
PCF8578U7	–	chip with bumps on tape	–
PCF8578H	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2

Full Data Sheet: on CD-ROM/WWW (Internet) or FOD-system (details in front Section/back of this HB), or updated Loose leaf or Parent HB

BLOCK DIAGRAM



(1) Operates at LCD voltage levels, all other blocks operate at logic levels.
The pin numbers given in parenthesis refer to the LQFP64 package.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN		DESCRIPTION
	VSO56	LQFP64	
SDA	1	7	I²C-bus serial data input/output
SCL	2	8	I²C-bus serial clock input
$\overline{SYNC}$	3	9	cascade synchronization output
CLK	4	10	external clock input/output
V_{SS}	5	11	ground (logic)
TEST	6	12	test pin (connect to V_{SS})
SA0	7	13	I²C-bus slave address input (bit 0)
OSC	8	16	oscillator input
V_{DD}	9	20	positive supply voltage
V_2 to V_5	10 to 13	21 to 24	LCD bias voltage inputs
V_{LCD}	14	25	LCD supply voltage
n.c.	15, 16	14, 15, 17 to 19, 26 to 28, 36, 47	not connected
C39 to C32	17 to 24	29 to 35, 37	LCD column driver outputs
R31/C31 to R8/C8	25 to 48	38 to 46, 48 to 62	LCD row/column driver outputs
R7 to R0	49 to 56	63, 64, 1 to 6	LCD row driver outputs

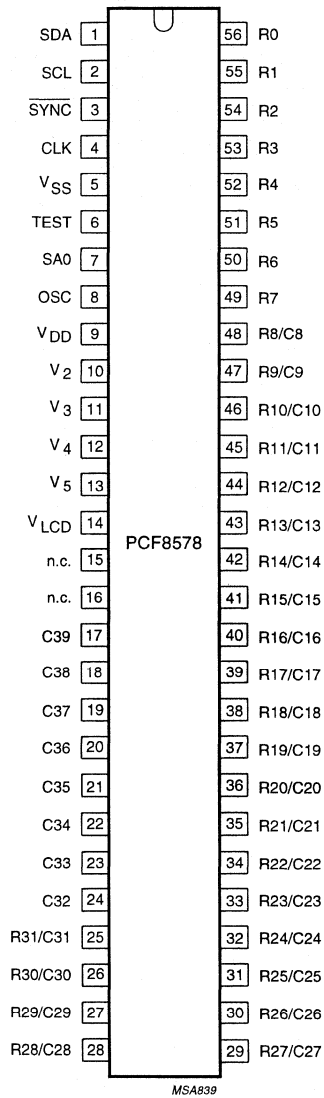


Fig.2 Pin configuration (VSO56).

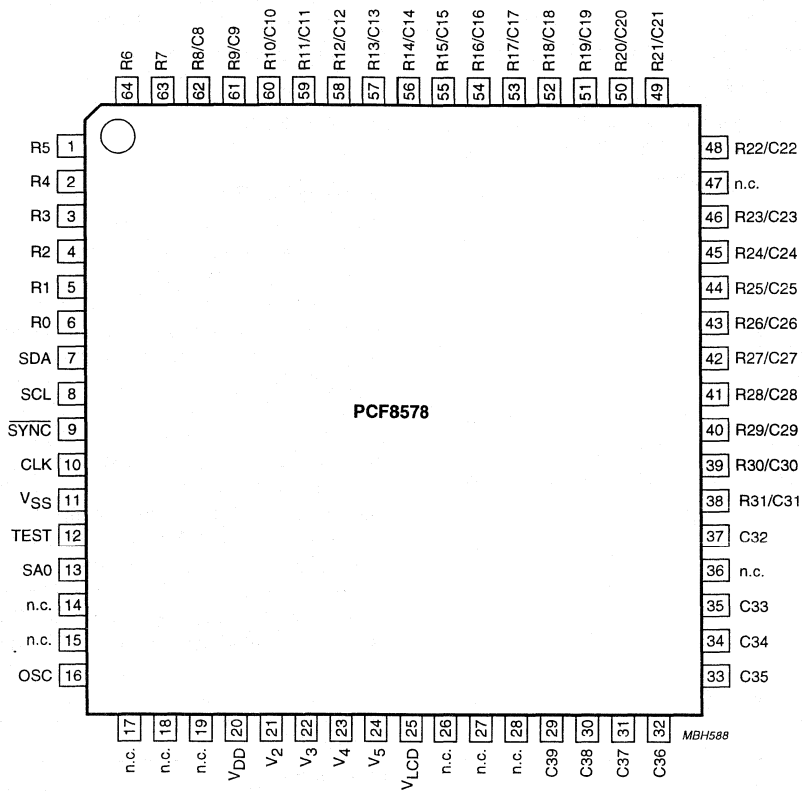


Fig.3 Pin configuration (LQFP64).

LCD column driver for dot matrix graphic displays

PCF8579

FEATURES

- LCD column driver
- Used in conjunction with the PCF8578, this device forms part of a chip set capable of driving up to 40960 dots
- 40 column outputs
- Selectable multiplex rates; 1 : 8, 1 : 16, 1 : 24 or 1 : 32
- Externally selectable bias configuration, 5 or 6 levels
- Easily cascadable for large applications (up to 32 devices)
- 1280-bit RAM for display data storage
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries (with PCF8578)
- Power-on reset blanks display
- Logic voltage supply range 2.5 to 6 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I²C-bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications (with PCF8578)
- Space saving 56-lead plastic mini-pack and 64-pin plastic low profile quad flat package
- Compatible with chip-on-glass technology
- I²C-bus address: 011110 SA0.

APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Computer terminals
- Instrumentation.

GENERAL DESCRIPTION

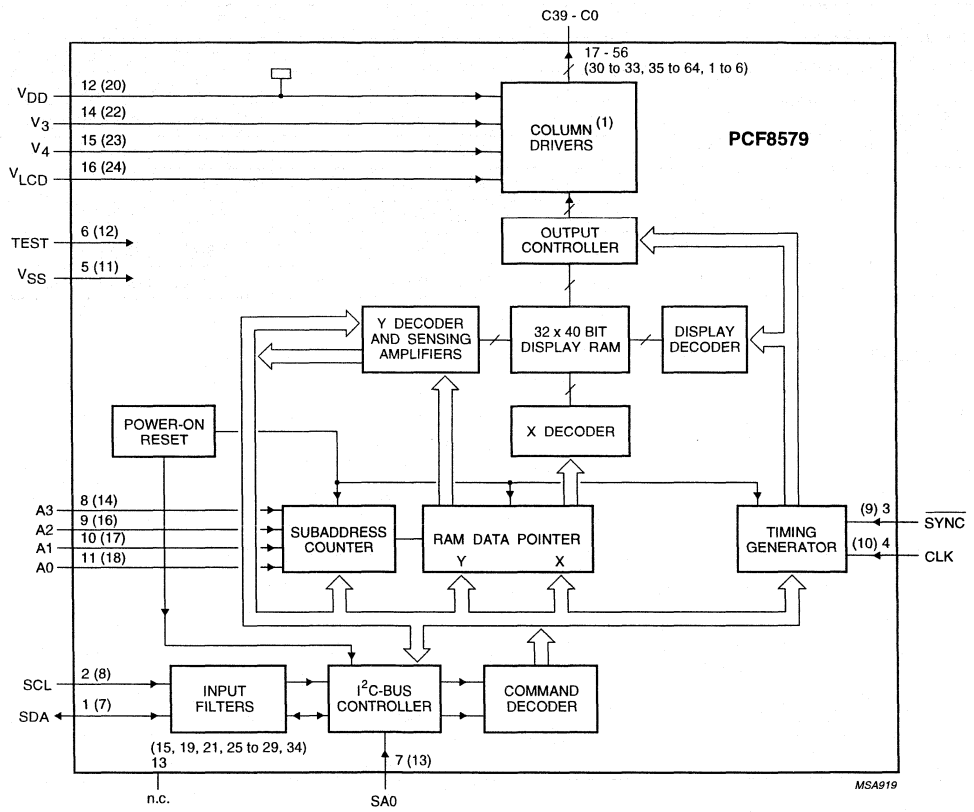
The PCF8579 is a low power CMOS LCD column driver, designed to drive dot matrix graphic displays at multiplex rates of 1 : 8, 1 : 16, 1 : 24 or 1 : 32. The device has 40 outputs and can drive 32 × 40 dots in a 32 row multiplexed LCD. Up to 16 PCF8579s can be cascaded and up to 32 devices may be used on the same I²C-bus (using the two slave addresses). The device is optimized for use with the PCF8578 LCD row/column driver. Together these two devices form a general purpose LCD dot matrix driver chip set, capable of driving displays of up to 40960 dots. The PCF8579 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I²C-bus). To allow partial V_{DD} shutdown the ESD protection system of the SCL and SDA pins does not use a diode connected to V_{DD}. Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8579T	VSO56	plastic very small outline package; 56 leads	SOT190
PCF8579U7	–	chip with bumps on tape	–
PCF8579H	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2

Full Data Sheet: on CD-ROM/WWW (Internet) or FOD-system (details in front Section/back of this HB), or updated Loose leaf or Parent HB

BLOCK DIAGRAM



(1) Operates at LCD voltage levels, all other blocks operate at logic levels.
The pin numbers given in parenthesis refer to the LQFP64 package.

Fig.1 Block diagram.

PINNING

SYMBOL	PINS		DESCRIPTION
	VSO56	LQFP64	
SDA	1	7	I²C-bus serial data input/output
SCL	2	8	I²C-bus serial clock input
$\overline{SYNC}$	3	9	cascade synchronization input
CLK	4	10	external clock input
V_{SS}	5	11	ground (logic)
TEST	6	12	test pin (connect to V_{SS})
SA0	7	13	I²C-bus slave address input (bit 0)
A3 to A0	8 to 11	14, 16 to 18	I²C-bus subaddress inputs
V_{DD}	12	20	supply voltage
n.c.	13(1)	15, 19, 21,25 to 29, 34	not connected
V_3, V_4	14 and 15	22 and 23	LCD bias voltage inputs
V_{LCD}	16	24	LCD supply voltage
C39 to C0	17 to 56	30 to 33, 35 to 64 and 1 to 6	LCD column driver outputs

Note

1. Do not connect, this pin is reserved.

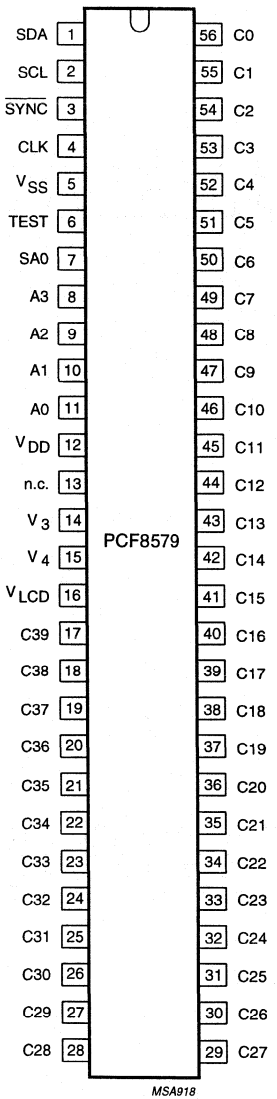


Fig.2 Pin configuration (VSO56).

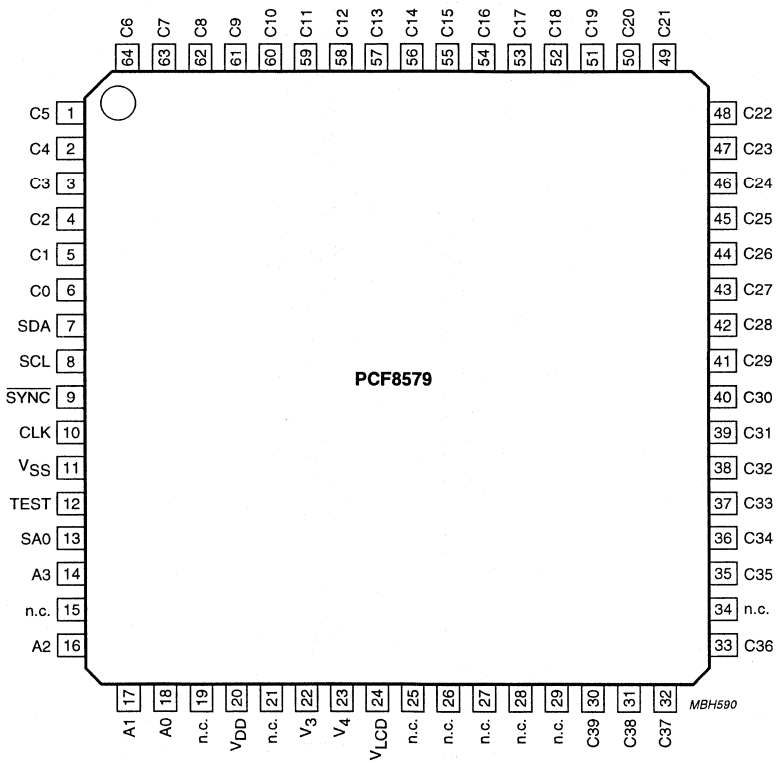


Fig.3 Pin configuration (LQFP64).

Low power clock/calendar | PCF8593

FEATURES

- I²C-bus interface operating supply voltage: 2.5 to 6.0 V
- Clock operating supply voltage (T_{amb} = 0 to +70 °C): 1.0 to 6.0 V
- 8 bytes scratchpad RAM (when alarm not used)
- Data retention voltage: 1.0 to 6.0 V
- External $\overline{RESET}$ input resets I²C interface (only)
- Operating current (f_{scl} = 0 Hz, 32 kHz time base, V_{DD} = 2.0 V): typ. 1 µA
- Clock function with four year calendar
- Universal timer with alarm and overflow indication
- 24 or 12 hour format
- 32.768 kHz or 50 Hz time base
- Serial input/output bus (I²C-bus)
- Automatic word address incrementing
- Programmable alarm, timer and interrupt function
- Space-saving SO8 package available
- Slave address:
  - READ A3
  - WRITE A2.

GENERAL DESCRIPTION

The PCF8593 is a CMOS clock/calendar circuit, optimized for low power consumption. Addresses and data are transferred serially via the two-line bidirectional I²C-bus. The built-in word address register is incremented automatically after each written or read data byte.
The built-in 32.768 kHz oscillator circuit and the first 8 bytes of RAM are used for the clock/calendar and counter functions. The next 8 bytes may be programmed as alarm registers or used as free RAM space.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage operating mode	I²C-bus active	2.5	–	6.0	V
		I²C-bus inactive	1.0	–	6.0	V
I_{DD}	supply current operating mode	f_{scl} = 100 kHz	–	–	200	µA
I_{DD}	supply current clock mode	f_{scl} = 0 Hz; V_{DD} = 5 V	–	4.0	15.0	µA
		f_{scl} = 0 Hz; V_{DD} = 2 V	–	1.0	8.0	µA
T_{amb}	operating ambient temperature		−40	–	+85	°C
T_{stg}	storage temperature		−65	–	+150	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8593P	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
PCF8593T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

Full Data Sheet: on CD-ROM/WWW (Internet) or FOD-system (details in front Section/back of this HB), or updated Loose leaf or Parent HB

BLOCK DIAGRAM

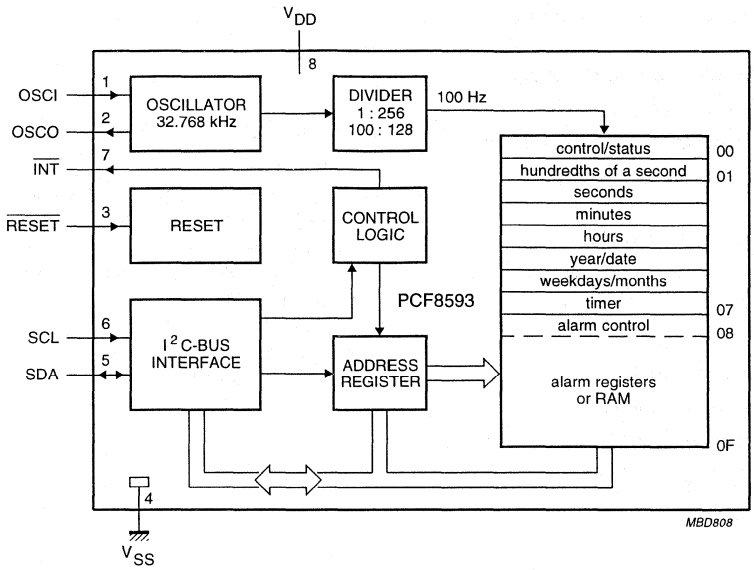


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
OSCI	1	oscillator input, 50 Hz or event-pulse input
OSCO	2	oscillator output
$\overline{\text{RESET}}$	3	reset input (active LOW)
V_{SS}	4	negative supply
SDA	5	serial data input/output
SCL	6	serial clock input
$\overline{\text{INT}}$	7	open drain interrupt output (active LOW)
V_{DD}	8	positive supply

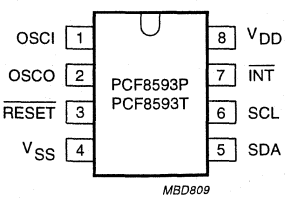


Fig.2 Pin configuration.

Complementary enhancement mode MOS transistors

PHC20512

FEATURES

- High-speed switching
- No secondary breakdown
- Very low on-state resistance.

APPLICATIONS

- Motor and actuator driver
- Power management
- Synchronized rectification.

DESCRIPTION

One N-channel and one P-channel enhancement mode MOS transistor in an 8-pin plastic SOT96-1 (SO8) package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT96-1 (SO8)

PIN	SYMBOL	DESCRIPTION
1	s_1	source 1
2	g_1	gate 1
3	s_2	source 2
4	g_2	gate 2
5	d_2	drain 2
6	d_2	drain 2
7	d_1	drain 1
8	d_1	drain 1

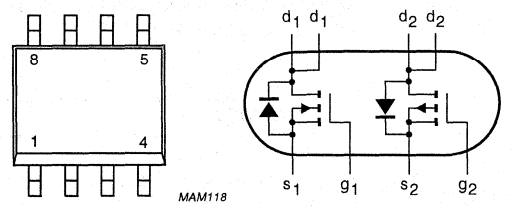


Fig.1 Simplified outline and symbol.

Complementary enhancement mode MOS transistors

PHC21025

FEATURES

- High-speed switching
- No secondary breakdown
- Very low on-resistance.

APPLICATIONS

- Motor and actuator driver
- Power management
- Synchronized rectification.

DESCRIPTION

One N-channel and one P-channel enhancement mode MOS transistor in an 8-pin plastic SOT96-1 (SO8) package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT96-1 (SO8)

PIN	SYMBOL	DESCRIPTION
1	s_1	source 1
2	g_1	gate 1
3	s_2	source 2
4	g_2	gate 2
5	d_2	drain 2
6	d_2	drain 2
7	d_1	drain 1
8	d_1	drain 1

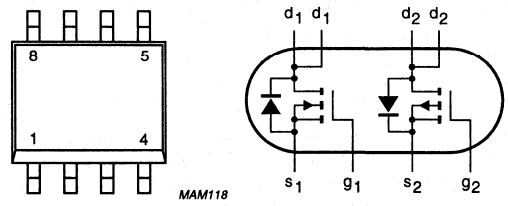


Fig.1 Simplified outline and symbol.

Dual N-channel enhancement mode MOS transistor

PHN205

FEATURES

- High-speed switching
- No secondary breakdown
- Very low on-state resistance.

APPLICATIONS

- Motor and actuator driver
- Power management
- Synchronized rectification.

DESCRIPTION

Two N-channel enhancement mode MOS transistors in an 8-pin plastic SOT96-1 (SO8) package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT96-1 (SO8)

PIN	SYMBOL	DESCRIPTION
1	s_1	source 1
2	g_1	gate 1
3	s_2	source 2
4	g_2	gate 2
5	d_2	drain 2
6	d_2	drain 2
7	d_1	drain 1
8	d_1	drain 1

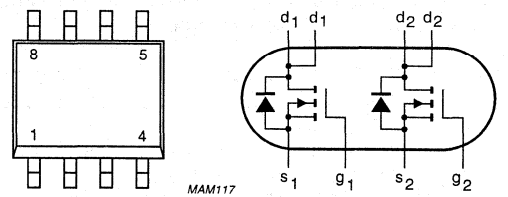


Fig.1 Simplified outline and symbol.

Dual N-channel enhancement mode MOS transistor

PHN210

FEATURES

- High-speed switching
- No secondary breakdown
- Very low on-resistance.

APPLICATIONS

- Motor and actuator driver
- Power management
- Synchronized rectification.

DESCRIPTION

Two N-channel enhancement mode MOS transistors in an 8-pin plastic SOT96-1 (SO8) package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT96-1 (SO8)

PIN	SYMBOL	DESCRIPTION
1	s_1	source 1
2	g_1	gate 1
3	s_2	source 2
4	g_2	gate 2
5	d_2	drain 2
6	d_2	drain 2
7	d_1	drain 1
8	d_1	drain 1

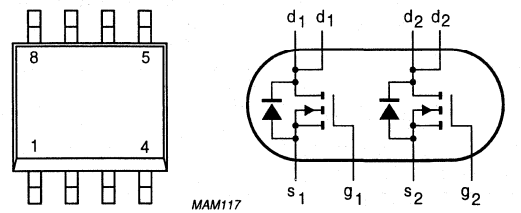


Fig.1 Simplified outline and symbol.

Dual P-channel enhancement mode MOS transistor

PHP212

FEATURES

- High-speed switching
- No secondary breakdown
- Very low on-state resistance.

APPLICATIONS

- Motor and actuator driver
- Power management
- Synchronized rectification.

DESCRIPTION

Two P-channel enhancement mode MOS transistors in an 8-pin plastic SOT96-1 (SO8) package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT96-1 (SO8)

PIN	SYMBOL	DESCRIPTION
1	s_1	source 1
2	g_1	gate 1
3	s_2	source 2
4	g_2	gate 2
5	d_2	drain 2
6	d_2	drain 2
7	d_1	drain 1
8	d_1	drain 1

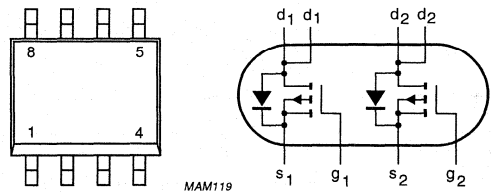


Fig.1 Simplified outline and symbol.

Dual P-channel enhancement mode MOS transistor

PHP212L

FEATURES

- High-speed switching
- No secondary breakdown
- Very low on-state resistance
- Low threshold.

APPLICATIONS

- Motor and actuator driver
- Power management
- Synchronized rectification.

DESCRIPTION

Two P-channel enhancement mode MOS transistors in an 8-pin plastic SOT96-1 (SO8) package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT96-1 (SO8)

PIN	SYMBOL	DESCRIPTION
1	s_1	source 1
2	g_1	gate 1
3	s_2	source 2
4	g_2	gate 2
5	d_2	drain 2
6	d_2	drain 2
7	d_1	drain 1
8	d_1	drain 1

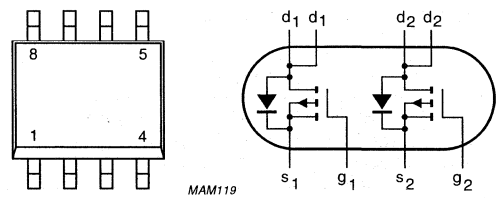


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–30	V
V_{SD}	source-drain diode forward voltage	I_S = –1.25 A	–	–1.3	V
V_{GS}	gate-source voltage (DC)		–	±12	V
V_{GSth}	gate-source threshold voltage	I_D = –1 mA; V_{DS} = V_{GS}	–0.5	–1.1	V
I_D	drain current (DC)	T_s = 80 °C	–	–4	A
R_{DSon}	drain-source on-state resistance	I_D = –2 A; V_{GS} = –4.5 V	–	0.12	Ω
P_{tot}	total power dissipation	T_s = 80 °C	–	3.5	W

Dual P-channel enhancement mode MOS transistor

PHP212L

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per P-channel					
V_{DS}	drain-source voltage (DC)		–	–30	V
V_{GS}	gate-source voltage (DC)		–	±12	V
I_D	drain current (DC)	T_s = 80 °C; note 1	–	–4	A
I_{DM}	peak drain current	note 2	–	–16	A
P_{tot}	total power dissipation	T_s = 80 °C; note 3	–	3.5	W
		T_{amb} = 25 °C; note 4	–	2.6	W
		T_{amb} = 25 °C; note 5	–	1.1	W
		T_{amb} = 25 °C; note 6	–	1.5	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–55	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 80 °C	–	–2.6	A
I_{SM}	peak pulsed source current	note 2	–	–10	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Maximum permissible dissipation per MOS transistor. Both devices may be loaded up to 3.5 W at the same time.
4. Maximum permissible dissipation per MOS transistor. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
5. Maximum permissible dissipation per MOS transistor. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.
6. Maximum permissible dissipation if only one MOS transistor dissipates. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	20	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per P-channel						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = −10 μA	−30	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = −1 mA	−0.5	–	−1.1	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = −24 V	–	–	−100	nA
I_{GSS}	gate leakage current	V_{GS} = ±12 V; V_{DS} = 0	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = −2.5 V; I_D = −1 A	–	–	0.25	Ω
		V_{GS} = −4.5 V; I_D = −2 A	–	–	0.12	Ω
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = −24 V; f = 1 MHz	–	450	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = −24 V; f = 1 MHz	–	200	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = −24 V; f = 1 MHz	–	100	–	pF
Q_G	total gate charge	V_{GS} = −6 V; V_{DD} = −15 V; I_D = −1 A	–	13	–	nC
Q_{GS}	gate-source charge	V_{GS} = −6 V; V_{DD} = −15 V; I_D = −1 A	–	1	–	nC
Q_{GD}	gate-drain charge	V_{GS} = −6 V; V_{DD} = −15 V; I_D = −1 A	–	4	–	nC
Switching times						
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to −6 V; V_{DD} = −15 V; I_D = −1 A; R_{gen} = 6 Ω	–	6	–	ns
t_r	rise time	V_{GS} = 0 to −6 V; V_{DD} = −15 V; I_D = −1 A; R_{gen} = 6 Ω	–	4	–	ns
t_{on}	turn-on switching time	V_{GS} = 0 to −6 V; V_{DD} = −15 V; I_D = −1 A; R_{gen} = 6 Ω	–	10	–	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = −6 to 0 V; V_{DD} = −15 V; I_D = −1 A; R_{gen} = 6 Ω	–	29	–	ns
t_f	fall time	V_{GS} = −6 to 0 V; V_{DD} = −15 V; I_D = −1 A; R_{gen} = 6 Ω	–	16	–	ns
t_{off}	turn-off switching time	V_{GS} = −6 to 0 V; V_{DD} = −15 V; I_D = −1 A; R_{gen} = 6 Ω	–	45	–	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = −1.25 A	–	–	−1.3	V
t_{rr}	reverse recovery time	I_S = −1.25 A; di/dt = 100 A/μs	–	75	–	ns

Dual P-channel enhancement mode MOS transistor

PHP225

FEATURES

- High-speed switching
- No secondary breakdown
- Very low on-resistance.

APPLICATIONS

- Motor and actuator driver
- Power management
- Synchronized rectification.

DESCRIPTION

Two P-channel enhancement mode MOS transistors in an 8-pin plastic SOT96-1 (SO8) package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT96-1 (SO8)

PIN	SYMBOL	DESCRIPTION
1	s_1	source 1
2	g_1	gate 1
3	s_2	source 2
4	g_2	gate 2
5	d_2	drain 2
6	d_2	drain 2
7	d_1	drain 1
8	d_1	drain 1

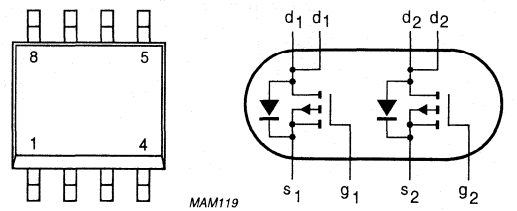


Fig.1 Simplified outline and symbol.

Compandor SA571

DESCRIPTION

The SA571 is a versatile low cost dual gain control circuit in which either channel may be used as a dynamic range compressor or expandor. Each channel has a full-wave rectifier to detect the average value of the signal, a linerarized temperature-compensated variable gain cell, and an operational amplifier.

The SA571 is well suited for use in cellular radio and radio communications systems, modems, telephone, and satellite broadcast/receive audio systems.

FEATURES

- Complete compressor and expandor in one IChip
- Temperature compensated
- Greater than 110dB dynamic range
- Operates down to 6VDC
- System levels adjustable with external components
- Distortion may be trimmed out
- Dynamic noise reduction systems
- Voltage-controlled amplifier

PIN CONFIGURATION

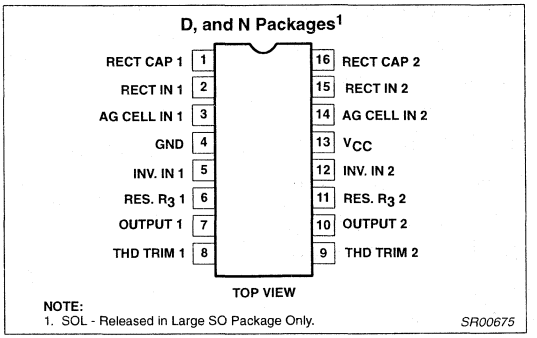


Figure 1. Pin Configuration

APPLICATIONS

- Cellular radio
- High level limiter
- Low level expandor—noise gate
- Dynamic filters
- CD Player

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Small Outline Large (SOL)	-40 to +85°C	SA571D	SOT162-1
16-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA571N	SOT38-4

BLOCK DIAGRAM

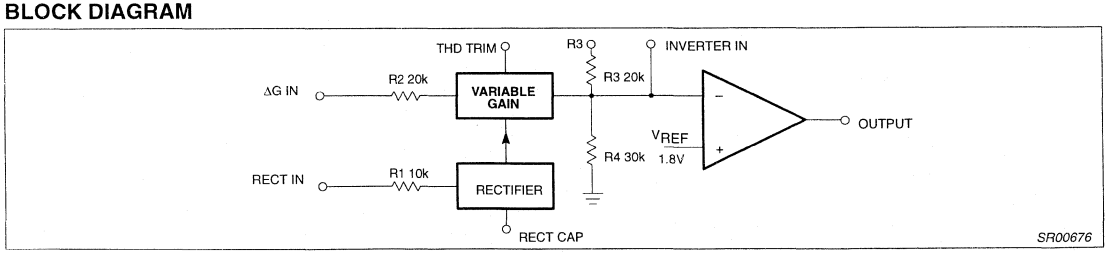


Figure 2. Block Diagram

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Maximum operating voltage 571	18	VDC
T_A	Operating ambient temperature range SA	-40 to +85	°C
P_D	Power dissipation	400	mW

AC ELECTRICAL CHARACTERISTICS

V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA571[5]			
			MIN	TYP	MAX	
V_{CC}	Supply voltage		6		18	V
I_{CC}	Supply current	No signal		3.2	4.8	mA
I_{OUT}	Output current capability		±20			mA
SR	Output slew rate			±.5		V/µs
	Gain cell distortion[2]	Untrimmed Trimmed		0.5 0.1	2.0	%
	Resistor tolerance			±5	±15	%
	Internal reference voltage		1.65	1.8	1.95	V
	Output DC shift[3]	Untrimmed		±30	±150	mV
	Expandor output noise	No signal, 15Hz-20kHz[1]		20	60	µV
	Unity gain level[6]	1kHz	-1.5	0	+1.5	dBm
	Gain change[2, 4]			±0.1		dB
	Reference drift[4]			+2, -25	+20, -50	mV
	Resistor drift[4]			+8, -0		%
	Tracking error (measured relative to value at unity gain) equals [V_O - V_O (unity gain)] dB - V_2dBm	Rectifier input, V_2 = +6dBm, V_1 = 0dB V_2 = -30dBm, V_1 = 0dB		+0.2 +0.2	 -1, +1.5	dB
	Channel separation			60		dB

NOTES:
1. Input to V_1 and V_2 grounded.
2. Measured at 0dBm, 1kHz.
3. Expandor AC input change from no signal to 0dBm.
4. Relative to value at T_A = 25°C.
5. Electrical characteristics for the SA571 only are specified over -40 to +85°C temperature range.
6. 0dBm = 775mV_{RMS}.

CIRCUIT DESCRIPTION

The SA571 compandor building blocks, as shown in the block diagram, are a full-wave rectifier, a variable gain cell, an operational amplifier and a bias system. The arrangement of these blocks in the IC result in a circuit which can perform well with few external components, yet can be adapted to many diverse applications.

The full-wave rectifier rectifies the input current which flows from the rectifier input, to an internal summing node which is biased at V_{REF}. The rectified current is averaged on an external filter capacitor tied to the C_{RECT} terminal, and the average value of the input current controls the gain of the variable gain cell. The gain will thus be proportional to the average value of the input signal for capacitively-coupled voltage inputs as shown in the following equation. Note that for capacitively-coupled inputs there is no offset voltage capable of producing a gain error. The only error will come from the bias current of the rectifier (supplied internally) which is less than 0.1μA.

$$G \propto \frac{|V_{IN} - V_{REF}|_{avg}}{R_1}$$

or

$$G \propto \frac{|V_{IN}|_{avg}}{R_1}$$

The speed with which gain changes to follow changes in input signal levels is determined by the rectifier filter capacitor. A small capacitor will yield rapid response but will not fully filter low frequency signals. Any ripple on the gain control signal will modulate the signal passing through the variable gain cell. In an expander or compressor application, this would lead to third harmonic distortion, so there is a trade-off to be made between fast attack and decay times and distortion. For step changes in amplitude, the change in gain with time is shown by this equation.

$$G(t) = (G_{initial} - G_{final})e^{-t/\tau} + G_{final} \; ; \; \tau = 10k \times C_{RECT}$$

The variable gain cell is a current-in, current-out device with the ratio I_{OUT}/I_{IN} controlled by the rectifier. I_{IN} is the current which flows from the ΔG input to an internal summing node biased at V_{REF}. The following equation applies for capacitively-coupled inputs. The output current, I_{OUT}, is fed to the summing node of the op amp.

$$I_{IN} = \frac{V_{IN} - V_{REF}}{R_2} = \frac{V_{IN}}{R_2}$$

A compensation scheme built into the ΔG cell compensates for temperature and cancels out odd harmonic distortion. The only distortion which remains is even harmonics, and they exist only because of internal offset voltages. The THD trim terminal provides a means for nulling the internal offsets for low distortion operation.

The operational amplifier (which is internally compensated) has the non-inverting input tied to V_{REF}, and the inverting input connected to the ΔG cell output as well as brought out externally. A resistor, R_3, is brought out from the summing node and allows compressor or expander gain to be determined only by internal components.

The output stage is capable of ±20mA output current. This allows a +13dBm ($3.5V_{RMS}$) output into a 300Ω load which, with a series resistor and proper transformer, can result in +13dBm with a 600Ω output impedance.

A bandgap reference provides the reference voltage for all summing nodes, a regulated supply voltage for the rectifier and ΔG cell, and a bias current for the ΔG cell. The low tempco of this type of reference provides very stable biasing over a wide temperature range.

The typical performance characteristics illustration shows the basic input-output transfer curve for basic compressor or expander circuits.

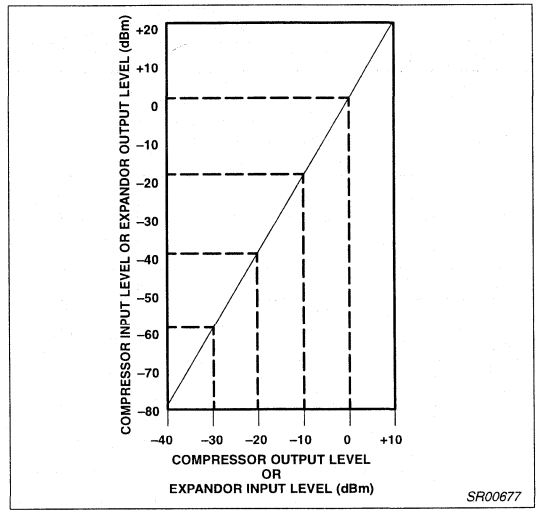


Figure 3. Basic Input-Output Transfer Curve

TYPICAL TEST CIRCUIT

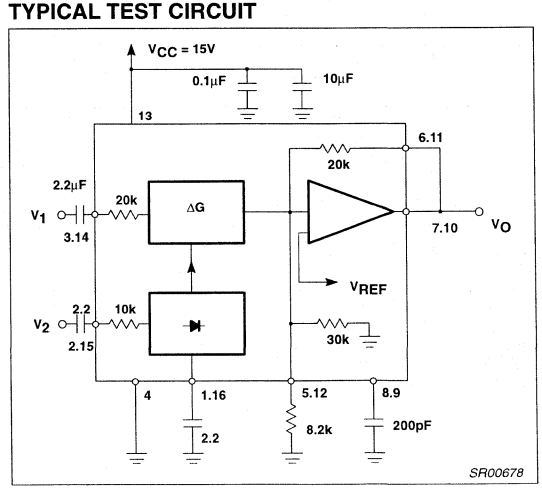


Figure 4. Typical Test Circuit

INTRODUCTION

Much interest has been expressed in high performance electronic gain control circuits. For non-critical applications, an integrated circuit operational transconductance amplifier can be used, but when high-performance is required, one has to resort to complex discrete circuitry with many expensive, well-matched components.

This paper describes an inexpensive integrated circuit, the SA571 Compandor, which offers a pair of high performance gain control circuits featuring low distortion (<0.1%), high signal-to-noise ratio (90dB), and wide dynamic range (110dB).

CIRCUIT BACKGROUND

The SA571 Compandor was originally designed to satisfy the requirements of the telephone system. When several telephone channels are multiplexed onto a common line, the resulting signal-to-noise ratio is poor and companding is used to allow a wider dynamic range to be passed through the channel. Figure 5 graphically shows what a compandor can do for the signal-to-noise ratio of a restricted dynamic range channel. The input level range of +20 to -80dB is shown undergoing a 2-to-1 compression where a 2dB input level change is compressed into a 1dB output level change by the compressor. The original 100dB of dynamic range is thus compressed to a 50dB range for transmission through a restricted dynamic range channel. A complementary expansion on the receiving end restores the original signal levels and reduces the channel noise by as much as 45dB.

The significant circuits in a compressor or expander are the rectifier and the gain control element. The phone system requires a simple full-wave averaging rectifier with good accuracy, since the rectifier accuracy determines the (input) output level tracking accuracy. The gain cell determines the distortion and noise characteristics, and the phone system specifications here are very loose. These specs could have been met with a simple operational transconductance multiplier, or OTA, but the gain of an OTA is proportional to temperature and this is very undesirable. Therefore, a linearized transconductance multiplier was designed which is insensitive to temperature and offers low noise and low distortion performance. These features make the circuit useful in audio and data systems as well as in telecommunications systems.

BASIC CIRCUIT HOOK-UP AND OPERATION

Figure 6 shows the block diagram of one half of the chip, (there are two identical channels on the IC). The full-wave averaging rectifier provides a gain control current, I_G, for the variable gain (ΔG) cell. The output of the ΔG cell is a current which is fed to the summing node of the operational amplifier. Resistors are provided to establish circuit gain and set the output DC bias.

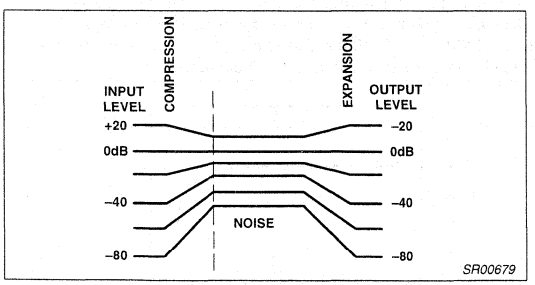


Figure 5. Restricted Dynamic Range Channel

The circuit is intended for use in single power supply systems, so the internal summing nodes must be biased at some voltage above ground. An internal band gap voltage reference provides a very stable, low noise 1.8V reference denoted V_{REF}. The non-inverting input of the op amp is tied to V_{REF}, and the summing nodes of the rectifier and ΔG cell (located at the right of R_1 and R_2) have the same potential. The THD trim pin is also at the V_{REF} potential.

Figure 7 shows how the circuit is hooked up to realize an expandor. The input signal, V_{IN}, is applied to the inputs of both the rectifier and the ΔG cell. When the input signal drops by 6dB, the gain control current will drop by a factor of 2, and so the gain will drop 6dB. The output level at V_{OUT} will thus drop 12dB, giving us the desired 2-to-1 expansion.

Figure 8 shows the hook-up for a compressor. This is essentially an expandor placed in the feedback loop of the op amp. The ΔG cell is setup to provide AC feedback only, so a separate DC feedback loop is provided by the two R_{DC} and C_{DC}. The values of R_{DC} will determine the DC bias at the output of the op amp. The output will bias to:

$$V_{OUT}\ DC = 1 + \frac{R_{DC1} + R_{DC2}}{R_4}$$

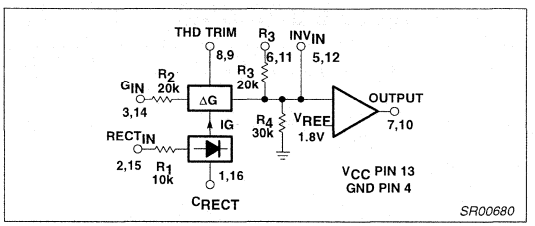


Figure 6. Chip Block Diagram (1 of 2 Channels)

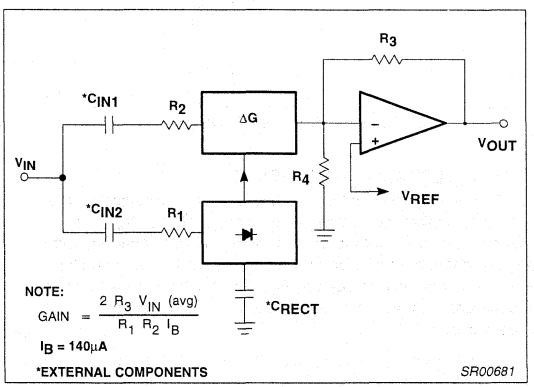


Figure 7. Basic Expander

$$V_{REF} = \left(1 + \frac{R_{DCTOT}}{30k}\right) 1.8V$$

The output of the expander will bias up to:

$$V_{OUT}\ DC = 1 + \frac{R_3}{R_4}\ V_{REF}$$

$$V_{REF} = \left(1 + \frac{20k}{30k}\right) 1.8V = 3.0V$$

The output will bias to 3.0V when the internal resistors are used. External resistors may be placed in series with R_3, (which will affect the gain), or in parallel with R_4 to raise the DC bias to any desired value.

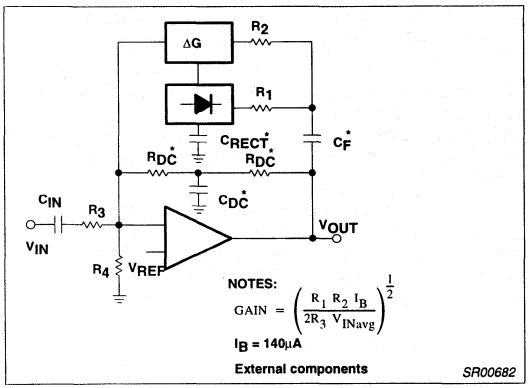


Figure 8. Basic Compressor

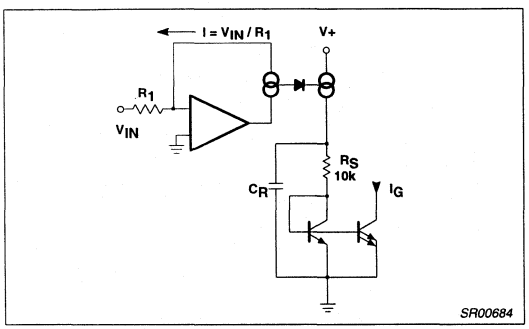


Figure 9. Rectifier Concept

CIRCUIT DETAILS—RECTIFIER

Figure 9 shows the concept behind the full-wave averaging rectifier. The input current to the summing node of the op amp, $V_{IN}R_1$, is supplied by the output of the op amp. If we can mirror the op amp output current into a unipolar current, we will have an ideal rectifier. The output current is averaged by R_S, CR, which set the averaging time constant, and then mirrored with a gain of 2 to become I_G, the gain control current.

Figure 10 shows the rectifier circuit in more detail. The op amp is a one-stage op amp, biased so that only one output device is on at a time. The non-inverting input, (the base of Q_1), which is shown grounded, is actually tied to the internal 1.8V V_{REF}. The inverting input is tied to the op amp output, (the emitters of Q_5 and Q_6), and the input summing resistor R_1. The single diode between the bases of Q_5 and Q_6 assures that only one device is on at a time. To detect the output current of the op amp, we simply use the collector currents of the output devices Q_5 and Q_6. Q_6 will conduct when the input swings positive and Q_5 conducts when the input swings negative. The collector currents will be in error by the *a* of Q_5 or Q_6 on negative or positive signal swings, respectively. ICs such as this have typical NPN βs of 200 and PNP βs of 40. The *a*'s of 0.995 and 0.975 will produce errors of 0.5% on negative swings and 2.5% on positive swings. The 1.5% average of these errors yields a mere 0.13dB gain error.

At very low input signal levels the bias current of Q_2, (typically 50nA), will become significant as it must be supplied by Q_5. Another low level error can be caused by DC coupling into the rectifier. If an offset voltage exists between the V_{IN} input pin and the base of Q_2, an error current of V_{OS}/R_1 will be generated. A mere 1mV of offset will cause an input current of 100nA which will produce twice the error of the input bias current. For highest accuracy, the rectifier should be coupled into capacitively. At high input levels the β of the PNP Q_6 will begin to suffer, and there will be an increasing error until the circuit saturates. Saturation can be avoided by limiting the current into the rectifier input to 250μA. If necessary, an external resistor may be placed in series with R_1 to limit the current to this value. Figure 11 shows the rectifier accuracy vs input level at a frequency of 1kHz.

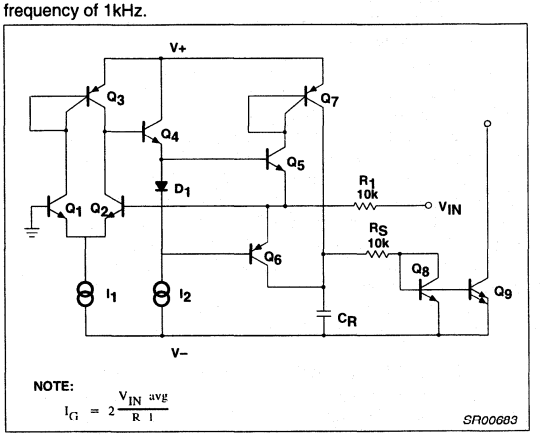


Figure 10. Simplified Rectifier Schematic

At very high frequencies, the response of the rectifier will fall off. The roll-off will be more pronounced at lower input levels due to the increasing amount of gain required to switch between Q_5 or Q_6 conducting. The rectifier frequency response for input levels of 0dBm, -20dBm, and -40dBm is shown in Figure 12. The response at all three levels is flat to well above the audio range.

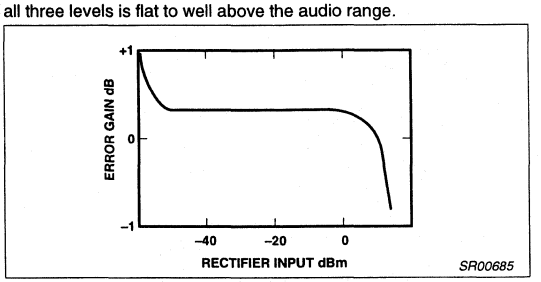


Figure 11. Rectifier Accuracy

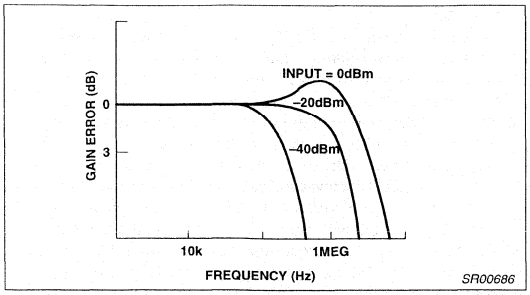


Figure 12. Rectifier Frequency Response vs Input Level

VARIABLE GAIN CELL

Figure 13 is a diagram of the variable gain cell. This is a linearized two-quadrant transconductance multiplier. Q_1, Q_2 and the op amp provide a predistorted drive signal for the gain control pair, Q_3 and Q_4. The gain is controlled by I_G and a current mirror provides the output current.

The op amp maintains the base and collector of Q_1 at ground potential (V_{REF}) by controlling the base of Q_2. The input current I_{IN} ($=V_{IN}/R_2$) is thus forced to flow through Q_1 along with the current I_1, so $I_{C1}=I_1+I_{IN}$. Since I_2 has been set at twice the value of I_1, the current through Q_2 is:

$I_2-(I_1+I_{IN})=I_1-I_{IN}=I_{C2}$.

The op amp has thus forced a linear current swing between Q_1 and Q_2 by providing the proper drive to the base of Q_2. This drive signal will be linear for small signals, but very non-linear for large signals, since it is compensating for the non-linearity of the differential pair, Q_1 and Q_2, under large signal conditions.

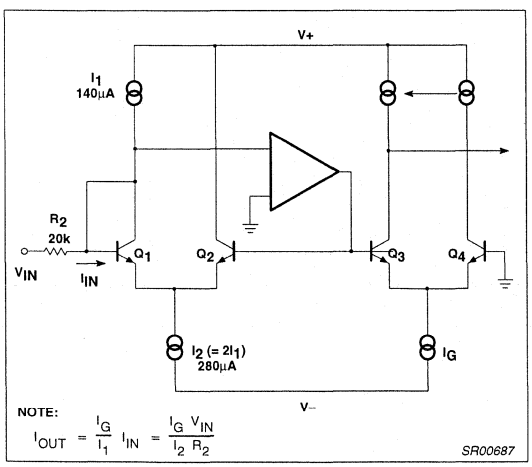


Figure 13. Simplified ΔG Cell Schematic

The key to the circuit is that this same predistorted drive signal is applied to the gain control pair, Q_3 and Q_4. When two differential pairs of transistors have the same signal applied, their collector current ratios will be identical regardless of the magnitude of the currents. This gives us:

$$\frac{I_{C1}}{I_{C2}} = \frac{I_{C4}}{I_{C3}} = \frac{I_1 + I_{IN}}{I_1 - I_{IN}}$$

plus the relationships $I_G=I_{C3}+I_{C4}$ and $I_{OUT}=I_{C4}-I_{C3}$ will yield the multiplier transfer function,

$$I_{OUT} = \frac{I_G}{I_1} I_{IN} = \frac{V_{IN} I_G}{R_2 I_1}$$

This equation is linear and temperature-insensitive, but it assumes ideal transistors.

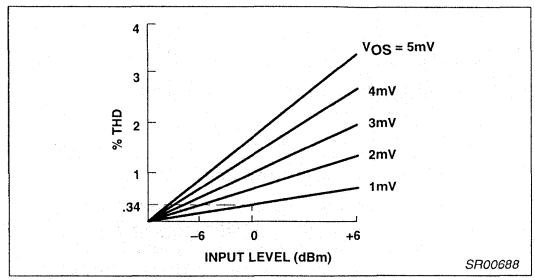


Figure 14. ΔG Cell Distortion vs Offset Voltage

If the transistors are not perfectly matched, a parabolic, non-linearity is generated, which results in second harmonic distortion. Figure 14 gives an indication of the magnitude of the distortion caused by a given input level and offset voltage. The distortion is linearly proportional to the magnitude of the offset and the input level. Saturation of the gain cell occurs at a +8dBm level. At a nominal operating level of 0dBm, a 1mV offset will yield 0.34% of second harmonic distortion. Most circuits are somewhat better than this, which means our overall offsets are typically about mV. The distortion is not affected by the magnitude of the gain control current, and it does not increase as the gain is changed. This second harmonic distortion could be eliminated by making perfect transistors, but since that would be difficult, we have had to resort to other methods. A trim pin has been provided to allow trimming of the internal offsets to zero, which effectively eliminated

second harmonic distortion. Figure 15 shows the simple trim network required.

Figure 16 shows the noise performance of the ΔG cell. The maximum output level before clipping occurs in the gain cell is plotted along with the output noise in a 20kHz bandwidth. Note that the noise drops as the gain is reduced for the first 20dB of gain reduction. At high gains, the signal to noise ratio is 90dB, and the total dynamic range from maximum signal to minimum noise is 110dB.

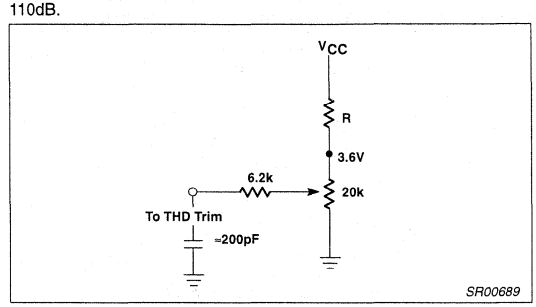


Figure 15. THD Trim Network

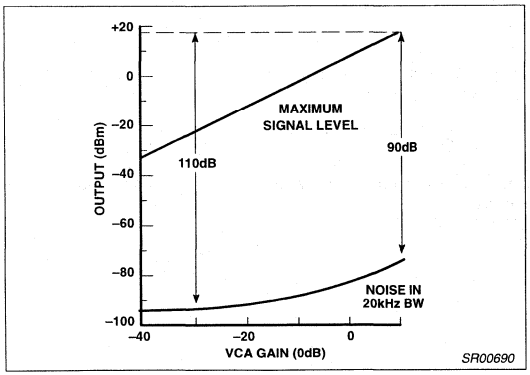


Figure 16. Dynamic Range

Control signal feedthrough is generated in the gain cell by imperfect device matching and mismatches in the current sources, I_1 and I_2. When no input signal is present, changing I_G will cause a small output signal. The distortion trim is effective in nulling out any control signal feedthrough, but in general, the null for minimum feedthrough will be different than the null in distortion. The control signal feedthrough can be trimmed independently of distortion by tying a current source to the ΔG input pin. This effectively trims I_1. Figure 17 shows such a trim network.

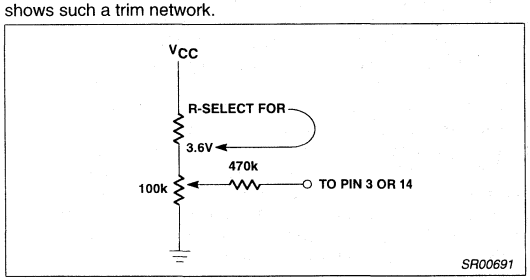


Figure 17. Control Signal Feedthrough

OPERATIONAL AMPLIFIER

The main op amp shown in the chip block diagram is equivalent to a 741 with a 1MHz bandwidth. Figure 18 shows the basic circuit. Split collectors are used in the input pair to reduce g_M, so that a small compensation capacitor of just 10pF may be used. The output stage, although capable of output currents in excess of 20mA, is biased for a low quiescent current to conserve power. When driving heavy loads, this leads to a small amount of crossover distortion.

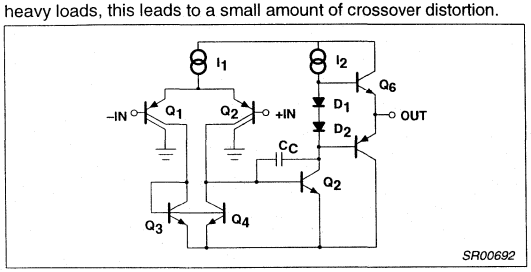


Figure 18. Operational Amplifier

RESISTORS

Inspection of the gain equations in Figures 7 and 8 will show that the basic compressor and expander circuit gains may be set entirely by resistor ratios and the internal voltage reference. Thus, any form of resistors that match well would suffice for these simple hook-ups, and absolute accuracy and temperature coefficient would be of no importance. However, as one starts to modify the gain equation with external resistors, the internal resistor accuracy and tempco become very significant. Figure 19 shows the effects of temperature on the diffused resistors which are normally used in integrated circuits, and the ion-implanted resistors which are used in this circuit. Over the critical 0°C to +70°C temperature range, there is a 10-to-1 improvement in drift from a 5% change for the diffused resistors, to a 0.5% change for the implemented resistors. The implanted resistors have another advantage in that they can be made the size of the diffused resistors due to the higher resistivity. This saves a significant amount of chip area.

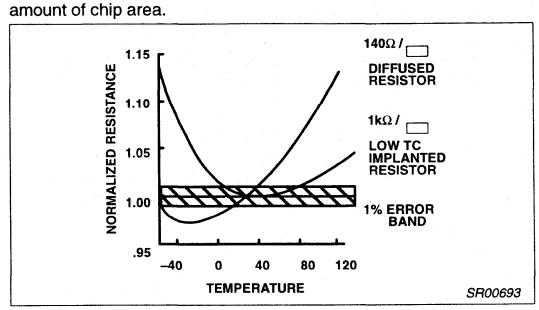


Figure 19. Resistance vs Temperature

Programmable analog compandor SA572

DESCRIPTION

The SA572 is a dual-channel, high-performance gain control circuit in which either channel may be used for dynamic range compression or expansion. Each channel has a full-wave rectifier to detect the average value of input signal, a linearized, temperature-compensated variable gain cell (ΔG) and a dynamic time constant buffer. The buffer permits independent control of dynamic attack and recovery time with minimum external components and improved low frequency gain control ripple distortion over previous compandors.

The SA572 is intended for noise reduction in high-performance audio systems. It can also be used in a wide range of communication systems and video recording applications.

FEATURES

- Independent control of attack and recovery time
- Improved low frequency gain control ripple
- Complementary gain compression and expansion with external op amp
- Wide dynamic range—greater than 110dB
- Temperature-compensated gain control
- Low distortion gain cell
- Low noise—6μV typical
- Wide supply voltage range—6V-22V
- System level adjustable with external components

PIN CONFIGURATION

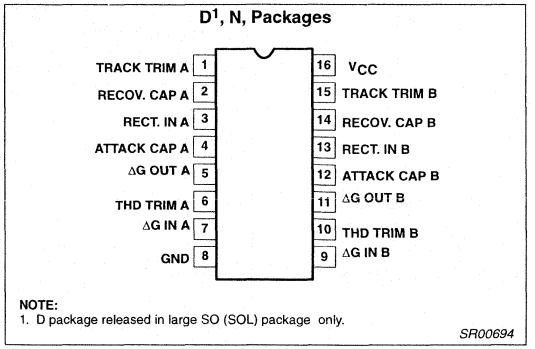


Figure 1. Pin Configuration

APPLICATIONS

- Dynamic noise reduction system
- Voltage control amplifier
- Stereo expandor
- Automatic level control
- High-level limiter
- Low-level noise gate
- State variable filter

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Small Outline (SO)	–40 to +85°C	SA572D	SOT109-1
16-Pin Plastic Dual In-Line Package (DIP)	–40 to +85°C	SA572N	SOT38-4

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	22	V_{DC}
T_A	Operating temperature range		
	SA572	–40 to +85	°C
P_D	Power dissipation	500	mW

BLOCK DIAGRAM

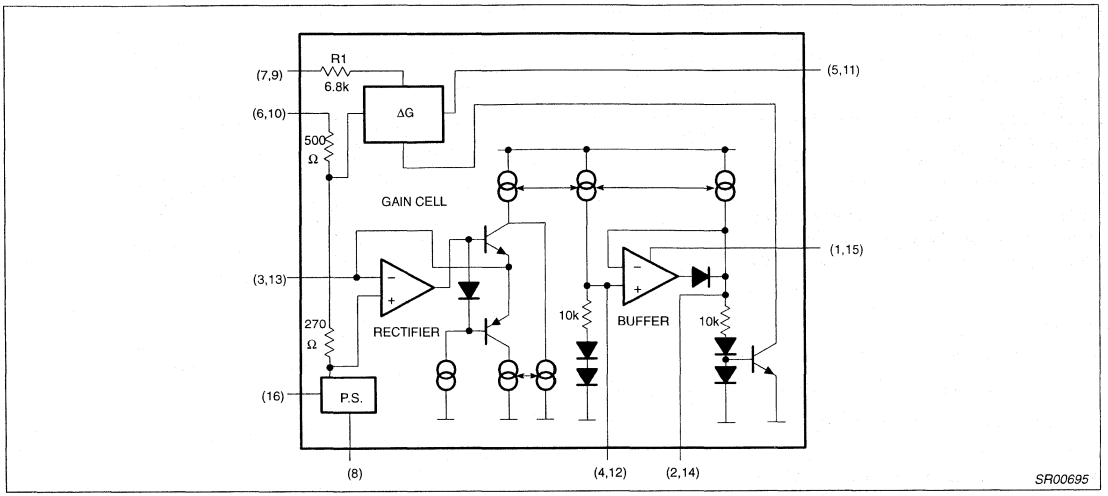


Figure 2. Block Diagram

DC ELECTRICAL CHARACTERISTICS

Standard test conditions (unless otherwise noted) V_{CC}=15V, T_A=25°C; Expandor mode (see Test Circuit). Input signals at unity gain level (0dB) = 100mV$_{RMS}$ at 1kHz; $V_1 = V_2$; R_2 = 3.3kΩ; R_3 = 17.3kΩ.

SYMBOL	PARAMETER	TEST CONDITIONS	SA572			UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage		6		22	V_{DC}
I_{CC}	Supply current	No signal			6.3	mA
V_R	Internal voltage reference		2.3	2.5	2.7	V_{DC}
THD	Total harmonic distortion (un-trimmed)	1kHz C_A=1.0μF		0.2	1.0	%
THD	Total harmonic distortion (trimmed)	1kHz C_R=10μF		0.05		%
THD	Total harmonic distortion (trimmed)	100Hz		0.25		%
	No signal output noise	Input to V_1 and V_2 grounded (20–20kHz)		6	25	μV
	DC level shift (untrimmed)	Input change from no signal to 100mV$_{RMS}$		±20	±50	mV
	Unity gain level		–1.5	0	+1.5	dB
	Large–signal distortion	V_1=V_2=400mV		0.7	3	%
	Tracking error (measured relative to value at unity gain)= [V_O–V_O (unity gain)]dB –V_2dB	Rectifier input V_2=+6dB V_1=0dB V_2=–30dB V_1=0dB		±0.2 ±0.5	 –2.5 +1.6	dB
	Channel crosstalk	200mV$_{RMS}$ into channel A, measured output on channel B	60			dB
PSRR	Power supply rejection ratio	120Hz		70		dB

TEST CIRCUIT

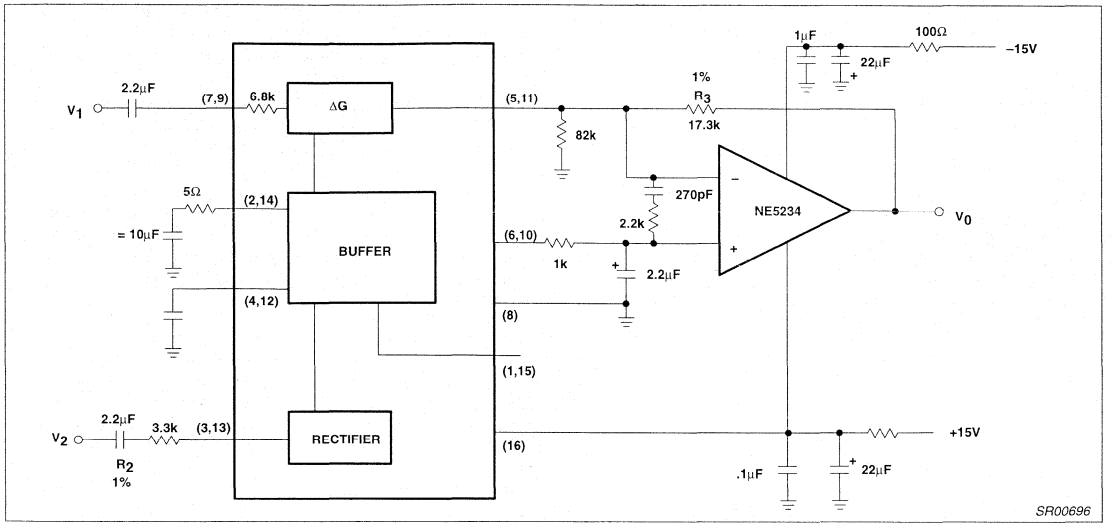


Figure 3. Test Circuit

AUDIO SIGNAL PROCESSING IC COMBINES VCA AND FAST ATTACK/SLOW RECOVERY LEVEL SENSOR

In high-performance audio gain control applications, it is desirable to independently control the attack and recovery time of the gain control signal. This is true, for example, in compandor applications for noise reduction. In high end systems the input signal is usually split into two or more frequency bands to optimize the dynamic behavior for each band. This reduces low frequency distortion due to control signal ripple, phase distortion, high frequency channel overload and noise modulation. Because of the expense in hardware, multiple band signal processing up to now was limited to professional audio applications.

With the introduction of the Signetics SA572 this high-performance noise reduction concept becomes feasible for consumer hi fi applications. The SA572 is a dual channel gain control IC. Each channel has a linearized, temperature-compensated gain cell and an improved level sensor. In conjunction with an external low noise op amp for current-to-voltage conversion, the VCA features low distortion, low noise and wide dynamic range.

The novel level sensor which provides gain control current for the VCA gives lower gain control ripple and independent control of fast attack, slow recovery dynamic response. An attack capacitor C_A with an internal 10k resistor R_A defines the attack time t_A. The recovery time t_R of a tone burst is defined by a recovery capacitor C_R and an internal 10k resistor R_R. Typical attack time of 4ms for the high-frequency spectrum and 40ms for the low frequency band can be obtained with 0.1μF and 1.0μF attack capacitors, respectively. Recovery time of 200ms can be obtained with a 4.7μF recovery capacitor for a 100Hz signal, the third harmonic distortion is improved by more than 10dB over the simple RC ripple filter with a single 1.0μF attack and recovery capacitor, while the attack time remains the same.

The SA572 is assembled in a standard 16-pin dual in-line plastic package and in oversized SOL package. It operates over a wide supply range from 6V to 22V. Supply current is less than 6mA. The SA572 is designed for applications from –40°C to +85°C.

SA572 BASIC APPLICATIONS

Description

The SA572 consists of two linearized, temperature-compensated gain cells (ΔG), each with a full-wave rectifier and a buffer amplifier as shown in the block diagram. The two channels share a 2.5V common bias reference derived from the power supply but otherwise operate independently. Because of inherent low distortion, low noise and the capability to linearize large signals, a wide dynamic range can be obtained. The buffer amplifiers are provided to permit control of attack time and recovery time independent of each other. Partitioned as shown in the block diagram, the IC allows flexibility in the design of system levels that optimize DC shift, ripple distortion, tracking accuracy and noise floor for a wide range of application requirements.

Gain Cell

Figure 4 shows the circuit configuration of the gain cell. Bases of the differential pairs Q_1-Q_2 and Q_3-Q_4 are both tied to the output and inputs of OPA A_1. The negative feedback through Q_1 holds the V_{BE} of Q_1-Q_2 and the V_{BE} of Q_3-Q_4 equal. The following relationship can be derived from the transistor model equation in the forward active region.

$\Delta V_{BE_{Q3Q4}}$ $\Delta_{BE_{Q1Q2}}$

($V_{BE} = V_T I_{IN} IC/IS$)

$V_T I_n \frac{\frac{1}{2}I_G \pm \frac{1}{2}I_O}{I_S}$ $V_T I_n \frac{\frac{1}{2}I_G \frac{1}{2}I_O}{I_S}$

where $I_{IN} \frac{V_{IN}}{R_1}$

$R_1 = 6.8k\Omega$
$I_1 = 140\mu A$
$I_2 = 280\mu A$

$V_T I_n \frac{I_1 \pm I_{IN}}{I_S}$ $V_T I_n \frac{I_2 I_1 I_{IN}}{I_S}$ (2)

where $I_{IN} \frac{V_{IN}}{R_1}$

$R_1 = 6.8k\Omega$
$I_1 = 140\mu A$
$I_2 = 280\mu A$

I_O is the differential output current of the gain cell and I_G is the gain control current of the gain cell.

If all transistors Q_1 through Q_4 are of the same size, equation (2) can be simplified to:

$I_O \frac{2}{I_2} I_{IN} I_G \frac{1}{I_2} I_2 2I_1 I_G$ (3)

The first term of Equation 3 shows the multiplier relationship of a linearized two quadrant transconductance amplifier. The second term is the gain control feedthrough due to the mismatch of devices.

In the design, this has been minimized by large matched devices and careful layout. Offset voltage is caused by the device mismatch and it leads to even harmonic distortion. The offset voltage can be trimmed out by feeding a current source within ±25μA into the THD trim pin.

The residual distortion is third harmonic distortion and is caused by gain control ripple. In a compandor system, available control of fast attack and slow recovery improve ripple distortion significantly. At the unity gain level of 100mV, the gain cell gives THD (total harmonic distortion) of 0.17% typ. Output noise with no input signals is only 6μV in the audio spectrum (10Hz-20kHz). The output current I_O must feed the virtual ground input of an operational amplifier with a resistor from output to inverting input. The non-inverting input of the operational amplifier has to be biased at V_{REF} if the output current I_O is DC coupled.

Rectifier

The rectifier is a full-wave design as shown in Figure 5. The input voltage is converted to current through the input resistor R_2 and turns on either Q_5 or Q_6 depending on the signal polarity. Deadband of the voltage to current converter is reduced by the loop gain of the gain block A_2. If AC coupling is used, the rectifier error comes only from input bias current of gain block A_2. The input bias current is typically about 70nA. Frequency response of the gain block A_2 also causes second-order error at high frequency. The collector current of Q_6 is mirrored and summed at the collector of Q_5 to form the full wave rectified output current I_R. The rectifier transfer function is

$I_R \frac{V_{IN} V_{REF}}{R_2}$ (4)

If V_{IN} is AC-coupled, then the equation will be reduced to:

$I_{RAC} \frac{V_{IN}(AVG)}{R_2}$

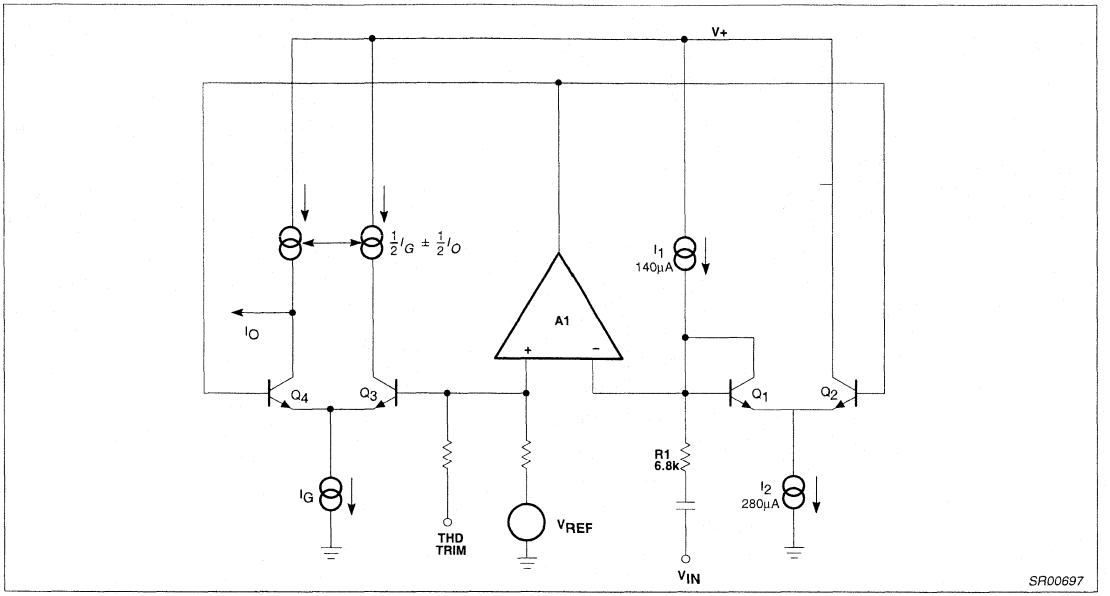


Figure 4. Basic Gain Cell Schematic

The internal bias scheme limits the maximum output current I_R to be around 300µA. Within a ±1dB error band the input range of the rectifier is about 52dB.

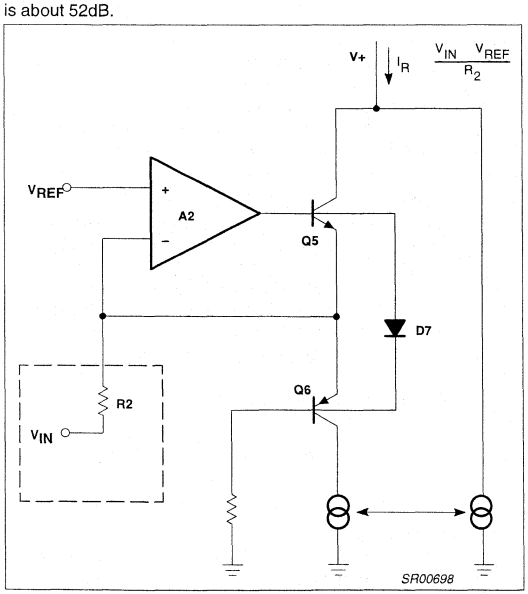


Figure 5. Simplified Rectifier Schematic

Buffer Amplifier

In audio systems, it is desirable to have fast attack time and slow recovery time for a tone burst input. The fast attack time reduces transient channel overload but also causes low-frequency ripple distortion. The low-frequency ripple distortion can be improved with the slow recovery time. If different attack times are implemented in corresponding frequency spectrums in a split band audio system, high quality performance can be achieved. The buffer amplifier is designed to make this feature available with minimum external components. Referring to Figure 6, the rectifier output current is mirrored into the input and output of the unipolar buffer amplifier A_3 through Q_8, Q_9 and Q_{10}. Diodes D_{11} and D_{12} improve tracking accuracy and provide common-mode bias for A_3. For a positive-going input signal, the buffer amplifier acts like a voltage-follower. Therefore, the output impedance of A_3 makes the contribution of capacitor CR to attack time insignificant. Neglecting diode impedance, the gain Ga(t) for ΔG can be expressed as follows:

$$Ga(t) \quad (Ga_{INT} \quad Ga_{FNL}\, e^{\frac{-t}{A}} \pm Ga_{FNL}$$

Ga_{INT}=Initial Gain

Ga_{FNL}=Final Gain

$\tau_A = R_A \bullet CA = 10k \bullet CA$

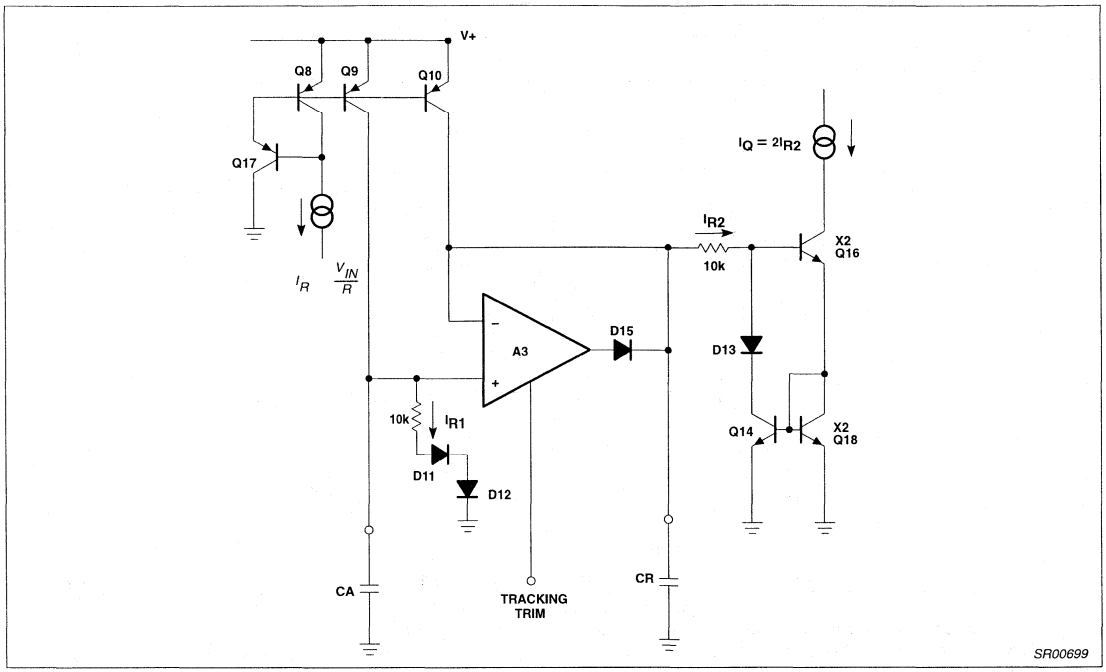


Figure 6. Buffer Amplifier Schematic

where τ_A is the attack time constant and R_A is a 10k internal resistor. Diode D_{15} opens the feedback loop of A_3 for a negative-going signal if the value of capacitor CR is larger than capacitor CA. The recovery time depends only on CR • R_R. If the diode impedance is assumed negligible, the dynamic gain G_R (t) for ΔG is expressed as follows.

$$G_R(t) \quad (G_{RINT} \quad G_{RFNL}\, e^{\frac{-t}{R}} \pm G_{RFNL}$$

$$G_R(t)=(G_{R\,INT}-G_{R\,FNL})\, e +G_{R\,FNL}$$

$$\tau R=R_R \bullet CR=10k \bullet CR$$

where τR is the recovery time constant and R_R is a 10k internal resistor. The gain control current is mirrored to the gain cell through Q_{14}. The low level gain errors due to input bias current of A_2 and A_3 can be trimmed through the tracking trim pin into A_3 with a current source of ±3µA.

Basic Expandor

Figure 7 shows an application of the circuit as a simple expandor. The gain expression of the system is given by

$$\frac{V_{OUT}}{V_{IN}} \quad \frac{2}{I_1} \quad \frac{R_3}{R_2} \quad \frac{V_{IN(AVG)}}{R_1} \qquad (5)$$

(I_1=140µA)

Both the resistors R_1 and R_2 are tied to internal summing nodes. R_1 is a 6.8k internal resistor. The maximum input current into the gain cell can be as large as 140µA. This corresponds to a voltage level of 140µA • 6.8k=952mV peak. The input peak current into the rectifier is limited to 300µA by the internal bias system. Note that the value of R_1 can be increased to accommodate higher input level. R_2 and R_3 are external resistors. It is easy to adjust the ratio of R_3/R_2 for desirable system voltage and current levels. A small R_2 results in higher gain control current and smaller static and dynamic tracking error. However, an impedance buffer A_1 may be necessary if the input is voltage drive with large source impedance.

The gain cell output current feeds the summing node of the external OPA A_2. R_3 and A_2 convert the gain cell output current to the output voltage. In high-performance applications, A_2 has to be low-noise, high-speed and wide band so that the high-performance output of the gain cell will not be degraded. The non-inverting input of A_2 can be biased at the low noise internal reference Pin 6 or 10. Resistor R_4 is used to bias up the output DC level of A_2 for maximum swing. The output DC level of A_2 is given by

$$V_{ODC} \quad V_{REF}\ 1 \pm \frac{R_3}{R_4} \quad V_B \frac{R_3}{R_4} \qquad (6)$$

V_B can be tied to a regulated power supply for a dual supply system and be grounded for a single supply system. CA sets the attack time constant and CR sets the recovery time constant. *5COL

Basic Compressor

Figure 8 shows the hook-up of the circuit as a compressor. The IC is put in the feedback loop of the OPA A_1. The system gain expression is as follows:

$$\frac{V_{OUT}}{V_{IN}} \quad \frac{I_1}{2} \quad \frac{R_2}{R_3}\frac{R_1}{V_{IN(AVG)}}^{\frac{1}{2}} \qquad (7)$$

R_{DC1}, R_{DC2}, and CDC form a DC feedback for A_1. The output DC level of A_1 is given by

$$V_{ODC} \quad V_{REF}\ 1 \pm \frac{R_{DC1} \pm R_{DC2}}{R_4} \qquad (8)$$

$$V_B \quad \frac{R_{DC1} \pm R_{DC2}}{R_4}$$

The zener diodes D_1 and D_2 are used for channel overload protection.

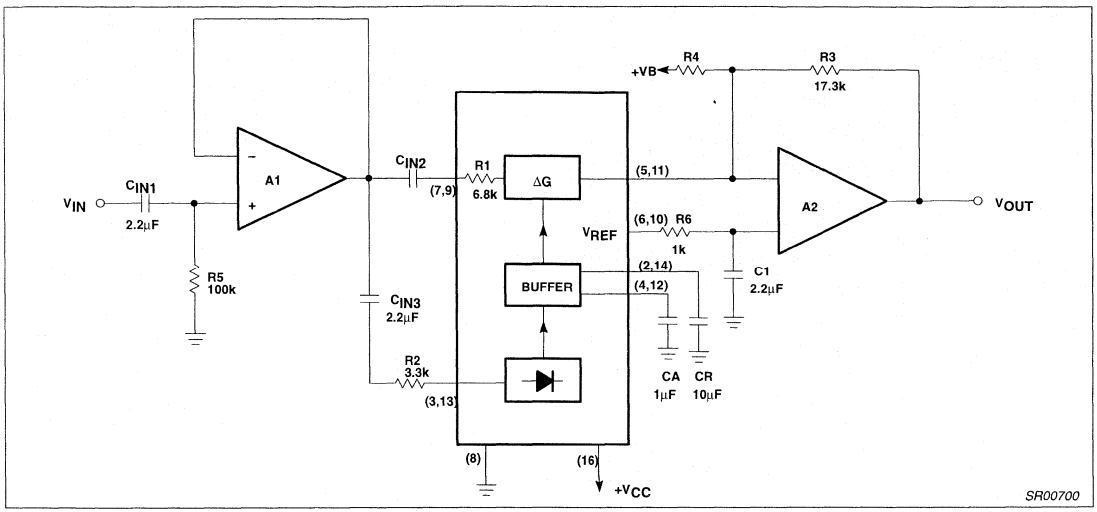


Figure 7. Basic Expandor Schematic

Basic Compandor System

The above basic compressor and expandor can be applied to systems such as tape/disc noise reduction, digital audio, bucket brigade delay lines. Additional system design techniques such as bandlimiting, band splitting, pre-emphasis, de-emphasis and equalization are easy to incorporate. The IC is a versatile functional block to achieve a high performance audio system. Figure 9 shows the system level diagram for reference.

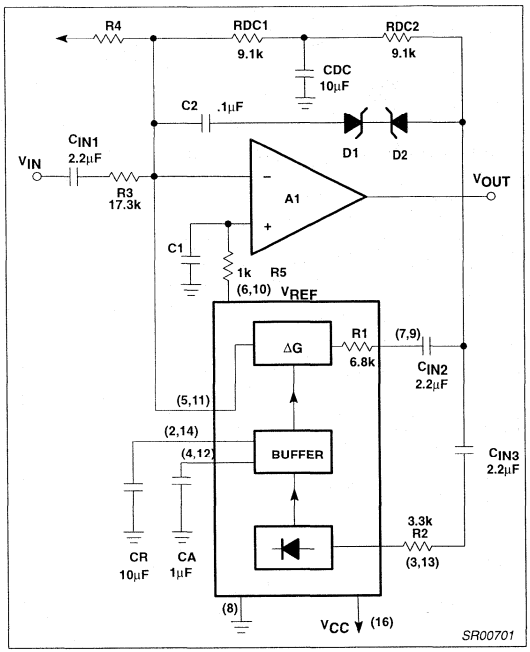


Figure 8. Basic Compressor Schematic

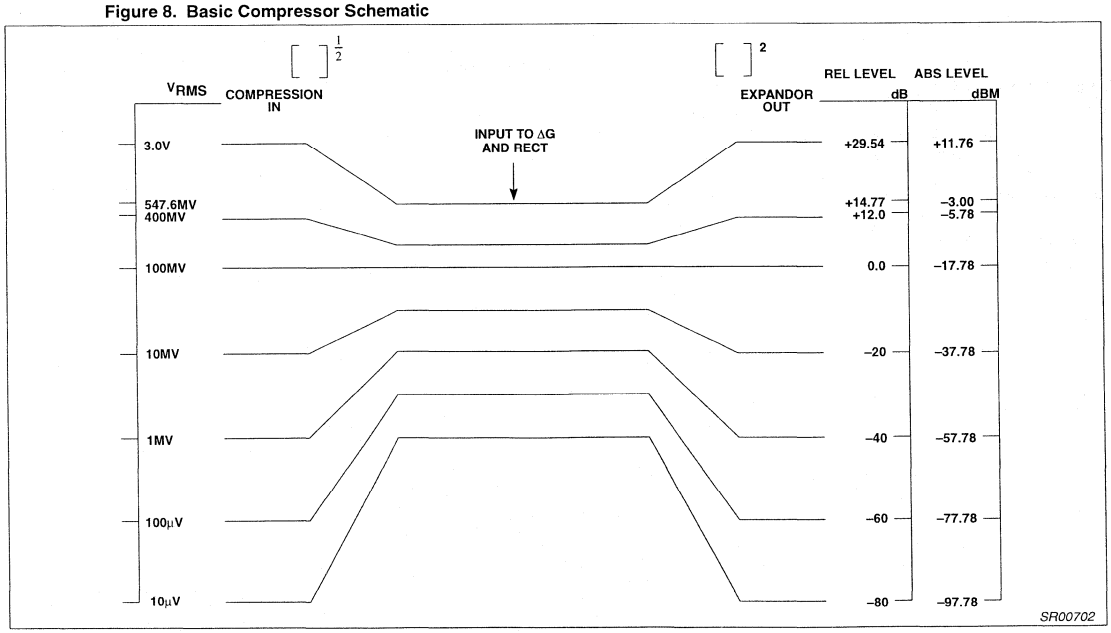


Figure 9. SA572 System Level

Low voltage compandor SA575

DESCRIPTION

The SA575 is a precision dual gain control circuit designed for low voltage applications. The SA575's channel 1 is an expandor, while channel 2 can be configured either for expandor, compressor, or automatic level controller (ALC) application.

FEATURES

- Operating voltage range from 3V to 7V
- Reference voltage of 100mV$_{RMS}$ = 0dB
- One dedicated summing op amp per channel and two extra uncommitted op amps
- 600Ω drive capability
- Single or split supply operation
- Wide input/output swing capability
- 3000V ESD protection

APPLICATIONS

- Portable communications
- Cellular radio
- Cordless telephone
- Consumer audio
- Portable broadcast mixers
- Wireless microphones
- Modems
- Electric organs
- Hearing aids

PIN CONFIGURATION

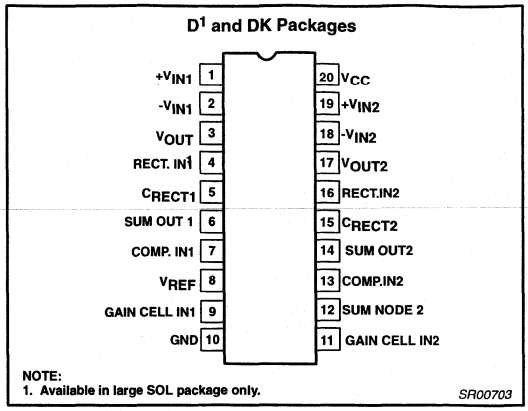


Figure 1. Pin Configuration

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG
20-Pin Plastic Small Outline Large	-40 to +85°C	SA575D	SOT163-1
20-Pin Plastic Shrink Small Outline Package (SSOP)	-40 to +85°C	SA575DK	SOT266-1

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING SA575	UNITS
V_{CC}	Single supply voltage	–0.3 to 8	V
V_{IN}	Voltage applied to any other pin	–0.3 to (V_{CC}+0.3)	V
T_A	Operating ambient temperature range	-40 to +85	°C
T_{STG}	Storage temperature range	-65 to +150	°C
θ_{JA}	Thermal impedance SOL	112	°C/W
	Thermal impedance SSOP	117	°C/W

BLOCK DIAGRAM and TEST CIRCUIT

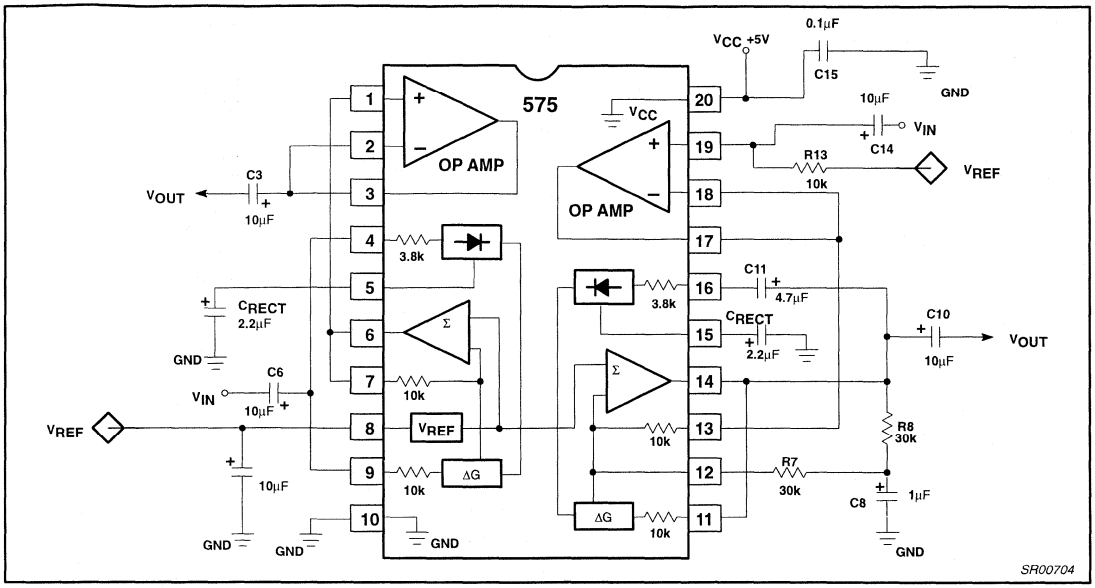


Figure 2. Block Diagram and Test Circuit

DC ELECTRICAL CHARACTERISTICS

Typical values are at T_A = 25°C. Minimum and Maximum values are for the full operating temperature range: -40 to +85°C for SA575, except SSOP package is tested at +25°C only. V_{CC} = 5V, unless otherwise stated. Both channels are tested in the Expandor mode (see Test Circuit)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA575			
			MIN	TYP	MAX	
For compandor, including summing amplifier						
V_{CC}	Supply voltage[1]		3	5	7	V
I_{CC}	Supply current	No signal	3	4.2	5.5	mA
V_{REF}	Reference voltage[2]	V_{CC} = 5V	2.4	2.5	2.6	V
R_L	Summing amp output load		10			kΩ
THD	Total harmonic distortion	1kHz, 0dB BW = 3.5kHz		0.12	1.5	%
E_{NO}	Output voltage noise	BW = 20kHz, R_S = 0Ω		6	30	µV
0dB	Unity gain level	1kHz	-1.5		1.5	dB
V_{OS}	Output voltage offset	No signal	-150		150	mV
	Output DC shift	No signal to 0dB	-100		100	mV
	Tracking error relative to 0dB	Gain cell input = 0dB, 1kHz Rectifier input = 6dB, 1kHz	-1.0		1.0	dB
		Gain cell input = 0dB, 1kHz Rectifier input = -30dB, 1kHz	-1.0		1.0	dB

DC ELECTRICAL CHARACTERISTICS (cont.)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS SA575 MIN	LIMITS SA575 TYP	LIMITS SA575 MAX	UNITS
	Crosstalk	1kHz, 0dB, C_{REF} = 220µF		-80	-65	dB
For operational amplifier						
V_O	Output swing	R_L = 10kΩ	V_{CC}-0.4	V_{CC}		V
R_L	Output load	1kHz	600			Ω
CMR	Input common-mode range		0		V_{CC}	V
CMRR	Common-mode rejection ratio		60	80		dB
I_B	Input bias current	V_{IN} = 0.5V to 4.5V	-1		1	µA
V_{OS}	Input offset voltage			3		mV
A_{VOL}	Open-loop gain	R_L = 10kΩ		80		dB
SR	Slew rate	Unity gain		1		V/µs
GBW	Bandwidth	Unity gain		3		MHz
E_{NI}	Input voltage noise	BW = 20kHz		2.5		µV
PSRR	Power supply rejection ratio	1kHz, 250mV		60		dB

NOTES:
1. Operation down to V_{CC} = 2V is possible, but performance is reduced. See curves in Figure 7a and 7b.
2. Reference voltage, V_{REF}, is typically at 1/2V_{CC}.

FUNCTIONAL DESCRIPTION

This section describes the basic subsystems and applications of the SA575 Compandor. More theory of operation on compandors can be found in AN174 and AN176. The typical applications of the SA575 low voltage compandor in an Expandor (1:2), Compressor (2:1) and Automatic Level Control (ALC) function are explained. These three circuit configurations are shown in Figures 3, 4, 5 respectively.

The SA575 has two channels for a complete companding system. The left channel, A, can be configured as a 1:2 Expandor while the right channel, B, can be configured as either a 2:1 Compressor, a 1:2 Expandor or an ALC. Each channel consists of the basic companding building blocks of rectifier cell, variable gain cell, summing amplifier and V_{REF} cell. In addition, the SA575 has two additional high performance uncommitted op amps which can be utilized for application such as filtering, pre-emphasis/de-emphasis or buffering.

Figure 6 shows the complete schematic for the applications demo board. Channel A is configured as an expandor while channel B is configured so that it can be used either as a compressor or as an ALC circuit. The switch, S1, toggles the circuit between compressor and ALC mode. Jumpers J1 and J2 can be used to either include the additional op amps for signal conditioning or exclude them from the signal path. Bread boarding space is provided for R1, R2, C1, C2, R10, R11, C10 and C11 so that the response can be tailored for each individual need. The components as specified are suitable for the complete audio spectrum from 20Hz to 20kHz.

The most common configuration is as a unity gain non-inverting buffer where R1, C1, C2, R10, C10 and C11 are eliminated and R2 and R11 are shorted. Capacitors C3, C5, C8, and C12 are for DC blocking. In systems where the inputs and outputs are AC coupled, these capacitors and resistors can be eliminated. Capacitors C4 and C9 are for setting the attack and release time constant.

C6 is for decoupling and stabilizing the voltage reference circuit. The value of C6 should be such that it will offer a very low impedance to the lowest frequencies of interest. Too small a capacitor will allow supply ripple to modulate the audio path. The better filtered the power supply, the smaller this capacitor can be. R12 provides DC reference voltage to the amplifier of channel B. R6 and R7 provide a DC feedback path for the summing amp of channel B, while C7 is a short-circuit to ground for signals. C14 and C15 are for power supply decoupling. C14 can also be eliminated if the power supply is well regulated with very low noise and ripple.

DEMONSTRATED PERFORMANCE

The applications demo board was built and tested for a frequency range of 20Hz to 20kHz with the component values as shown in Figure 6 and V_{CC} = 5V. In the expandor mode, the typical input dynamic range was from -34dB to +12dB where 0dB is equal to 100mV_{RMS}. The typical unity gain level measured at 0dB @ 1kHz input was ±0.5dB and the typical tracking error was ±0.1dB for input range of -30 to +10dB.

In the compressor mode, the typical input dynamic range was from -42dB to ±18dB with a tracking error +0.1dB and the typical unity gain level was ±0.5dB.

In the ALC mode, the typical input dynamic range was from -42dB to +8dB with typical output deviation of ±0.2dB about the nominal output of 0dB. For input greater than +9dB in ALC configuration, the summing amplifier sometimes exhibits high frequency oscillations. There are several solutions to this problem. The first is to lower the values of R6 and R7 to 20kΩ each. The second is to add a current limiting resistor in series with C12 at Pin 13. The third is to add a compensating capacitor of about 22 to 30pF between the input and output of summing amplifier (Pins 12 and 14). With any one of the above recommendations, the typical ALC mode input range increased to +18dB yielding a dynamic range of over 60dB.

EXPANDOR

The typical expandor configuration is shown in Figure 3. The variable gain cell and the rectifier cell are in the signal input path. The V_{REF} is always 1/2 V_{CC} to provide the maximum headroom without clipping. The 0dB ref is 100mV_{RMS}. The input is AC coupled through C5, and the output is AC coupled through C3. If in a system the inputs and outputs are AC coupled, then C3 and C5 can be eliminated, thus requiring only one external component, C4. The variable gain cell and rectifier cell are DC coupled so any offset

voltage between Pins 4 and 9 will cause small offset error current in the rectifier cell. This will affect the accuracy of the gain cell. This can be improved by using an extra capacitor from the input to Pin 4 and eliminating the DC connection between Pins 4 and 9.
The expandor gain expression and the attack and release time constant is given by Equation 1 and Equation 2, respectively.

Equation 1.

$$\text{Expandor gain} = \frac{4V_{IN}(avg)}{3.8k \times 100\mu A}$$

where $V_{IN}(avg) = 0.95V_{IN(RMS)}$

Equation 2.

$$\tau_R = \tau_A = 10k \times C_{RECT} = 10k \times C4$$

COMPRESSOR

The typical compressor configuration is shown in Figure 4. In this mode, the rectifier cell and variable gain cell are in the feedback path. R6 and R7 provide the DC feedback to the summing amplifier. The input is AC coupled through C12 and output is AC coupled through C8. In a system with inputs and outputs AC coupled, C8 and C12 could be eliminated and only R6, R7, C7, and C13 would be required. If the external components R6, R7 and C7 are eliminated, then the output of the summing amplifier will motor-boat in absence of signals or at extremely low signals. This is because there is no DC feedback path from the output to input. In the presence of an AC signal this phenomenon is not observed and the circuit will appear to function properly.
The compressor gain expression and the attack and release time constant is given by Equation 3 and Equation 4, respectively.

Equation 3.

$$\text{Compressor gain} = \left[\frac{3.8k \times 100\mu A}{4V_{IN}(avg)}\right]^{1/2}$$

where $V_{IN}(avg) = 0.95V_{IN(RMS)}$

Equation 4.

$$\tau_R = \tau_A = 10k \times C_{RECT} = 10k \times C4$$

AUTOMATIC LEVEL CONTROL

The typical Automatic Level Control circuit configuration is shown in Figure 5. It can be seen that it is quite similar to the compressor schematic except that the input to the rectifier cell is from the input path and not from the feedback path. The input is AC coupled through C12 and C13 and the output is AC coupled through C8. Once again, as in the previous cases, if the system input and output signals are already AC coupled, then C12, C13 and C8 could be eliminated. Concerning the compressor, removing R6, R7 and C7 will cause motor-boating in absence of signals. C_{COMP} is necessary to stabilize the summing amplifier at higher input levels. This circuit provides an input dynamic range greater than 60dB with the output within ±0.5dB typical. The necessary design expressions are given by Equation 5 and Equation 6, respectively.

Equation 5.

$$\text{ALC gain} = \frac{3.8k \times 100\mu A}{4V_{IN}(avg)}$$

Equation 6.

$$\tau_R = \tau_A = 10k \times C_{RECT} = 10k \times C9$$

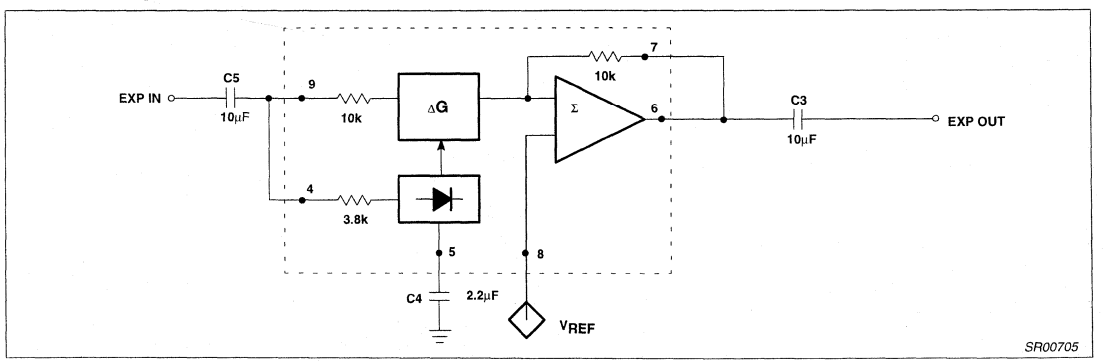


Figure 3. Typical Expandor Configuration

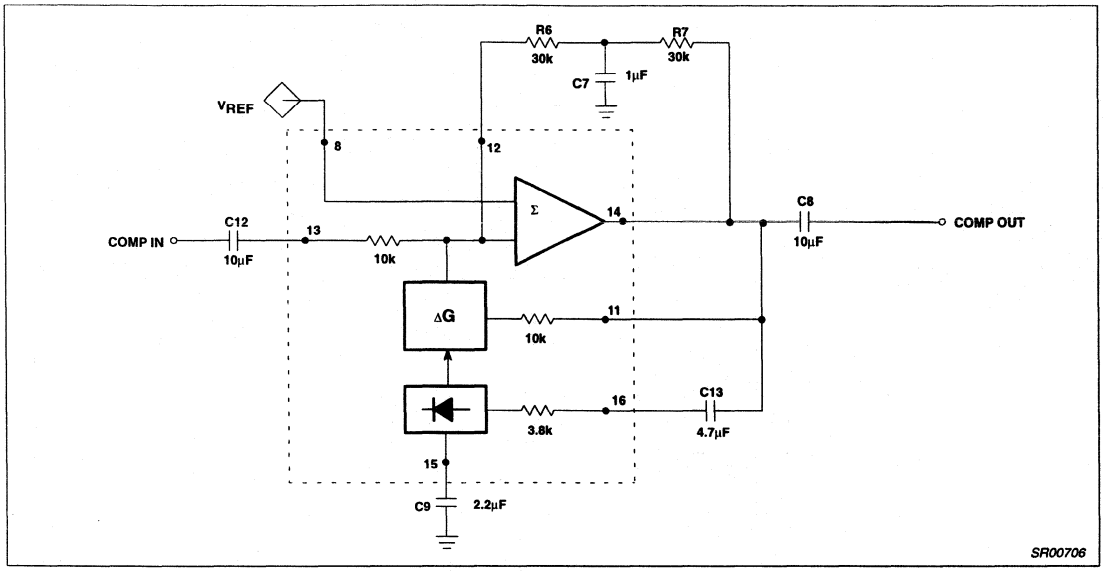


Figure 4. Typical Compressor Configuration

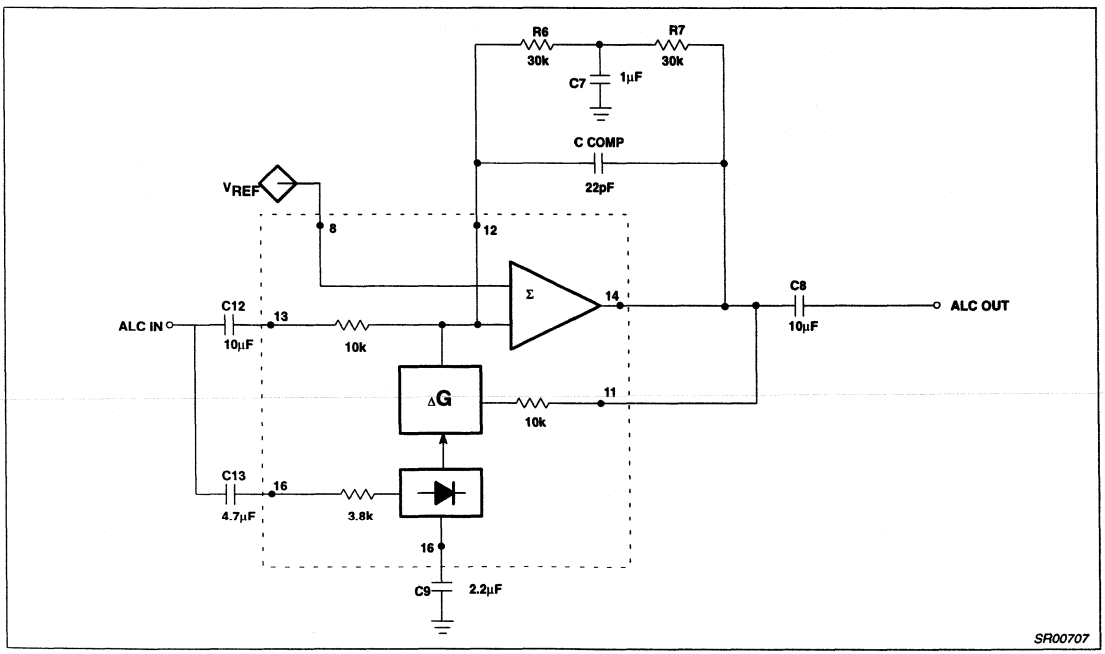


Figure 5. Typical ALC Configuration

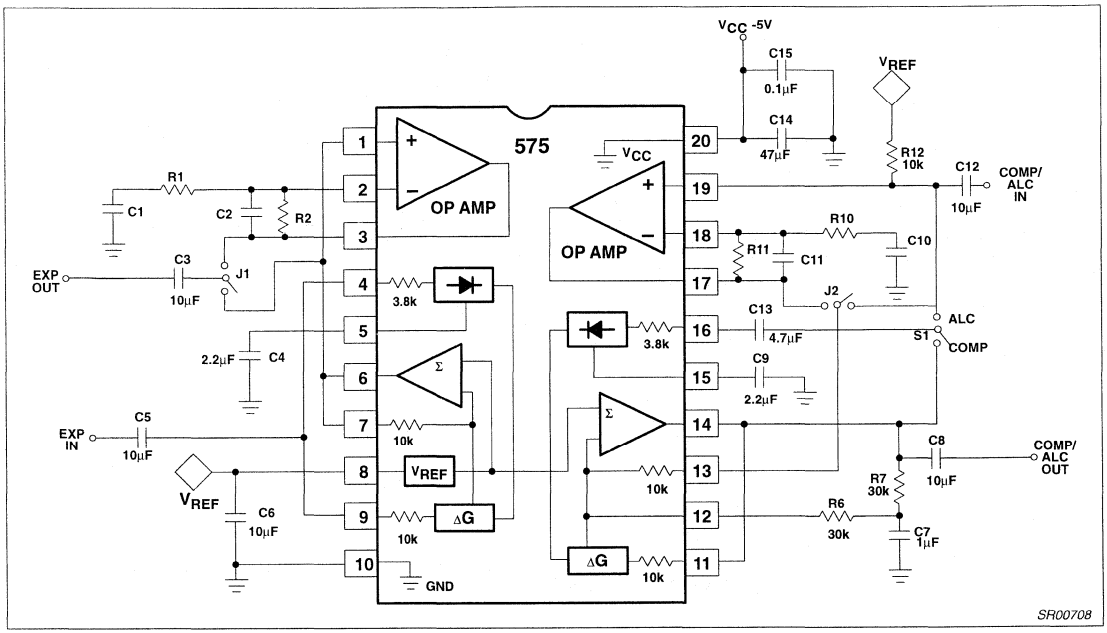


Figure 6. SA575 Low Voltage Expandor/Compressor/ALC Demo Board

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

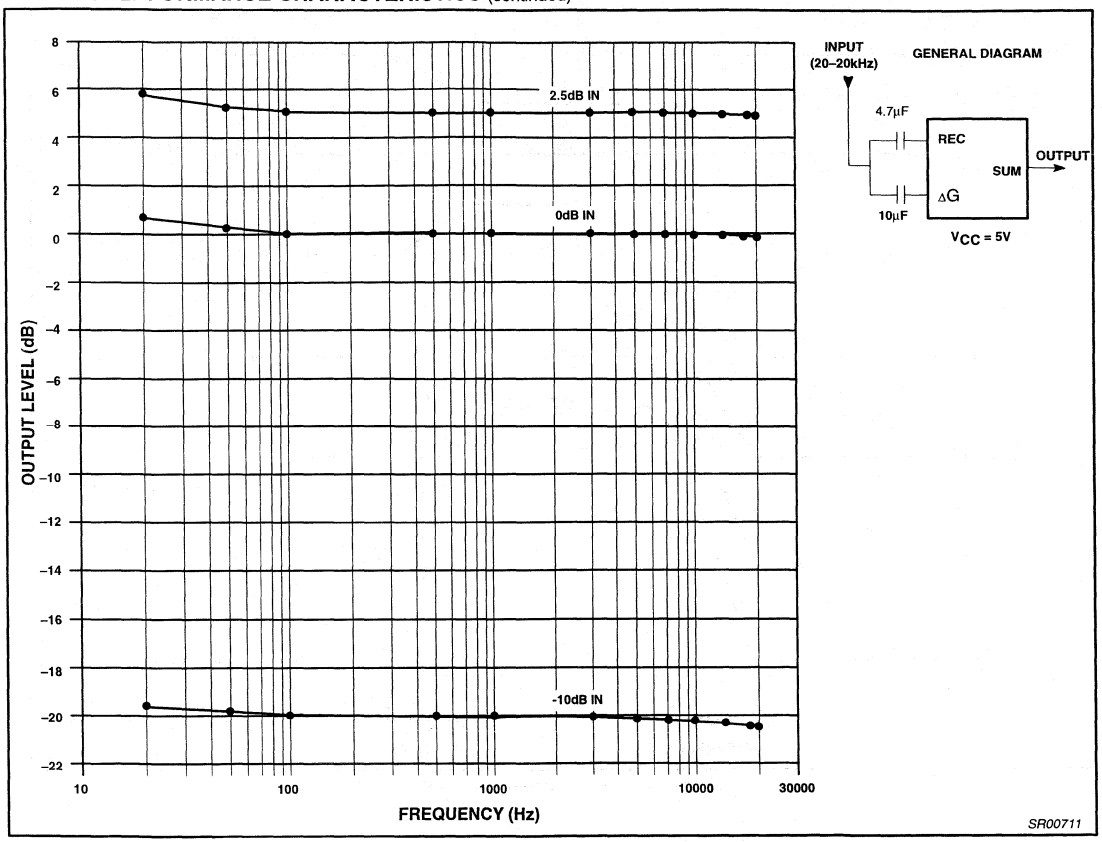


Figure 9. Expandor Output Frequency Response

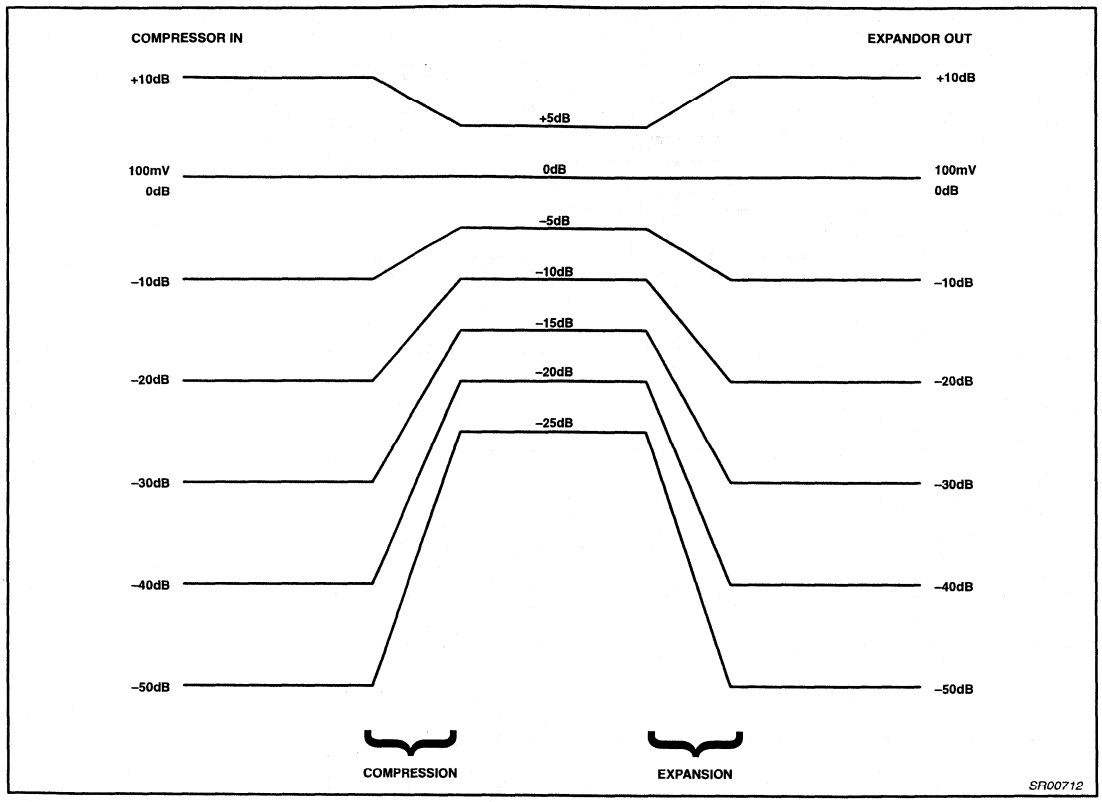


Figure 10. The Companding Function

Low power compandor SA576

DESCRIPTION

The SA576 is a unity gain level programmable compandor designed for low power applications. The SA576 is internally configured as an expandor and a compressor to minimize external component count.

The SA576 can operate at 1.8V. During normal operations, the SA576 can operate from at least a 2V battery. If the battery voltage drops to 1.8V, this part will still continue to function, however, turning on the part at a V_{CC} of 1.8V requires two external resistors to bring V_{REF} to half V_{CC}. One resistor connects between V_{CC} and V_{REF}; the other connects from V_{REF} to ground. A typical value for these external resistors is approximately 20k. A lower value can be used, but the power consumption will go up.

The SA576 is available in a 14-pin plastic DIP and SO packages.

FEATURES

- Operating voltage range: 1.8V to 7V
- Low power consumption (1.4mA @ 3.6V)
- Over 80dB of dynamic range
- Wide input/output swing capability (rail-to-rail)
- Low external component count
- ESD hardened

PIN CONFIGURATION

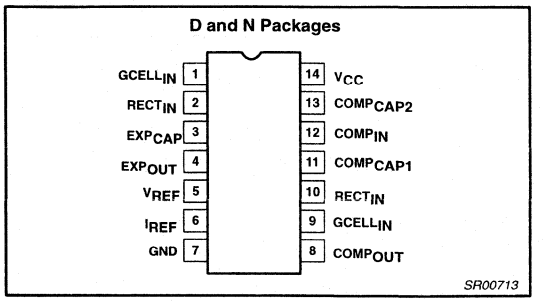


Figure 1. Pin Configuration

APPLICATIONS

- Cordless telephone
- Consumer audio
- Wireless microphones
- Modems
- Electric organs
- Hearing aids
- Automatic level control

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
14-Pin Plastic Dual In-Line Package (DIP)	–40 to +85°C	SA576N	SOT27-1
14-Pin Plastic Small Outline (SO)	–40 to +85°C	SA576D	SOT108-1

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
		SA576	
V_{CC}	Supply voltage	8	V
T_A	Operating ambient temperature range	–40 to +85	°C
T_{STG}	Storage temperature range	–65 to +150	°C
θ_{JA}	Thermal impedance DIP SO	90 125	°C/W °C/W

BLOCK DIAGRAM and TEST AND APPLICATION CIRCUIT

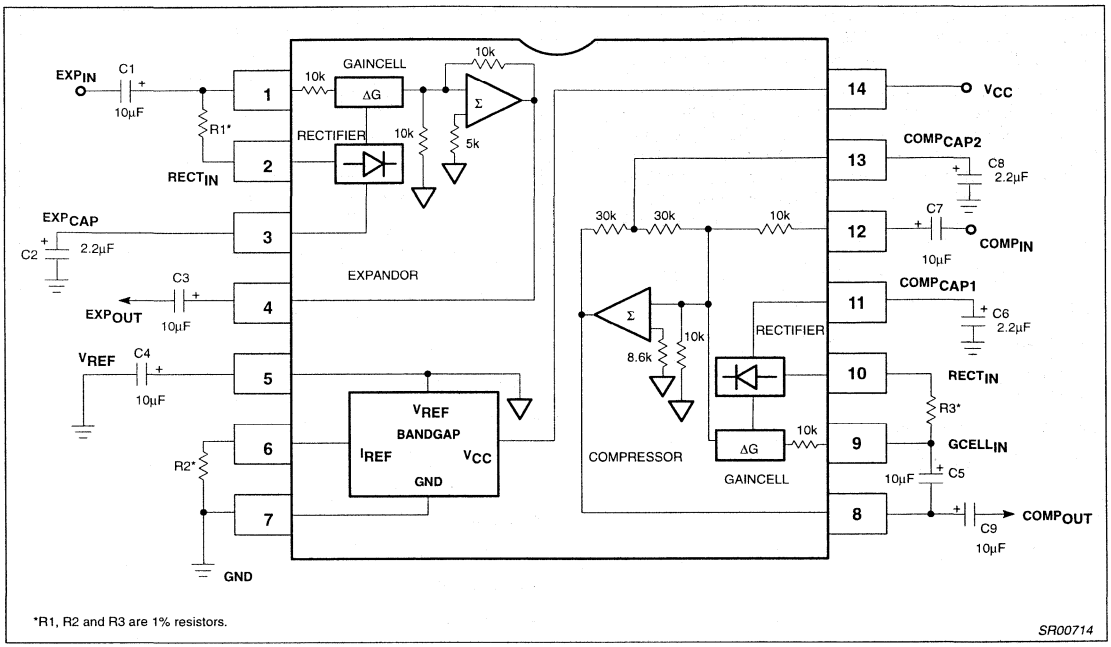


Figure 2. Block Diagram and Test and Application Circuit

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 3.6VDC, compandor 0dB level = –20dBV = 100mV_{RMS}, output load R_L = 10kΩ, Freq = 1kHz, unless otherwise specified. R1, R2 and R3 are 1% resistors.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS SA576 MIN	LIMITS SA576 TYP	LIMITS SA576 MAX	UNITS
V_{CC}	Supply voltage[1]		2	3.6	7	V
I_{CC}	Supply current	No signal R_2 = 100kΩ		1.4	3	mA
V_{REF}	Reference voltage[2]	V_{CC} = 3.6V		1.8		V
R_L	Summing amp output load		10			kΩ
THD	Total harmonic distortion	1kHz, 0dB, BW = 3.5kHz		0.25	1.5	%
E_{NO}	Expandor output noise voltage	BW = 20kHz, R_S = 0Ω		10	30	µV
0dB	Unity gain level	0dB at 1kHz	–1.5	0.18	1.5	dB
V_{OS}	Output voltage offset	No signal	–150	1	150	mV
	Expandor output DC shift	No signal to 0dB	–100	7	100	mV
	Tracking error relative to 0dB output	-20dB expandor	–1.0	0.3	1.0	dB
	Crosstalk, COMP to EXP	1kHz, 0dB, C_{REF} = 10µF		–80		dB
V_O	Output swing low			0.2		V
	Output swing high			V_{CC} – 0.2		

NOTE:
1. Operation down to V_{CC} = 1.8V is possible, see description on front page of SA576 data sheet.
2. Reference voltage, V_{REF}, is typically at 1/2 V_{CC}.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 3.6V, T_A = 25°C, R1=R3=7.15kΩ, R2=100kΩ, 0dB level = 100mV, Freq. = 1kHz

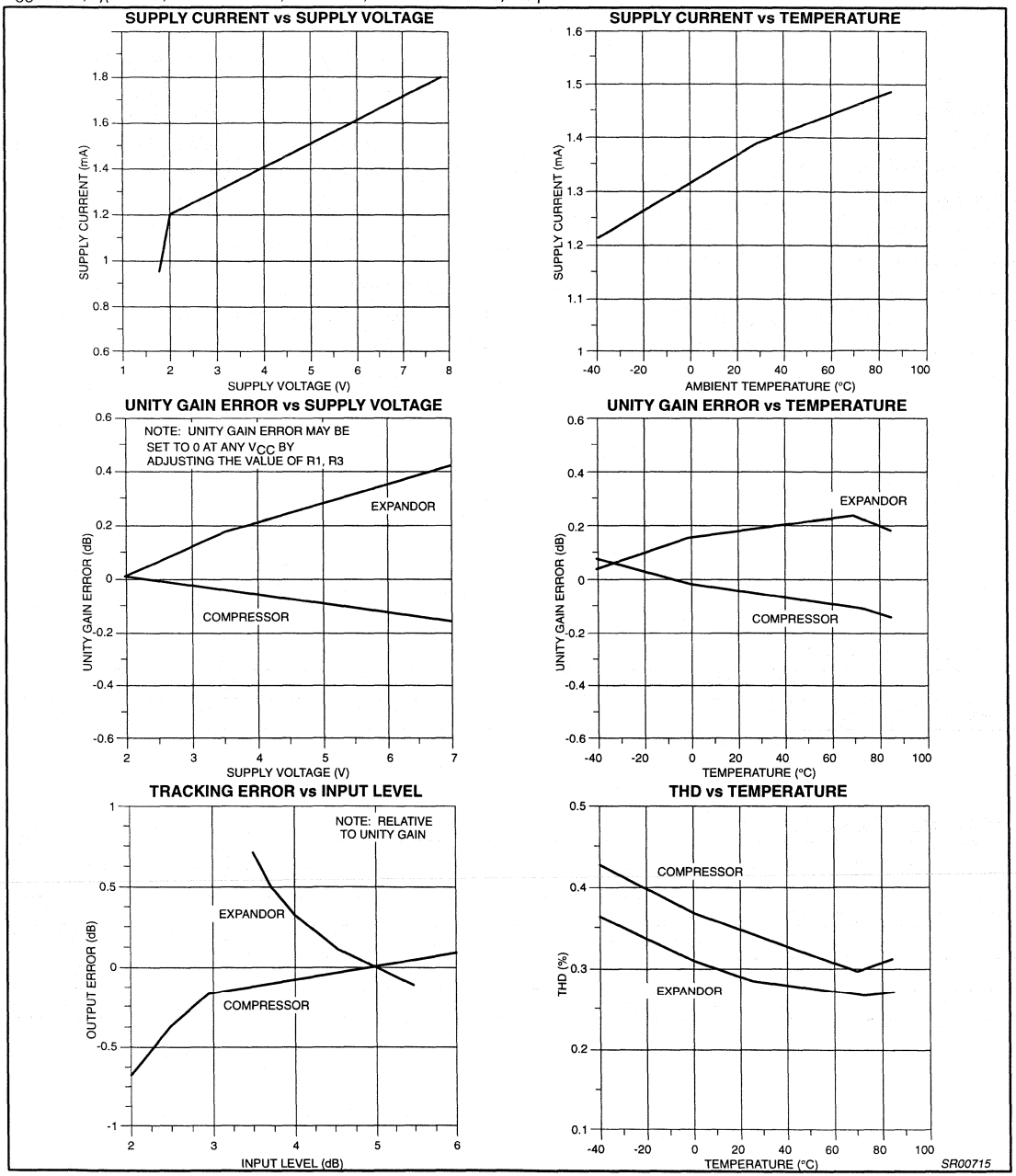


Figure 3. Typical Performance Characteristics

Unity gain level programmable low power compandor SA577

DESCRIPTION

The SA577 is a unity gain level programmable compandor designed for low power applications. The SA577 is internally configured as an expandor and a compressor to minimize external component count.

FEATURES

- Operating voltage range: 1.8V to 7V
- Low power consumption (1.4mA @ 3.6V)
- 0dB level programmable (10mV$_{RMS}$ to 1.0V$_{RMS}$)
- Over 90dB of dynamic range
- Wide input/output swing capability (rail-to-rail)
- Low external component count
- SA577 meets cellular radio specifications
- ESD hardened

PIN CONFIGURATION

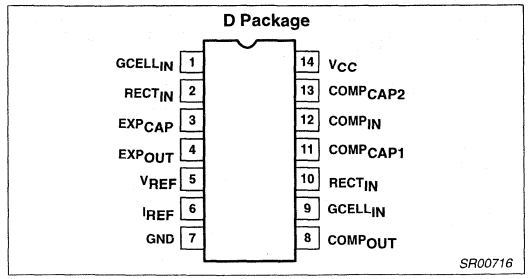


Figure 1. Pin Configuration

APPLICATIONS

- High performance portable communications
- Cellular radio
- Cordless telephone
- Consumer audio
- Wireless microphones
- Modems
- Electric organs
- Hearing aids
- Automatic level control (ALC)

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
14-Pin Plastic Small Outline (SO)	–40 to +85°C	SA577D	SOT108-1

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING SA577	UNITS
V_{CC}	Supply voltage	8	V
T_A	Operating ambient temperature range	–40 to +85	°C
T_{STG}	Storage temperature range	–65 to +150	°C
θ_{JA}	Thermal impedance SO	125	°C/W

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 3.6VDC, compandor 0dB level = –20dBV = 100mV_{RMS}, output load R_L = 10kΩ, Freq = 1kHz, unless otherwise specified. R1, R2 and R3 are 1% resistors.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA577			
			MIN	TYP	MAX	
V_{CC}	Supply voltage[1]		2	3.6	7	V
I_{CC}	Supply current	No signal R_2 = 100kΩ		1.4	2	mA
V_{REF}	Reference voltage[2]	V_{CC} = 3.6V	1.7	1.8	1.9	V
R_L	Summing amp output load		10			kΩ
THD	Total harmonic distortion	1kHz, 0dB, BW = 3.5kHz		0.25	1.5	%
E_{NO}	Expandor output noise voltage	BW = 20kHz, R_S = 0Ω		10	25	μV
0dB	Unity gain level	0dB at 1kHz	–1.5	0.18	1.5	dB
	Programmable range[3]	R1 = R3 = 18.7kΩ, R2 = 24.3kΩ		0		dBV
		R1 = R3 = 22.6kΩ, R2 = 100kΩ		–10		
		R1 = R3 = 7.15kΩ, R2 = 100kΩ		–20		
		R1 = R3 = 1.33kΩ, R2 = 200kΩ		–40		
V_{OS}	Output voltage offset	No signal	–150	1	150	mV
	Expandor output DC shift	No signal to 0dB	–100	7	100	mV
	Tracking error relative to 0dB output	-20dB expandor	–1.0	0.3	1.0	dB
	Crosstalk, COMP to EXP	1kHz, 0dB, C_{REF} = 10μF		–80	–65	dB
V_O	Output swing low			0.2		V
	Output swing high			V_{CC} – 0.2		

NOTE:
1. Operation down to V_{CC} = 1.8V is possible, see application note AN1762.
2. Reference voltage, V_{REF}, is typically at 1/2 V_{CC}.
3. Unity gain level can be adjusted CONTINUOUSLY between –40dBV = 10mV_{RMS} and 0dBV = 1.0V_{RMS}. For details see application note AN1762.

BLOCK DIAGRAM and TEST AND APPLICATION CIRCUIT

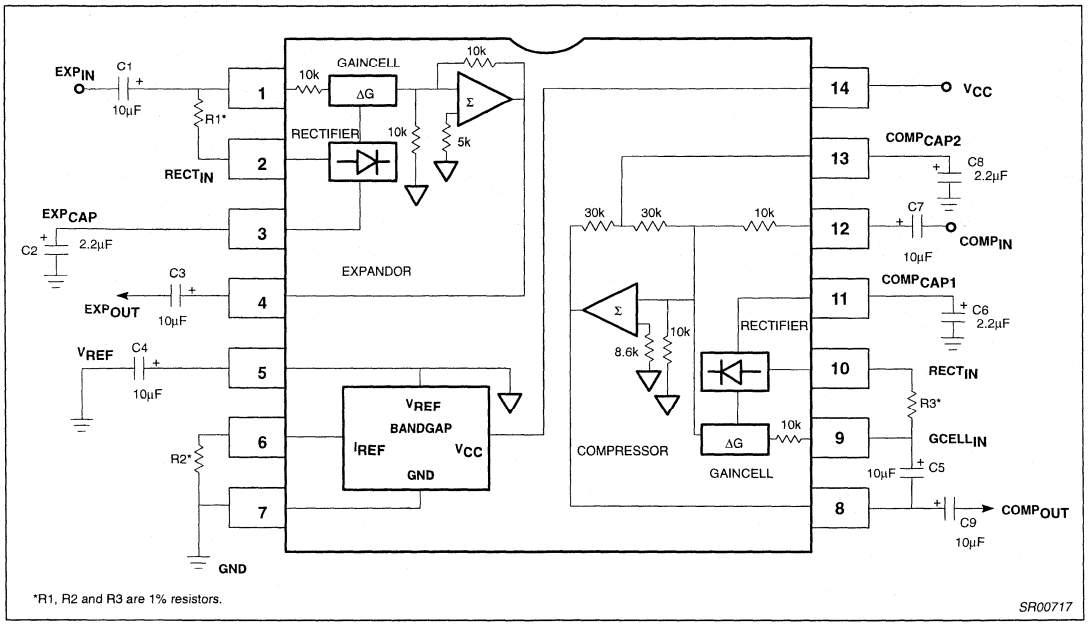


Figure 2. Block Diagram and Test and Application Circuit

TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 3.6V, T_A = 25°C, R1=R3=7.15kΩ, R2=100kΩ, 0dB level = 100mV, Freq. = 1kHz

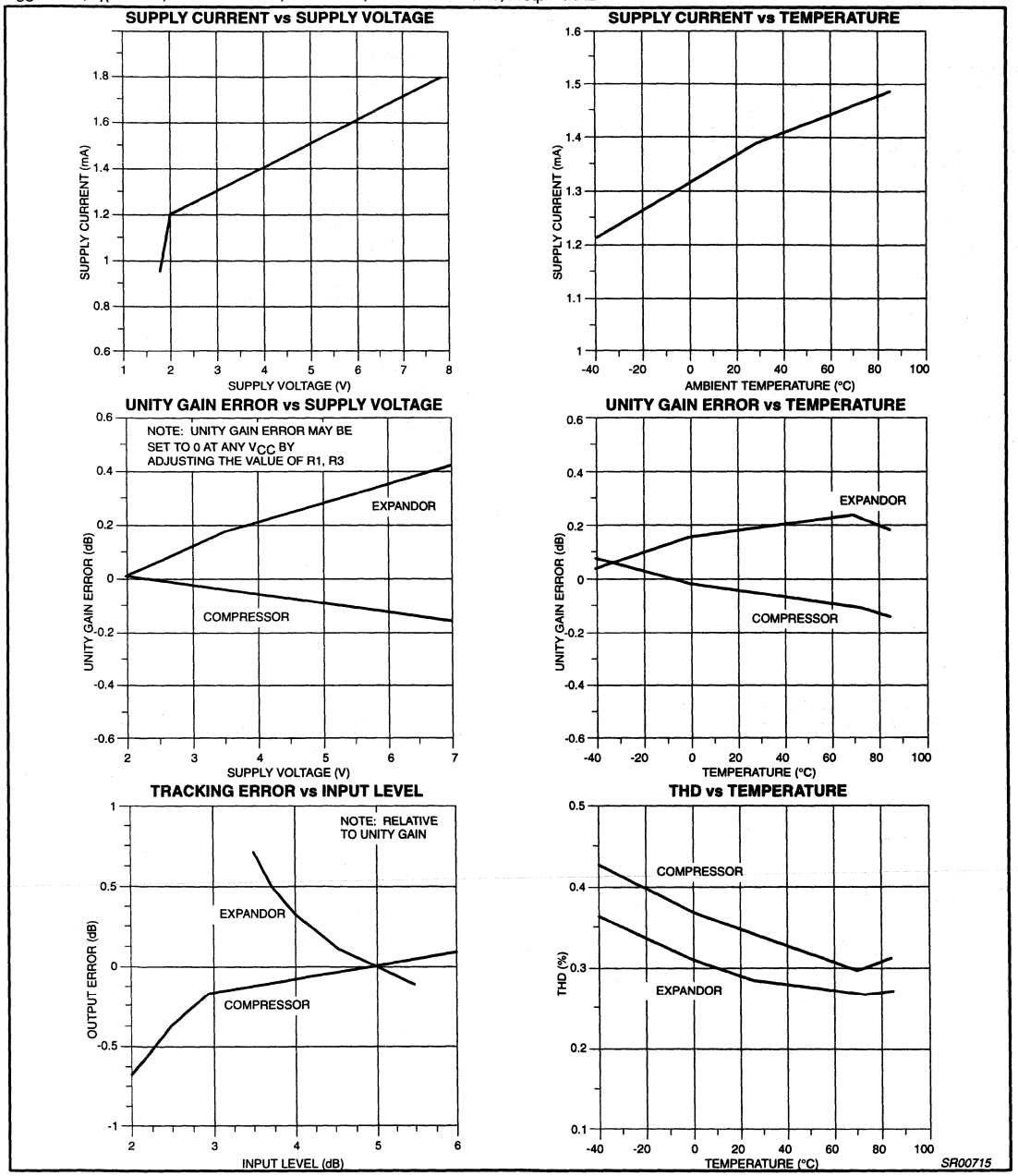


Figure 3. Typical Performance Characteristics

Unity gain level programmable low power compandor SA578

DESCRIPTION

The SA578 is a unity gain level programmable compandor designed for low power applications. The SA578 is internally configured as an expandor and a compressor to minimize external component count.

The summing amplifiers of the SA578 have 600Ω drive capability and the inverting input of the compressor amplifier is accessible through Pin 9 for summing multiple external signals. Power Down/Mute function is active low and requires an open collector output logic configuration at Pin 8. If Power Down/Mute is not needed, Pin 8 should be left open. When the part is muted, supply current drops to 170mA at 3.6V.

FEATURES

- Operating voltage range: 1.8V to 7V
- Low power consumption (1.4mA @ 3.6V)
- 0dB level programmable ($10mV_{RMS}$ to $1.0V_{RMS}$)
- Over 90dB of dynamic range
- Wide input/output swing capability
- Low external component count
- SA578 meets cellular radio specifications
- ESD hardened
- Power Down mode (I_{CC} = 170μA @ 3.6V)
- Mute function
- Multiple external summing capability
- 600Ω drive capability

PIN CONFIGURATION

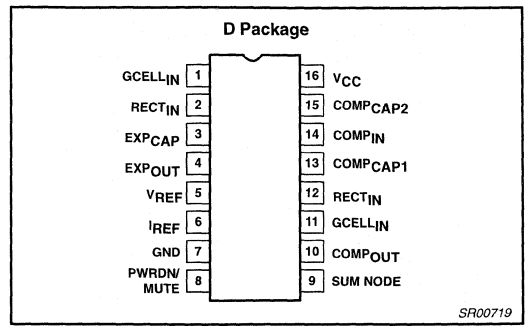


Figure 1. Pin Configuration

APPLICATIONS

- High performance portable communications
- Cellular radio
- Cordless telephone
- Consumer audio
- Wireless microphones
- Modems
- Electric organs
- Hearing aids
- Automatic level control (ALC)

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Small Outline (SO)	–40 to +85°C	SA578D	SOT109-1

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING SA578	UNITS
V_{CC}	Supply voltage	8	V
T_A	Operating ambient temperature range	–40 to +85	°C
T_{STG}	Storage temperature range	–65 to +150	°C
θ_{JA}	Thermal impedance SO	125	°C/W

BLOCK DIAGRAM and TEST AND APPLICATION CIRCUIT

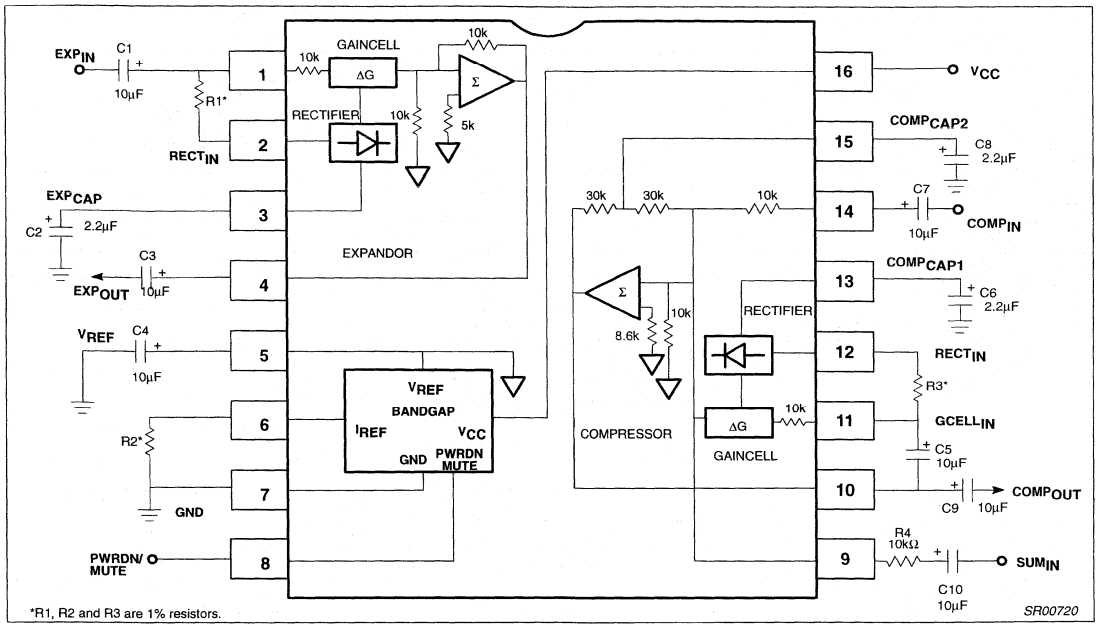


Figure 2. Block Diagram and Test and Application Circuit

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 3.6VDC, compandor 0dB level = –20dBV = 100mV_{RMS}, output load R_L = 10kΩ, Freq = 1kHz, unless otherwise specified. R1, R2 and R3 are 1% resistors.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA578			
			MIN	TYP	MAX	
V_{CC}	Supply voltage[1]		2	3.6	7	V
I_{CC}	Supply current operating power down	No signal, R_2 = 100kΩ		1.4 170	2	mA µA
V_{REF}	Reference voltage[2]	V_{CC} = 3.6V	1.7	1.8	1.9	V
R_L	Summing amp minimum output load			600		Ω
THD	Total harmonic distortion	1kHz, 0dB, BW = 3.5kHz		0.25	1.0	%
E_{NO}	Expandor output noise voltage	BW = 20kHz, R_S = 0Ω		10	20	µV
0dB	Unity gain level	0dB at 1kHz	–1.0	0.18	1.0	dB
	Programmable range[3]	R1 = R3 = 18.7kΩ, R2 = 24.3kΩ		0		dBV
		R1 = R3 = 22.6kΩ, R2 = 100kΩ		–10		
		R1 = R3 = 7.15kΩ, R2 = 100kΩ		–20		
		R1 = R3 = 1.33kΩ, R2 = 200kΩ		–40		
V_{OS}	Output voltage offset	No signal	–150	1	150	mV
	Expandor output DC shift	No signal to 0dB	–100	7	100	mV
	Tracking error relative to 0dB output	-20dB expandor	–1.0	0.3	1.0	dB
	Crosstalk, COMP to EXP	1kHz, 0dB, C_{REF} = 10µF		–80	–65	dB
V_O	Output swing low			0.2		V
	Output swing high			V_{CC} – 0.2		
	Power Down/Mute low level		0		0.4	V
	Power Down/Mute input current	Pin 8 grounded		–65		µA

NOTE:
1. Operation down to V_{CC} = 1.8V is possible.
2. Reference voltage, V_{REF}, is typically at 1/2 V_{CC}.
3. Unity gain level can be adjusted CONTINUOUSLY between –40dBV = 10mV_{RMS} and 0dBV = 1.0V_{RMS}. For details see application note AN1762.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 3.6V, T_A = 25°C, R1=R3=7.15kΩ, R2=100kΩ, 0dB level = 100mV, Freq. = 1kHz

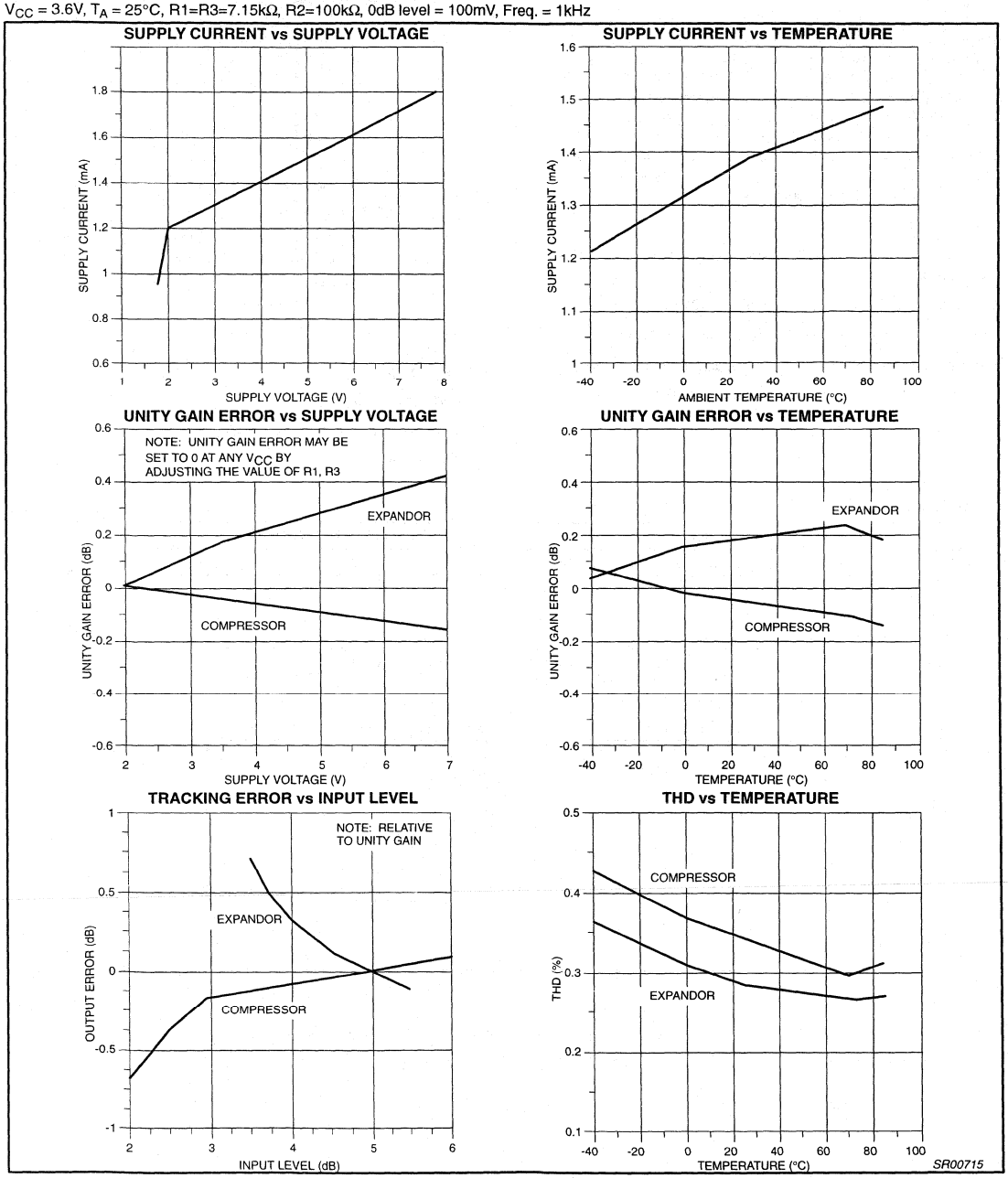


Figure 3. Typical Performance Characteristics

Low voltage LNA and mixer - 1GHz | SA601

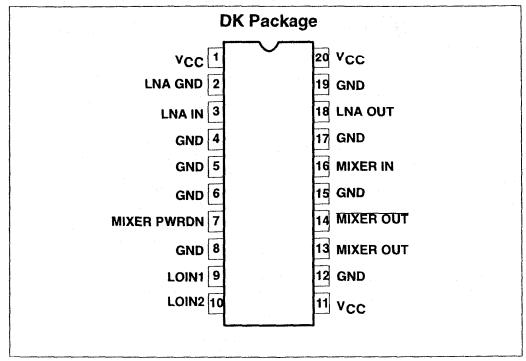
DESCRIPTION

The SA601 is a combined RF amplifier and mixer designed for high-performance low-power communication systems from 800-1200MHz. The low-noise preamplifier has a 1.6dB noise figure at 900MHz with 11.5dB gain and an IP3 intercept of -2dBm at the input. The gain is stabilized by on-chip compensation to vary less than ±0.2dB over -40 to +85°C temperature range. The wide-dynamic-range mixer has a 9.5dB noise figure and IP3 of –2dBm at the input at 900MHz. The nominal current drawn from a single 3V supply is 7.4mA. The Mixer can be powered down to further reduce the supply current to 4.4mA.

FEATURES

- Low current consumption: 7.4mA nominal, 4.4mA with the mixer powered-down
- Outstanding LNA noise figure: 1.6dB at 900MHz
- High system power gain: 18dB (LNA + Mixer) at 900MHz
- Excellent gain stability versus temperature and supply voltage
- External >-7dBm LO can be used to drive the mixer

PIN CONFIGURATION



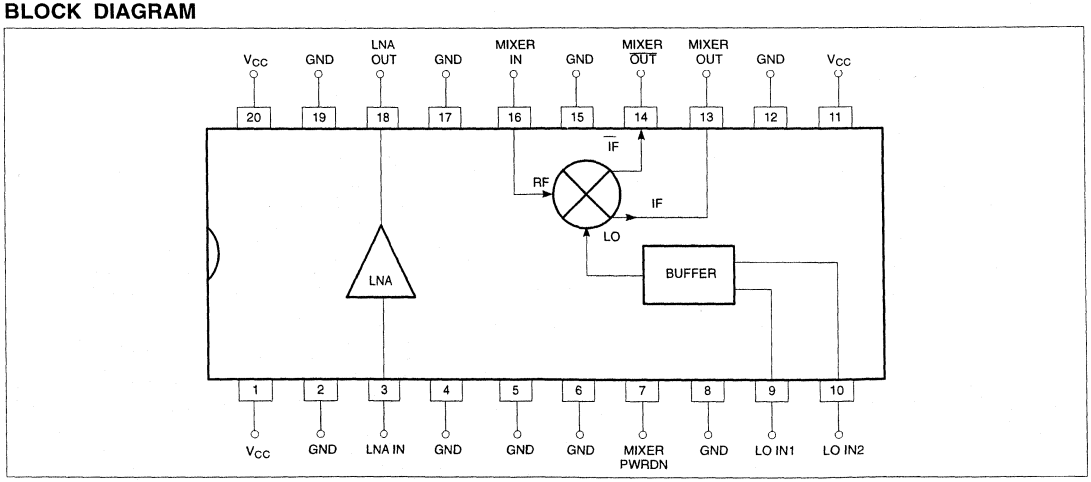
APPLICATIONS

- 900MHz cellular front-end (NADC, GSM, AMPS, TACS)
- 900MHz cordless front-end (CT1, CT2)
- 900MHz receivers

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Shrink Small Outline Package (Surface-mount, SSOP)	-40 to +85°C	SA601DK	1563

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[3]

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage[1]	-0.3 to +6	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{CC} + 0.3)	V
P_D	Power dissipation, T_A = 25°C (still air)[2] 20-Pin Plastic SSOP	980	mW
T_{JMAX}	Maximum operating junction temperature	150	°C
P_{MAX}	Maximum power input/output	+20	dBm
T_{STG}	Storage temperature range	–65 to +150	°C

NOTE:
1. Transients exceeding 8V on V_{CC} pin may damage product.
2. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance,
   θ_{JA}: 20-Pin SSOP = 110°C/W
3. Pins 9 and 10 are sensitive to electrostatic discharge (ESD).

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	2.7 to 5.5	V
T_A	Operating ambient temperature range	-40 to +85	°C
T_J	Operating junction temperature	-40 to +105	°C

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
I_{CC}	Supply current			7.4		mA
		Mixer power-down input low		4.4		
V_{LNA-IN}	LNA input bias voltage			0.78		V
$V_{LNA-OUT}$	LNA output bias voltage			2.1		V
V_{MX-IN}	Mixer RF input bias voltage			0.94		V

AC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; LO_{IN} = -7dBm @ 964MHz; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			-3σ	TYP	+3σ	
S_{21}	Amplifier gain	881MHz	10	11.5	13	dB
$\Delta S_{21}/\Delta T$	Gain temperature sensitivity	881MHz		0.003		dB/°C
$\Delta S_{21}/\Delta f$	Gain frequency variation	800MHz - 1.2GHz		0.01		dB/MHz
S_{12}	Amplifier reverse isolation	881MHz		-20		dB
S_{11}	Amplifier input match[1]	881MHz		-10		dB
S_{22}	Amplifier output match[1]	881MHz		-10		dB
P_{-1dB}	Amplifier input 1dB gain compression	881MHz		-16		dBm
IP3	Amplifier input third order intercept	$f_2 - f_1$ = 25kHz, 881MHz	-3.5	-2	-0.5	dBm
NF	Amplifier noise figure	881MHz	1.3	1.6	1.9	dB
VG_C	Mixer voltage conversion gain: $R_P = R_L$ = 1kΩ	f_S = 881MHz, f_{LO} = 964MHz, f_{IF} = 83MHz	18.0	19.5	21.0	dB
PG_C	Mixer power conversion gain: $R_P = R_L$ = 1kΩ	f_S = 881MHz, f_{LO} = 964MHz, f_{IF} = 83MHz	5.0	6.5	8.0	dB
S_{11M}	Mixer input match[1]	881MHz		-10		dB
NF_M	Mixer SSB noise figure	881MHz	8.0	9.5	11.0	dB
P_{-1dB}	Mixer input 1dB gain compression	881MHz		-13		dBm
$IP3_M$	Mixer input third order intercept	$f_2 - f_1$ = 25kHz, 881MHz	-3.5	-2	-0.5	dBm
IP_{2INT}	Mixer input second order intercept	881MHz		12		dBm
P_{RFM-IF}	Mixer RF feedthrough	881MHz		-7		dB
P_{LO-IF}	LO feedthrough to IF	881MHz		-25		dB
P_{LO-RFM}	LO to mixer input feedthrough	881MHz		-38		dB
P_{LO-RF}	LO to LNA input feedthrough	881MHz		-40		dB
$P_{LNA-RFM}$	LNA output to mixer input	881MHz		-40		dB
P_{RFM-LO}	Mixer input to LO feedthrough	881MHz		-23		dB
LO_{IN}	LO drive level	964MHz		-7		dBm

NOTE:
1. Simple L/C elements are needed to achieve specified return loss.

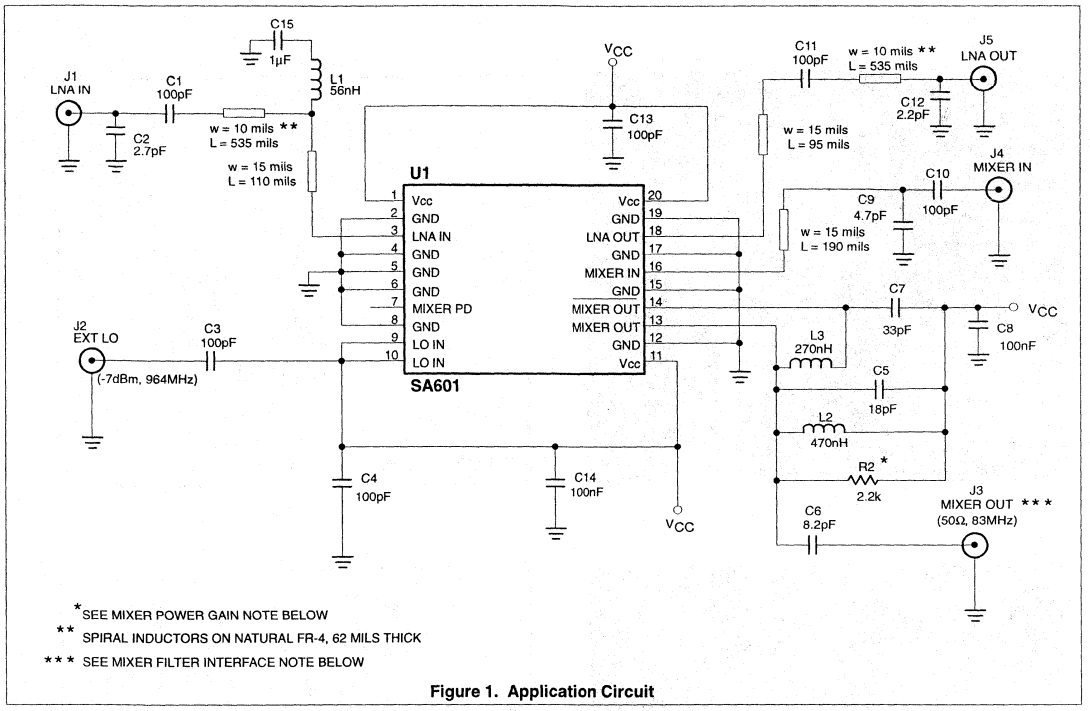


Figure 1. Application Circuit

CIRCUIT TECHNOLOGY

LNA

Impedance Match: Intrinsic return loss at the input and output ports is 7dB and 9dB, respectively. With no external matching, the associated LNA gain is ≈10dB and the noise figure is ≈1.4dB. However, the return loss can be improved at 881MHz using suggested L/C elements (Figure 1) as the LNA is unconditionally stable.

Noise Match: The LNA achieves 1.6dB noise figure at 881MHz when S_{11} = -10dB. Further improvements in S_{11} will slightly decrease the NF and increase S_{21}.

Temperature Compensation: The LNA has a built-in temperature compensation scheme to reduce the gain drift to 0.003dB/°C from –40°C to +85°C.

Supply Voltage Compensation: Unique circuitry provides gain stabilization over wide supply voltage range. The gain changes no more than 0.5dB when V_{CC} increases from 3V to 5V.

LO Drive Level: Resistor R1 can be replaced by an inductor of 4.7nH and C13 should be adjusted to achieve a good return loss at the LO port. Under this condition, the mixer will operate with less than -10dBm LO drive.

IP3 Performance: C9 between Pin 16 and ground can be removed to introduce 3dB mismatch loss, while improving the IP3 to +3dBm. The associated noise figure is 11dB.

Mixer

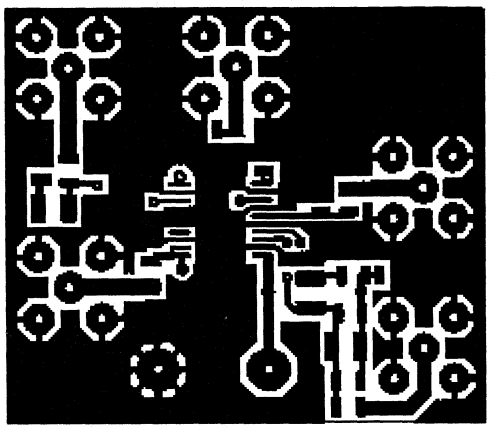
Input Match: The mixer is configured for maximum gain and best noise figure. The user needs to supply L/C elements to achieve this performance.

Power Gain: The gain can be increased by approximately 1.5dB by placing R2 across C7, instead of C5.

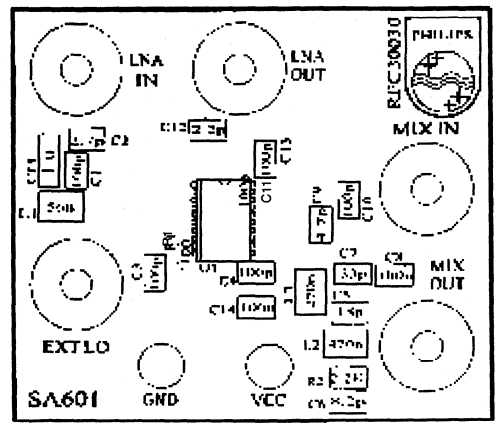
Power Down: The mixer can be disabled by connecting Pin 7 to ground. When the mixer is disabled, 3mA is saved.

Power Combining: The mixer output circuit features passive power combining (patent pending) to optimize conversion gain and noise figure performance without using extra DC current or degrading the IP3. For IF frequencies significantly different than 83MHz, the component values must be altered accordingly.

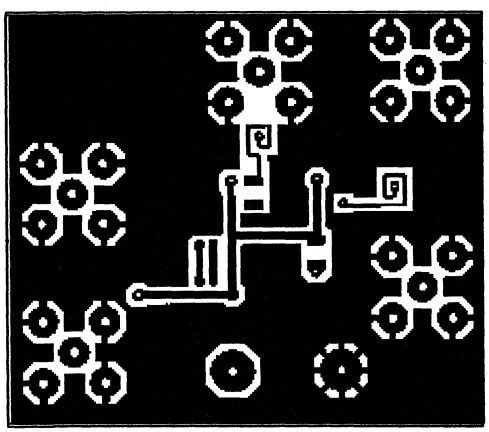
Filter Interface: For system integration where a high impedance filter of 1kΩ is to be cascaded at the mixer IF output, capacitors C5 and C6 need to be changed to 27pF and 1000pF, respectively.



Top View



Silk Screen



Bottom View



Via Layer

Figure 2. SA601 Demoboard Layout (Not Actual Size)

TYPICAL PERFORMANCE CHARACTERISTICS

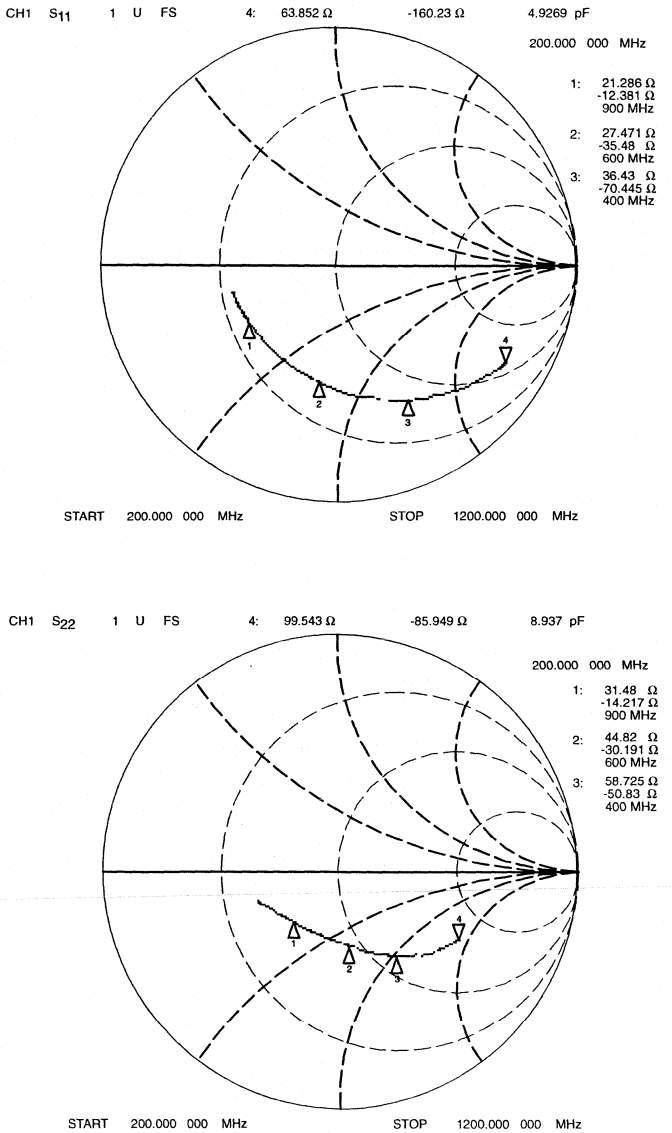
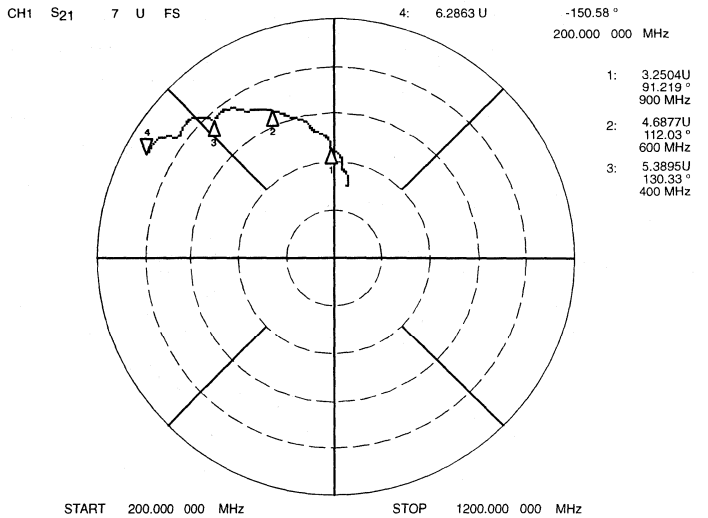


Figure 3. LNA Input and Output Match (at Device Pin)

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



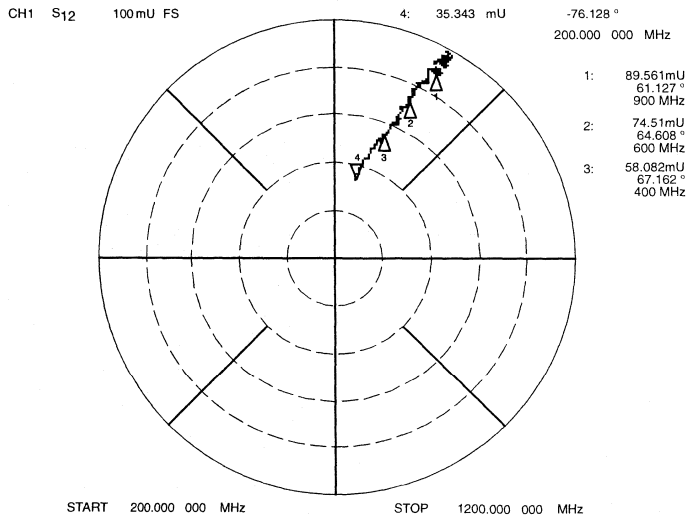


Figure 4. LNA Transmission and Isolation Characteristics (at Device Pin)

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

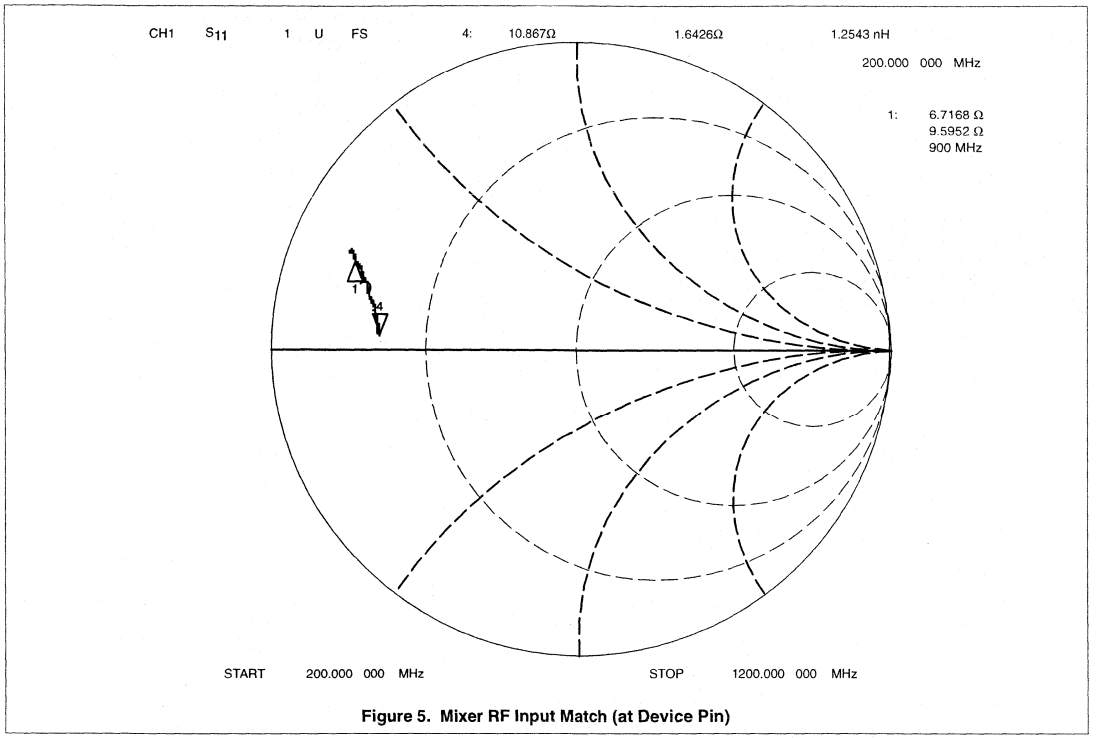


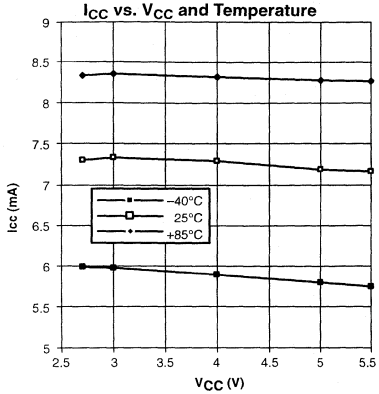
Figure 5. Mixer RF Input Match (at Device Pin)

Table 1. Typical LNA and Mixer S-Parameters

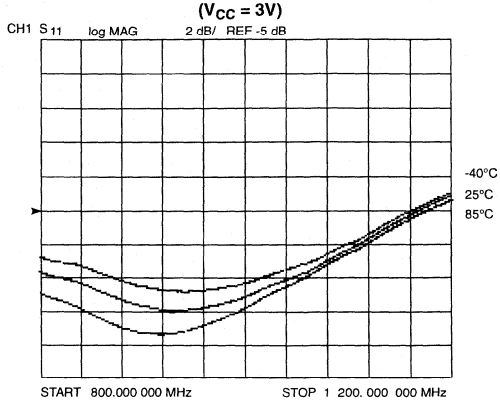
	LNA				Mixer
f	**S_{11}**	**S_{22}**	**S_{21}**	**S_{12}**	**S_{11}**
200MHz	63.852Ω – j 160.23Ω	99.543Ω – j 85.949Ω	6.2863U ∠ 150.58°	35.343mU ∠ 76.128°	10.867Ω + j 1.6426Ω
300MHz	44.879Ω – j 101.69Ω	73.387Ω – j 67.707Ω	5.8096U ∠ 140.47°	47.946mU ∠ 71.169°	10.4Ω + j 3.4609Ω
400MHz	36.43Ω – j 70.445Ω	58.725Ω – j 50.83Ω	5.3895U ∠ 130.33°	58.082mU ∠ 67.162°	10.067Ω + j 4.897Ω
500MHz	30.395Ω – j 48.393Ω	49.928Ω – j 38.813Ω	5.0428U ∠ 120.5°	66.44mU ∠ 66.388°	9.394Ω + j 6.0142Ω
600MHz	27.471Ω – j 35.48Ω	44.82Ω – j 30.191Ω	4.6877U ∠ 112.03°	74.51mU ∠ 64.608°	8.8945Ω + j 7.2227Ω
700MHz	24.428Ω – j 25Ω	39.268Ω – j 24.502Ω	4.2409U ∠ 104.44°	82.235mU ∠ 65.002°	8.1353Ω + j 8.1597Ω
800MHz	22.434Ω – j 17.255Ω	34.664Ω – j 18.59Ω	3.7491U ∠ 97.765°	86.582mU ∠ 62.743°	7.976Ω + j 9.1958Ω
900MHz	21.286Ω – j 12.381Ω	31.48Ω – j 14.217Ω	3.2504U ∠ 91.219°	89.561mU ∠ 61.127°	6.7168Ω + j 9.5952Ω
1000MHz	20.261Ω – j 8.7109Ω	27.887Ω – j 10.77Ω	2.8785U ∠ 84.957°	95.135mU ∠ 60.539°	6.2393Ω + j 10.271Ω
1100MHz	19.718Ω – j 6.252Ω	25.741Ω – j 8.2607Ω	2.5752U ∠ 82.893°	97.348mU ∠ 62.202°	6.0791Ω + j 10.571Ω
1200MHz	19.101Ω – j 4.9316Ω	23.584Ω – j 6.2715Ω	2.1386U ∠ 80.257°	96.558mU ∠ 61.563°	5.8185Ω + j 10.288Ω

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

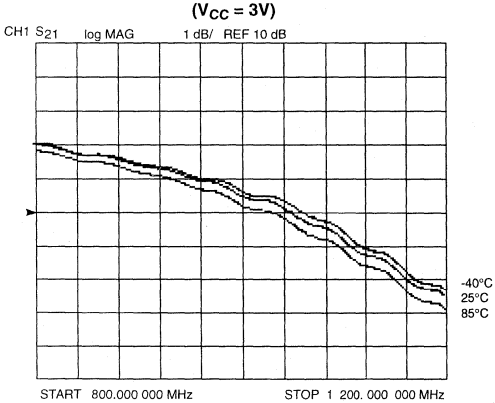
I_{CC} vs. V_{CC} and Temperature



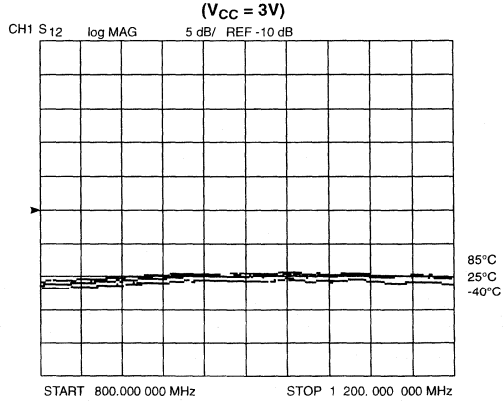
Mixer RF Input Match vs. Frequency (V_{CC} = 3V)



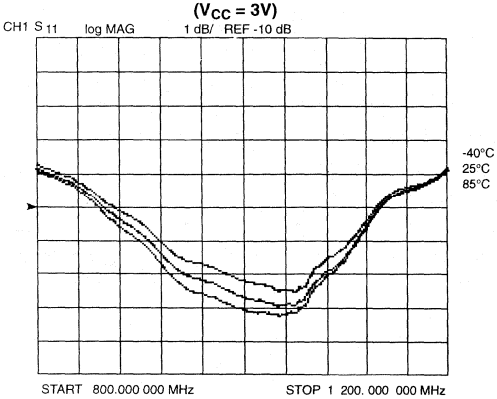
LNA Gain (S_{21}) vs. Frequency (V_{CC} = 3V)



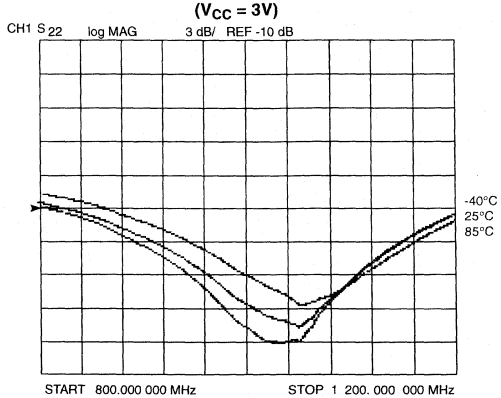
LNA Isolation (S_{12}) vs. Frequency (V_{CC} = 3V)



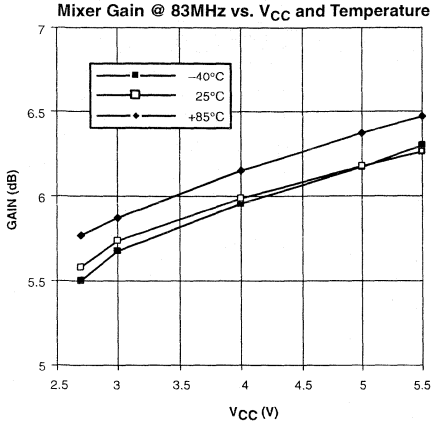
LNA Input Match (S_{11}) vs. Frequency (V_{CC} = 3V)



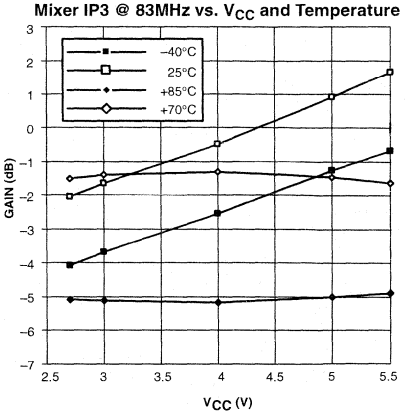
LNA Output Match (S_{22}) vs. Frequency (V_{CC} = 3V)



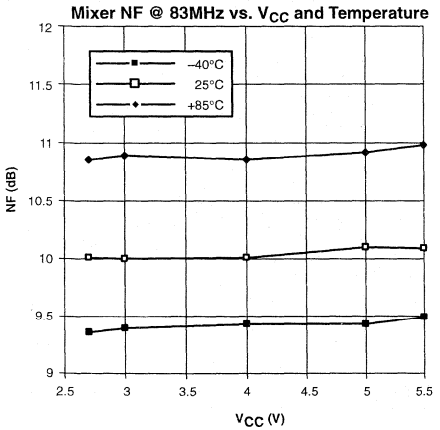
Mixer Gain @ 83MHz vs. V_{CC} and Temperature



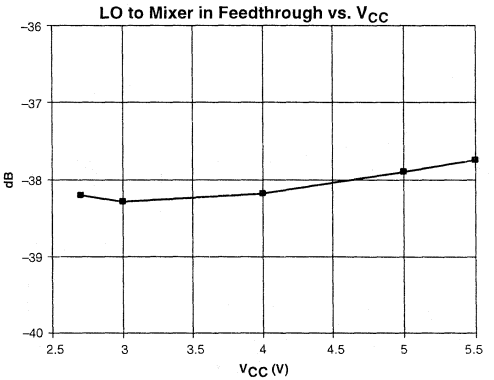
Mixer IP3 @ 83MHz vs. V_{CC} and Temperature



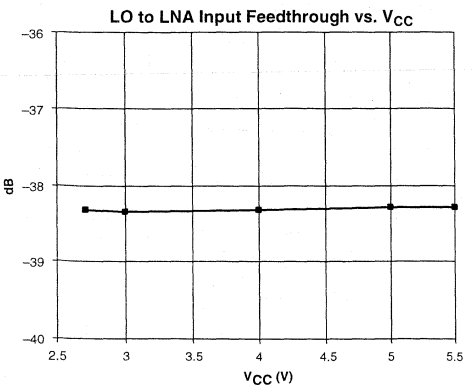
Mixer NF @ 83MHz vs. V_{CC} and Temperature



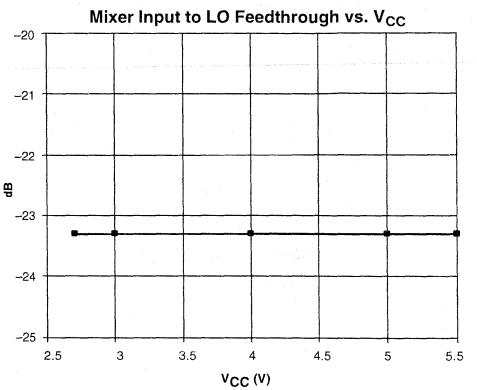
LO to Mixer in Feedthrough vs. V_{CC}

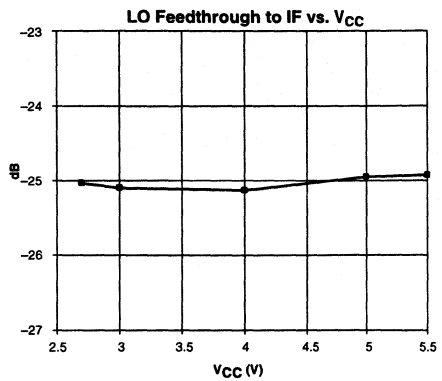


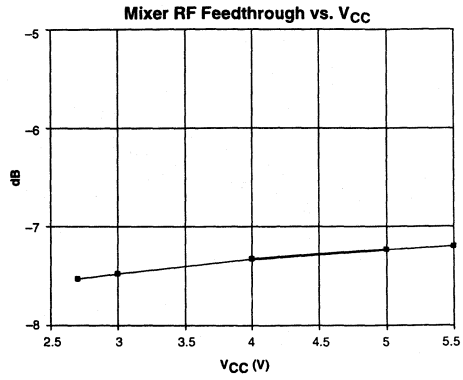
LO to LNA Input Feedthrough vs. V_{CC}

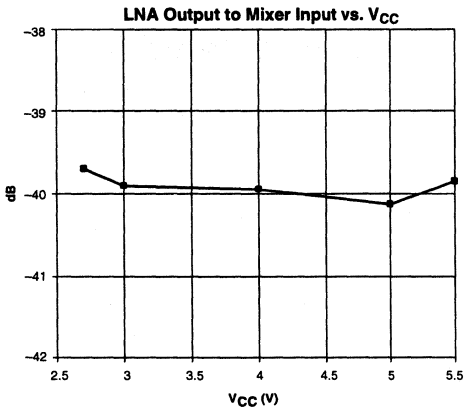


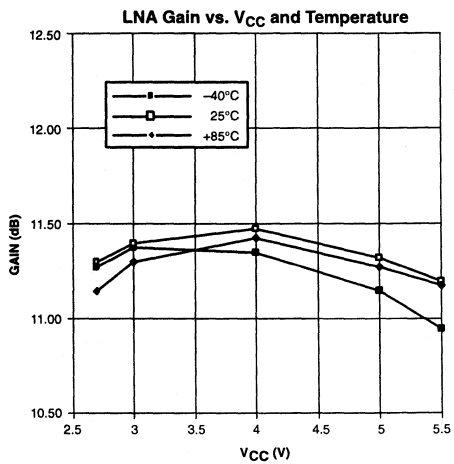
Mixer Input to LO Feedthrough vs. V_{CC}

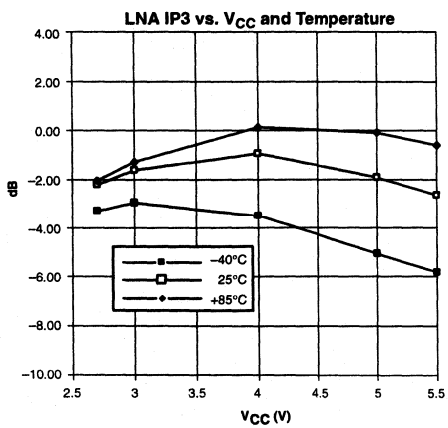


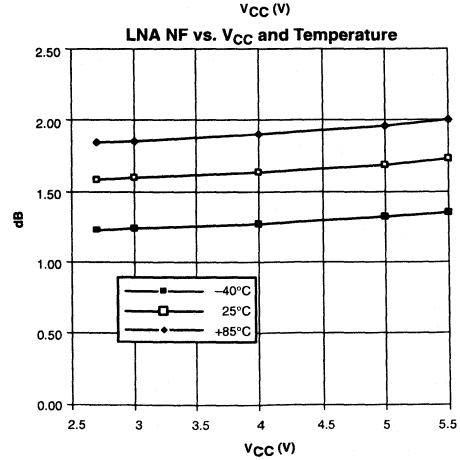

LO Feedthrough to IF vs. VCC
dB
-23
-24
-25
-26
-27
2.5
3
3.5
4
4.5
5
5.5
VCC (V)


Mixer RF Feedthrough vs. VCC
dB
-5
-6
-7
-8
2.5
3
3.5
4
4.5
5
5.5
VCC (V)


LNA Output to Mixer Input vs. VCC
dB
-38
-39
-40
-41
-42
2.5
3
3.5
4
4.5
5
5.5
VCC (V)


LNA Gain vs. VCC and Temperature
GAIN (dB)
12.50
12.00
11.50
11.00
10.50
2.5
3
3.5
4
4.5
5
5.5
VCC (V)
-40°C
25°C
+85°C


LNA IP3 vs. VCC and Temperature
dB
4.00
2.00
0.00
-2.00
-4.00
-6.00
-8.00
-10.00
2.5
3
3.5
4
4.5
5
5.5
VCC (V)
-40°C
25°C
+85°C


LNA NF vs. VCC and Temperature
dB
2.50
2.00
1.50
1.00
0.50
0.00
2.5
3
3.5
4
4.5
5
5.5
VCC (V)
-40°C
25°C
+85°C

Double-balanced mixer and oscillator SA602A

DESCRIPTION

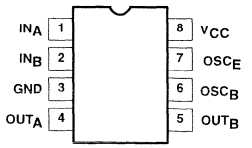
The SA602A is a low-power VHF monolithic double-balanced mixer with input amplifier, on-board oscillator, and voltage regulator. It is intended for high performance, low power communication systems. The guaranteed parameters of the SA602A make this device particularly well suited for cellular radio applications. The mixer is a "Gilbert cell" multiplier configuration which typically provides 18dB of gain at 45MHz. The oscillator will operate to 200MHz. It can be configured as a crystal oscillator, a tuned tank oscillator, or a buffer for an external LO. For higher frequencies the LO input may be externally driven. The noise figure at 45MHz is typically less than 5dB. The gain, intercept performance, low-power and noise characteristics make the SA602A a superior choice for high-performance battery operated equipment. It is available in an 8-lead dual in-line plastic package and an 8-lead SO (surface-mount miniature package).

FEATURES

- Low current consumption: 2.4mA typical
- Excellent noise figure: <4.7dB typical at 45MHz
- High operating frequency
- Excellent gain, intercept and sensitivity
- Low external parts count; suitable for crystal/ceramic filters
- SA602A meets cellular radio specifications

PIN CONFIGURATION

D and N Packages



SR00068

Figure 1. Pin Configuration

APPLICATIONS

- Cellular radio mixer/oscillator
- Portable radio
- VHF transceivers
- RF data links
- HF/VHF frequency conversion
- Instrumentation frequency conversion
- Broadband LANs

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Dual In-Line Plastic (DIP)	-40 to +85°C	SA602AN	SOT97-1
8-Pin Plastic Small Outline (SO) package (Surface-mount)	-40 to +85°C	SA602AD	SOT96-1

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Maximum operating voltage	9	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range SA602A	-40 to +85	°C
θ_{JA}	Thermal impedance D package	90	°C/W
	N package	75	°C/W

BLOCK DIAGRAM

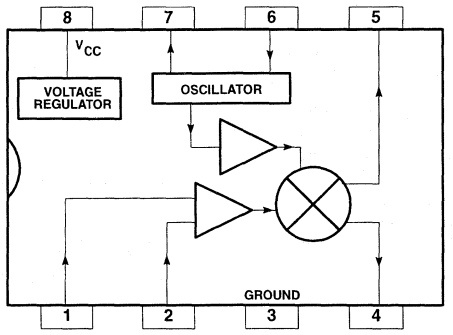


Figure 2. Block Diagram

AC/DC ELECTRICAL CHARACTERISTICS

V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA602A			
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		4.5		8.0	V
	DC current drain			2.4	2.8	mA
f_{IN}	Input signal frequency			500		MHz
f_{OSC}	Oscillator frequency			200		MHz
	Noise figure at 45MHz			5.0	5.5	dB
	Third-order intercept point	RF_{IN} = -45dBm: f_1 = 45.0MHz, f_2 = 45.06MHz		-13	-15	dBm
	Conversion gain at 45MHz		14	17		dB
R_{IN}	RF input resistance		1.5			kΩ
C_{IN}	RF input capacitance			3	3.5	pF
	Mixer output resistance	(Pin 4 or 5)		1.5		kΩ

DESCRIPTION OF OPERATION

The SA602A is a Gilbert cell, an oscillator/buffer, and a temperature compensated bias network as shown in the equivalent circuit. The Gilbert cell is a differential amplifier (Pins 1 and 2) which drives a balanced switching cell. The differential input stage provides gain and determines the noise figure and signal handling performance of the system.

The SA602A is designed for optimum low power performance. When used with the SA604 as a 45MHz cellular radio second IF and demodulator, the SA602A is capable of receiving -119dBm signals with a 12dB S/N ratio. Third-order intercept is typically -13dBm (that is approximately +5dBm output intercept because of the RF gain). The system designer must be cognizant of this large signal limitation. When designing LANs or other closed systems where transmission levels are high, and small-signal or signal-to-noise issues are not critical, the input to the SA602A should be appropriately scaled.

Besides excellent low power performance well into VHF, the SA602A is designed to be flexible. The input, RF mixer output and oscillator ports can support a variety of configurations provided the designer understands certain constraints, which will be explained here.

The RF inputs (Pins 1 and 2) are biased internally. They are symmetrical. The equivalent AC input impedance is approximately 1.5k ll 3pF through 50MHz. Pins 1 and 2 can be used interchangeably, but they should not be DC biased externally. Figure 5 shows three typical input configurations.

The mixer outputs (Pins 4 and 5) are also internally biased. Each output is connected to the internal positive supply by a 1.5kΩ resistor. This permits direct output termination yet allows for balanced output as well. Figure 6 shows three single ended output configurations and a balanced output.

The oscillator is capable of sustaining oscillation beyond 200MHz in crystal or tuned tank configurations. The upper limit of operation is determined by tank "Q" and required drive levels. The higher the "Q" of the tank or the smaller the required drive, the higher the permissible oscillation frequency. If the required LO is beyond oscillation limits, or the system calls for an external LO, the external signal can be injected at Pin 6 through a DC blocking capacitor. External LO should be at least 200mV$_{P-P}$.

Figure 7 shows several proven oscillator circuits. Figure 7a is appropriate for cellular radio. As shown, an overtone mode of operation is utilized. Capacitor C3 and inductor L1 suppress oscillation at the crystal fundamental frequency. In the fundamental mode, the suppression network is omitted.

Figure 8 shows a Colpitts varactor tuned tank oscillator suitable for synthesizer-controlled applications. It is important to buffer the output of this circuit to assure that switching spikes from the first counter or prescaler do not end up in the oscillator spectrum. The dual-gate MOSFET provides optimum isolation with low current. The FET offers good isolation, simplicity, and low current, while the bipolar transistors provide the simple solution for non-critical applications. The resistive divider in the emitter-follower circuit should be chosen to provide the minimum input signal which will assure correct system operation.

When operated above 100MHz, the oscillator may not start if the Q of the tank is too low. A 22kΩ resistor from Pin 7 to ground will increase the DC bias current of the oscillator transistor. This improves the AC operating characteristic of the transistor and should help the oscillator to start. A 22kΩ resistor will not upset the other DC biasing internal to the device, but smaller resistance values should be avoided.

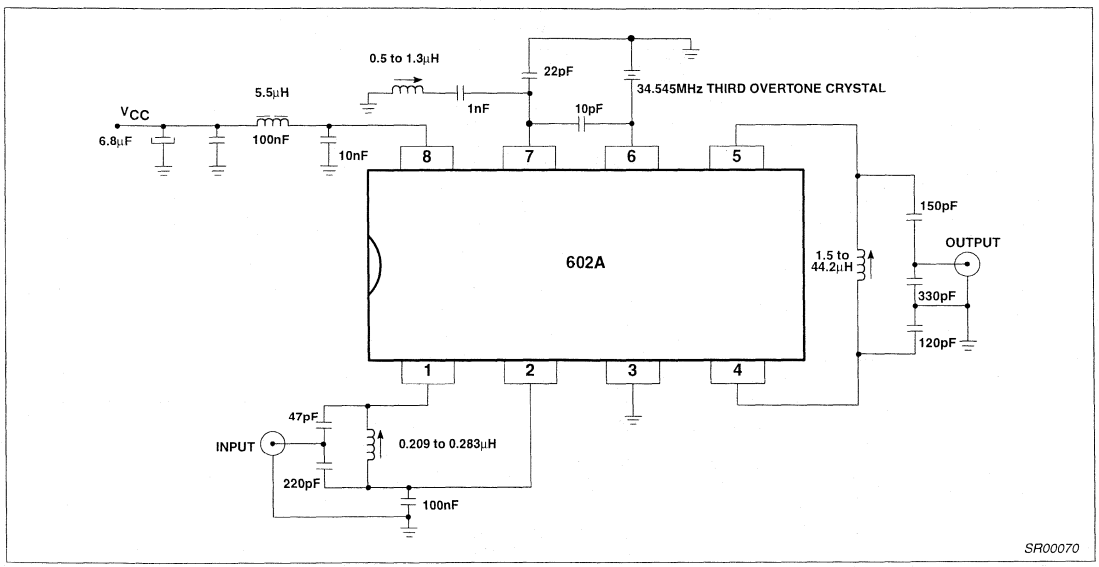


Figure 3. Test Configuration

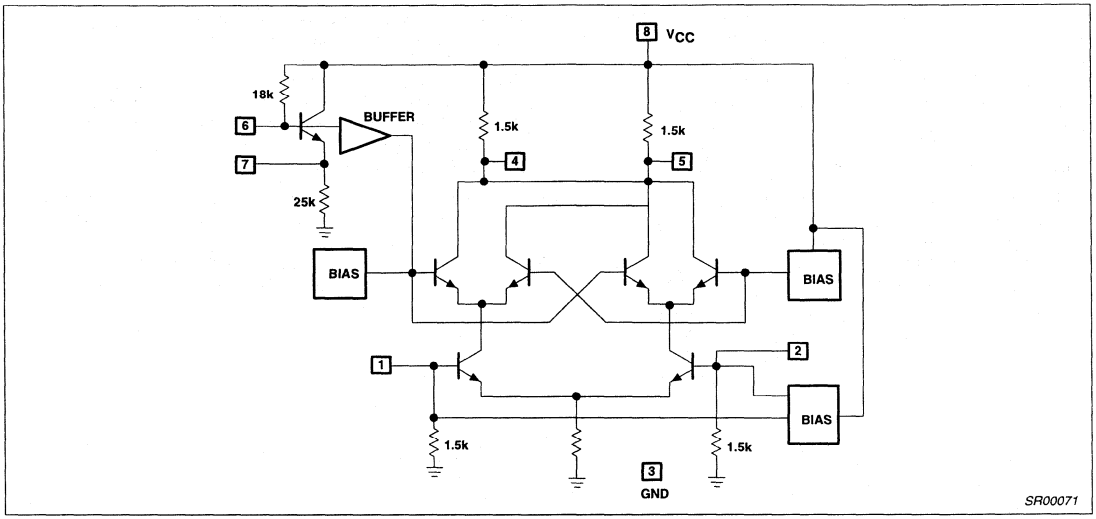


Figure 4. Equivalent Circuit

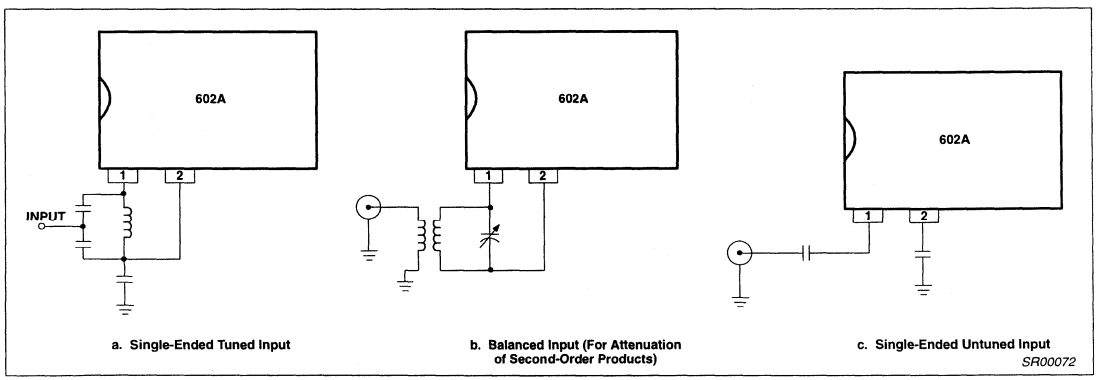


Figure 5. Input Configuration

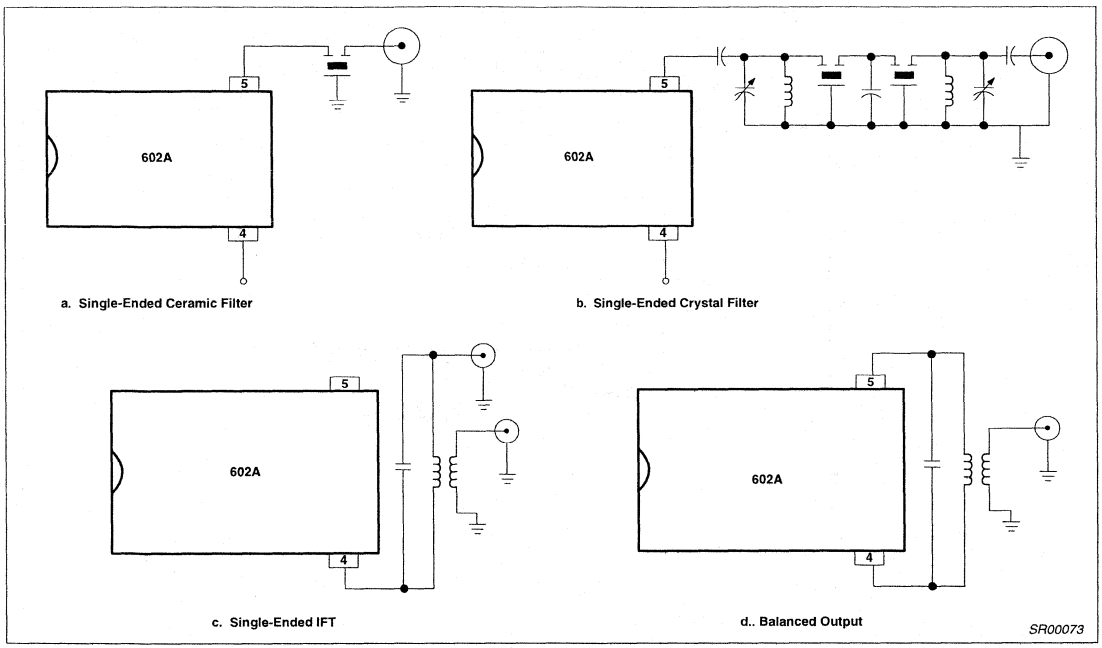


Figure 6. Output Configuration

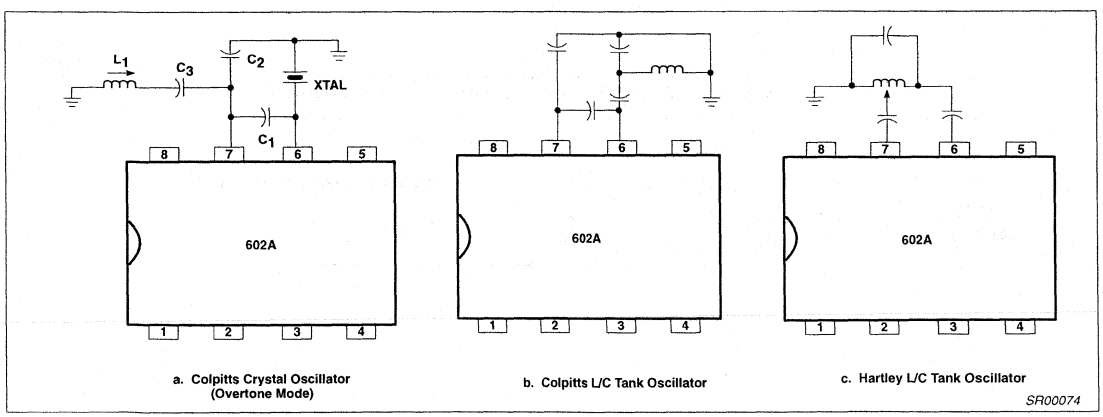


Figure 7. Oscillator Circuits

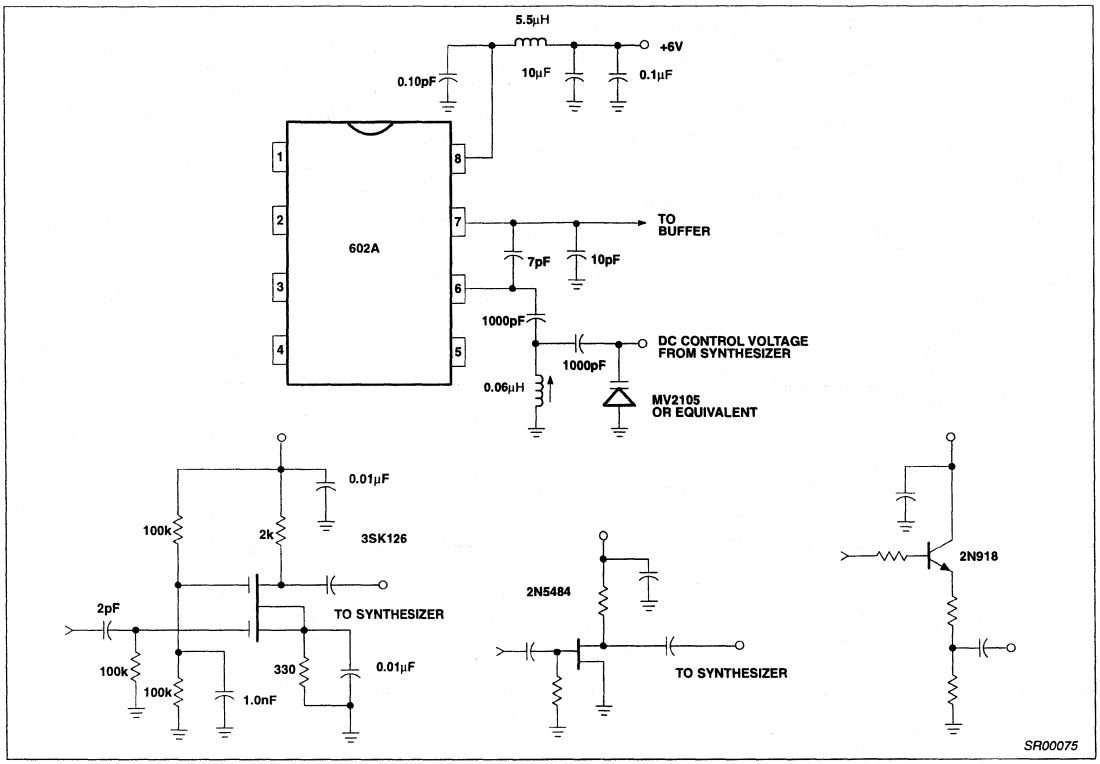


Figure 8. Colpitts Oscillator Suitable for Synthesizer Applications and Typical Buffers

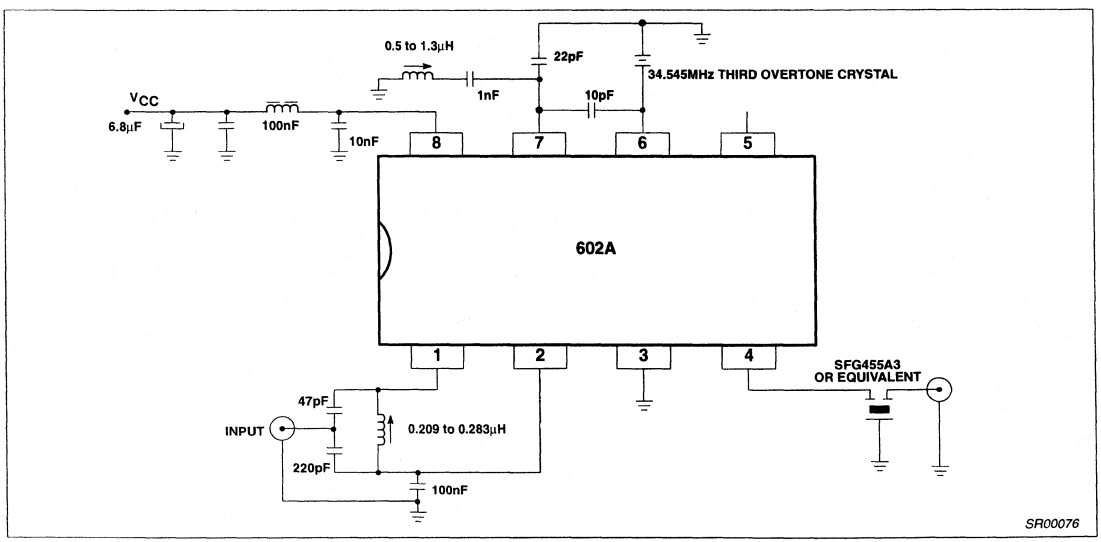


Figure 9. Typical Application for Cellular Radio

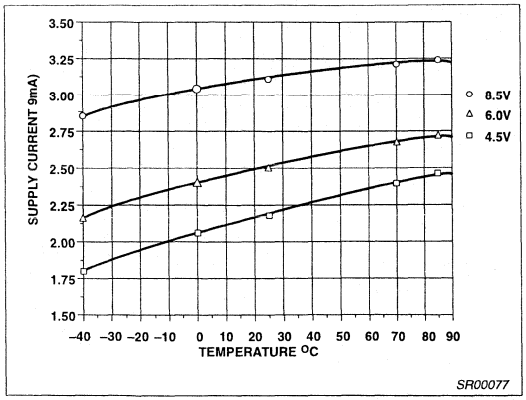


Figure 10. I_{CC} vs Supply Voltage

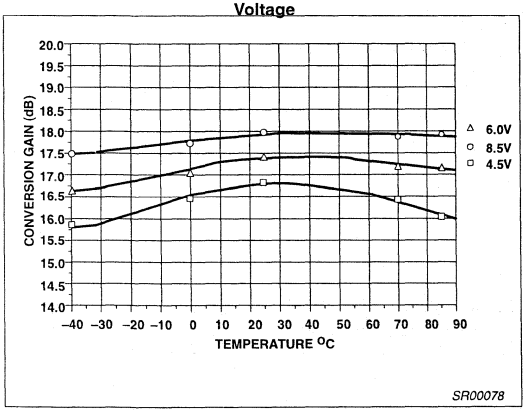


Figure 11. Conversion Gain vs Supply Voltage

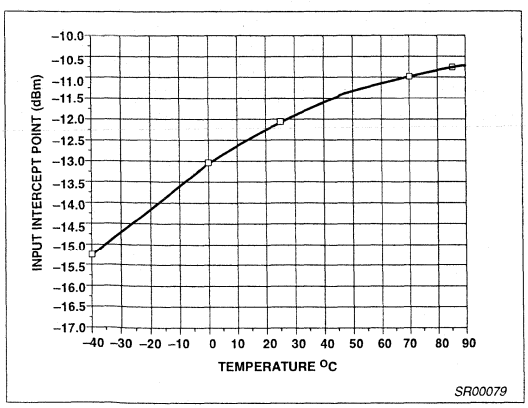


Figure 12. Third-Order Intercept Point

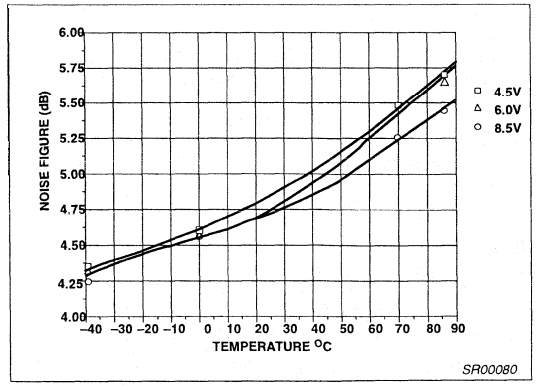


Figure 13. Noise Figure

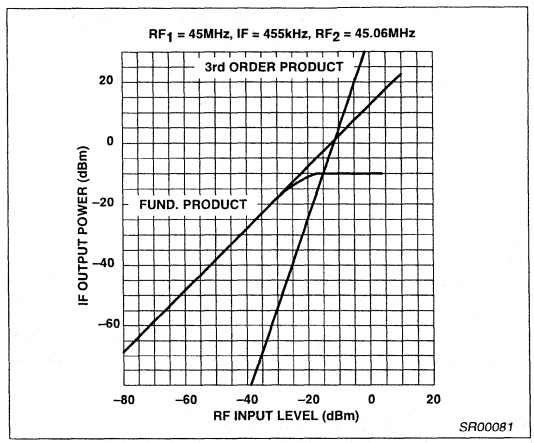


Figure 14. Third-Order Intercept and Compression

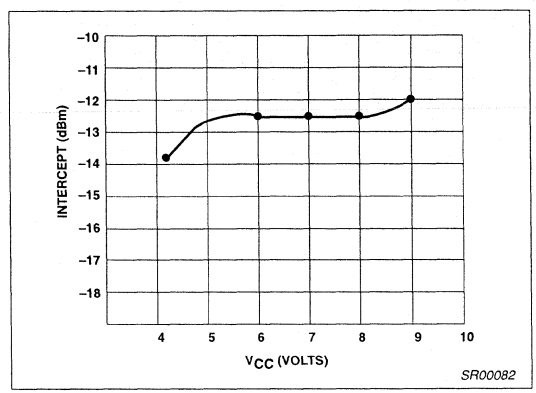


Figure 15. Input Third-Order Intermod Point vs V_{CC}

High performance low power FM IF system SA604A

DESCRIPTION

The SA604A is an improved monolithic low-power FM IF system incorporating two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic received signal strength indicator, and voltage regulator. The SA604A features higher IF bandwidth (25MHz) and temperature compensated RSSI and limiters permitting higher performance application compared with the SA604. The SA604A is available in a 16-lead SO (surface-mounted miniature) package.

FEATURES

- Low power consumption: 3.3mA typical
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- Two audio outputs - muted and unmuted
- Low external component count; suitable for crystal/ceramic filters
- Excellent sensitivity: 1.5μV across input pins (0.22μV into 50Ω matching network) for 12dB SINAD (Signal to Noise and Distortion ratio) at 455kHz
- SA604A meets cellular radio specifications

PIN CONFIGURATION

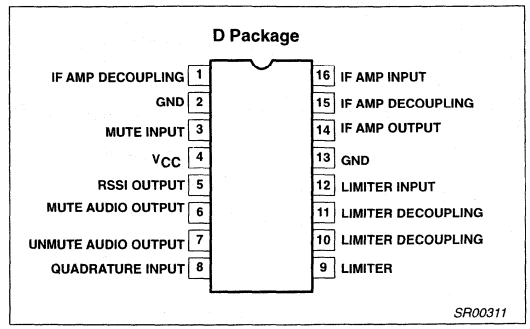


Figure 1. Pin Configuration

APPLICATIONS

- Cellular radio FM IF
- High performance communications receivers
- Intermediate frequency amplification and detection up to 25MHz
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Small Outline (SO) package (Surface-mount)	-40 to +85°C	SA604AD	SOT109-1

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	9	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range SA604A	40 to +85	°C
θ_{JA}	Thermal impedance D package	90	°C/W

BLOCK DIAGRAM

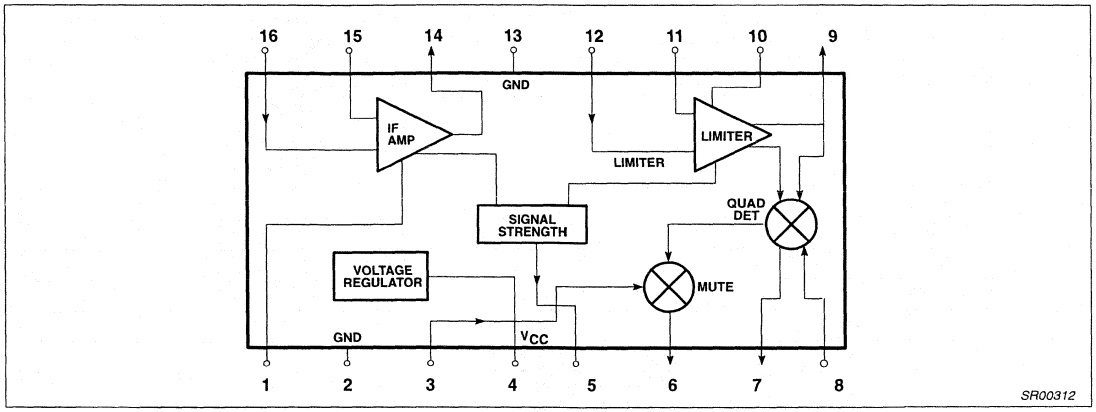


Figure 2. Block Diagram

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA604A			
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		4.5		8.0	V
I_{CC}	DC current drain		2.5	3.3	4.0	mA
	Mute switch input threshold (ON) (OFF)		1.7		 1.0	V V

AC ELECTRICAL CHARACTERISTICS

Typical reading at $T_A = 25^{\circ}C$; $V_{CC} = \pm 6V$, unless otherwise stated. IF frequency = 455kHz; IF level = -47dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 3. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA604A			
			MIN	TYP	MAX	
	Input limiting -3dB	Test at Pin 16		-92		dBm/50Ω
	AM rejection	80% AM 1kHz	30	34		dB
	Recovered audio level	15nF de-emphasis	80	175	260	mV_{RMS}
	Recovered audio level	150pF de-emphasis		530		mV_{RMS}
THD	Total harmonic distortion		-34	-42		dB
S/N	Signal-to-noise ratio	No modulation for noise		73		dB
	RSSI output[1]	RF level = -118dBm	0	160	650	mV
		RF level = -68dBm	1.9	2.65	3.1	V
		RF level = -18dBm	4.0	4.85	5.6	V
	RSSI range	R_4 = 100k (Pin 5)		90		dB
	RSSI accuracy	R_4 = 100k (Pin 5)		±1.5		dB
	IF input impedance		1.4	1.6		kΩ
	IF output impedance		0.85	1.0		kΩ
	Limiter input impedance		1.4	1.6		kΩ
	Unmuted audio output resistance			58		kΩ
	Muted audio output resistance			58		kΩ

NOTE:

1. SA604 data sheets refer to power at 50Ω input termination; about 21dB less power actually enters the internal 1.5k input.

SA604 (50)	SA604A (1.5k)/SA605 (1.5k
-97dBm	-118dBm
-47dBm	-68dBm
+3dBm	-18dBm

The SA605 and SA604A are both derived from the same basic die. The SA605 performance plots are directly applicable to the SA604A.

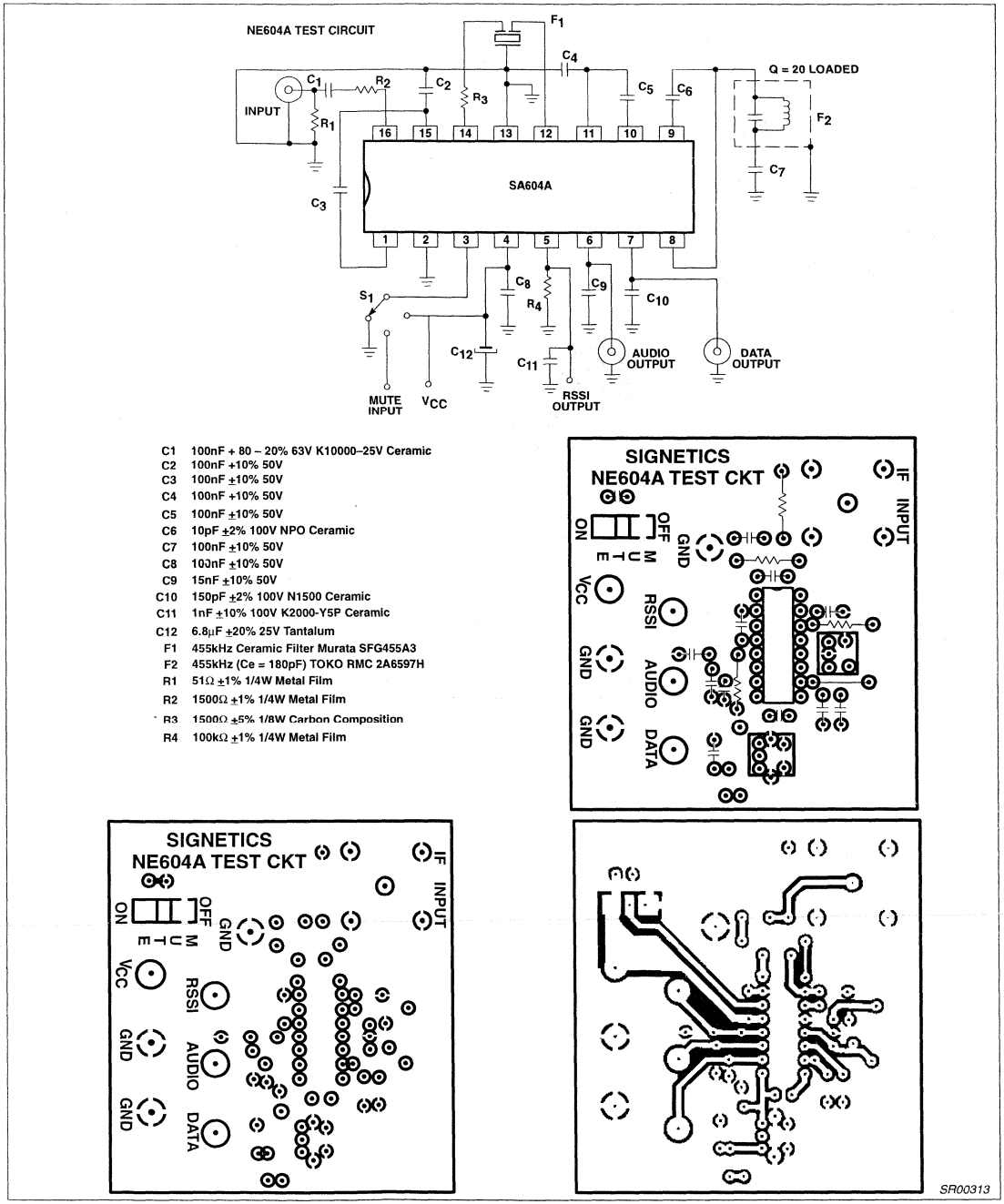


Figure 3. SA604A Test Circuit

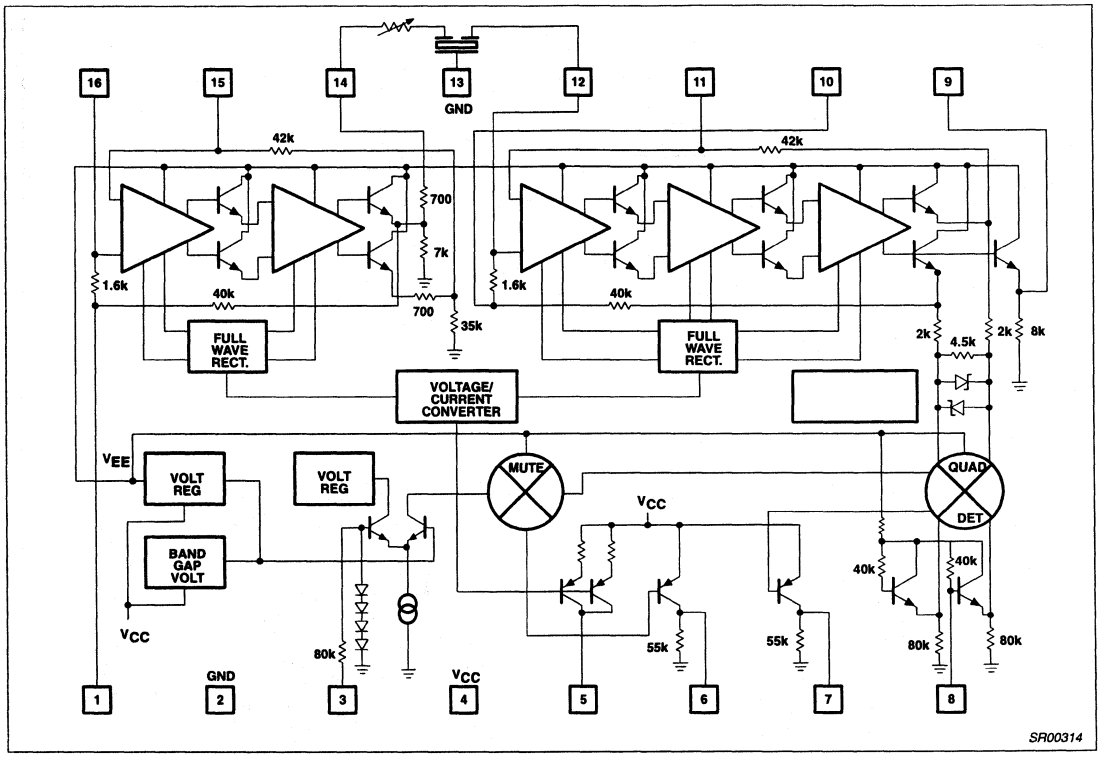


Figure 4. Equivalent Circuit

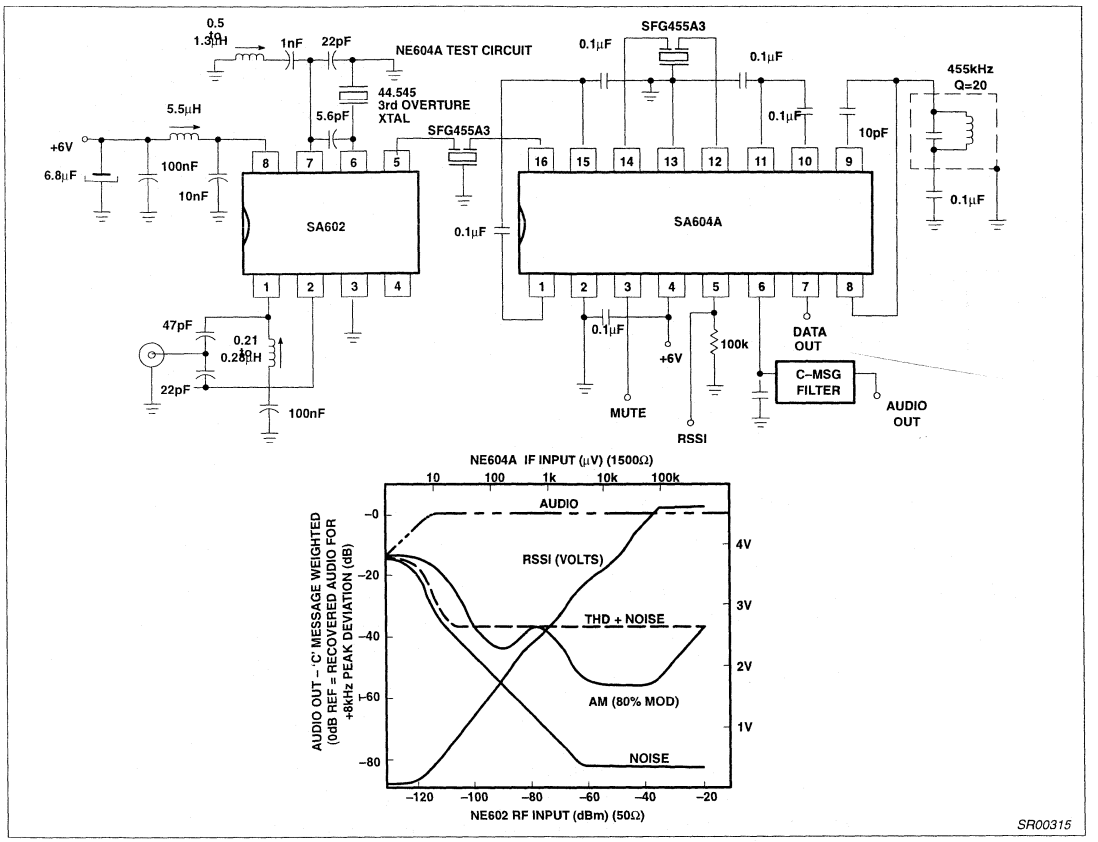


Figure 5. Typical Application Cellular Radio (45MHz to 455kHz)

CIRCUIT DESCRIPTION

The SA604A is a very high gain, high frequency device. Correct operation is not possible if good RF layout and gain stage practices are not used. The SA604A cannot be evaluated independent of circuit, components, and board layout. A physical layout which correlates to the electrical limits is shown in Figure 3. This configuration can be used as the basis for production layout.

The SA604A is an IF signal processing system suitable for IF frequencies as high as 21.4MHz. The device consists of two limiting amplifiers, quadrature detector, direct audio output, muted audio output, and signal strength indicator (with output characteristic). The sub-systems are shown in Figure 4. A typical application with 45MHz input and 455kHz IF is shown in Figure 5.

IF Amplifiers

The IF amplifier section consists of two log-limiting stages. The first consists of two differential amplifiers with 39dB of gain and a small signal bandwidth of 41MHz (when driven from a 50Ω source). The output of the first limiter is a low impedance emitter follower with 1kΩ of equivalent series resistance. The second limiting stage consists of three differential amplifiers with a gain of 62dB and a small signal AC bandwidth of 28MHz. The outputs of the final differential stage are buffered to the internal quadrature detector. One of the outputs is available at Pin 9 to drive an external quadrature capacitor and L/C quadrature tank.

Both of the limiting amplifier stages are DC biased using feedback. The buffered output of the final differential amplifier is fed back to the input through 42kΩ resistors. As shown in Figure 4, the input impedance is established for each stage by tapping one of the feedback resistors 1.6kΩ from the input. This requires one additional decoupling capacitor from the tap point to ground.

Because of the very high gain, bandwidth and input impedance of the limiters, there is a very real potential for instability at IF frequencies above 455kHz. The basic phenomenon is shown in Figure 8. Distributed feedback (capacitance, inductance and radiated fields)

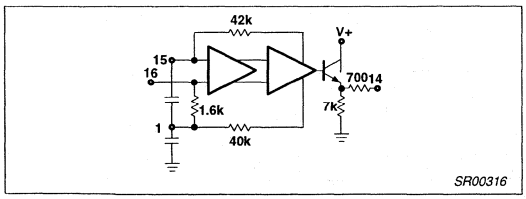


Figure 6. First Limiter Bias

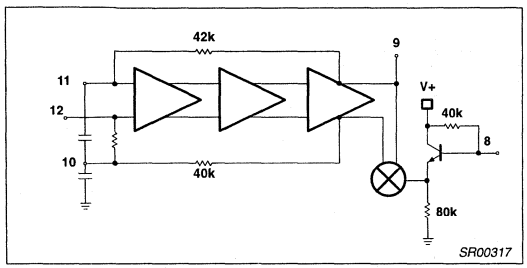


Figure 7. Second Limiter and Quadrature Detector

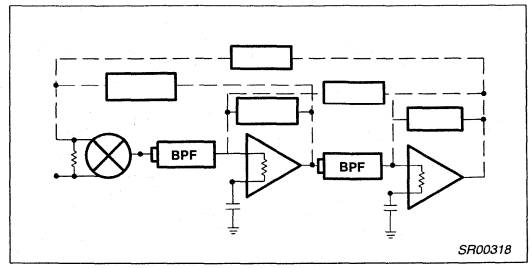


Figure 8. Feedback Paths

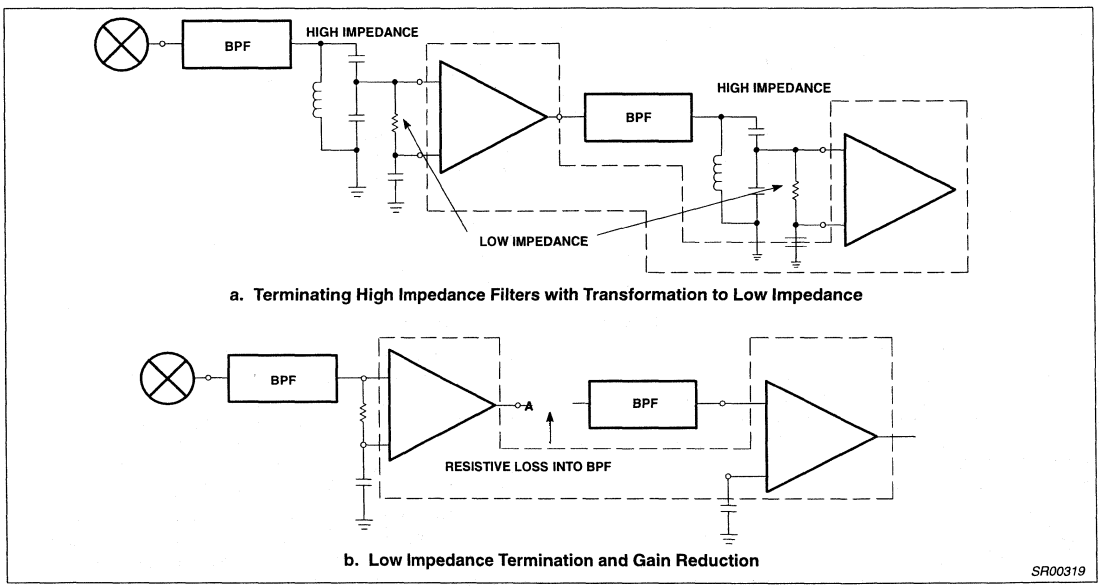


Figure 9. Practical Termination

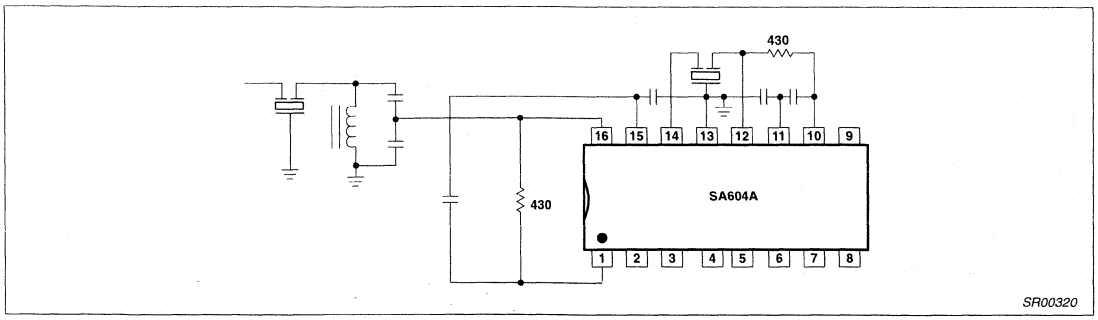


Figure 10. Crystal Input Filter with Ceramic Interstage Filter

forms a divider from the output of the limiters back to the inputs (including RF input). If this feedback divider does not cause attenuation greater than the gain of the forward path, then oscillation or low level regeneration is likely. If regeneration occurs, two symptoms may be present: (1)The RSSI output will be high with no signal input (should nominally be 250mV or lower), and (2) the demodulated output will demonstrate a threshold. Above a certain input level, the limited signal will begin to dominate the regeneration, and the demodulator will begin to operate in a "normal" manner.

There are three primary ways to deal with regeneration: (1) Minimize the feedback by gain stage isolation, (2) lower the stage input impedances, thus increasing the feedback attenuation factor, and (3) reduce the gain. Gain reduction can effectively be accomplished by adding attenuation between stages. This can also lower the input impedance if well planned. Examples of impedance/gain adjustment are shown in Figure 9. Reduced gain will result in reduced limiting sensitivity.

A feature of the SA604A IF amplifiers, which is not specified, is low phase shift. The SA604A is fabricated with a 10GHz process with very small collector capacitance. It is advantageous in some applications that the phase shift changes only a few degrees over a wide range of signal input amplitudes.

Stability Considerations

The high gain and bandwidth of the SA604A in combination with its very low currents permit circuit implementation with superior performance. However, stability must be maintained and, to do that, every possible feedback mechanism must be addressed. These mechanisms are: 1) Supply lines and ground, 2) stray layout inductances and capacitances, 3) radiated fields, and 4) phase shift. As the system IF increases, so must the attention to fields and strays. However, ground and supply loops cannot be overlooked, especially at lower frequencies. Even at 455kHz, using the test layout in Figure 3, instability will occur if the supply line is not decoupled with two high quality RF capacitors, a 0.1µF monolithic right at the V_{CC} pin, and a 6.8µF tantalum on the supply line. An electrolytic is not an adequate substitute. At 10.7MHz, a 1µF tantalum has proven acceptable with this layout. Every layout must be evaluated on its own merit, but don't underestimate the importance of good supply bypass.

At 455kHz, if the layout of Figure 3 or one substantially similar is used, it is possible to directly connect ceramic filters to the input and between limiter stages with no special consideration. At frequencies above 2MHz, some input impedance reduction is usually necessary. Figure 9 demonstrates a practical means.

As illustrated in Figure 10, 430Ω external resistors are applied in parallel to the internal 1.6kΩ load resistors, thus presenting approximately 330Ω to the filters. The input filter is a crystal type for narrowband selectivity. The filter is terminated with a tank which transforms to 330Ω. The interstage filter is a ceramic type which doesn't contribute to system selectivity, but does suppress wideband noise and stray signal pickup. In wideband 10.7MHz IFs the input filter can also be ceramic, directly connected to Pin 16.

In some products it may be impractical to utilize shielding, but this mechanism may be appropriate to 10.7MHz and 21.4MHz IF. One of the benefits of low current is lower radiated field strength, but lower does not mean non-existent. A spectrum analyzer with an active probe will clearly show IF energy with the probe held in the proximity of the second limiter output or quadrature coil. No specific recommendations are provided, but mechanical shielding should be considered if layout, bypass, and input impedance reduction do not solve a stubborn instability.

The final stability consideration is phase shift. The phase shift of the limiters is very low, but there is phase shift contribution from the quadrature tank and the filters. Most filters demonstrate a large phase shift across their passband (especially at the edges). If the quadrature detector is tuned to the edge of the filter passband, the combined filter and quadrature phase shift can aggravate stability. This is not usually a problem, but should be kept in mind.

Quadrature Detector

Figure 7 shows an equivalent circuit of the SA604A quadrature detector. It is a multiplier cell similar to a mixer stage. Instead of mixing two different frequencies, it mixes two signals of common frequency but different phase. Internal to the device, a constant amplitude (limited) signal is differentially applied to the lower port of the multiplier. The same signal is applied single-ended to an external capacitor at Pin 9. There is a 90° phase shift across the plates of this capacitor, with the phase shifted signal applied to the upper port of the multiplier at Pin 8. A quadrature tank (parallel L/C network) permits frequency selective phase shifting at the IF frequency. This quadrature tank must be returned to ground through a DC blocking capacitor.

The loaded Q of the quadrature tank impacts three fundamental aspects of the detector: Distortion, maximum modulated peak deviation, and audio output amplitude. Typical quadrature curves are illustrated in Figure 12. The phase angle translates to a shift in the multiplier output voltage.

Thus a small deviation gives a large output with a high Q tank. However, as the deviation from resonance increases, the non-linearity of the curve increases (distortion), and, with too much deviation, the signal will be outside the quadrature region (limiting the peak deviation which can be demodulated). If the same peak deviation is applied to a lower Q tank, the deviation will remain in a region of the curve which is more linear (less distortion), but creates a smaller phase angle (smaller output amplitude). Thus the Q of the quadrature tank must be tailored to the design. Basic equations and an example for determining Q are shown below. This explanation includes first-order effects only.

Frequency Discriminator Design Equations for SA604A

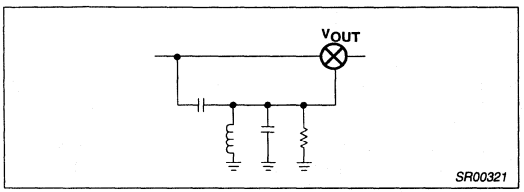


Figure 11.

$$V_O = \frac{C_S}{C_P + C_S} \bullet \frac{1}{1 + \frac{\omega_1}{Q_1 S} + \left(\frac{\omega_1}{S}\right)^2} \bullet V_{IN} \quad (1a)$$

$$\text{where } \omega_1 = \frac{1}{\sqrt{L(C_P + C_S)}} \quad (1b)$$

$$Q_1 = R\,(C_P + C_S)\,\omega_1 \quad (1c)$$

From the above equation, the phase shift between nodes 1 and 2, or the phase across C_S will be:

$$\phi = \angle V_O - \angle V_{IN} = t_g^{-1}\left[\frac{\frac{\omega_1}{Q_1\omega}}{1 - \left(\frac{\omega_1}{\omega}\right)^2}\right] \quad (2)$$

Figure 12 is the plot of ϕ vs. $\left(\frac{\omega}{\omega_1}\right)$

It is notable that at $\omega = \omega_1$, the phase shift is $\frac{\pi}{2}$ and the response is close to a straight line with a slope of $\frac{\Delta\phi}{\Delta\omega} = \frac{2Q_1}{\omega_1}$

The signal V_O would have a phase shift of $\left[\frac{\pi}{2} - \frac{2Q_1}{\omega_1}\,\omega\right]$ with respect to the V_{IN}.

If $V_{IN} = A \sin \omega t \Rightarrow V_O = A$ (3)

$$\sin\left[\omega t + \frac{\pi}{2} - \frac{2Q_1}{\omega_1}\,\omega\right]$$

Multiplying the two signals in the mixer, and low pass filtering yields:

$V_{IN} \bullet V_O = A^2 \sin \omega t$ (4)

$$\sin\left[\omega t + \frac{\pi}{2} - \frac{2Q_1}{\omega_1}\,\omega\right]$$

after low pass filtering

$$\Rightarrow V_{OUT} = \frac{1}{2} A^2 \cos\left[\frac{\pi}{2} - \frac{2Q_1}{\omega_1}\,\omega\right] \quad (5)$$

$$= \frac{1}{2} A^2 \sin\left(\frac{2Q_1}{\omega_1}\right)\omega$$

$$V_{OUT} \propto 2Q_1 \frac{\omega}{\omega_1} = \left[2Q_1\left(\frac{\omega_1 + \Delta\omega}{\omega_1}\right)\right] \quad (6)$$

For $\frac{2Q_1\omega}{\omega_1} << \frac{\pi}{2}$

Which is discriminated FM output. (Note that $\Delta\omega$ is the deviation frequency from the carrier ω_1.

Ref. Krauss, Raab, Bastian; Solid State Radio Eng.; Wiley, 1980, p. 311. Example: At 455kHz IF, with ±5kHz FM deviation. The maximum normalized frequency will be

$$\frac{455 \pm 5\text{kHz}}{455} = 1.010 \text{ or } 0.990$$

Go to the f vs. normalized frequency curves (Figure 12) and draw a vertical straight line at $\frac{\omega}{\omega_1} = 1.01$.

The curves with Q = 100, Q = 40 are not linear, but Q = 20 and less shows better linearity for this application. Too small Q decreases the amplitude of the discriminated FM signal. (Eq. 6) $\Rightarrow$ Choose a Q = 20

The internal R of the 604A is 40k. From Eq. 1c, and then 1b, it results that

$C_P + C_S = 174\text{pF}$ and $L = 0.7\text{mH}$.

A more exact analysis including the source resistance of the previous stage shows that there is a series and a parallel resonance in the phase detector tank. To make the parallel and series resonances close, and to get maximum attenuation of higher harmonics at 455kHz IF, we have found that a $C_S = 10\text{pF}$ and $C_P = 164\text{pF}$ (commercial values of 150pF or 180pF may be practical), will give the best results. A variable inductor which can be adjusted around 0.7mH should be chosen and optimized for minimum distortion. (For 10.7MHz, a value of $C_S = 1\text{pF}$ is recommended.)

Audio Outputs

Two audio outputs are provided. Both are PNP current-to-voltage converters with 55kΩ nominal internal loads. The unmuted output is always active to permit the use of signaling tones in systems such as cellular radio. The other output can be muted with 70dB typical attenuation. The two outputs have an internal 180° phase difference.

The nominal frequency response of the audio outputs is 300kHz. this response can be increased with the addition of external resistors from the output pins to ground in parallel with the internal 55k resistors, thus lowering the output time constant. Singe the output structure is a current-to-voltage converter (current is driven into the resistance, creating a voltage drop), adding external parallel resistance also has the effect of lowering the output audio amplitude and DC level.

This technique of audio bandwidth expansion can be effective in many applications such as SCA receivers and data transceivers. Because the two outputs have a 180° phase relationship, FSK demodulation can be accomplished by applying the two output

differentially across the inputs of an op amp or comparator. Once the threshold of the reference frequency (or "no-signal" condition) has been established, the two outputs will shift in opposite directions (higher or lower output voltage) as the input frequency shifts. The output of the comparator will be logic output. The choice of op amp or comparator will depend on the data rate. With high IF frequency (10MHz and above), and wide IF bandwidth (L/C filters) data rates in excess of 4Mbaud are possible.

RSSI

The "received signal strength indicator", or RSSI, of the SA604A demonstrates monotonic logarithmic output over a range of 90dB. The signal strength output is derived from the summed stage currents in the limiting amplifiers. It is essentially independent of the IF frequency. Thus, unfiltered signals at the limiter inputs, spurious products, or regenerated signals will manifest themselves as RSSI outputs. An RSSI output of greater than 250mV with no signal (or a very small signal) applied, is an indication of possible regeneration or oscillation.

In order to achieve optimum RSSI linearity, there must be a 12dB insertion loss between the first and second limiting amplifiers. With a typical 455kHz ceramic filter, there is a nominal 4dB insertion loss in the filter. An additional 6dB is lost in the interface between the filter and the input of the second limiter. A small amount of additional loss must be introduced with a typical ceramic filter. In the test circuit used for cellular radio applications (Figure 5) the optimum linearity was achieved with a 5.1kΩ resistor from the output of the first limiter (Pin 14) to the input of the interstage filter. With this resistor from Pin 14 to the filter, sensitivity of 0.25μV for 12dB SINAD was achieved. With the 3.6kΩ resistor, sensitivity was optimized at 0.22μV for 12dB SINAD with minor change in the RSSI linearity.

Any application which requires optimized RSSI linearity, such as spectrum analyzers, cellular radio, and certain types of telemetry, will require careful attention to limiter interstage component selection. This will be especially true with high IF frequencies which require insertion loss or impedance reduction for stability.

At low frequencies the RSSI makes an excellent logarithmic AC voltmeter.

For data applications the RSSI is effective as an amplitude shift keyed (ASK) data slicer. If a comparator is applied to the RSSI and the threshold set slightly above the no signal level, when an in-band signal is received the comparator will be sliced. Unlike FSK demodulation, the maximum data rate is somewhat limited. An internal capacitor limits the RSSI frequency response to about 100kHz. At high data rates the rise and fall times will not be symmetrical.

The RSSI output is a current-to-voltage converter similar to the audio outputs. However, an external resistor is required. With a 91kΩ resistor, the output characteristic is 0.5V for a 10dB change in the input amplitude.

Additional Circuitry

Internal to the SA604A are voltage and current regulators which have been temperature compensated to maintain the performance of the device over a wide temperature range. These regulators are not accessible to the user.

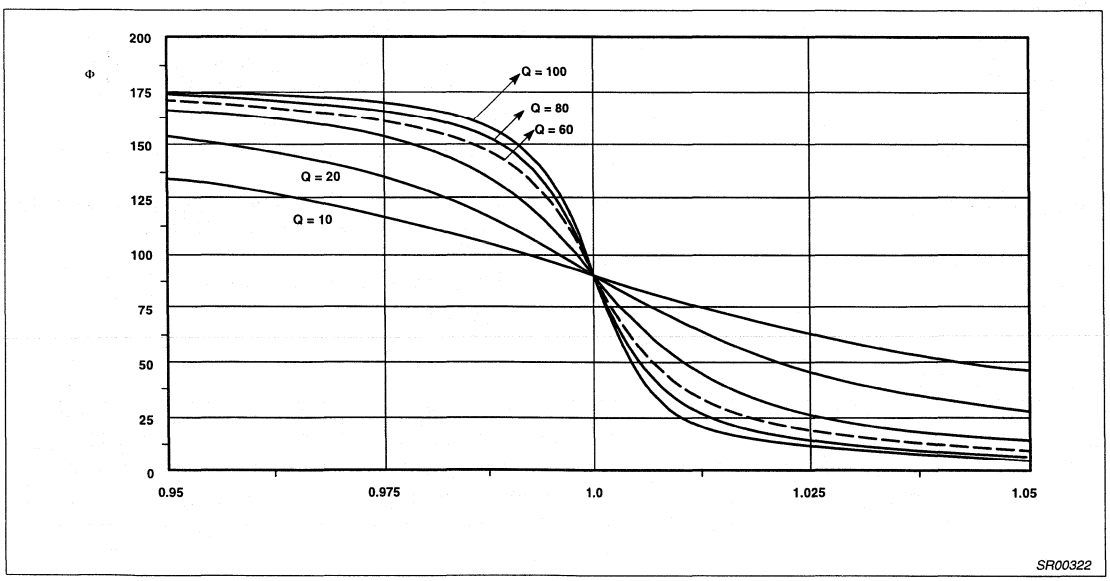


Figure 12. Phase vs Normalized IF Frequency $\frac{\omega}{\omega_1}$ $1 \pm \frac{\Delta\omega}{\omega_1}$

High performance low power mixer FM IF system SA605

DESCRIPTION

The SA605 is a high performance monolithic low-power FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic received signal strength indicator (RSSI), and voltage regulator. The SA605 combines the functions of Signetics' SA602 and SA604A, but features a higher mixer input intercept point, higher IF bandwidth (25MHz) and temperature compensated RSSI and limiters permitting higher performance application. The SA605 is available in 20-lead dual-in-line plastic, 20-lead SOL (surface-mounted miniature package) and 20-lead SSOP (shrink small outline package).

The SA605 and SA615 are functionally the same device types. The difference between the two devices lies in the guaranteed specifications. The SA615 has a higher I_{CC}, lower input third order intercept point, lower conversion mixer gain, lower limiter gain, lower AM rejection, lower SINAD, higher THD, and higher RSSI error than the SA605. Both the SA605 and SA615 devices will meet the EIA specifications for AMPS and TACS cellular radio applications.

For additional technical information please refer to application notes AN1994, 1995 and 1996, which include example application diagrams, a complete overview of the product, and artwork for reference.

APPLICATIONS

- Cellular radio FM IF
- High performance communications receivers
- Single conversion VHF/UHF receivers
- SCA receivers
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Wideband low current amplification

PIN CONFIGURATION

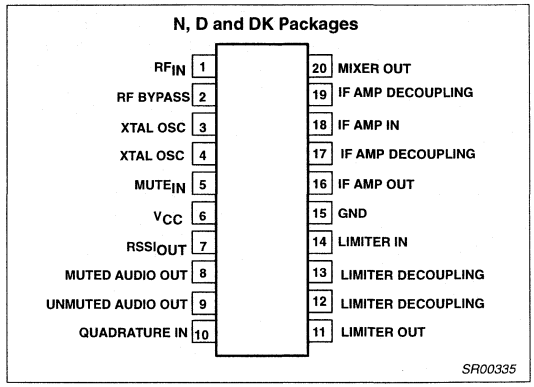


Figure 1. Pin Configuration

FEATURES

- Low power consumption: 5.7mA typical at 6V
- Mixer input to >500MHz
- Mixer conversion power gain of 13dB at 45MHz
- Mixer noise figure of 4.6dB at 45MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator to 1GHz local oscillator can be injected)
- 102dB of IF Amp/Limiter gain
- 25MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- Two audio outputs - muted and unmuted
- Low external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.22μV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone with RF at 45MHz and IF at 455kHz
- SA605 meets cellular radio specifications
- ESD hardened

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Dual In-Line Package (DIP)	–40 to +85°C	SA605N	SOT146-1
20-Pin Plastic Small Outline Large (SOL) package	–40 to +85°C	SA605D	SOT163-1
20-Pin Plastic Shrink Small Outline Package (SSOP)	–40 to +85°C	SA605DK	SOT266-1

BLOCK DIAGRAM

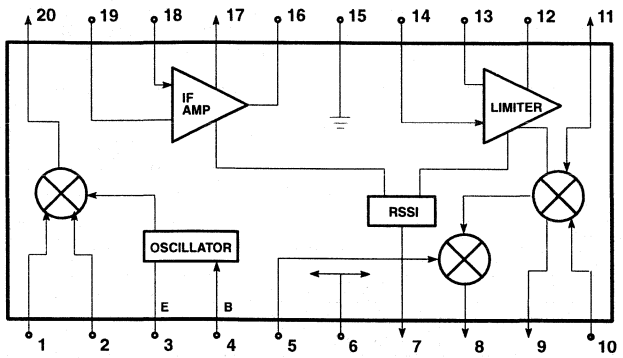


Figure 2. Block Diagram

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	9	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range SA605	–40 to +85	°C
θ_{JA}	Thermal impedance D package N package SSOP package	90 75 117	°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA605			
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		4.5		8.0	V
I_{CC}	DC current drain		4.55	5.7	6.55	mA
	Mute switch input threshold (ON)		1.7			V
	(OFF)				1.0	V

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +6V, unless otherwise stated. RF frequency = 45MHz + 14.5dBV RF input step-up; IF frequency = 455kHz; R17 = 5.1k; RF level = -45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 3. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA605			
			MIN	TYP	MAX	
Mixer/Osc section (ext LO = 300mV)						
f_{IN}	Input signal frequency			500		MHz
f_{OSC}	Crystal oscillator frequency			150		MHz
	Noise figure at 45MHz			5.0		dB
	Third-order input intercept point	f1 = 45.0; f2 = 45.06MHz		-10		dBm
	Conversion power gain	Matched 14.5dBV step-up	10	13	15	dB
		50Ω source		-1.7		dB
	RF input resistance	Single-ended input	3.0	4.7		kΩ
	RF input capacitance			3.5	4.0	pF
	Mixer output resistance	(Pin 20)	1.25	1.5		kΩ
IF section						
	IF amp gain	50Ω source		39.7		dB
	Limiter gain	50Ω source		62.5		dB
	Input limiting -3dB, R_{17} = 5.1k	Test at Pin 18		-113		dBm
	AM rejection	80% AM 1kHz	29	34	43	dB
	Audio level, R_{10} = 100k	15nF de-emphasis	80	150	260	mV_{RMS}
	Unmuted audio level, R_{11} = 100k	150pF de-emphasis		480		mV
	SINAD sensitivity	RF level -118dB		16		dB
THD	Total harmonic distortion		-34	-42		dB
S/N	Signal-to-noise ratio	No modulation for noise		73		dB
	IF RSSI output, R_9 = 100kΩ[1]	IF level = -118dBm	0	160	650	mV
		IF level = -68dBm	1.9	2.5	3.1	V
		IF level = -18dBm	4.0	4.8	5.6	V
	RSSI range	R_9 = 100kΩ Pin 16		90		dB
	RSSI accuracy	R_9 = 100kΩ Pin 16		±1.5		dB
	IF input impedance		1.40	1.6		kΩ
	IF output impedance		0.85	1.0		kΩ
	Limiter input impedance		1.40	1.6		kΩ
	Unmuted audio output resistance			58		kΩ
	Muted audio output resistance			58		kΩ
RF/IF section (int LO)						
	Unmuted audio level	4.5V = V_{CC}, RF level = -27dBm		450		mV_{RMS}
	System RSSI output	4.5V = V_{CC}, RF level = -27dBm		4.3		V

NOTE:

1. The generator source impedance is 50Ω, but the SA605 input impedance at Pin 18 is 1500Ω. As a result, IF level refers to the actual signal that enters the SA605 input (Pin 8) which is about 21dB less than the "available power" at the generator.

CIRCUIT DESCRIPTION

The SA605 is an IF signal processing system suitable for second IF or single conversion systems with input frequency as high as 1GHz. The bandwidth of the IF amplifier is about 40MHz, with 39.7dB(v) of gain from a 50Ω source. The bandwidth of the limiter is about 28MHz with about 62.5dB(v) of gain from a 50Ω source. However, the gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 5dB, conversion gain of 13dB, and input third-order intercept of -10dBm. The oscillator will operate in excess of 1GHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

The output of the mixer is internally loaded with a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. To achieve optimum linearity of the log signal strength indicator, there must be a 12dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dB(v) insertion loss, a fixed or variable resistor can be added between the first IF output (Pin 16) and the interstage network.

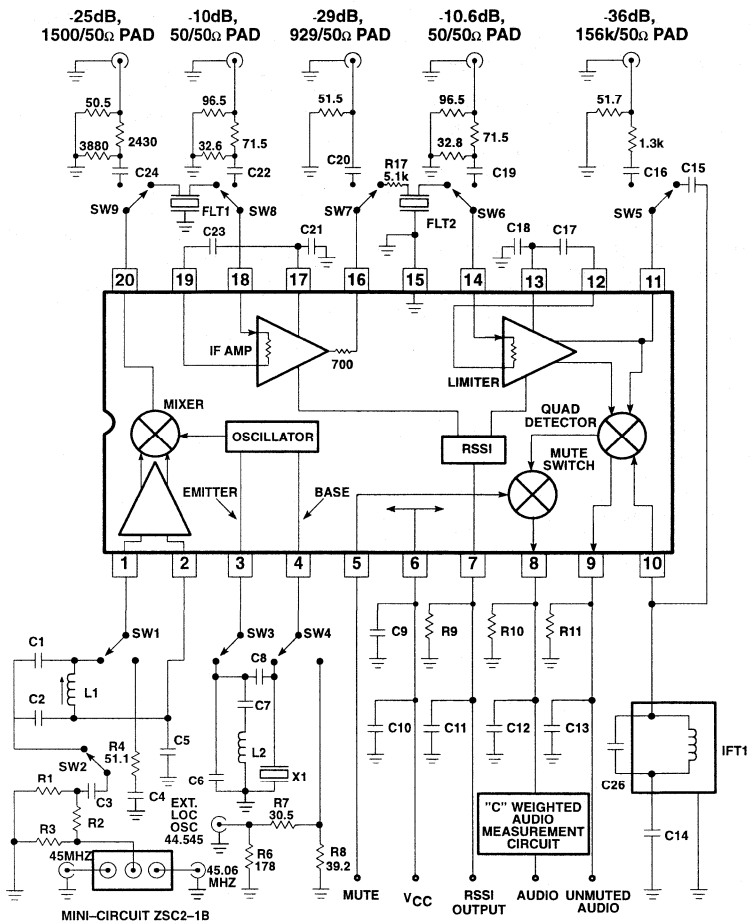
The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

Overall, the IF section has a gain of 90dB. For operation at intermediate frequencies greater than 455kHz, special care must be given to layout, termination, and interstage loss to avoid instability.

The demodulated output of the quadrature detector is available at two pins, one continuous and one with a mute switch. Signal attenuation with the mute activated is greater than 60dB. The mute input is very high impedance and is compatible with CMOS or TTL levels.

A log signal strength completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone.

NOTE: $dB(v) = 20\log V_{OUT}/V_{IN}$



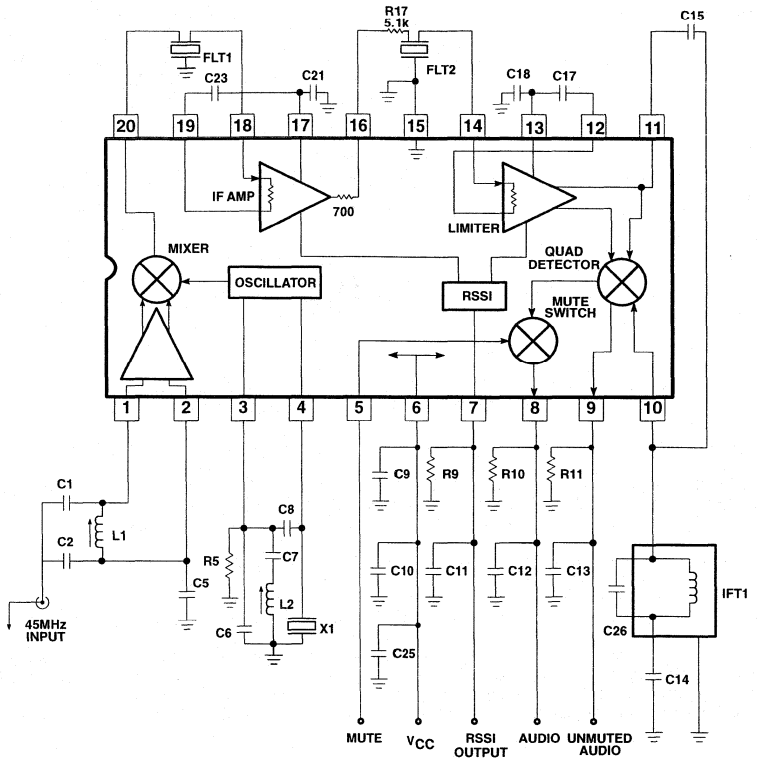
Automatic Test Circuit Component List

C1	47pF NPO Ceramic	C21	100nF ±10% Monolithic Ceramic
C2	180pF NPO Ceramic	C23	100nF ±10% Monolithic Ceramic
C5	100nF ±10% Monolithic Ceramic	C25	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic	C26	390pF ±10% Monolithic Ceramic
C7	1nF Ceramic	Flt 1	Ceramic Filter Murata SFG455A3 or equiv
C8	10.0pF NPO Ceramic	Flt 2	Ceramic Filter Murata SFG455A3 or equiv
C9	100nF ±10% Monolithic Ceramic	IFT 1	455kHz 270µH TOKO #303LN-1129
C10	6.8µF Tantalum (minimum) *	L1	300nH TOKO #5CB-1055Z
C11	100nF ±10% Monolithic Ceramic	L2	0.8µH TOKO 292CNS–T1038Z
C12	15nF ±10% Ceramic	X1	44.545MHz Crystal ICM4712701
C13	150pF ±2% N1500 Ceramic	R9	100k ±1% 1/4W Metal Film
C14	100nF ±10% Monolithic Ceramic	R17	5.1k ±5% 1/4W Carbon Composition
C15	10pF NPO Ceramic	R10	100k ±1% 1/4W Metal Film (optional)
C17	100nF ±10% Monolithic Ceramic	R11	100k ±1% 1/4W Metal Film (optional)
C18	100nF ±10% Monolithic Ceramic		

* NOTE: This value can be reduced when a battery is the power source.

SR00337

Figure 3. SA605 45MHz Test Circuit (Relays as shown)



Application Component List

C1	47pF NPO Ceramic
C2	180pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	6.8µF Tantalum (minimum)
C11	100nF ±10% Monolithic Ceramic
C12	15nF ±10% Ceramic
C13	150pF ±2% N1500 Ceramic
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
C26	390pF ±10% Monolithic Ceramic
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	455kHz 270µH TOKO #303LN-1129
L1	300nH TOKO #5CB-1055Z
L2	0.8µH TOKO 292CNS–T1038Z
X1	44.545MHz Crystal ICM4712701
R9	100k ±1% 1/4W Metal Film
R17	5.1k ±5% 1/4W Carbon Composition
R10	100k ±1% 1/4W Metal Film (optional)
R11	100k ±1% 1/4W Metal Film (optional)

* NOTE: This value can be reduced when a battery is the power source.

SR00338

Figure 4. SA605 45MHz Application Circuit

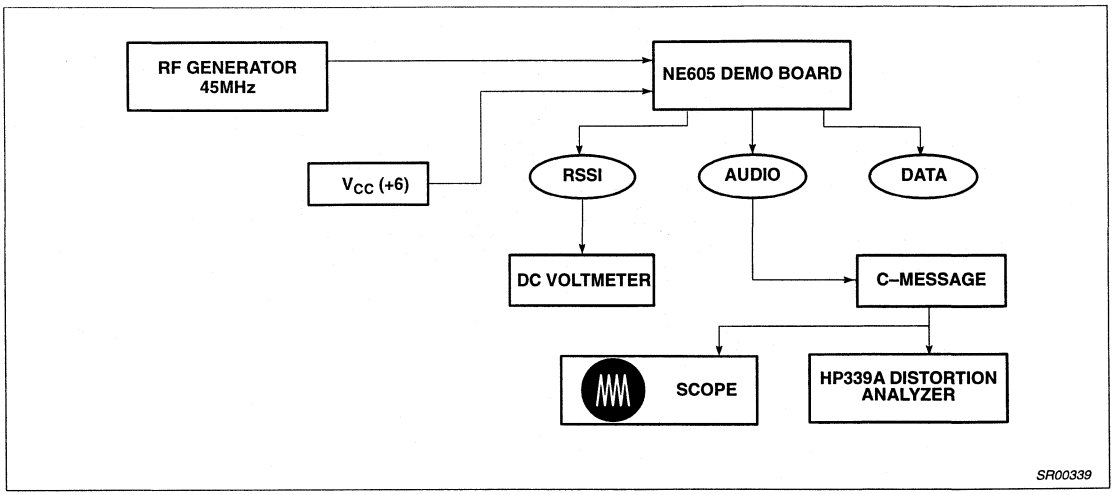


Figure 5. SA605 Application Circuit Test Set Up

NOTES:

1. C-message: The C-message filter has a peak gain of 100 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339 analyzer.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All of our specifications and testing are done with the more wideband filter.
3. RF generator: Set your RF generator at 45.000MHz, use a 1kHz modulation frequency and a 6kHz deviation if you use 16kHz filters, or 8kHz if you use 30kHz filters.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.22μV or -120dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 250mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10-15μF or higher value tantalum capacitor on the supply line is essential. A low frequency ESR screening test on this capacitor will ensure consistent good sensitivity in production. A 0.1μF bypass capacitor on the supply pin, and grounded near the 44.545MHz oscillator improves sensitivity by 2-3dB.
8. R5 can be used to bias the oscillator transistor at a higher current for operation above 45MHz. Recommended value is 22kΩ, but should not be below 10kΩ.

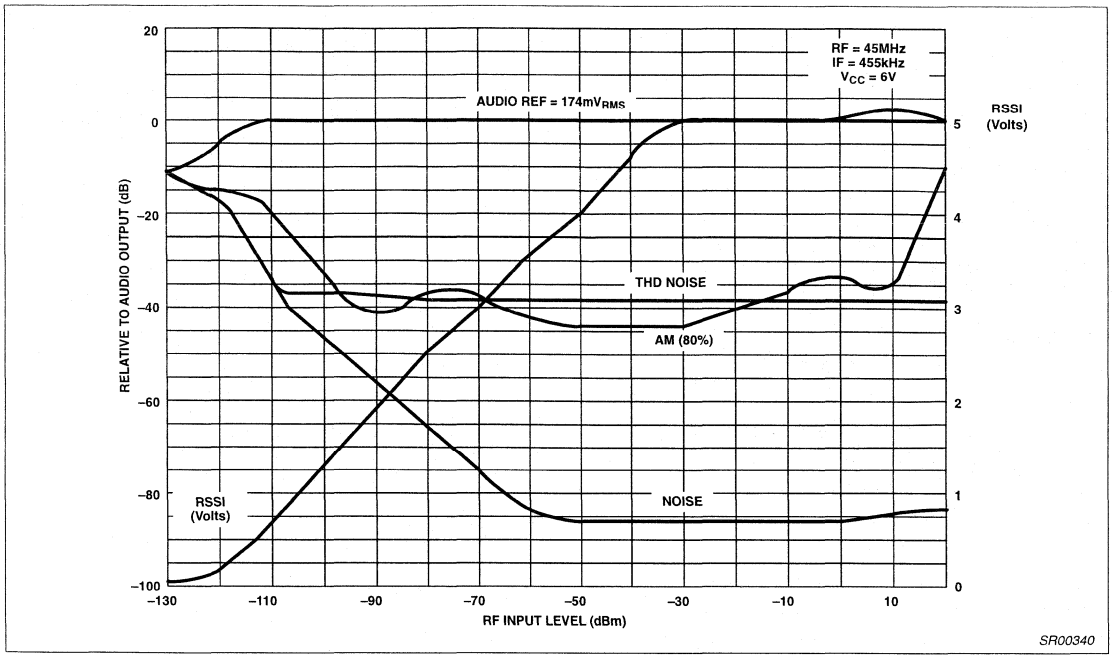


Figure 6. SA605 Application Board at 25°C

Low-voltage high performance mixer FM IF system SA606

DESCRIPTION

The SA606 is a low-voltage high performance monolithic FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, logarithmic received signal strength indicator (RSSI), voltage regulator and audio and RSSI op amps. The SA606 is available in 20-lead SOL (surface-mounted small outline large package) and 20-lead SSOP (shrink small outline package).

The SA606 was designed for portable communication applications and will function down to 2.7V. The RF section is similar to the famous SA605. The audio and RSSI outputs have amplifiers with access to the feedback path. This enables the designer to level adjust the outputs or add filtering.

FEATURES

- Low power consumption: 3.5mA typical at 3V
- Mixer input to >150MHz
- Mixer conversion power gain of 17dB at 45MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator or external oscillator can be used at higher frequencies)
- 102dB of IF Amp/Limiter gain
- 2MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a 90dB dynamic range
- Low external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.31μV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone with RF at 45MHz and IF at 455kHz
- SA606 meets cellular radio specifications
- Audio output internal op amp
- RSSI output internal op amp
- Internal op amps with rail-to-rail outputs

PIN CONFIGURATION

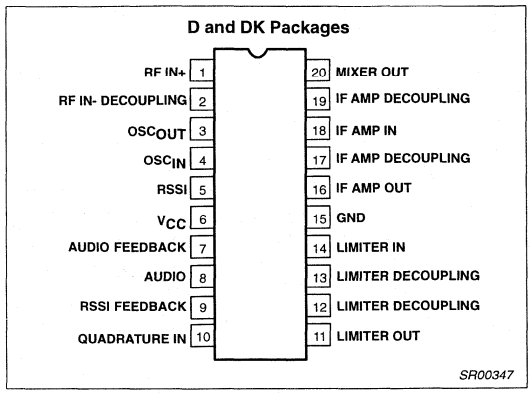


Figure 1. Pin Configuration

- ESD protection: Human Body Model 2kV
  Robot Model 200V

APPLICATIONS

- Portable cellular radio FM IF
- Cordless phones
- Wireless systems
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Portable high performance communication receiver
- Single conversion VHF receivers

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Small Outline Large (SOL) package (Surface-mount)	-40 to +85°C	SA606D	SOT163-1
20-Pin Plastic Shrink Small Outline Package (SSOP) (Surface-mount)	-40 to +85°C	SA606DK	SOT266-1

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	7	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range	-40 to +85	°C
θ_{JA}	Thermal impedance D package DK package	90 117	°C/W

BLOCK DIAGRAM

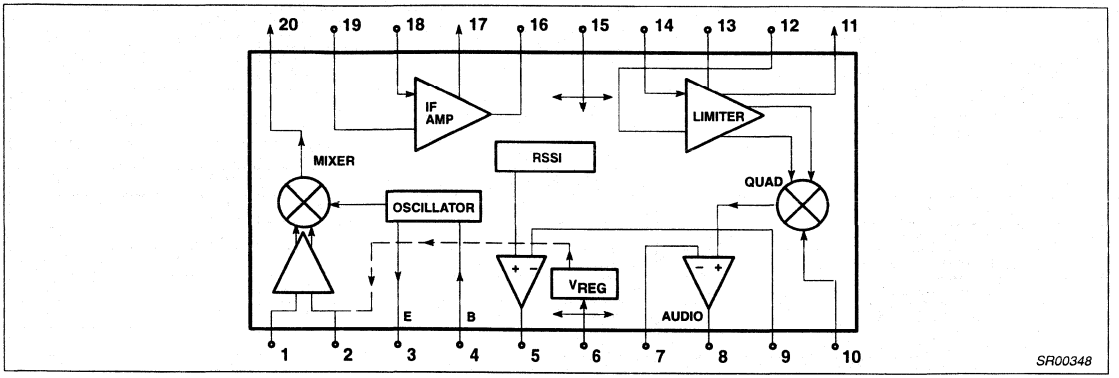


Figure 2. Block Diagram

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		2.7		7.0	V
I_{CC}	DC current drain			3.5	4.2	mA

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +3V, unless otherwise stated. RF frequency = 45MHz + 14.5dBV RF input step-up; IF frequency = 455kHz; R17 = 2.4kΩ and R18 = 3.3kΩ; RF level = -45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with de-emphasis filter and C-message weighted filter. Test circuit Figure 3. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Mixer/Osc section (ext LO = 220mV$_{RMS}$)						
f_{IN}	Input signal frequency			150		MHz
f_{OSC}	Crystal oscillator frequency			150		MHz
	Noise figure at 45MHz			6.2		dB
	Third-order input intercept point (50Ω source)	f1 = 45.0; f2 = 45.06MHz Input RF level = -52dBm		-9		dBm
	Conversion voltage gain	Matched 14.5dBV step-up	13.5	17	19.5	dB
		50Ω source		+2.5		dB
	RF input resistance	Single-ended input		8		kΩ
	RF input capacitance			3.0	4.0	pF
	Mixer output resistance	(Pin 20)	1.25	1.5		kΩ
IF section						
	IF amp gain	50Ω source		44		dB
	Limiter gain	50Ω source		58		dB
	Input limiting -3dB, R_{17a} = 2.4k, R_{17b} = 3.3k	Test at Pin 18		-109		dBm
	AM rejection	80% AM 1kHz		45		dB
	Audio level	Gain of two (2kΩ AC load)	70	120	160	mV
	SINAD sensitivity	IF level -110dBm		17		dB

AC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
THD	Total harmonic distortion		-35	-50		dB
S/N	Signal-to-noise ratio	No modulation for noise		62		dB
	RF RSSI output, R_9 = 2kΩ	RF level = -118dBm		0.3	.80	V
		RF level = -68dBm	.70	1.1	1.80	V
		RF level = -23dBm	1.20	1.8	2.50	V
	RSSI range			90		dB
	RSSI accuracy			±1.5		dB
	IF input impedance	Pin 18	1.3	1.5		kΩ
	IF output impedance	Pin 16		0.3		kΩ
	Limiter input impedance	Pin 14	1.3	1.5		kΩ
	Limiter output impedance	Pin 11		0.3		kΩ
	Limiter output voltage	Pin 11		130		mV_{RMS}
RF/IF section (int LO)						
	Audio level	3V = V_{CC}, RF level = -27dBm		120		mV_{RMS}
	System RSSI output	3V = V_{CC}, RF level = -27dBm		2.2		V
	System SINAD sensitivity	RF level = -117dBm		12		dB

CIRCUIT DESCRIPTION

The SA606 is an IF signal processing system suitable for second IF systems with input frequency as high as 150MHz. The bandwidth of the IF amplifier and limiter is at least 2MHz with 90dB of gain. The gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 6.2dB, conversion gain of 17dB, and input third-order intercept of -9dBm. The oscillator will operate in excess of 200MHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

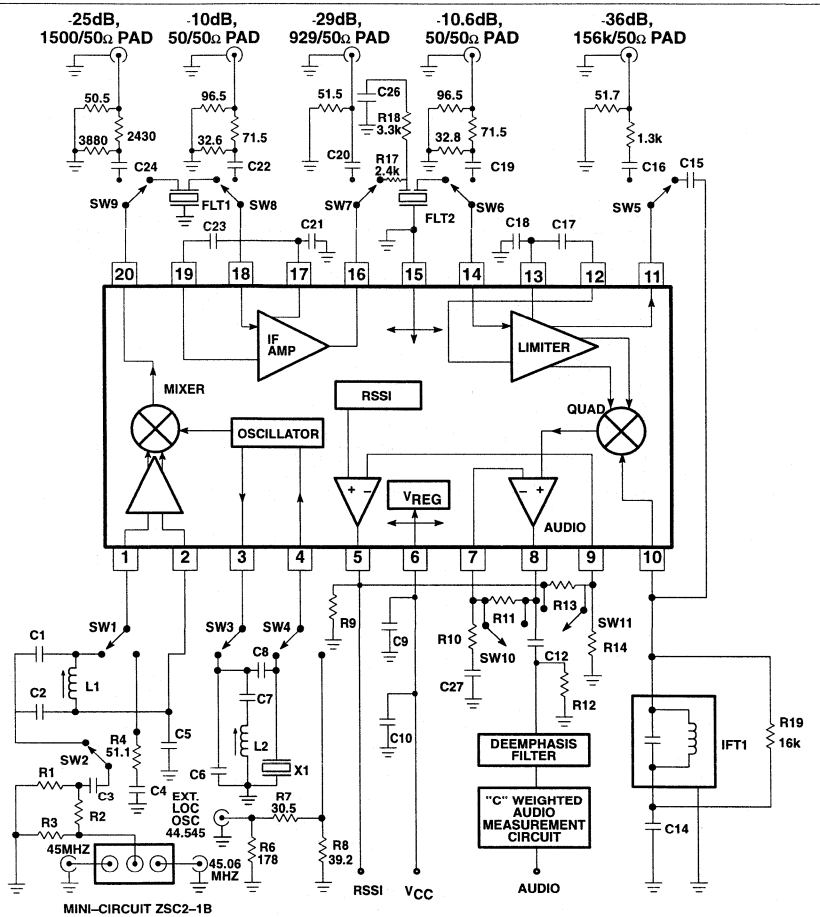
The output impedance of the mixer is a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. The IF amplifier has 43dB of gain and 5.5MHz bandwidth. The IF limiter has 60dB of gain and 4.5MHz bandwidth. To achieve optimum linearity of the log signal strength indicator, there must be a 12dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dB(v) insertion loss, a fixed or variable resistor or an L pad for simultaneous loss and impedance matching can be added between the first IF output (Pin 16) and the interstage network. The overall gain will then be 90dB with 2MHz bandwidth.

The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

The demodulated output of the quadrature drives an internal op amp. This op amp can be configured as a unity gain buffer, or for simultaneous gain, filtering, and 2nd-order temperature compensation if needed. It can drive an AC load as low as 5kΩ with a rail-to-rail output.

A log signal strength completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone. This signal drives an internal op amp. The op amp is capable of rail-to-rail output. It can be used for gain, filtering, or 2nd-order temperature compensation of the RSSI, if needed.

NOTE: $dB(v) = 20\log V_{OUT}/V_{IN}$



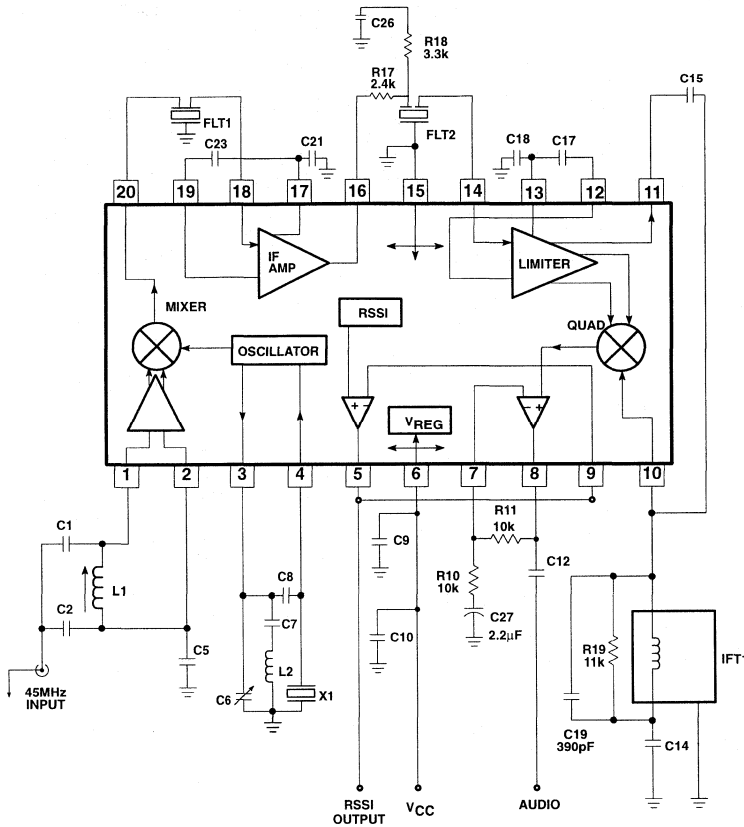
Automatic Test Circuit Component List

C1	100pF NPO Ceramic	C27	2.2µF ±10% Monolithic Ceramic
C2	390pF NPO Ceramic	Flt 1	Ceramic Filter Murata SFG455A3 or equiv
C5	100nF ±10% Monolithic Ceramic	Flt 2	Ceramic Filter Murata SFG455A3 or equiv
C6	22pF NPO Ceramic	IFT 1	455kHz (Ce = 180pF) Toko RMC–2A6597H
C7	1nF Ceramic	L1	147–160nH Coilcraft UNI–10/142–04J08S
C8	10.0pF NPO Ceramic	L2	0.8µH nominal
C9	100nF ±10% Monolithic Ceramic		Toko 292CNS–T1038Z
C10	10µF Tantalum (minimum) *	X1	44.545MHz Crystal ICM4712701
C12	2.2µF	R9	2kΩ ±1% 1/4W Metal Film
C14	100nF ±10% Monolithic Ceramic	R10	10kΩ ±1%
C15	10pF NPO Ceramic	R11	10kΩ ±1%
C17	100nF ±10% Monolithic Ceramic	R12	2kΩ ±1%
C18	100nF ±10% Monolithic Ceramic	R13	20kΩ ±1%
C21	100nF ±10% Monolithic Ceramic	R14	10kΩ ±1%
C23	100nF ±10% Monolithic Ceramic	R17	2.4kΩ ±5% 1/4W Carbon Composition
C25	100nF ±10% Monolithic Ceramic	R18	3.3kΩ
C26	100nF ±10% Monolithic Ceramic	R19	16kΩ

*NOTE: This value can be reduced when a battery is the power source.

SR00349

Figure 3. SA606 45MHz Test Circuit (Relays as shown)



NE606D/DK Demo Board
Application Component List

C1	51pF NPO Ceramic
C2	220pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	5-30pF trim cap
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	10µF Tantalum (minimum) *
C12	2.2µF ±10% Tantalum
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C19	390pF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C26	100nF ±10% Monolithic Ceramic
C27	2.2µF Tantalum
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	330µH TOKO 303LN-1130
L1	.33µH TOKO SCB-1320Z
L2	1.2µH
X1	44.545MHz Crystal ICM4712701
R5	Not Used in Application Board (see Note 8, pg 8)
R10	8.2k ±5% 1/4W Carbon Composition
R11	10k ±5% 1/4W Carbon Composition
R17	2.4k ±5% 1/4W Carbon Composition
R18	3.3k ±5% 1/4W Carbon Composition
R19	11k ±5% 1/4W Carbon Composition

* NOTE: This value can be reduced when a battery is the power source.

SR00350

Figure 4. SA606 45MHz Application Circuit

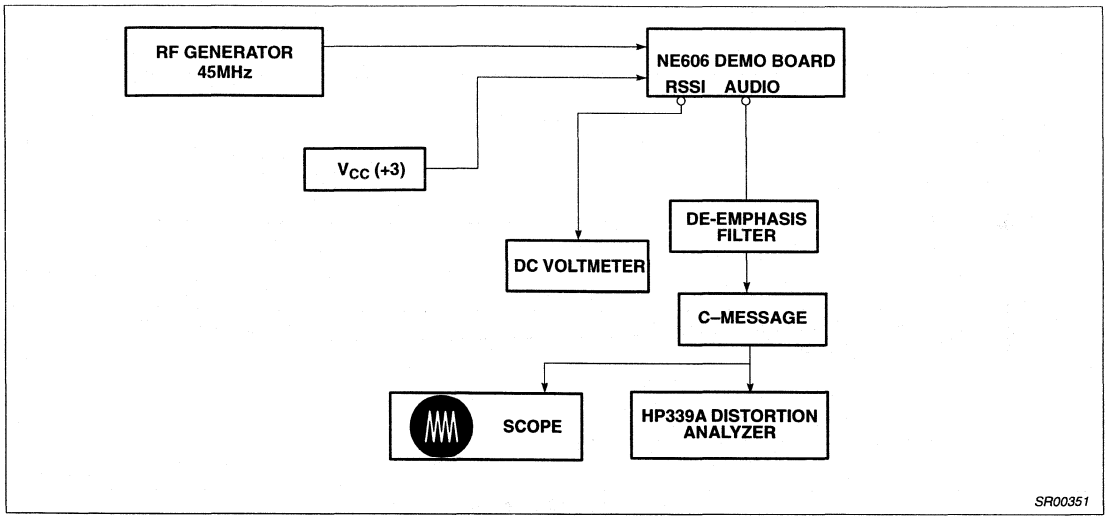


Figure 5. SA606 Application Circuit Test Set Up

NOTES:

1. C-message: The C-message and de-emphasis filter combination has a peak gain of 10 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339 analyzer. The de-emphasis filter has a fixed -6dB/Octave slope between 300Hz and 3kHz.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All of our specifications and testing are done with the more wideband filter.
3. RF generator: Set your RF generator at 45.000MHz, use a 1kHz modulation frequency and a 6kHz deviation if you use 16kHz filters, or 8kHz if you use 30kHz filters.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.35µV or -116dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 500mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10-15µF or higher value tantalum capacitor on the supply line is essential. A low frequency ESR screening test on this capacitor will ensure consistent good sensitivity in production. A 0.1µF bypass capacitor on the supply pin, and grounded near the 44.545MHz oscillator improves sensitivity by 2-3dB.
8. R5 can be used to bias the oscillator transistor at a higher current for operation above 45MHz. Recommended value is 10kΩ.

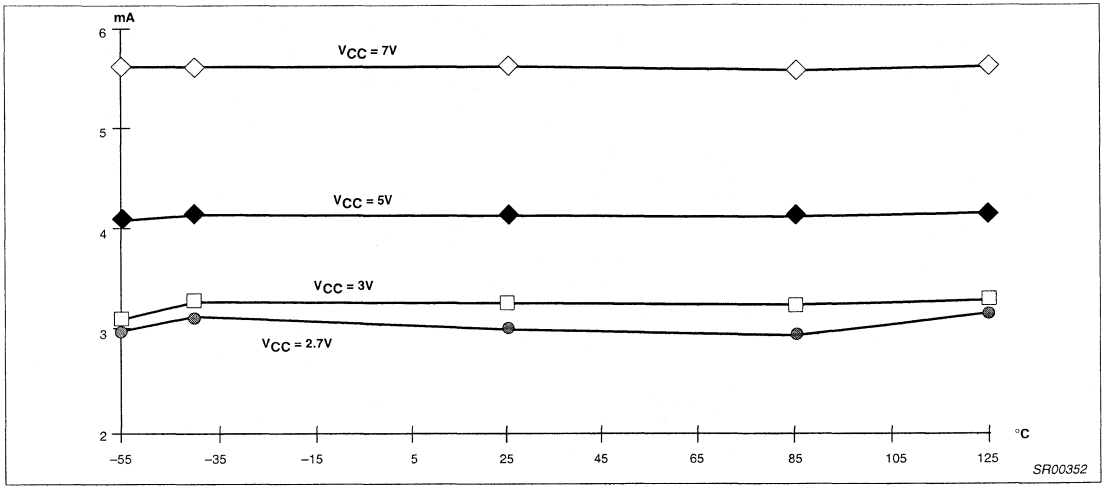


Figure 6. I_{CC} vs Temperature

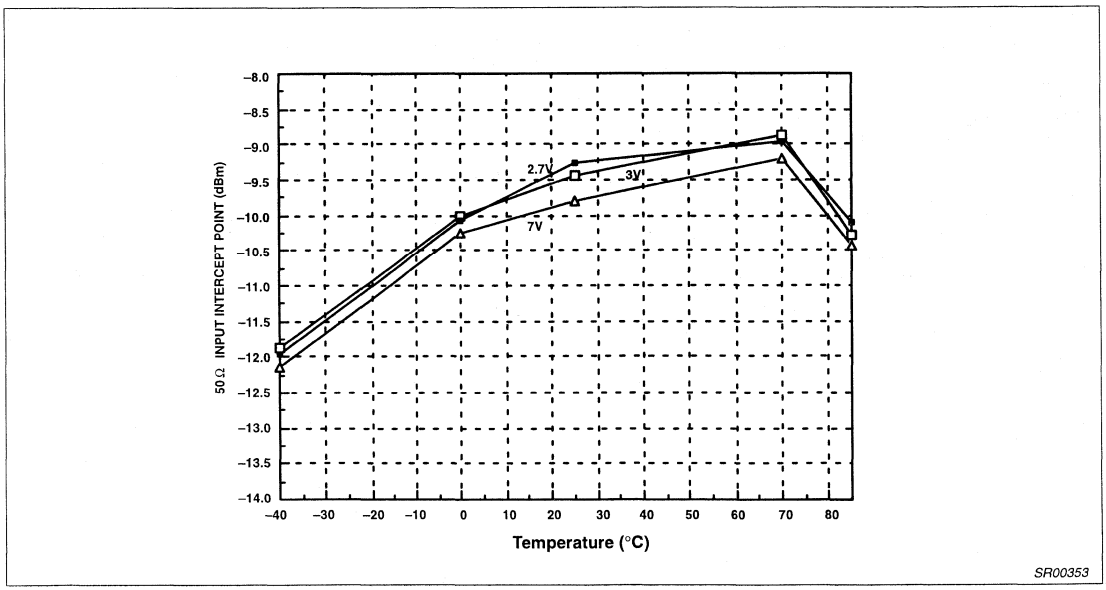


Figure 7. Third Order Intercept Point vs Supply Voltage

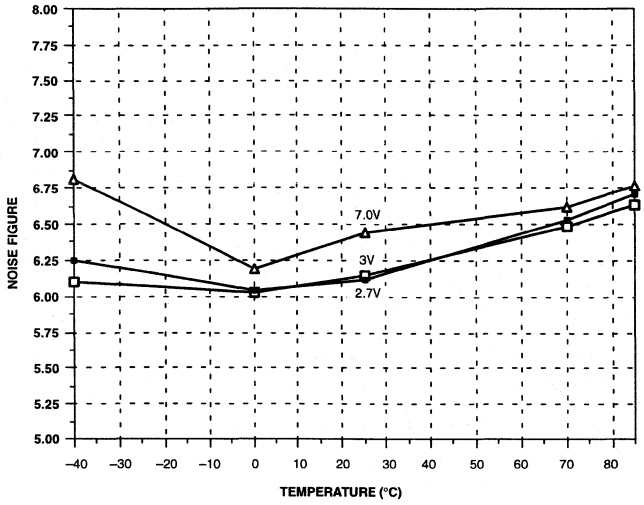


Figure 8. Mixer Noise Figure vs Supply Voltage

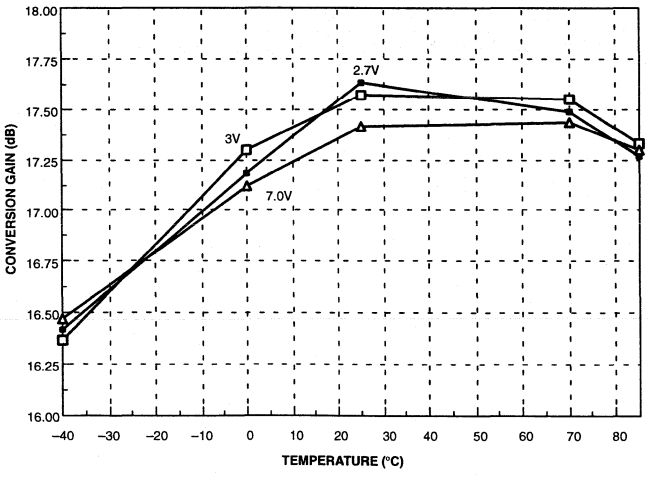


Figure 9. Conversion Gain vs Supply Voltage

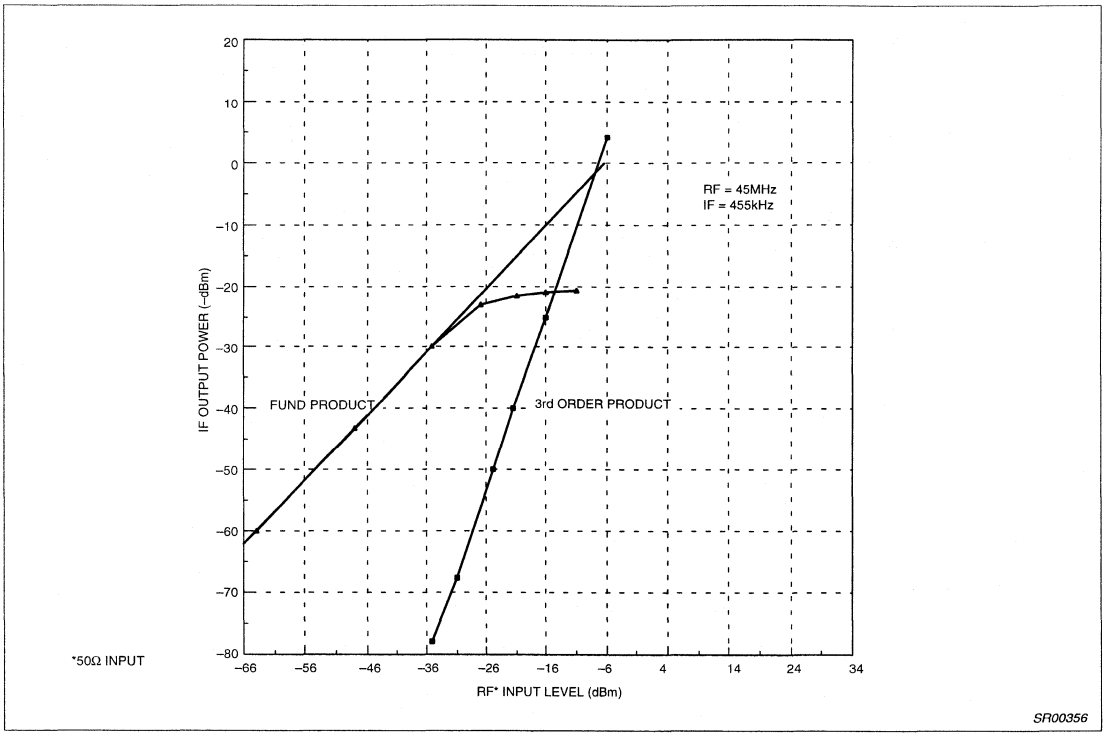


Figure 10. Mixer Third Order Intercept and Compression

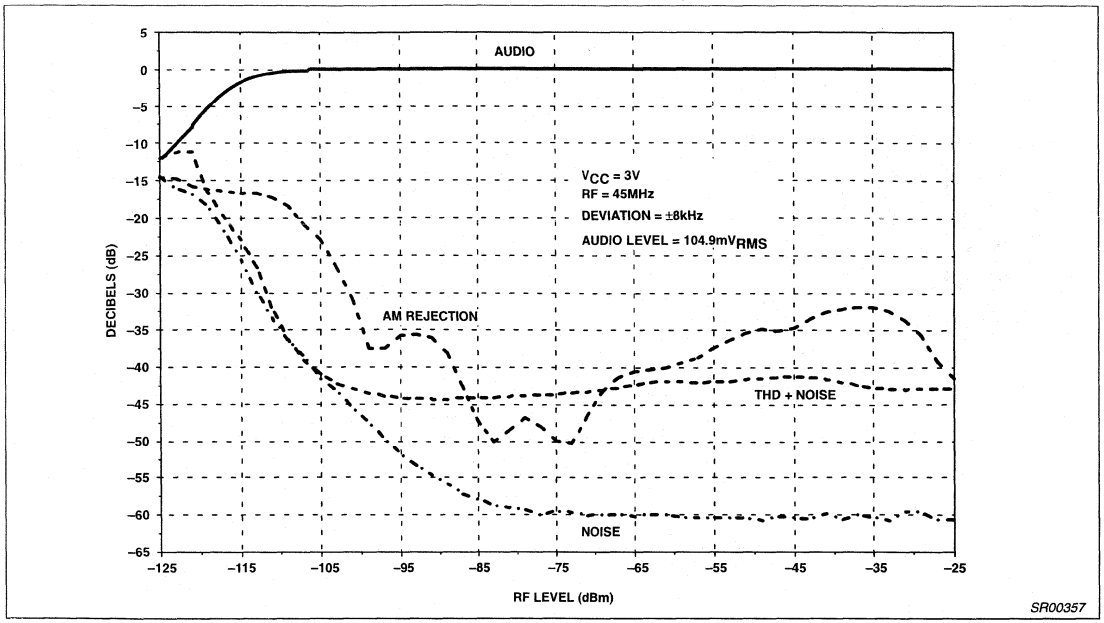


Figure 11. Sensitivity vs RF Level (-40°C)

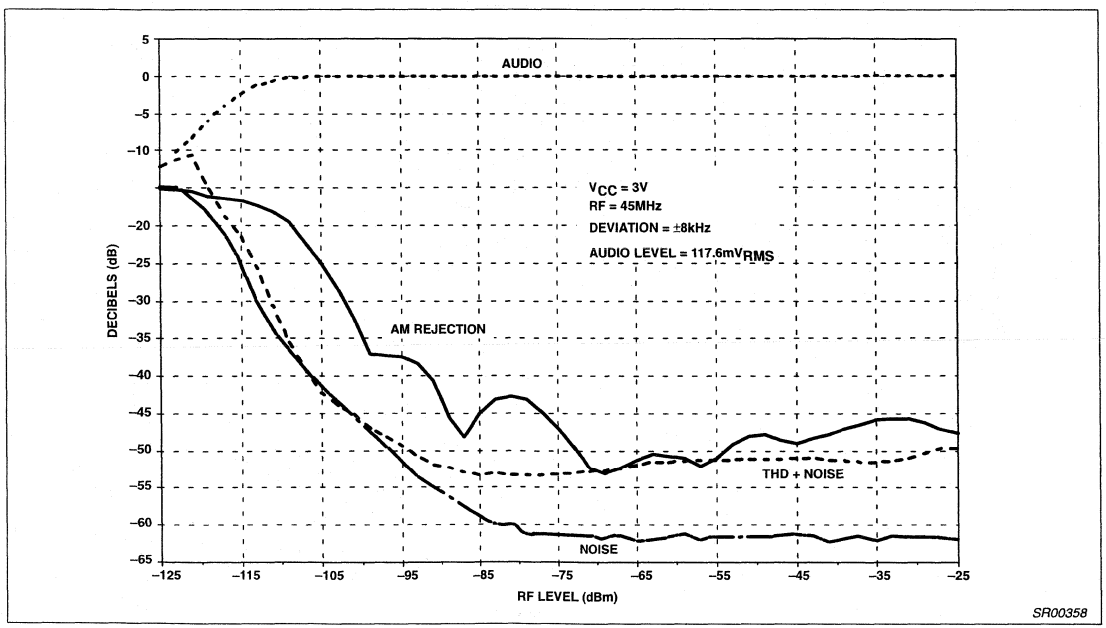


Figure 12. Sensitivity vs RF Level (+25°C)

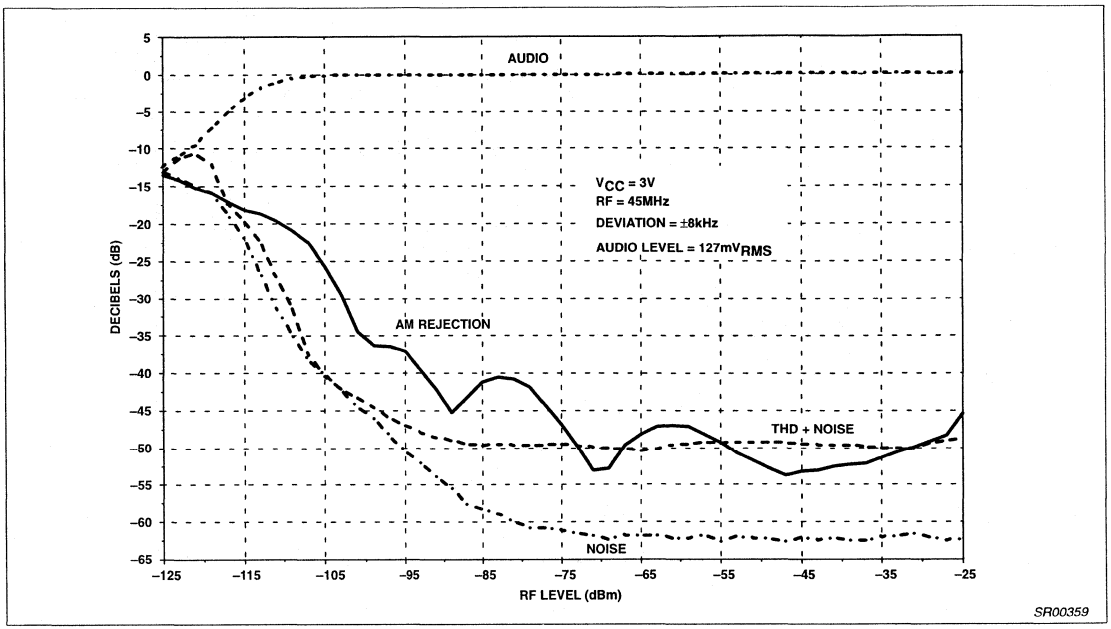


Figure 13. Sensitivity vs RF Level (Temperature 85°C)

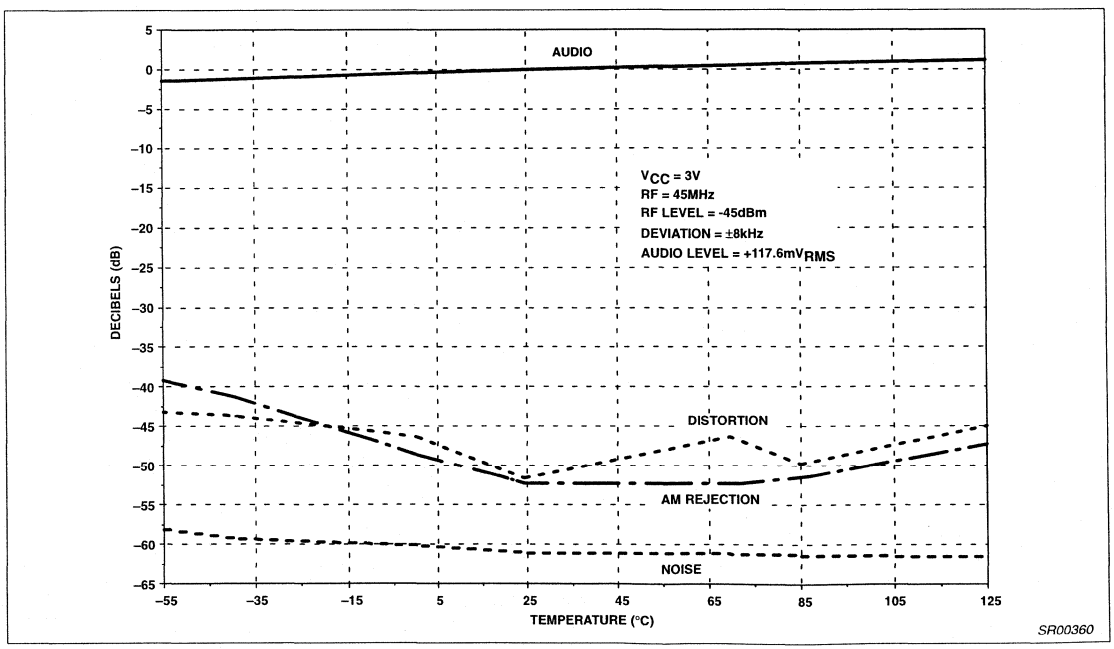


Figure 14. Relative Audio Level, Distortion, AM Rejection and Noise vs Temperature

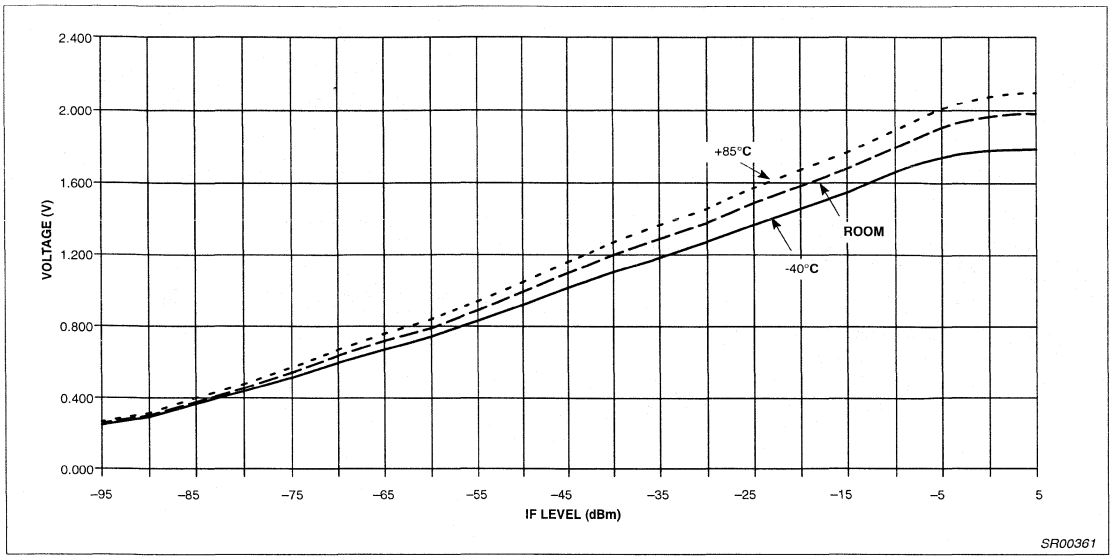


Figure 15. RSSI (455kHz IF @ 3V)

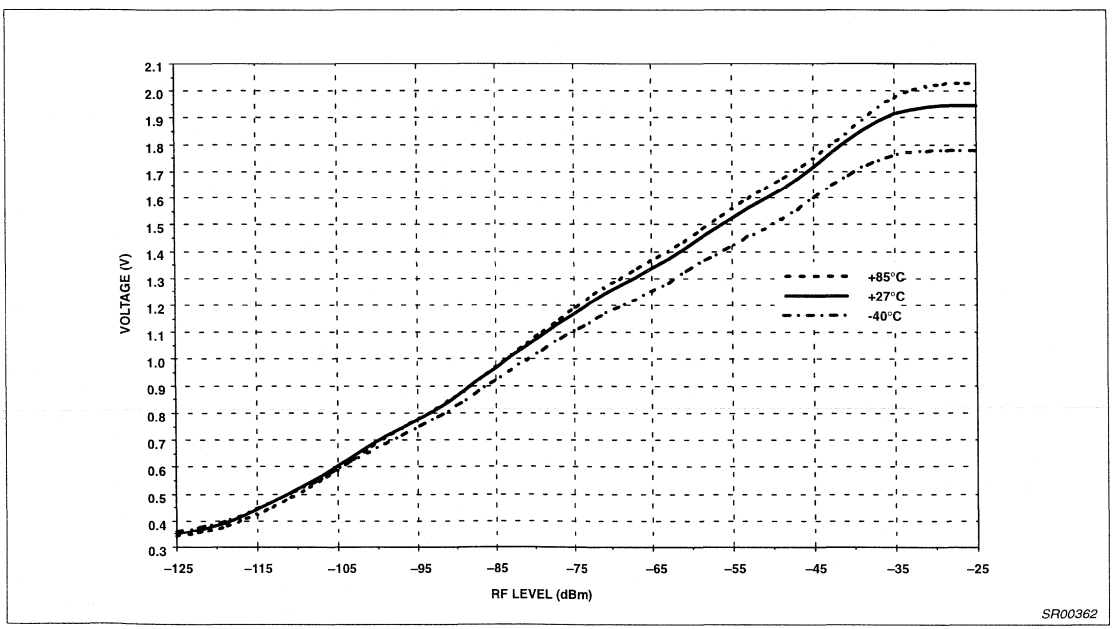


Figure 16. RSSI vs RF Level and Temperature - V_{CC} = 3V

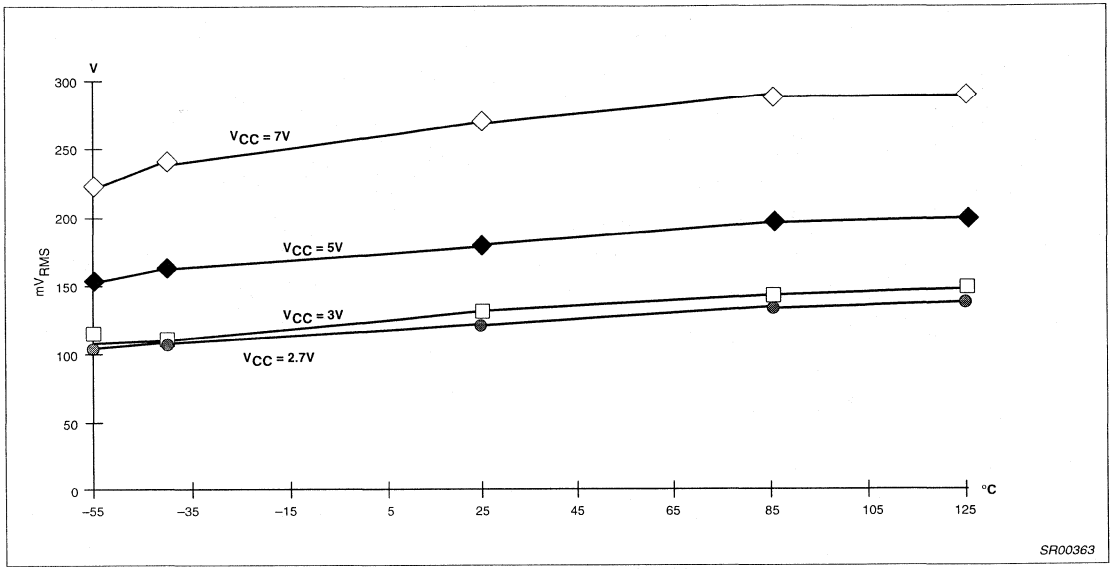
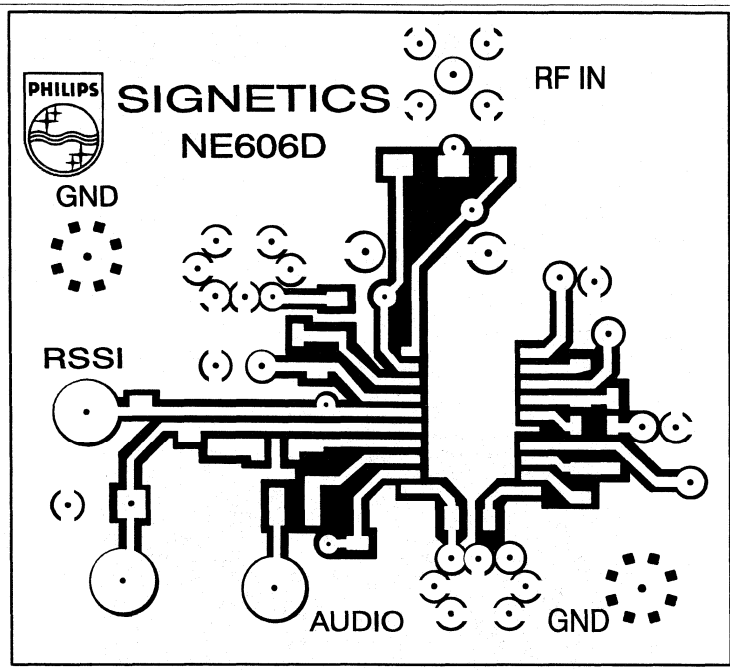
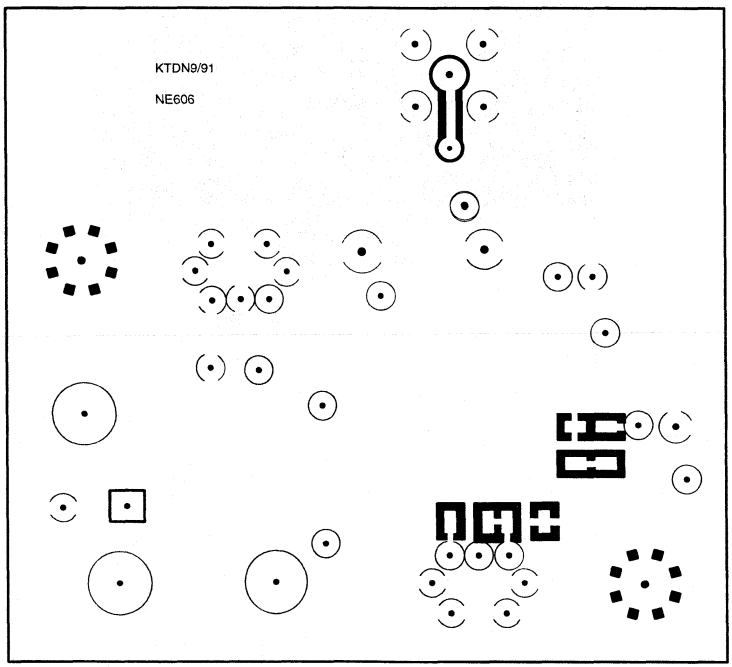


Figure 17. Audio Output vs Temperature



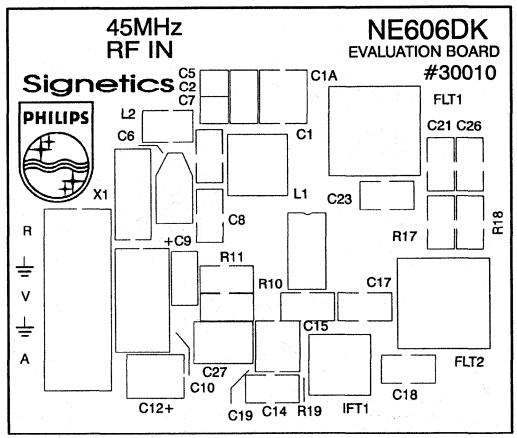
*Applies to Stand-Alone data sheets only.



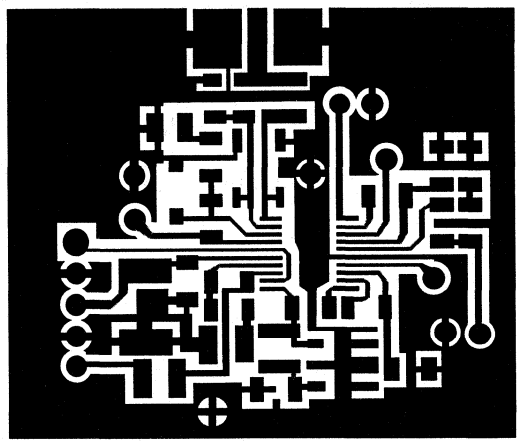
SR00365

Figure 18. SA606D SOL Product Board Layout (2X Actual Size* — For Reference Use Only)

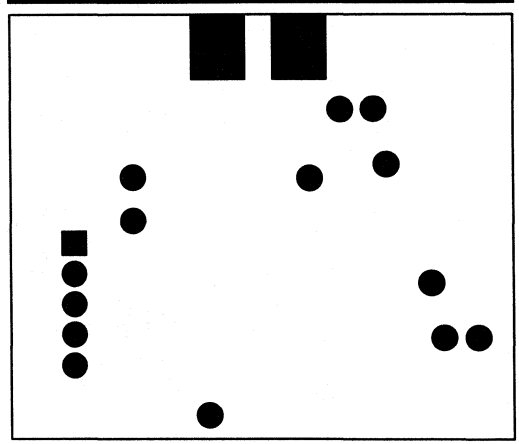
606 Silk Screen



606 TOP



606 BOTTOM



NOTE;
All views are TOP VIEW and not actual size. For reference only.

SR00366

Figure 19.

Low voltage high performance mixer FM IF system SA607

DESCRIPTION

The SA607 is a low voltage high performance monolithic FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, logarithmic received signal strength indicator (RSSI), voltage regulator and audio and RSSI op amps. The SA607 is available in 20-lead SOL (surface-mounted miniature package) and 20-lead SSOP package.

The SA607 was designed for portable communication applications and will function down to 2.7V. The RF section is similar to the famous SA605. The audio output has an internal amplifier with the feedback pin accessible. The RSSI output is buffered. The SA607 also has an extra limiter output. This signal is buffered from the output of the limiter and can be used to perform frequency check. This is accomplished by comparing a reference frequency with the frequency check signal using a comparator to a varactor or PLL at the oscillator inputs.

FEATURES

- Low power consumption: 3.5mA typical at 3V
- Mixer input to >150MHz
- Mixer conversion power gain of 17dB at 45MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator or external oscillator can be used at higher frequencies)
- 102dB of IF Amp/Limiter gain
- 2MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a 90dB dynamic range
- Low external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.31μV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone, 8kHz deviation with RF at 45MHz and IF at 455kHz
- SA607 meets cellular radio specifications
- Audio output internal op amp
- RSSI output internal op amp

PIN CONFIGURATION

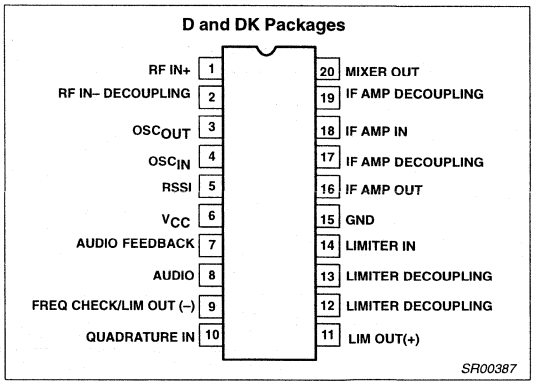


Figure 1. Pin Configuration

- Buffered frequency check output
- Internal op amps with rail-to-rail outputs
- ESD protection: Human Body Model 2kV
  Robot Model 200V

APPLICATIONS

- Portable cellular radio FM IF
- Cordless phones
- Narrow band cellular applications (NAMPS/NTACS)
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Portable high performance communication receivers
- Single conversion VHF receivers
- Wireless systems

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Small Outline Large (SOL) package (Surface-mount)	-40 to +85°C	SA607D	SOT163-1
20-Pin Plastic Shirnk Small Outline Package (SSOP) (Surface-mount)	-40 to +85°C	SA607DK	SOT266-1

BLOCK DIAGRAM

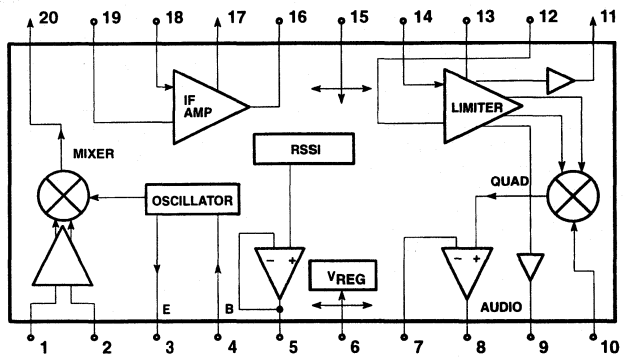


Figure 2. Block Diagram

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	7	V
T_{STG}	Storage temperature range	–65 to +150	°C
T_A	Operating ambient temperature range SA607	–40 to +85	°C
θ_{JA}	Thermal impedance D package DK package	90 117	°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA607			
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		2.7		7.0	V
I_{CC}	DC current drain			3.5	4.2	mA

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +3V, unless otherwise stated. RF frequency = 45MHz + 14.5dBV RF input step-up; IF frequency = 455kHz; R17 = 2.4k; R18 = 3.3k; RF level = –45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with de-emphasis filter and C-message weighted filter. Test circuit 3. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA607			
			MIN	TYP	MAX	
Mixer/Osc section (ext LO = 220mV$_{RMS}$)						
f_{IN}	Input signal frequency			150		MHz
f_{OSC}	Crystal oscillator frequency			150		MHz
	Noise figure at 45MHz			6.2		dB
	Third–order input intercept point (50Ω source)	f1 = 45.0; f2 = 45.06MHz Input RF Level = –52dBm		–9		dBm
	Conversion power gain	Matched 14.5dBV step–up	13.5	17	19.5	dB
		50Ω source		+2.5		dB
	RF input resistance	Single–ended input		8		kΩ
	RF input capacitance			3.0	4.0	pF
	Mixer output resistance	(Pin 20)	1.25	1.5		kΩ
IF section						
	IF amp gain	50Ω source		44		dB
	Limiter gain	50Ω source		58		dB
	Input limiting –3dB, R_{17} = 2.4k	Test at Pin 18		–109		dBm
	AM rejection	80% AM 1kHz		45		dB
	Audio level	Gain of two (2kΩ AC load)	70	120	160	mV
	SINAD sensitivity	RF level –110dB		17		dB
THD	Total harmonic distortion		–35	–50		dB
S/N	Signal–to–noise ratio	No modulation for noise		62		dB
	IF RSSI output, R_9 = 2kΩ[1]	IF level = –118dBm		0.3	0.8	V
		IF level = –68dBm	.70	1.1	1.80	V
		IF level = –23dBm	1.2	1.8	2.5	V
	RSSI range			90		dB
	RSSI accuracy			±1.5		dB
	IF input impedance		1.3	1.5		kΩ
	IF output impedance			0.3		kΩ
	Limiter input impedance		1.30	1.5		kΩ
	Limiter output impedance	(Pin 11)		200		Ω
	Limiter output level	(Pin 11) No load 5kΩ load		130 115		mV$_{RMS}$
	Frequency check/limiter output impedance	(Pin 9)		200		Ω
	Frequency check/limiter output level	(Pin 9) No load 5kΩ load		130 115		mV$_{RMS}$
RF/IF section (int LO)						
	Audio level	3V = V_{CC}, RF level = –27dBm		120		mV$_{RMS}$
	System RSSI output	3V = V_{CC}, RF level = –27dBm		2.2		V
	System SINAD sensitivity	RF level = –117dBm		12		dB

NOTE:

1. The generator source impedance is 50Ω, but the SA607 input impedance at Pin 18 is 1500Ω. As a result, IF level refers to the actual signal that enters the SA607 input (Pin 18) which is about 21dB less than the "available power" at the generator.

CIRCUIT DESCRIPTION

The SA607 is an IF signal processing system suitable for second IF systems with input frequency as high as 150MHz. The bandwidth of the IF amplifier and limiter is at least 2MHz with 90dB of gain. The gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 6.2dB, conversion gain of 17dB, and input third-order intercept of –9dBm. The oscillator will operate in excess of 200MHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

The output impedance of the mixer is a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. The IF amplifier has 43dB of gain and 5.5MHz bandwidth. The IF limiter has 60dB of gain and 4.5MHz bandwidth. To achieve optimum linearity of the log signal strength indicator, there must be a 12dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dB(v) insertion loss, a fixed or variable resistor or an L pad for simultaneous loss and impedance matching can be added between the first IF output (Pin 16) and the interstage network. The overall gain will then be 90dB with 2MHz bandwidth.

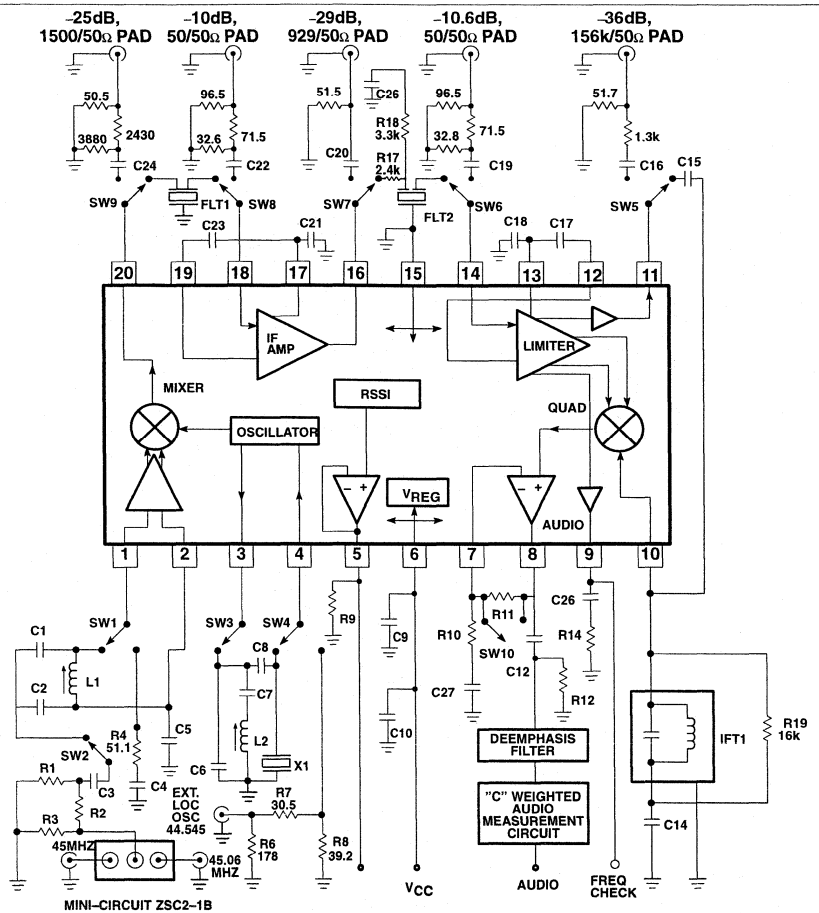
The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

The demodulated output of the quadrature drives an internal op amp. This op amp can be configured as a unity gain buffer, or for simultaneous gain, filtering, and 2nd-order temperature compensation if needed. It can drive an AC load as low as 5kΩ with a rail-to-rail output.

A log signal strength completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone. This signal is buffered through an internal unity gain op amp. The frequency check pin provides a buffered limiter output. This is useful for implementing an AFC (Automatic Frequency Check) function. This same output can also be used in conjunction with limiter output (Pin 11) for demodulating FSK (Frequency Shift Keying) data. Both pins are of the same amplitude, but 180° out of phase.

NOTE: Limiter output or Frequency Check output has drive capability of a load minimum of 2kΩ or higher to obtain 115mV output level.

NOTE: $dB(v) = 20\log V_{OUT}/V_{IN}$



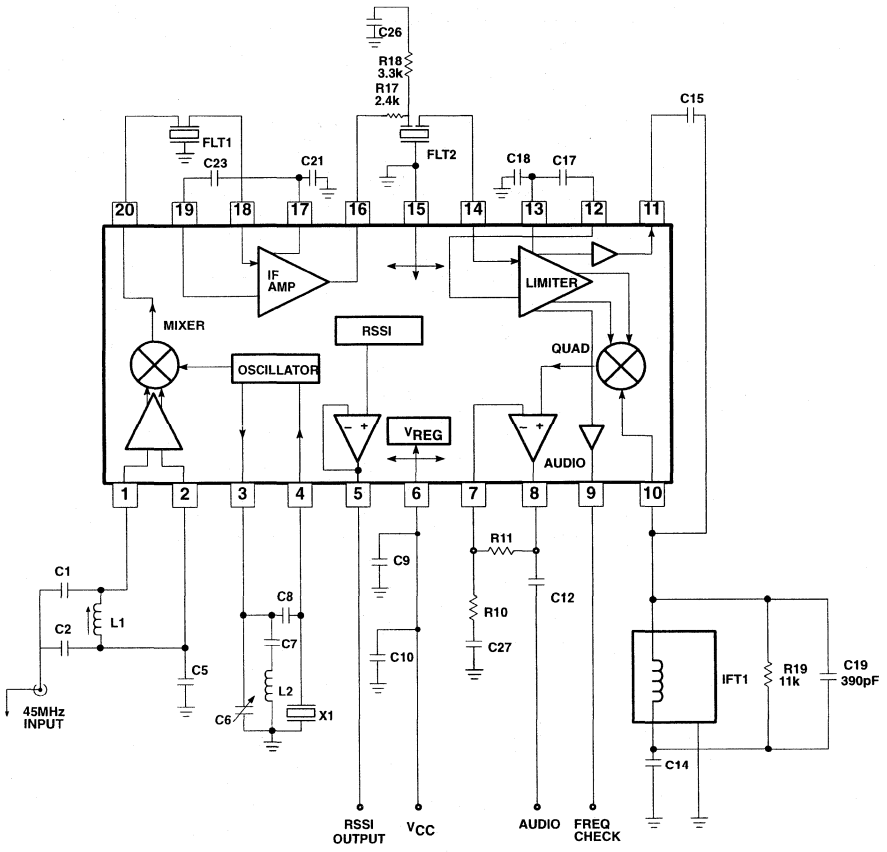
Automatic Test Circuit Component List

C1	100pF NPO Ceramic
C2	390pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	10μF Tantalum (minimum) *
C12	2.2μF
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
C26	0.1μF ±10% Monolithic Ceramic
C27	2.2μF
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	455kHz (Ce = 180pF) Toko RMC-2A6597H
L1	147-160nH Coilcraft UNI-10/142-04J08S
L2	0.8μH nominal Toko 292CNS-T1038Z
X1	44.545MHz Crystal ICM4712701
R9	2kΩ ±1% 1/4W Metal Film
R10	8.2kΩ ±1%
R11	10kΩ ±1%
R12	2kΩ ±1%
R14	5kΩ ±1%
R17	2.4kΩ ±5% 1/4W Carbon Composition
R18	3.3kΩ ±5% 1/4W Carbon Composition
R19	16kΩ ±5% 1/4W Carbon Composition

*NOTE: This value can be reduced when a battery is the power source.

SR00389

Figure 3. SA607 45MHz Test Circuit (Relays as shown)



SA607D/DK
Application Component List

C1	51pF NPO Ceramic
C2	220pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	5-30pF trim cap
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	10µF Tantalum (minimum) *
C12	2.2µF ±10% Tantalum
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C19	390pF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C26	100nF ±10% Monolithic Ceramic
C27	2.2µF Tantalum
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	330µH TOKO 303LN-1130
L1	.33µH TOKO SCB-1320Z
L2	1.2µH Coilcraft 1008C S-122
X1	44.545MHz Crystal Hy–Q
R5	Not Used in Application Board (see Note 8, pg 8)
R10	8.2k ±5% 1/4W Carbon Composition
R11	10k ±5% 1/4W Carbon Composition
R17	2.4k ±5% 1/4W Carbon Composition
R18	3.3k ±5% 1/4W Carbon Composition
R19	11k ±5% 1/4W Carbon Composition

*NOTE: This value can be reduced when a battery is the power source.

SR00390

Figure 4. SA607 45MHz Application Circuit

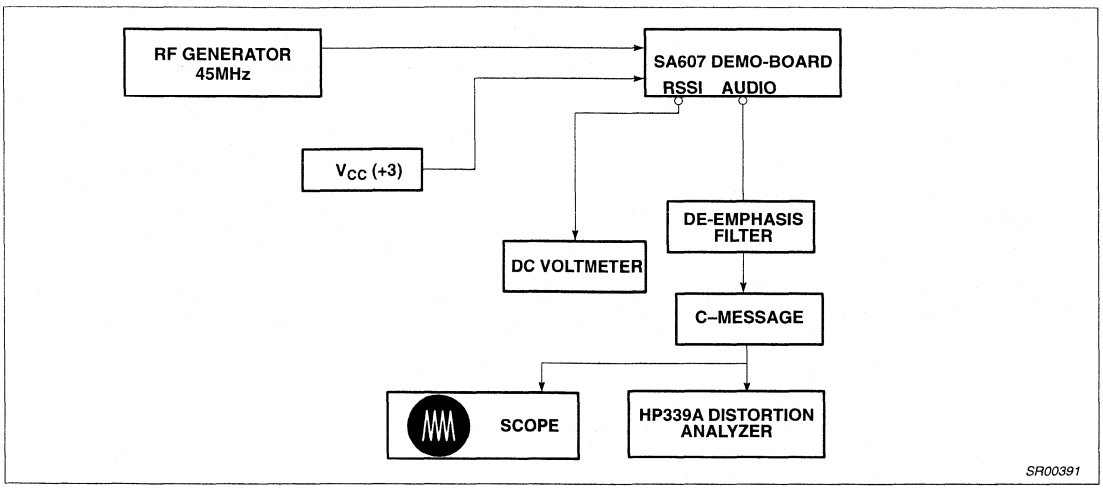


Figure 5. SA607 Application Circuit Test Set Up

NOTES:

1. C-message: The C-message and de-emphasis filter combination has a peak gain of 10 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339 analyzer. The de-emphasis filter has a fixed -6dB/Octave slope between 300Hz and 3kHz.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All of our specifications and testing are done with the more wideband filter.
3. RF generator: Set your RF generator at 45.000MHz, use a 1kHz modulation frequency and a 6kHz deviation if you use 16kHz filters, or 8kHz if you use 30kHz filters.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.35μV or –116dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 500mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10-15μF or higher value tantalum capacitor on the supply line is essential. A low frequency ESR screening test on this capacitor will ensure consistent good sensitivity in production. A 0.1μF bypass capacitor on the supply pin, and grounded near the 44.545MHz oscillator improves sensitivity by 2-3dB.
8. R5 can be used to bias the oscillator transistor at a higher current for operation above 45MHz. Recommended value is 22kΩ, but should not be below 10kΩ.

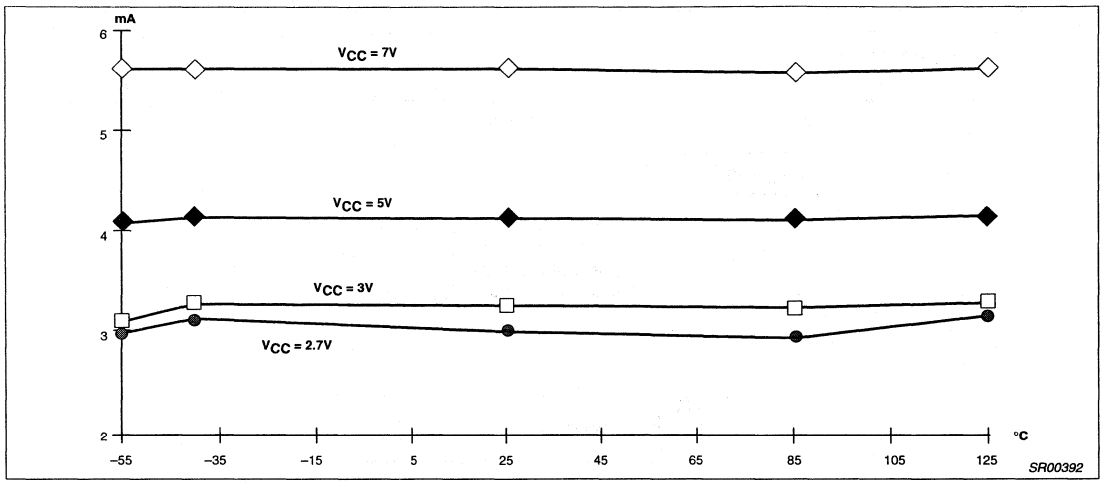


Figure 6. I_{CC} vs Temperature

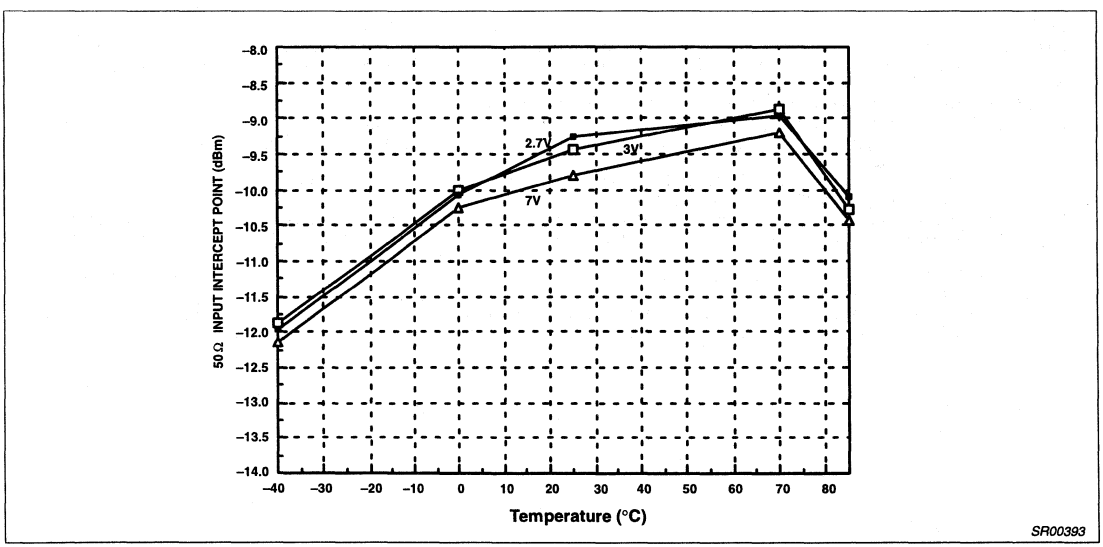


Figure 7. Third Order Intercept Point vs Supply Voltage

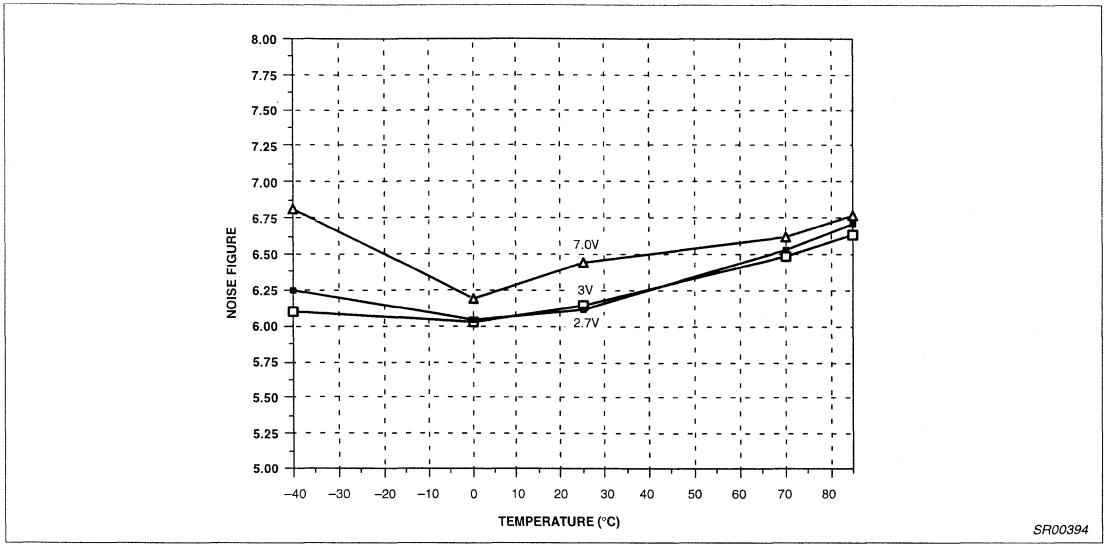


Figure 8. Mixer Noise Figure vs Supply Voltage

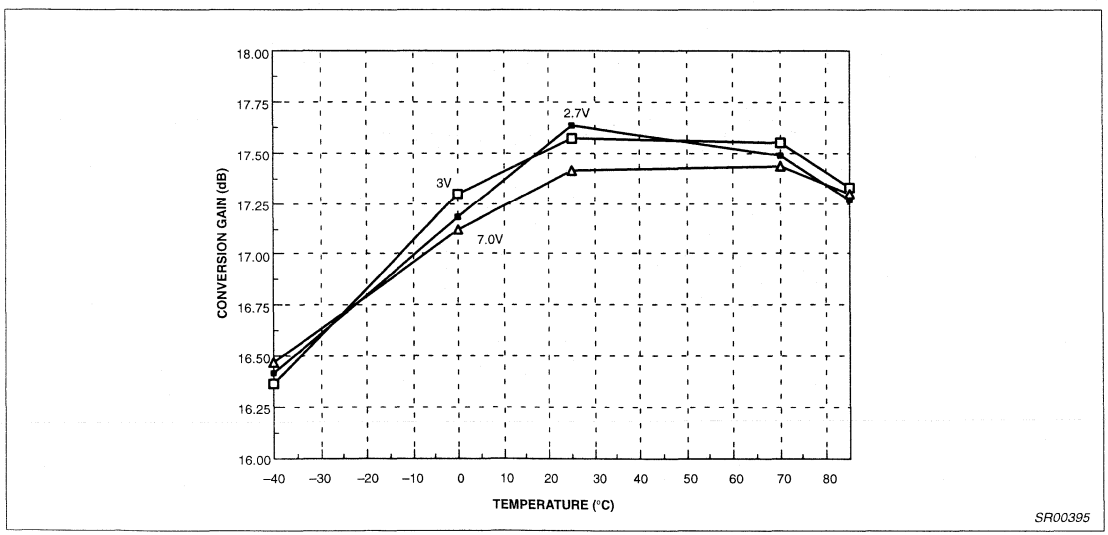


Figure 9. Conversion Gain vs Supply Voltage

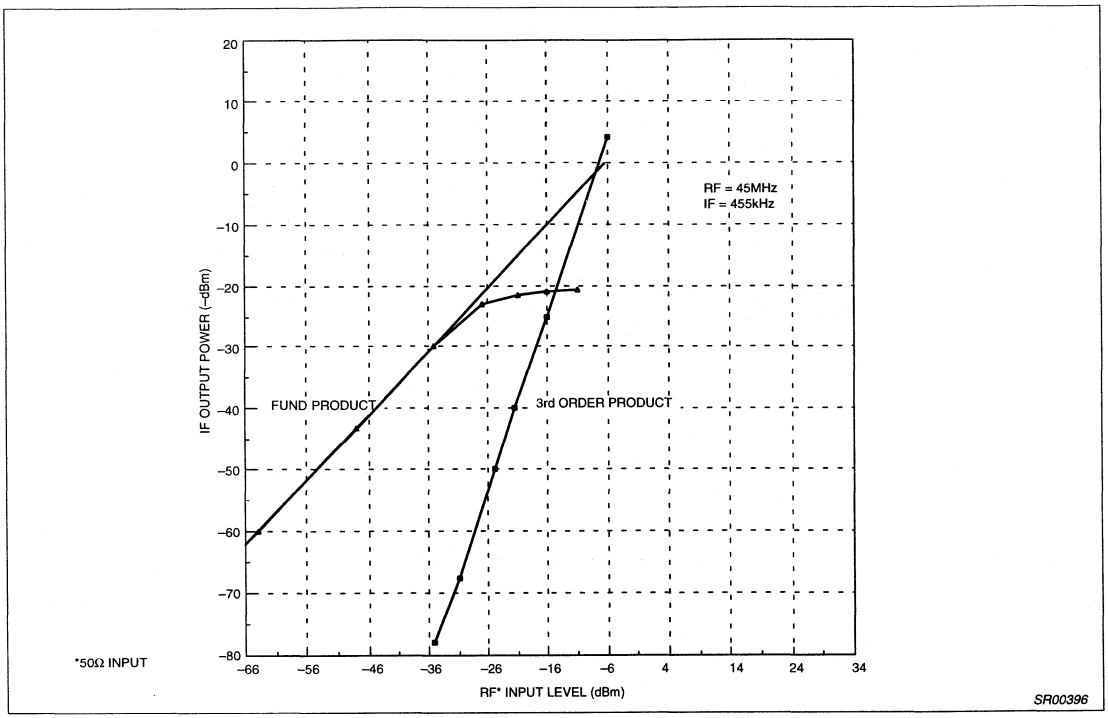


Figure 10. Mixer Third Order Intercept and Compression

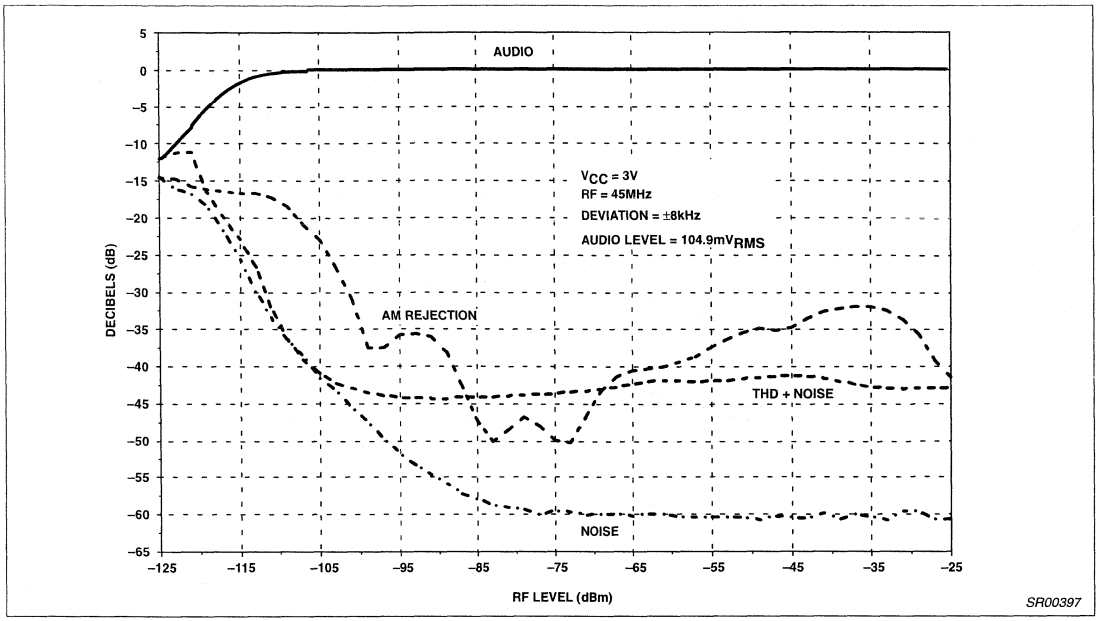


Figure 11. Sensitivity vs RF Level (–40°C)

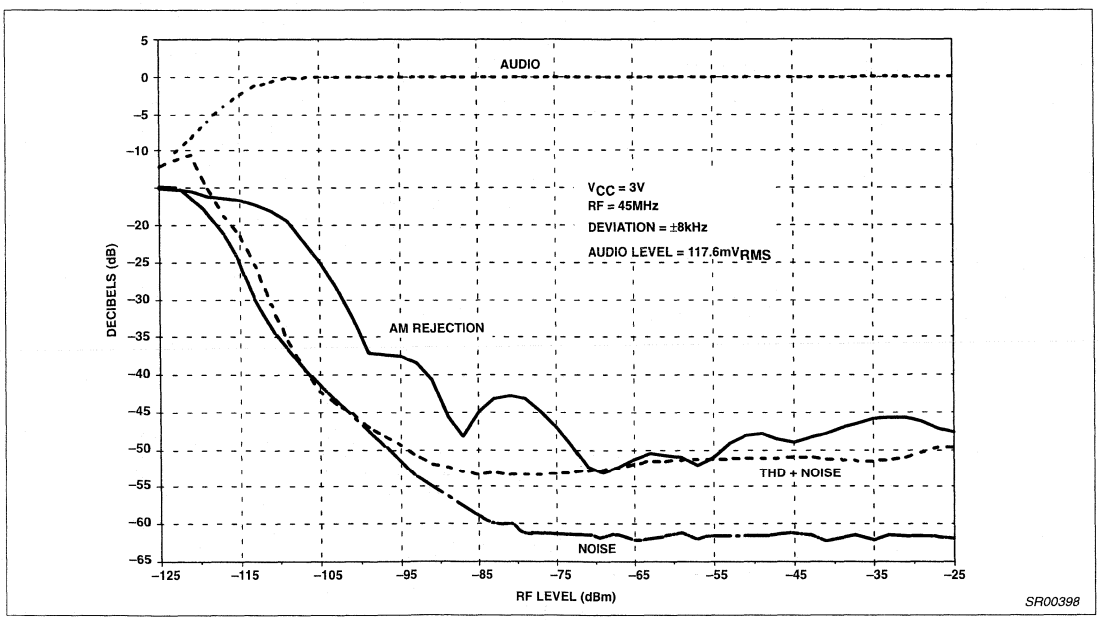


Figure 12. Sensitivity vs RF Level (+25°C)

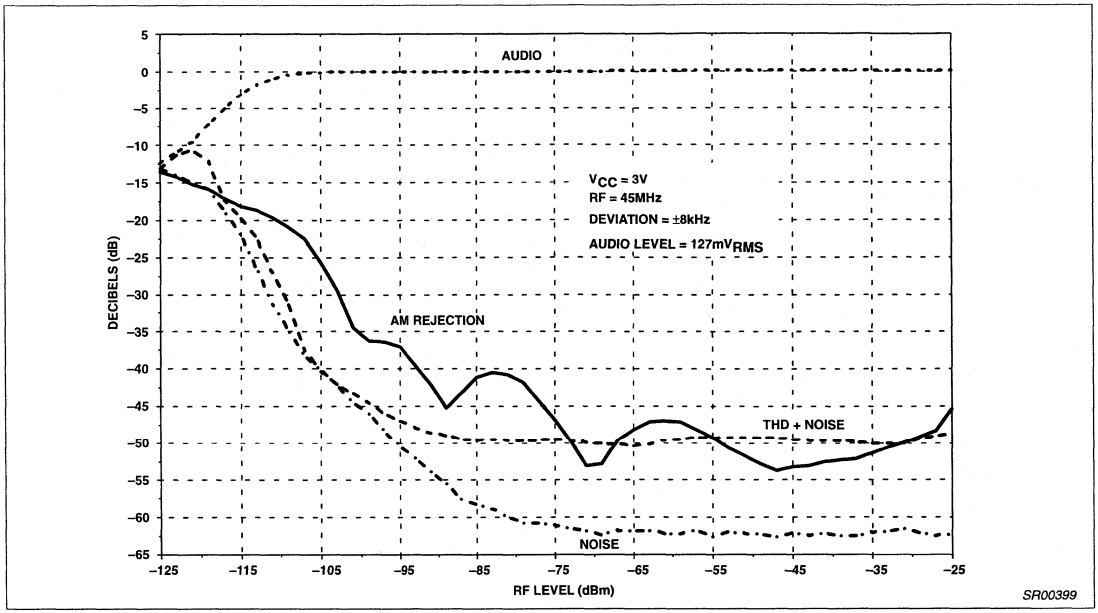


Figure 13. Sensitivity vs RF Level (Temperature 85°C)

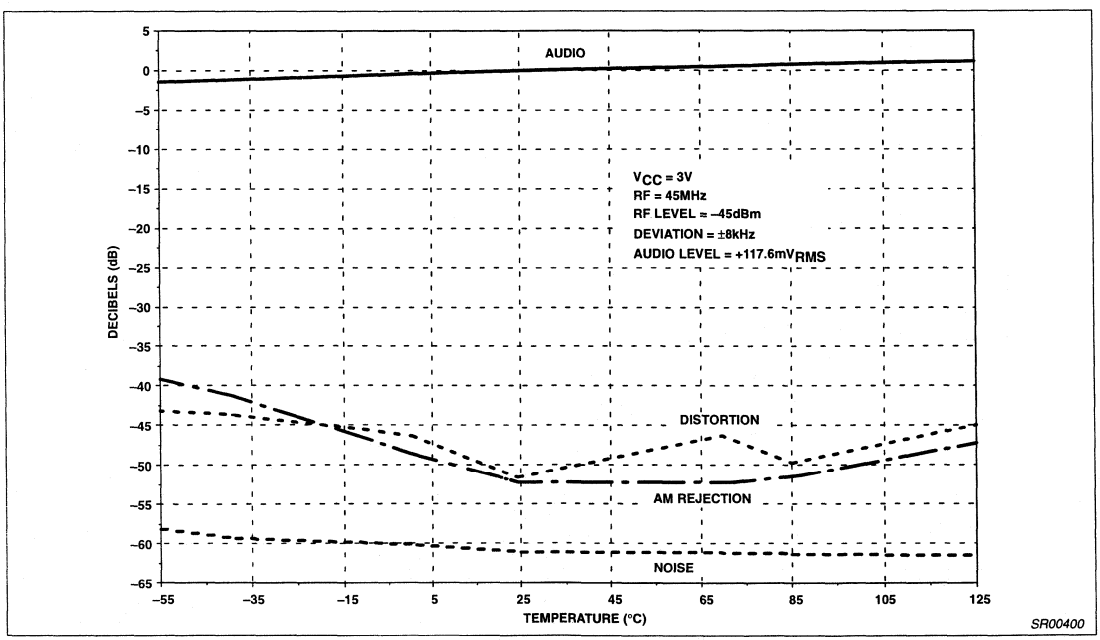


Figure 14. Relative Audio Level, Distortion, AM Rejection and Noise vs Temperature

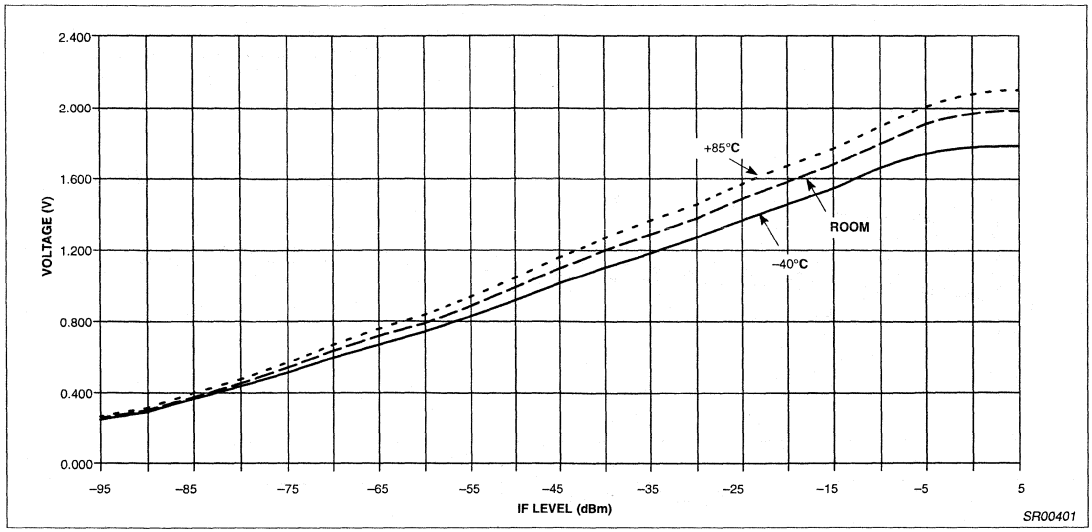


Figure 15. RSSI (455kHz IF @ 3V)

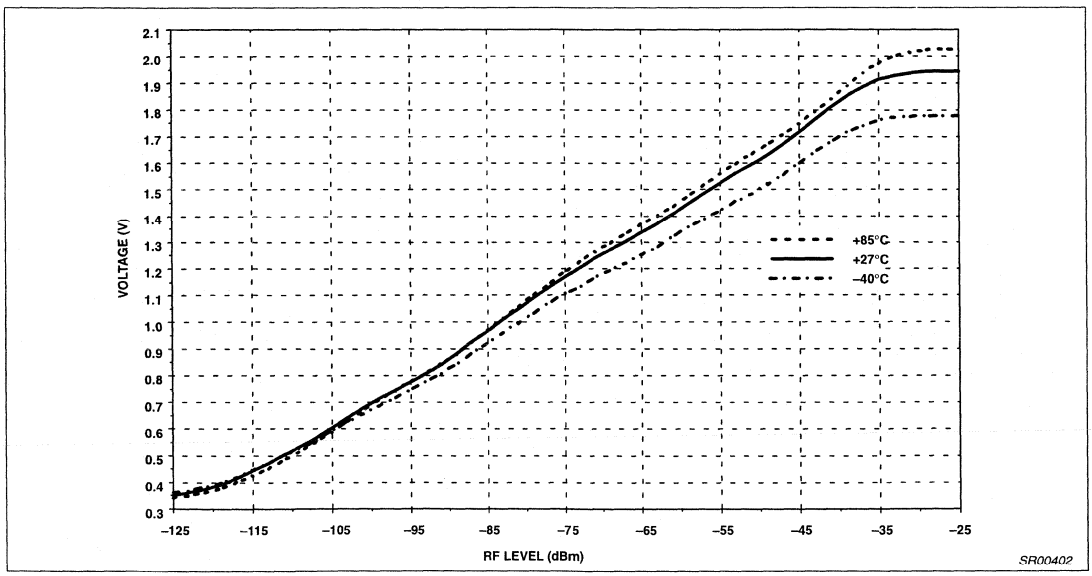


Figure 16. RSSI vs RF Level and Temperature - V_{CC} = 3V

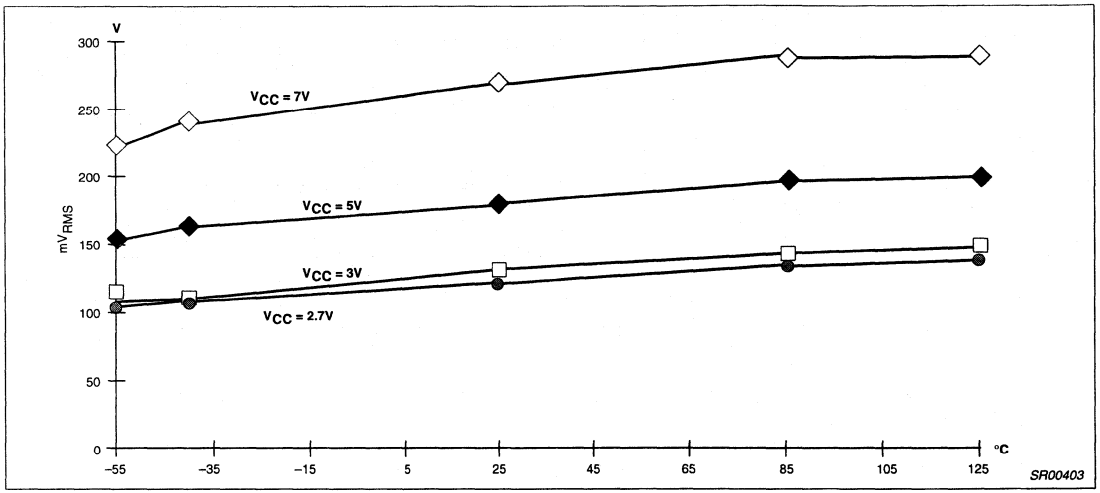
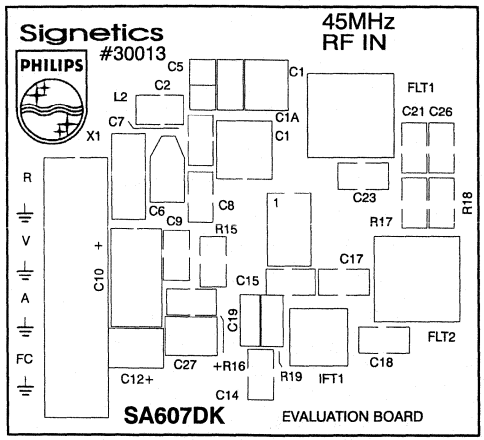
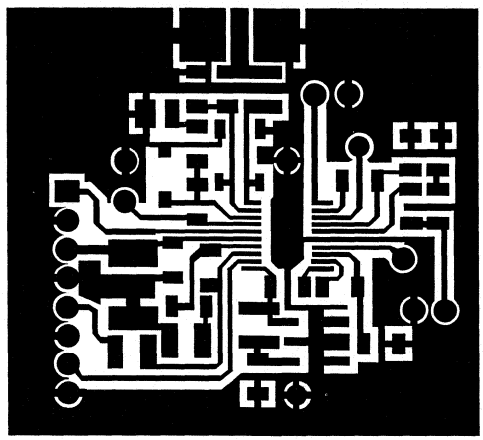


Figure 17. Audio Output vs Temperature

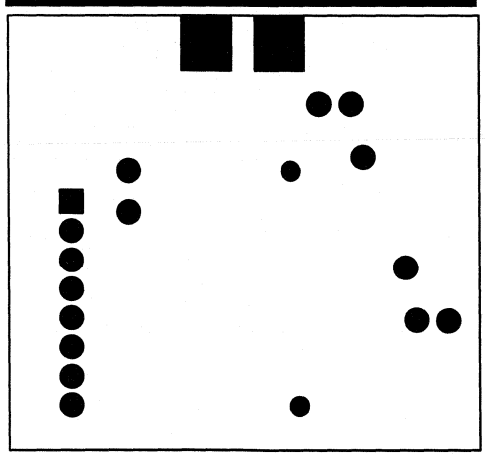
607 Silk Screen



607 TOP



607 BOTTOM



NOTE;
All views are TOP VIEW and not actual size. For reference only.

SR00404

Figure 18.

Low voltage high performance mixer FM IF system — SA608

DESCRIPTION

The SA608 is a low voltage high performance monolithic FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, logarithmic received signal strength indicator (RSSI), voltage regulator and audio and RSSI op amps. The SA608 is available in 20-lead dual-in-line plastic, 20-lead SOL (surface-mounted miniature package) and 20-lead SSOP package.

The SA608 was designed for portable communication applications and will function down to 2.7V. The RF section is similar to the famous NE605. The audio output is buffered. The RSSI output has an internal amplifier with the feedback pin accessible. The SA608 also has an extra limiter output. This signal is buffered from the output of the limiter and can be used to perform frequency check. This is accomplished by comparing a reference frequency with the frequency check signal using a comparator to a varactor or PLL at the oscillator inputs.

FEATURES

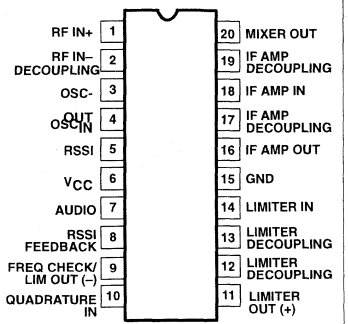
- Low power consumption: 3.5mA typical at 3V
- Mixer input to >150MHz
- Mixer conversion power gain of 17dB at 45MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator or external oscillator can be used at higher frequencies)
- 102dB of IF Amp/Limiter gain
- 2MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a 90dB dynamic range
- Low external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.31μV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone, 8kHz deviation with RF at 45MHz and IF at 455kHz
- SA608 meets cellular radio specifications
- Audio output internal op amp
- RSSI output internal op amp
- Buffered frequency check output
- Internal op amps with rail-to-rail outputs
- ESD protection: Human Body Model 2kV
  Robot Model 200V

APPLICATIONS

- Portable cellular radio FM IF
- Cordless phones
- Narrow band cellular applications (NAMPS/NTACS)
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Portable high performance communication receivers
- Single conversion VHF receivers
- Wireless systems

PIN CONFIGURATION

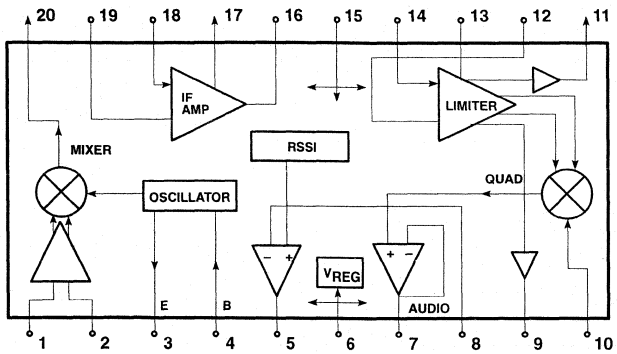
D, DK and N Packages



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA608N	0408B
20-Pin Plastic Small Outline Large (SOL) package (Surface-mount)	-40 to +85°C	SA608D	0172D
20-Pin Plastic Shrink Small Outline Package (SSOP) (Surface-mount)	-40 to +85°C	SA608DK	1563

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	7	V
T_{STG}	Storage temperature range	–65 to +150	°C
T_A	Operating ambient temperature range SA608	–40 to +85	°C
θ_{JA}	Thermal impedance D package DK package N package	90 117 75	°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA608			
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		2.7		7.0	V
I_{CC}	DC current drain			3.5	4.2	mA

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +3V, unless otherwise stated. RF frequency = 45MHz + 14.5dBV RF input step-up; IF frequency = 455kHz; R17 = 2.4k; R18 = 3.3k; RF level = –45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with de-emphasis filter and C-message weighted filter. Test circuit 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS SA608			UNITS
			MIN	TYP	MAX	
Mixer/Osc section (ext LO = 220mV$_{RMS}$)						
f_{IN}	Input signal frequency			150		MHz
f_{OSC}	Crystal oscillator frequency			150		MHz
	Noise figure at 45MHz			6.2		dB
	Third–order input intercept point (50Ω source)	f1 = 45.0; f2 = 45.06MHz Input RF Level = –52dBm		–9		dBm
	Conversion power gain	Matched 14.5dBV step–up	13.5	17	19.5	dB
		50Ω source		+2.5		dB
	RF input resistance	Single–ended input		8		kΩ
	RF input capacitance			3.0	4.0	pF
	Mixer output resistance	(Pin 20)	1.25	1.5		kΩ
IF section						
	IF amp gain	50Ω source		44		dB
	Limiter gain	50Ω source		58		dB
	Input limiting –3dB, R_{17} = 2.4k	Test at Pin 18		–109		dBm
	AM rejection	80% AM 1kHz		45		dB
	Audio level[2]		35	60	80	mV
	SINAD sensitivity	RF level –110dB		17		dB
THD	Total harmonic distortion		–35	–50		dB
S/N	Signal–to–noise ratio	No modulation for noise		62		dB
	IF RSSI output, R_9 = 2kΩ[1]	IF level = –118dBm		0.3	0.8	V
		IF level = –68dBm	.70	1.1	1.80	V
		IF level = –23dBm	1.2	1.8	2.5	V
	RSSI range			90		dB
	RSSI accuracy			±1.5		dB
	IF input impedance		1.3	1.5		kΩ
	IF output impedance			0.3		kΩ
	Limiter input impedance		1.30	1.5		kΩ
	Limiter output impedance	(Pin 11)		200		Ω
	Limiter output level	(Pin 11) no load 5kΩ load		130 115		mV$_{RMS}$
	Frequency check/lim (–) output impedance	(Pin 9)		200		Ω
	Frequency check/lim (–) output level	(Pin 9) no load 5kΩ load		130 115		mV$_{RMS}$
RF/IF section (int LO)						
	Audio level	3V = V_{CC}, RF level = –27dBm		120		mV$_{RMS}$
	System RSSI output	3V = V_{CC}, RF level = –27dBm		2.2		V
	System SINAD sensitivity	RF level = –117dBm		12		dB

NOTE:
1. The generator source impedance is 50Ω, but the SA608 input impedance at Pin 18 is 1500Ω. As a result, IF level refers to the actual signal that enters the SA608 input (Pin 18) which is about 21dB less than the "available power" at the generator.
2. By using 45kΩ load across the Quad detector coil, you will have Audio output at 115mV with –42dB distortion.

CIRCUIT DESCRIPTION

The SA608 is an IF signal processing system suitable for second IF systems with input frequency as high as 150MHz. The bandwidth of the IF amplifier and limiter is at least 2MHz with 90dB of gain. The gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 6.2dB, conversion gain of 17dB, and input third-order intercept of –9dBm. The oscillator will operate in excess of 200MHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

The output impedance of the mixer is a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ.

With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. The IF amplifier has 43dB of gain and 5.5MHz bandwidth. The IF limiter has 60dB of gain and 4.5MHz bandwidth. To achieve optimum linearity of the log signal strength indicator, there must be a 12dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dB(v) insertion loss, a fixed or variable resistor or an L pad for simultaneous loss and impedance matching can be added between the first IF output (Pin 16) and the interstage network. The overall gain will then be 90dB with 2MHz bandwidth.

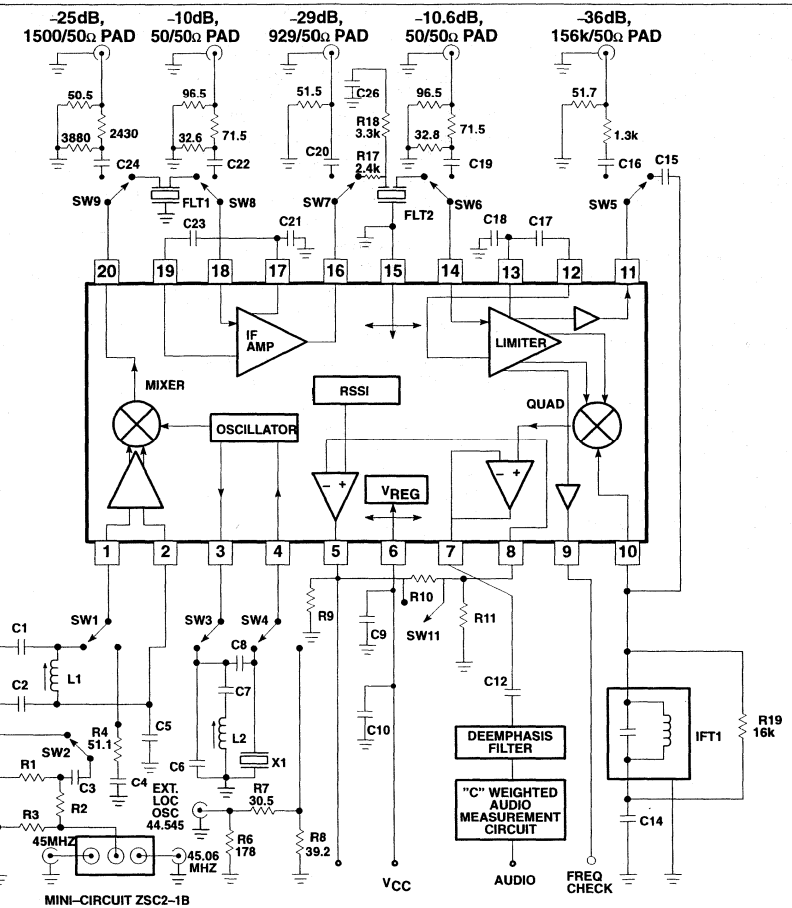
The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

The demodulated output of the quadrature drives an internal op amp. This op amp is configured as a unity gain buffer.

A log signal strength completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone. This signal is buffered through an internal unity gain op amp. The frequency check pin provides a buffered limiter output. This is useful for implementing an AFC (Automatic Frequency Check) function. This same output can also be used in conjunction with limiter output (Pin 11) for demodulating FSK (Frequency Shift Keying) data. Both pins are of the same amplitude, but 180° out of phase.

NOTE: Limiter or Frequency Check output has drive capability of a 5kΩ minimum or higher in order to obtain 120mV$_{RMS}$ output level.

NOTE: dB(v) = 20log V_{OUT}/V_{IN}

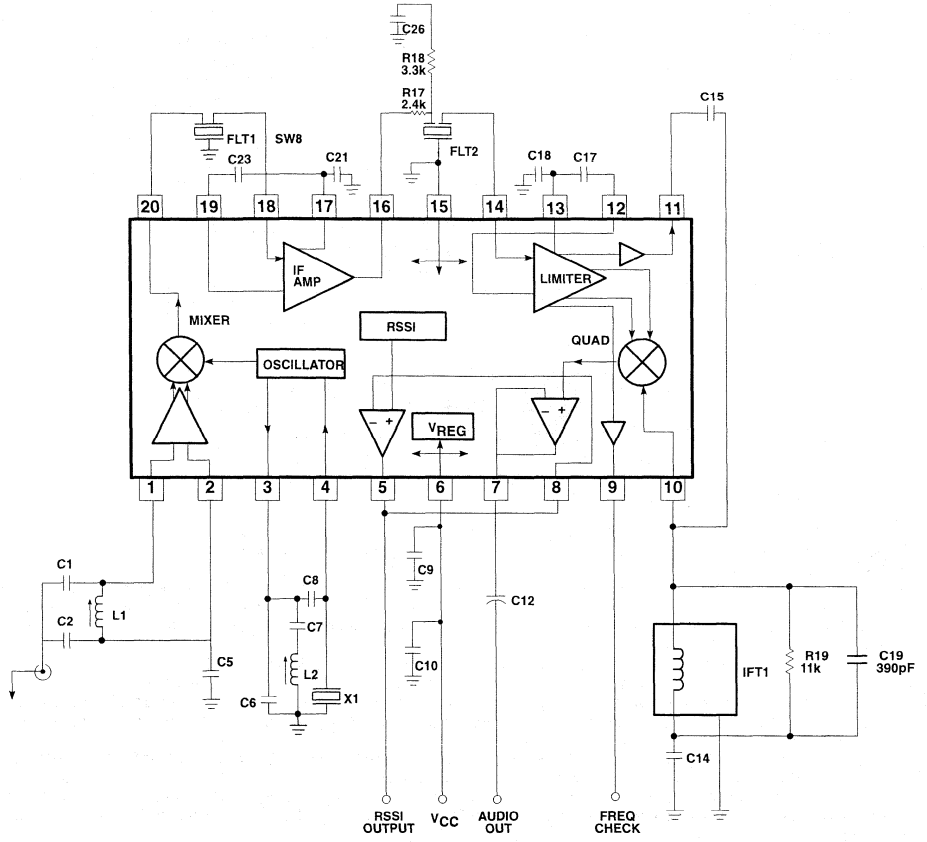


Automatic Test Circuit Component List

C1	100pF NPO Ceramic
C2	390pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	10μF Tantalum (minimum) *
C12	2.2μF
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
C26	0.1μF ±10% Monolithic Ceramic
C27	2.2μF
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	455kHz (Ce = 180pF) Toko RMC–2A6597H
L1	147–160nH Coilcraft UNI–10/142–04J08S
L2	0.8μH nominal Toko 292CNS–T1038Z
X1	44.545MHz Crystal ICM4712701
R9	2kΩ ±1% 1/4W Metal Film
R10	10kΩ ±1%
R11	10kΩ ±1%
R14	5kΩ ±1%
R17	2.4kΩ ±5% 1/4W Carbon Composition
R18	3.3kΩ ±5% 1/4W Carbon Composition
R19	16kΩ ±5% 1/4W Carbon Composition

*NOTE: This value can be reduced when a battery is the power source.

Figure 1. SA607 45MHz Test Circuit (Relays as shown)



Product Board SA608D/DK Component List

C1	51pF NPO Ceramic
C2	220pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	5-30pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	10μF Tantalum (minimum) *
C12	2.2μF
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C19	390pF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
C26	0.1μF ±10% Monolithic Ceramic
C27	2.2μF
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	330μH TOKO 303LN–1130
L1	0.33μH TOKO SCB–1320Z
L2	1.2μH Coilcraft 1008CS–122
X1	44.545MHz Crystal Hy-Q
R9	2kΩ ±1% 1/4W Metal Film
R10	8.2kΩ ±1%
R11	10kΩ ±1%
R14	10kΩ ±1%
R17	2.4kΩ ±5% 1/4W Carbon Composition
R18	3.3kΩ ±5% 1/4W Carbon Composition
R19	16kΩ ±5% 1/4W Carbon Composition

*NOTE: This value can be reduced when a battery is the power source.

Figure 2. SA608 45MHz Test Circuit (Relays as shown)

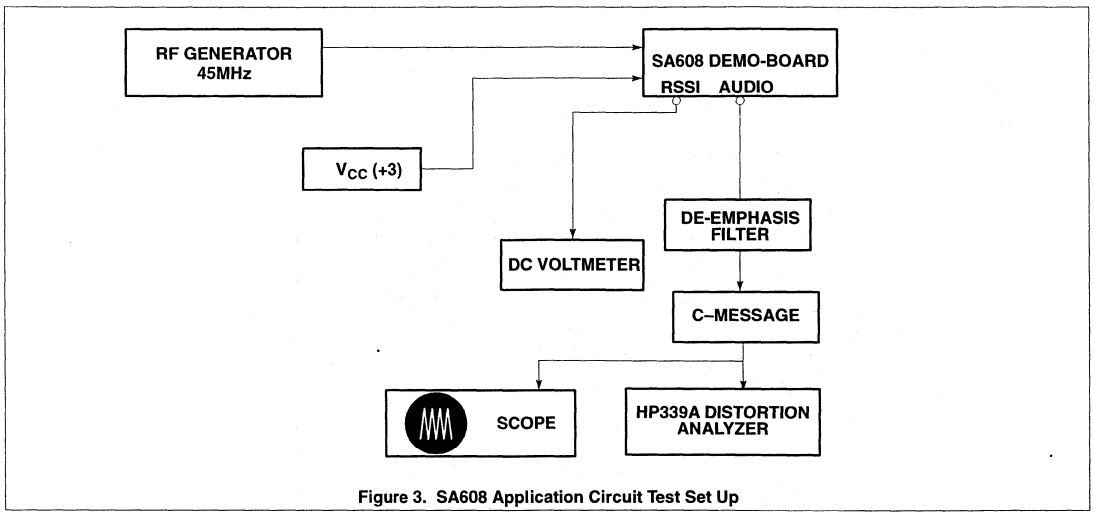


Figure 3. SA608 Application Circuit Test Set Up

NOTES:

1. C-message: The C-message and de-emphasis filter combination has a peak gain of 10 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339 analyzer. The de-emphasis filter has a fixed -6dB/Octave slope between 300Hz and 3kHz.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All of our specifications and testing are done with the more wideband filter.
3. RF generator: Set your RF generator at 45.000MHz, use a 1kHz modulation frequency and a 6kHz deviation if you use 16kHz filters, or 8kHz if you use 30kHz filters.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.35µV or –116dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 500mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10-15µF or higher value tantalum capacitor on the supply line is essential. A low frequency ESR screening test on this capacitor will ensure consistent good sensitivity in production. A 0.1µF bypass capacitor on the supply pin, and grounded near the 44.545MHz oscillator improves sensitivity by 2-3dB.
8. R5 can be used to bias the oscillator transistor at a higher current for operation above 45MHz. Recommended value is 22kΩ, but should not be below 10kΩ.

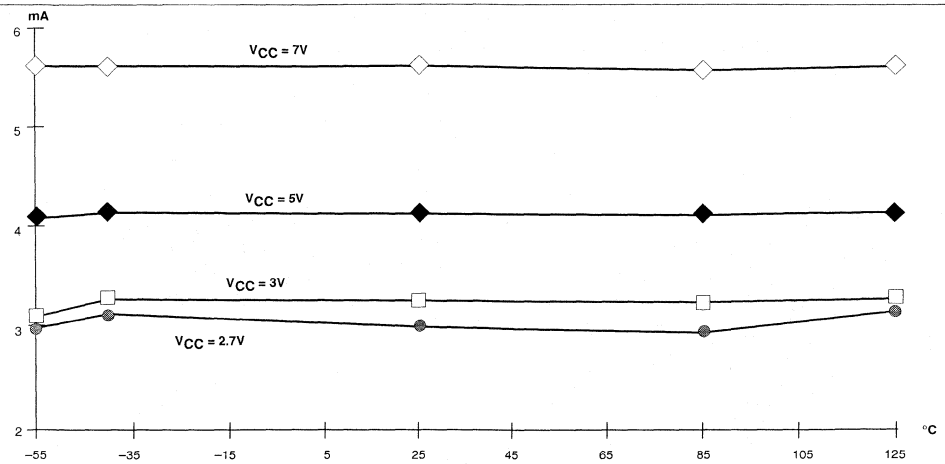


Figure 4. I_{CC} vs Temperature

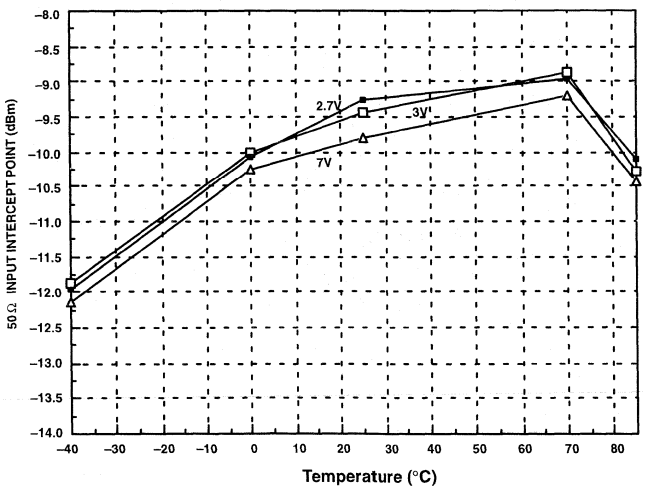


Figure 5. Third Order Intercept Point vs Supply Voltage

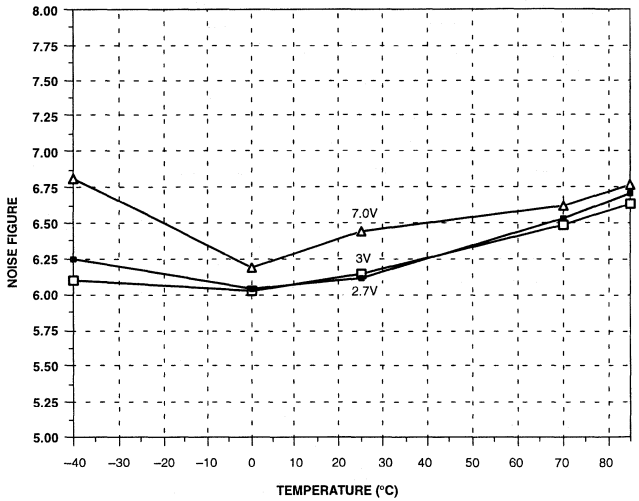


Figure 6. Mixer Noise Figure vs Supply Voltage

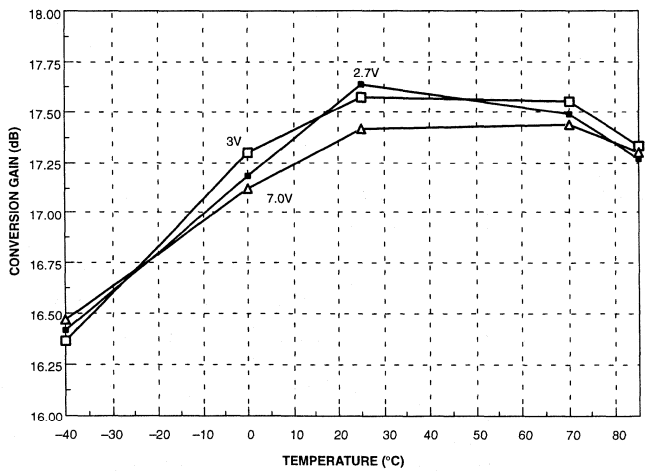


Figure 7. Conversion Gain vs Supply Voltage

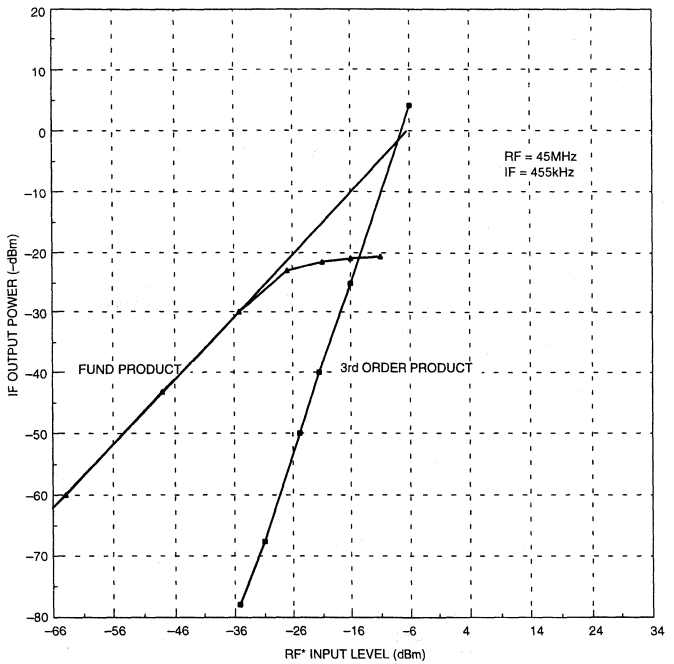


Figure 8. Mixer Third Order Intercept and Compression

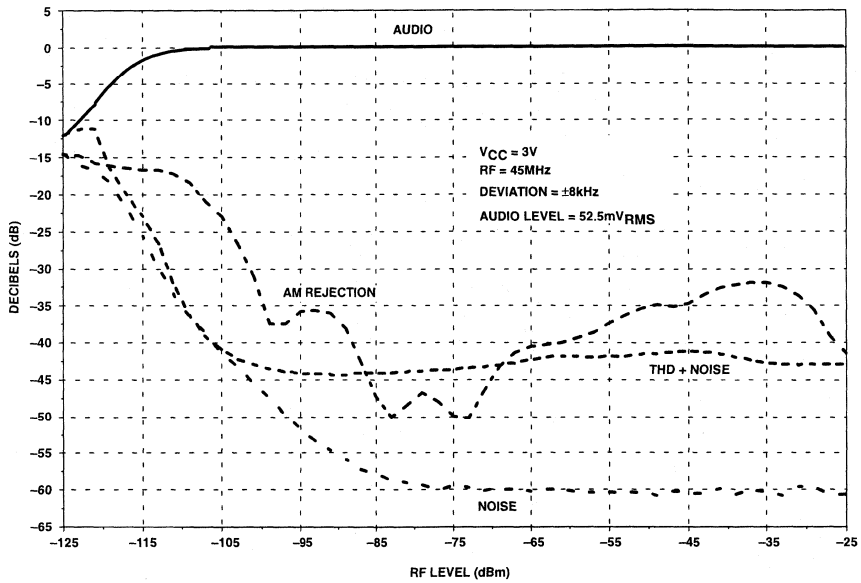


Figure 9. Sensitivity vs RF Level (–40°C)

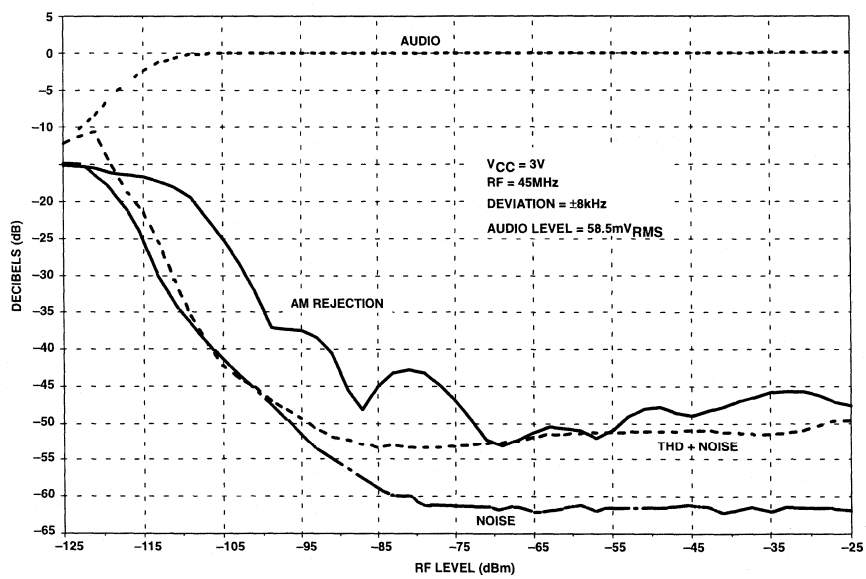


Figure 10. Sensitivity vs RF Level (+25°C)

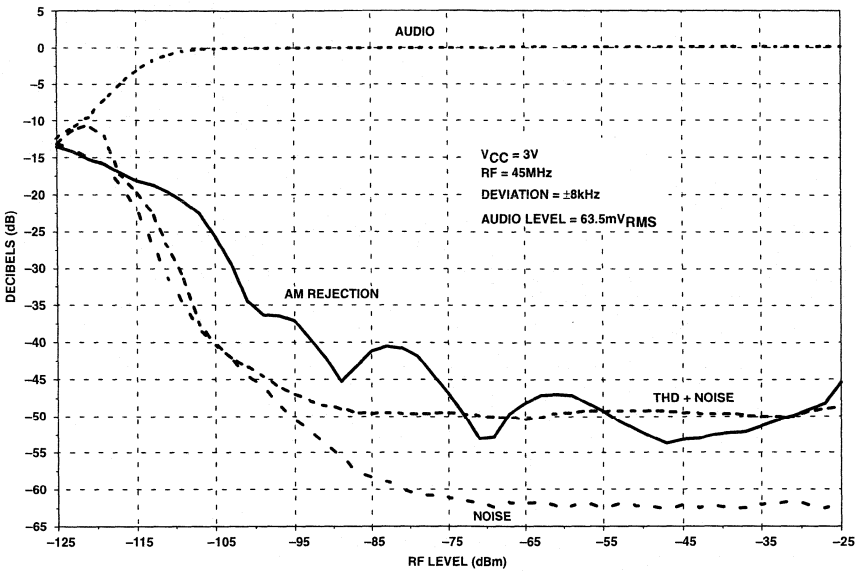


Figure 11. Sensitivity vs RF Level (Temperature 85°C)

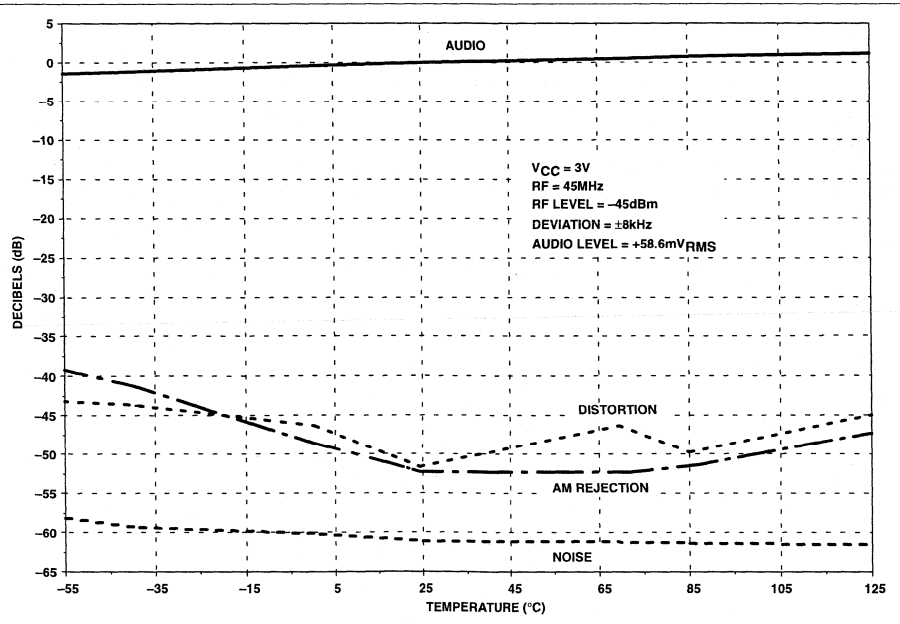


Figure 12. Relative Audio Level, Distortion, AM Rejection and Noise vs Temperature

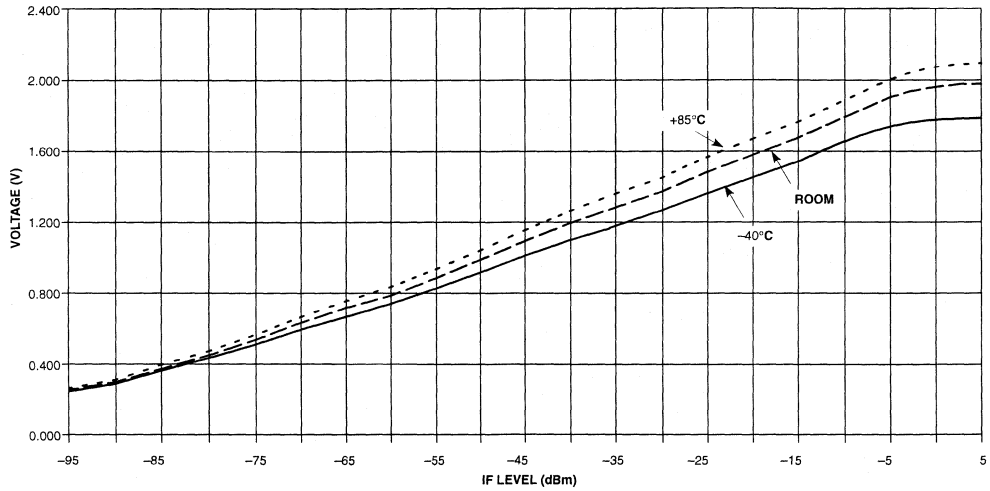


Figure 13. RSSI (455kHz IF @ 3V)

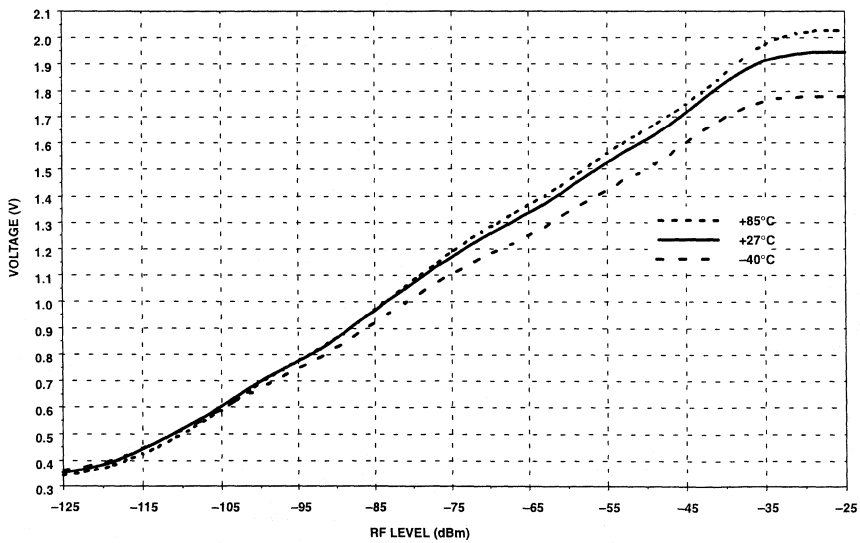


Figure 14. RSSI vs RF Level and Temperature - V_{CC} = 3V

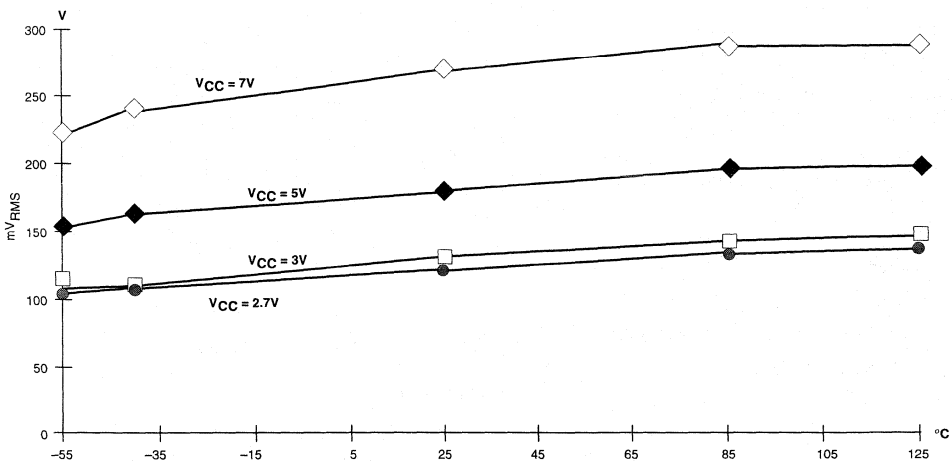


Figure 15. Audio Output vs Temperature

1GHz low voltage LNA and mixer SA611

DESCRIPTION

The SA611 is a combined low-noise amplifier, and mixer designed for high-performance low-power communication systems from 800-1000MHz. The low-noise preamplifier has a 1.7dB noise figure at 881MHz with 15dB gain and an IP3 intercept of -7dBm at the input. The gain is stabilized by on-chip compensation to vary less than ±0.2dB over -40 to +85°C temperature range. The wide-dynamic-range mixer has a 12dB noise figure and IP3 of +7.0dBm at the input at 881MHz. The nominal current drawn from a single 3V supply is 8.3mA. Additionally, the entire circuit can be powered down to further reduce the supply current to less than 20µA.

FEATURES

- Low current consumption
- Outstanding gain and noise figure
- Excellent gain stability versus temperature and supply voltage
- LNA and mixer power down capability

PIN CONFIGURATION

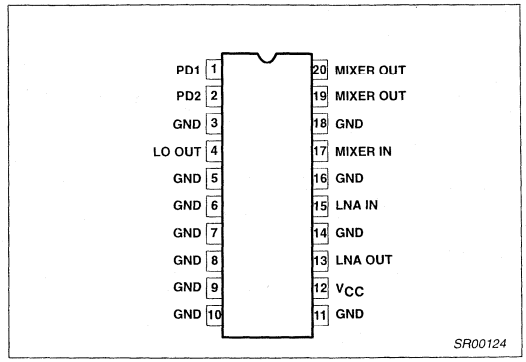


Figure 1. Pin Configuration

APPLICATIONS

- 900MHz cellular and cordless front-end
- Spread spectrum receivers
- RF data links
- UHF frequency conversion
- Portable radio

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Thin Shrink Small Outline Package (Surface-mount, TSSOP)	-40 to +85°C	SA611DH	SOT360-1

BLOCK DIAGRAM

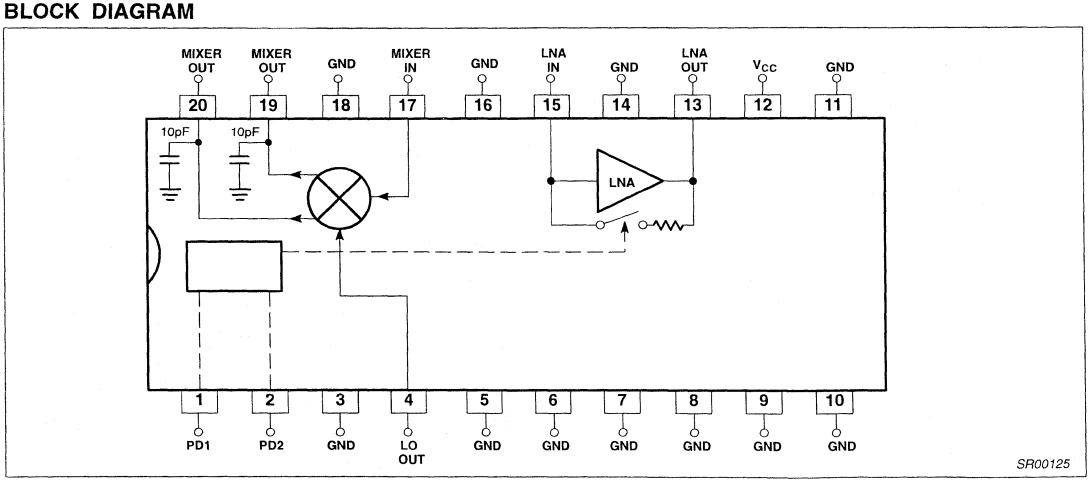


Figure 2. SA611 Block Diagram

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage[NO TAG]	-0.3 to +6	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{CC} + 0.3)	V
P_D	Power dissipation, T_A = 25°C (still air)NO TAG 20-Pin Plastic SSOP	980	mW
T_{JMAX}	Maximum operating junction temperature	150	°C
P_{MAX}	Maximum power input/output	+20	dBm
T_{STG}	Storage temperature range	–65 to +150	°C

NOTE:
1. Transients exceeding 8V on V_{CC} pin may damage product.
2. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance,
   θ_{JA}: 20-Pin SSOP = 110°C/W
3. Pins 19 and 20 are ESD sensitive (mixer outputs).

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	2.7 to 5.5	V
T_A	Operating ambient temperature range	-40 to +85	°C
T_J	Operating junction temperature	-40 to +105	°C

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3.0V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
I_{CC}	Supply current	Full power-on		8.3		mA
		LNA powered-down		5.2		mA
		Full power-down		20		µA
V_T	PD logic threshold voltage		1.2	1.6	1.8	V
V_{IH}	Logic 1 level		2.0		V_{CC}	V
V_{IL}	Logic 0 level		–0.3		0.8	V
I_{IL}	PD1 input current	Enable = 0.4V		10		µA
I_{IH}	PD2 input current	Enable = 2.4V		10		µA

AC ELECTRICAL CHARACTERISTICS

V_{CC} = +3.0V, T_A = 25°C; RF_{IN} = 881MHz, f_{VCO} = 964MHz; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			−3Ω	TYP	+3Ω	
Low Noise Amplifier						
f_{RF}	RF input frequency range		800		1000	MHz
S_{21}	Amplifier gain			15		dB
S_{21}	Amplifier gain in power-down mode			-28		dB
$\Delta S_{21}/\Delta T$	Gain temperature sensitivity enabled			0.006		dB/°C
$\Delta S_{21}/\Delta f$	Gain frequency variation	800MHz - 1.0GHz		±0.013		dB/MHz
S_{12}	Amplifier reverse isolation	@ 881 MHz		-28		dB
S_{11}	Amplifier input match	With ext. impedance matching		-10		dB
S_{22}	Amplifier output match			-10		dB
P_{-1dB}	Amplifier input 1dB gain compression			-20		dBm
IP3	Amplifier input third order intercept			-7		dBm
NF	Amplifier noise figure			1.7		dB
t_{ON}	Amplifier turn-on time (Enable Lo → Hi)			120		µs
t_{OFF}	Amplifier turn-off time (Enable Hi → Lo)			0.3		µs
Mixer						
PG_C	Mixer power conversion gain: $R_P = R_L$ = 1.2kΩ,	f_{RF} = 881MHz, f_{LO} = 964MHz, f_{IF} = 83MHz		8.7		dB
S_{11M}	Mixer input match	Ext. impedance matching req.		-10		dB
NF_M	Mixer SSB noise figure			12		dB
P_{-1dB}	Mixer input 1dB gain compression			-14.5		dBm
$IP3_M$	Mixer input third order intercept			7.0		dBm
IP_{2INT}	Mixer input second order intercept			15		dBm
P_{RFM-IF}	Mixer RF feedthrough	RF_{IN} = -28dBm		-45		dBm
P_{LO-IF}	LO feedthrough to IF	LO = -0dBm		-23		dBm
P_{LO-RFM}	LO to mixer input feedthrough			-36		dBm
P_{LO-RF}	LO to LNA input feedthrough			-38		dBm
Overall System						
G_{SYS}	System gain	LNA + Mixer	23.0	23.7	24.4	dB

Table 1. Power ON/OFF Control Logic

PD1	PD2	
0	0	Full chip power-down
0	1 or open	Mixer on, LNA power-down
1 or open	0	Standby (bias on)
1 or open	1 or open	Full chip power-on (default)

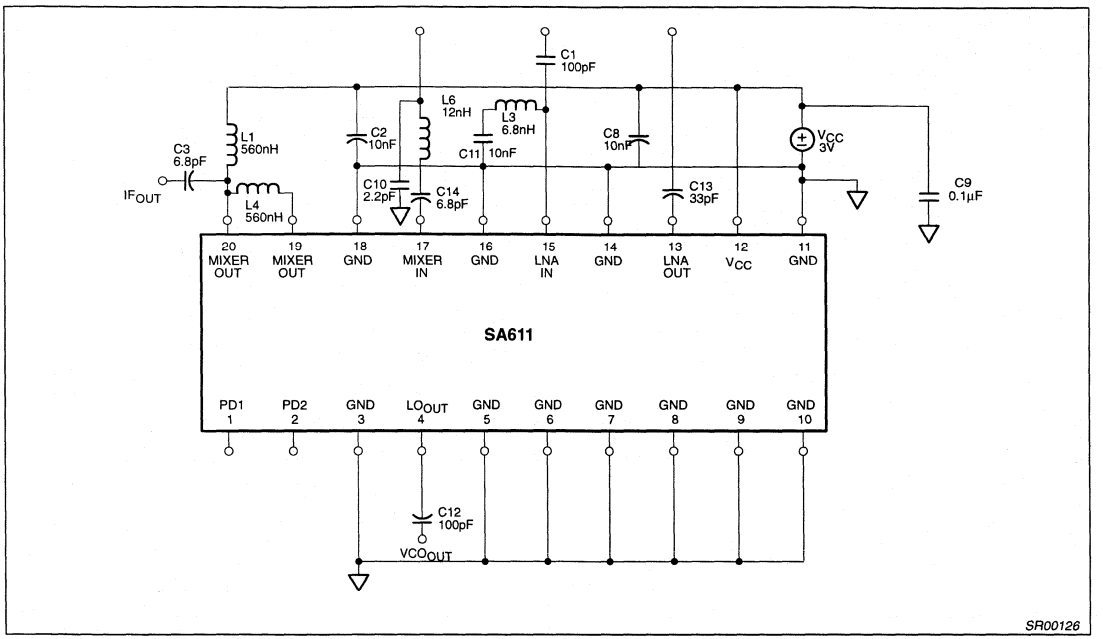


Figure 3. SA611 Applications Circuit

PERFORMANCE CHARACTERISTICS

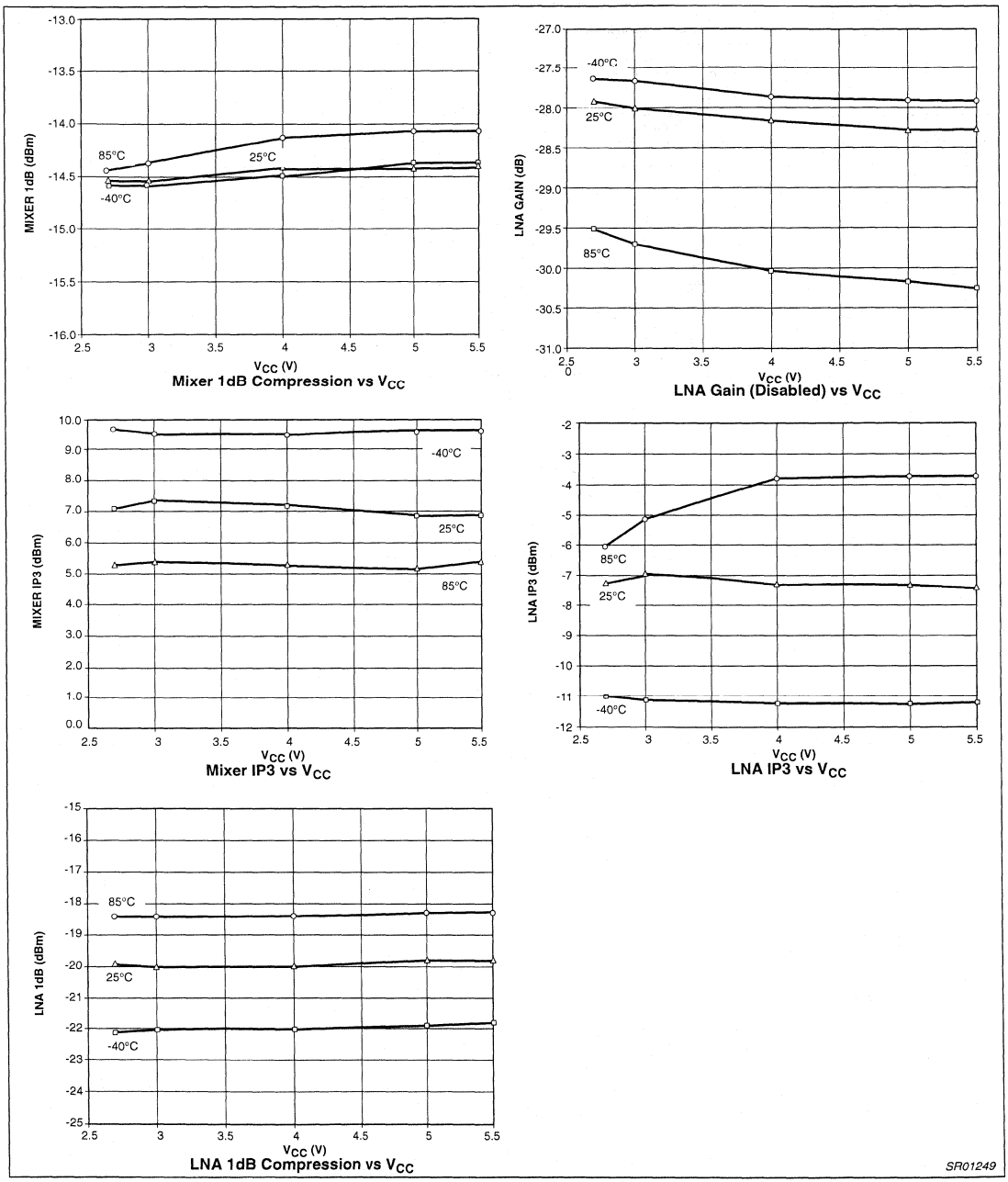
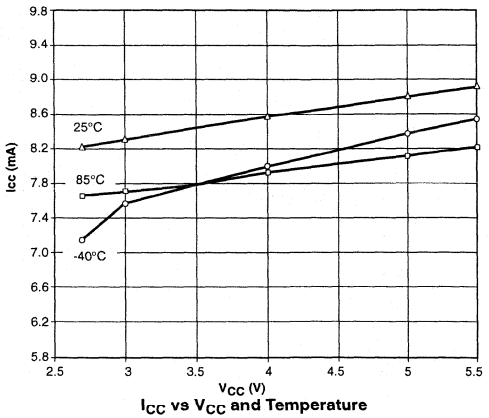
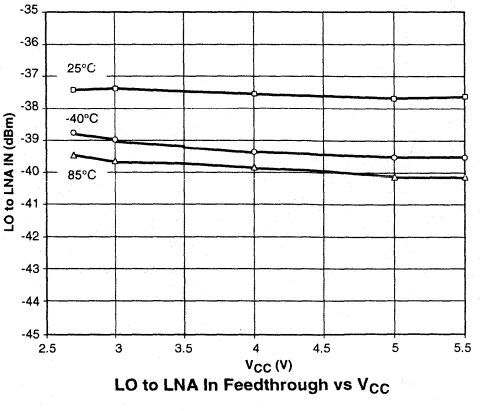


Figure 4.

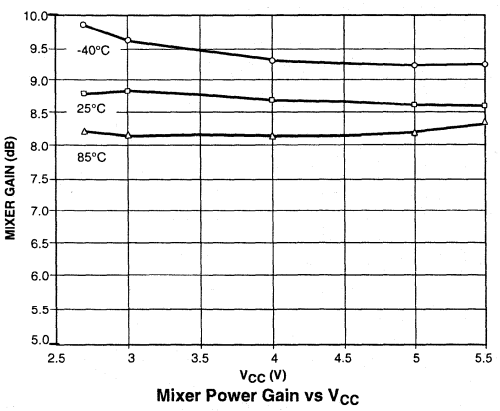
PERFORMANCE CHARACTERISTICS



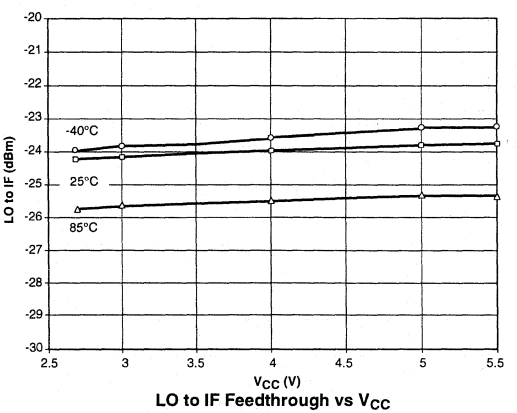
I_{CC} vs V_{CC} and Temperature



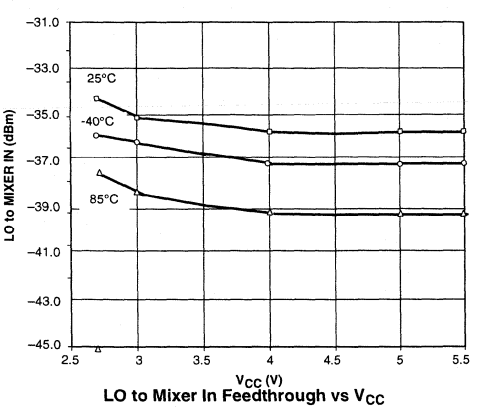
LO to LNA In Feedthrough vs V_{CC}



Mixer Power Gain vs V_{CC}



LO to IF Feedthrough vs V_{CC}



LO to Mixer In Feedthrough vs V_{CC}

SR01250

Figure 5.

PERFORMANCE CHARACTERISTICS

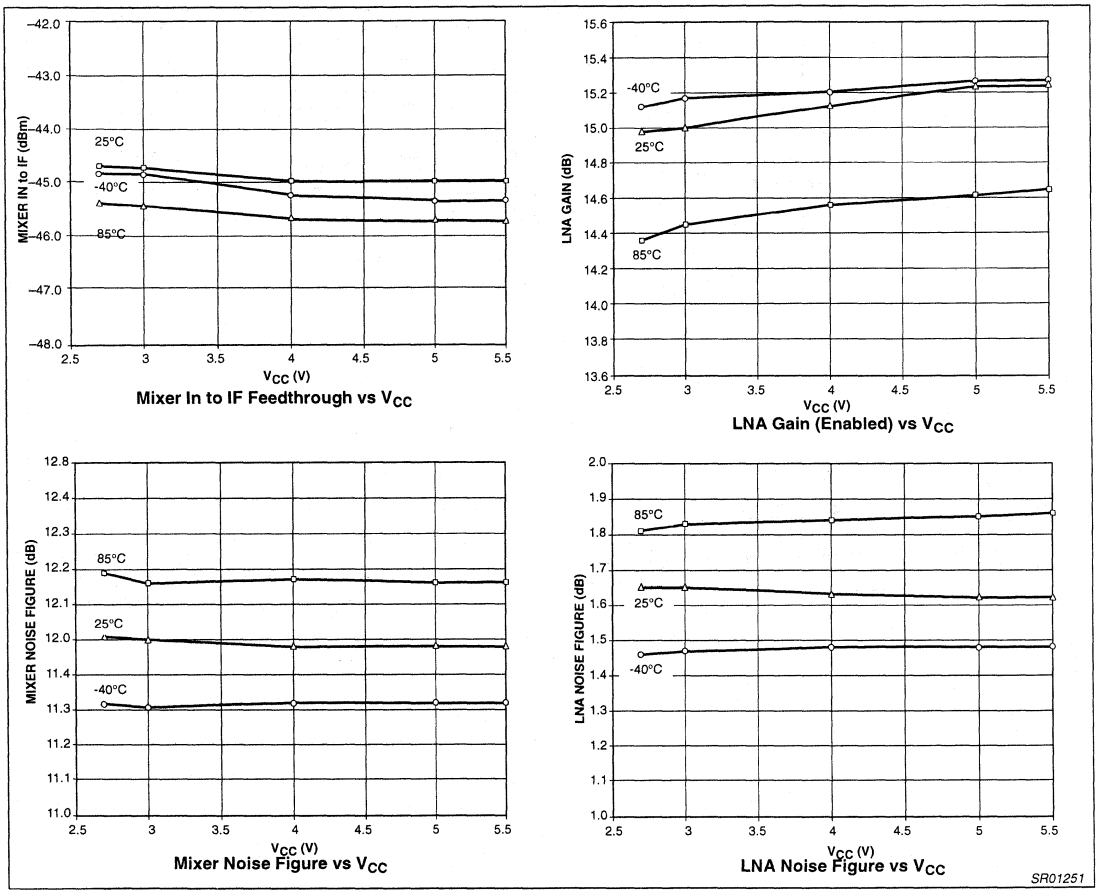
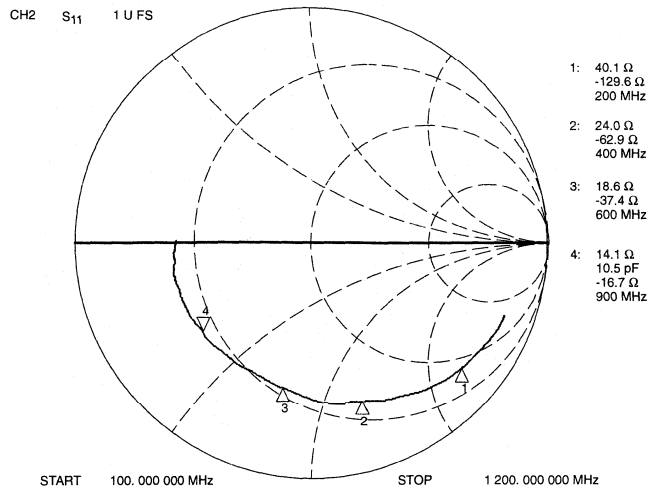
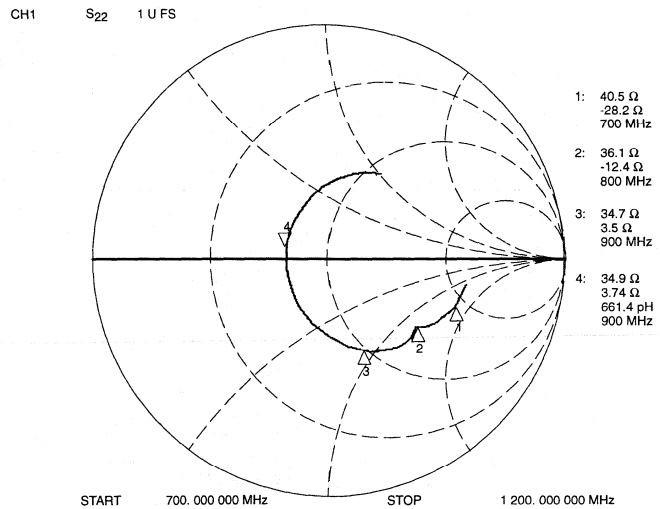


Figure 6.



A. S11 DATA



B. S22 DATA

SR01252

Figure 7. Typical S_{11} of LNA at 3V

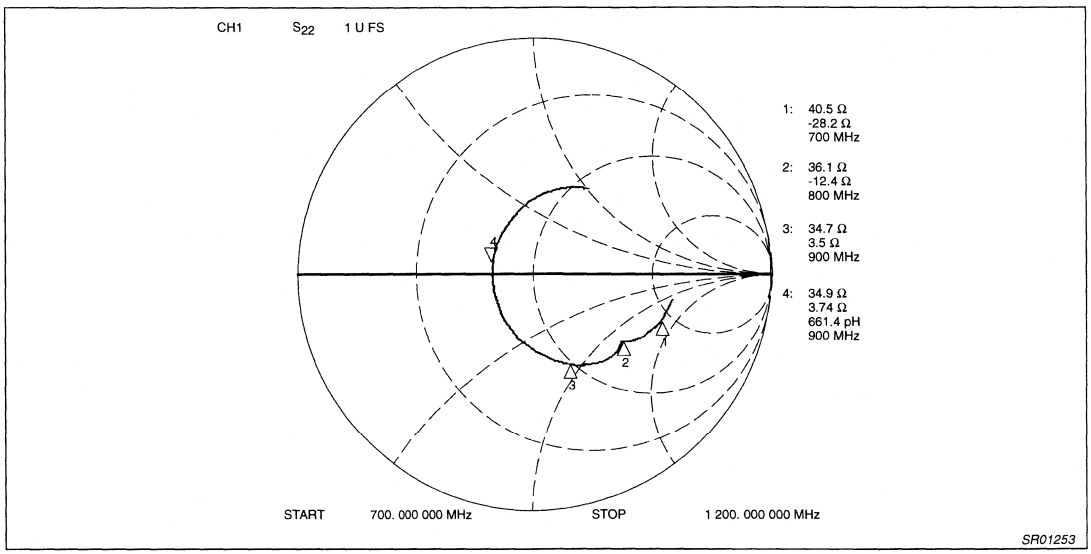


Figure 8. Typical S_{22} of LNA at 3V

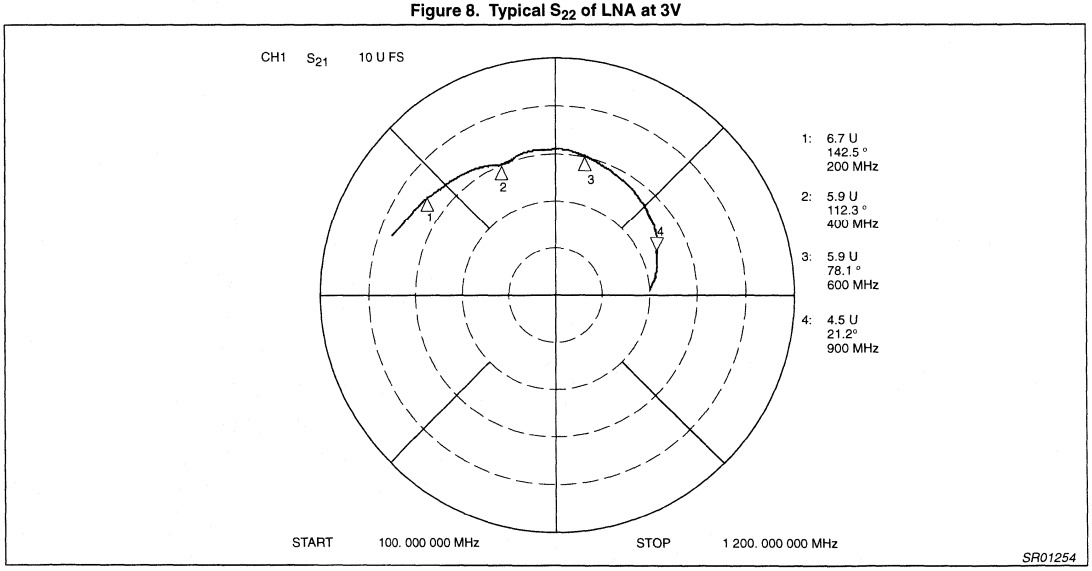


Figure 9. Typical S_{21} of LNA at 3V

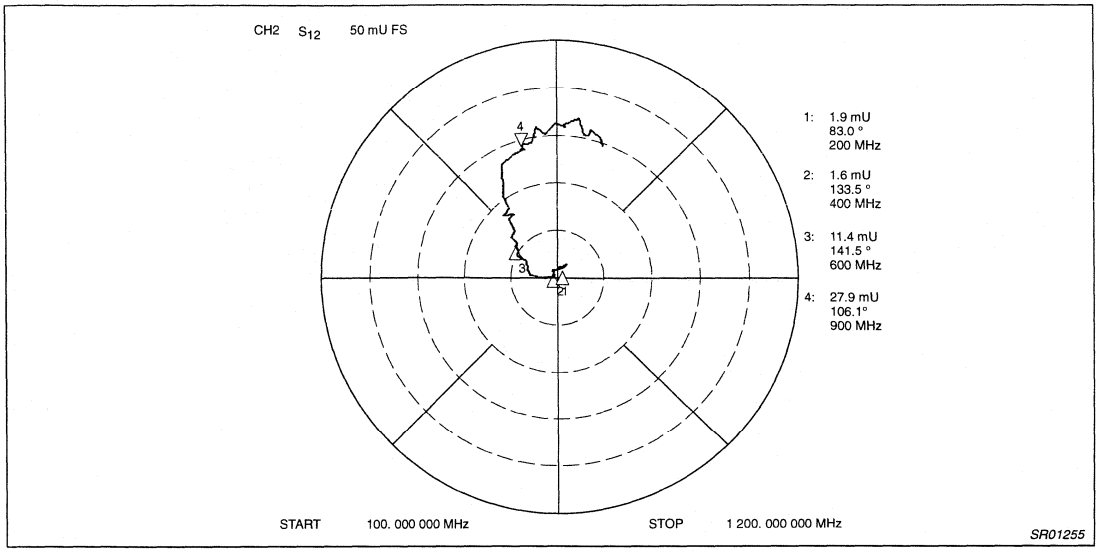


Figure 10. Typical S_{12} of LNA at 3V

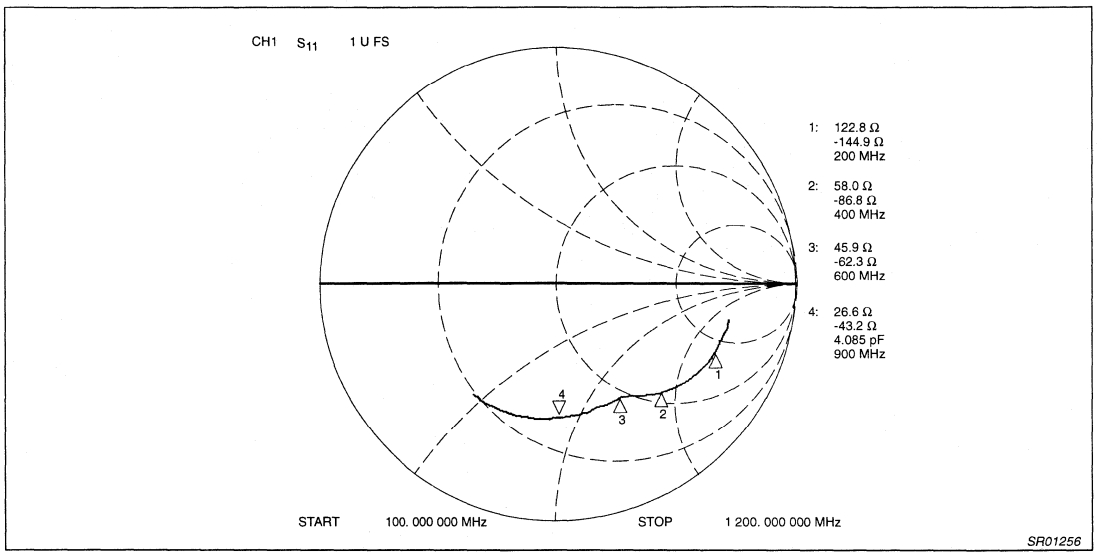


Figure 11. Typical S_{11} of Mixer at 3V

Table 2. Typical S-Parameters of LNA at 3V

LNA								
Freq (MHz)	$\|S_{11}\|$ (U)	$<S_{11}$ (deg)	$\|S_{21}\|$ (U)	$<S_{21}$ (deg)	$\|S_{12}\|$ (U)	$<S_{12}$ (deg)	$\|S_{22}\|$ (U)	$<S_{22}$ (deg)
100	0.86	-20	7.4	160	0.001	91.91	0.59	-9.62
122	0.86	-24	7.1	156	0.001	62	0.58	-11.71
144	0.85	-28	7.0	151	0.001	105.42	0.58	-13.86
166	0.83	-32	6.9	148	0.000	91.65	0.57	-15.89
188	0.82	-36	6.8	144	0.002	100.23	0.57	-17.80
210	0.81	-41	6.7	140	0.002	73.57	0.56	-20.05
232	0.80	-45	6.6	136	0.002	99.70	0.55	-22.37
254	0.79	-48	6.5	133	0.001	84.00	0.54	-24.60
276	0.78	-52	6.4	130	0.001	103.18	0.53	-26.89
298	0.76	-56	6.3	126	0.002	94.33	0.52	-28.72
320	0.75	-59	6.3	123	0.002	66.98	0.51	-30.98
342	0.73	-63	6.2	119	0.002	108.53	0.50	-32.79
364	0.71	-66	6.1	116	0.002	118.13	0.48	-34.68
386	0.70	-69	6.0	113	0.001	103.4	0.47	-36.06
408	0.69	-72	5.9	111	0.001	175.94	0.46	-36.64
430	0.68	-76	5.9	109	0.004	174.1	0.45	-37.21
452	0.69	-78	6.0	106	0.006	162.02	0.46	-38.41
474	0.68	-82	6.1	102	0.007	160.07	0.47	-41.54
496	0.67	-85	6.1	97	0.008	153.6	0.47	-45.75
518	0.66	-89	6.1	93	0.010	146.17	0.46	-50.35
540	0.65	-92	6.1	89	0.009	142.13	0.45	-54.73
562	0.63	-96	6.1	85	0.010	138.49	0.43	-59.16
584	0.62	-99	6.0	81	0.011	146.17	0.42	-63.93
606	0.62	-102	5.9	77	0.011	140.55	0.40	-68.56
628	0.61	-104	5.8	72	0.013	137.2	0.38	-73.48
650	0.61	-107	5.7	69	0.013	130.62	0.36	-78.19
672	0.60	-109	5.7	65	0.016	129.77	0.34	-83.75
694	0.60	-112	5.6	61	0.016	131.94	0.31	-89.81
716	0.59	-115	5.5	57	0.017	128.67	0.29	-96.92
738	0.59	-118	5.5	53	0.019	127.53	0.27	-104.48
760	0.59	-121	5.3	48	0.021	123.42	0.24	-112.81
782	0.59	-124	5.3	44	0.021	122.31	0.22	-122.41
804	0.59	-126	5.1	40	0.022	119.52	0.21	-132.81
826	0.59	-129	5.0	36	0.024	118.29	0.19	-145.39
848	0.59	-132	4.9	31	0.026	115.98	0.18	-159.13
870	0.59	-135	4.8	26	0.027	111.9	0.17	-175.11
892	0.59	-138	4.6	22	0.028	108.11	0.18	169.02
914	0.59	-142	4.5	18	0.028	105.92	0.19	154.96
936	0.59	-144	4.3	14	0.028	106.13	0.20	141.94
958	0.59	-148	4.2	9	0.030	99.79	0.22	130.27
980	0.59	-151	4.0	4	0.031	99.30	0.24	119.5
1002	0.59	-153	3.8	0	0.031	94.81	0.26	110.61
1024	0.59	-157	3.6	-2	0.032	90.91	0.28	102.16
1046	0.59	-160	3.5	-6	0.032	85.65	0.30	94.98
1068	0.59	-164	3.3	-10	0.033	86.10	0.33	88.45
1090	0.59	-167	3.2	-14	0.033	80.59	0.35	82.47
1112	0.59	-170	3.0	-18	0.031	79.18	0.36	77.17
1134	0.58	-172	2.8	-22	0.030	46.32	0.38	71.98
1156	0.58	-175	2.7	-25	0.031	78.57	0.39	67.45
1178	0.57	-178	2.5	-28	0.031	73.66	0.41	62.73
1200	0.57	178	2.4	-31	0.029	71.78	0.42	58.87

Table 3. Typical S-Parameters of Mixer at 3V

Mixer		
Freq (MHz)	$\|S_{11}\|$ (U)	$<S_{11}$ (deg)
100	0.73	-11
122	0.73	-147
144	0.72	-16
166	0.72	-19
188	0.72	-21
210	0.71	-24
232	0.70	-27
254	0.70	-29
276	0.69	-32
298	0.68	-34
320	0.67	-37
342	0.66	-39
364	0.64	-42
386	0.63	-44
408	0.62	-46
430	0.61	-48
452	0.59	-50
474	0.58	-52
496	0.57	-53
518	0.56	-54
540	0.55	-56
562	0.55	-57
584	0.54	-59
606	0.54	-61
628	0.54	-62
650	0.54	-64

Mixer		
Freq (MHz)	$\|S_{11}\|$ (U)	$<S_{11}$ (deg)
672	0.54	-65
694	0.54	-67
716	0.54	-69
738	0.54	-71
760	0.54	-73
782	0.55	-76
804	0.55	-78
826	0.55	-80
848	0.55	-82
870	0.55	-85
892	0.56	-87
914	0.55	-90
936	0.56	-93
958	0.56	-96
980	0.56	-98
1002	0.56	-101
1024	0.57	-104
1046	0.57	-106
1068	0.57	-110
1090	0.57	-112
1112	0.57	-115
1134	0.57	-118
1156	0.57	-121
1178	0.57	-124
1200	0.57	-127

Double-balanced mixer and oscillator SA612A

DESCRIPTION

The SA612A is a low-power VHF monolithic double-balanced mixer with on-board oscillator and voltage regulator. It is intended for low cost, low power communication systems with signal frequencies to 500MHz and local oscillator frequencies as high as 200MHz. The mixer is a "Gilbert cell" multiplier configuration which provides gain of 14dB or more at 45MHz.

The oscillator can be configured for a crystal, a tuned tank operation, or as a buffer for an external L.O. Noise figure at 45MHz is typically below 6dB and makes the device well suited for high performance cordless phone/cellular radio. The low power consumption makes the SA612A excellent for battery operated equipment. Networking and other communications products can benefit from very low radiated energy levels within systems. The SA612A is available in an 8-lead dual in-line plastic package and an 8-lead SO (surface mounted miniature package).

FEATURES

- Low current consumption
- Low cost
- Operation to 500MHz
- Low radiated energy
- Low external parts count; suitable for crystal/ceramic filter
- Excellent sensitivity, gain, and noise figure

PIN CONFIGURATION

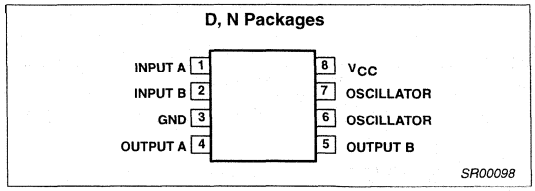


Figure 1. Pin Configuration

APPLICATIONS

- Cordless telephone
- Portable radio
- VHF transceivers
- RF data links
- Sonabuoys
- Communications receivers
- Broadband LANs
- HF and VHF frequency conversion
- Cellular radio mixer/oscillator

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Dual In-Line Plastic (DIP)	-40 to +85°C	SA612AN	SOT97-1
8-Pin Plastic Small Outline (SO) package (Surface-Mount)	-40 to +85°C	SA612AD	SOT96-1

BLOCK DIAGRAM

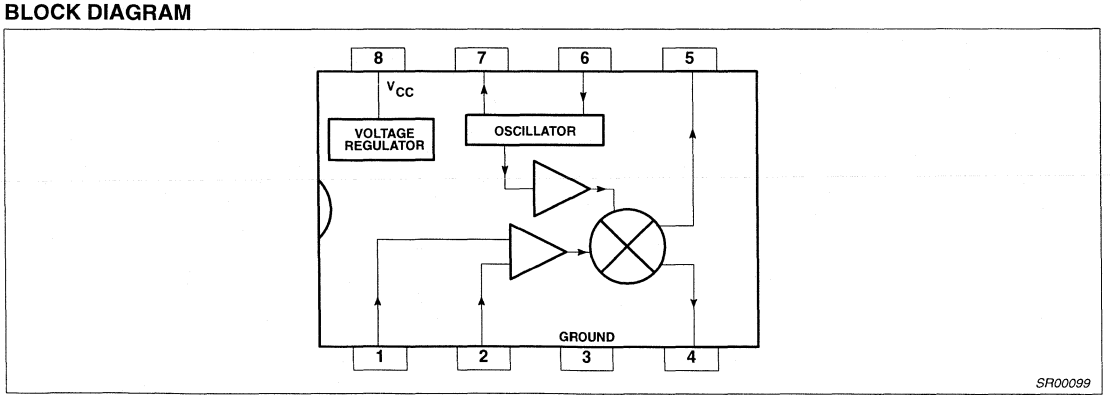


Figure 2. Block Diagram

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Maximum operating voltage	9	V
T_{STG}	Storage temperature	-65 to +150	°C
T_A	Operating ambient temperature range SA612A	-40 to +85	°C

AC/DC ELECTRICAL CHARACTERISTICS

T_A=25°C, V_{CC} = 6V, Figure 3

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Power supply voltage range		4.5		8.0	V
	DC current drain			2.4	3.0	mA
f_{IN}	Input signal frequency			500		MHz
f_{OSC}	Oscillator frequency			200		MHz
	Noise figured at 45MHz			5.0		dB
	Third-order intercept point at 45MHz	RF_{IN}=-45dBm		-13		dBm
	Conversion gain at 45MHz		14	17		dB
R_{IN}	RF input resistance		1.5			kΩ
C_{IN}	RF input capacitance			3		pF
	Mixer output resistance	(Pin 4 or 5)		1.5		kΩ

DESCRIPTION OF OPERATION

The SA612A is a Gilbert cell, an oscillator/buffer, and a temperature compensated bias network as shown in the equivalent circuit. The Gilbert cell is a differential amplifier (Pins 1 and 2) which drives a balanced switching cell. The differential input stage provides gain and determines the noise figure and signal handling performance of the system.

The SA612A is designed for optimum low power performance. When used with the SA614A as a 45MHz cordless phone/cellular radio 2nd IF and demodulator, the SA612A is capable of receiving -119dBm signals with a 12dB S/N ratio. Third-order intercept is typically -15dBm (that's approximately +5dBm output intercept because of the RF gain). The system designer must be cognizant of this large signal limitation. When designing LANs or other closed systems where transmission levels are high, and small-signal or signal-to-noise issues not critical, the input to the SA612A should be appropriately scaled.

TEST CONFIGURATION

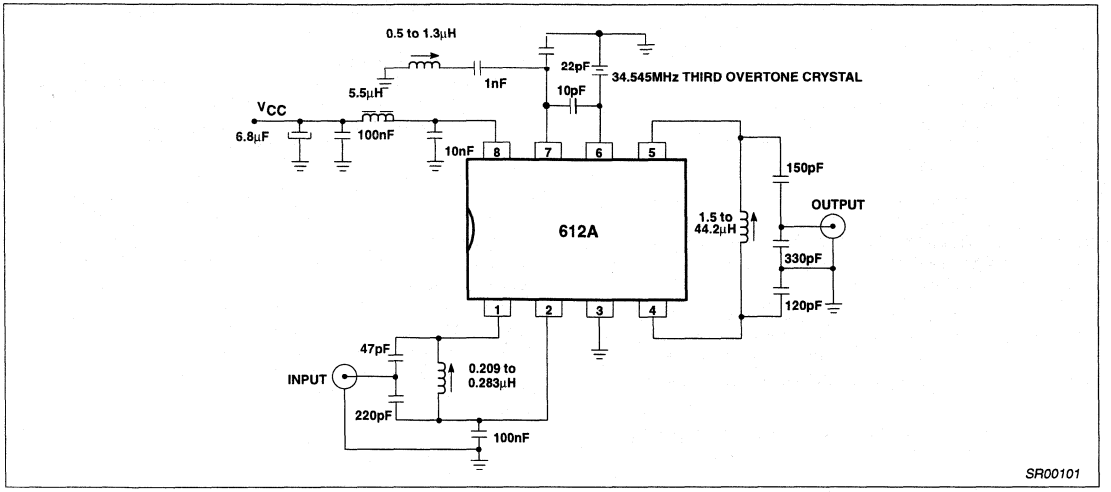


Figure 3. Test Configuration

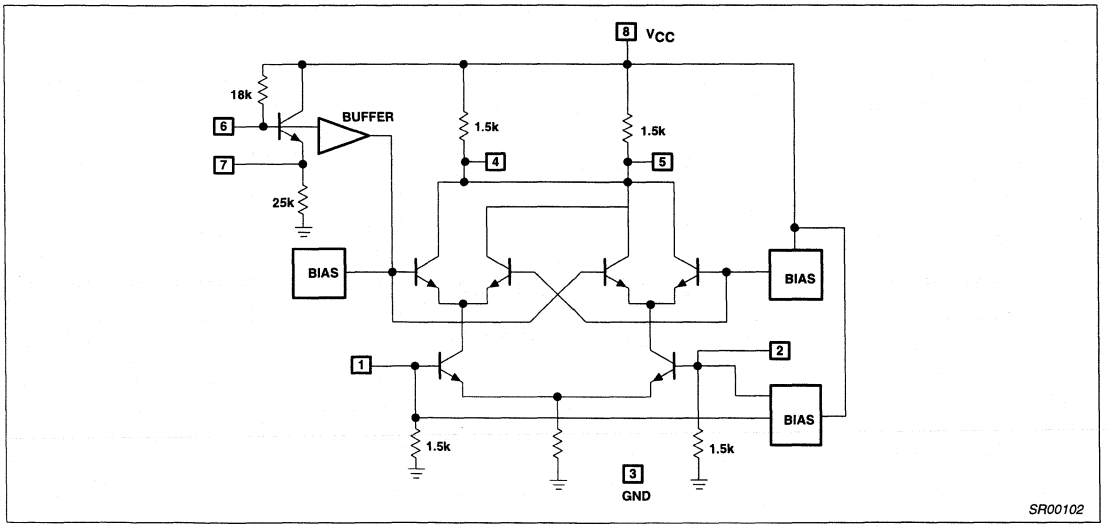


Figure 4. Equivalent Circuit

Besides excellent low power performance well into VHF, the SA612A is designed to be flexible. The input, output, and oscillator ports can support a variety of configurations provided the designer understands certain constraints, which will be explained here.

The RF inputs (Pins 1 and 2) are biased internally. They are symmetrical. The equivalent AC input impedance is approximately 1.5k ll 3pF through 50MHz. Pins 1 and 2 can be used interchangeably, but they should not be DC biased externally. Figure 5 shows three typical input configurations.

The mixer outputs (Pins 4 and 5) are also internally biased. Each output is connected to the internal positive supply by a 1.5kΩ resistor. This permits direct output termination yet allows for balanced output as well. Figure 6 shows three single-ended output configurations and a balanced output.

The oscillator is capable of sustaining oscillation beyond 200MHz in crystal or tuned tank configurations. The upper limit of operation is determined by tank "Q" and required drive levels. The higher the Q of the tank or the smaller the required drive, the higher the permissible oscillation frequency. If the required L.O. is beyond oscillation limits, or the system calls for an external L.O., the external signal can be injected at Pin 6 through a DC blocking capacitor. External L.O. should be 200mV$_{P-P}$ minimum to 300mV$_{P-P}$ maximum.

Figure 7 shows several proven oscillator circuits. Figure 7a is appropriate for cordless phones/cellular radio. In this circuit a third overtone parallel-mode crystal with approximately 5pF load capacitance should be specified. Capacitor C3 and inductor L1 act as a fundamental trap. In fundamental mode oscillation the trap is omitted.

Figure 8 shows a Colpitts varacter tuned tank oscillator suitable for synthesizer-controlled applications. It is important to buffer the output of this circuit to assure that switching spikes from the first counter or prescaler do not end up in the oscillator spectrum. The dual-gate MOSFET provides optimum isolation with low current. The FET offers good isolation, simplicity, and low current, while the bipolar circuits provide the simple solution for non-critical applications. The resistive divider in the emitter-follower circuit should be chosen to provide the minimum input signal which will assume correct system operation.

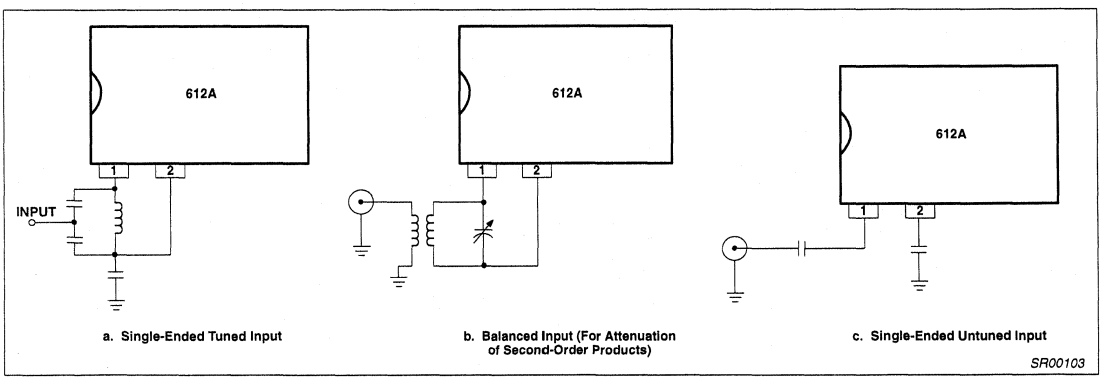


Figure 5. Input Configuration

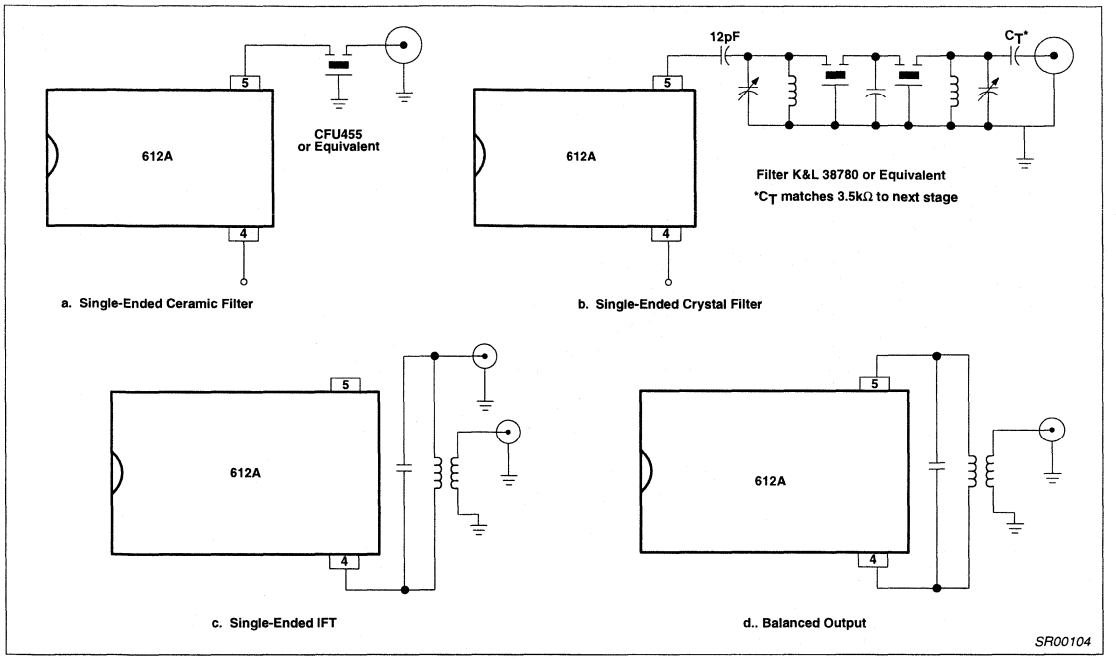


Figure 6. Output Configuration

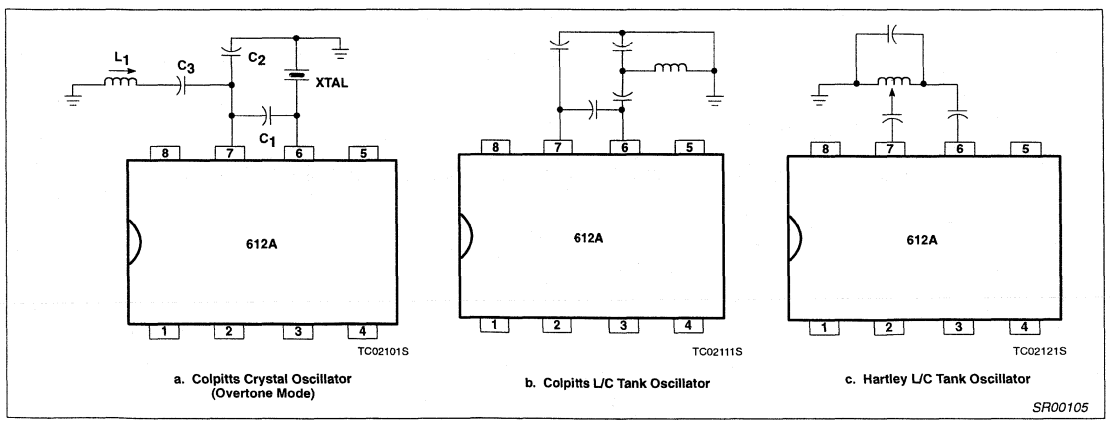


Figure 7. Oscillator Circuits

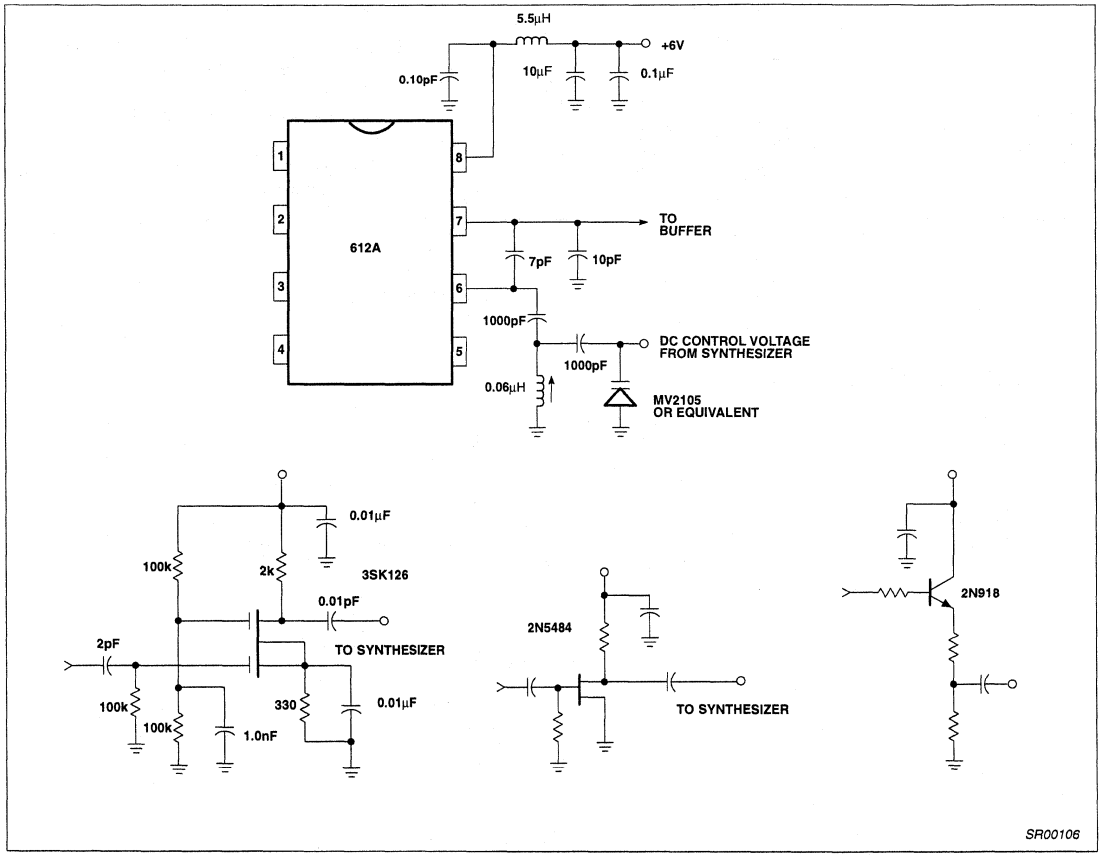


Figure 8. Colpitts Oscillator Suitable for Synthesizer Applications and Typical Buffers

TEST CONFIGURATION

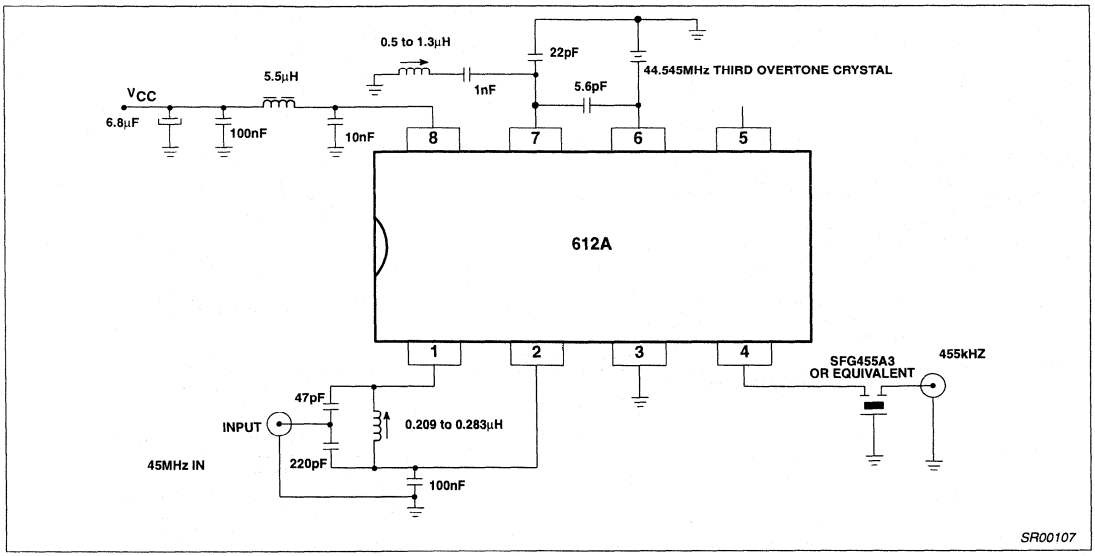


Figure 9. Typical Application for Cordless/Cellular Radio

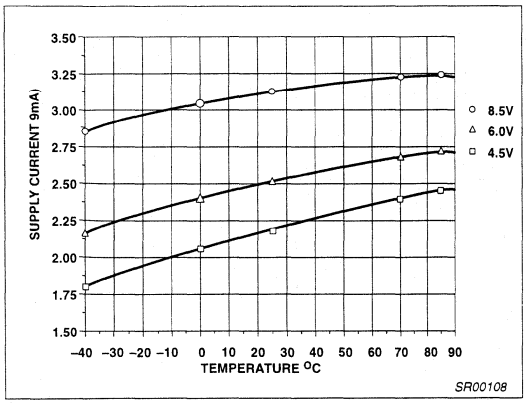


Figure 10. I_{CC} vs Supply Voltage

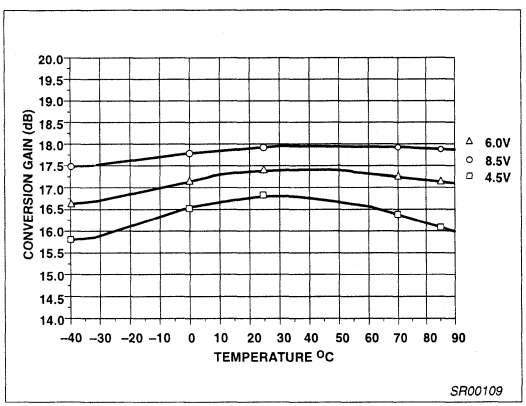


Figure 11. Conversion Gain vs Supply Voltage

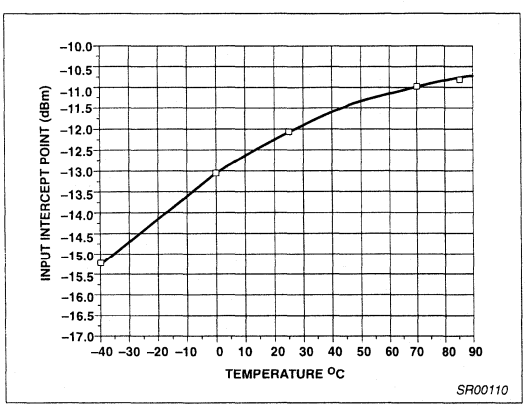


Figure 12. Third-Order Intercept Point

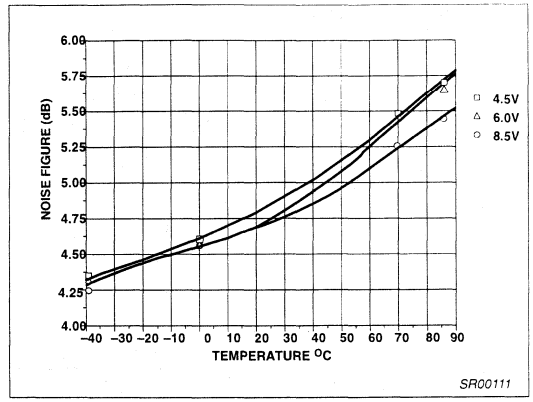


Figure 13. Noise Figure

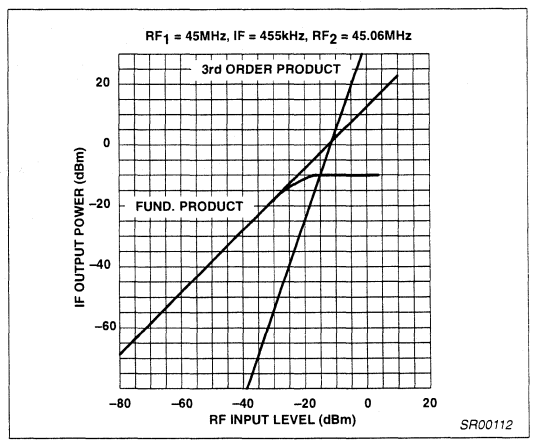


Figure 14. Third-Order Intercept and Compression

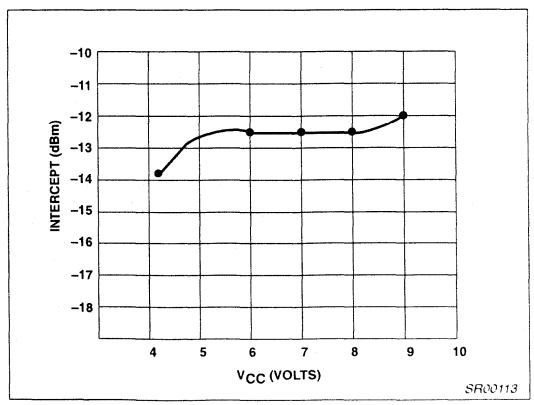


Figure 15. Input Third-Order Intermod Point vs V_{CC}

Low power FM IF system SA614A

DESCRIPTION

The SA614A is an improved monolithic low-power FM IF system incorporating two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic received signal strength indicator, and voltage regulator. The SA614A features higher IF bandwidth (25MHz) and temperature compensated RSSI and limiters permitting higher performance application compared with the SA604. The SA614A is available in a 16-lead dual-in-line plastic and 16-lead SO (surface-mounted miniature) package.

FEATURES

- Low power consumption: 3.3mA typical
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- Two audio outputs - muted and unmuted
- Low external component count; suitable for crystal/ceramic filters
- Excellent sensitivity: 1.5μV across input pins (0.22μV into 50Ω matching network) for 12dB SINAD (Signal to Noise and Distortion ratio) at 455kHz
- SA614A meets cellular radio specifications

PIN CONFIGURATION

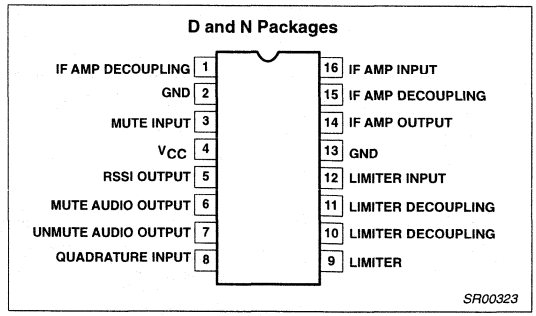


Figure 1. Pin Configuration

APPLICATIONS

- Cellular radio FM IF
- High performance communications receivers
- Intermediate frequency amplification and detection up to 25MHz
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA614AN	SOT28-4
16-Pin Plastic Small Outline (SO) package (Surface-mount)	-40 to +85°C	SA614AD	SOT109-1

BLOCK DIAGRAM

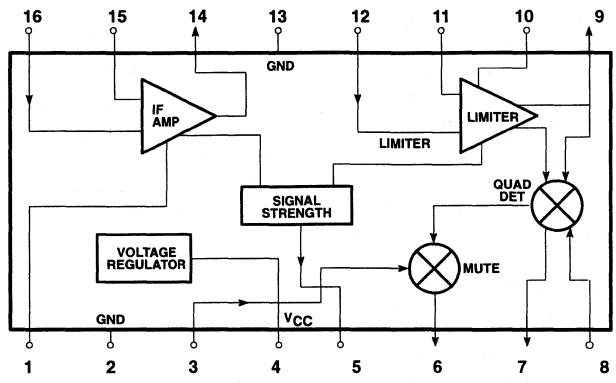


Figure 2. Block Diagram

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	9	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range SA614A	-40 to +85	°C
θ_{JA}	Thermal impedance D package N package	90 75	°C/W °C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA614A			
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		4.5		8.0	V
I_{CC}	DC current drain		2.5	3.3	4.0	mA
	Mute switch input threshold (ON) (OFF)		1.7		 1.0	V V

AC ELECTRICAL CHARACTERISTICS

Typical reading at $T_A = 25°C$; $V_{CC} = \pm 6V$, unless otherwise stated. IF frequency = 455kHz; IF level = -47dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 3. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

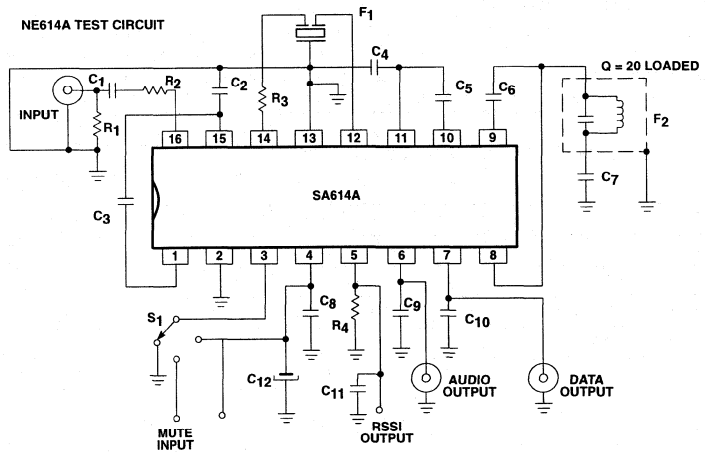
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA614A			
			MIN	TYP	MAX	
	Input limiting -3dB	Test at Pin 16		-92		dBm/50Ω
	AM rejection	80% AM 1kHz	25	33		dB
	Recovered audio level	15nF de-emphasis	60	175	260	mV_{RMS}
	Recovered audio level	150pF de-emphasis		530		mV_{RMS}
THD	Total harmonic distortion		-30	-42		dB
S/N	Signal-to-noise ratio	No modulation for noise		68		dB
	RSSI output[1]	RF level = -118dBm	0	160	800	mV
		RF level = -68dBm	1.7	2.50	3.3	V
		RF level = -18dBm	3.6	4.80	5.8	V
	RSSI range	R_4 = 100k (Pin 5)		80		dB
	RSSI accuracy	R_4 = 100k (Pin 5)		±2.0		dB
	IF input impedance		1.4	1.6		kΩ
	IF output impedance		0.85	1.0		kΩ
	Limiter input impedance		1.4	1.6		kΩ
	Unmuted audio output resistance			58		kΩ
	Muted audio output resistance			58		kΩ

NOTE:

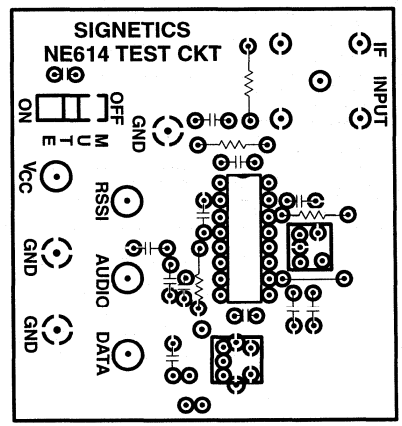
1. SA614A data sheets refer to power at 50Ω input termination; about 21dB less power actually enters the internal 1.5k input.

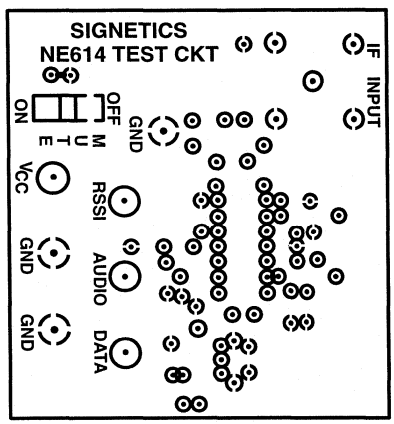
SA614A (50)	SA614A (1.5k)/SA615 (1.5k)
-97dBm	-118dBm
-47dBm	-68dBm
+3dBm	-18dBm

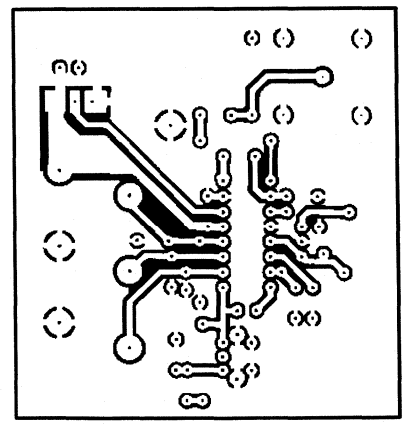
The SA615 and SA614A are both derived from the same basic die. The SA615 performance plots are directly applicable to the SA614A.



C1	100nF + 80 – 20% 63V K10000–25V Ceramic
C2	100nF +10% 50V
C3	100nF ±10% 50V
C4	100nF +10% 50V
C5	100nF ±10% 50V
C6	10pF ±2% 100V NPO Ceramic
C7	100nF ±10% 50V
C8	100nF ±10% 50V
C9	15nF ±10% 50V
C10	150pF ±2% 100V N1500 Ceramic
C11	1nF ±10% 100V K2000-Y5P Ceramic
C12	6.8µF ±20% 25V Tantalum
F1	455kHz Ceramic Filter Murata SFG455A3
F2	455kHz (Ce = 180pF) TOKO RMC 2A6597H
R1	51Ω ±1% 1/4W Metal Film
R2	1500Ω ±1% 1/4W Metal Film
R3	1500Ω ±5% 1/8W Carbon Composition
R4	100kΩ ±1% 1/4W Metal Film







SR00325

Figure 3. SA614A Test Circuit

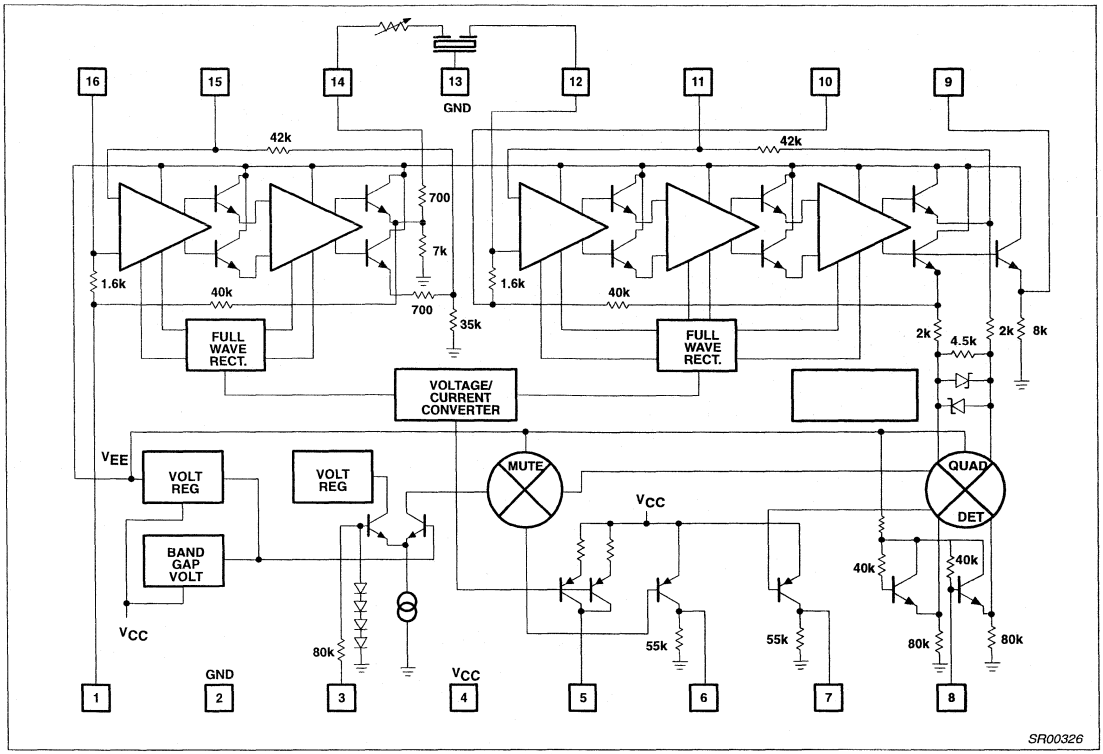


Figure 4. Equivalent Circuit

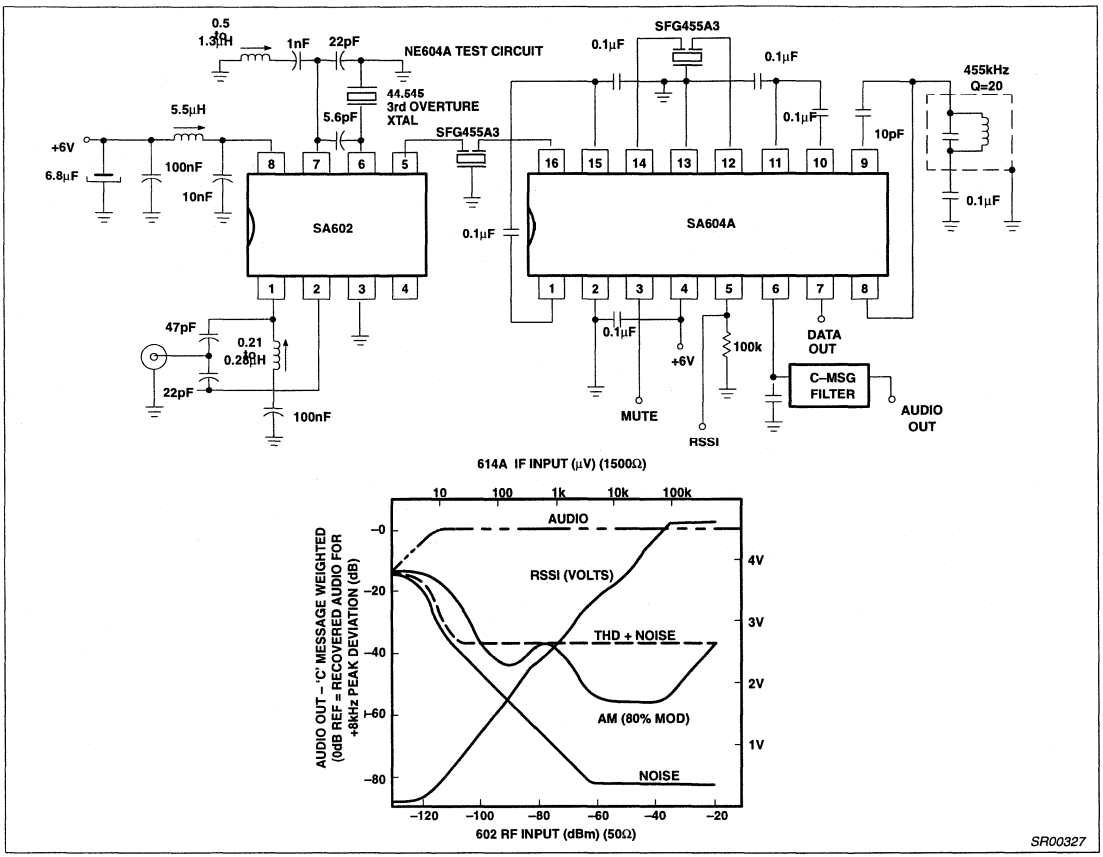


Figure 5. Typical Application Cellular Radio (45MHz to 455kHz)

CIRCUIT DESCRIPTION

The SA614A is a very high gain, high frequency device. Correct operation is not possible if good RF layout and gain stage practices are not used. The SA614A cannot be evaluated independent of circuit, components, and board layout. A physical layout which correlates to the electrical limits is shown in Figure 3. This configuration can be used as the basis for production layout.

The SA614A is an IF signal processing system suitable for IF frequencies as high as 21.4MHz. The device consists of two limiting amplifiers, quadrature detector, direct audio output, muted audio output, and signal strength indicator (with log output characteristic). The sub-systems are shown in Figure 4. A typical application with 45MHz input and 455kHz IF is shown in Figure 5.

IF Amplifiers

The IF amplifier section consists of two log-limiting stages. The first consists of two differential amplifiers with 39dB of gain and a small signal bandwidth of 41MHz (when driven from a 50Ω source). The output of the first limiter is a low impedance emitter follower with 1kΩ of equivalent series resistance. The second limiting stage consists of three differential amplifiers with a gain of 62dB and a small signal AC bandwidth of 28MHz. The outputs of the final differential stage are buffered to the internal quadrature detector. One of the outputs is available at Pin 9 to drive an external quadrature capacitor and L/C quadrature tank.

Both of the limiting amplifier stages are DC biased using feedback. The buffered output of the final differential amplifier is fed back to the input through 42kΩ resistors. As shown in Figure 4, the input impedance is established for each stage by tapping one of the feedback resistors 1.6kΩ from the input. This requires one additional decoupling capacitor from the tap point to ground.

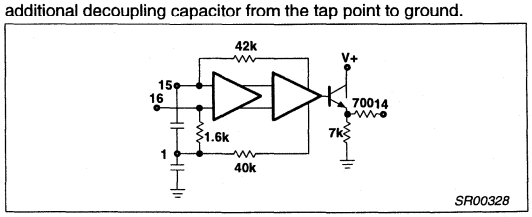


Figure 6. First Limiter Bias

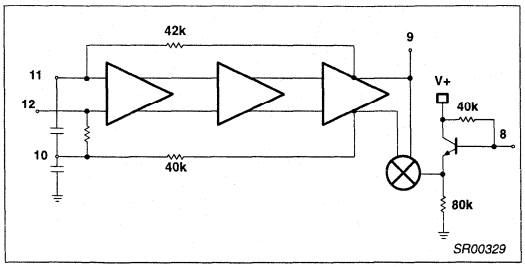


Figure 7. Second Limiter and Quadrature Detector

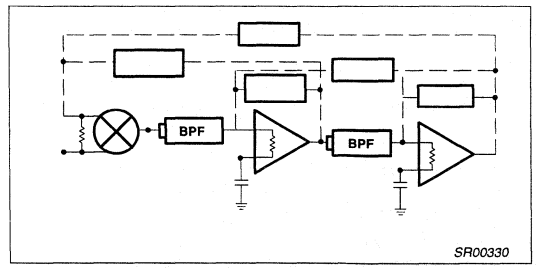


Figure 8. Feedback Paths

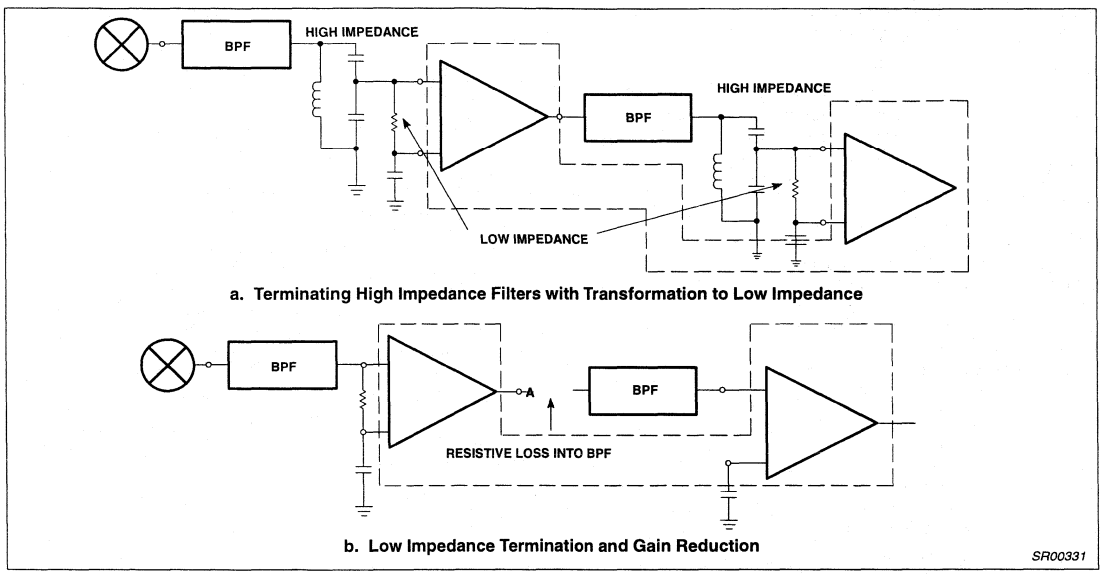


Figure 9. Practical Termination

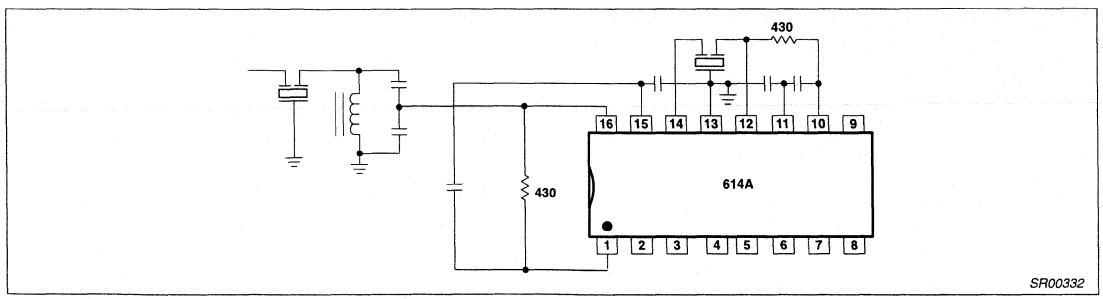


Figure 10. Crystal Input Filter with Ceramic Interstage Filter

Because of the very high gain, bandwidth and input impedance of the limiters, there is a very real potential for instability at IF frequencies above 455kHz. The basic phenomenon is shown in Figure 8. Distributed feedback (capacitance, inductance and radiated fields) forms a divider from the output of the limiters back to the inputs (including RF input). If this feedback divider does not cause attenuation greater than the gain of the forward path, then oscillation or low level regeneration is likely. If regeneration occurs, two symptoms may be present: (1)The RSSI output will be high with no signal input (should nominally be 250mV or lower), and (2) the demodulated output will demonstrate a threshold. Above a certain

input level, the limited signal will begin to dominate the regeneration, and the demodulator will begin to operate in a "normal" manner.

There are three primary ways to deal with regeneration: (1) Minimize the feedback by gain stage isolation, (2) lower the stage input impedances, thus increasing the feedback attenuation factor, and (3) reduce the gain. Gain reduction can effectively be accomplished by adding attenuation between stages. This can also lower the input impedance if well planned. Examples of impedance/gain adjustment are shown in Figure 9. Reduced gain will result in reduced limiting sensitivity.

A feature of the SA614A IF amplifiers, which is not specified, is low phase shift. The SA614A is fabricated with a 10GHz process with very small collector capacitance. It is advantageous in some applications that the phase shift changes only a few degrees over a wide range of signal input amplitudes.

Stability Considerations

The high gain and bandwidth of the SA614A in combination with its very low currents permit circuit implementation with superior performance. However, stability must be maintained and, to do that, every possible feedback mechanism must be addressed. These mechanisms are: 1) Supply lines and ground, 2) stray layout inductances and capacitances, 3) radiated fields, and 4) phase shift. As the system IF increases, so must the attention to fields and strays. However, ground and supply loops cannot be overlooked, especially at lower frequencies. Even at 455kHz, using the test layout in Figure 3, instability will occur if the supply line is not decoupled with two high quality RF capacitors, a 0.1µF monolithic right at the V_{CC} pin, and a 6.8µF tantalum on the supply line. An electrolytic is not an adequate substitute. At 10.7MHz, a 1µF tantalum has proven acceptable with this layout. Every layout must be evaluated on its own merit, but don't underestimate the importance of good supply bypass.

At 455kHz, if the layout of Figure 3 or one substantially similar is used, it is possible to directly connect ceramic filters to the input and between limiter stages with no special consideration. At frequencies above 2MHz, some input impedance reduction is usually necessary. Figure 9 demonstrates a practical means.

As illustrated in Figure 10, 430Ω external resistors are applied in parallel to the internal 1.6kΩ load resistors, thus presenting approximately 330Ω to the filters. The input filter is a crystal type for narrowband selectivity. The filter is terminated with a tank which transforms to 330Ω. The interstage filter is a ceramic type which doesn't contribute to system selectivity, but does suppress wideband noise and stray signal pickup. In wideband 10.7MHz IFs the input filter can also be ceramic, directly connected to Pin 16.

In some products it may be impractical to utilize shielding, but this mechanism may be appropriate to 10.7MHz and 21.4MHz IF. One of the benefits of low current is lower radiated field strength, but lower does not mean non-existent. A spectrum analyzer with an active probe will clearly show IF energy with the probe held in the proximity of the second limiter output or quadrature coil. No specific recommendations are provided, but mechanical shielding should be considered if layout, bypass, and input impedance reduction do not solve a stubborn instability.

The final stability consideration is phase shift. The phase shift of the limiters is very low, but there is phase shift contribution from the quadrature tank and the filters. Most filters demonstrate a large phase shift across their passband (especially at the edges). If the quadrature detector is tuned to the edge of the filter passband, the combined filter and quadrature phase shift can aggravate stability. This is not usually a problem, but should be kept in mind.

Quadrature Detector

Figure 7 shows an equivalent circuit of the SA614A quadrature detector. It is a multiplier cell similar to a mixer stage. Instead of mixing two different frequencies, it mixes two signals of common frequency but different phase. Internal to the device, a constant amplitude (limited) signal is differentially applied to the lower port of the multiplier. The same signal is applied single-ended to an external capacitor at Pin 9. There is a 90° phase shift across the plates of this capacitor, with the phase shifted signal applied to the upper port of the multiplier at Pin 8. A quadrature tank (parallel L/C network) permits frequency selective phase shifting at the IF frequency. This quadrature tank must be returned to ground through a DC blocking capacitor.

The loaded Q of the quadrature tank impacts three fundamental aspects of the detector: Distortion, maximum modulated peak deviation, and audio output amplitude. Typical quadrature curves are illustrated in Figure 12. The phase angle translates to a shift in the multiplier output voltage.

Thus a small deviation gives a large output with a high Q tank. However, as the deviation from resonance increases, the non-linearity of the curve increases (distortion), and, with too much deviation, the signal will be outside the quadrature region (limiting the peak deviation which can be demodulated). If the same peak deviation is applied to a lower Q tank, the deviation will remain in a region of the curve which is more linear (less distortion), but creates a smaller phase angle (smaller output amplitude). Thus the Q of the quadrature tank must be tailored to the design. Basic equations and an example for determining Q are shown below. This explanation includes first-order effects only.

Frequency Discriminator Design Equations for SA614A

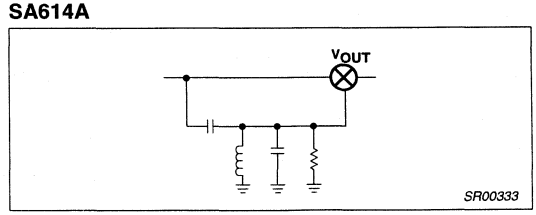


Figure 11.

$$V_O = \frac{C_S}{C_P + C_S} \cdot \frac{1}{1 + \frac{\omega_1}{Q_1 S} + \left(\frac{\omega_1}{S}\right)^2} \cdot V_{IN} \quad (1a)$$

$$\text{where } \omega_1 = \frac{1}{\sqrt{L(C_P + C_S)}} \quad (1b)$$

$$Q_1 = R\,(C_P + C_S)\,\omega_1 \quad (1c)$$

From the above equation, the phase shift between nodes 1 and 2, or the phase across C_S will be:

$$\phi = \angle V_O - \angle V_{IN} = t_g^{-1}\left[\frac{\frac{\omega_1}{Q_1\omega}}{1-\left(\frac{\omega_1}{\omega}\right)^2}\right] \quad (2)$$

Figure 12 is the plot of ϕ vs. $\left(\frac{\omega}{\omega_1}\right)$

It is notable that at $\omega = \omega_1$, the phase shift is $\frac{\pi}{2}$ and the response is close to a straight line with a slope of $\frac{\Delta\phi}{\Delta\omega} = \frac{2Q_1}{\omega_1}$

The signal V_O would have a phase shift of $\left[\frac{\pi}{2} - \frac{2Q_1}{\omega_1}\omega\right]$ with respect to the V_{IN}.

If $V_{IN} = A \sin \omega t \Rightarrow V_O = A$ (3)

$$\sin\left[\omega t + \frac{\pi}{2} - \frac{2Q_1}{\omega_1}\omega\right]$$

Multiplying the two signals in the mixer, and low pass filtering yields:

$V_{IN} \bullet V_O = A^2 \sin \omega t$ (4)

$$\sin\left[\omega t + \frac{\pi}{2} - \frac{2Q_1}{\omega_1}\omega\right]$$

after low pass filtering

$$\Rightarrow V_{OUT} = \frac{1}{2}A^2 \cos\left[\frac{\pi}{2} - \frac{2Q_1}{\omega_1}\omega\right] \quad (5)$$

$$= \frac{1}{2}A^2 \sin\left(\frac{2Q_1}{\omega_1}\right)\omega$$

$$V_{OUT} \propto 2Q_1\frac{\omega}{\omega_1} = \left[2Q_1\left(\frac{\omega_1 + \Delta\omega}{\omega_1}\right)\right] \quad (6)$$

For $\frac{2Q_1\omega}{\omega_1} << \frac{\pi}{2}$

Which is discriminated FM output. (Note that $\Delta\omega$ is the deviation frequency from the carrier ω_1.

Ref. Krauss, Raab, Bastian; Solid State Radio Eng.; Wiley, 1980, p. 311. Example: At 455kHz IF, with ±5kHz FM deviation. The maximum normalized frequency will be

$$\frac{455 \pm 5\text{kHz}}{455} = 1.010 \text{ or } 0.990$$

Go to the f vs. normalized frequency curves (Figure 12) and draw a vertical straight line at $\frac{\omega}{\omega_1} = 1.01$.

The curves with Q = 100, Q = 40 are not linear, but Q = 20 and less shows better linearity for this application. Too small Q decreases the amplitude of the discriminated FM signal. (Eq. 6) $\Rightarrow$ Choose a Q = 20

The internal R of the 614A is 40k. From Eq. 1c, and then 1b, it results that

$C_P + C_S = 174\text{pF}$ and $L = 0.7\text{mH}$.

A more exact analysis including the source resistance of the previous stage shows that there is a series and a parallel resonance in the phase detector tank. To make the parallel and series resonances close, and to get maximum attenuation of higher harmonics at 455kHz IF, we have found that a C_S = 10pF and C_P = 164pF (commercial values of 150pF or 180pF may be practical), will give the best results. A variable inductor which can be adjusted around 0.7mH should be chosen and optimized for minimum distortion. (For 10.7MHz, a value of C_S = 1pF is recommended.)

Audio Outputs

Two audio outputs are provided. Both are PNP current-to-voltage converters with 55kΩ nominal internal loads. The unmuted output is always active to permit the use of signaling tones in systems such as cellular radio. The other output can be muted with 70dB typical attenuation. The two outputs have an internal 180° phase difference.

The nominal frequency response of the audio outputs is 300kHz. this response can be increased with the addition of external resistors from the output pins to ground in parallel with the internal 55k resistors, thus lowering the output time constant. Singe the output structure is a current-to-voltage converter (current is driven into the resistance, creating a voltage drop), adding external parallel resistance also has the effect of lowering the output audio amplitude and DC level.

This technique of audio bandwidth expansion can be effective in many applications such as SCA receivers and data transceivers. Because the two outputs have a 180° phase relationship, FSK demodulation can be accomplished by applying the two output differentially across the inputs of an op amp or comparator. Once the threshold of the reference frequency (or "no-signal" condition) has been established, the two outputs will shift in opposite directions (higher or lower output voltage) as the input frequency shifts. The output of the comparator will be logic output. The choice of op amp or comparator will depend on the data rate. With high IF frequency (10MHz and above), and wide IF bandwidth (L/C filters) data rates in excess of 4Mbaud are possible.

RSSI

The "received signal strength indicator", or RSSI, of the SA614A demonstrates monotonic logarithmic output over a range of 90dB. The signal strength output is derived from the summed stage currents in the limiting amplifiers. It is essentially independent of the IF frequency. Thus, unfiltered signals at the limiter inputs, spurious products, or regenerated signals will manifest themselves as RSSI outputs. An RSSI output of greater than 250mV with no signal (or a very small signal) applied, is an indication of possible regeneration or oscillation.

In order to achieve optimum RSSI linearity, there must be a 12dB insertion loss between the first and second limiting amplifiers. With a typical 455kHz ceramic filter, there is a nominal 4dB insertion loss in the filter. An additional 6dB is lost in the interface between the filter and the input of the second limiter. A small amount of additional loss must be introduced with a typical ceramic filter. In the test circuit used for cellular radio applications (Figure 5) the optimum linearity was achieved with a 5.1kΩ resistor from the output of the first limiter (Pin 14) to the input of the interstage filter. With this resistor from Pin 14 to the filter, sensitivity of 0.25μV for 12dB SINAD was achieved. With the 3.6kΩ resistor, sensitivity was

optimized at 0.22μV for 12dB SINAD with minor change in the RSSI linearity.

Any application which requires optimized RSSI linearity, such as spectrum analyzers, cellular radio, and certain types of telemetry, will require careful attention to limiter interstage component selection. This will be especially true with high IF frequencies which require insertion loss or impedance reduction for stability.

At low frequencies the RSSI makes an excellent logarithmic AC voltmeter.

For data applications the RSSI is effective as an amplitude shift keyed (ASK) data slicer. If a comparator is applied to the RSSI and the threshold set slightly above the no signal level, when an in-band signal is received the comparator will be sliced. Unlike FSK demodulation, the maximum data rate is somewhat limited. An internal capacitor limits the RSSI frequency response to about 100kHz. At high data rates the rise and fall times will not be symmetrical.

The RSSI output is a current-to-voltage converter similar to the audio outputs. However, an external resistor is required. With a 91kΩ resistor, the output characteristic is 0.5V for a 10dB change in the input amplitude.

Additional Circuitry

Internal to the SA614A are voltage and current regulators which have been temperature compensated to maintain the performance of the device over a wide temperature range. These regulators are not accessible to the user.

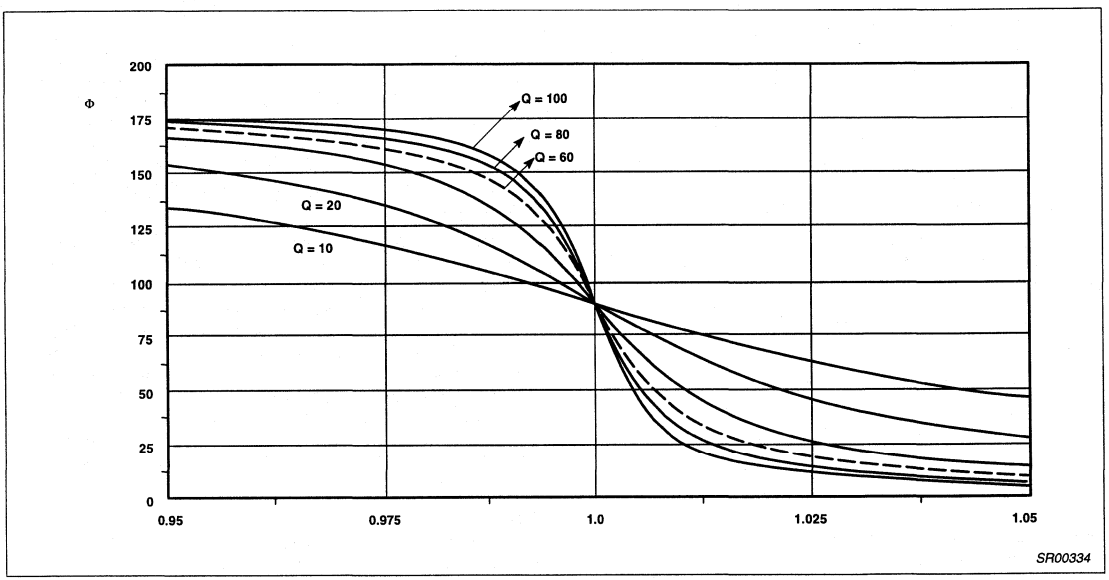


Figure 12. Phase vs Normalized IF Frequency $\frac{\omega}{\omega_I} \quad 1 \pm \frac{\Delta\omega}{\omega_I}$

High performance low power mixer FM IF system SA615

DESCRIPTION

The SA615 is a high performance monolithic low-power FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic received signal strength indicator (RSSI), and voltage regulator. The SA615 combines the functions of Signetics' SA602 and SA604A, but features a higher mixer input intercept point, higher IF bandwidth (25MHz) and temperature compensated RSSI and limiters permitting higher performance application. The SA615 is available in 20-lead dual-in-line plastic, 20-lead SOL (surface-mounted miniature package) and 20-lead SSOP (shrink small outline package).

The SA605 and SA615 are functionally the same device types. The difference between the two devices lies in the guaranteed specifications. The SA615 has a higher I_{CC}, lower input third order intercept point, lower conversion mixer gain, lower limiter gain, lower AM rejection, lower SINAD, higher THD, and higher RSSI error than the SA615. Both the SA605 and SA615 devices will meet the EIA specifications for AMPS and TACS cellular radio applications.

For additional technical information please refer to application notes AN1994, 1995 and 1996, which include example application diagrams, a complete overview of the product, and artwork for reference.

FEATURES

- Low power consumption: 5.7mA typical at 6V
- Mixer input to >500MHz
- Mixer conversion power gain of 13dB at 45MHz
- Mixer noise figure of 4.6dB at 45MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator to 1GHz local oscillator can be injected)
- 102dB of IF Amp/Limiter gain
- 25MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- Two audio outputs – muted and unmuted
- Low external component count; suitable for crystal/ceramic/LC filters

PIN CONFIGURATION

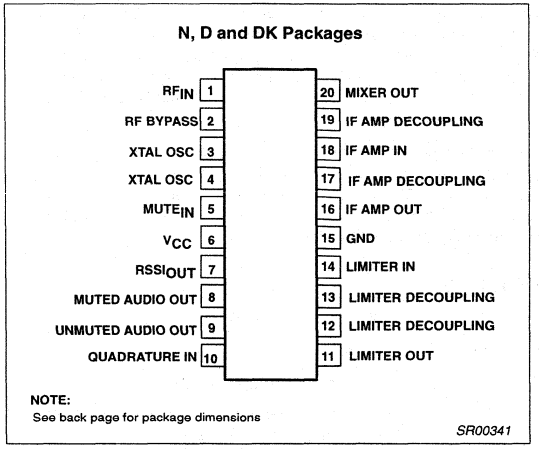


Figure 1. Pin Configuration

- Excellent sensitivity: 0.22μV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone with RF at 45MHz and IF at 455kHz
- SA615 meets cellular radio specifications
- ESD hardened

APPLICATIONS

- Cellular radio FM IF
- High performance communications receivers
- Single conversion VHF/UHF receivers
- SCA receivers
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Wideband low current amplification

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Dual In-Line Package (DIP)	–40 to +85°C	SA615N	SOT146-1
20-Pin Plastic Small Outline Large (SOL) package	–40 to +85°C	SA615D	SOT108-1
20-Pin Plastic Shrink Small Outline Package (SSOP)	–40 to +85°C	SA615DK	SOT266-1

Low-voltage high performance mixer FM IF system SA616

DESCRIPTION

The SA616 is a low-voltage high performance monolithic FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, logarithmic received signal strength indicator (RSSI), voltage regulator and audio and RSSI op amps. The SA616 is available in 20-lead SSOP (shrink small outline package).

The SA616 was designed for portable communication applications and will function down to 2.7V. The RF section is similar to the famous SA615. The audio and RSSI outputs have amplifiers with access to the feedback path. This enables the designer to adjust the output levels or add filtering.

FEATURES

- Low power consumption: 3.5mA typical at 3V
- Mixer input to >150MHz
- Mixer conversion power gain of 17dB at 45MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator or external oscillator can be used at higher frequencies)
- 102dB of IF Amp/Limiter gain
- 2MHz IF amp/limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a 80dB dynamic range
- Low external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.31μV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone with RF at 45MHz and IF at 455kHz
- SA616 meets cellular radio specifications
- Audio output internal op amp
- RSSI output internal op amp
- Internal op amps with rail-to-rail outputs
- ESD protection: Human Body Model 2kV
  Robot Model 200V

PIN CONFIGURATION

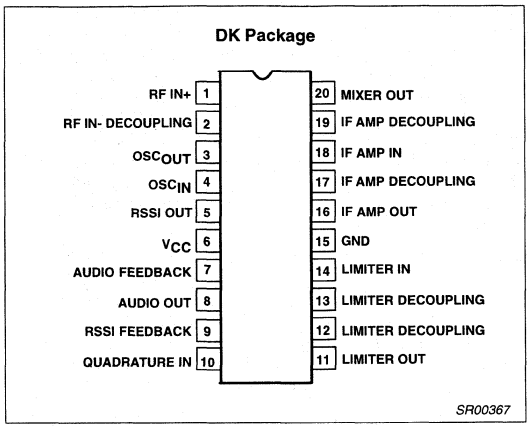


Figure 1. Pin Configuration

APPLICATIONS

- Portable cellular radio FM IF
- Cordless phones
- Wireless systems
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Portable high performance communication receiver
- Single conversion VHF receivers

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Shrink Small Outline Package (SSOP) (Surface-mount)	-40 to +85°C	SA616DK	SOT266-1

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	7	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range	-40 to +85	°C
θ_{JA}	Thermal impedance DK package	117	°C/W

BLOCK DIAGRAM

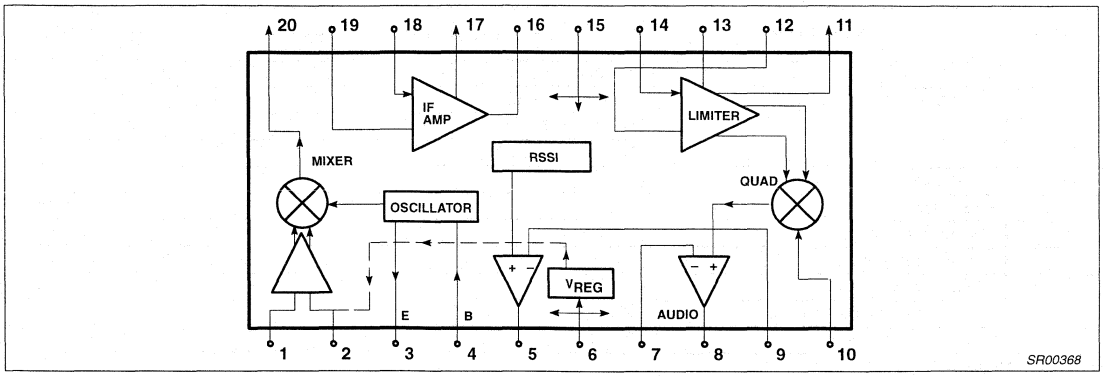


Figure 2. Block Diagram

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		2.7		7.0	V
I_{CC}	DC current drain			3.5	5.0	mA

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +3V, unless otherwise stated. RF frequency = 45MHz + 14.5dBV RF input step-up; IF frequency = 455kHz; R17 = 2.4kΩ and R18 = 3.3kΩ; RF level = -45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with de-emphasis filter and C-message weighted filter. Test circuit Figure 3. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Mixer/Osc section (ext LO = 220mV$_{RMS}$)						
f_{IN}	Input signal frequency			150		MHz
f_{OSC}	Crystal oscillator frequency			150		MHz
	Noise figure at 45MHz			6.8		dB
	Third-order input intercept point (50Ω source)	f1 = 45.0; f2 = 45.06MHz Input RF level = -52dBm		-9		dBm
	Conversion power gain	Matched 14.5dBV step-up	11	17		dB
		50Ω source		+2.5		dB
	RF input resistance	Single-ended input		8		kΩ
	RF input capacitance			3.0	4.0	pF
	Mixer output resistance	(Pin 20)	1.25	1.5		kΩ
IF section						
	IF amp gain	50Ω source		44		dB
	Limiter gain	50Ω source		58		dB
	Input limiting -3dB, R_{17a} = 2.4k, R_{17b} = 3.3k	Test at Pin 18		-105		dBm
	AM rejection	80% AM 1kHz		40		dB
	Audio level	Gain of two (2kΩ AC load)	60	120		mV
	SINAD sensitivity	IF level -110dBm		17		dB
THD	Total harmonic distortion		-30	-45		dB

AC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
S/N	Signal-to-noise ratio	No modulation for noise		62		dB
	RF RSSI output, R_g = 2kΩ	RF level = -118dBm		0.3	.80	V
		RF level = -68dBm	.70	1.1	2	V
		RF level = -23dBm	1.0	1.8	2.50	V
	RSSI range			80		dB
	RSSI accuracy			±2		dB
	IF input impedance	Pin 18	1.3	1.5		kΩ
	IF output impedance	Pin 16		0.3		kΩ
	Limiter input impedance	Pin 14	1.3	1.5		kΩ
	Limiter output impedance	Pin 11		0.3		kΩ
	Limiter output voltage	Pin 11		130		mV_{RMS}
RF/IF section (int LO)						
	Audio level	3V = V_{CC}, RF level = -27dBm		120		mV_{RMS}
	System RSSI output	3V = V_{CC}, RF level = -27dBm		2.2		V
	System SINAD sensitivity	RF level = -117dBm		12		dB

CIRCUIT DESCRIPTION

The SA616 is an IF signal processing system suitable for second IF systems with input frequency as high as 150MHz. The bandwidth of the IF amplifier and limiter is at least 2MHz with 90dB of gain. The gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 6.2dB, conversion gain of 17dB, and input third-order intercept of -9dBm. The oscillator will operate in excess of 200MHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

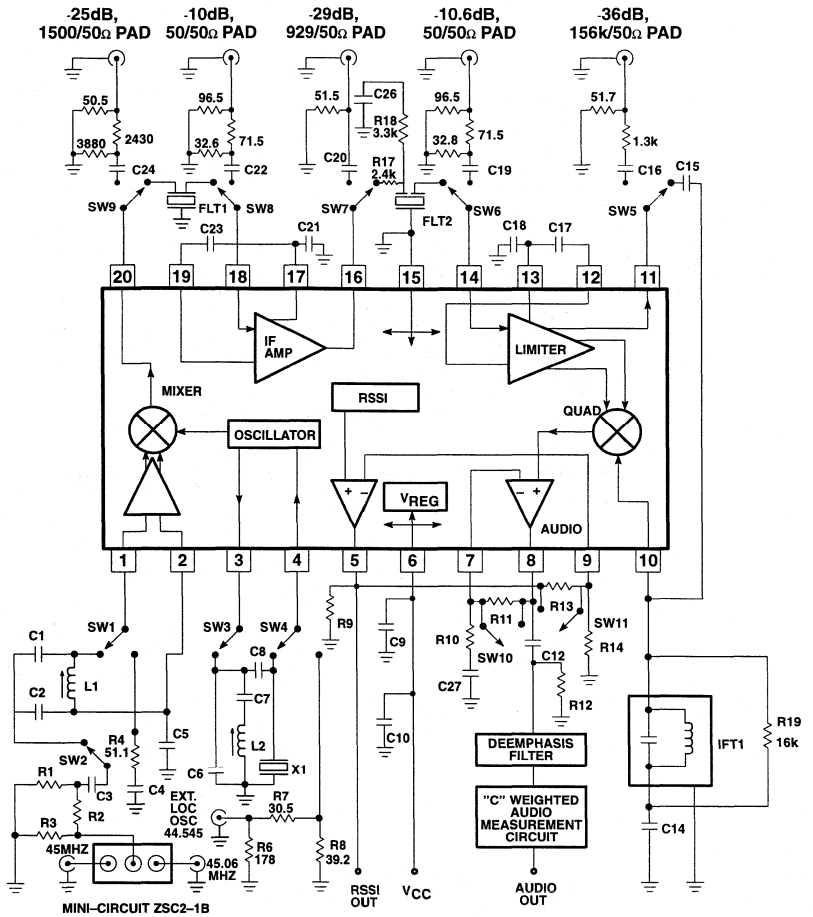
The output impedance of the mixer is a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. The IF amplifier has 43dB of gain and 5.5MHz bandwidth. The IF limiter has 60dB of gain and 4.5MHz bandwidth. To achieve optimum linearity of the log signal strength indicator, there must be a 12dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dB(v) insertion loss, a fixed or variable resistor or an L pad for simultaneous loss and impedance matching can be added between the first IF output (Pin 16) and the interstage network. The overall gain will then be 90dB with 2MHz bandwidth.

The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

The demodulated output of the quadrature drives an internal op amp. This op amp can be configured as a unity gain buffer, or for simultaneous gain, filtering, and 2nd-order temperature compensation if needed. It can drive an AC load as low as 5kΩ with a rail-to-rail output.

A log signal strength completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone. This signal drives an internal op amp. The op amp is capable of rail-to-rail output. It can be used for gain, filtering, or 2nd-order temperature compensation of the RSSI, if needed.

NOTE: $dB(v) = 20\log V_{OUT}/V_{IN}$

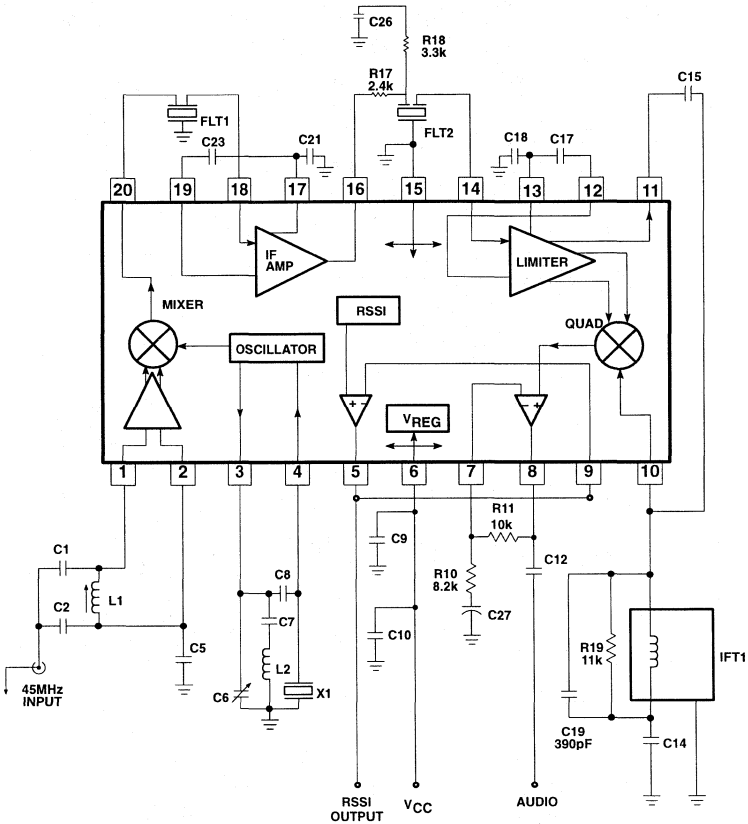


Automatic Test Circuit Component List

C1	100pF NPO Ceramic	C27	100nF ±10% Monolithic Ceramic
C2	390pF NPO Ceramic	Flt 1	Ceramic Filter Murata SFG455A3 or equiv
C5	100nF ±10% Monolithic Ceramic	Flt 2	Ceramic Filter Murata SFG455A3 or equiv
C6	22pF NPO Ceramic	IFT 1	455kHz (Ce = 180pF) Toko RMC–2A6597H
C7	1nF Ceramic	L1	147–160nH Coilcraft UNI–10/142–04J08S
C8	10.0pF NPO Ceramic	L2	0.8μH nominal
C9	100nF ±10% Monolithic Ceramic		Toko 292CNS–T1038Z
C10	15μF Tantalum (minimum)	X1	44.545MHz Crystal ICM4712701
C12	2.2μF	R9	2kΩ ±1% 1/4W Metal Film
C14	100nF ±10% Monolithic Ceramic	R10	8.2kΩ ±1%
C15	10pF NPO Ceramic	R11	10kΩ ±1%
C17	100nF ±10% Monolithic Ceramic	R12	2kΩ ±1%
C18	100nF ±10% Monolithic Ceramic	R13	20kΩ ±1%
C21	100nF ±10% Monolithic Ceramic	R14	10kΩ ±1%
C23	100nF ±10% Monolithic Ceramic	R17	2.4kΩ ±5% 1/4W Carbon Composition
C25	100nF ±10% Monolithic Ceramic	R18	3.3kΩ
C26	100nF ±10% Monolithic Ceramic	R19	16kΩ

SR00369

Figure 3. SA616 45MHz Test Circuit (Relays as shown)



SA616 DK demoboard
Application Component List

C1	51pF NPO Ceramic
C2	220pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	30pF trim cap
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	15μF Tantalum (minimum)
C12	2.2μF ±10% Tantalum
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C19	390pF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C26	100nF ±10% Monolithic Ceramic
C27	2.2μF Tantalum
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	330μH TOKO 303LN-1130
L1	.33μH TOKO SCB-1320Z
L2	1.2μH
X1	44.545MHz Crystal ICM4712701
R5	Not Used in Application Board (see Note 8, pg 8)
R10	8.2k ±5% 1/4W Carbon Composition
R11	10k ±5% 1/4W Carbon Composition
R17	2.4k ±5% 1/4W Carbon Composition
R18	3.3k ±5% 1/4W Carbon Composition
R19	11k ±5% 1/4W Carbon Composition

SR00370

Figure 4. SA616 45MHz Application Circuit

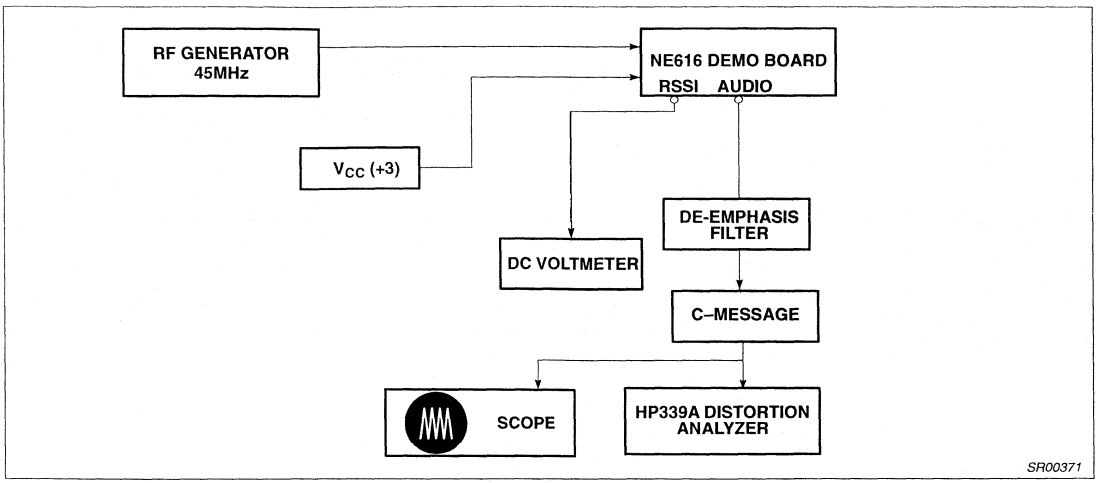


Figure 5. SA616 Application Circuit Test Set Up

NOTES:

1. C-message: The C-message and de-emphasis filter combination has a peak gain of 10 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339 analyzer. The de-emphasis filter has a fixed -6dB/Octave slope between 300Hz and 3kHz.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All of our specifications and testing are done with the more wideband filter.
3. RF generator: Set your RF generator at 45.000MHz, use a 1kHz modulation frequency and a 6kHz deviation if you use 16kHz filters, or 8kHz if you use 30kHz filters.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.35µV or -116dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 500mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10-15µF or higher value tantalum capacitor on the supply line is essential. A low frequency ESR screening test on this capacitor will ensure consistent good sensitivity in production. A 0.1µF bypass capacitor on the supply pin, and grounded near the 44.545MHz oscillator improves sensitivity by 2-3dB.
8. R5 can be used to bias the oscillator transistor at a higher current for operation above 45MHz. Recommended value is 22kΩ, but should not be below 10kΩ.

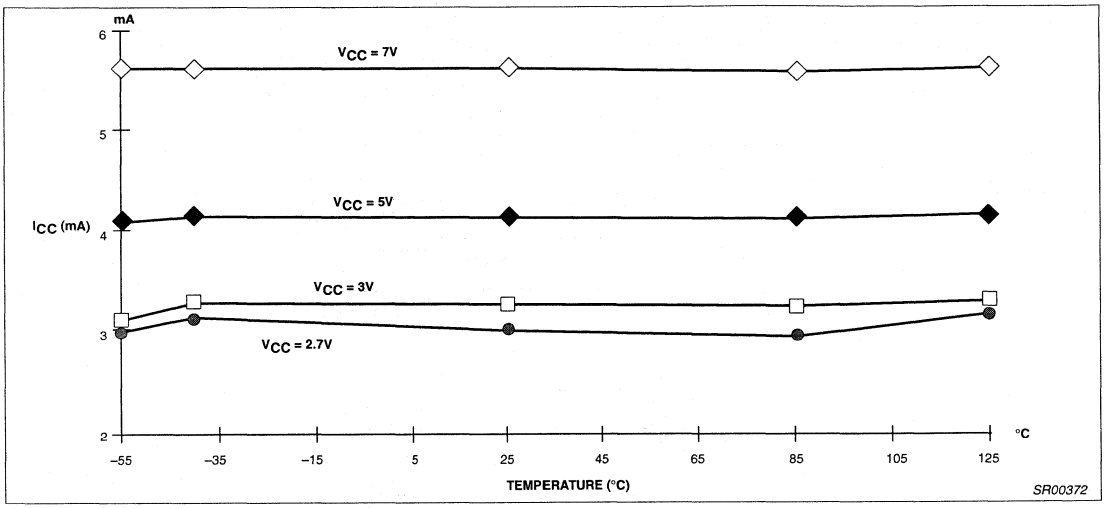


Figure 6. I_{CC} vs Temperature

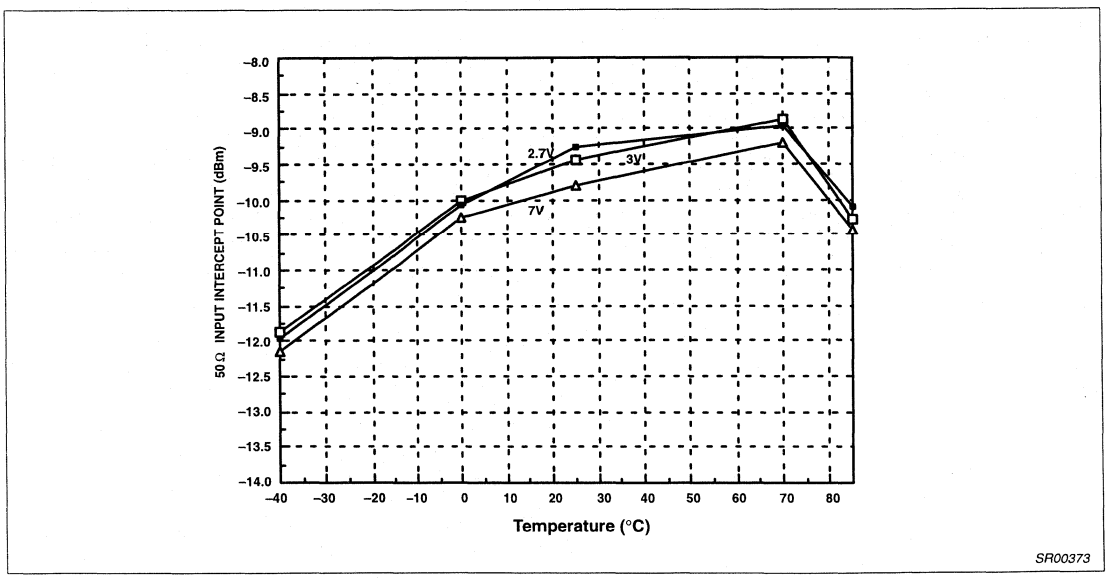


Figure 7. Third Order Intercept Point vs Supply Voltage

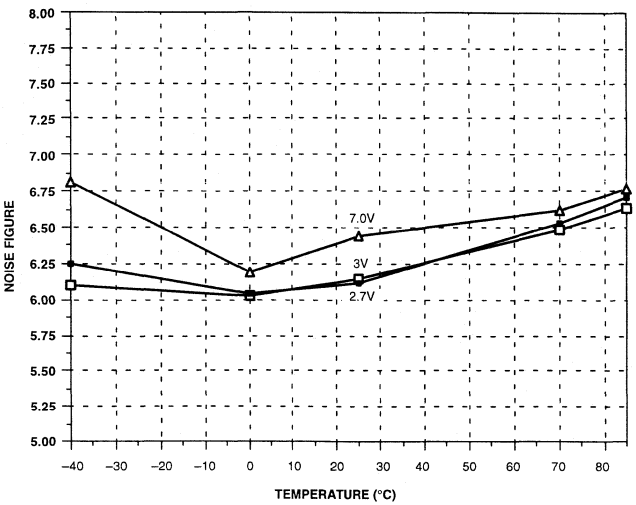


Figure 8. Mixer Noise Figure vs Supply Voltage

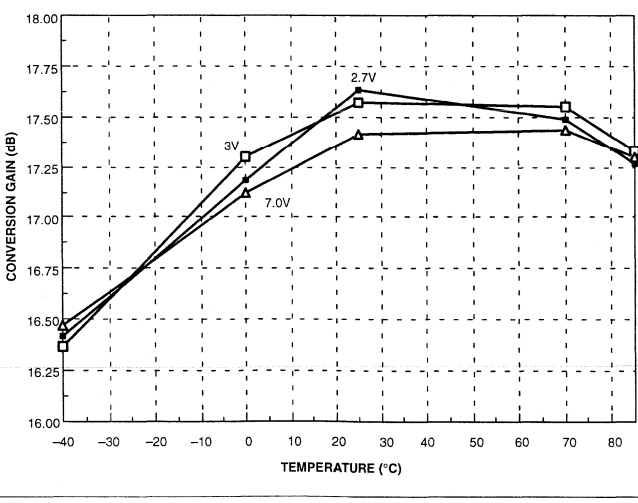


Figure 9. Conversion Gain vs Supply Voltage

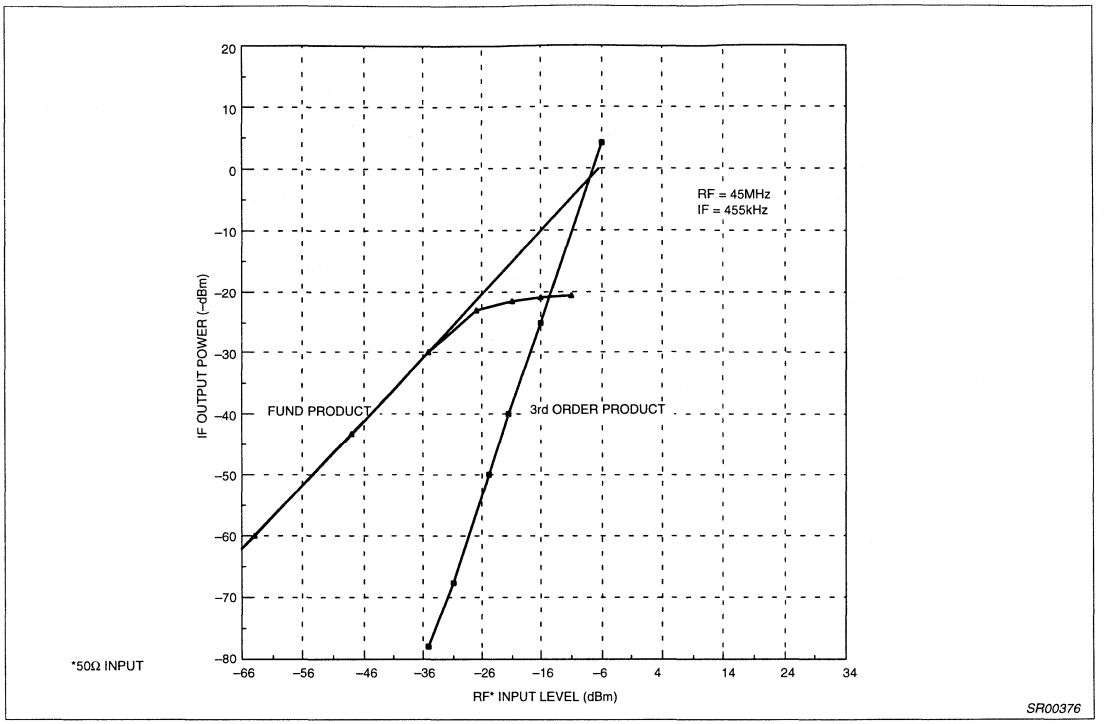


Figure 10. Mixer Third Order Intercept and Compression

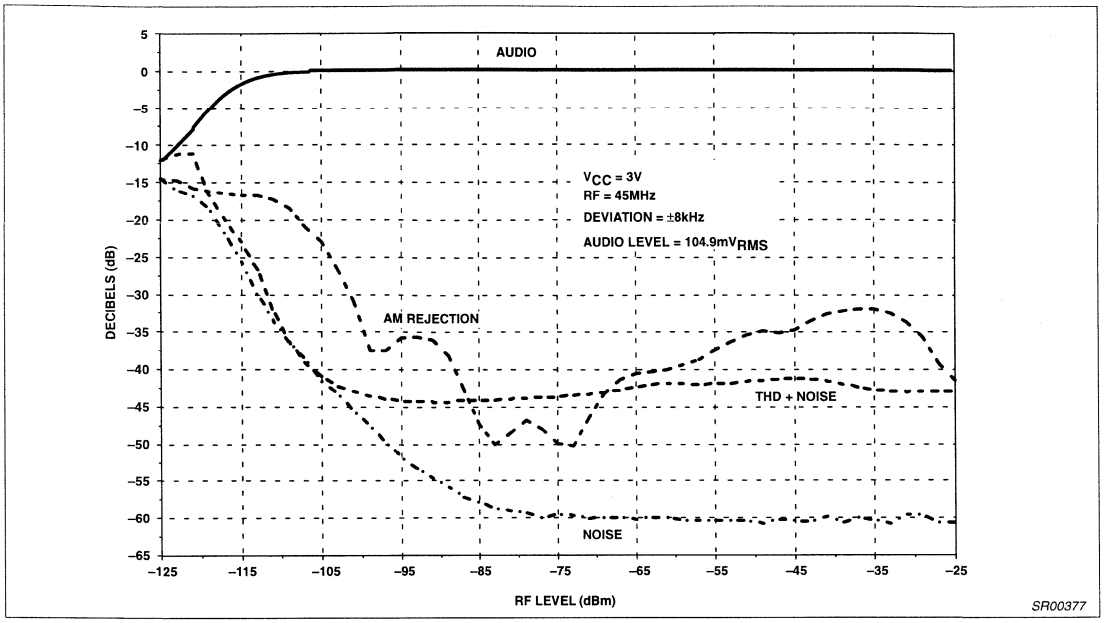


Figure 11. Sensitivity vs RF Level (-40°C)

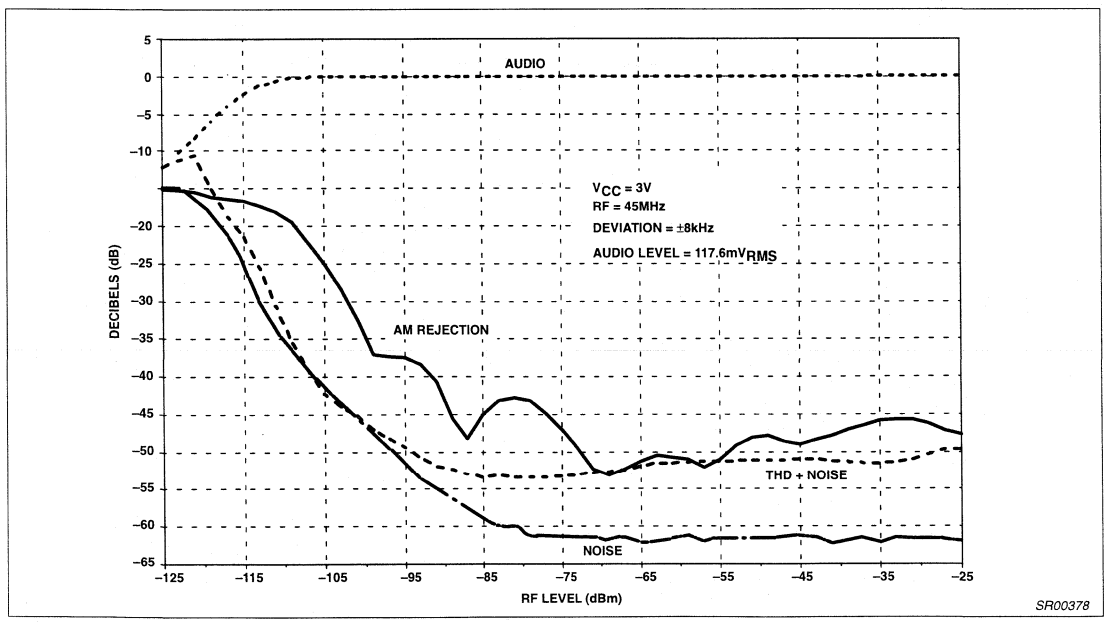


Figure 12. Sensitivity vs RF Level (+25°C)

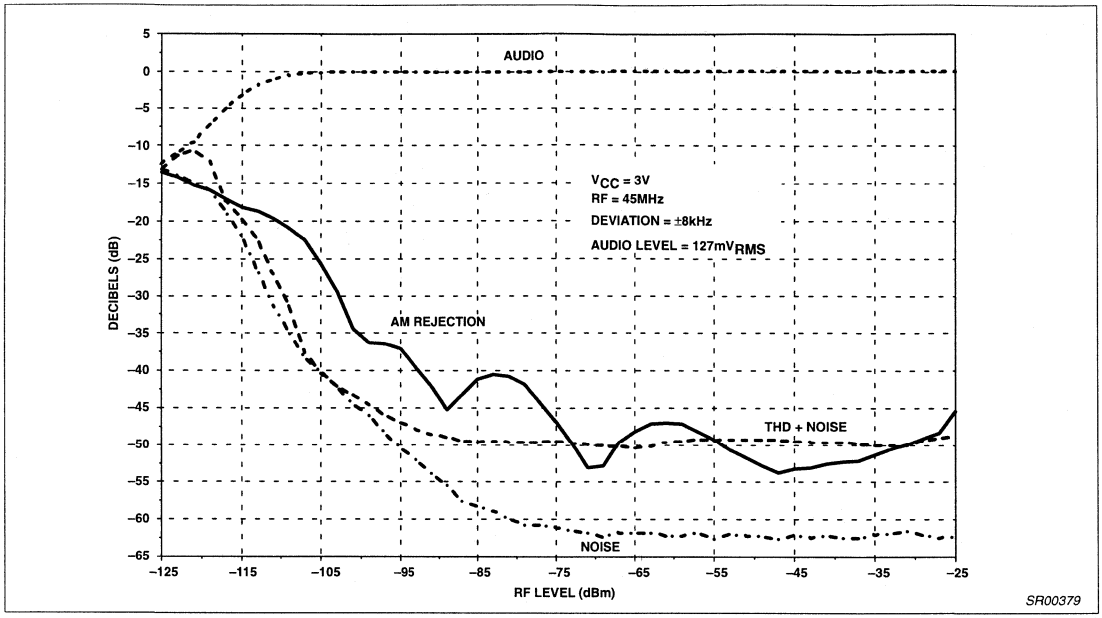


Figure 13. Sensitivity vs RF Level (Temperature 85°C)

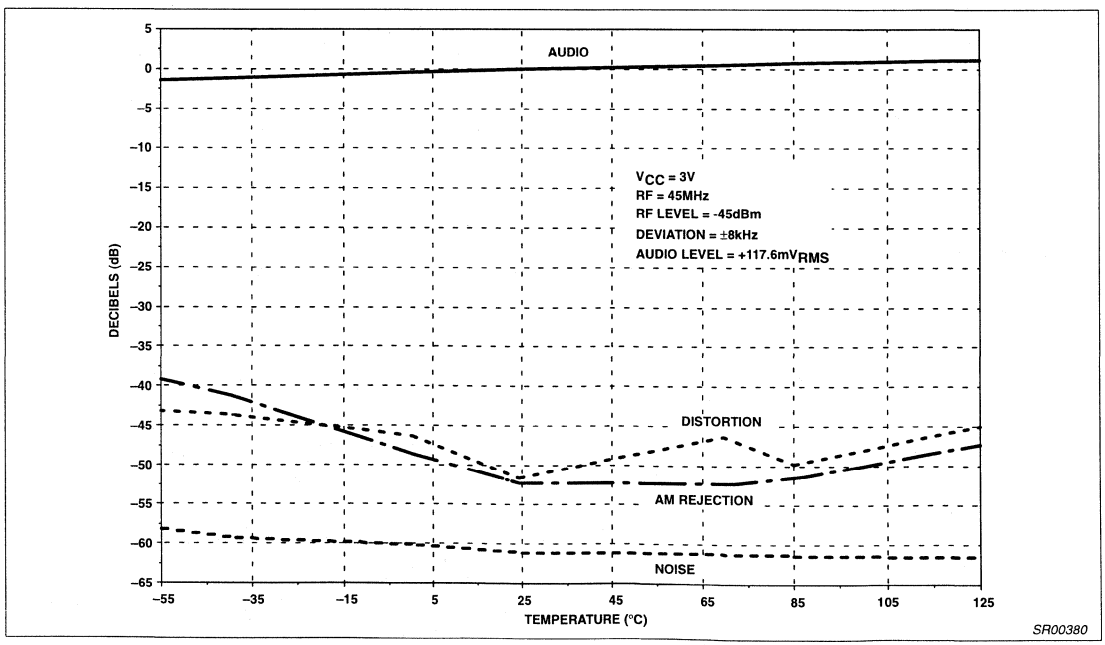


Figure 14. Relative Audio Level, Distortion, AM Rejection and Noise vs Temperature

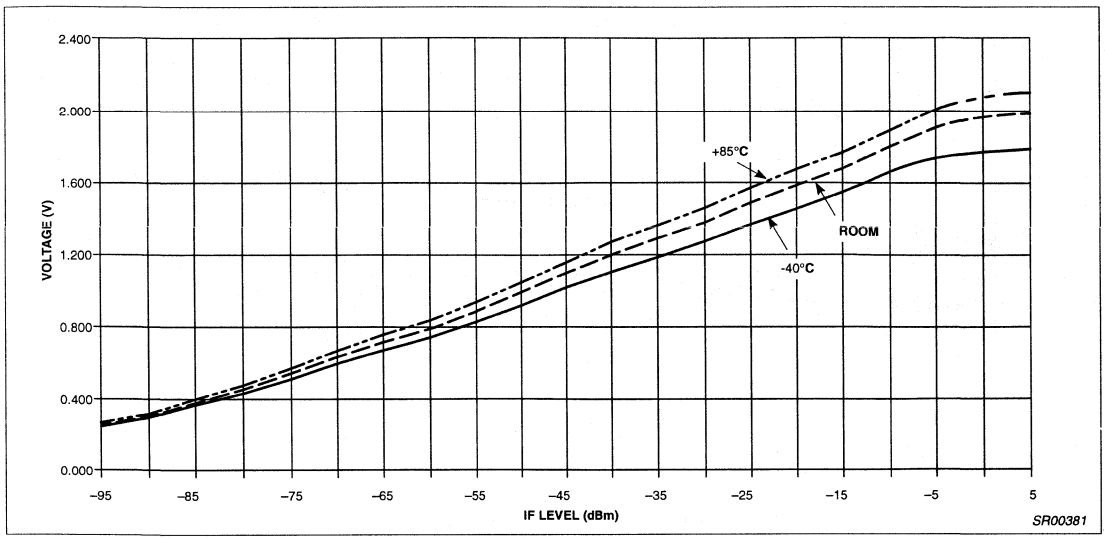


Figure 15. RSSI (455kHz IF @ 3V)

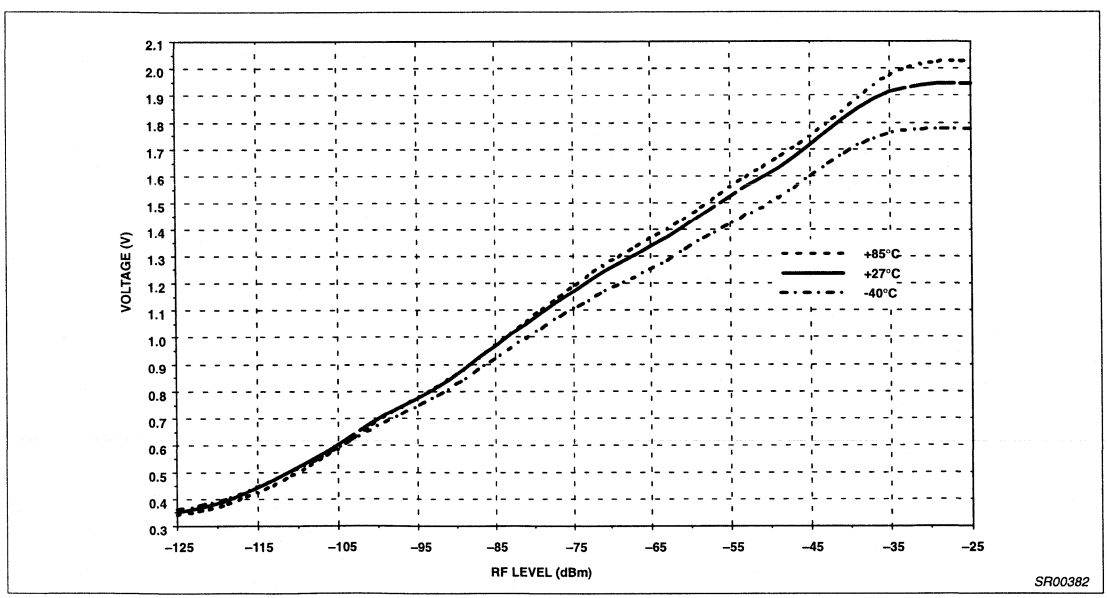


Figure 16. RSSI vs RF Level and Temperature - V_{CC} = 3V

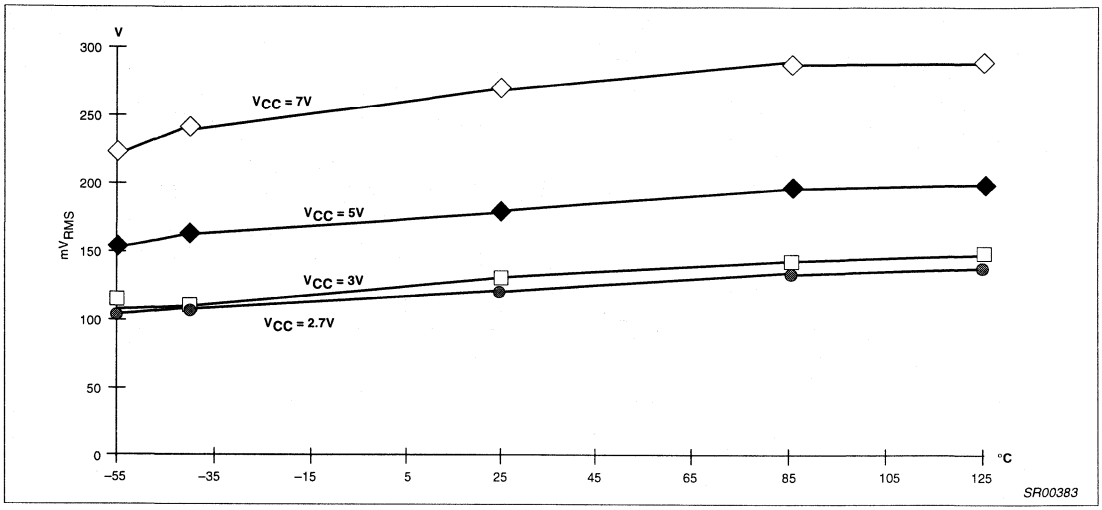
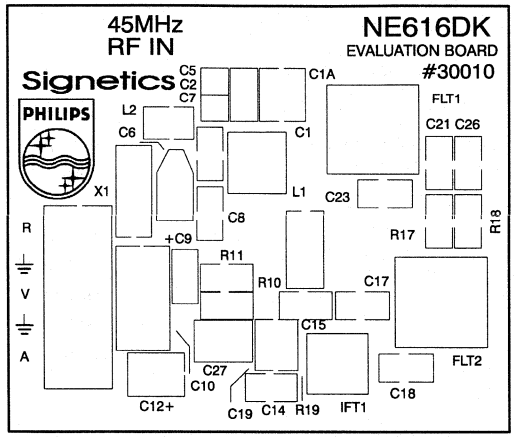
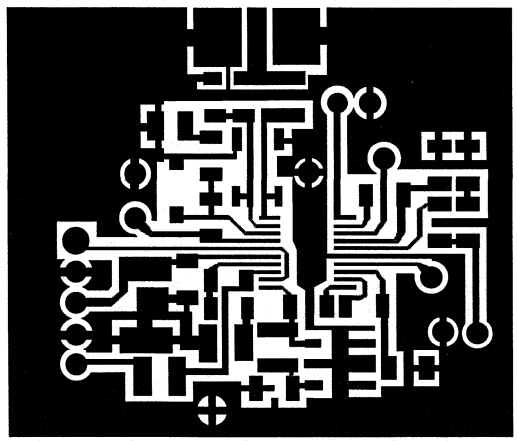


Figure 17. Audio Output vs Temperature

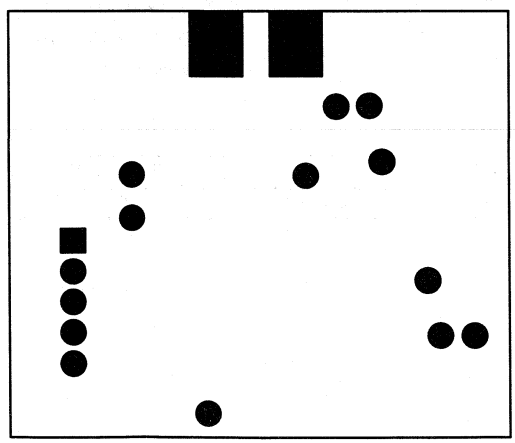
616 Silk Screen



616 TOP



616 BOTTOM



NOTE;
All views are TOP VIEW and not actual size. For reference only.

SR00386

Figure 18.

Low-voltage high performance mixer FM IF system SA617

DESCRIPTION

The SA617 is a low voltage high performance monolithic FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, logarithmic received signal strength indicator (RSSI), voltage regulator and audio and RSSI op amps. The SA617 is available in 20-lead SSOP package.

The SA617 was designed for portable communication applications and will function down to 2.7V. The RF section is similar to the famous SA605. The audio output has an internal amplifier with the feedback pin accessible. The RSSI output is buffered. The SA617 also has an extra limiter output. This signal is buffered from the output of the limiter and can be used to perform frequency check. This is accomplished by comparing a reference frequency with the frequency check signal using a comparator to a varactor or PLL at the oscillator inputs.

FEATURES

- Low power consumption: 3.5mA typical at 3V
- Mixer input to >150MHz
- Mixer conversion power gain of 17dB at 45MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator or external oscillator can be used at higher frequencies)
- 102dB of IF Amp/Limiter gain
- 2MHz IF amp/limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a 80dB dynamic range
- Low external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.31μV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone, 8kHz deviation with RF at 45MHz and IF at 455kHz
- SA617 meets cellular radio specifications
- Audio output internal op amp
- RSSI output internal op amp
- Buffered frequency check output

PIN CONFIGURATION

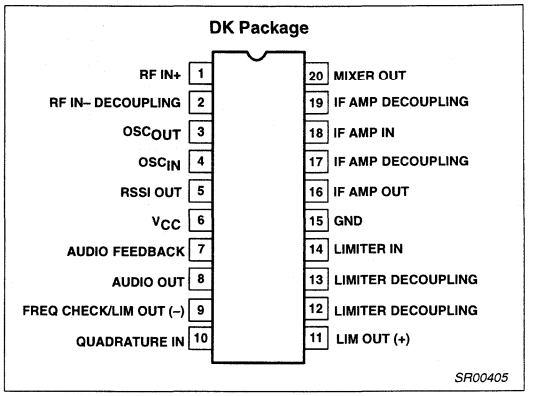


Figure 1. Pin Configuration

- Internal op amps with rail-to-rail outputs
- ESD protection: Human Body Model 2kV
  Robot Model 200V

APPLICATIONS

- Portable cellular radio FM IF
- Cordless phones
- Narrow band cellular applications (NAMPS/NTACS)
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Portable high performance communication receivers
- Single conversion VHF receivers
- Wireless systems

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Shrink Small Outline Package (SSOP) (Surface-mount)	-40 to +85°C	SA617DK	SOT266-1

BLOCK DIAGRAM

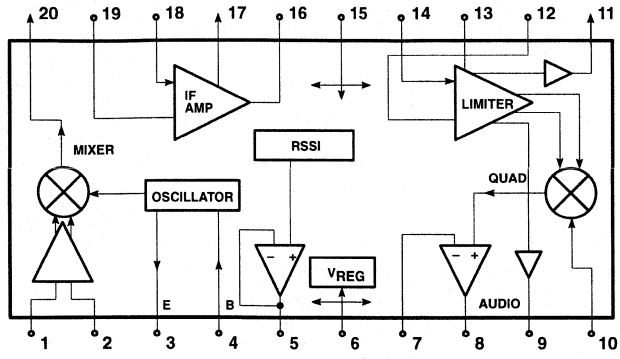


Figure 2. Block Diagram

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	7	V
T_{STG}	Storage temperature range	–65 to +150	°C
T_A	Operating ambient temperature range SA617	–40 to +85	°C
θ_{JA}	Thermal impedance DK package	117	°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA617			
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		2.7		7.0	V
I_{CC}	DC current drain			3.5	5.0	mA

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +3V, unless otherwise stated. RF frequency = 45MHz + 14.5dBV RF input step-up; IF frequency = 455kHz; R17 = 2.4k; R18 = 3.3k; RF level = –45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with de-emphasis filter and C-message weighted filter. Test circuit NO TAG. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS SA617 MIN	LIMITS SA617 TYP	LIMITS SA617 MAX	UNITS
Mixer/Osc section (ext LO = 220mV$_{RMS}$)						
f_{IN}	Input signal frequency			150		MHz
f_{OSC}	Crystal oscillator frequency			150		MHz
	Noise figure at 45MHz			6.8		dB
	Third–order input intercept point (50Ω source)	f1 = 45.0; f2 = 45.06MHz Input RF Level = –52dBm		–9		dBm
	Conversion power gain	Matched 14.5dBV step–up	11.0	17		dB
		50Ω source		+2.5		dB
	RF input resistance	Single–ended input		8		kΩ
	RF input capacitance			3.0	4.0	pF
	Mixer output resistance	(Pin 20)	1.25	1.5		kΩ
IF section						
	IF amp gain	50Ω source		44		dB
	Limiter gain	50Ω source		58		dB
	Input limiting –3dB, R_{17} = 2.4k	Test at Pin 18		–105		dBm
	AM rejection	80% AM 1kHz		40		dB
	Audio level	Gain of two (2kΩ AC load)	60	114		mV
	SINAD sensitivity	RF level –110dB		13		dB
THD	Total harmonic distortion		–30	–45		dB
S/N	Signal–to–noise ratio	No modulation for noise		62		dB
	IF RSSI output, R_9 = 2kΩ[1]	IF level = –118dBm		0.3	0.8	V
		IF level = –68dBm	.70	1.1	2.0	V
		IF level = –23dBm	1.0	1.8	2.5	V
	RSSI range			80		dB
	RSSI accuracy			±2.0		dB
	IF input impedance		1.3	1.5		kΩ
	IF output impedance			0.3		kΩ
	Limiter input impedance		1.30	1.5		kΩ
	Limiter output impedance	(Pin 11)		200		Ω
	Limiter output level	(Pin 11) No load 2.4kΩ load		130 115		mV$_{RMS}$
	Frequency Check/limiter output impedance	(Pin 9)		200		Ω
	Frequency Check/limiter output level	(Pin 9) No load 2.4kΩ load		130 115		mV$_{RMS}$
RF/IF section (int LO)						
	Audio level	3V = V_{CC}, RF level = –27dBm		240		mV$_{RMS}$
	System RSSI output	3V = V_{CC}, RF level = –27dBm		2.2		V
	System SINAD sensitivity	RF level = –117dBm		12		dB

NOTE:

1. The generator source impedance is 50Ω, but the SA617 input impedance at Pin 18 is 1500Ω. As a result, IF level refers to the actual signal that enters the SA617 input (Pin 18) which is about 21dB less than the "available power" at the generator.

CIRCUIT DESCRIPTION

The SA617 is an IF signal processing system suitable for second IF systems with input frequency as high as 150MHz. The bandwidth of the IF amplifier and limiter is at least 2MHz with 90dB of gain. The gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 6.2dB, conversion gain of 17dB, and input third-order intercept of –9dBm. The oscillator will operate in excess of 200MHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

The output impedance of the mixer is a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. The IF amplifier has 43dB of gain and 5.5MHz bandwidth. The IF limiter has 60dB of gain and 4.5MHz bandwidth. To achieve optimum linearity of the log signal strength indicator, there must be a 12dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dB(v) insertion loss, a fixed or variable resistor or an L pad for simultaneous loss and impedance matching can be added between the first IF output (Pin 16) and the interstage network. The overall gain will then be 90dB with 2MHz bandwidth.

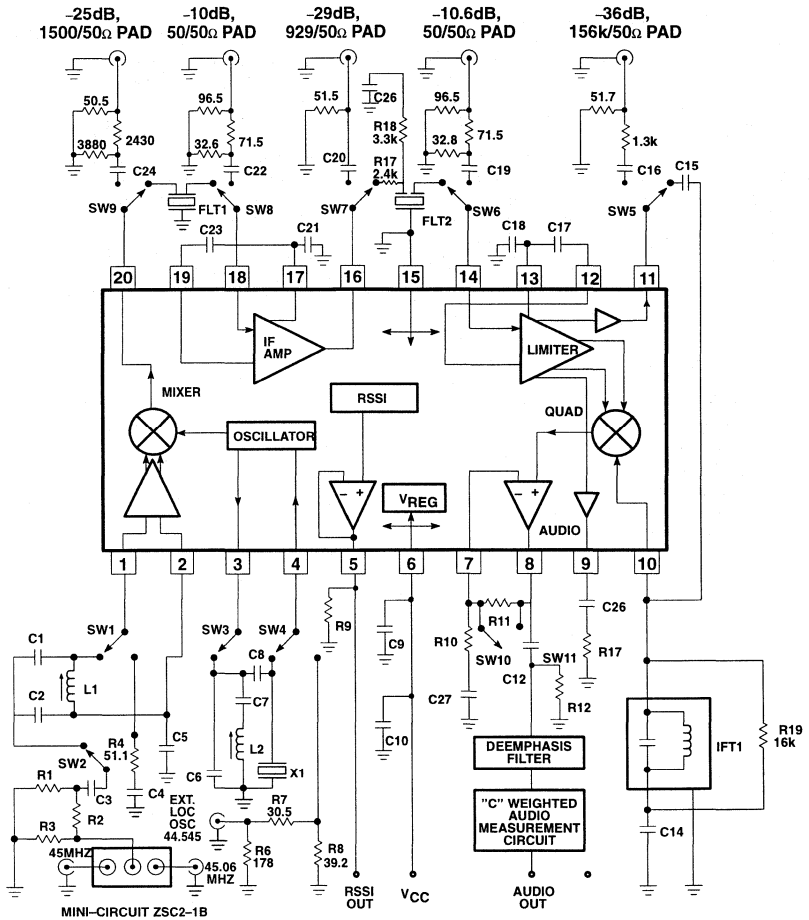
The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

The demodulated output of the quadrature drives an internal op amp. This op amp can be configured as a unity gain buffer, or for simultaneous gain, filtering, and 2nd-order temperature compensation if needed. It can drive an AC load as low as 2kΩ with a rail-to-rail output.

A log signal strength completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone. This signal is buffered through an internal unity gain op amp. The frequency check pin provides a buffered limiter output. This is useful for implementing an AFC (Automatic Frequency Check) function. This same output can also be used in conjunction with limiter output (Pin 11) for demodulating FSK (Frequency Shift Keying) data. Both pins are of the same amplitude, but 180° out of phase.

NOTE: Limiter output or Frequency Check output has drive capability of a load minimum of 2kΩ or higher to obtain 115mV output level.

NOTE: $dB(v) = 20\log V_{OUT}/V_{IN}$

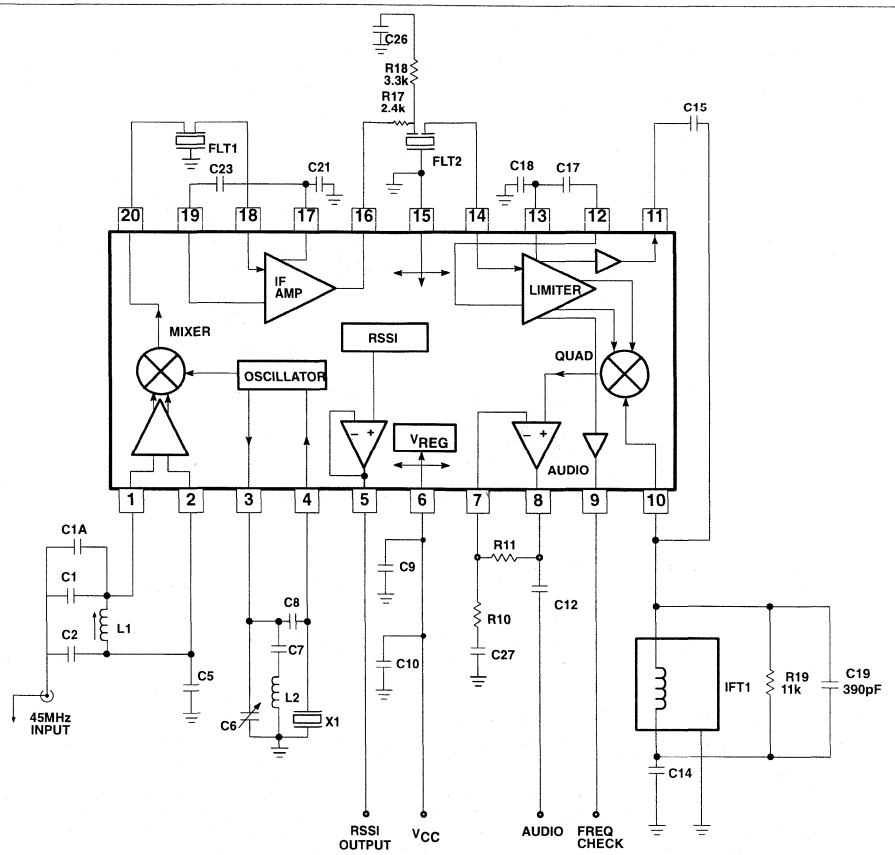


Automatic Test Circuit Component List

C1	100pF NPO Ceramic
C2	390pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	15μF Tantalum (minimum)
C12	2.2μF
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
C26	0.1μF ±10% Monolithic Ceramic
C27	2.2μF
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	455kHz (Ce = 180pF) Toko RMC–2A6597H
L1	147–160nH Coilcraft UNI–10/142–04J08S
L2	3.3μH nominal Toko 292CNS–T1046Z
X1	44.545MHz Crystal ICM4712701
R9	2kΩ ±1% 1/4W Metal Film
R10	8.2kΩ ±1%
R11	10kΩ ±1%
R12	2kΩ ±1%
R14	10kΩ ±1%
R17	2.4kΩ ±5% 1/4W Carbon Composition
R18	3.3kΩ ±5% 1/4W Carbon Composition
R19	16kΩ ±5% 1/4W Carbon Composition

SR00407

Figure 3. SA617 45MHz Test Circuit (Relays as shown)



SA617DK
Application Component List

C1A	18pF NPO Ceramic
C1	33pF NPO Ceramic
C2	220pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	30pF trim cap
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	15µF Tantalum (minimum)
C12	2.2µF ±10% Tantalum
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C19	390pF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C26	100nF ±10% Monolithic Ceramic
C27	2.2µF Tantalum
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	330µH TOKO 303LN-1130
L1	.33µH TOKO SCB-1320Z
L2	1.2µH
X1	44.545MHz Crystal ICM4712701
R5	Not Used in Application Board (see Note 8, pg 8)
R10	8.2k ±5% 1/4W Carbon Composition
R11	10k ±5% 1/4W Carbon Composition
R17	2.4k ±5% 1/4W Carbon Composition
R18	3.3k ±5% 1/4W Carbon Composition
R19	11k ±5% 1/4W Carbon Composition

SR00408

Figure 4. SA617 45MHz Application Circuit

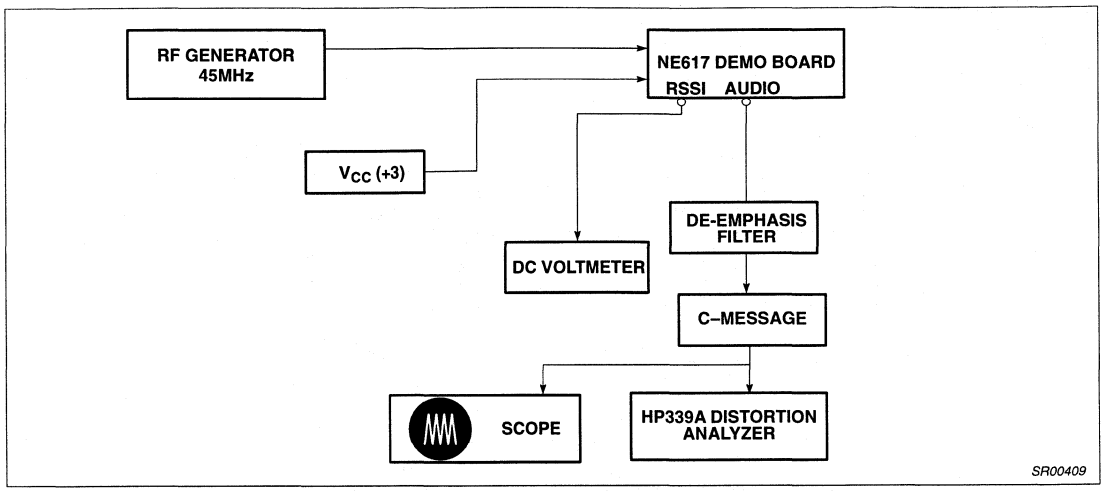


Figure 5. SA617 Application Circuit Test Set Up

NOTES:

1. C-message: The C-message and de-emphasis filter combination has a peak gain of 10 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339 analyzer. The de-emphasis filter has a fixed -6dB/Octave slope between 300Hz and 3kHz.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All of our specifications and testing are done with the more wideband filter.
3. RF generator: Set your RF generator at 45.000MHz, use a 1kHz modulation frequency and a 6kHz deviation if you use 16kHz filters, or 8kHz if you use 30kHz filters.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.35μV or –116dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 500mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10-15μF or higher value tantalum capacitor on the supply line is essential. A low frequency ESR screening test on this capacitor will ensure consistent good sensitivity in production. A 0.1μF bypass capacitor on the supply pin, and grounded near the 44.545MHz oscillator improves sensitivity by 2-3dB.
8. R5 can be used to bias the oscillator transistor at a higher current for operation above 45MHz. Recommended value is 22kΩ, but should not be below 10kΩ.

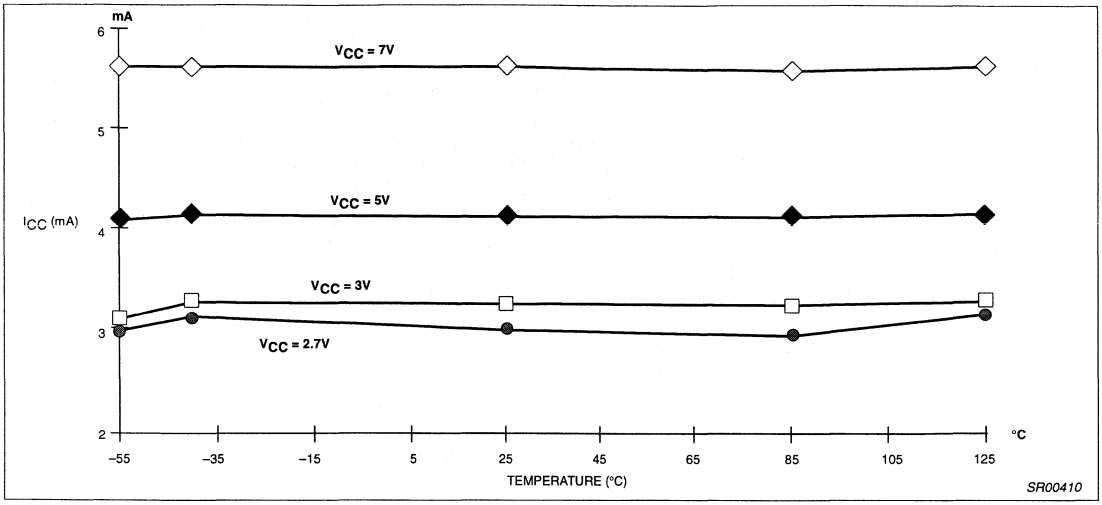


Figure 6. I_{CC} vs Temperature

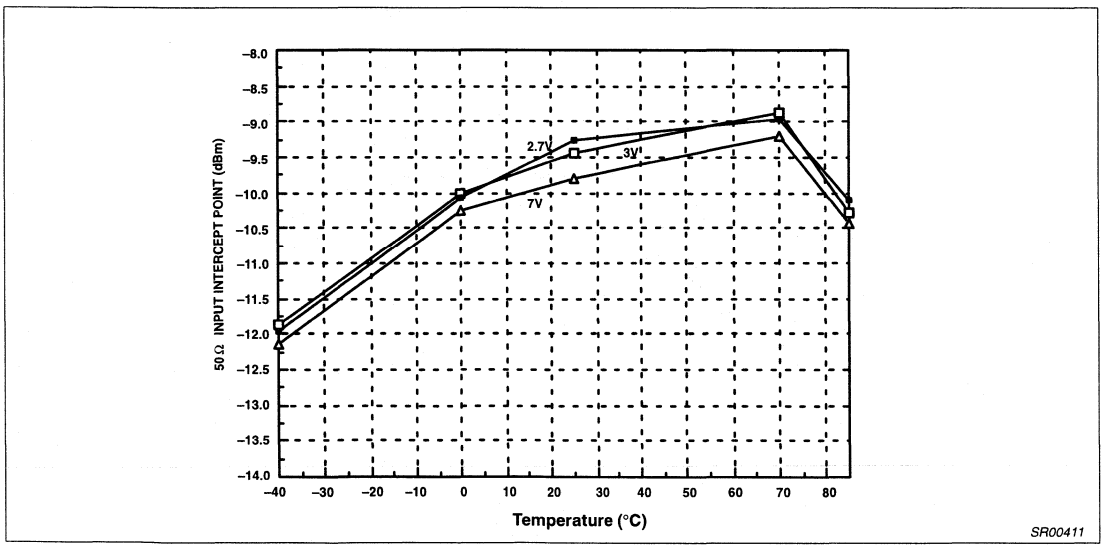


Figure 7. Third Order Intercept Point vs Supply Voltage

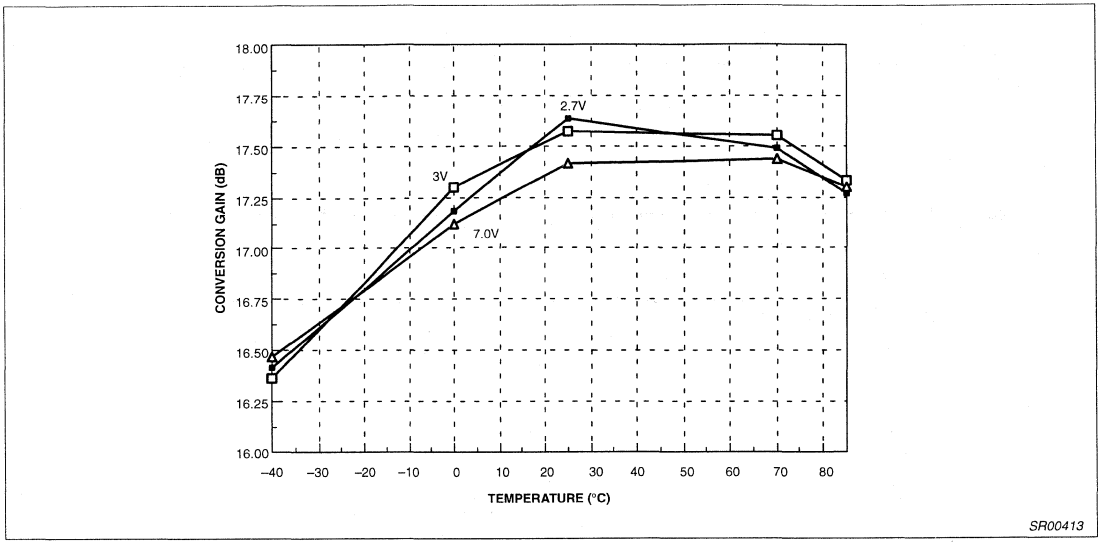


Figure 8. Mixer Noise Figure vs Supply Voltage

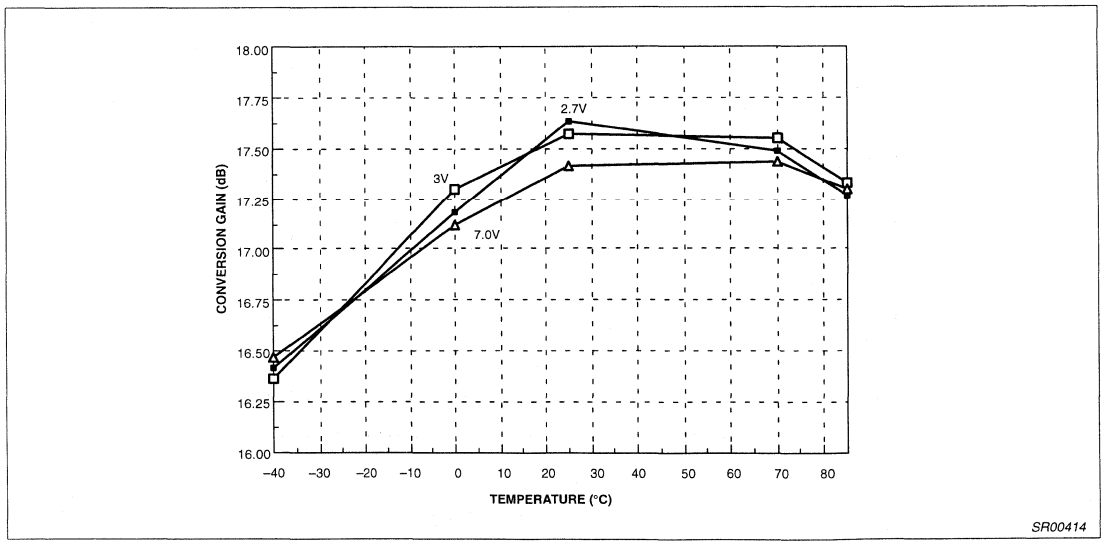


Figure 9. Conversion Gain vs Supply Voltage

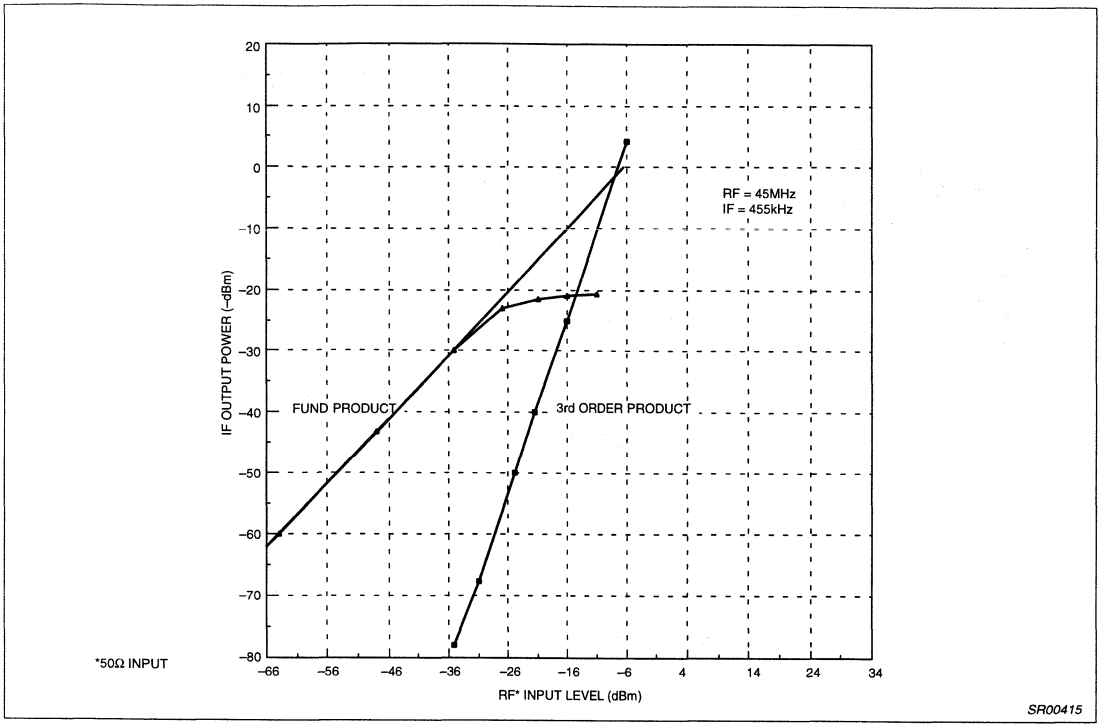


Figure 10. Mixer Third Order Intercept and Compression

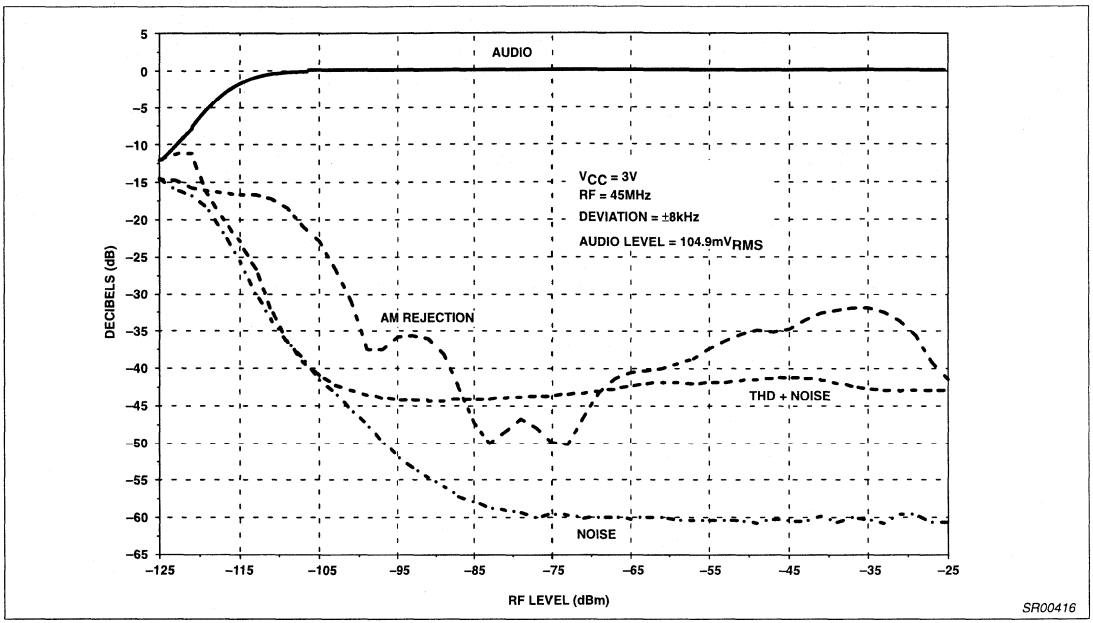


Figure 11. Sensitivity vs RF Level (–40°C)

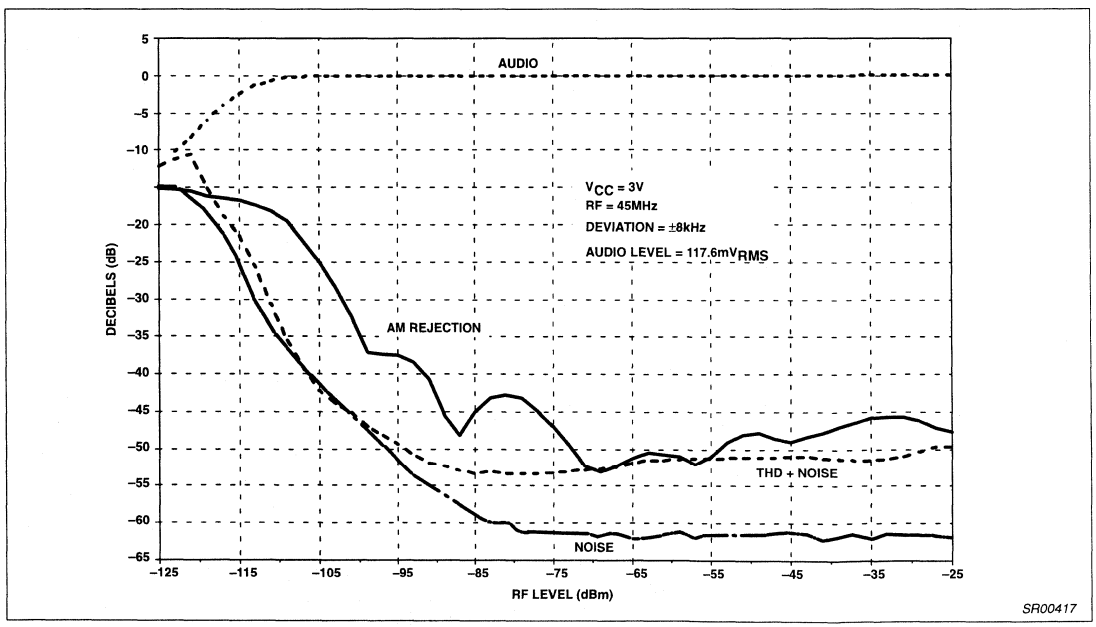


Figure 12. Sensitivity vs RF Level (+25°C)

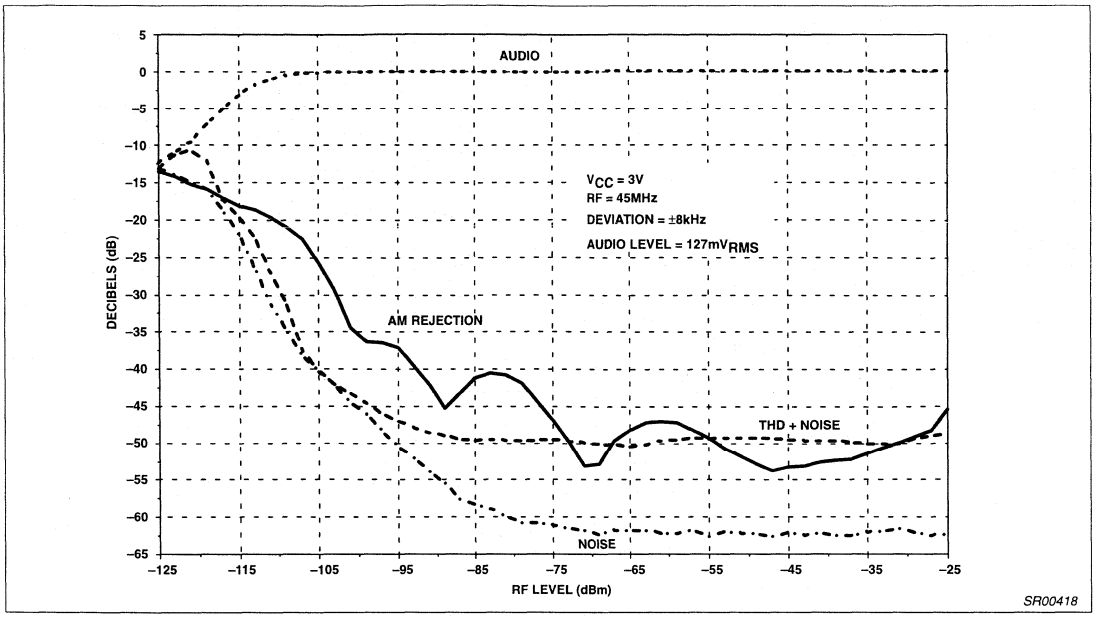


Figure 13. Sensitivity vs RF Level (Temperature 85°C)

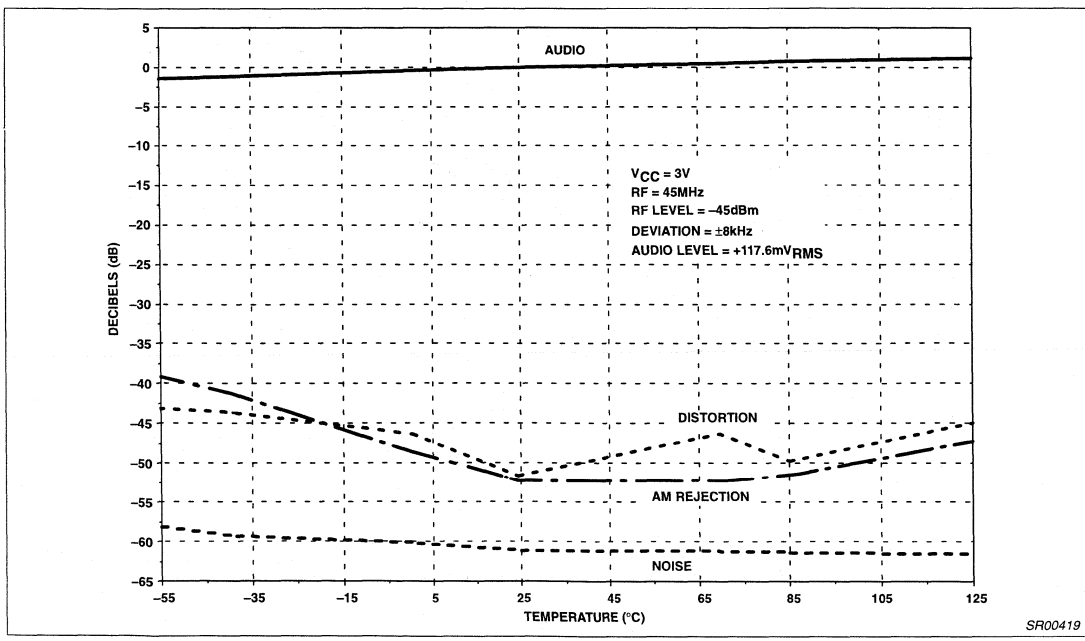


Figure 14. Relative Audio Level, Distortion, AM Rejection and Noise vs Temperature

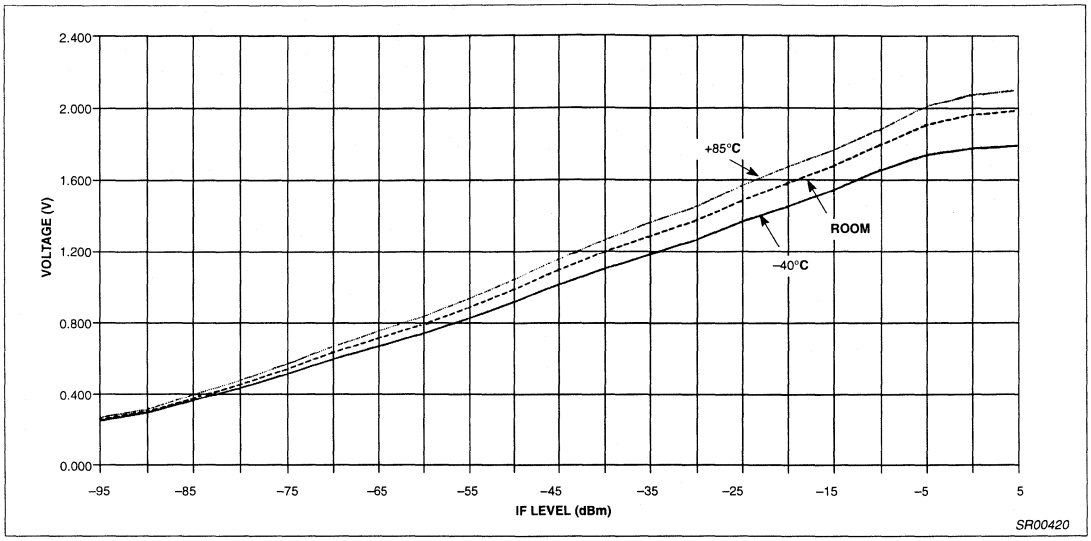


Figure 15. RSSI (455kHz IF @ 3V)

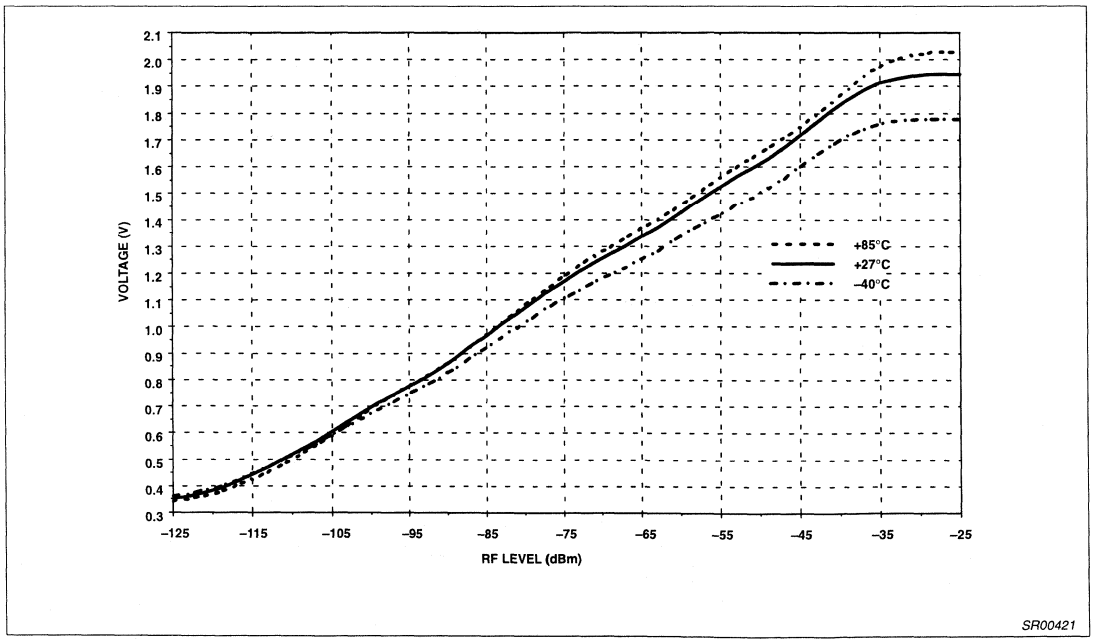


Figure 16. RSSI vs RF Level and Temperature - V_{CC} = 3V

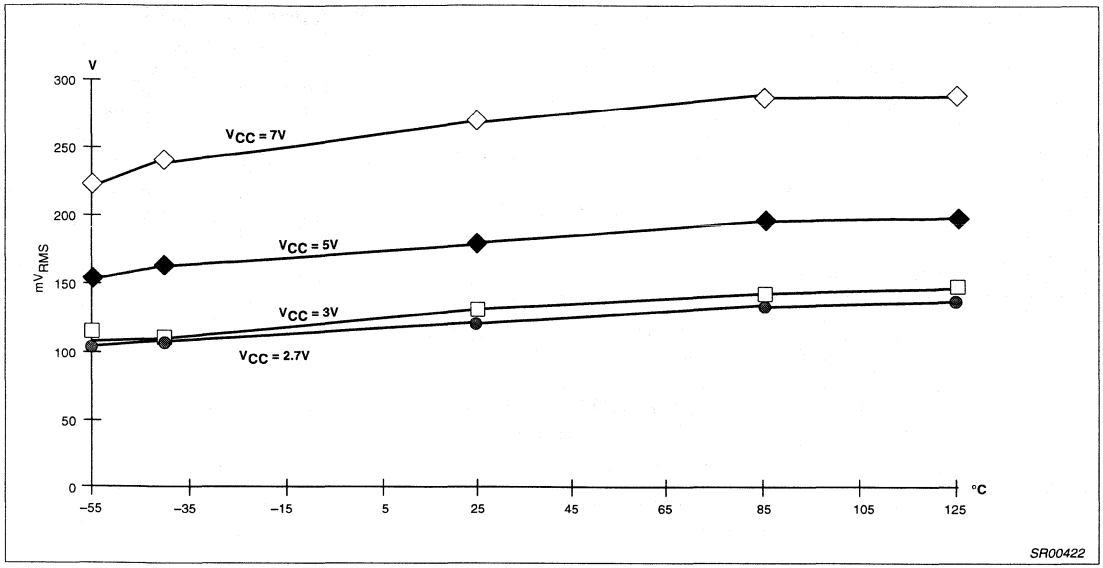


Figure 17. Audio Output vs Temperature

Low voltage LNA, mixer and VCO — 1GHz | SA620

DESCRIPTION

The SA620 is a combined RF amplifier, VCO with tracking bandpass filter and mixer designed for high-performance low-power communication systems from 800-1200MHz. The low-noise preamplifier has a 1.6dB noise figure at 900MHz with 11.5dB gain and an IP3 intercept of -3dBm at the input. The gain is stabilized by on-chip compensation to vary less than ±0.2dB over -40 to +85°C temperature range. The wide-dynamic-range mixer has an 9dB noise figure and IP3 of –6dBm at the input at 900MHz. An external LO can be used in place of the internal VCO for improved mixer input IP3 and a 3mA reduction in current. The chip incorporates a through-mode option so the RF amplifier can be disabled and replaced by an attenuator (S_{21} = –7.5dB). This is useful for improving the overall dynamic range of the receiver when in an overload situation. The nominal current drawn from a single 3V supply is 10.4mA and 7.2mA in the thru-mode. Additionally, the VCO and Mixer can be powered down to further reduce the supply current to 1.2mA.

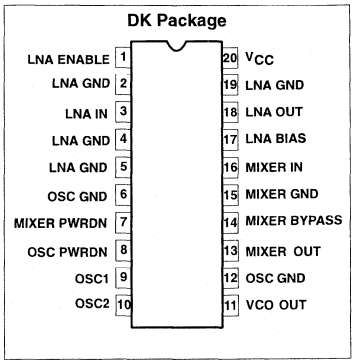
FEATURES

- Low current consumption: 10.4mA nominal, 7.2mA with thru-mode activated
- Outstanding noise figure: 1.6dB for the amplifier and 9dB for the mixer at 900MHz
- Excellent gain stability versus temperature and supply voltage
- Switchable overload capability
- Independent LNA, mixer and VCO power down capability
- Internal VCO automatic leveling loop
- Monotonic VCO frequency vs control voltage

APPLICATIONS

- 900MHz cellular front-end
- 900MHz cordless front-end
- Spread spectrum receivers
- RF data links
- UHF frequency conversion
- Portable radio

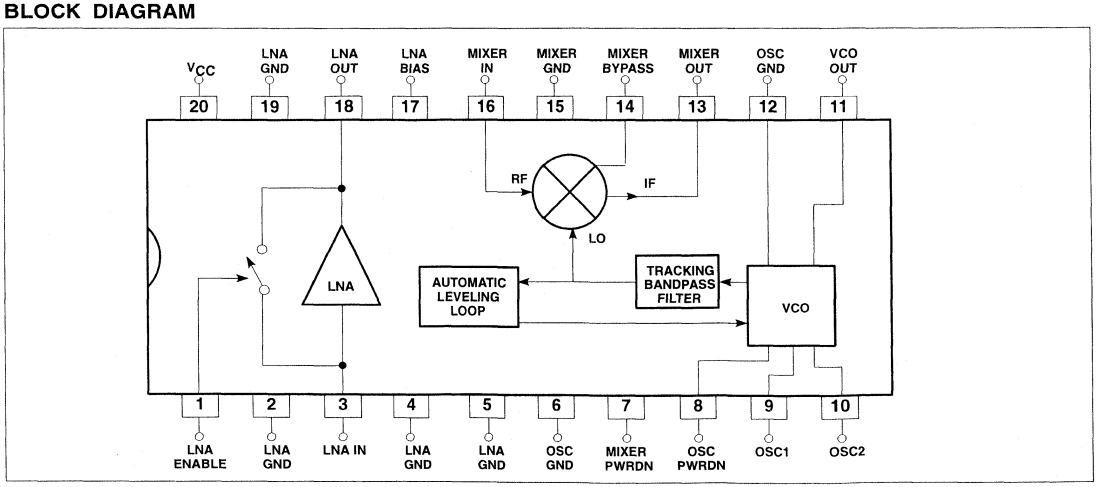
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Shrink Small Outline Package (Surface-mount, SSOP)	-40 to +85°C	SA620DK	1563

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage[1]	-0.3 to +6	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{CC} + 0.3)	V
P_D	Power dissipation, T_A = 25°C (still air)[2] 20-Pin Plastic SSOP	980	mW
T_{JMAX}	Maximum operating junction temperature	150	°C
P_{MAX}	Maximum power input/output	+20	dBm
T_{STG}	Storage temperature range	–65 to +150	°C

NOTE:
1. Transients exceeding 8V on V_{CC} pin may damage product.
2. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance,
   θ_{JA}: 20-Pin SSOP = 110°C/W

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	2.7 to 5.5	V
T_A	Operating ambient temperature range	-40 to +85	°C
T_J	Operating junction temperature	-40 to +105	°C

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
I_{CC}	Supply current	LNA enable input high		10.4		mA
		LNA enable input low		7.2		mA
		VCO power-down input low		7.4		mA
		Mixer power-down input low		7.4		mA
		Full chip power-down		1.2		mA
V_T	Enable logic threshold voltage[NO TAG]		1.2	1.5	1.8	V
V_{IH}	Logic 1 level	RF amp on	2.0		V_{CC}	V
V_{IL}	Logic 0 level	RF amp off	–0.3		0.8	V
I_{IL}	Enable input current	Enable = 0.4V	-1	0	1	µA
I_{IH}	Enable input current	Enable = 2.4V	-1	0	1	µA
V_{LNA-IN}	LNA input bias voltage	Enable = 2.4V		0.78		V
$V_{LNA-OUT}$	LNA output bias voltage	Enable = 2.4V		2.1		V
V_B	LNA bias voltage	Enable = 2.4V		2.1		V
V_{MX-IN}	Mixer RF input bias voltage			0.94		V

NOTE:
1. The ENABLE input must be connected to a valid logic level for proper operation of the SA620 LNA.

AC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; Enable = +3V; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			-3σ	TYP	+3σ	
S_{21}	Amplifier gain	900MHz	10	11.5	13	dB
S_{21}	Amplifier gain in through mode	Enable = 0.4V, 900MHz	-9	-7.5	-6	dB
$\Delta S_{21}/\Delta T$	Gain temperature sensitivity in pwr-dwn mode	900MHz		-0.014		dB/°C
$\Delta S_{21}/\Delta T$	Gain temperature sensitivity enabled	900MHz		0.003		dB/°C
$\Delta S_{21}/\Delta f$	Gain frequency variation	800MHz - 1.2GHz		0.01		dB/MHz
S_{12}	Amplifier reverse isolation	900MHz		-20		dB
S_{11}	Amplifier input match[1]	900MHz		-10		dB
S_{22}	Amplifier output match[1]	900MHz		-12		dB
P_{-1dB}	Amplifier input 1dB gain compression	900MHz		-16		dBm
IP3	Amplifier input third order intercept	900MHz	-4.5	-3	-1.5	dBm
NF	Amplifier noise figure	900MHz	1.3	1.6	1.9	dB
t_{ON}	Amplifier turn-on time (Enable Lo → Hi)	See Figure 1		50		µs
t_{OFF}	Amplifier turn-off time (Enable Hi → Lo)	See Figure 1		5		µs
VG_C	Mixer voltage conversion gain: $R_P = R_L = 1k\Omega$,	f_S = 0.9GHz, f_{LO} = 0.8GHz, f_{IF} = 100MHz	14.5	16	17.5	dB
PG_C	Mixer power conversion gain: $R_P = R_L = 1k\Omega$,	f_S = 0.9GHz, f_{LO} = 0.8GHz, f_{IF} = 100MHz	1.5	3	4.5	dB
S_{11M}	Mixer input match[1]	900MHz		-10		dB
NF_M	Mixer SSB noise figure	900MHz	7.5	9	10.5	dB
P_{-1dB}	Mixer input 1dB gain compression	900MHz		-13		dBm
$IP3_M$	Mixer input third order intercept	f_2–f_1 = 1MHz, 900MHz	-7.5	-6	-4.5	dBm
IP_{2INT}	Mixer input second order intercept	900MHz		12		dBm
P_{RFM-IF}	Mixer RF feedthrough	900MHz		-20		dB
P_{LO-IF}	LO feedthrough to IF	900MHz		-25		dBm
P_{LO-RFM}	LO to mixer input feedthrough	900MHz		-30		dBm
P_{LO-RF}	LO to LNA input feedthrough	900MHz		-45		dBm
P_{VCO}	VCO buffer out	900MHz		-16		dBm
	VCO frequency range		300 (min)		1200 (max)	MHz
	VCO phase noise	Offset = 60kHz		-105		dBc/Hz

NOTE:
1. Simple L/C elements are needed to achieve specified return loss.

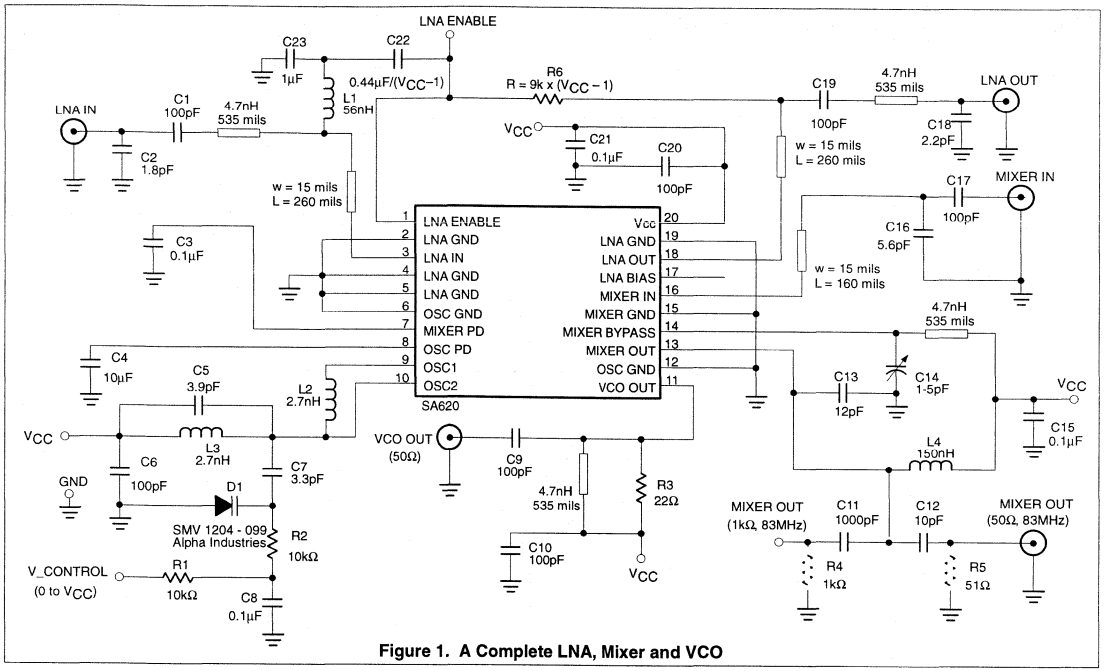


Figure 1. A Complete LNA, Mixer and VCO

CIRCUIT TECHNOLOGY

LNA

Impedance Match: Intrinsic return loss at the input and output ports is 7dB and 9dB, respectively. With no external matching, the associated LNA gain is ≈10dB and the noise figure is ≈1.4dB. However, the return loss can be improved at 900MHz using suggested L/C elements (Figure NO TAG) as the LNA is unconditionally stable.

Noise Match: The LNA achieves 1.6dB noise figure at 900MHz when S_{11} = -10dB. Further improvements in S_{11} will slightly increase the NF and S_{21}.

Thru-Mode: A series switch can be activated to feed RF signals from LNA input to output with an attenuator (S_{21} = −7.5dB). As a result, the power handling is greatly improved and current consumption is decreased by 3.2mA as well. However, if this mode is not required, C23 and R6 can be deleted.

Temperature Compensation: The LNA has a built-in temperature compensation scheme to reduce the gain drift to 0.003dB/°C from −40°C to +85°C.

Supply Voltage Compensation: Unique circuitry provides gain stabilization over wide supply voltage range. The gain changes no more than 0.5dB when V_{CC} increases from 3V to 5V.

Mixer

Input Match: The mixer is configured for maximum gain and best noise figure. The user needs to supply L/C elements to achieve this performance.

Mixer Bypass: To optimize the IP3 of the mixer input, one must adjust the value of C14 for the given board layout. The value typically lies between 1 and 5pF. Once a value if selected, a fixed capacitor can be used. Further improvements in mixer IP3 can be achieved by inserting a resistive loss at the mixer input, at the expense of system gain and noise figure.

Tracking Bandpass Filter: At the LO input port of the mixer there is a second-order bandpass filter (approx. 50MHz bandwidth) which will track the VCO center frequency. The result is the elimination of low frequency noise injected into the mixer LO port without the need for an external LO filter.

Power Down: The mixer can be disabled by connecting Pin 7 to ground. If a Schottky diode is connected between Pin 1 (cathode) and Pin 7 (anode), the LNA disable signal will control both LNA and mixer simultaneously When the mixer is disabled, 3mA is saved.

Test Port: Resistor R5 can be substituted with an external test port of 50Ω input impedance. Since R5 and MIXER OUT have the same output power, the result is a direct power gain measurement.

VCO

Automatic Leveling Loop: An on-chip detector and loop amplifier will adjust VCO bias current to regulate the VCO amplitude regardless of the Q-factor (>10) of the resonator and varactor diode. However, the real current reduction will not occur until the VCO frequency falls below 500MHz. For a typical resonator the steady-state current is 3mA at 800MHz.

Buffered VCO Output: The VCO OUT (Pin 11) signal can drive an external prescaler directly (see also the Philips SA7025 low voltage, fractional-N synthesizer). The extracted signal levels need to be limited to −16dBm or less to maintain mixer IIP3.

Phase Noise: If close-in phase noise is not critical, or if an external synthesizer is used, C4 (Pin 8) can be decreased to a lower value.

Power-Down: The VCO can be disabled by connecting Pin 8 to ground. If a Schottky diode is connected between Pin 1 (cathode) and Pin 8 (anode), the LNA disable signal will control both LNA and VCO simultaneously. When the VCO is disabled, 3mA is saved.

TYPICAL PERFORMANCE CHARACTERISTICS

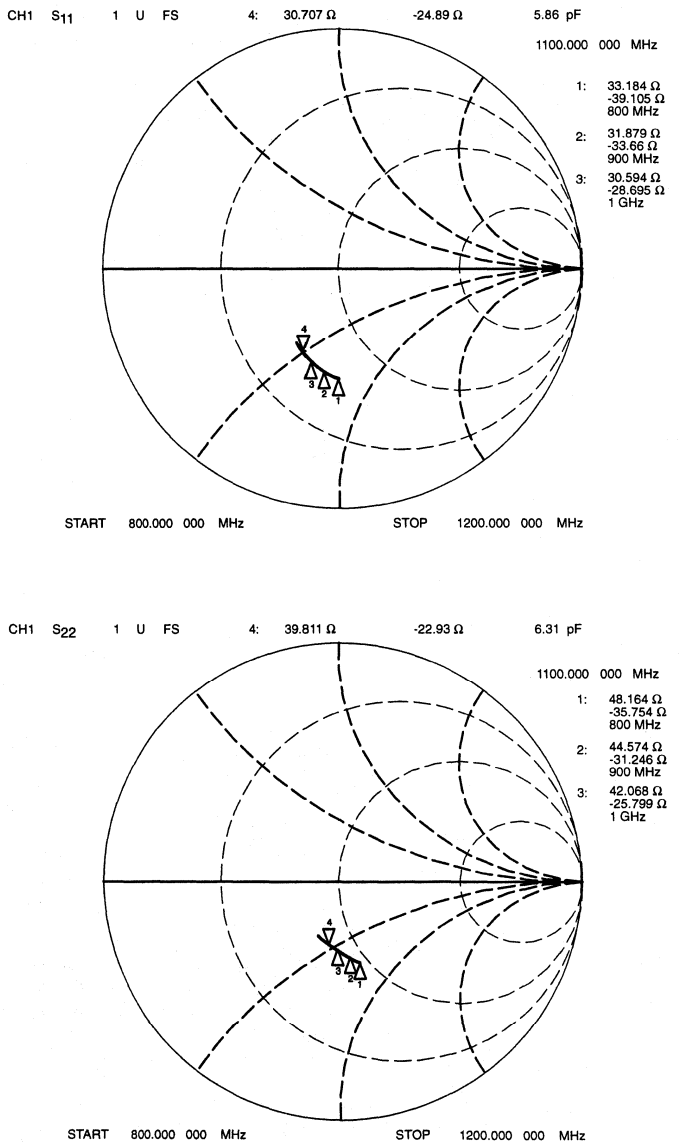
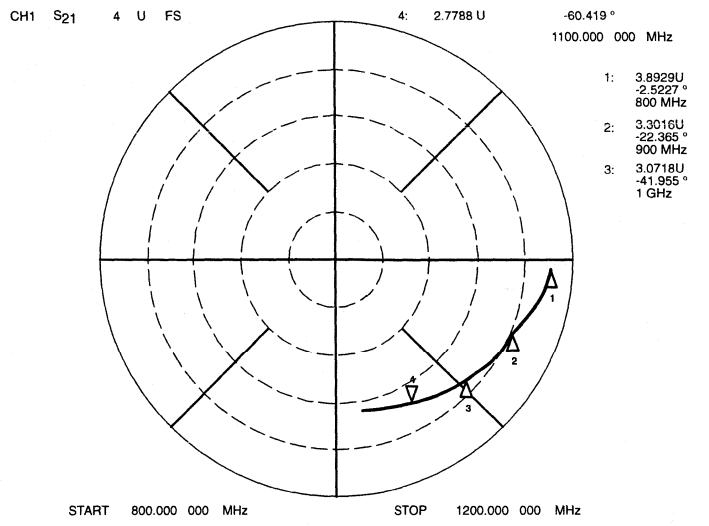


Figure 2. LNA Input and Output Match (at Device Pin)

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



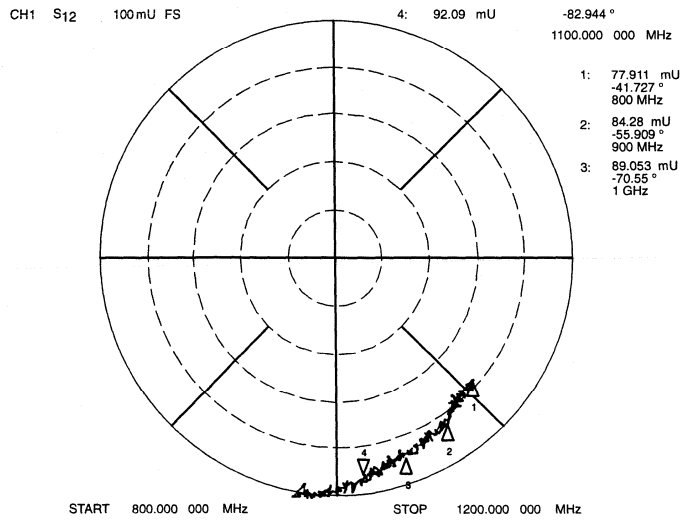


Figure 3. LNA Transmission and Isolation Characteristics (at Device Pin)

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

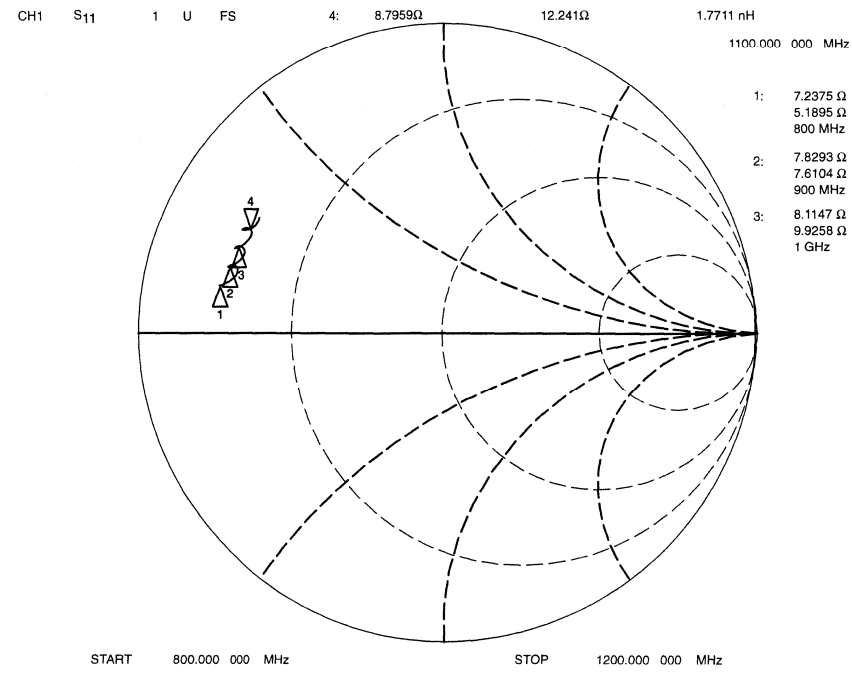
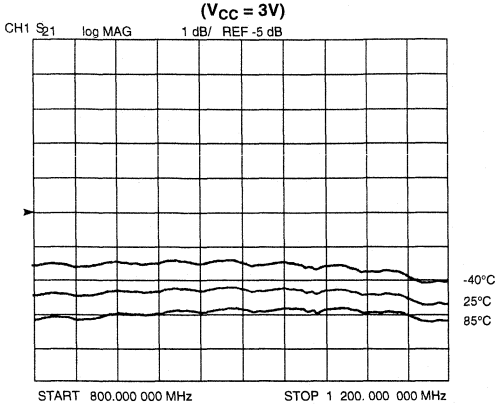


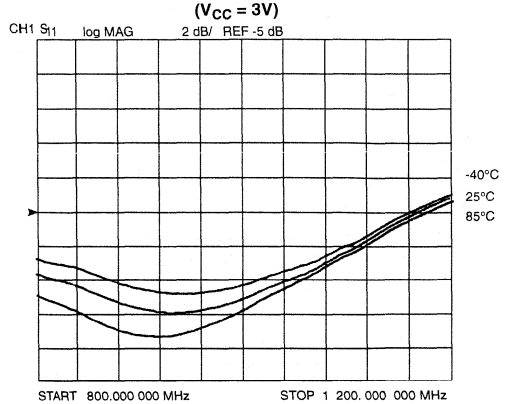
Figure 4. Mixer RF Input Match (at Device Pin)

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

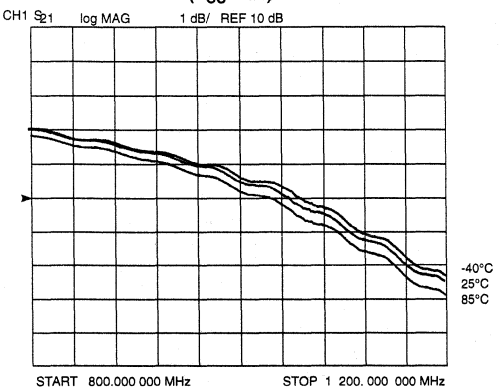
LNA Gain (S_{21}) In Through Mode vs. Frequency (V_{CC} = 3V)



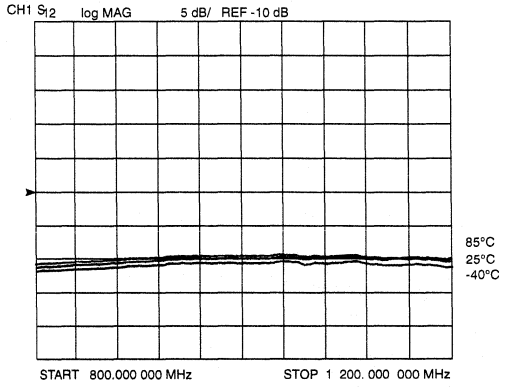
Mixer RF Input Match vs. Frequency (V_{CC} = 3V)



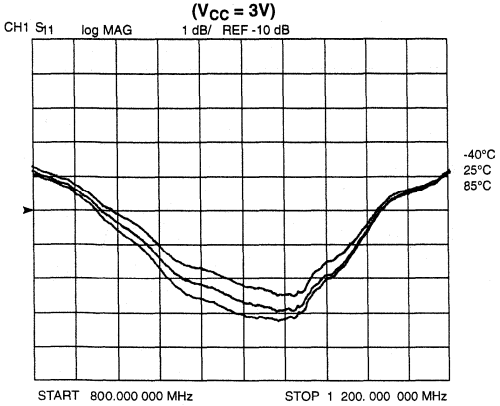
LNA Gain (S_{21}) vs. Frequency (V_{CC} = 3V)



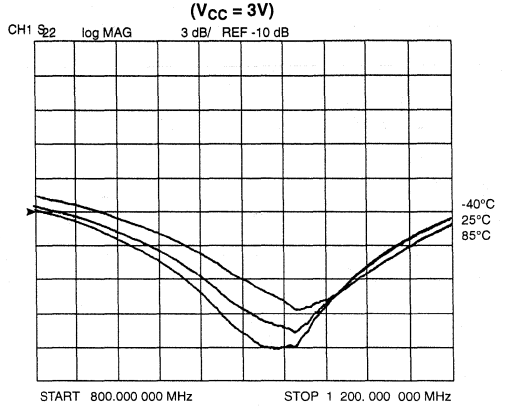
LNA Isolation (S_{12}) vs. Frequency (V_{CC} = 3V)



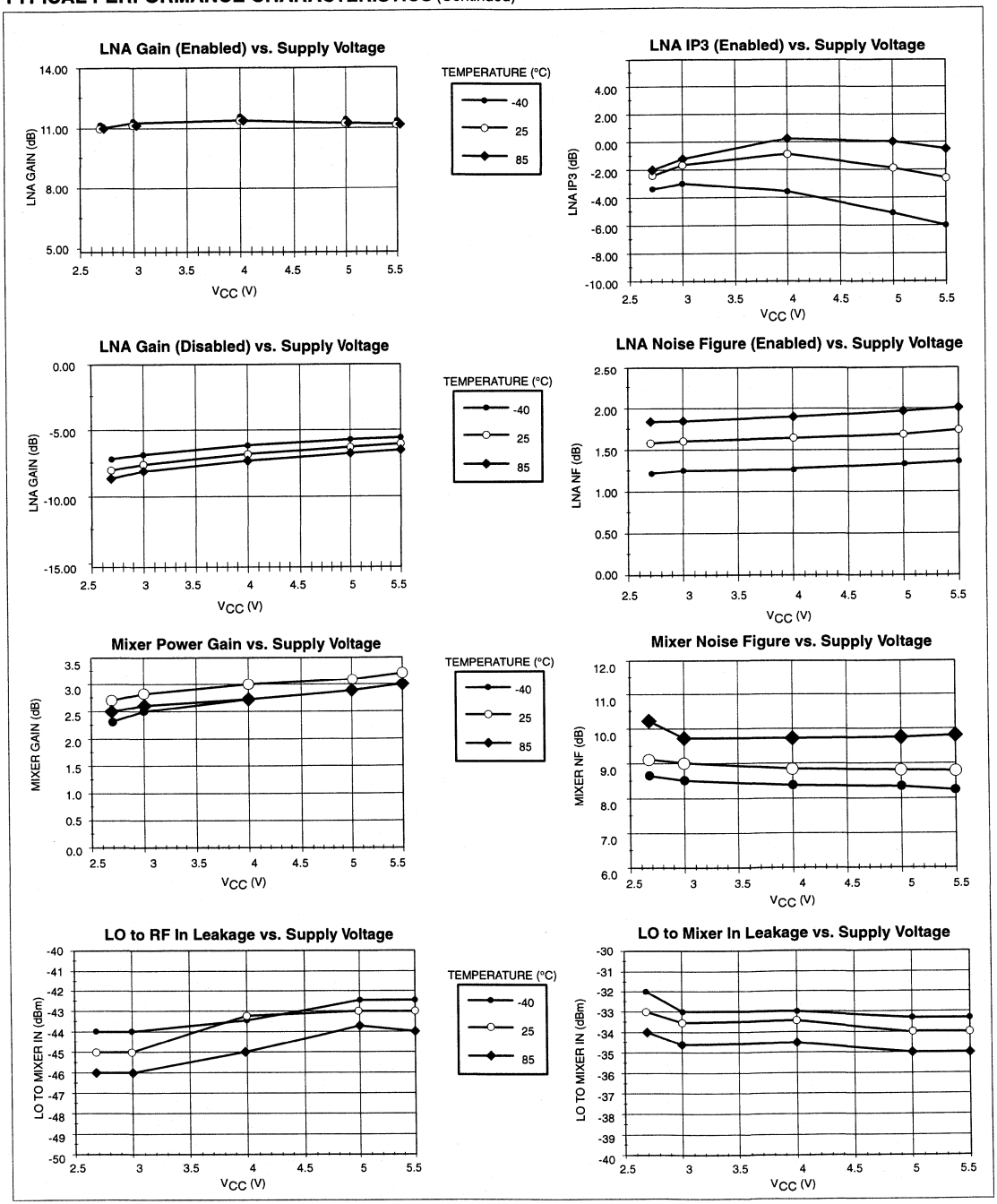
LNA Input Match (S_{11}) vs. Frequency (V_{CC} = 3V)



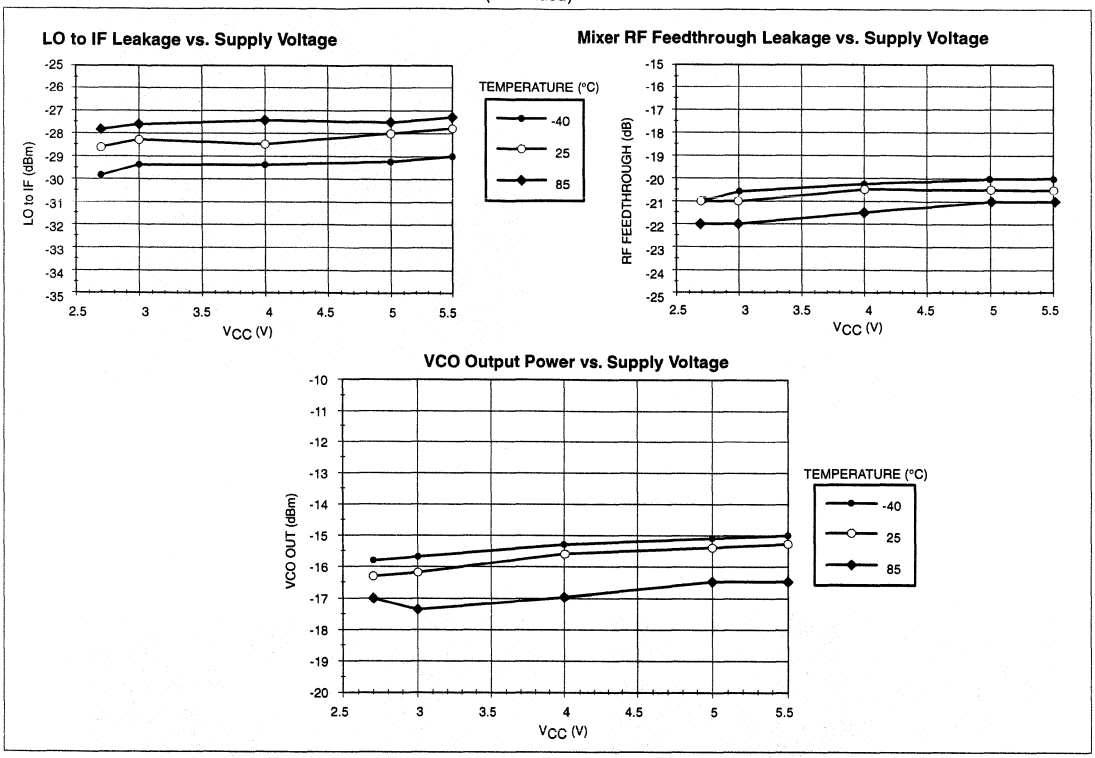
LNA Output Match (S_{22}) vs. Frequency (V_{CC} = 3V)



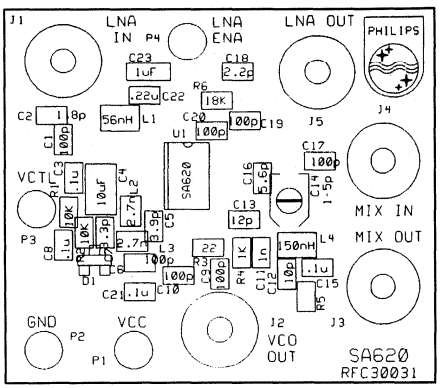
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

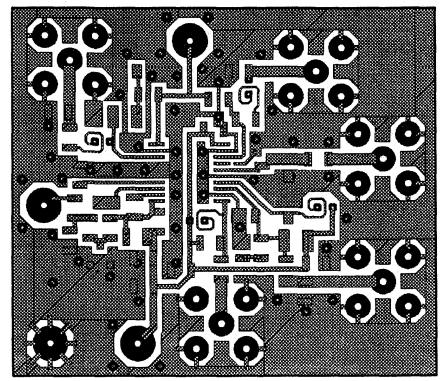


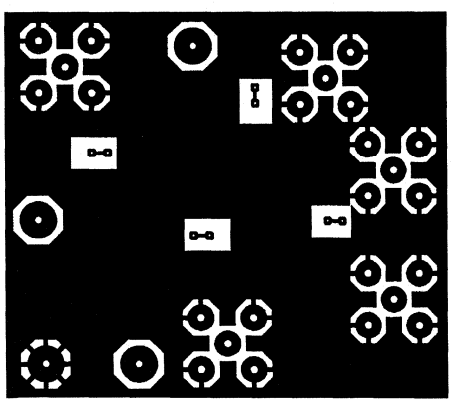
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

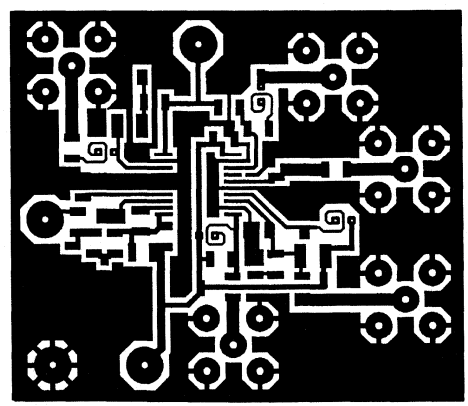


Low voltage LNA, mixer and VCO — 1GHz SA620









1GHz low voltage LNA, mixer and VCO SA621

DESCRIPTION

The SA621 is a combined low-noise amplifier, mixer and VCO designed for high-performance low-power communication systems from 800-1000MHz. The low-noise preamplifier has a 1.7dB noise figure at 881MHz with 15dB gain and an IP3 intercept of -7dBm at the input. The gain is stabilized by on-chip compensation to vary less than ±0.2dB over -40 to +85°C temperature range. The wide-dynamic-range mixer has a 12dB noise figure and IP3 of +4.5dBm at the input at 881MHz. The integrated VCO circuit with external resonator produces a high quality LO signal that drives the mixer and is buffered to an external PLL synthesizer IC. The nominal current drawn from a single 3V supply is 13.3mA. Additionally, the entire circuit can be powered down to further reduce the supply current to less than 20µA.

FEATURES

- Low current consumption
- Outstanding gain and noise figure
- Excellent gain stability versus temperature and supply voltage
- LNA, mixer and VCO power down capability
- Monotonic VCO frequency vs control voltage

PIN CONFIGURATION

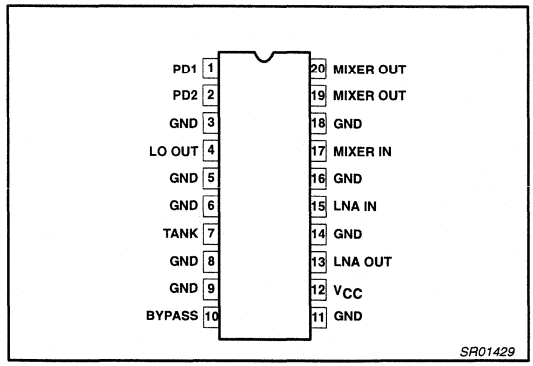


Figure 1. Pin Configuration

APPLICATIONS

- 900MHz cellular and cordless front-end
- Spread spectrum receivers
- RF data links
- UHF frequency conversion
- Portable radio

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Thin Shrink Small Outline Package (Surface-mount, TSSOP)	-40 to +85°C	SA621DH	SOT360-1

BLOCK DIAGRAM

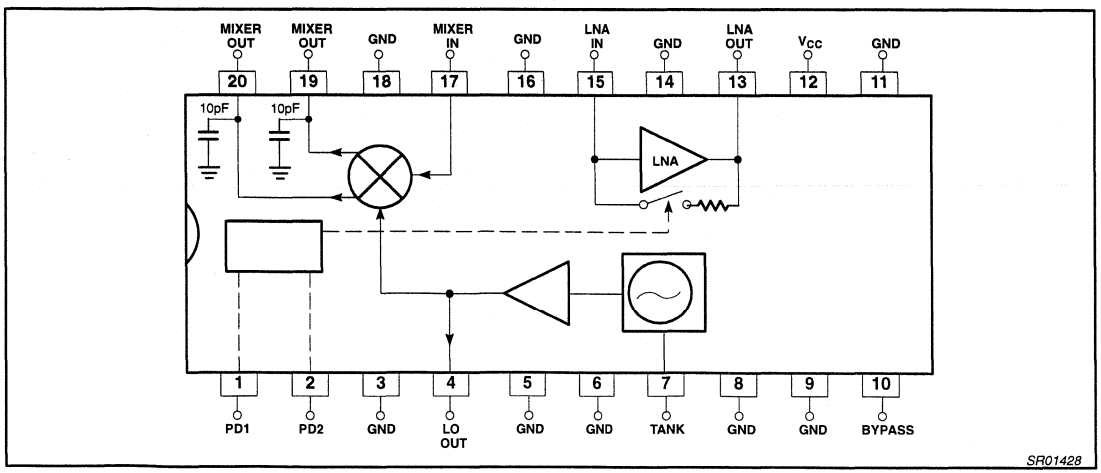


Figure 2. SA621 Block Diagram

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage[1]	-0.3 to +6	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{CC} + 0.3)	V
P_D	Power dissipation, T_A = 25°C (still air)2 20-Pin Plastic SSOP	980	mW
T_{JMAX}	Maximum operating junction temperature	150	°C
P_{MAX}	Maximum power input/output	+20	dBm
T_{STG}	Storage temperature range	–65 to +150	°C

NOTE:
1. Transients exceeding 8V on V_{CC} pin may damage product.
2. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance,
   θ_{JA}: 20-Pin SSOP = 110°C/W
3. Pins 19 and 20 are ESD sensitive (mixer outputs).

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	2.7 to 5.5	V
T_A	Operating ambient temperature range	-40 to +85	°C
T_J	Operating junction temperature	-40 to +105	°C

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3.0V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
I_{CC}	Supply current	Full power-on		13.3		mA
		LNA powered-down		10		mA
		Standby (VCO + bias)		5.7		mA
		Full power-down		20		µA
V_T	PD logic threshold voltage		1.2	1.6	1.8	V
V_{IH}	Logic 1 level		2.0		V_{CC}	V
V_{IL}	Logic 0 level		–0.3		0.8	V
I_{IL}	PD1 input current	Enable = 0.4V		10		µA
I_{IH}	PD2 input current	Enable = 2.4V		10		µA

AC ELECTRICAL CHARACTERISTICS

V_{CC} = +3.0V, T_A = 25°C; RF_{IN} = 881MHz, f_{VCO} = 964MHz; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			–3σ	TYP	+3σ	
Low Noise Amplifier						
f_{RF}	RF input frequency range		800		1000	MHz
S_{21}	Amplifier gain			15		dB
S_{21}	Amplifier gain in power-down mode			-28		dB
$\Delta S_{21}/\Delta T$	Gain temperature sensitivity enabled			0.006		dB/°C
$\Delta S_{21}/\Delta f$	Gain frequency variation	800MHz - 1.0GHz		±0.013		dB/MHz
S_{12}	Amplifier reverse isolation	@ 881 MHz		-28		dB
S_{11}	Amplifier input match	With ext. impedance matching		-10		dB
S_{22}	Amplifier output match			-10		dB
P_{-1dB}	Amplifier input 1dB gain compression			-20		dBm
IP3	Amplifier input third order intercept			-7		dBm
NF	Amplifier noise figure			1.7		dB
t_{ON}	Amplifier turn-on time (Enable Lo → Hi)			120		µs
t_{OFF}	Amplifier turn-off time (Enable Hi → Lo)			0.3		µs
Mixer						
PG_C	Mixer power conversion gain: $R_P = R_L$ = 1.2kΩ,	f_{RF} = 881MHz, f_{LO} = 964MHz, f_{IF} = 83MHz		8.7		dB
S_{11M}	Mixer input match	Ext. impedance matching req.		-10		dB
NF_M	Mixer SSB noise figure			12		dB
P_{-1dB}	Mixer input 1dB gain compression			-10		dBm
$IP3_M$	Mixer input third order intercept			4.5		dBm
IP_{2INT}	Mixer input second order intercept			15		dBm
P_{RFM-IF}	Mixer RF feedthrough	RF_{IN} = -25dBm		-41		dBm
P_{LO-IF}	LO feedthrough to IF	LO = -10dBm		-23		dBm
P_{LO-RFM}	LO to mixer input feedthrough			-52		dBm
P_{LO-RF}	LO to LNA input feedthrough			-38		dBm
Voltage Controlled Oscillator (VCO)[1]						
f_{VCO}	VCO frequency range		883		1083	MHz
P_{VCO}	VCO power out	See Figure 3	-10	-8		dBm
	VCO phase noise[2]	Offset = 30kHz		-109		dBc/Hz
		Offset = 60kHz		-115		
	Harmonic content			-22		dBc
	Residual modulation				45	dB
	Pulling figure	VSWR=2:1, all phases		±500		kHz
	Pushing figure			±100		kHz/V
Overall System						
G_{SYS}	System gain	LNA + Mixer	23.0	23.7	24.4	dB

NOTES:
1. VCO performance dependent on external components.
2. Based on copper-plated 2mm ceramic resonator (1/4 wave), f = 1025MHz, and can be improved by silver-plated or larger resonators.

Table 1. Power ON/OFF Control Logic

PD1	PD2	
0	0	Full chip power-down
0	1 or open	VCO on, Mixer on, LNA power-down
1 or open	0	VCO on, LNA and Mixer power-down
1 or open	1 or open	Full chip power-on (default)

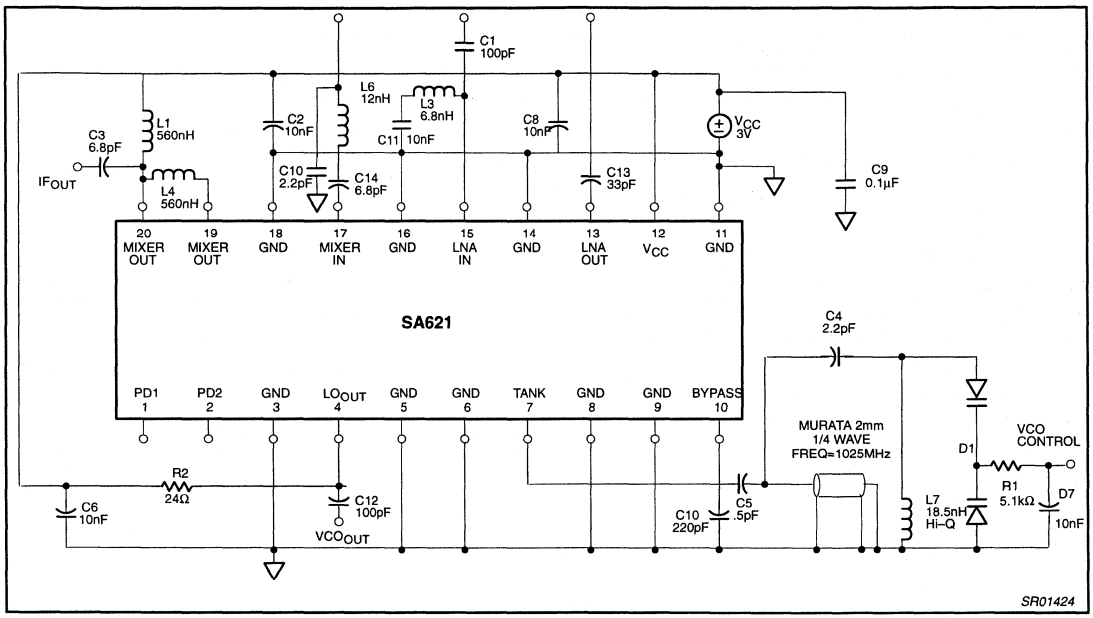


Figure 3. SA621 Applications Circuit

PERFORMANCE CHARACTERISTICS

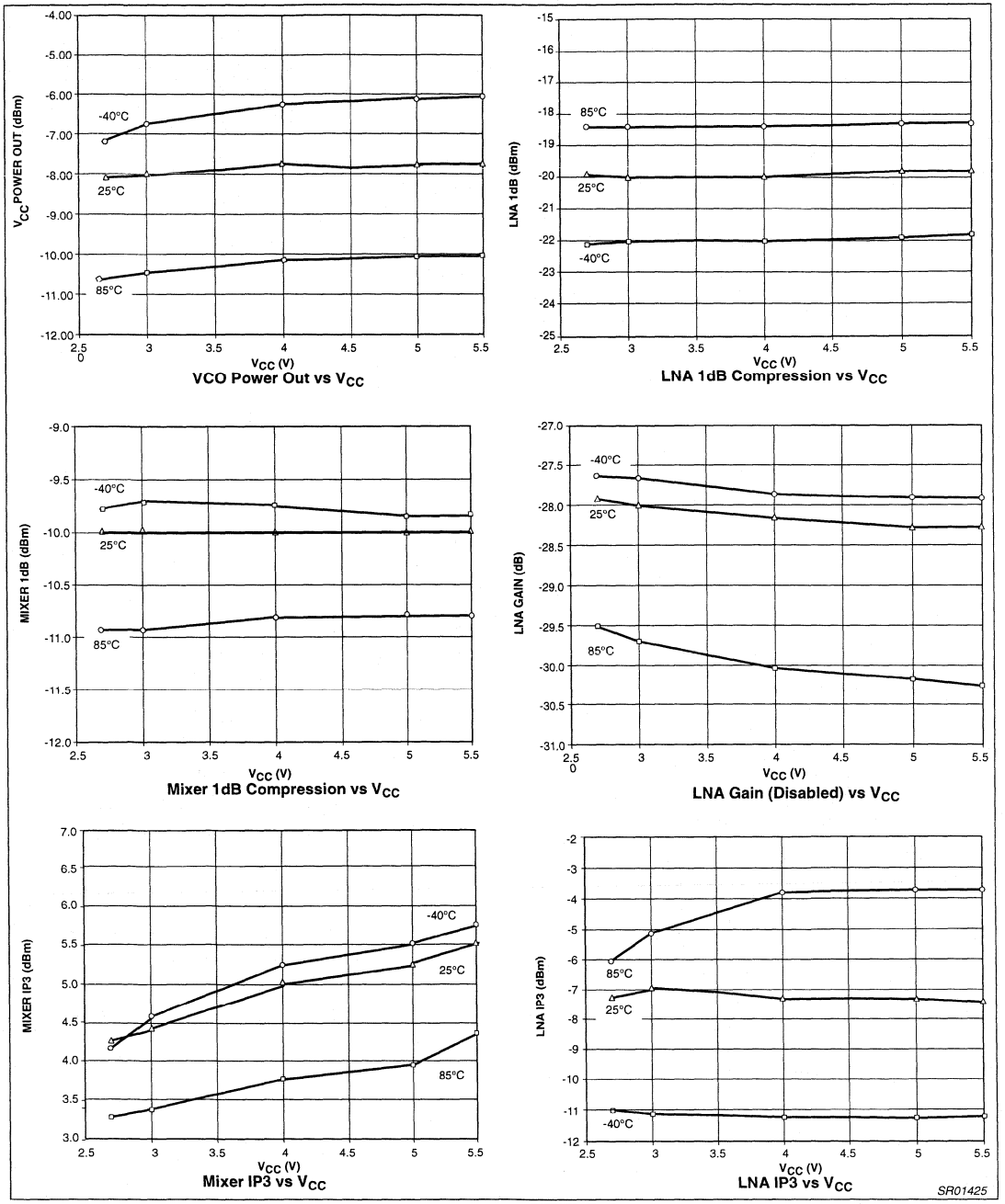
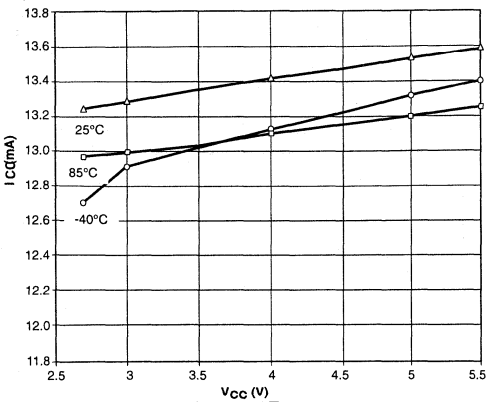
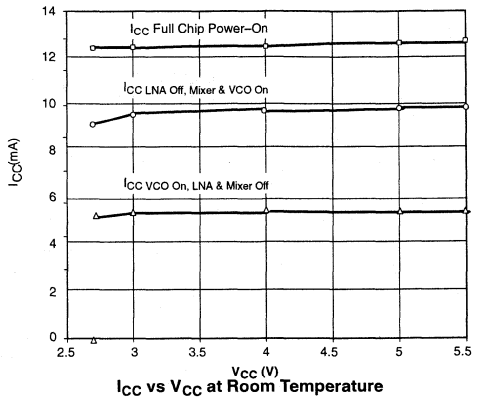


Figure 4.

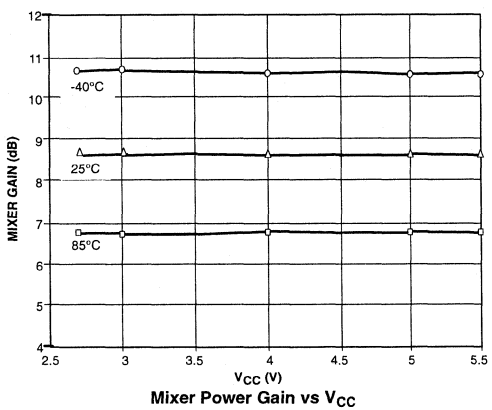
PERFORMANCE CHARACTERISTICS



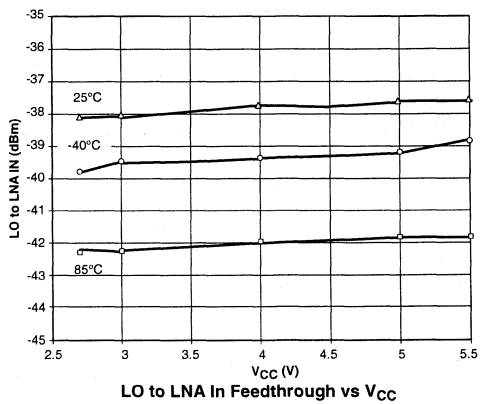
I_{CC} vs V_{CC} and Temperature



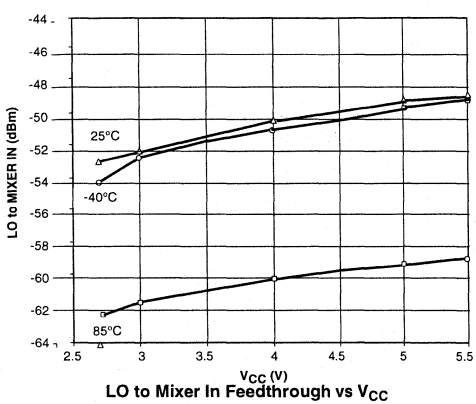
I_{CC} vs V_{CC} at Room Temperature



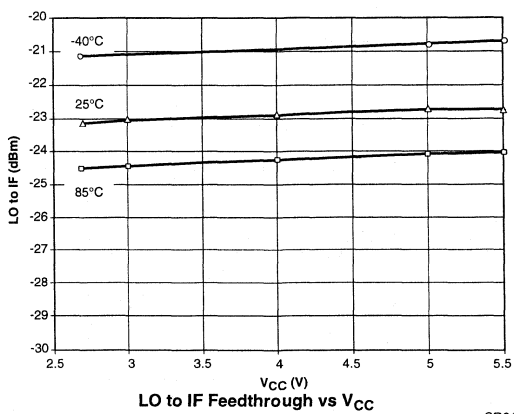
Mixer Power Gain vs V_{CC}



LO to LNA In Feedthrough vs V_{CC}



LO to Mixer In Feedthrough vs V_{CC}

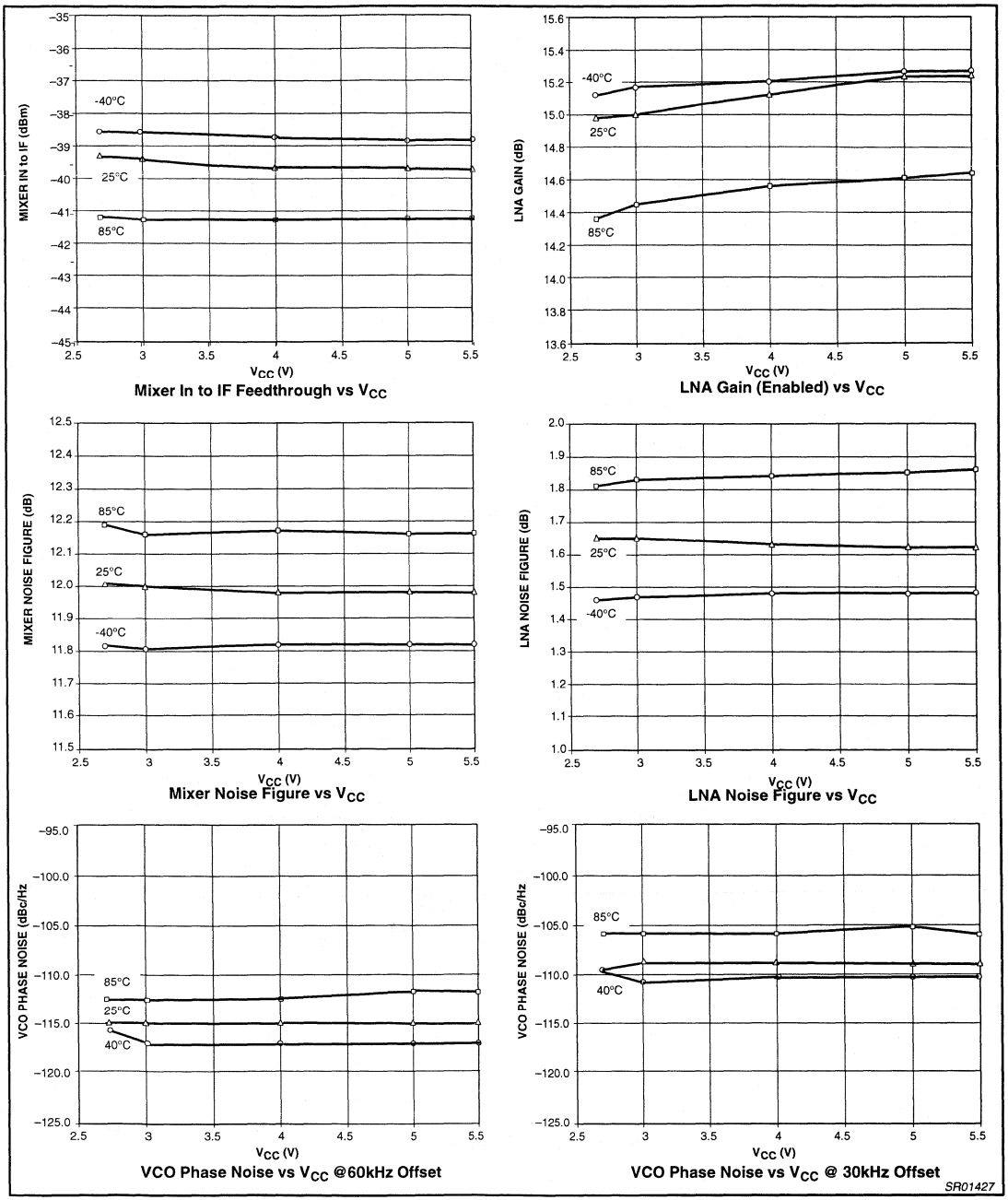


LO to IF Feedthrough vs V_{CC}

SR01426

Figure 5.

PERFORMANCE CHARACTERISTICS



Mixer In to IF Feedthrough vs V_{CC}

LNA Gain (Enabled) vs V_{CC}

Mixer Noise Figure vs V_{CC}

LNA Noise Figure vs V_{CC}

VCO Phase Noise vs V_{CC} @60kHz Offset

VCO Phase Noise vs V_{CC} @ 30kHz Offset

Figure 6.

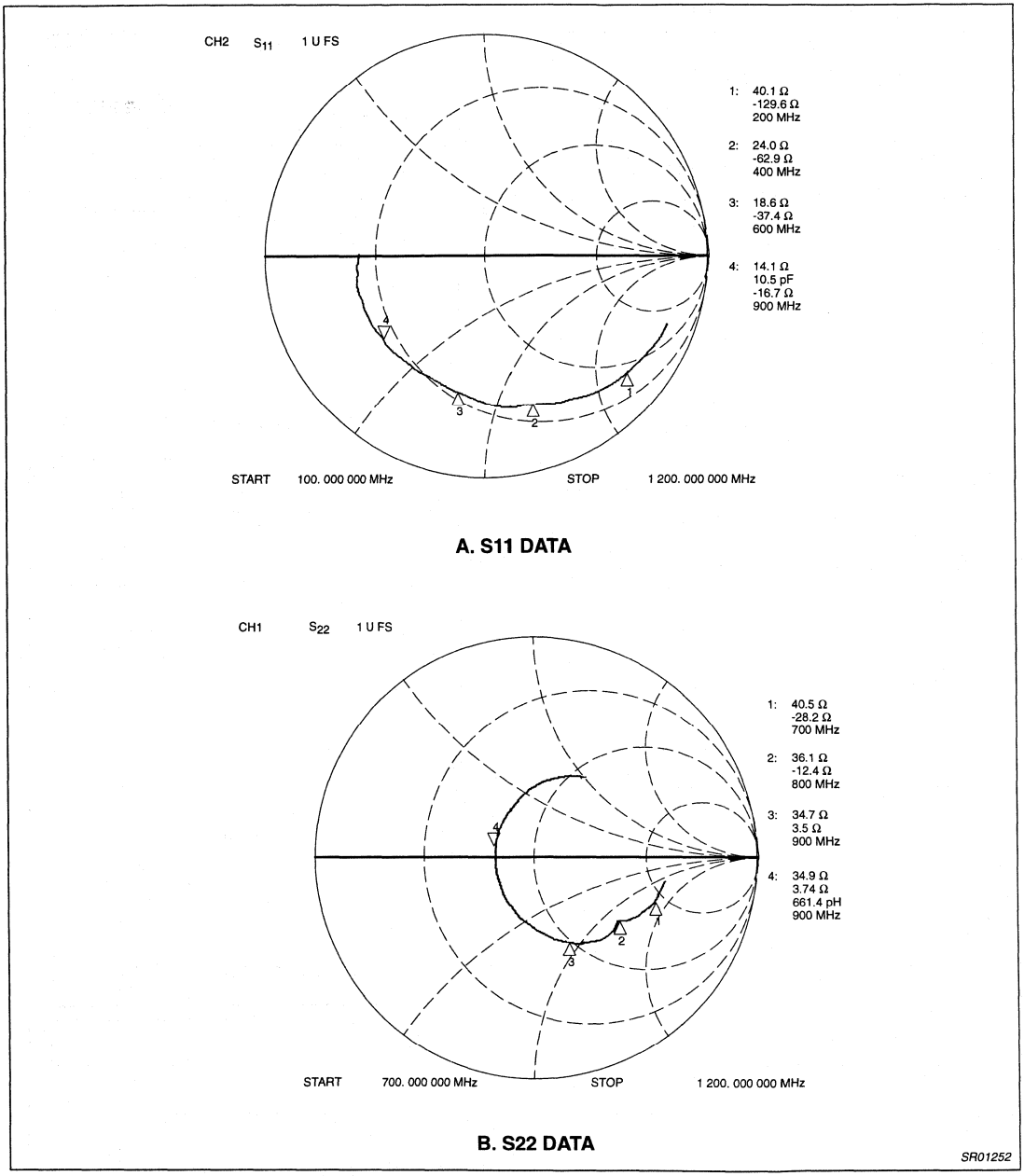


Figure 7. Typical S_{11} of LNA at 3V

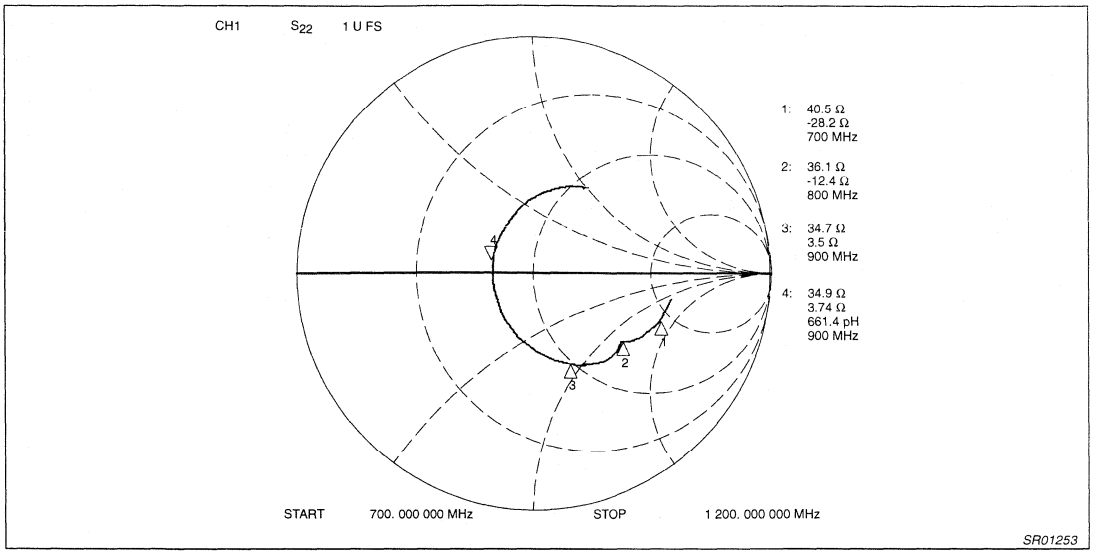


Figure 8. Typical S_{22} of LNA at 3V

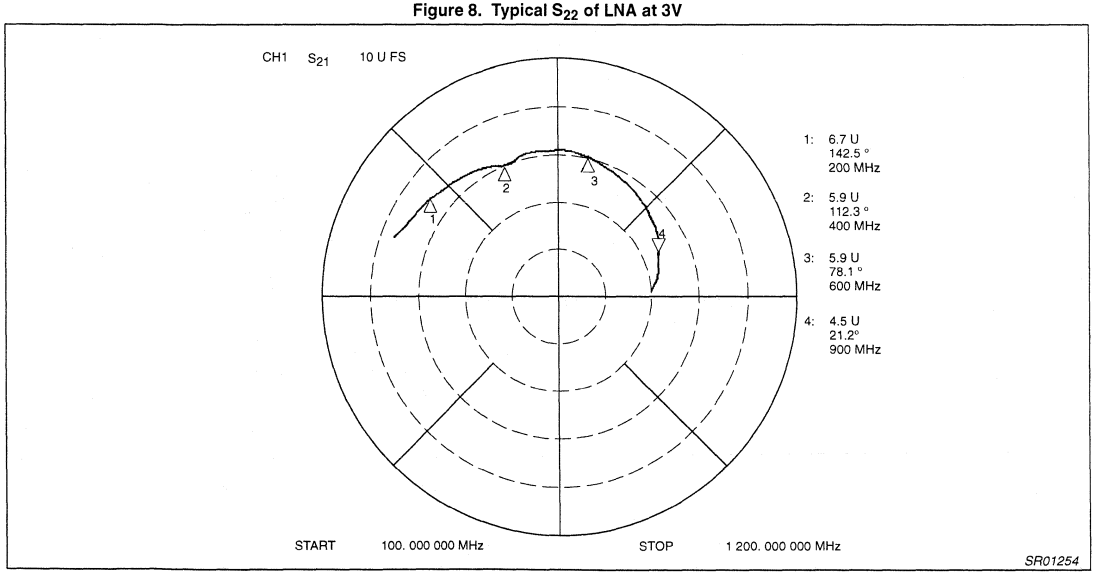


Figure 9. Typical S_{21} of LNA at 3V

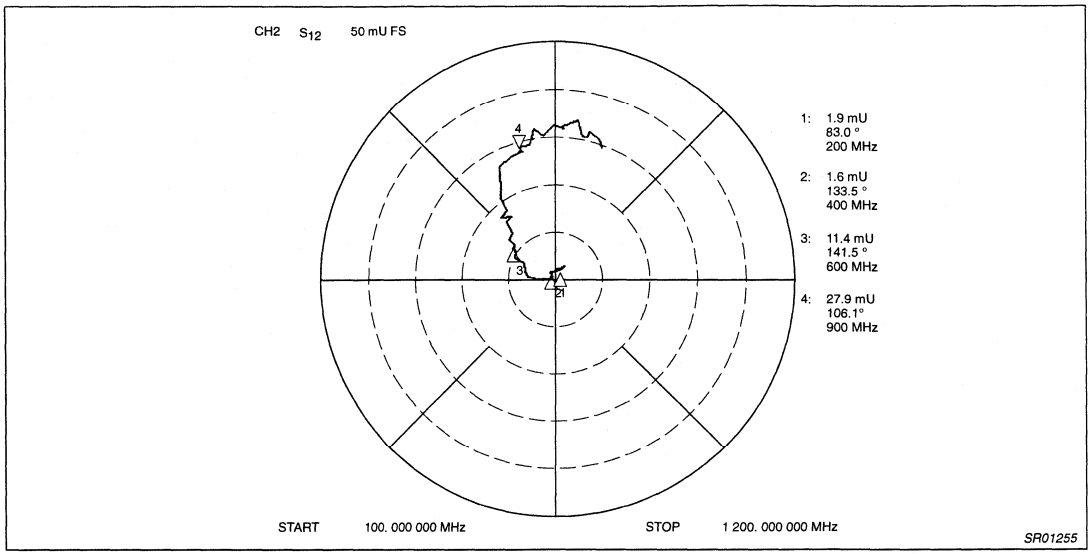


Figure 10. Typical S_{12} of LNA at 3V

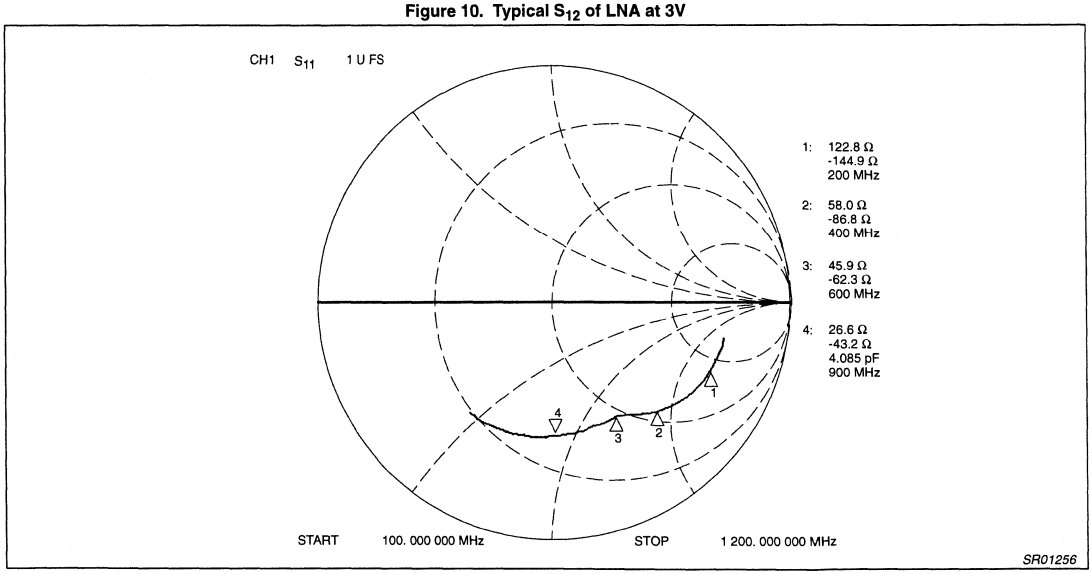


Figure 11. Typical S_{11} of Mixer at 3V

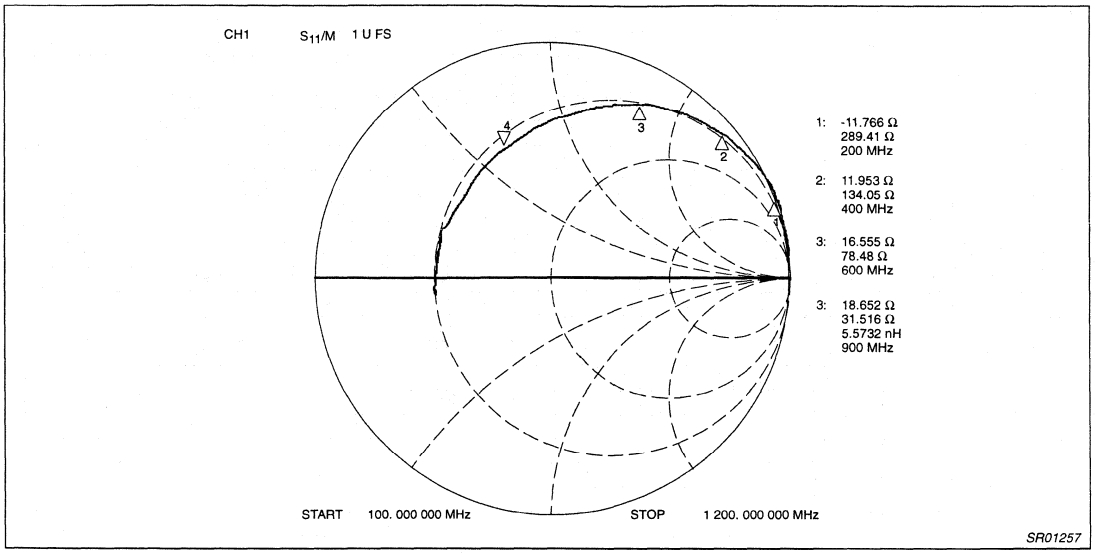


Figure 12. Typical $1/S_{11}$ of VCO (Pin 7)at 3V

Table 2. Typical S-Parameters of LNA at 3V

LNA								
Freq (MHz)	$\|S_{11}\|$ (U)	$<S_{11}$ (deg)	$\|S_{21}\|$ (U)	$<S_{21}$ (deg)	$\|S_{12}\|$ (U)	$<S_{12}$ (deg)	$\|S_{22}\|$ (U)	$<S_{22}$ (deg)
100	0.86	-20	7.4	160	0.001	92	0.59	-10
122	0.86	-24	7.1	156	0.001	62	0.58	-12
144	0.85	-28	7.0	151	0.001	105	0.58	-14
166	0.83	-32	6.9	148	0.000	92	0.57	-16
188	0.82	-36	6.8	144	0.002	100	0.57	-18
210	0.81	-41	6.7	140	0.002	74	0.56	-20
232	0.80	-45	6.6	136	0.002	100	0.55	-22
254	0.79	-48	6.5	133	0.001	84	0.54	-25
276	0.78	-52	6.4	130	0.001	103	0.53	-27
298	0.76	-56	6.3	126	0.002	94	0.52	-29
320	0.75	-59	6.3	123	0.002	67	0.51	-31
342	0.73	-63	6.2	119	0.002	108	0.50	-33
364	0.71	-66	6.1	116	0.002	118	0.48	-35
386	0.70	-69	6.0	113	0.001	103	0.47	-36
408	0.69	-72	5.9	111	0.001	176	0.46	-37
430	0.68	-76	5.9	109	0.004	174	0.45	-37
452	0.69	-78	6.0	106	0.006	162	0.46	-38
474	0.68	-82	6.1	102	0.007	160	0.47	-42
496	0.67	-85	6.1	97	0.008	153	0.47	-46
518	0.66	-89	6.1	93	0.010	146	0.46	-50
540	0.65	-92	6.1	89	0.009	142	0.45	-55
562	0.63	-96	6.1	85	0.010	138	0.43	-59
584	0.62	-99	6.0	81	0.011	146	0.42	-64
606	0.62	-102	5.9	77	0.011	141	0.40	-69
628	0.61	-104	5.8	72	0.013	137	0.38	-73
650	0.61	-107	5.7	69	0.013	131	0.36	-78
672	0.60	-109	5.7	65	0.016	130	0.34	-84
694	0.60	-112	5.6	61	0.016	132	0.31	-90
716	0.59	-115	5.5	57	0.017	129	0.29	-97
738	0.59	-118	5.5	53	0.019	128	0.27	-104
760	0.59	-121	5.3	48	0.021	123	0.24	-113
782	0.59	-124	5.3	44	0.021	122	0.22	-122
804	0.59	-126	5.1	40	0.022	120	0.21	-133
826	0.59	-129	5.0	36	0.024	118	0.19	-145
848	0.59	-132	4.9	31	0.026	116	0.18	-159
870	0.59	-135	4.8	26	0.027	112	0.17	-175
892	0.59	-138	4.6	22	0.028	108	0.18	169
914	0.59	-142	4.5	18	0.028	106	0.19	155
936	0.59	-144	4.3	14	0.028	106	0.20	142
958	0.59	-148	4.2	9	0.030	100	0.22	130
980	0.59	-151	4.0	4	0.031	99	0.24	120
1002	0.59	-153	3.8	0	0.031	95	0.26	111
1024	0.59	-157	3.6	-2	0.032	91	0.28	102
1046	0.59	-160	3.5	-6	0.032	86	0.30	95
1068	0.59	-164	3.3	-10	0.033	86	0.33	88
1090	0.59	-167	3.2	-14	0.033	81	0.35	82
1112	0.59	-170	3.0	-18	0.031	79	0.36	77
1134	0.58	-172	2.8	-22	0.030	46	0.38	72
1156	0.58	-175	2.7	-25	0.031	79	0.39	67
1178	0.57	-178	2.5	-28	0.031	74	0.41	63
1200	0.57	178	2.4	-31	0.029	72	0.42	59

Table 3. Typical S-Parameters of Mixer at 3V

Mixer		
Freq (MHz)	$\|S_{11}\|$ (U)	$<S_{11}$ (deg)
100	0.73	-11
122	0.73	-147
144	0.72	-16
166	0.72	-19
188	0.72	-21
210	0.71	-24
232	0.70	-27
254	0.70	-29
276	0.69	-32
298	0.68	-34
320	0.67	-37
342	0.66	-39
364	0.64	-42
386	0.63	—44
408	0.62	-46
430	0.61	-48
452	0.59	-50
474	0.58	-52
496	0.57	-53
518	0.56	-54
540	0.55	-56
562	0.55	-57
584	0.54	-59
606	0.54	-61
628	0.54	-62
650	0.54	-64

Mixer		
Freq (MHz)	$\|S_{11}\|$ (U)	$<S_{11}$ (deg)
672	0.54	-65
694	0.54	-67
716	0.54	-69
738	0.54	-71
760	0.54	-73
782	0.55	-76
804	0.55	-78
826	0.55	-80
848	0.55	-82
870	0.55	-85
892	0.56	-87
914	0.55	-90
936	0.56	-93
958	0.56	-96
980	0.56	-98
1002	0.56	-101
1024	0.57	-104
1046	0.57	-106
1068	0.57	-110
1090	0.57	-112
1112	0.57	-115
1134	0.57	-118
1156	0.57	-121
1178	0.57	-124
1200	0.57	-127

High performance low power FM IF system with high-speed RSSI

SA624

DESCRIPTION

The SA624 is pin-to-pin compatible with the SA604A, but has faster RSSI rise and fall time. The SA624 is an improved monolithic low-power FM IF system incorporating two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic received signal strength indicator, and voltage regulator. The SA624 features higher IF bandwidth (25MHz) and temperature compensated RSSI and limiters permitting higher performance application compared with the SA604. The SA624 is available in 16-lead SO (surface-mounted miniature) package.

FEATURES

- Low power consumption: 3.4mA typical
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- Fast RSSI rise and fall time
- Two audio outputs - muted and unmuted
- Low external component count; suitable for crystal/ceramic filters
- Excellent sensitivity: 1.5μV across input pins (0.22μV into 50Ω matching network) for 12dB SINAD (Signal to Noise and Distortion ratio) at 455kHz
- SA624 meets cellular radio specifications

PIN CONFIGURATION

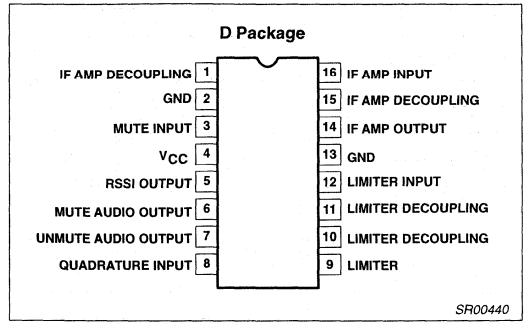


Figure 1. Pin Configuration

APPLICATIONS

- Digital cellular base station
- Cellular radio FM IF
- High performance communications receivers
- Intermediate frequency amplification and detection up to 25MHz
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Small Outline (SO) package (Surface-mount)	-40 to +85°C	SA624D	SOT109-1

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	9	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range SA624	-40 to +85	°C
θ_{JA}	Thermal impedance D package	90	°C/W

BLOCK DIAGRAM

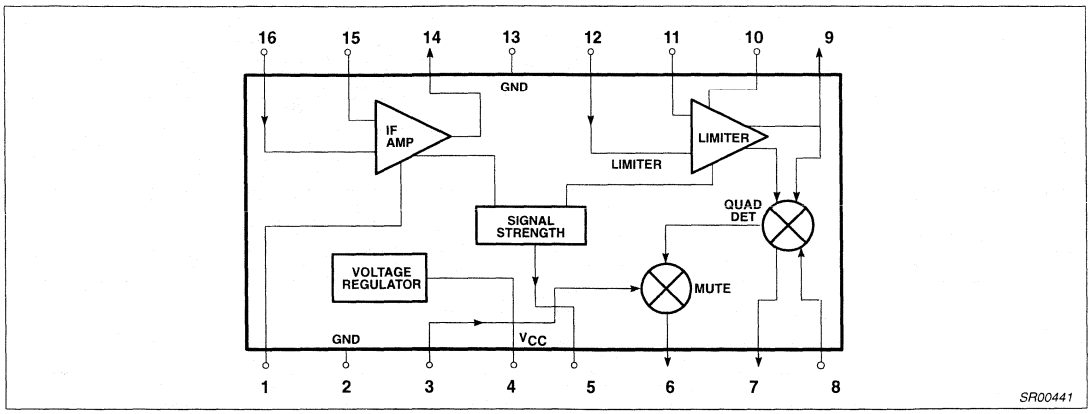


Figure 2. Block Diagram

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA624			
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		4.5		8.0	V
I_{CC}	DC current drain		2.5	3.4	4.2	mA
	Mute switch input threshold (ON) (OFF)		1.7		 1.0	V V

AC ELECTRICAL CHARACTERISTICS

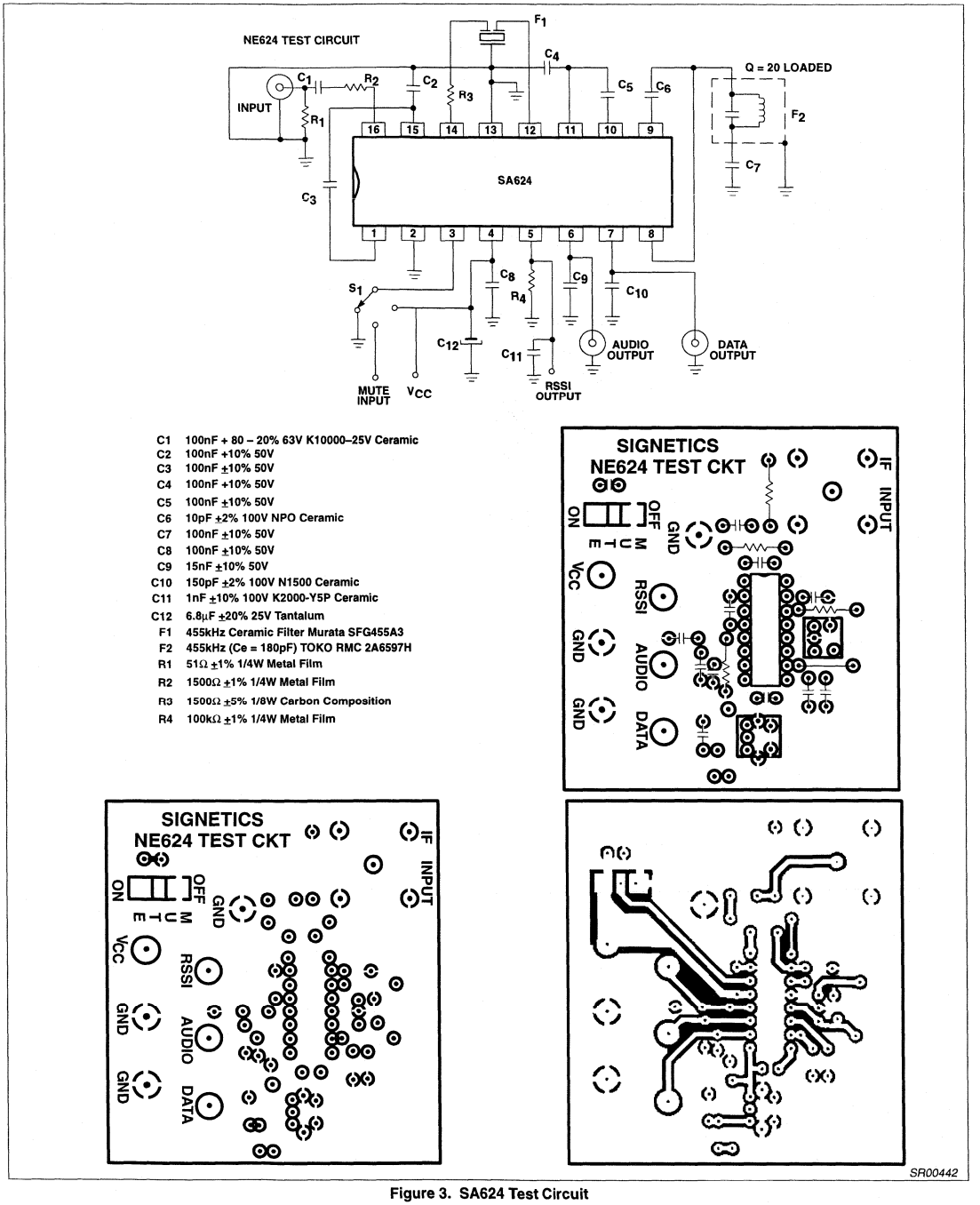
Typical reading at $T_A = 25°C$; $V_{CC} = +6V$, unless otherwise stated. IF frequency = 455kHz; IF level = -47dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 3. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA624			
			MIN	TYP	MAX	
	Input limiting -3dB	Test at Pin 16		-92		dBm/50Ω
	AM rejection	80% AM 1kHz	30	34		dB
	Recovered audio level	15nF de-emphasis	80	175	260	mV_{RMS}
	Recovered audio level	150pF de-emphasis		530		mV_{RMS}
THD	Total harmonic distortion		-34	-42		dB
S/N	Signal-to-noise ratio	No modulation for noise		73		dB
	RSSI output[1]	RF level = -118dBm	0	160	650	mV
		RF level = -68dBm	1.9	2.65	3.1	V
		RF level = -18dBm	4.0	4.85	5.6	V
	RSSI output rise time (10kHz pulse, no IF filter)	IF freq. = 455kHz				
		IF level = -44dBm		1.1		µs
		IF level = -16dBm		1.2		µs
		IF freq. = 10.7MHz				
		IF level = -44dBm		1.2		µs
		IF level = -16dBm		1.1		µs
	RSSI output fall time (10kHz pulse, no IF filter)	IF freq. = 455kHz				
		IF level = -44dBm		1.3		µs
		IF level = -16dBm		4.7		µs
		IF freq. = 10.7MHz				
		IF level = -44dBm		1.6		µs
		IF level = -16dBm		4.2		µs
	RSSI range	R_4 = 100k (Pin 5)		90		dB
	RSSI accuracy	R_4 = 100k (Pin 5)		±1.5		dB
	IF input impedance		1.4	1.6		kΩ
	IF output impedance		0.85	1.0		kΩ
	Limiter input impedance		1.4	1.6		kΩ
	Limiter output impedance			300		Ω
	Limiter output level no load			280		mV_{RMS}
	Unmuted audio output resistance			58		kΩ
	Muted audio output resistance			58		kΩ

NOTE:

1. SA604 data sheets refer to power at 50Ω input termination; about 21dB less power actually enters the internal 1.5k input.

SA604 (50)	SA624 (1.5k)/SA605 (1.5k
-97dBm	-118dBm
-47dBm	-68dBm
+3dBm	-18dBm



C1	100nF + 80 – 20% 63V K10000–25V Ceramic
C2	100nF +10% 50V
C3	100nF ±10% 50V
C4	100nF +10% 50V
C5	100nF ±10% 50V
C6	10pF ±2% 100V NPO Ceramic
C7	100nF ±10% 50V
C8	100nF ±10% 50V
C9	15nF ±10% 50V
C10	150pF ±2% 100V N1500 Ceramic
C11	1nF ±10% 100V K2000-Y5P Ceramic
C12	6.8µF ±20% 25V Tantalum
F1	455kHz Ceramic Filter Murata SFG455A3
F2	455kHz (Ce = 180pF) TOKO RMC 2A6597H
R1	51Ω ±1% 1/4W Metal Film
R2	1500Ω ±1% 1/4W Metal Film
R3	1500Ω ±5% 1/8W Carbon Composition
R4	100kΩ ±1% 1/4W Metal Film

Figure 3. SA624 Test Circuit

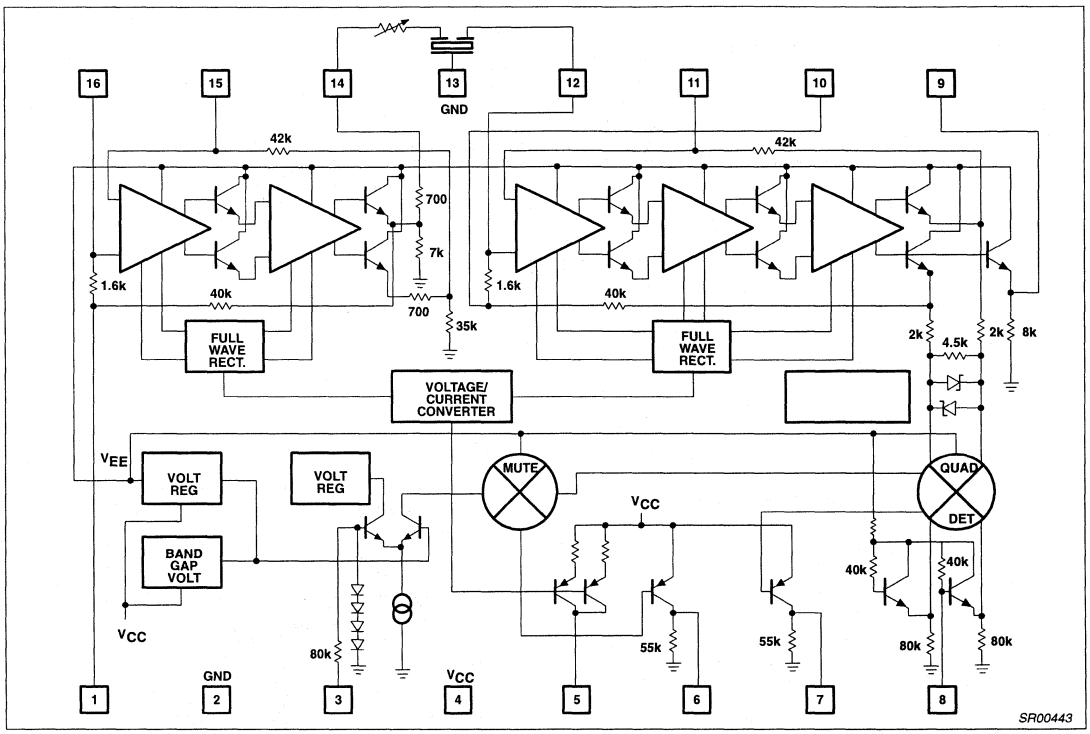


Figure 4. Equivalent Circuit

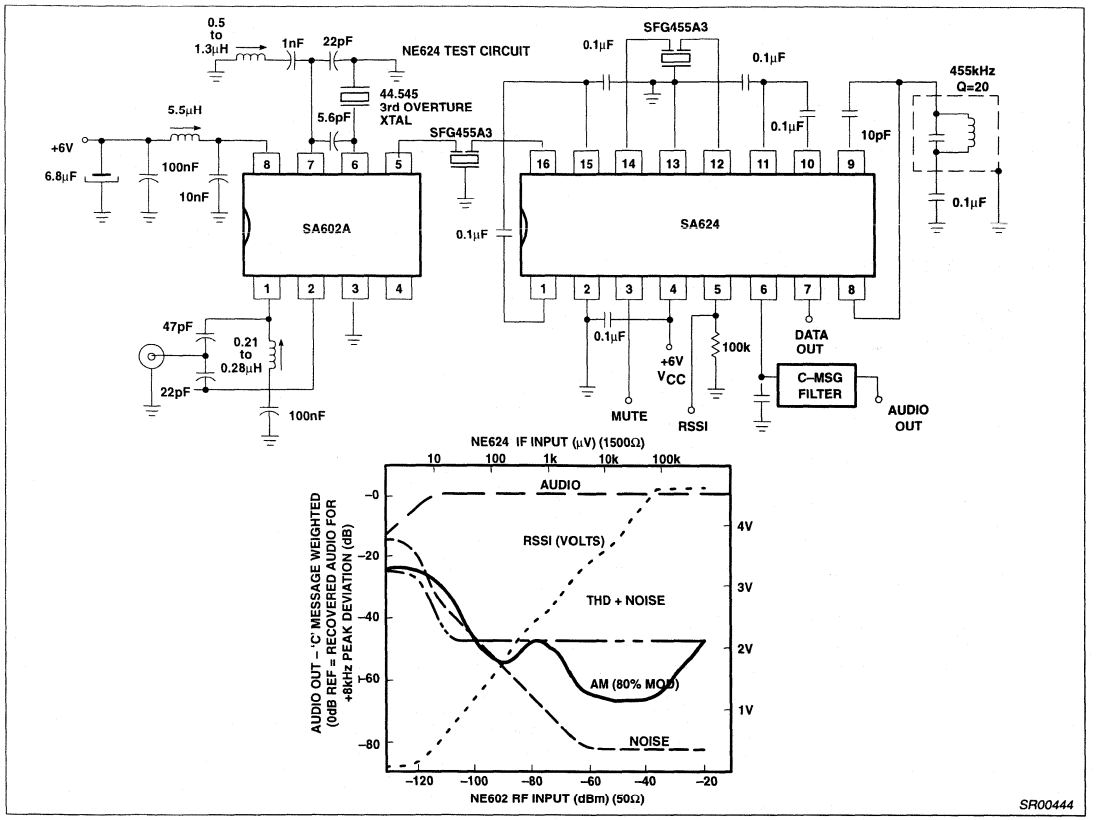


Figure 5. Typical Application Cellular Radio (45MHz to 455kHz)

CIRCUIT DESCRIPTION

The SA624 is a very high gain, high frequency device. Correct operation is not possible if good RF layout and gain stage practices are not used. The SA624 cannot be evaluated independent of circuit, components, and board layout. A physical layout which correlates to the electrical limits is shown in Figure 3. This configuration can be used as the basis for production layout.

The SA624 is an IF signal processing system suitable for IF frequencies as high as 21.4MHz. The device consists of two limiting amplifiers, quadrature detector, direct audio output, muted audio output, and signal strength indicator (with output characteristic). The sub-systems are shown in Figure 4. A typical application with 45MHz input and 455kHz IF is shown in Figure 5.

IF Amplifiers

The IF amplifier section consists of two log-limiting stages. The first consists of two differential amplifiers with 39dB of gain and a small signal bandwidth of 41MHz (when driven from a 50Ω source). The output of the first limiter is a low impedance emitter follower with 1kΩ of equivalent series resistance. The second limiting stage consists of three differential amplifiers with a gain of 62dB and a small signal AC bandwidth of 28MHz. The outputs of the final differential stage are buffered to the internal quadrature detector.

One of the outputs is available at Pin 9 to drive an external quadrature capacitor and L/C quadrature tank.

Both of the limiting amplifier stages are DC biased using feedback. The buffered output of the final differential amplifier is fed back to the input through 42kΩ resistors. As shown in Figure 4, the input impedance is established for each stage by tapping one of the feedback resistors 1.6kΩ from the input. This requires one additional decoupling capacitor from the tap point to ground.

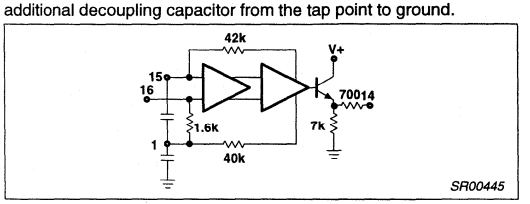


Figure 6. First Limiter Bias

Because of the very high gain, bandwidth and input impedance of the limiters, there is a very real potential for instability at IF frequencies above 455kHz. The basic phenomenon is shown in Figure 8. Distributed feedback (capacitance, inductance and radiated fields)

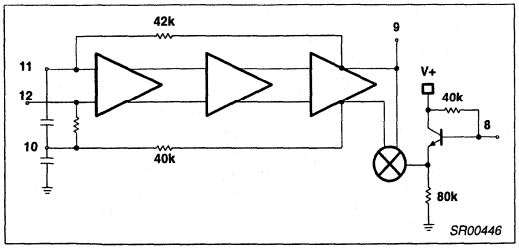


Figure 7. Second Limiter and Quadrature Detector

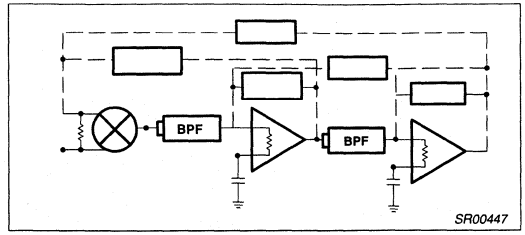


Figure 8. Feedback Paths

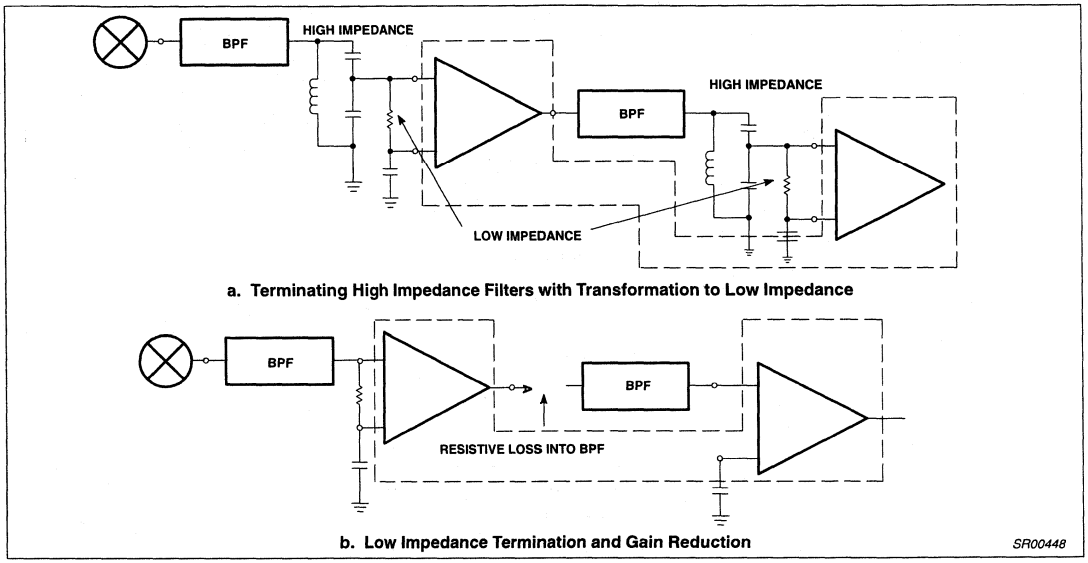


Figure 9. Practical Termination

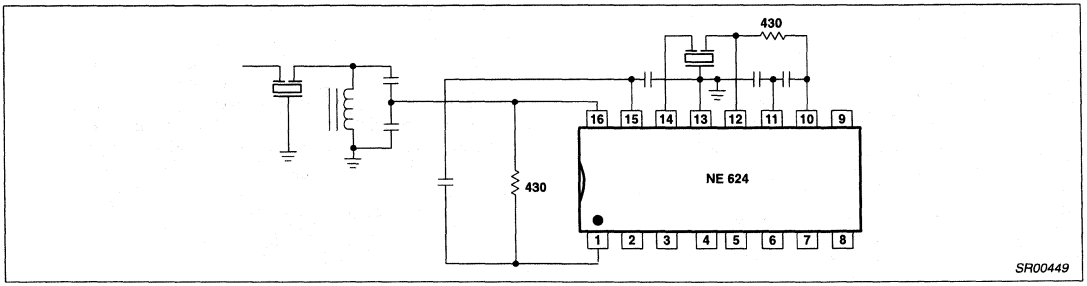


Figure 10. Crystal Input Filter with Ceramic Interstage Filter

forms a divider from the output of the limiters back to the inputs (including RF input). If this feedback divider does not cause attenuation greater than the gain of the forward path, then oscillation or low level regeneration is likely. If regeneration occurs, two symptoms may be present: (1)The RSSI output will be high with no signal input (should nominally be 250mV or lower), and (2) the demodulated output will demonstrate a threshold. Above a certain input level, the limited signal will begin to dominate the regeneration, and the demodulator will begin to operate in a "normal" manner.

There are three primary ways to deal with regeneration: (1) Minimize the feedback by gain stage isolation, (2) lower the stage input impedances, thus increasing the feedback attenuation factor, and (3) reduce the gain. Gain reduction can effectively be

accomplished by adding attenuation between stages. This can also lower the input impedance if well planned. Examples of impedance/gain adjustment are shown in Figure 9. Reduced gain will result in reduced limiting sensitivity.

A feature of the SA624 IF amplifiers, which is not specified, is low phase shift. The SA624 is fabricated with a 10GHz process with very small collector capacitance. It is advantageous in some applications that the phase shift changes only a few degrees over a wide range of signal input amplitudes. Additional information will be provided in the upcoming product specification (this is a preliminary specification) when characterization is complete.

Stability Considerations

The high gain and bandwidth of the SA624 in combination with its very low currents permit circuit implementation with superior performance. However, stability must be maintained and, to do that, every possible feedback mechanism must be addressed. These mechanisms are: 1) Supply lines and ground, 2) stray layout inductances and capacitances, 3) radiated fields, and 4) phase shift. As the system IF increases, so must the attention to fields and strays. However, ground and supply loops cannot be overlooked, especially at lower frequencies. Even at 455kHz, using the test layout in Figure 3, instability will occur if the supply line is not decoupled with two high quality RF capacitors, a 0.1µF monolithic right at the V_{CC} pin, and a 6.8µF tantalum on the supply line. An electrolytic is not an adequate substitute. At 10.7MHz, a 1µF tantalum has proven acceptable with this layout. Every layout must be evaluated on its own merit, but don't underestimate the importance of good supply bypass.

At 455kHz, if the layout of Figure 3 or one substantially similar is used, it is possible to directly connect ceramic filters to the input and between limiter stages with no special consideration. At frequencies above 2MHz, some input impedance reduction is usually necessary. Figure 9 demonstrates a practical means.

As illustrated in Figure 10, 430Ω external resistors are applied in parallel to the internal 1.6kΩ load resistors, thus presenting approximately 330Ω to the filters. The input filter is a crystal type for narrowband selectivity. The filter is terminated with a tank which transforms to 330Ω. The interstage filter is a ceramic type which doesn't contribute to system selectivity, but does suppress wideband noise and stray signal pickup. In wideband 10.7MHz IFs the input filter can also be ceramic, directly connected to Pin 16.

In some products it may be impractical to utilize shielding, but this mechanism may be appropriate to 10.7MHz and 21.4MHz IF. One of the benefits of low current is lower radiated field strength, but lower does not mean non-existent. A spectrum analyzer with an active probe will clearly show IF energy with the probe held in the proximity of the second limiter output or quadrature coil. No specific recommendations are provided, but mechanical shielding should be considered if layout, bypass, and input impedance reduction do not solve a stubborn instability.

The final stability consideration is phase shift. The phase shift of the limiters is very low, but there is phase shift contribution from the quadrature tank and the filters. Most filters demonstrate a large phase shift across their passband (especially at the edges). If the quadrature detector is tuned to the edge of the filter passband, the combined filter and quadrature phase shift can aggravate stability. This is not usually a problem, but should be kept in mind.

Quadrature Detector

Figure 7 shows an equivalent circuit of the SA624 quadrature detector. It is a multiplier cell similar to a mixer stage. Instead of mixing two different frequencies, it mixes two signals of common frequency but different phase. Internal to the device, a constant amplitude (limited) signal is differentially applied to the lower port of the multiplier. The same signal is applied single-ended to an external capacitor at Pin 9. There is a 90° phase shift across the plates of this capacitor, with the phase shifted signal applied to the upper port of the multiplier at Pin 8. A quadrature tank (parallel L/C network) permits frequency selective phase shifting at the IF frequency. This quadrature tank must be returned to ground through a DC blocking capacitor.

The loaded Q of the quadrature tank impacts three fundamental aspects of the detector: Distortion, maximum modulated peak deviation, and audio output amplitude. Typical quadrature curves are illustrated in Figure 12. The phase angle translates to a shift in the multiplier output voltage.

Thus a small deviation gives a large output with a high Q tank. However, as the deviation from resonance increases, the non-linearity of the curve increases (distortion), and, with too much deviation, the signal will be outside the quadrature region (limiting the peak deviation which can be demodulated). If the same peak deviation is applied to a lower Q tank, the deviation will remain in a region of the curve which is more linear (less distortion), but creates a smaller phase angle (smaller output amplitude). Thus the Q of the quadrature tank must be tailored to the design. Basic equations and an example for determining Q are shown below. This explanation includes first-order effects only.

Frequency Discriminator Design Equations for SA624

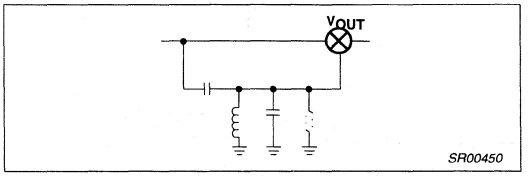


Figure 11.

$$V_O = \frac{C_S}{C_P + C_S} \bullet \frac{1}{1 + \frac{\omega_1}{Q_1 S} + \left(\frac{\omega_1}{S}\right)^2} \bullet V_{IN} \quad (1a)$$

$$\text{where } \omega_1 = \frac{1}{\sqrt{L(C_P + C_S)}} \quad (1b)$$

$$Q_1 = R\,(C_P + C_S)\,\omega_1 \quad (1c)$$

From the above equation, the phase shift between nodes 1 and 2, or the phase across C_S will be:

$$\phi = \angle V_O - \angle V_{IN} = t_g^{-1}\left[\frac{\frac{\omega_1}{Q_1\omega}}{1-\left(\frac{\omega_1}{\omega}\right)^2}\right] \quad (2)$$

Figure 12 is the plot of ϕ vs. $\left(\frac{\omega}{\omega_1}\right)$

It is notable that at $\omega = \omega_1$, the phase shift is $\frac{\pi}{2}$ and the response is close to a straight line with a slope of $\frac{\Delta\phi}{\Delta\omega} = \frac{2Q_1}{\omega_1}$

The signal V_O would have a phase shift of $\left[\frac{\pi}{2} - \frac{2Q_1}{\omega_1}\omega\right]$ with respect to the V_{IN}.

If $V_{IN} = A \sin \omega t \Rightarrow V_O = A$ (3)

$$\sin\left[\omega t + \frac{\pi}{2} - \frac{2Q_1}{\omega_1}\omega\right]$$

Multiplying the two signals in the mixer, and low pass filtering yields:

$V_{IN} \bullet V_O = A^2 \sin \omega t$ (4)

$$\sin\left[\omega t + \frac{\pi}{2} - \frac{2Q_1}{\omega_1}\omega\right]$$

after low pass filtering

$$\Rightarrow V_{OUT} = \frac{1}{2}A^2 \cos\left[\frac{\pi}{2} - \frac{2Q_1}{\omega_1}\omega\right] \quad (5)$$

$$= \frac{1}{2}A^2 \sin\left(\frac{2Q_1}{\omega_1}\right)\omega$$

$$V_{OUT} \propto 2Q_1\frac{\omega_1}{\omega} = \left[2Q_1\left(\frac{\omega_1 + \Delta\omega}{\omega_1}\right)\right] \quad (6)$$

For $\frac{2Q_1\omega}{\omega_1} << \frac{\pi}{2}$

Which is discriminated FM output. (Note that $\Delta\omega$ is the deviation frequency from the carrier ω_1.

Ref. Krauss, Raab, Bastian; Solid State Radio Eng.; Wiley, 1980, p. 311. Example: At 455kHz IF, with ±5kHz FM deviation. The maximum normalized frequency will be

$$\frac{455 \pm 5\text{kHz}}{455} = 1.010 \text{ or } 0.990$$

Go to the f vs. normalized frequency curves (Figure 12) and draw a vertical straight line at $\frac{\omega}{\omega_1} = 1.01$.

The curves with Q = 100, Q = 40 are not linear, but Q = 20 and less shows better linearity for this application. Too small Q decreases the amplitude of the discriminated FM signal. (Eq. 6) $\Rightarrow$ Choose a Q = 20

The internal R of the 624 is 40k. From Eq. 1c, and then 1b, it results that

$C_P + C_S = 174\text{pF}$ and $L = 0.7\text{mH}$.

A more exact analysis including the source resistance of the previous stage shows that there is a series and a parallel resonance in the phase detector tank. To make the parallel and series resonances close, and to get maximum attenuation of higher harmonics at 455kHz IF, we have found that a $C_S = 10\text{pF}$ and $C_P = 164\text{pF}$ (commercial values of 150pF or 180pF may be practical), will give the best results. A variable inductor which can be adjusted around 0.7mH should be chosen and optimized for minimum distortion. (For 10.7MHz, a value of $C_S = 1\text{pF}$ is recommended.)

Audio Outputs

Two audio outputs are provided. Both are PNP current-to-voltage converters with 55kΩ nominal internal loads. The unmuted output is always active to permit the use of signaling tones in systems such as cellular radio. The other output can be muted with 70dB typical attenuation. The two outputs have an internal 180° phase difference.

The nominal frequency response of the audio outputs is 300kHz. this response can be increased with the addition of external resistors from the output pins to ground in parallel with the internal 55k resistors, thus lowering the output time constant. Singe the output structure is a current-to-voltage converter (current is driven into the resistance, creating a voltage drop), adding external parallel resistance also has the effect of lowering the output audio amplitude and DC level.

This technique of audio bandwidth expansion can be effective in many applications such as SCA receivers and data transceivers. Because the two outputs have a 180° phase relationship, FSK demodulation can be accomplished by applying the two output differentially across the inputs of an op amp or comparator. Once the threshold of the reference frequency (or "no-signal" condition) has been established, the two outputs will shift in opposite directions (higher or lower output voltage) as the input frequency shifts. The output of the comparator will be logic output. The choice of op amp or comparator will depend on the data rate. With high IF frequency (10MHz and above), and wide IF bandwidth (L/C filters) data rates in excess of 4Mbaud are possible.

RSSI

The "received signal strength indicator", or RSSI, of the SA624 demonstrates monotonic logarithmic output over a range of 90dB. The signal strength output is derived from the summed stage currents in the limiting amplifiers. It is essentially independent of the IF frequency. Thus, unfiltered signals at the limiter inputs, spurious products, or regenerated signals will manifest themselves as RSSI outputs. An RSSI output of greater than 250mV with no signal (or a very small signal) applied, is an indication of possible regeneration or oscillation.

In order to achieve optimum RSSI linearity, there must be a 12dB insertion loss between the first and second limiting amplifiers. With a typical 455kHz ceramic filter, there is a nominal 4dB insertion loss in the filter. An additional 6dB is lost in the interface between the filter and the input of the second limiter. A small amount of additional loss must be introduced with a typical ceramic filter. In the test circuit used for cellular radio applications (Figure 5) the optimum linearity was achieved with a 5.1kΩ resistor from the output of the first limiter (Pin 14) to the input of the interstage filter. With this resistor from Pin 14 to the filter, sensitivity of 0.25μV for 12dB SINAD was achieved. With the 3.6kΩ resistor, sensitivity was optimized at 0.22μV for 12dB SINAD with minor change in the RSSI linearity.

Any application which requires optimized RSSI linearity, such as spectrum analyzers, cellular radio, and certain types of telemetry,

will require careful attention to limiter interstage component selection. This will be especially true with high IF frequencies which require insertion loss or impedance reduction for stability.

At low frequencies the RSSI makes an excellent logarithmic AC voltmeter.

For data applications the RSSI is effective as an amplitude shift keyed (ASK) data slicer. If a comparator is applied to the RSSI and the threshold set slightly above the no signal level, when an in-band signal is received the comparator will be sliced. Unlike FSK demodulation, the maximum data rate is somewhat limited. An internal capacitor limits the RSSI frequency response to about 100kHz. At high data rates the rise and fall times will not be symmetrical.

The RSSI output is a current-to-voltage converter similar to the audio outputs. However, an external resistor is required. With a 91kΩ resistor, the output characteristic is 0.5V for a 10dB change in the input amplitude.

Additional Circuitry

Internal to the SA624 are voltage and current regulators which have been temperature compensated to maintain the performance of the device over a wide temperature range. These regulators are not accessible to the user.

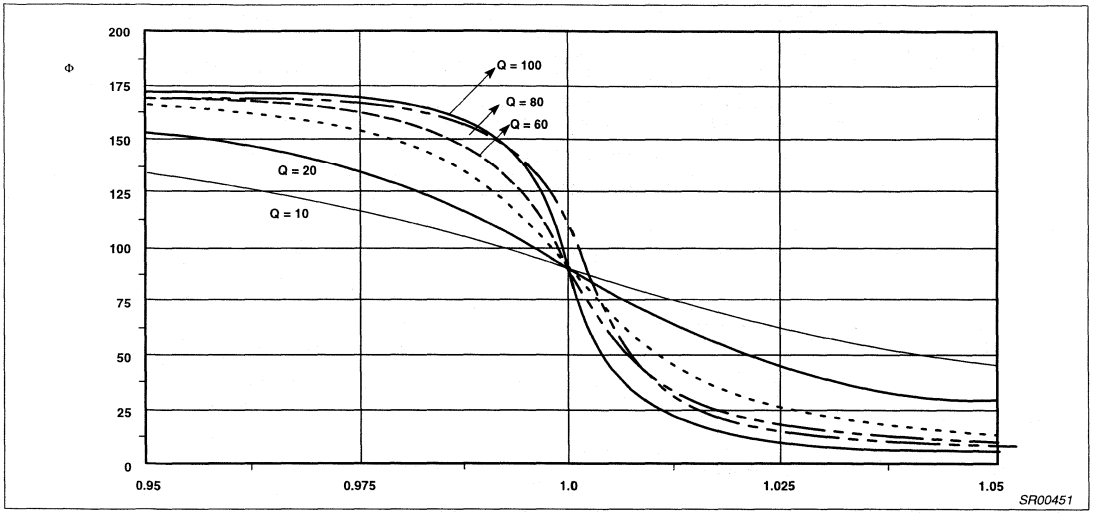


Figure 12. Phase vs Normalized IF Frequency $\frac{\omega}{\omega_1} = 1 + \frac{\Delta\omega}{\omega_1}$

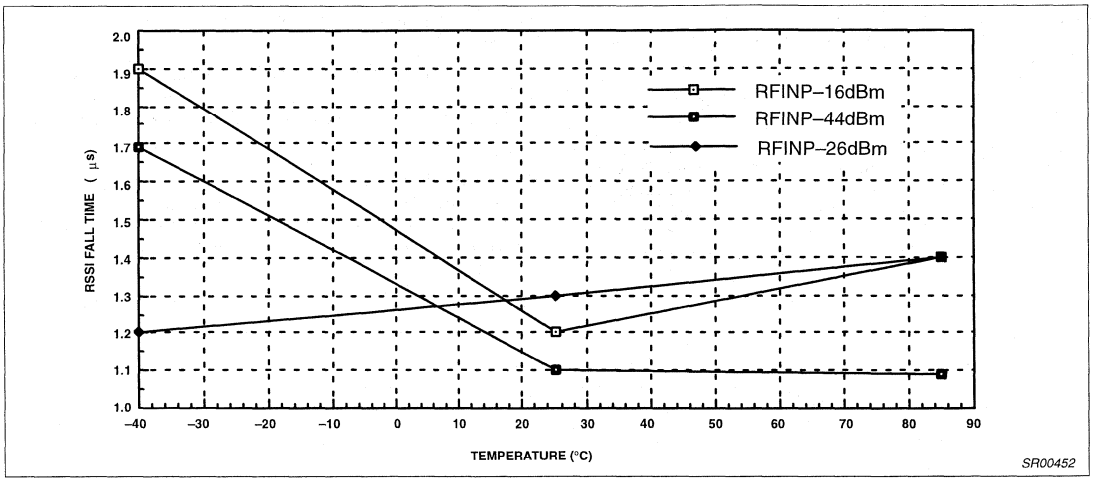


Figure 13. SA624 Rise Time 455kHz IF Frequency

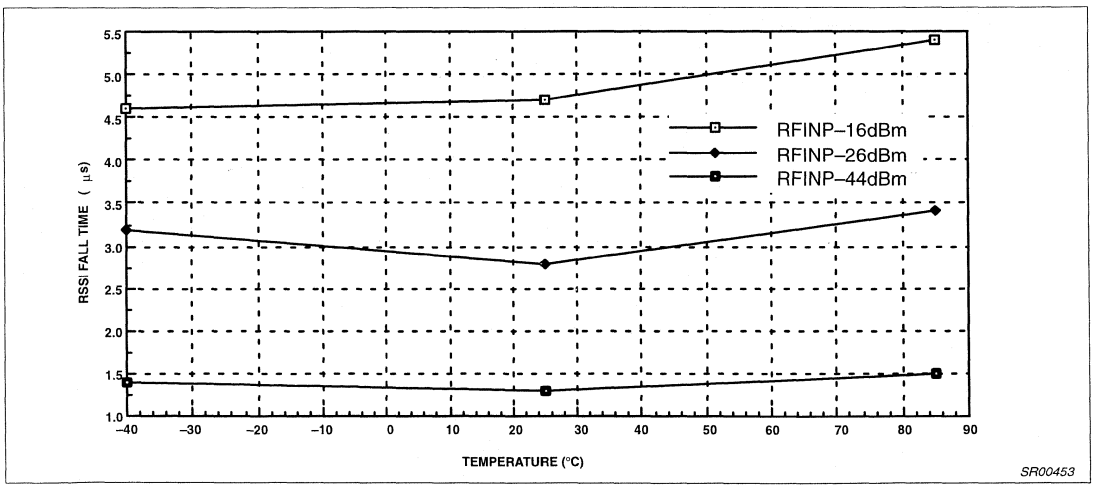


Figure 14. SA624 Fall Time 455kHz IF Frequency

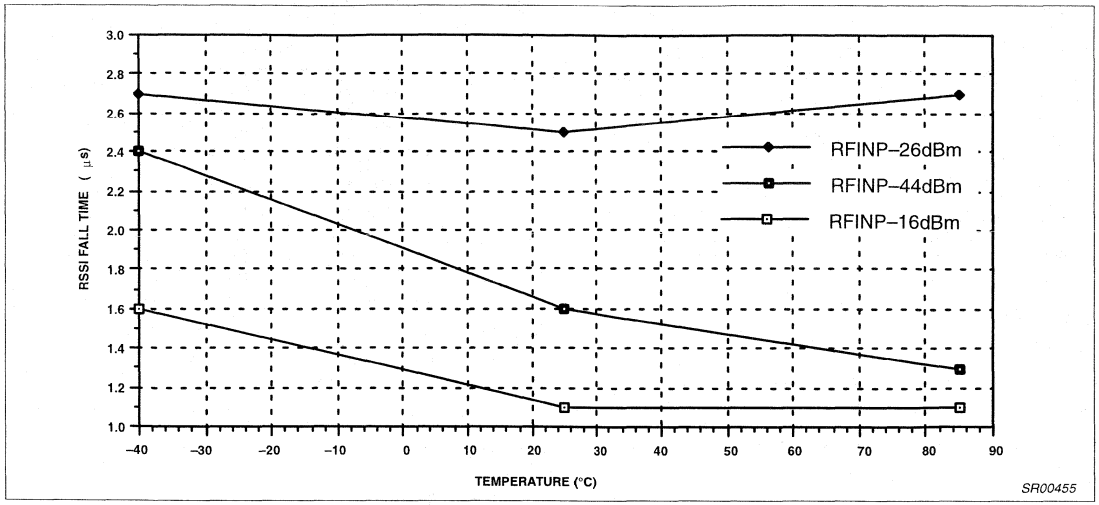


Figure 15. SA624 Rise Time 10.7MHz IF Frequency

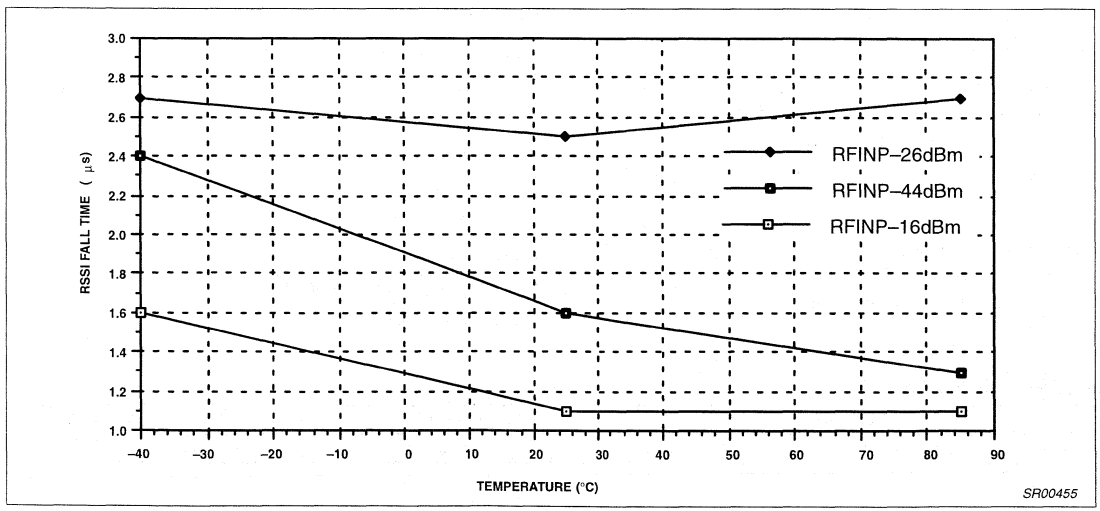


Figure 16. SA624 Fall Time 10.7MHz IF Frequency

High performance low power mixer FM IF system with high-speed RSSI

SA625

DESCRIPTION

The SA625 is pin-to-pin compatible with the SA605, but has faster RSSI rise and fall times. The SA625 is a high performance monolithic low-power FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic received signal strength indicator (RSSI) with fast rise and fall time, and voltage regulator. The SA625 combines the functions of Signetics' SA602A and SA624. The SA625 is available in 20-lead SSOP (shrink small outline package).

For additional technical information please refer to application notes AN1994, 1995 and 1996, which include example application diagrams, a complete overview of the product and artwork for reference.

FEATURES

- Fast RSSI rise and fall times
- Low power consumption: 5.8mA typical at 6V
- Mixer input to >500MHz
- Mixer conversion power gain of 13dB at 45MHz
- Mixer noise figure of 4.6dB at 45MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator to 1GHz local oscillator can be injected)
- 102dB of IF Amp/Limiter gain
- 25MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- Two audio outputs - muted and unmuted
- Low external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.22μV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone with RF at 45MHz and IF at 455kHz
- SA625 meets cellular radio specifications

PIN CONFIGURATION

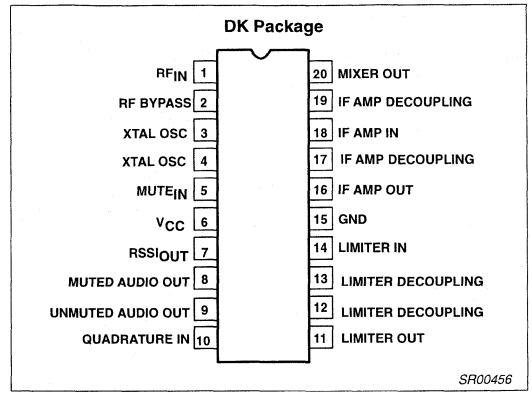


Figure 1. Pin Configuration

- ESD hardened

APPLICATIONS

- Digital cellular base stations
- High performance communications receivers
- Single conversion VHF/UHF receivers
- SCA receivers
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Wideband low current amplification
- Digital cordless telephones

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Shrink Small Outline Package (SSOP) (Surface-mount)	-40 to +85°C	SA625DK	SOT266-1

BLOCK DIAGRAM

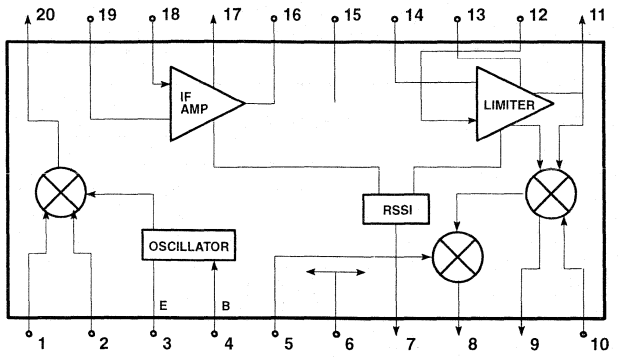


Figure 2. Block Diagram

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	9	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range SA625	-40 to +85	°C
θ_{JA}	Thermal impedance DK package	117	°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA625			
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		4.5		8.0	V
I_{CC}	DC current drain		4.55	5.8	6.75	mA
	Mute switch input threshold (ON)		1.7			V
	(OFF)				1.0	V

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +6V, unless otherwise stated. RF frequency = 45MHz + 14.5dBV RF input step-up; IF frequency = 455kHz; R17 = 5.1k; RF level = -45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 3. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS SA625 MIN	LIMITS SA625 TYP	LIMITS SA625 MAX	UNITS
Mixer/Osc section (ext LO = 300mV)						
f_{IN}	Input signal frequency			500		MHz
f_{OSC}	Crystal oscillator frequency			150		MHz
	Noise figure at 45MHz			5.0		dB
	Third-order input intercept point	f1 = 45.0; f2 = 45.06MHz		-10		dBm
	Conversion power gain	Matched 14.5dBV step-up	10	13	15	dB
		50Ω source		-1.7		dB
	RF input resistance	Single-ended input	3.0	4.7		kΩ
	RF input capacitance			3.5	4.0	pF
	Mixer output resistance	(Pin 20)	1.25	1.5		kΩ
IF section						
	IF amp gain	50Ω source		39.7		dB
	Limiter gain	50Ω source		62.5		dB
	Input limiting -3dB, R_{17} = 5.1k	Test at Pin 18		-113		dBm
	AM rejection	80% AM 1kHz	29	34	43	dB
	Audio level, R_{10} = 100k	15nF de-emphasis	80	150	260	mV_{RMS}
	Unmuted audio level, R_{11} = 100k	150pF de-emphasis		480		mV
	SINAD sensitivity	RF level -118dB		16		dB
THD	Total harmonic distortion		-34	-42		dB
S/N	Signal-to-noise ratio	No modulation for noise		73		dB
	IF RSSI output, R_9 = 100kΩ[1]	IF level = -118dBm	0	160	650	mV
		IF level = -68dBm	1.9	2.5	3.1	V
		IF level = -18dBm	4.0	4.8	5.6	V
	IF RSSI output rise time (10kHz pulse, no 455kHz filter) (no RSSI bypass capacitor)	IF frequency = 455kHz				
		RF level = -56dBm		1.2		µs
		RF level = -28dBm		1.2		µs
		IF frequency = 10.7MHz				
		RF level = -56dBm		1.2		µs
		RF level = -28dBm		1.1		µs
	IF RSSI output fall time (10kHz pulse, no 455kHz filter) (no RSSI bypass capacitor)	IF frequency = 455kHz				
		RF level = -56dBm		2.1		µs
		RF level = -28dBm		7.6		µs
		IF frequency = 10.7MHz				
		RF level = -56dBm		2.0		µs
		RF level = -28dBm		7.3		µs
	RSSI range	R_9 = 100kΩ Pin 16		90		dB
	RSSI accuracy	R_9 = 100kΩ Pin 16		±1.5		dB
	IF input impedance		1.40	1.6		kΩ
	IF output impedance		0.85	1.0		kΩ
	Limiter intput impedance		1.40	1.6		kΩ
	Limiter output impedance			300		Ω
	Limiter output level with no load			280		mV_{RMS}

AC ELECTRICAL CHARACTERISTICS(Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA625			
			MIN	TYP	MAX	
IF section (continued)						
	Unmuted audio output resistance			58		kΩ
	Muted audio output resistance			58		kΩ
RF/IF section (int LO)						
	Unmuted audio level	4.5V = V_{CC}, RF level = -27dBm		450		mV_{RMS}
	System RSSI output	4.5V = V_{CC}, RF level = -27dBm		4.3		V

NOTE:
1. The generator source impedance is 50Ω, but the SA625 input impedance at Pin 18 is 1500Ω. As a result, IF level refers to the actual signal that enters the SA625 input (Pin 8) which is about 21dB less than the "available power" at the generator.

CIRCUIT DESCRIPTION

The SA625 is an IF signal processing system suitable for second IF or single conversion systems with input frequency as high as 1GHz. The bandwidth of the IF amplifier is about 40MHz, with 39.7dB(v) of gain from a 50Ω source. The bandwidth of the limiter is about 28MHz with about 62.5dB(v) of gain from a 50Ω source. However, the gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 5dB, conversion gain of 13dB, and input third-order intercept of -10dBm. The oscillator will operate in excess of 1GHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

The output of the mixer is internally loaded with a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. To achieve optimum linearity of the log signal strength indicator, there must be a 12dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dB(v) insertion loss, a fixed or variable resistor can be added between the first IF output (Pin 16) and the interstage network.

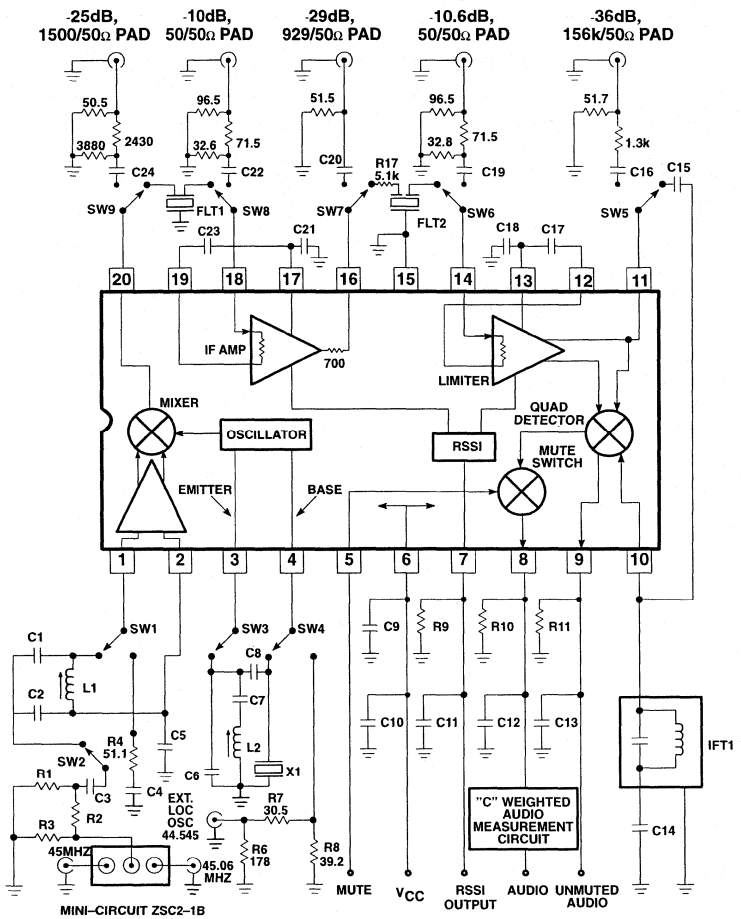
The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

Overall, the IF section has a gain of 90dB. For operation at intermediate frequencies greater than 455kHz, special care must be given to layout, termination, and interstage loss to avoid instability.

The demodulated output of the quadrature detector is available at two pins, one continuous and one with a mute switch. Signal attenuation with the mute activated is greater than 60dB. The mute input is very high impedance and is compatible with CMOS or TTL levels.

A log signal strength completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone.

NOTE: $dB(v) = 20\log V_{OUT}/V_{IN}$



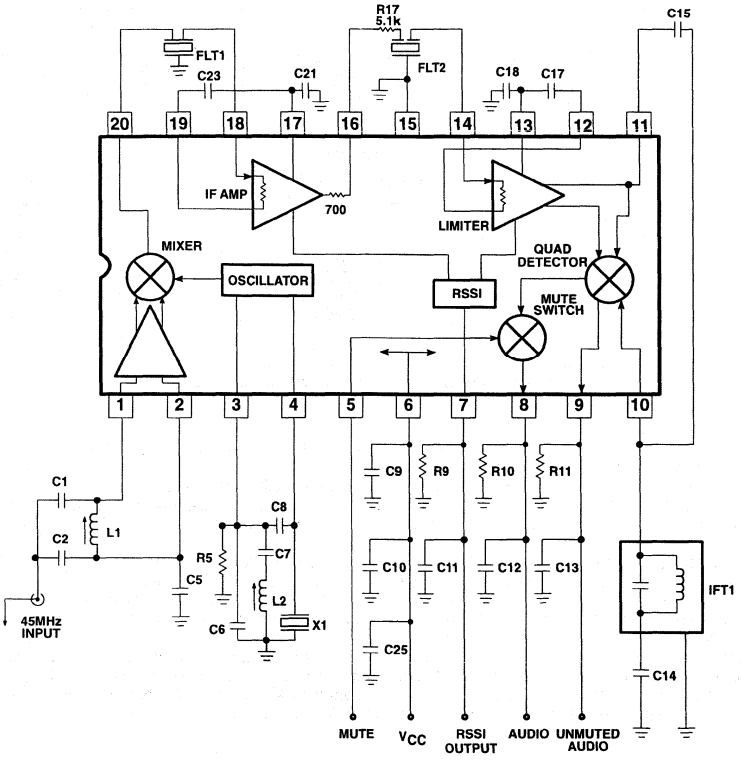
Automatic Test Circuit Component List

C1	100pF NPO Ceramic	C21	100nF ±10% Monolithic Ceramic
C2	390pF NPO Ceramic	C23	100nF ±10% Monolithic Ceramic
C5	100nF ±10% Monolithic Ceramic	C25	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic	Flt 1	Ceramic Filter Murata SFG455A3 or equiv
C7	1nF Ceramic	Flt 2	Ceramic Filter Murata SFG455A3 or equiv
C8	10.0pF NPO Ceramic	IFT 1	455kHz (Ce = 180pF) Toko RMC–2A6597H
C9	100nF ±10% Monolithic Ceramic	L1	147–160nH Coilcraft UNI–10/142–04J08S
C10	6.8μF Tantalum (minimum) *	L2	0.8μH nominal Toko 292CNS–T1038Z
C11	100nF ±10% Monolithic Ceramic	X1	44.545MHz Crystal ICM4712701
C12	15nF ±10% Ceramic	R9	100k ±1% 1/4W Metal Film
C13	150pF ±2% N1500 Ceramic	R17	5.1k ±5% 1/4W Carbon Composition
C14	100nF ±10% Monolithic Ceramic	R10	100k ±1% 1/4W Metal Film (optional)
C15	10pF NPO Ceramic	R11	100k ±1% 1/4W Metal Film (optional)
C17	100nF ±10% Monolithic Ceramic		
C18	100nF ±10% Monolithic Ceramic		

*NOTE: This value can be reduced when a battery is the power source.

SR00458

Figure 3. SA625 45MHz Test Circuit (Relays as shown)



Application Component List

C1	100pF NPO Ceramic
C2	390pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	6.8μF Tantalum (minimum) *
C11	100nF ±10% Monolithic Ceramic
C12	15nF ±10% Ceramic
C13	150pF ±2% N1500 Ceramic
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	455kHz (Ce = 180pF) Toko RMC–2A6597H
L1	147–160nH Coilcraft UNI–10/142–04J08S
L2	0.8μH nominal Toko 292CNS–T1038Z
X1	44.545MHz Crystal ICM4712701
R9	100k ±1% 1/4W Metal Film
R17	5.1k ±5% 1/4W Carbon Composition
R5	Not Used in Application Board (see Note 8)
R10	100k ±1% 1/4W Metal Film (optional)
R11	100k ±1% 1/4W Metal Film (optional)

*NOTE: This value can be reduced when a battery is the power source.

SR00459

Figure 4. SA625 45MHz Application Circuit

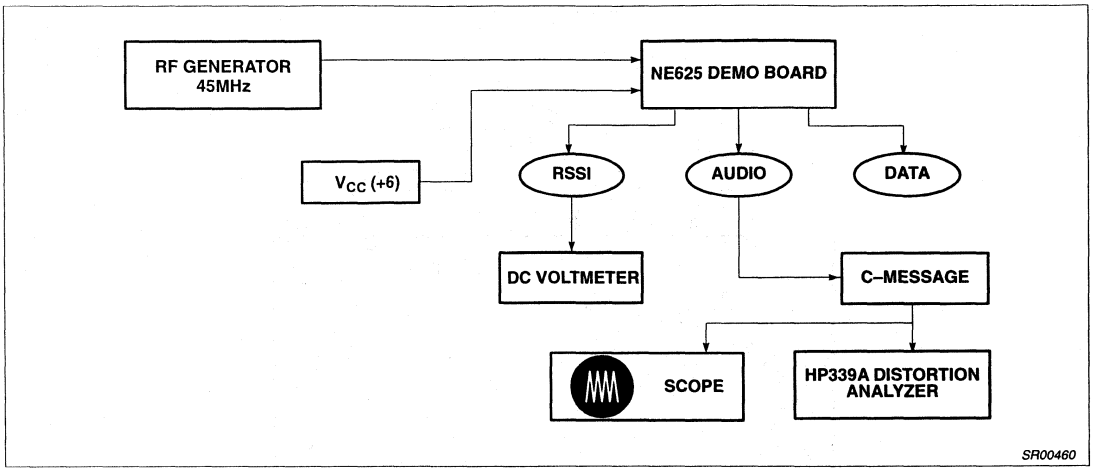


Figure 5. SA625 Application Circuit Test Set Up

NOTES:

1. C-message: The C-message filter has a peak gain of 100 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339 analyzer.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All of our specifications and testing are done with the more wideband filter.
3. RF generator: Set your RF generator at 45.000MHz, use a 1kHz modulation frequency and a 6kHz deviation if you use 16kHz filters, or 8kHz if you use 30kHz filters.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.22μV or -120dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 250mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10-15μF or higher value tantalum capacitor on the supply line is essential. A low frequency ESR screening test on this capacitor will ensure consistent good sensitivity in production. A 0.1μF bypass capacitor on the supply pin, and grounded near the 44.545MHz oscillator improves sensitivity by 2-3dB.
8. R5 can be used to bias the oscillator transistor at a higher current for operation above 45MHz. Recommended value is 22kΩ, but should not be below 10kΩ.

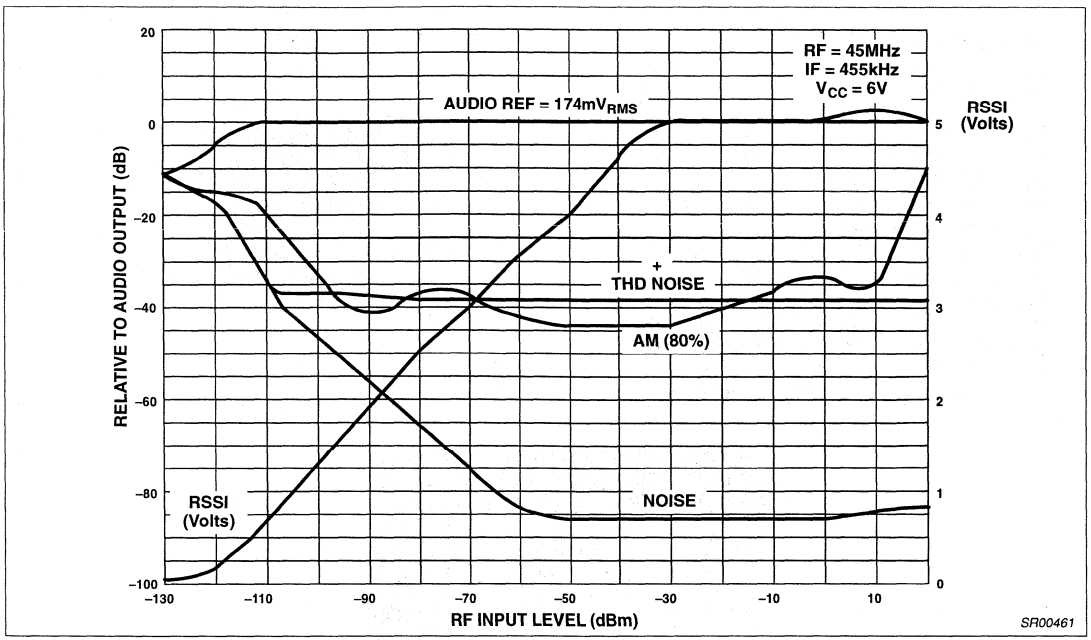


Figure 6. SA625 Application Board at 25°C

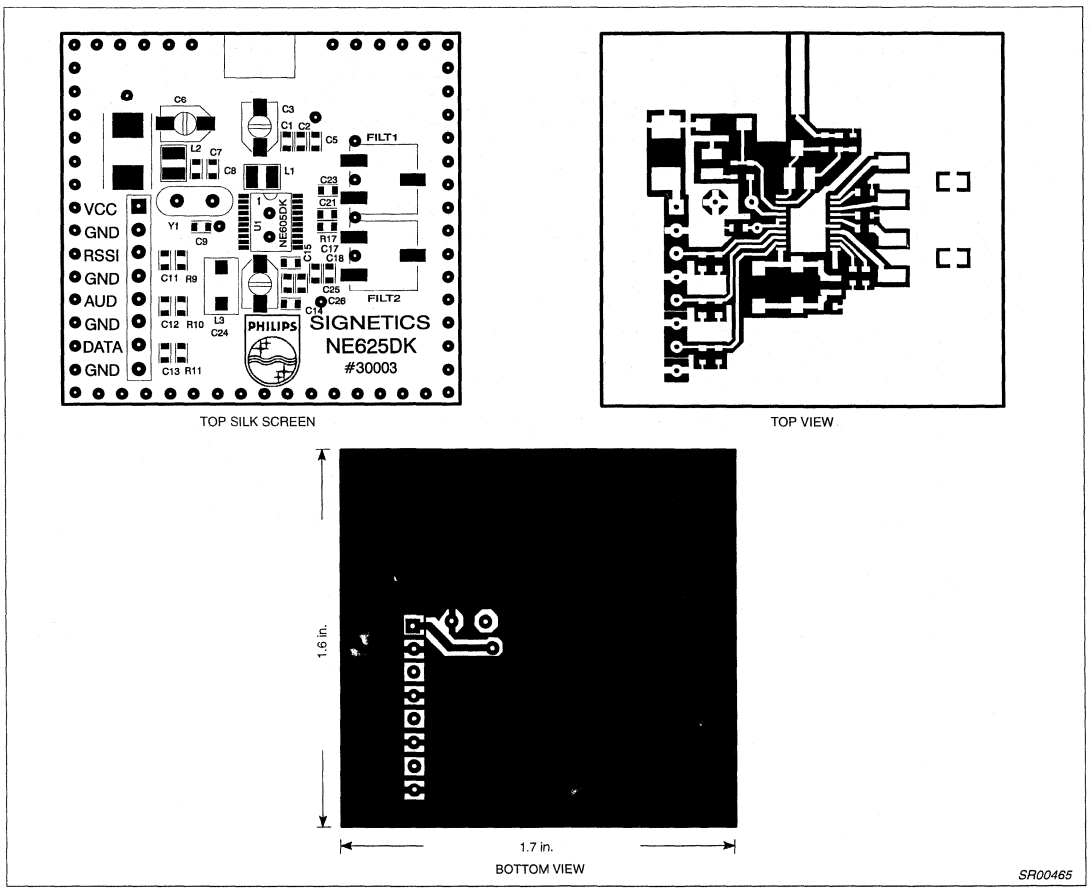


Figure 7. SA625 SSOP Demo-board Layout (Not Actual Size)

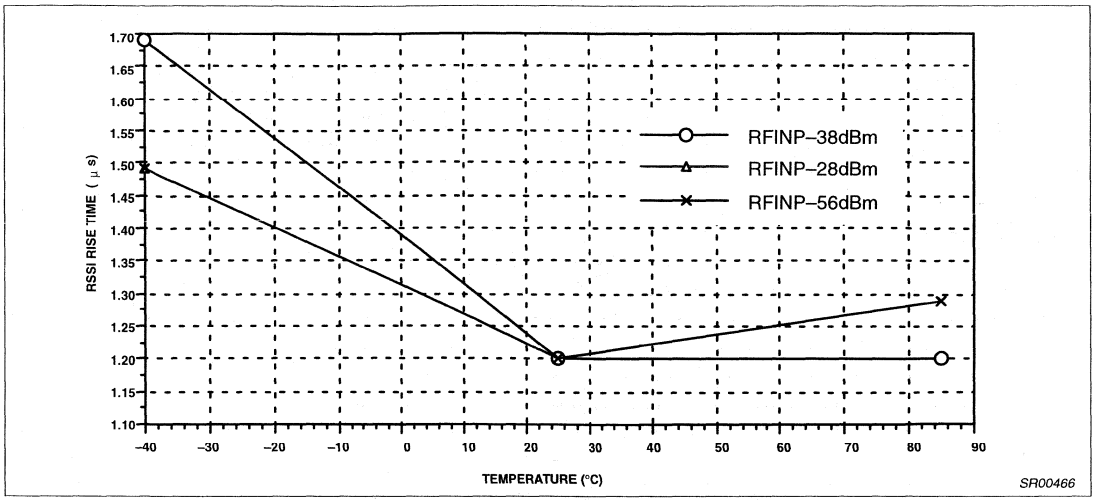


Figure 8. SA625 Rise Time 455kHz IF Frequency

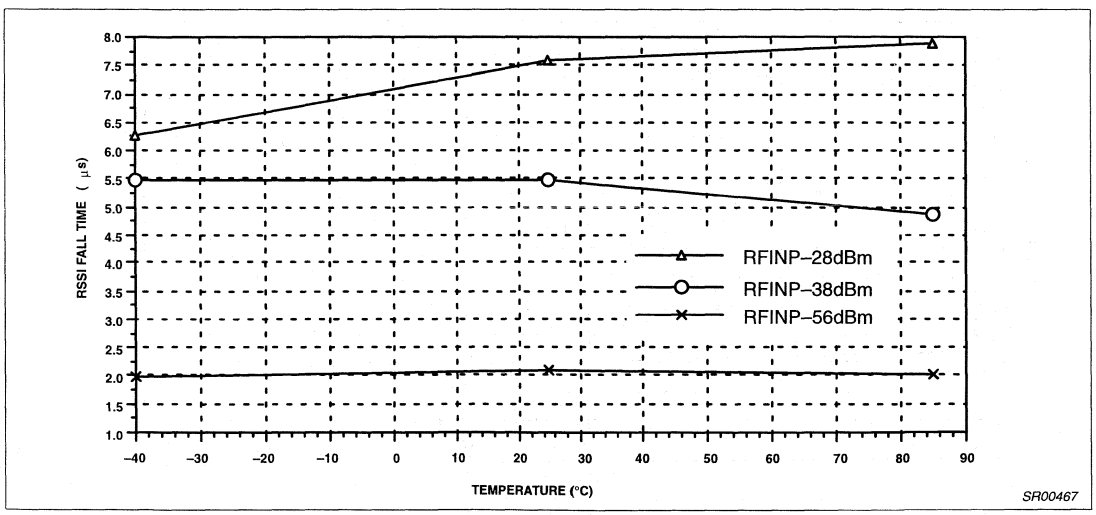


Figure 9. SA625 Fall Time 455kHz IF Frequency

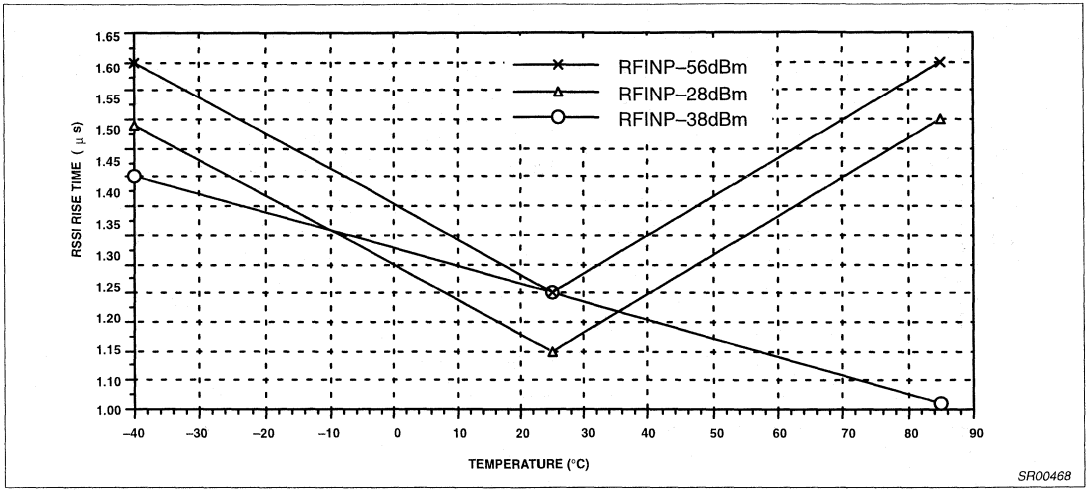


Figure 10. SA625 Rise Time 10.7MHz IF Frequency

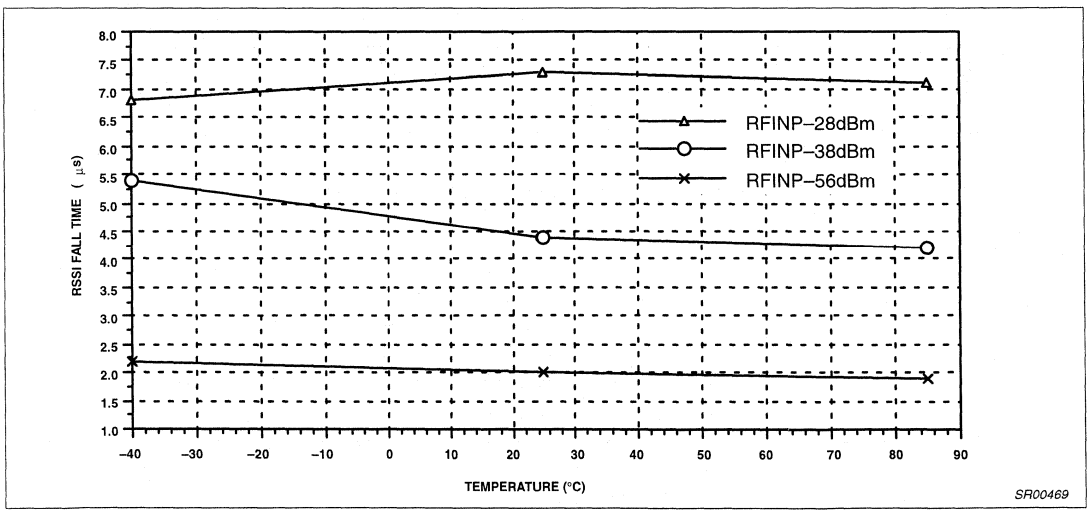


Figure 11. SA625 Fall Time 10.7MHz IF Frequency

Low voltage high performance mixer FM IF system with high-speed RSSI

SA626

DESCRIPTION

The SA626 is a low-voltage high performance monolithic FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, high speed logarithmic received signal strength indicator (RSSI), voltage regulator and audio and fast RSSI op amps. The SA626 is available in 20-lead SOL (surface-mounted small outline large package) and 20-lead SSOP (shrink small outline package).

The SA626 was designed for high bandwidth portable communication applications and will function down to 2.7V. The RF section is similar to the famous NE605. The audio and RSSI outputs have amplifiers. The RSSI output has access to the feedback pin. This enables the designer to level adjust the outputs or add filtering.

SA626 incorporates a power down mode which powers down the device when Pin 8 is low. Power down logic levels are CMOS and TTL compatible with high input impedance.

APPLICATIONS

- Digital cordless telephones
- Digital cellular telephones
- Digital cellular base stations
- Portable high performance communications receivers
- Single conversion VHF/UHF receivers
- SCA receivers
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Wideband low current amplification

FEATURES

- Fast RSSI rise and fall times
- Low power consumption: 6.5mA typ at 3V
- Power down mode (I_{CC} = 200µA)

PIN CONFIGURATION

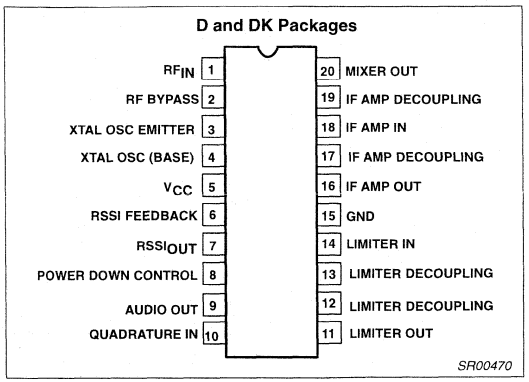


Figure 1. Pin Configuration

- Mixer input to >500MHz
- Mixer conversion power gain of 11dB at 240MHz
- Mixer noise figure of 14dB at 240MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator to 1GHz, local oscillator can be injected)
- 92dB of IF Amp/Limiter power gain
- 25MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- Audio output internal buffer
- RSSI output internal buffer
- Internal op amps with rail-to-rail outputs
- 10.7MHz filter matching (330Ω) reduces external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.54µV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone with RF at 240MHz and IF at 10.7MHz
- SA626 meets cellular radio specifications
- ESD hardened

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Small Outline Large (SOL) package (Surface-mount)	-40 to +85°C	SA626D	SOT163-1
20-Pin Plastic Shrink Small Outline Package (Surface-mount)	-40 to +85°C	SA626DK	SOT266-1

BLOCK DIAGRAM

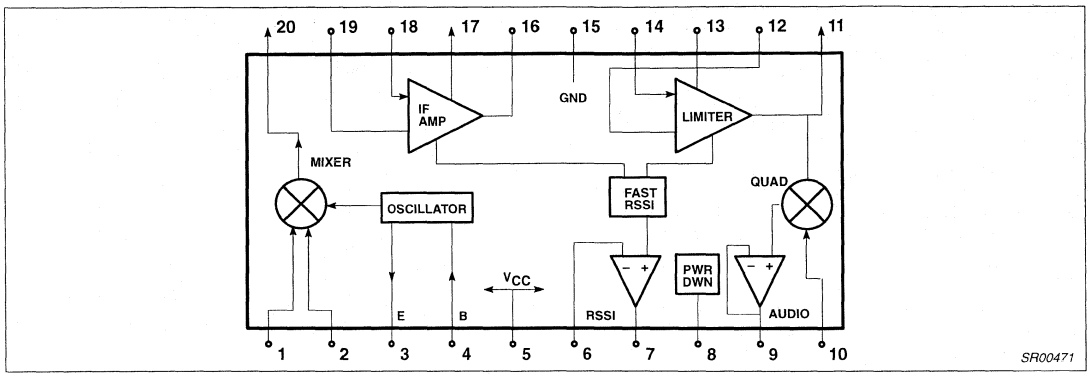


Figure 2. Block Diagram

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		RATING	UNITS
V_{CC}	Single supply voltage		0.3 to 7	V
V_{IN}	Voltage applied to any other pin		–0.3 to (V_{CC}+0.3)	V
T_{STG}	Storage temperature range		-65 to +150	°C
T_A	Operating ambient temperature range SA626		–40 to +85	°C
θ_{JA}	Thermal impedance	D package	90	°C/W
		DK package	117	°C/W

DC ELECTRICAL CHARACTERISTICS

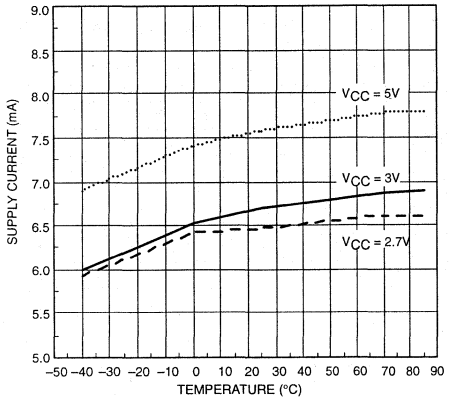
V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA626			
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		2.7	3.0	5.5	V
I_{CC}	DC current drain	Pin 8 = HIGH	5.5	6.5	7.5	mA
I_{CC}	Standby	Pin 8 = LOW		0.2	0.5	mA
	Input current	Pin 8 LOW	–10		10	µA
		Pin 8 HIGH	–10		10	µA
	Input level	Pin 8 LOW	0		0.3V_{CC}	V
		Pin 8 HIGH	0.7V_{CC}		V_{CC}	V
t_{ON}	Power up time	RSSI valid (10% to 90%)		10		µs
t_{OFF}	Power down time	RSSI invalid (90% to 10%)		5		µs

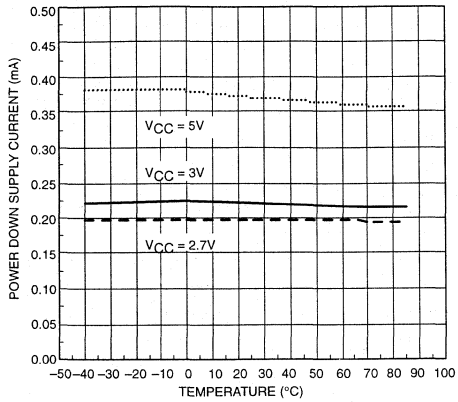
AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +3V, unless otherwise stated. RF frequency = 240.05MHz + 14.5dBV RF input step-up; IF frequency = 10.7MHz; RF level = -68dBm; FM modulation = 1kHz with ±125kHz peak deviation. Audio output with C-message weighted filter and de-emphasis filter. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characteristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

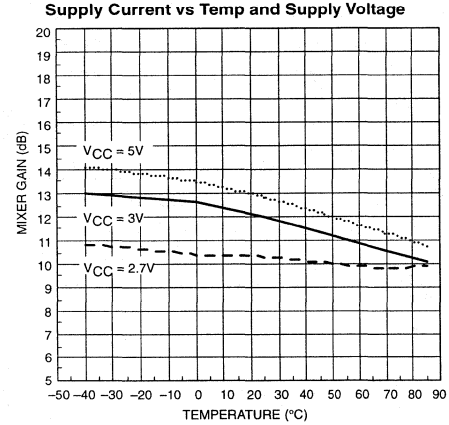
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS SA626			UNITS
			MIN	TYP	MAX	
Mixer/Osc section (ext LO = 160mV$_{RMS}$)						
f_{IN}	Input signal frequency			500		MHz
f_{OSC}	External oscillator (buffer)			500		MHz
	Noise figure at 240MHz			14		dB
	Third-order input intercept point	Matched f1=240.05; f2=240.35MHz		-16		dBm
	Conversion power gain	Matched 14.5dBV step-up	8	11	14	dB
	RF input resistance	Single-ended input		700		Ω
	RF input capacitance			3.5		pF
	Mixer output resistance	(Pin 20)		330		Ω
IF section						
	IF amp power gain			38		dB
	Limiter amp power gain			54		dB
	Input limiting -3dB	Test at Pin 18		–105		dBm
	AM rejection	80% AM 1kHz		50		dB
	Audio level	Unity gain	120	160	200	mV$_{RMS}$
	Audio DC level	Pin 9, no signal		1.0		V
	SINAD sensitivity	IF level = -111dBm		16		dB
THD	Total harmonic distortion			-43	–38	dB
S/N	Signal-to-noise ratio	No modulation for noise		60		dB
	IF RSSI output with buffer	IF level = -118dBm		0.2	0.5	V
		IF level = -68dBm	0.3	0.6	1.0	V
		IF level = -10dBm	0.9	1.3	1.8	V
	IF RSSI output rise time	IF frequency = 10.7MHz				
	(10kHz pulse, no 10.7MHz filter)	RF level = -56dBm		1.2		µs
	(no RSSI bypass capacitor)	RF level = -28dBm		1.1		µs
	IF RSSI output fall time	IF frequency = 10.7MHz				
	(10kHz pulse, no 10.7MHz filter)	RF level = -56dBm		2.0		µs
	(no RSSI bypass capacitor)	RF level = -28dBm		7.3		µs
	RSSI range			90		dB
	RSSI accuracy			±1.5		dB
	IF input impedance			330		Ω
	IF output impedance			330		Ω
	Limiter input impedance			330		Ω
	Limiter output impedance			300		Ω
	Limiter output level with no load			130		mV$_{RMS}$
RF/IF section (int LO)						
	Audio level	RF level = -10dBm		160		mV$_{RMS}$
	System RSSI output	RF level = -10dBm		1.4		V
	System SINAD	RF level = -106dBm		12		dB



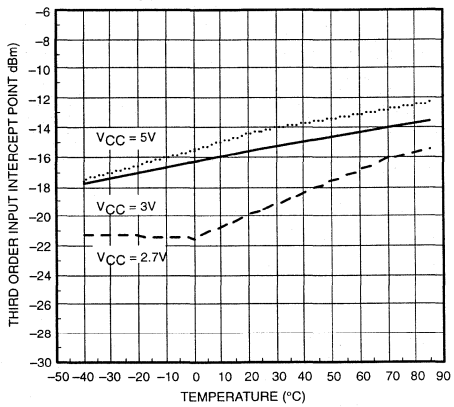
Supply Current vs Temp and Supply Voltage



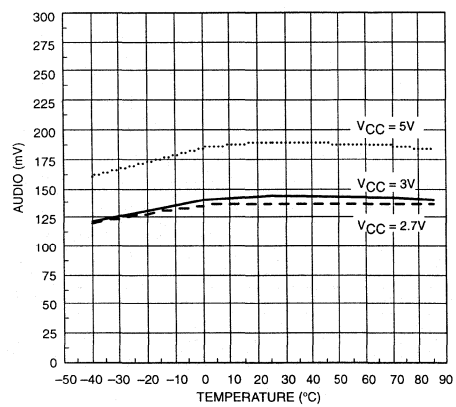
Power Down Supply Current vs Temp and Supply Voltage



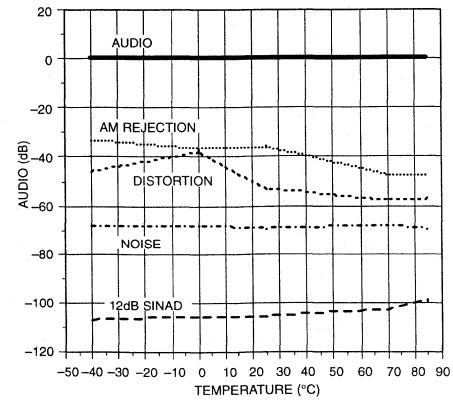
Mixer Power Gain vs Temperature and Supply Voltage



Third Order Input Intercept Point vs Temp and Supply Voltage



Audio Output Level vs. Temp and Supply Voltage



12dB SINAD and Relative Audio, THD, Noise and AM Rejection for VCC = 3V vs Temperature RF = 240MHz, Level = –68dBm, Deviation = 125kHz SR00472

Figure 3. Performance Characteristics

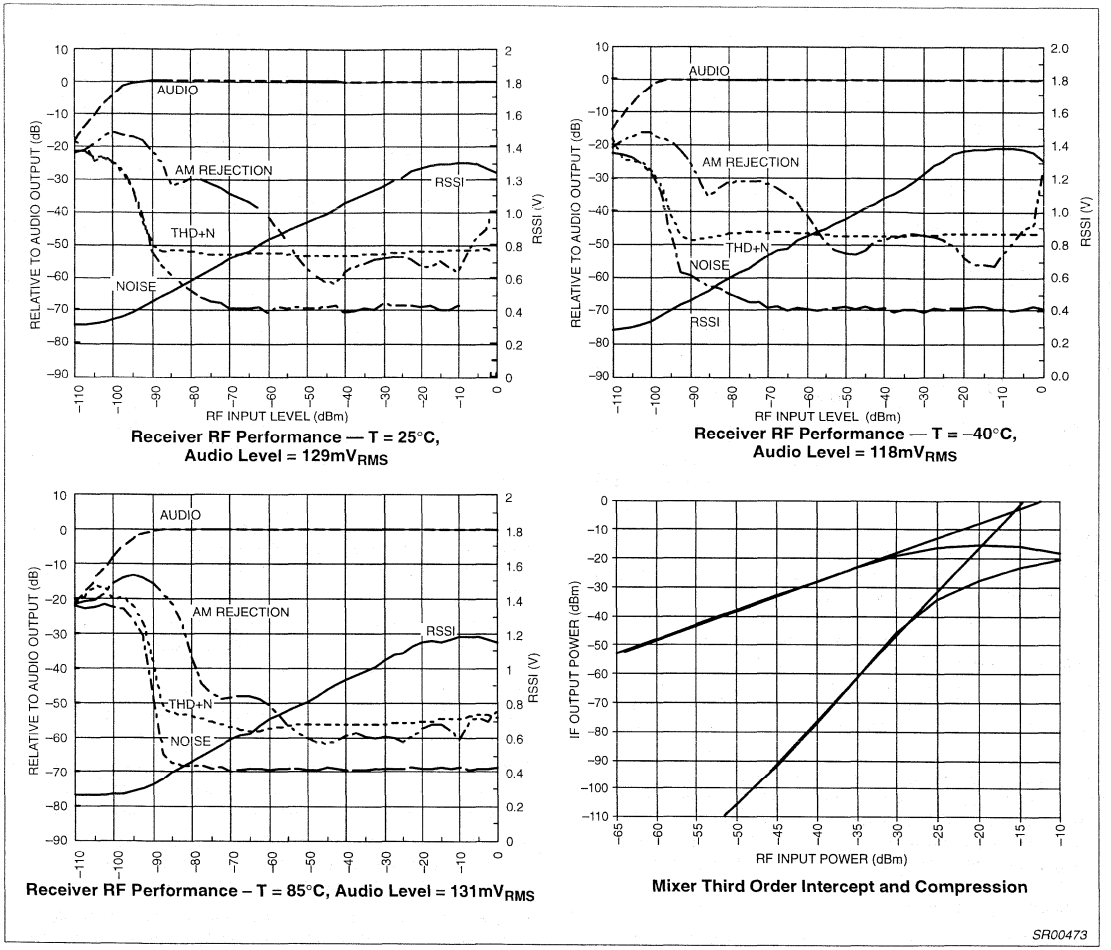
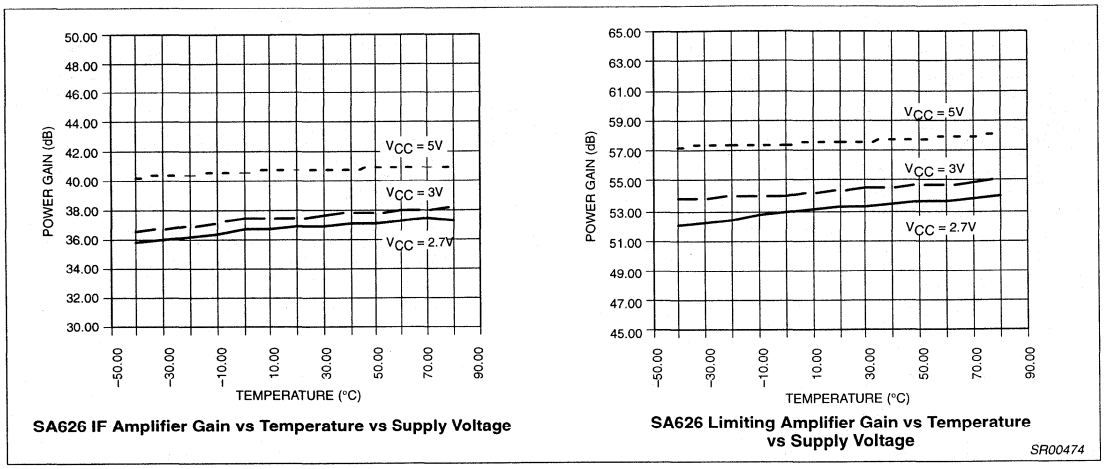


Figure 4. Performance Characteristics



SA626 IF Amplifier Gain vs Temperature vs Supply Voltage

SA626 Limiting Amplifier Gain vs Temperature vs Supply Voltage

SR00474

Figure 5. Performance Characteristics

CIRCUIT DESCRIPTION

The SA626 is an IF signal processing system suitable for second IF or single conversion systems with input frequency as high as 1GHz. The bandwidth of the IF amplifier is about 40MHz, with 38dB of power gain from a 50Ω source. The bandwidth of the limiter is about 28MHz with about 54dB of power gain from a 50Ω source. However, the gain/bandwidth distribution is optimized for 10.7MHz, 330Ω source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types, such as cordless and cellular hand-held phones.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 14dB, conversion power gain of 11dB, and input third-order intercept of -16dBm. The oscillator will operate in excess of 1GHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

The output of the mixer is internally loaded with a 330Ω resistor permitting direct connection to a 10.7MHz ceramic filter. The input resistance of the limiting IF amplifiers is also 330Ω. With most 10.7MHz ceramic filters and many crystal filters, no impedance matching network is necessary. To achieve optimum linearity of the log signal strength indicator, there must be a 3dB insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 3dB insertion loss, a fixed or variable resistor can be added between the first IF output (Pin 16) and the interstage network.

The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

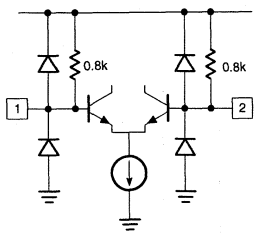
Overall, the IF section has a power gain of 92dB. For operation at intermediate frequency at 10.7MHz. Special care must be given to layout, termination, and interstage loss to avoid instability.

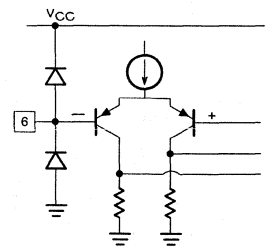
The demodulated output of the quadrature drives an internal op amp. This op amp is configured as a unity gain buffer. It can drive an AC load as low as 5kΩ with a rail-to-rail output.

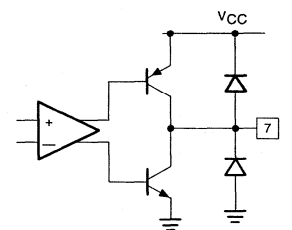
A log signal strength indicator completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone, and RCR-28 cordless telephone. This signal drives an internal op amp. The op amp is capable of rail-to-rail output. It can be used for gain, filtering, or 2nd-order temperature compensation of the RSSI, if needed.

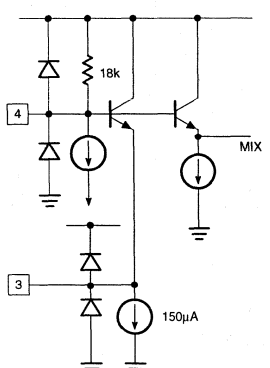
PIN FUNCTIONS

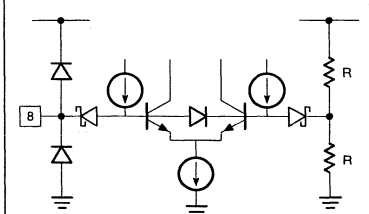
PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT	PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
1	RF IN	+1.07		6	RSSI FEEDBACK	+0.20	
2	RF BYPASS	+1.07		7	RSSI OUT	+0.20	
3	XTAL OSC	+1.57		8	POWER DOWN	+2.75	
4	XTAL OSC	+2.32		9	AUDIO OUT	+1.09	
5	V_{CC}	+3.00		10	QUAD. IN	+3.00	

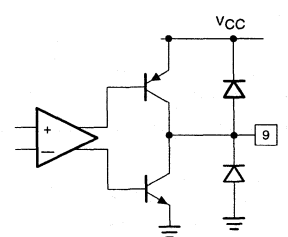


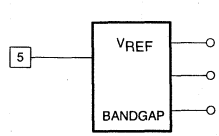


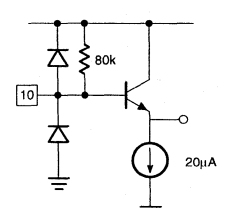












SR00475

Figure 6. Pin Functions

PIN FUNCTIONS (continued)

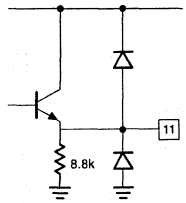
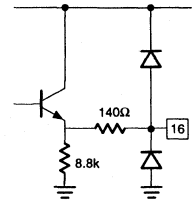
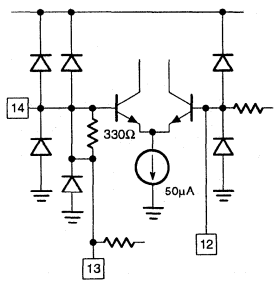
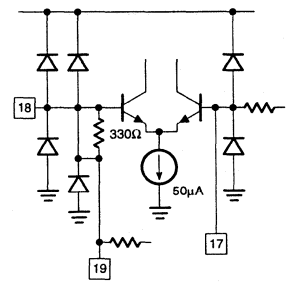
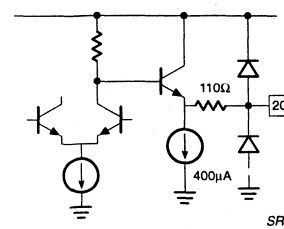
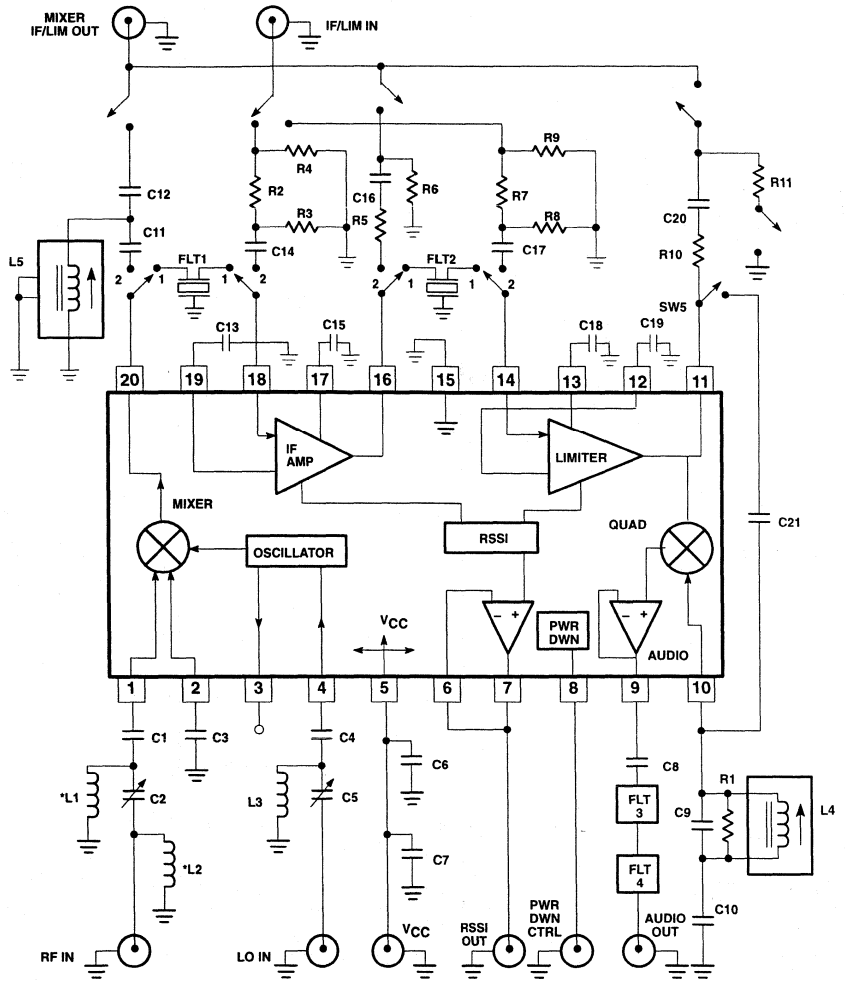
PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT	PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
11	LIMITER OUT	+1.35		16	IF AMP OUT	+1.22	
12	LIMITER DECOUP	+1.23		17	IF AMP DECOUP	+1.22	
13	LIMITER COUPLING	+1.23		18	IF AMP IN	+1.22	
14	LIMITER IN	+1.23		19	IF AMP DECOUP	+1.22	
15	GND	0		20	MIXER OUT	+1.03	

Figure 7. Pin Functions (cont.)



Automatic Test Circuit Component List

R1	8.2kΩ select	C1	0.1μF	C12	160pF select	L1	150nH select for input match
R2	6.42kΩ	C2	1–5pF select for input match	C13	1000pF	L2	22nH select for input match
R3	347.8Ω	C3	0.1μF	C14	0.1μF	L3	47nH select for input match
R4	49.9Ω	C4	0.1μF	C15	1000pF	L4	5.6μH select for input match
R5	1kΩ	C5	1–5pF select for input match	C16	0.1μF	L5	1.27–2.25μH select for mixer output match
R6	49.9Ω	C6	100pF	C17	0.1μF		
R7	6.42kΩ	*C7	6.8μF 10V	C18	1000pF	FLT1	10.7MHz (Murata SFE10.7MA5-A)
R8	347.8Ω	C8	1μF	C19	1000pF	FLT2	10.7MHz (Murata SFE10.7MA5-A)
R9	49.9Ω	C9	39pF select	C20	0.1μF	FLT3	"C" message weighted
R10	1kΩ	C10	0.1μF	C21	1pF	FLT4	Active de-emphasis
R11	49.9Ω	C11	0.1μF				

*NOTE: This value can be reduced when a battery is the power source.

SR00477

Figure 8. SA626 240.5MHz (RF) / 10.7MHz (IF) Test Circuit

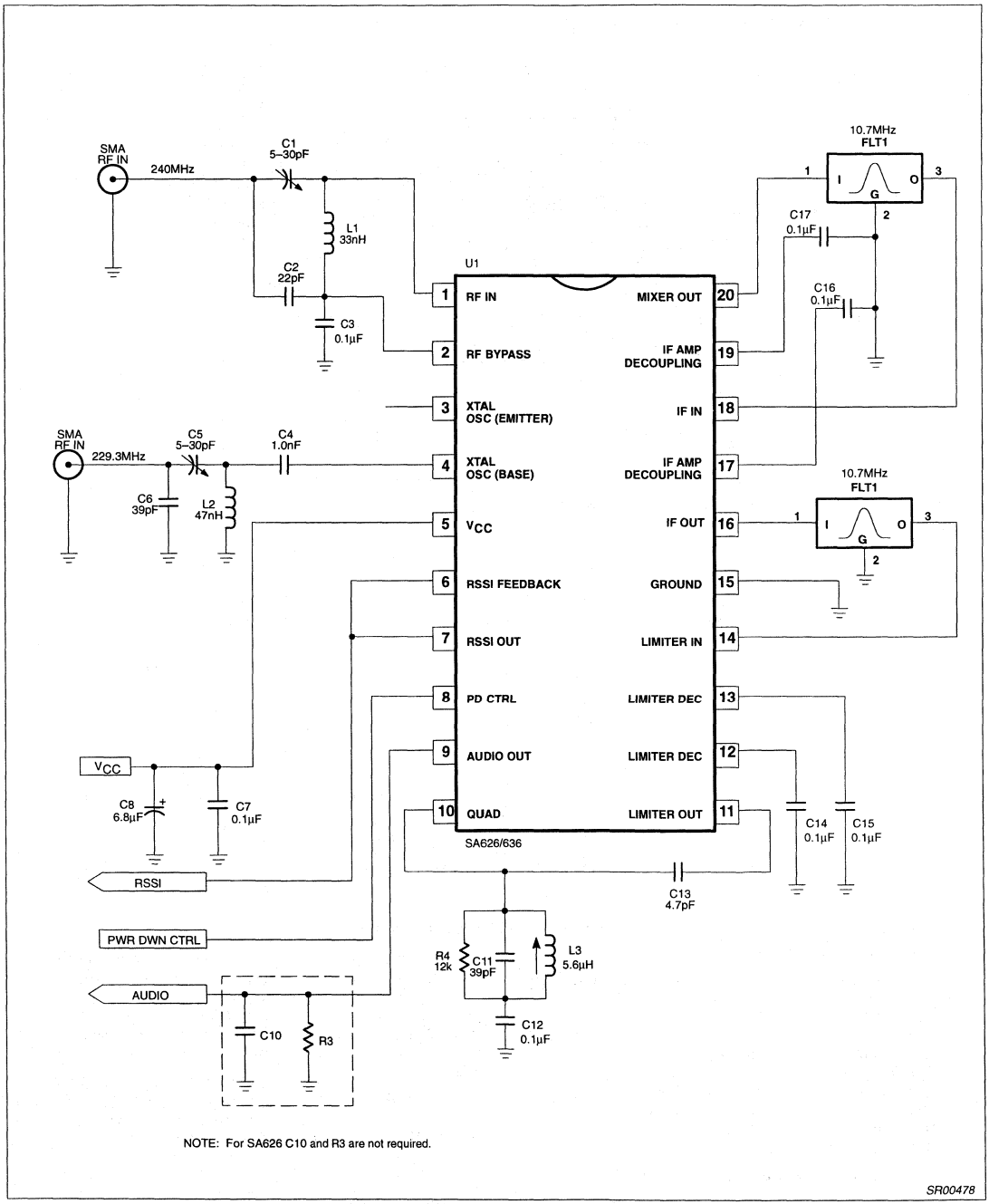


Figure 9. SA626 240MHz (RF) / 10.7MHz (IF) Application Circuit

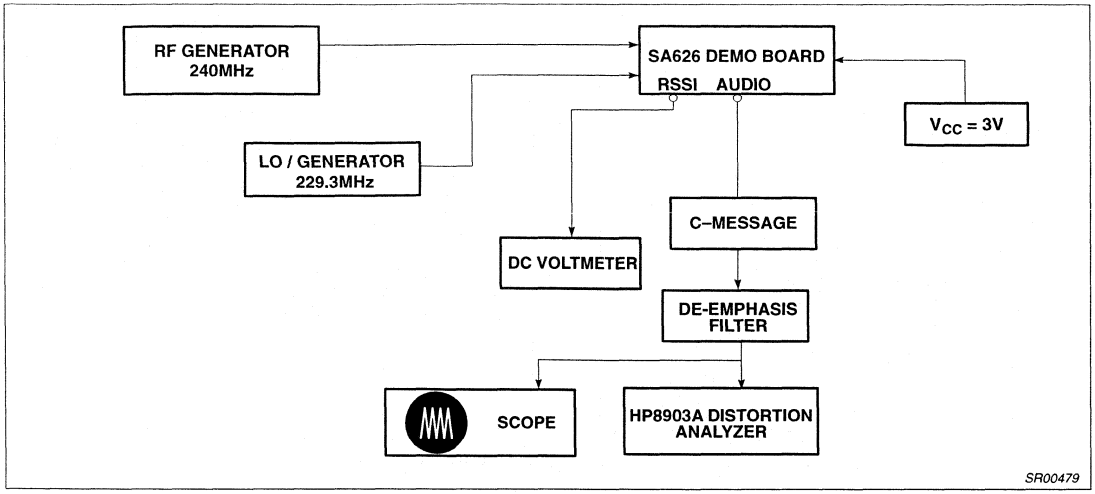


Figure 10. SA626 Application Circuit Test Set Up

NOTES:

1. C-message: The C-message and de-emphasis filter combination has a peak gain of 10 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP8903A analyzer. The de-emphasis filter has a fixed -6dB/Octave slope between 300Hz and 3kHz.
2. Ceramic filters: The ceramic filter can be SFE10.7MA5-A made by Murata which has 280kHz IF bandwidth.
3. RF generator: Set your RF generator at 240.000MHz, use a 1kHz modulation frequency and a 125kHz deviation.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.54μV or –112dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 500mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 0.1μF bypass capacitor on the supply pin improves sensitivity.

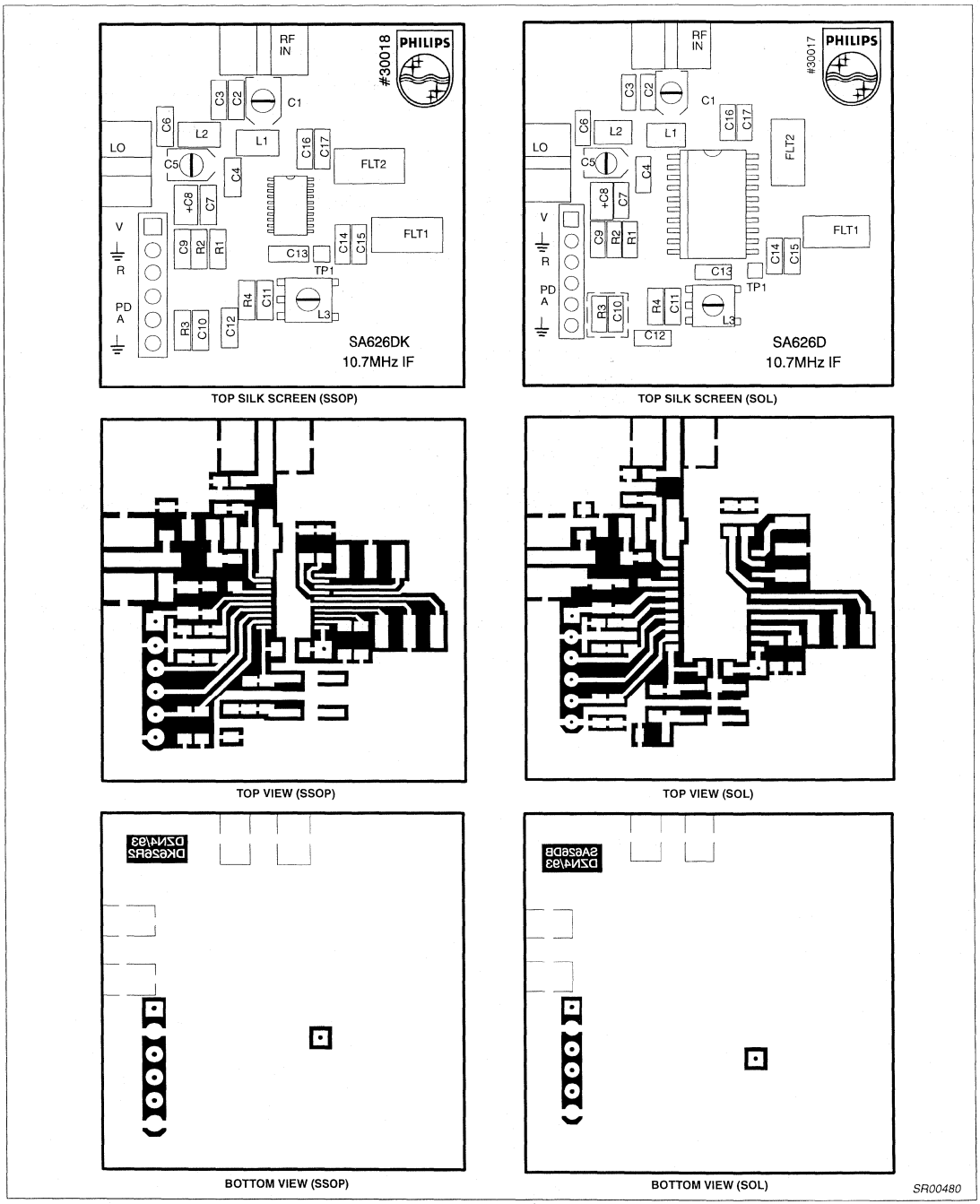


Figure 11. SA626 Demoboard Layout (Not Actual Size)

High performance low power mixer FM IF system with high-speed RSSI

SA627

DESCRIPTION

The SA627 has faster RSSI rise and fall times. The SA627 is a high performance monolithic low-power FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic received signal strength indicator (RSSI) with fast rise and fall time, voltage regulator and frequency check/limiter out (–). The SA627 also has an extra limiter output. This signal is buffered from the output of the limiter and provides a negative (–) limiter output. This can be used to provide a frequency check function. The SA627 is available in 20-lead SOL (surface-mounted miniature package) and 20-lead SSOP (shrink small outline package).

FEATURES

- Fast RSSI rise and fall times
- Low power consumption: 5.8mA typical at 6V
- Mixer input to >500MHz
- Mixer conversion power gain of 13dB at 45MHz
- Mixer noise figure of 4.6dB at 45MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator to 1GHz local oscillator can be injected)
- 102dB of IF Amp/Limiter gain
- 25MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- Audio output - mutable
- Low external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.22μV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone, 8kHz deviation with RF at 45MHz and IF at 455kHz
- SA627 meets cellular radio specifications
- ESD hardened

PIN CONFIGURATION

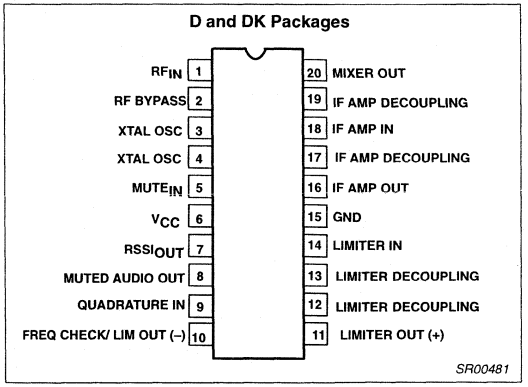


Figure 1. Pin Configuration

APPLICATIONS

- Digital cellular base stations
- High performance communications receivers
- Single conversion VHF/UHF receivers
- SCA receivers
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Wideband low current amplification
- Digital cordless telephones

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Small Outline Large (SOL) package (Surface-mount)	-40 to +85°C	SA627D	SOT163-1
20-Pin Plastic Shrink Small Outline Package (SSOP) (Surface-mount)	-40 to +85°C	SA627DK	SOT266-1

BLOCK DIAGRAM

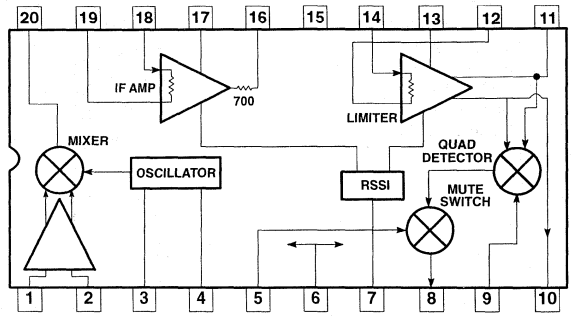


Figure 2. Block Diagram

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	9	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range SA627	-40 to +85	°C
θ_{JA}	Thermal impedance D package	90	°C/W
	DK package	117	°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA627			
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		4.5		8.0	V
I_{CC}	DC current drain		4.55	5.8	6.75	mA
	Mute switch input threshold (ON)		1.7			V
	(OFF)				1.0	V

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +6V, unless otherwise stated. RF frequency = 45MHz + 14.5dBV RF input step-up; IF frequency = 455kHz; R17 = 5.1k; RF level = -45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 3. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS SA627 MIN	LIMITS SA627 TYP	LIMITS SA627 MAX	UNITS
Mixer/Osc section (ext LO = 300mV)						
f_{IN}	Input signal frequency			500		MHz
f_{OSC}	Crystal oscillator frequency			150		MHz
	Noise figure at 45MHz			5.0		dB
	Third-order input intercept point	f1 = 45.0; f2 = 45.06MHz		-10		dBm
	Conversion power gain	Matched 14.5dBV step-up	10	13	15	dB
		50Ω source		-1.7		dB
	RF input resistance	Single-ended input	3.0	4.7		kΩ
	RF input capacitance			3.5	4.0	pF
	Mixer output resistance	(Pin 20)	1.25	1.5		kΩ
IF section						
	IF amp gain	50Ω source		39.7		dB
	Limiter gain	50Ω source		62.5		dB
	Input limiting -3dB, R_{17} = 5.1k	Test at Pin 18		-113		dBm
	AM rejection	80% AM 1kHz	29	34	43	dB
	Audio level, R_{10} = 100k	15nF de-emphasis	80	150	260	mV_{RMS}
	SINAD sensitivity	RF level -118dB		16		dB
THD	Total harmonic distortion		-34	-42		dB
S/N	Signal-to-noise ratio	No modulation for noise		73		dB
	IF RSSI output, R_9 = 100kΩ[1]	IF level = -118dBm	0	160	650	mV
		IF level = -68dBm	1.9	2.5	3.1	V
		IF level = -18dBm	4.0	4.8	5.6	V
	IF RSSI output rise time (10kHz pulse, no 455kHz filter) (no RSSI bypass capacitor)	IF frequency = 455kHz				
		RF level = -56dBm		1.2		µs
		RF level = -28dBm		1.2		µs
		IF frequency = 10.7MHz				
		RF level = -56dBm		1.2		µs
		RF level = -28dBm		1.1		µs
	IF RSSI output fall time (10kHz pulse, no 455kHz filter) (no RSSI bypass capacitor)	IF frequency = 455kHz				
		RF level = -56dBm		2.1		µs
		RF level = -28dBm		7.6		µs
		IF frequency = 10.7MHz				
		RF level = -56dBm		2.0		µs
		RF level = -28dBm		7.3		µs
	RSSI range	R_9 = 100kΩ Pin 16		90		dB
	RSSI accuracy	R_9 = 100kΩ Pin 16		±1.5		dB
	IF input impedance		1.40	1.6		kΩ
	IF output impedance		0.85	1.0		kΩ
	Limiter input impedance		1.40	1.6		kΩ
	Limiter output impedance	Pin 10 or 11		300		Ω
	Limiter output level	Pin 10 or 11 with no load 3kΩ load (min)		280 250		mV_{RMS}

AC ELECTRICAL CHARACTERISTICS(Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS SA627 MIN	LIMITS SA627 TYP	LIMITS SA627 MAX	UNITS
IF section (continued)						
	Muted audio output resistance			58		kΩ
RF/IF section (int LO)						
	System RSSI output	4.5V = V_{CC}, RF level = -27dBm		4.3		V

NOTE:
1. The generator source impedance is 50Ω, but the SA627 input impedance at Pin 18 is 1500Ω. As a result, IF level refers to the actual signal that enters the SA627 input (Pin 8) which is about 21dB less than the "available power" at the generator.

CIRCUIT DESCRIPTION

The SA627 is an IF signal processing system suitable for second IF or single conversion systems with input frequency as high as 1GHz. The bandwidth of the IF amplifier is about 40MHz, with 39.7dB(v) of gain from a 50Ω source. The bandwidth of the limiter is about 28MHz with about 62.5dB(v) of gain from a 50Ω source. However, the gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 5dB, conversion gain of 13dB, and input third-order intercept of -10dBm. The oscillator will operate in excess of 1GHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

The output of the mixer is internally loaded with a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. To achieve optimum linearity of the log signal strength indicator, there must be a 12dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dB(v) insertion loss, a fixed or variable resistor can be added between the first IF output (Pin 16) and the interstage network.

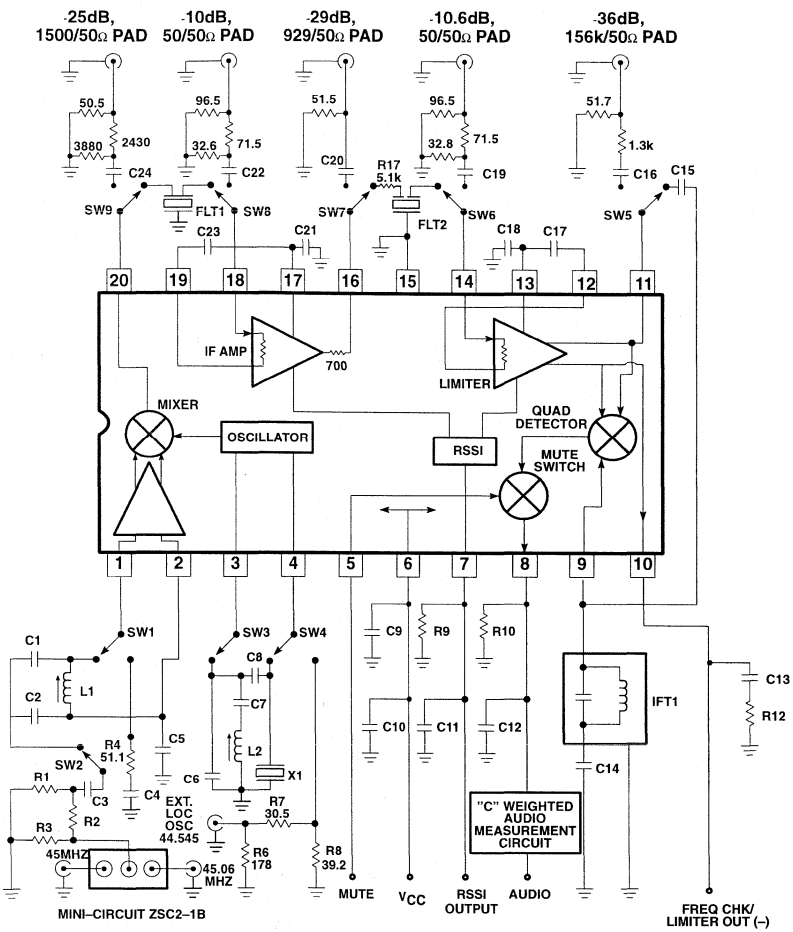
The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

Overall, the IF section has a gain of 90dB. For operation at intermediate frequencies greater than 455kHz, special care must be given to layout, termination, and interstage loss to avoid instability.

The demodulated output of the quadrature detector is available at two pins, one continuous and one with a mute switch. Signal attenuation with the mute activated is greater than 60dB. The mute input is very high impedance and is compatible with CMOS or TTL levels.

A log signal strength completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone.

NOTE: dB(v) = 20log V_{OUT}/V_{IN}



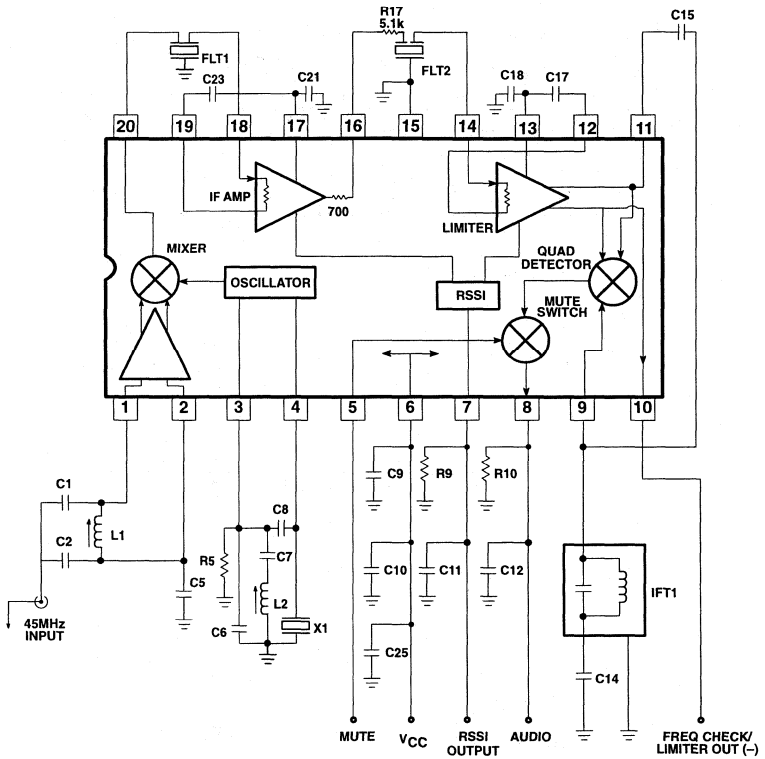
Automatic Test Circuit Component List

C1	100pF NPO Ceramic	C21	100nF ±10% Monolithic Ceramic
C2	390pF NPO Ceramic	C23	100nF ±10% Monolithic Ceramic
C5	100nF ±10% Monolithic Ceramic	C25	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic	Flt 1	Ceramic Filter Murata SFG455A3 or equiv
C7	1nF Ceramic	Flt 2	Ceramic Filter Murata SFG455A3 or equiv
C8	10.0pF NPO Ceramic	IFT 1	455kHz (Ce = 180pF) Toko RMC–2A6597H
C9	100nF ±10% Monolithic Ceramic	L1	147–160nH Coilcraft UNI–10/142–04J08S
C10	10μF Tantalum (minimum)	L2	0.8μH nominal Toko 292CNS–T1038Z
C11	100nF ±10% Monolithic Ceramic	X1	44.545MHz Crystal ICM4712701
C12	15nF ±10% Ceramic	R9	100k ±1% 1/4W Metal Film
C13	0.1μF ±10% Monolithic Ceramic	R17	5.1k ±5% 1/4W Carbon Composition
C14	100nF ±10% Monolithic Ceramic	R10	100k ±1% 1/4W Metal Film (optional)
C15	10pF NPO Ceramic	R11	100k ±1% 1/4W Metal Film (optional)
C17	100nF ±10% Monolithic Ceramic	R12	3kΩ ±5% 1/4W Metal Film (optional)
C18	100nF ±10% Monolithic Ceramic		

*NOTE: This value can be reduced when a battery is the power source.

SR00483

Figure 3. SA627 45MHz Test Circuit (Relays as shown)



Application Component List

C1	100pF NPO Ceramic
C2	390pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	10μF Tantalum (minimum) *
C11	100nF ±10% Monolithic Ceramic
C12	15nF ±10% Ceramic
C13	150pF ±2% N1500 Ceramic
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	455kHz (Ce = 180pF) Toko RMC–2A6597H
L1	147–160nH Coilcraft UNI–10/142–04J08S
L2	0.8μH nominal Toko 292CNS–T1038Z
X1	44.545MHz Crystal ICM4712701
R9	100k ±1% 1/4W Metal Film
R17	5.1k ±5% 1/4W Carbon Composition
R5	Not Used in Application Board (see Note 8)
R10	100k ±1% 1/4W Metal Film (optional)
R11	100k ±1% 1/4W Metal Film (optional)

*NOTE: This value can be reduced when a battery is the power source.

SR00484

Figure 4. SA627 45MHz Application Circuit

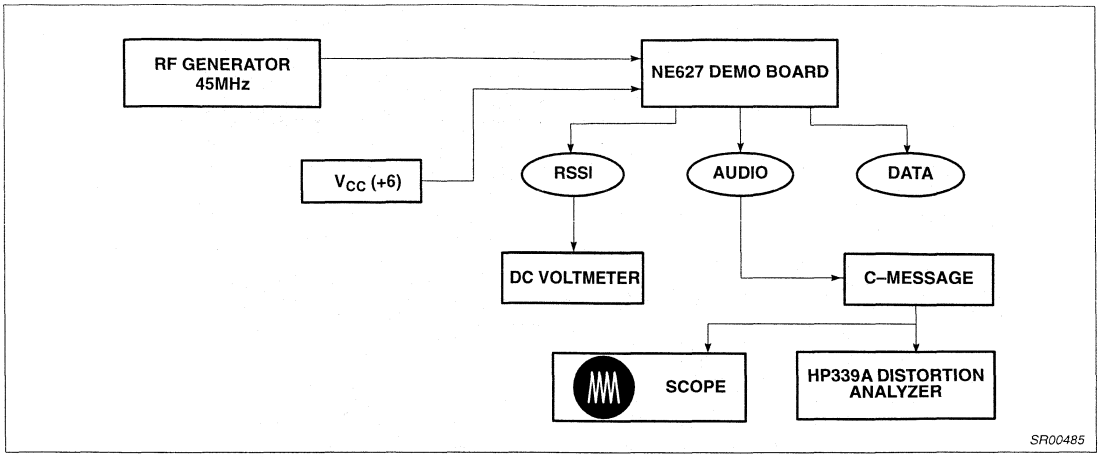


Figure 5. SA627 Application Circuit Test Set Up

NOTES:

1. C-message: The C-message filter has a peak gain of 100 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339 analyzer.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All of our specifications and testing are done with the more wideband filter.
3. RF generator: Set your RF generator at 45.000MHz, use a 1kHz modulation frequency and a 6kHz deviation if you use 16kHz filters, or 8kHz if you use 30kHz filters.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.22μV or -120dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 250mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10-15μF or higher value tantalum capacitor on the supply line is essential. A low frequency ESR screening test on this capacitor will ensure consistent good sensitivity in production. A 0.1μF bypass capacitor on the supply pin, and grounded near the 44.545MHz oscillator improves sensitivity by 2-3dB.
8. R5 can be used to bias the oscillator transistor at a higher current for operation above 45MHz. Recommended value is 22kΩ, but should not be below 10kΩ.

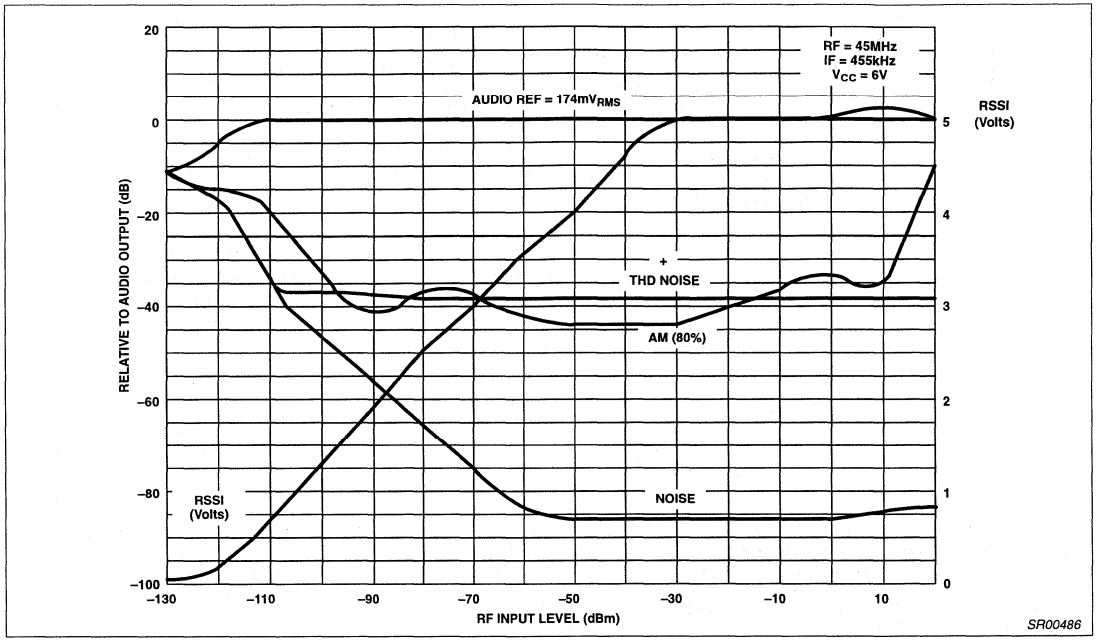


Figure 6. SA627 Application Board at 25°C

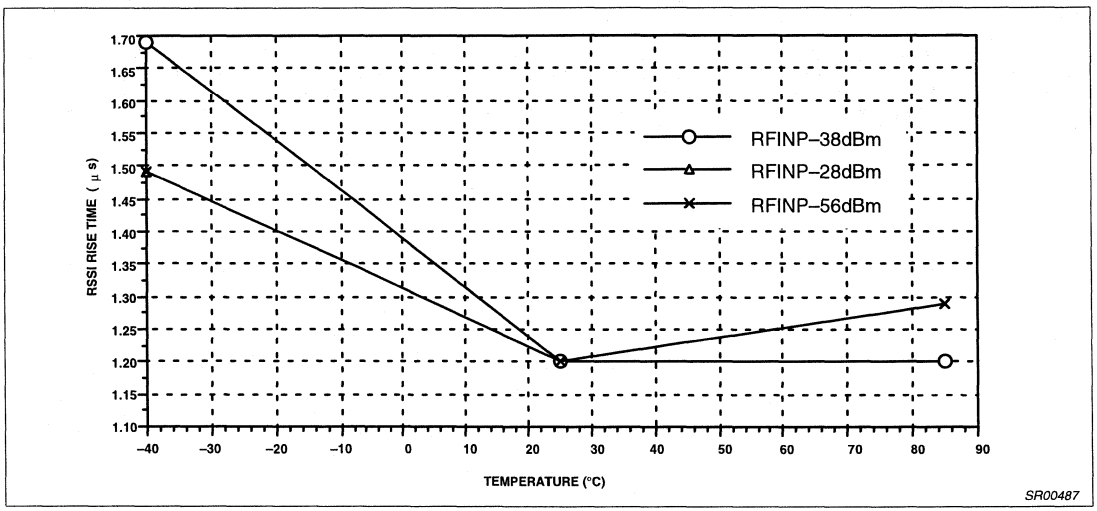


Figure 7. SA627 Rise Time 455kHz IF Frequency

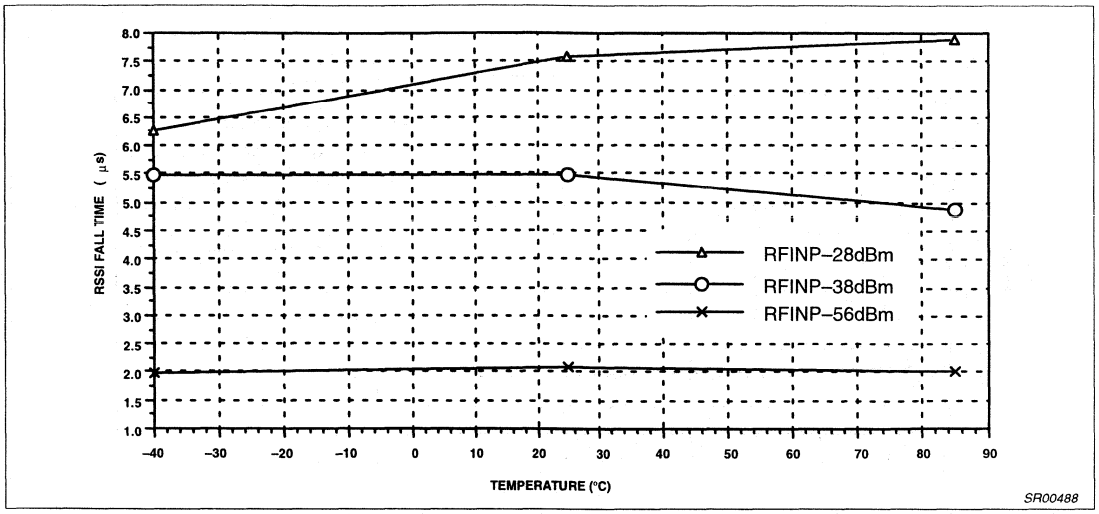


Figure 8. SA627 Fall Time 455kHz IF Frequency

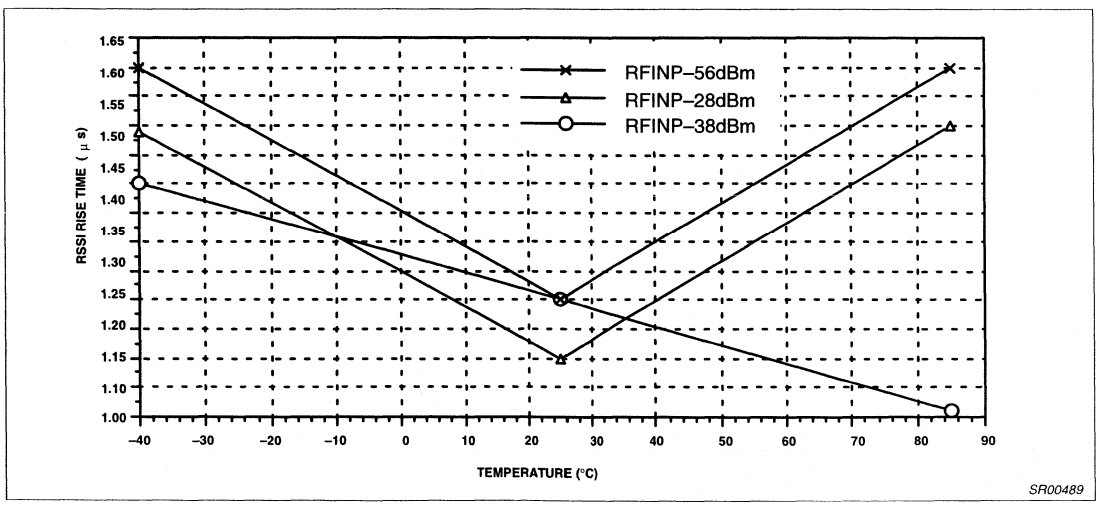


Figure 9. SA627 Rise Time 10.7MHz IF Frequency

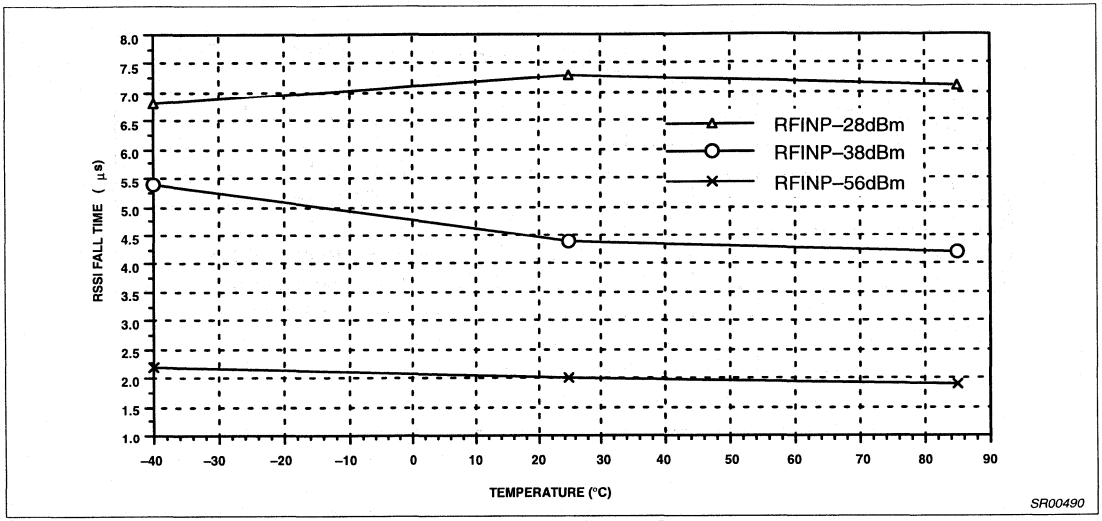


Figure 10. SA627 Fall Time 10.7MHz IF Frequency

Single pole double throw (SPDT) switch SA630

DESCRIPTION

The SA630 is a wideband RF switch fabricated in BiCMOS technology and incorporating on-chip CMOS/TTL compatible drivers. Its primary function is to switch signals in the frequency range DC - 1GHz from one 50Ω channel to another. The switch is activated by a CMOS/TTL compatible signal applied to the enable channel 1 pin (ENCH1).

The extremely low current consumption makes the SA630 ideal for portable applications. The excellent isolation and low loss makes this a suitable replacement for PIN diodes.

The SA630 is available in an 8-pin dual in-line plastic package and an 8-pin SO (surface mounted miniature) package.

FEATURES

- Wideband (DC - 1GHz)
- Low through loss (1dB typical at 200MHz)
- Unused input is terminated internally in 50Ω
- Excellent overload capability (1dB gain compression point +18dBm at 300MHz)
- Low DC power (170μA from 5V supply)
- Fast switching (20ns typical)
- Good isolation (off channel isolation 60dB at 100MHz)

PIN CONFIGURATION

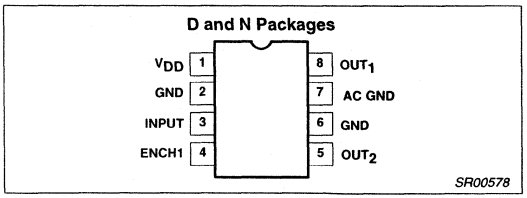


Figure 1. Pin Configuration

- Low distortion (IP_3 intercept +33dBm)
- Good 50Ω match (return loss 18dB at 400MHz)
- Full ESD protection
- Bidirectional operation

APPLICATIONS

- Digital transceiver front-end switch
- Antenna switch
- Filter selection
- Video switch
- FSK transmitter

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA630N	SOT97-1
8-Pin Plastic Small Outline (SO) package (Surface-mount)	-40 to +85°C	SA630D	SOT96-1

BLOCK DIAGRAM

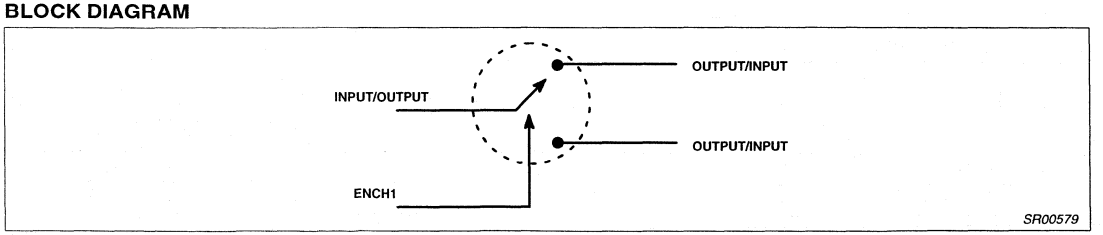


Figure 2. Block Diagram

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{DD}	Supply voltage	3.0 to 5.5V	V
T_A	Operating ambient temperature range SA Grade	-40 to +85	°C
T_J	Operating junction temperature range SA Grade	-40 to +105	°C

EQUIVALENT CIRCUIT

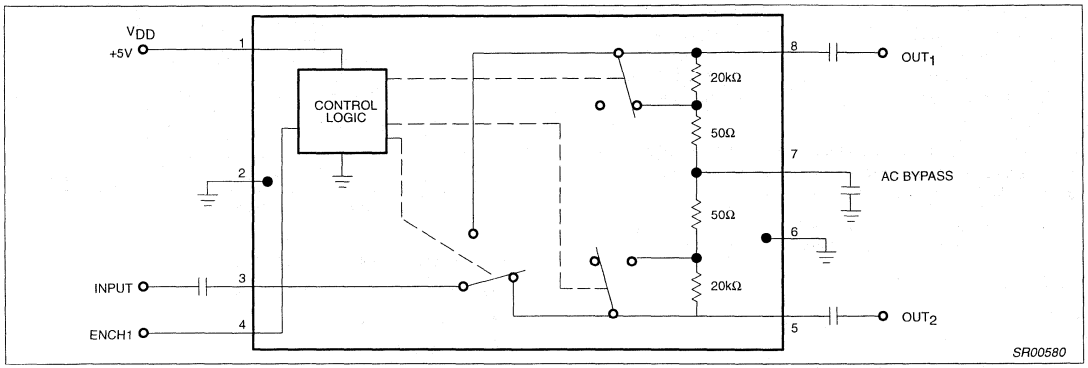


Figure 3. Equivalent Circuit

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{DD}	Supply voltage	-0.5 to +5.5	V
P_D	Power dissipation, T_A = 25°C (still air)[1] 8-Pin Plastic DIP 8-Pin Plastic SO	 1160 780	 mW mW
T_{JMAX}	Maximum operating junction temperature	150	°C
P_{MAX}	Maximum power input/output	+20	dBm
T_{STG}	Storage temperature range	-65 to +150	°C

NOTES:
1. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance, θ_{JA}:
   8-Pin DIP: θ_{JA} = 108°C/W
   8-Pin SO: θ_{JA} = 158°C/W

DC ELECTRICAL CHARACTERISTICS

V_{DD} = +5V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA630			
			MIN	TYP	MAX	
I_{DD}	Supply current		40	170	300	µA
V_T	TTL/CMOS logic threshold voltage[1]		1.1	1.25	1.4	V
V_{IH}	Logic 1 level	Enable channel 1	2.0		V_{DD}	V
V_{IL}	Logic 0 level	Enable channel 2	-0.3		0.8	V
I_{IL}	ENCH1 input current	ENCH1 = 0.4V	-1	0	1	µA
I_{IH}	ENCH1 input current	ENCH1 = 2.4V	-1	0	1	µA

NOTE:
1. The ENCH1 input must be connected to a valid Logic Level for proper operation of the SA630.

AC ELECTRICAL CHARACTERISTICS[1] - D PACKAGE

V_{DD} = +5V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA630			
			MIN	TYP	MAX	
S_{21}, S_{12}	Insertion loss (ON channel)	DC - 100MHz 500MHz 900MHz		1 1.4 2	 2.8	dB
S_{21}, S_{12}	Isolation (OFF channel)[2]	10MHz 100MHz 500MHz 900MHz	70 24	80 60 50 30		dB
S_{11}, S_{22}	Return loss (ON channel)	DC - 400MHz 900MHz		20 12		dB
S_{11}, S_{22}	Return loss (OFF channel)	DC - 400MHz 900MHz		17 13		dB
t_D	Switching speed (on-off delay)	50% TTL to 90/10% RF		20		ns
t_r, t_f	Switching speeds (on-off rise/fall time)	90%/10% to 10%/90% RF		5		ns
	Switching transients			165		mV_{P-P}
P_{-1dB}	1dB gain compression	DC - 1GHz		+18		dBm
IP_3	Third-order intermodulation intercept	100MHz		+33		dBm
IP_2	Second-order intermodulation intercept	100MHz		+52		dBm
NF	Noise figure (Z_O = 50Ω)	100MHz 900MHz		1.0 2.0		dB

NOTE:
1. All measurements include the effects of the D package SA630 Evaluation Board (see Figure 4B). Measurement system impedance is 50Ω.
2. The placement of the AC bypass capacitor is critical to achieve these specifications. See the applications section for more details.

AC ELECTRICAL CHARACTERISTICS[1] - N PACKAGE

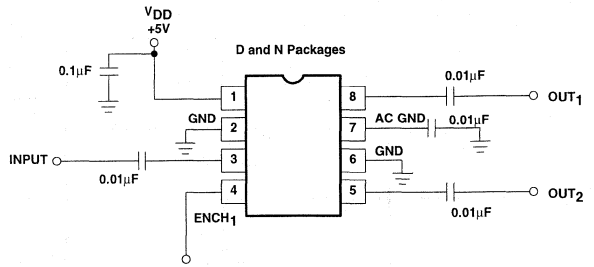
V_{DD} = +5V, T_A = 25°C; all other characteristics similar to the D-Package, unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA630			
			MIN	TYP	MAX	
S_{21}, S_{12}	Insertion loss (ON channel)	DC - 100MHz 500MHz 900MHz		1 1.4 2.5		dB
S_{21}, S_{12}	Isolation (OFF channel)	10MHz 100MHz 500MHz 900MHz	58	68 50 37 15		dB
NF	Noise figure (Z_O = 50Ω)	100MHz 900MHz		1.0 2.5		dB

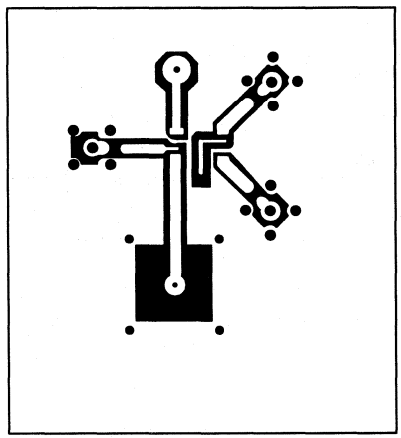
NOTE:
1. All measurements include the effects of the N package SA630 Evaluation Board (see Figure 4C). Measurement system impedance is 50Ω.

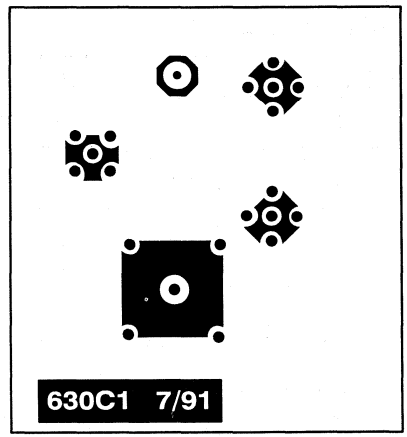
APPLICATIONS

The typical applications schematic and printed circuit board layout of the SA630 evaluation board is shown in Figure 4. The layout of the board is simple, but a few cautions need to be observed. The input and output traces should be 50Ω. The placement of the AC bypass capacitor is *extremely critical* if a symmetric isolation between the two channels is desired. The trace from Pin 7 should be drawn back towards the package and then be routed downwards. The capacitor should be placed straight down as close to the device as practical. For better isolation between the two channels at higher frequencies, it is also advisable to run the two output/input traces at an angle. This also minimizes any inductive coupling between the two traces. The power supply bypass capacitor should be placed close to the device. Figure 10 shows the frequency response of the SA630. The loss matching between the two channels is excellent to 1.2GHz as shown in Figure 13.

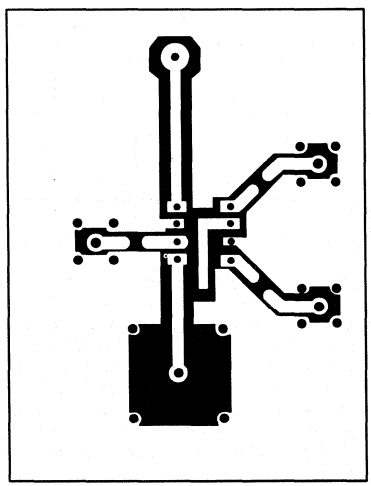


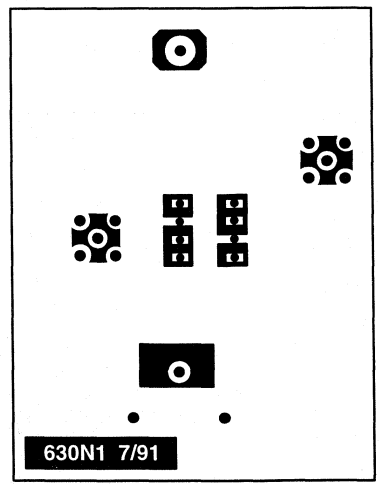
a. Evaluation Board Schematic





b. 630 D-Package Board Layout





c. 630 N-Package Board Layout

SR00581

Figure 4. Board and Package Graphics

The isolation and matching of the two channels over frequency is shown in Figures 15 and 17, respectively.

The SA630 is a very versatile part and can be used in many applications. Figure 5 shows a block diagram of a typical Digital RF transceiver front-end. In this application the SA630 replaces the duplexer which is typically very bulky and lossy. Due to the low power consumption of the device, it is ideally suited for handheld applications such as in CT2 cordless telephones. The SA630 can also be used to generate Amplitude Shift Keying (ASK) or On-Off Keying (OOK) and Frequency Shift Keying (FSK) signals for digital RF communications systems. Block diagrams for these applications are shown in Figures 6 and 7, respectively.

For applications that require a higher isolation at 1GHz than obtained from a single SA630, several SA630s can be cascaded as shown in Figure 8. The cascaded configuration will have a higher loss but greater than 35dB of isolation at 1GHz and greater than 65dB @ 500MHz can be obtained from this configuration. By modifying the enable control, an RF multiplexer/ de-multiplexer or antenna selector can be constructed. The simplicity of SA630 coupled with its ease of use and high performance lends itself to many innovative applications.

The SA630 switch terminates the OFF channel in 50Ω. The 50Ω resistor is internal and is in series with the external AC bypass capacitor. Matching to impedances other than 50Ω can be achieved by adding a resistor in series with the AC bypass capacitor (e.g., 25Ω additional to match to a 75Ω environment).

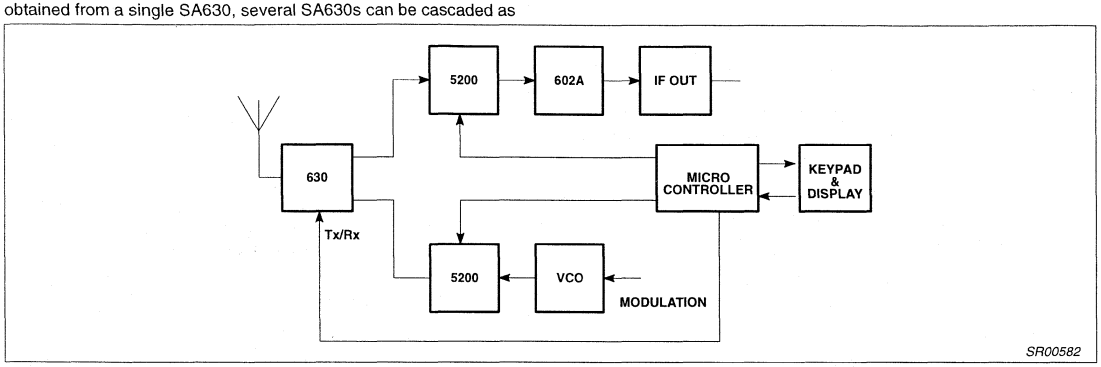


Figure 5. A Typical TDMA/Digital RF Transceiver System Front-End

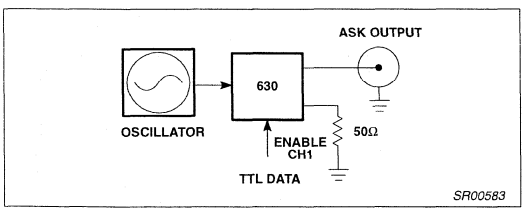


Figure 6. Amplitude Shift Keying (ASK) Generator

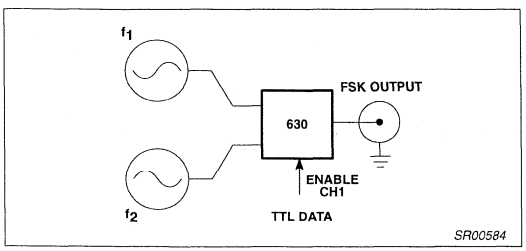


Figure 7. Frequency Shift Keying (FSK) Gnerator

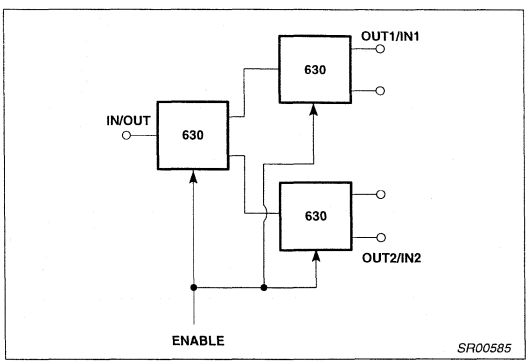


Figure 8.

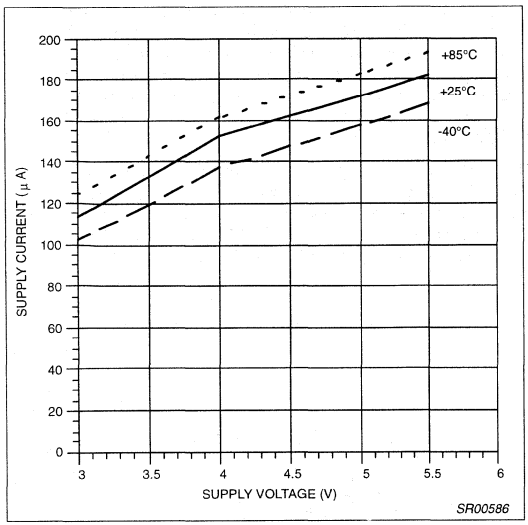


Figure 9. Supply Current vs. V_{DD} and Temperature

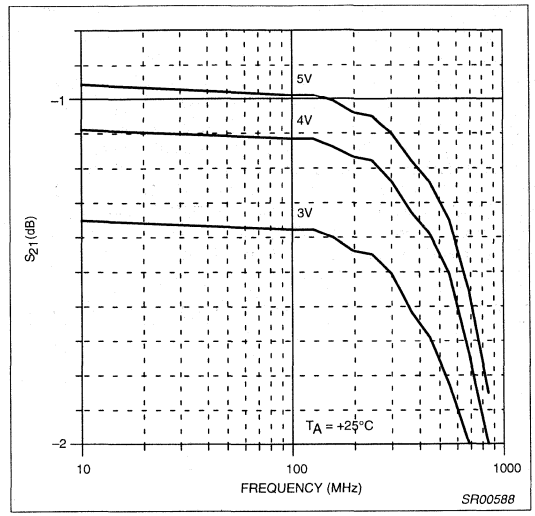


Figure 11. Loss vs. Frequency and V_{DD} for D-Package-Expanded Detail-

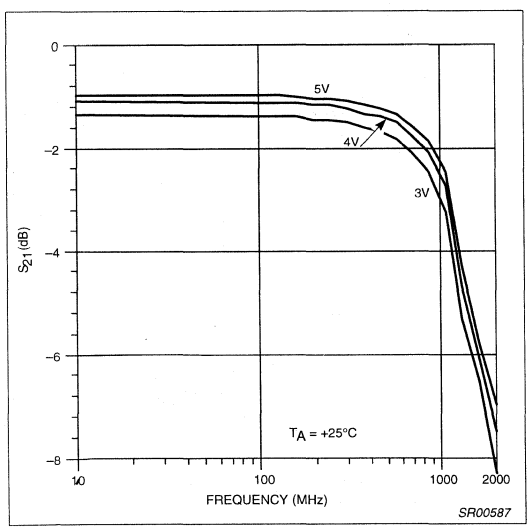


Figure 10. Loss vs. Frequency and V_{DD} for D-Package

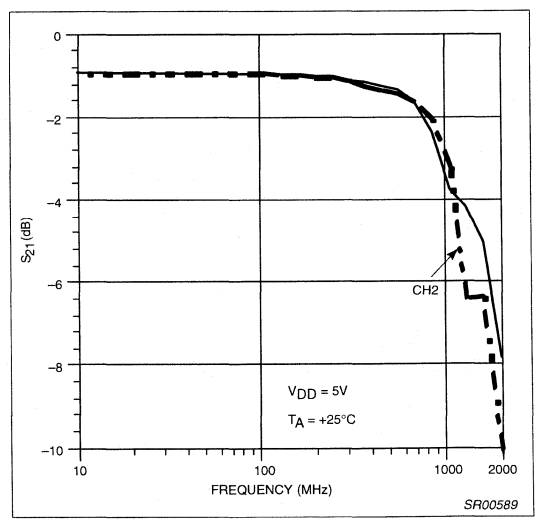


Figure 12. Loss Matching vs. Frequency for N-Package (DIP)

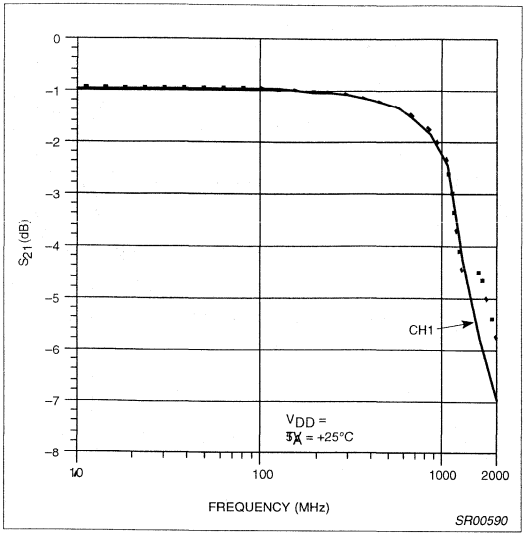


Figure 13. Loss Matching vs. Frequency; CH1 vs. CH2 for D-Pakage

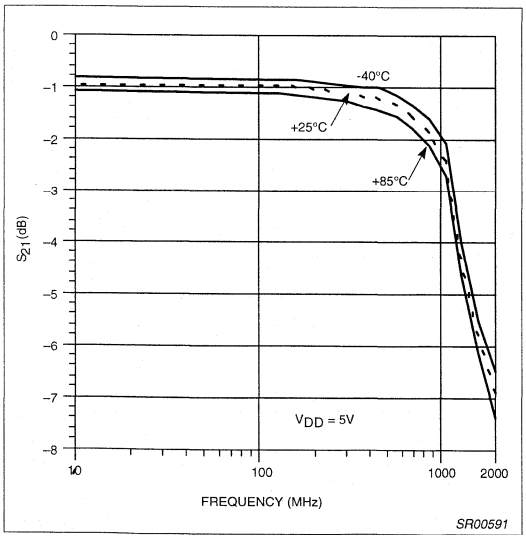


Figure 14. Loss vs. Frequency and Temperature for D-Package

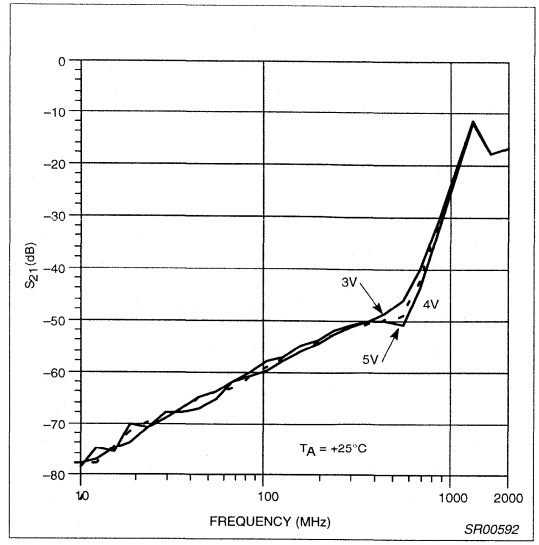


Figure 15. Isolation vs. Frequency and V_{DD} for D-Package

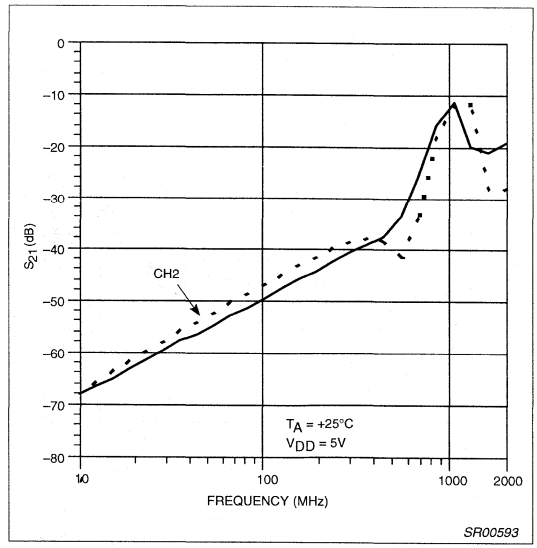


Figure 16. Isolation Matching vs. Frequency for N-Package (DIP)

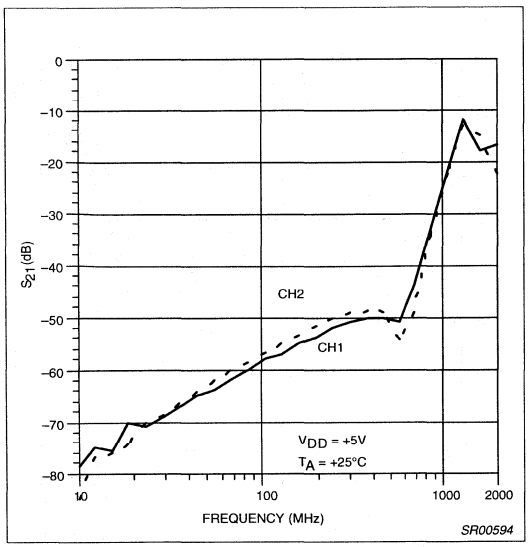


Figure 17. Isolation Matching vs. Frequency; CH1 vs. CH2 for D-Package

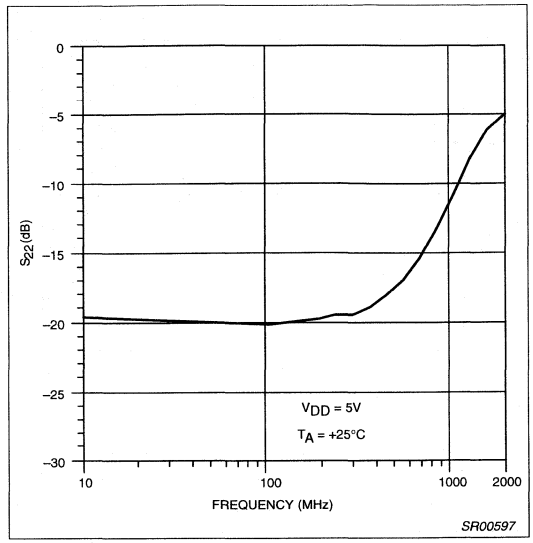


Figure 19. Output Match On-Channel vs. Frequency

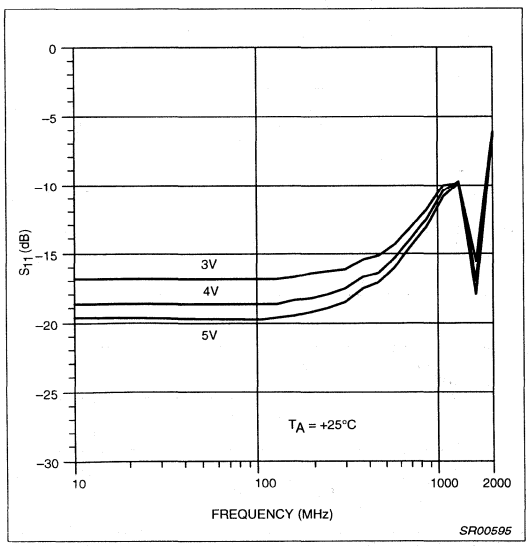


Figure 18. Input Match On-Channel vs. Frequency and V_{DD}

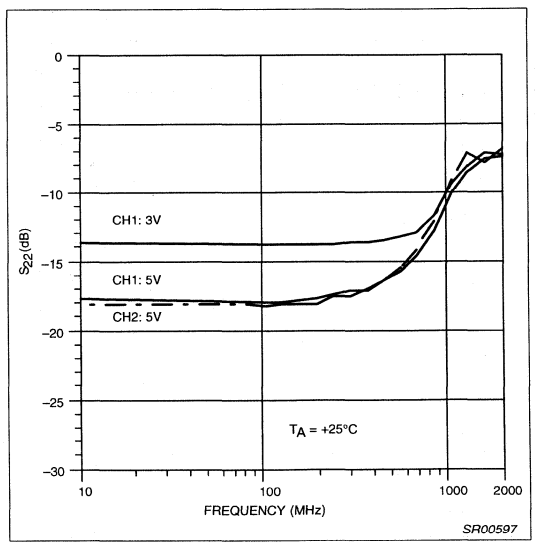


Figure 20. OFF-Channel Match vs. Frequency and V_{DD}

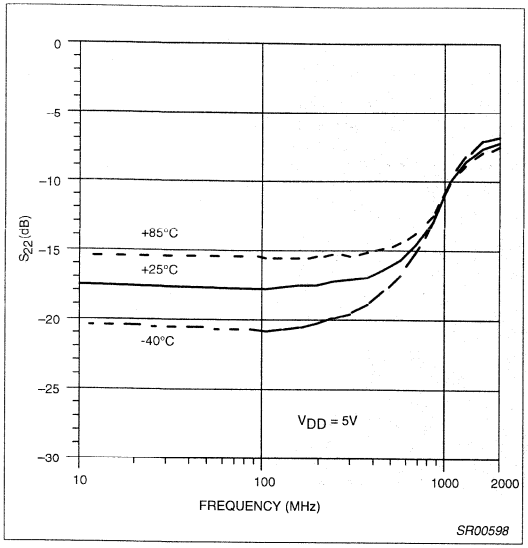


Figure 21. OFF Channel Match vs. Frequency and Temperature

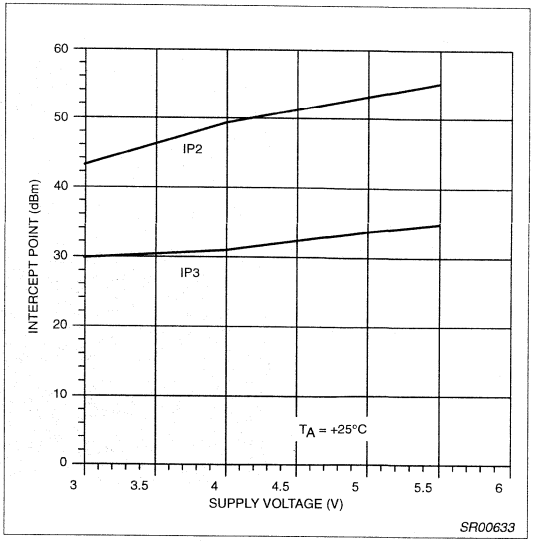


Figure 23. Intercept Points vs.V_{DD}

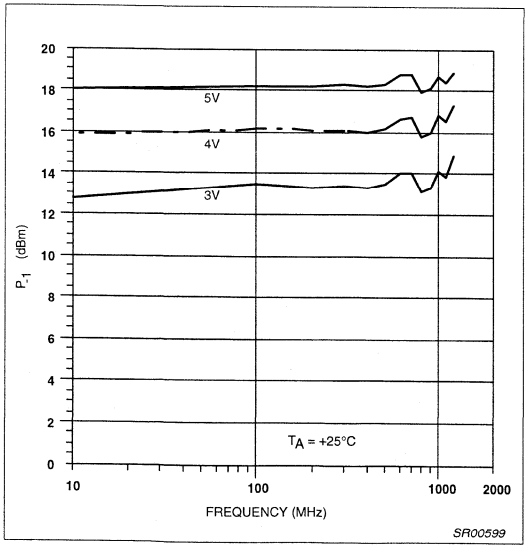


Figure 22. P_{-1} dB vs. Frequency and V_{DD}

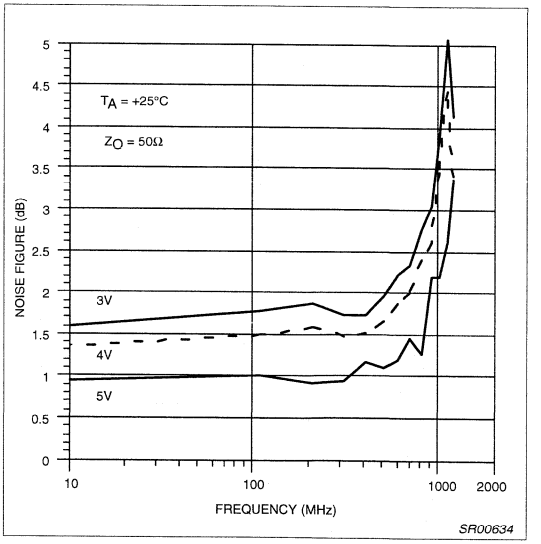


Figure 24. Noise Figure vs. Frequency and V_{DD} for D-Package

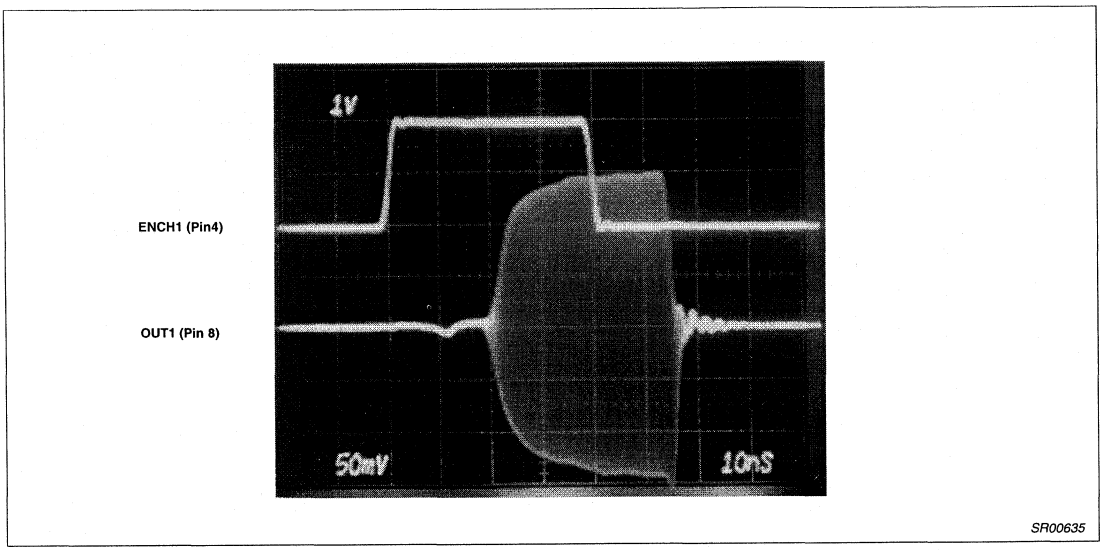


Figure 25. Switching Speed; f_{IN} = 100MHz at -6dBm, V_{DD} = 5V

Low voltage high performance mixer FM IF system with high-speed RSSI

SA636

DESCRIPTION

The SA636 is a low-voltage high performance monolithic FM IF system with high-speed RSSI incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, logarithmic received signal strength indicator (RSSI), voltage regulator, wideband data output and fast RSSI op amps. The SA636 is available in 20-lead SSOP (shrink small outline package).

The SA636 was designed for high bandwidth portable communication applications and will function down to 2.7V. The RF section is similar to the famous SA605. The data output has a minimum bandwidth of 600kHz. This is designed to demodulate wideband data. The RSSI output is amplified. The RSSI output has access to the feedback pin. This enables the designer to adjust the level of the outputs or add filtering.

SA636 incorporates a power down mode which powers down the device when Pin 8 is low. Power down logic levels are CMOS and TTL compatible with high input impedance.

APPLICATIONS

- DECT (Digital European Cordless Telephone)
- Digital cordless telephones
- Digital cellular telephones
- Portable high performance communications receivers
- Single conversion VHF/UHF receivers
- FSK and ASK data receivers
- Wireless LANs

FEATURES

- Wideband data output (600kHz min.)
- Fast RSSI rise and fall times
- Low power consumption: 6.5mA typ at 3V
- Mixer input to >500MHz
- Mixer conversion power gain of 11dB at 240MHz
- Mixer noise figure of 12dB at 240MHz

PIN CONFIGURATION

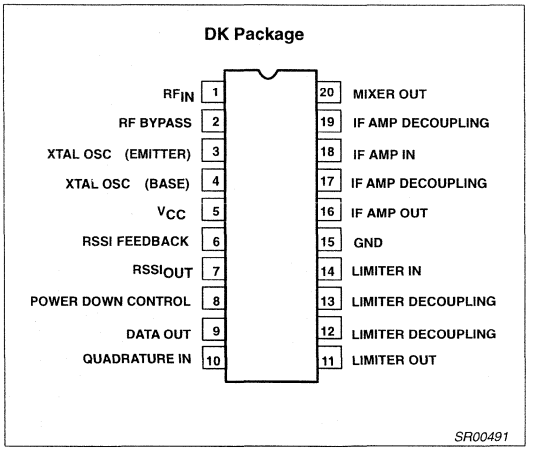


Figure 1. Pin Configuration

- XTAL oscillator effective to 150MHz (L.C. oscillator to 1GHz local oscillator can be injected)
- 92dB of IF Amp/Limiter gain
- 25MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- RSSI output internal op amp
- Internal op amps with rail-to-rail outputs
- Low external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.54μV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone with RF at 240MHz and IF at 10.7MHz
- ESD hardened
- 10.7MHz filter matching (330Ω)
- Power down mode (I_{CC} = 200μA)

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Shrink Small Outline Package (Surface-mount)	-40 to +85°C	SA636DK	SOT266-1

BLOCK DIAGRAM

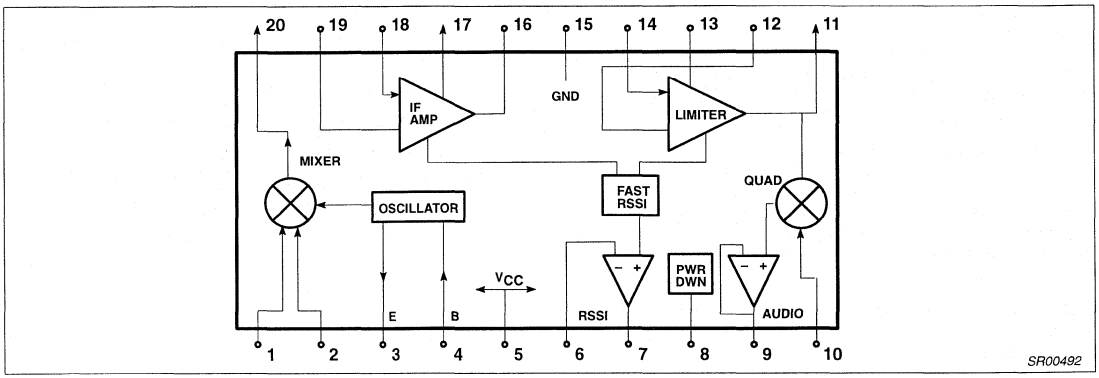


Figure 2. Block Diagram

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	0.3 to 7	V
V_{IN}	Voltage applied to any other pin	–0.3 to (V_{CC}+0.3)	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range SA636	–40 to +85	°C

NOTE: θ_{JA}, Thermal impedance DK package 117°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

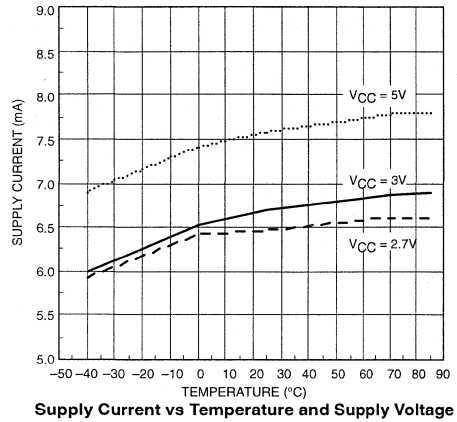
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA636			
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		2.7	3.0	5.5	V
I_{CC}	DC current drain	Pin 8 = HIGH	5.5	6.5	7.5	mA
	Input current	Pin 8 LOW	–10		10	µA
		Pin 8 HIGH	–10		10	
	Input level	Pin 8 LOW	0		$0.3V_{CC}$	V
		Pin 8 HIGH	$0.7V_{CC}$		V_{CC}	
I_{CC}	Standby	Pin 8 = LOW		0.2	0.5	mA
t_{ON}	Power up time	RSSI valid (10% to 90%)		10		µs
t_{OFF}	Power down time	RSSI invalid (90% to 10%)		5		µs

AC ELECTRICAL CHARACTERISTICS

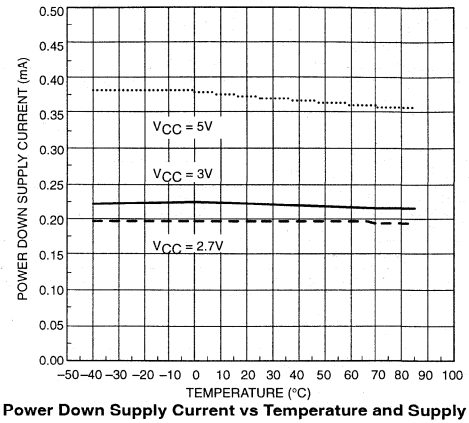
T_A = 25°C; V_{CC} = +3V, unless otherwise stated. RF frequency = 240.05MHz + 14.5dBV RF input step-up; IF frequency = 10.7MHz; RF level = -45dBm; FM modulation = 1kHz with ±125kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characteristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA636			
			MIN	TYP	MAX	
Mixer/Osc section (ext LO = 160mV$_{RMS}$)						
f_{IN}	Input signal frequency			500		MHz
f_{OSC}	External oscillator (buffer)			500		MHz
	Noise figure at 240MHz			12		dB
	Third-order input intercept point	Matched f1=240.05; f2=240.35MHz		-16		dBm
	Conversion power gain	Matched 14.5dBV step-up	8	11	14	dB
	RF input resistance	Single-ended input		700		Ω
	RF input capacitance			3.5		pF
	Mixer output resistance	(Pin 20)		330		Ω
IF section						
	IF amp gain	330Ω load		38		dB
	Limiter gain	330Ω load		54		dB
	Input limiting -3dB	Test at Pin 18		–105		dBm
	AM rejection	80% AM 1kHz		50		dB
	Data level	R_{LOAD} = 100kΩ	120	130		mV$_{RMS}$
	3dB data bandwidth		600	700		kHz
	SINAD sensitivity	RF level = -111dBm		16		dB
THD	Total harmonic distortion			-43	-38	dB
S/N	Signal-to-noise ratio	No modulation for noise		60		dB
	IF RSSI output with buffer	IF level = -118dBm		0.2	0.5	V
		IF level = -68dBm	0.3	0.6	1.0	V
		IF level = -10dBm	0.9	1.3	1.8	V
	IF RSSI output rise time	IF frequency = 10.7MHz				
	(10kHz pulse, no 10.7MHz filter)	RF level = -56dBm		1.2		µs
	(no RSSI bypass capacitor)	RF level = -28dBm		1.1		µs
	IF RSSI output fall time	IF frequency = 10.7MHz				
	(10kHz pulse, no 10.7MHz filter)	RF level = -56dBm		2.0		µs
	(no RSSI bypass capacitor)	RF level = -28dBm		7.3		µs
	RSSI range			90		dB
	RSSI accuracy			±1.5		dB
	IF input impedance			330		Ω
	IF output impedance			330		Ω
	Limiter input impedance			330		Ω
	Limiter output impedance			300		Ω
	Limiter output level with no load			130		mV$_{RMS}$
RF/IF section (Int LO)						
	System RSSI output	RF level = -10dBm		1.4		V
	System SINAD	RF level = -106dBm		12		dB

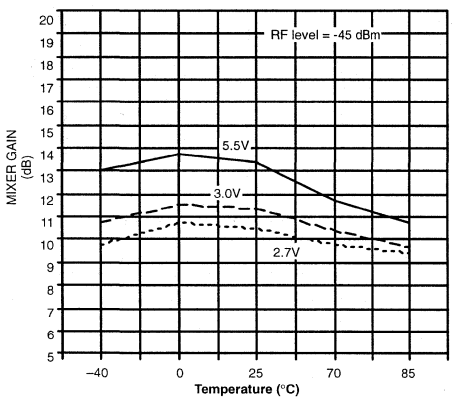
PERFORMANCE CHARACTERISTICS



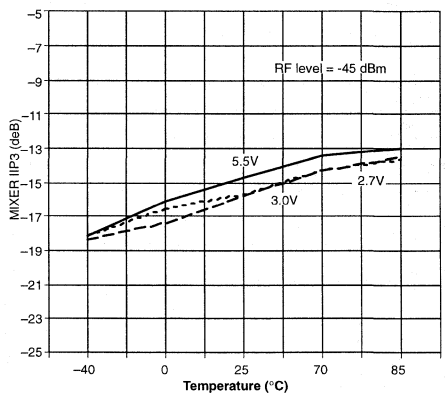
Supply Current vs Temperature and Supply Voltage



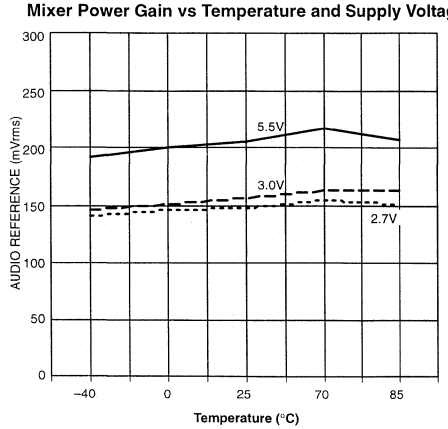
Power Down Supply Current vs Temperature and Supply Voltage



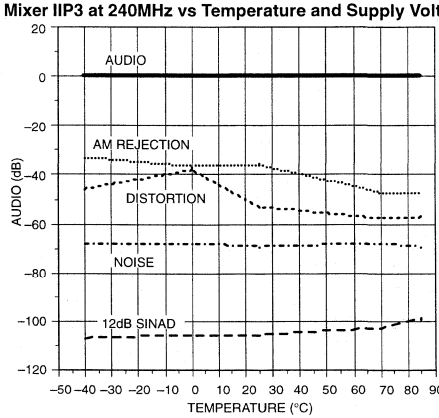
Mixer Power Gain vs Temperature and Supply Voltage



Mixer IIP3 at 240MHz vs Temperature and Supply Voltage



Audio Reference Level vs Temperature and Supply Voltage

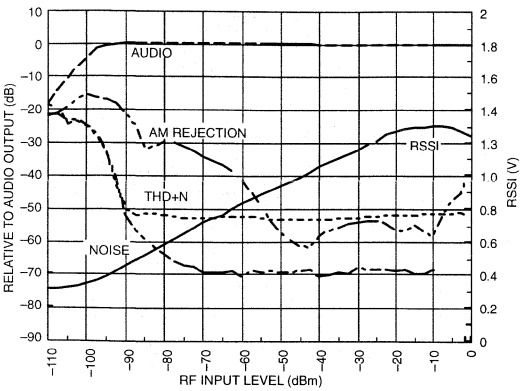


12dB SINAD and Relative Audio, THD, Noise and AM Rejection for VCC = 3V vs Temperature RF = 240MHz, Level = –68dBm, Deviation = 125kHz

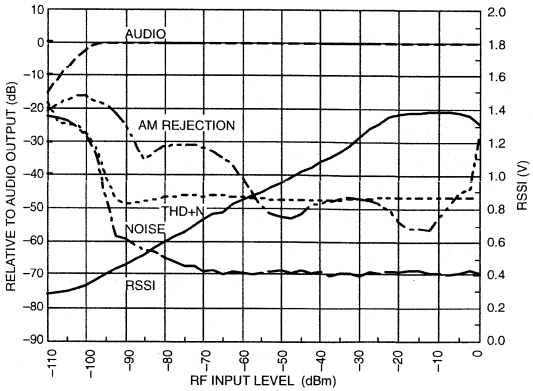
SR00493

Figure 3. Performance Characteristics

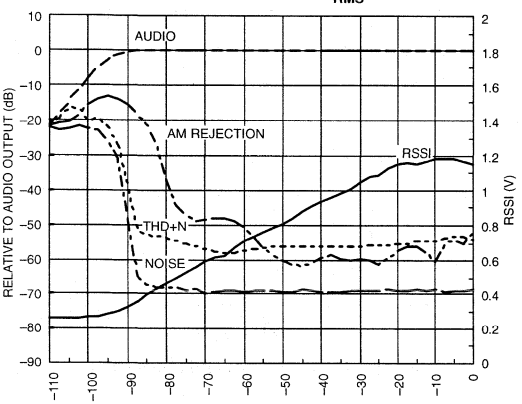
PERFORMANCE CHARACTERISTICS (continued)



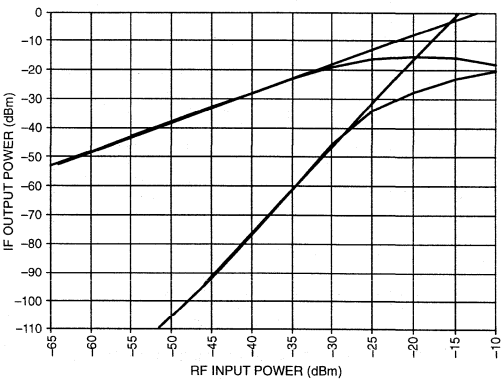
Receiver RF Performance — T = 25°C, Audio Level = 129mV$_{RMS}$



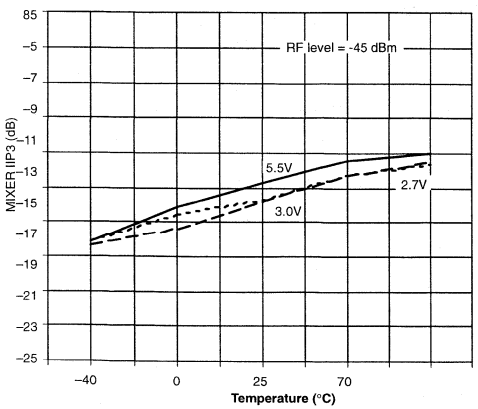
Receiver RF Performance — T = –40°C, Audio Level = 118mV$_{RMS}$



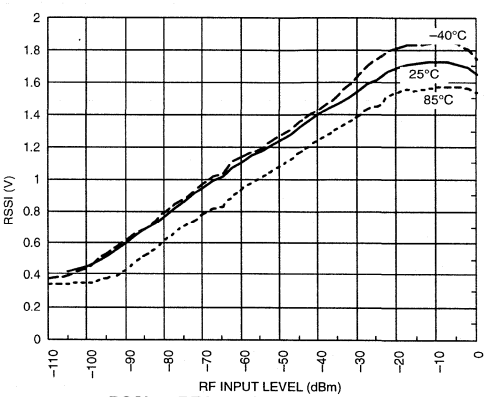
Receiver RF Performance – T = 85°C, Audio Level = 131mV$_{RMS}$



Mixer Third Order Intercept and Compression



Mixer IIP3 at 240MHz vs Temperature and Supply Voltage

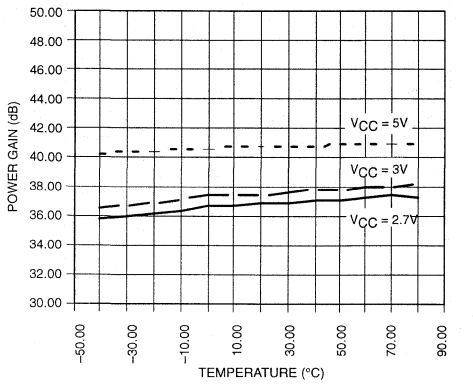


RSSI vs RF Input Level and Temperature

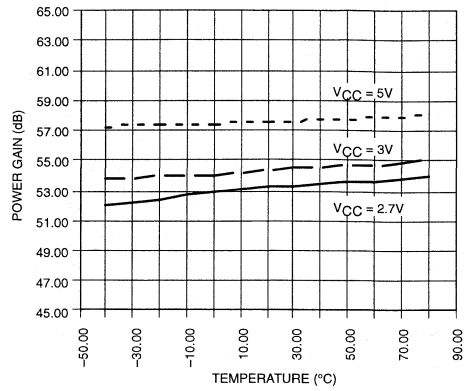
SR00494

Figure 4. Performance Characteristics

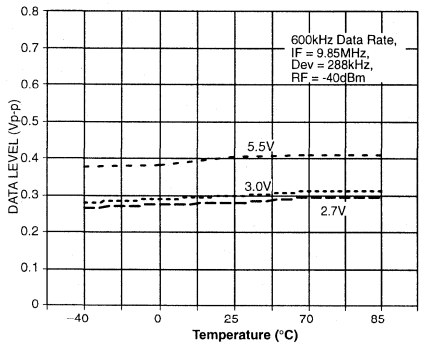
PERFORMANCE CHARACTERISTICS (continued)



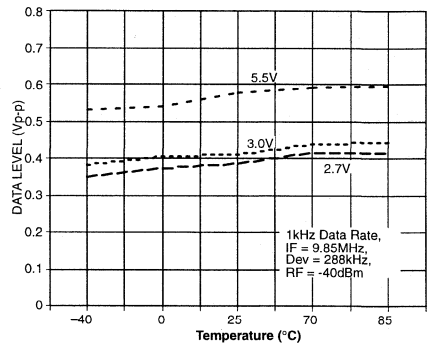
SA626 IF Amplifier Gain vs Temperature vs Supply Voltage



SA626 Limiting Amplifier Gain vs Temperature vs Supply Voltage



Data Level vs Temperature and Supply Voltage

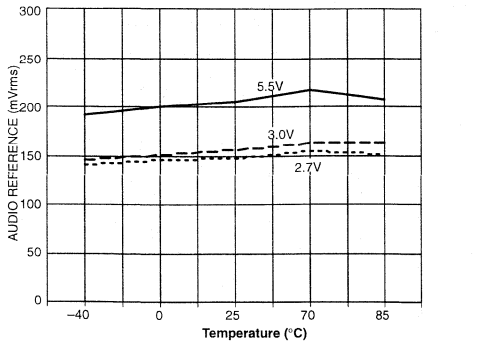


Data Level vs Temperature and Supply Voltage

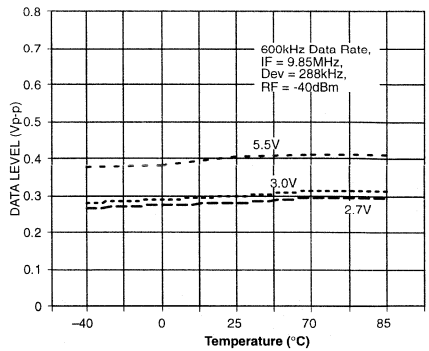
SR00495

Figure 5. Performance Characteristics

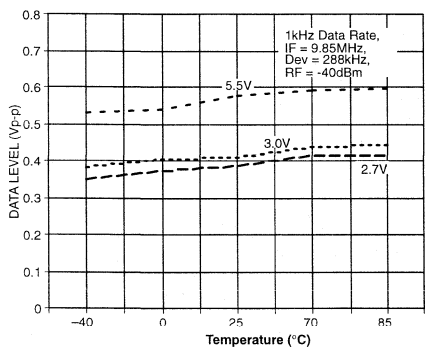
PERFORMANCE CHARACTERISTICS (continued)



Audio Reference Level vs Temperature and Supply Voltage



Data Level vs Temperature and Supply Voltage

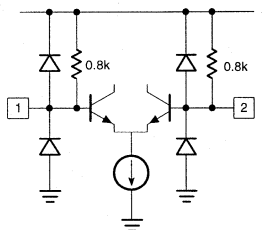
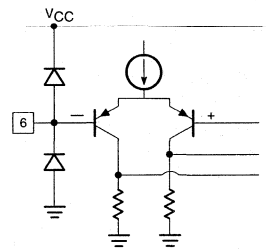
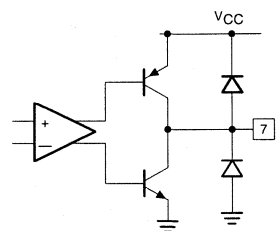
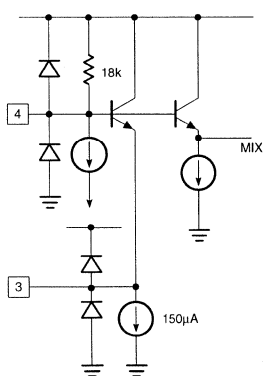
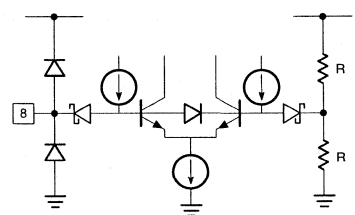
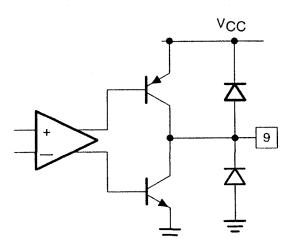
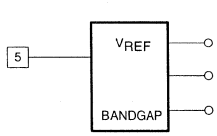
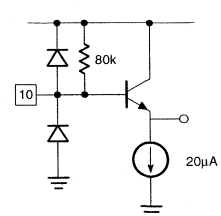


Data Level vs Temperature and Supply Voltage

SR00496

Figure 6. Performance Characteristics

PIN FUNCTIONS

PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT	PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
1	RF IN	+1.07		6	RSSI FEEDBACK	+0.20	
2	RF BYPASS	+1.07		7	RSSI OUT	+0.20	
3	XTAL OSC	+1.57		8	POWER DOWN	+2.75	
4	XTAL OSC	+2.32		9	DATA OUT	+1.09	
5	VCC	+3.00		10	QUAD. IN	+3.00	

SR00497

Figure 7. Pin Functions

PIN FUNCTIONS (continued)

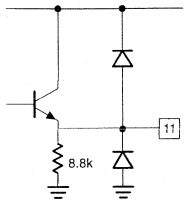
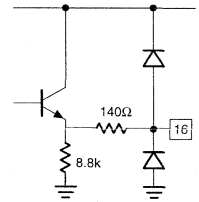
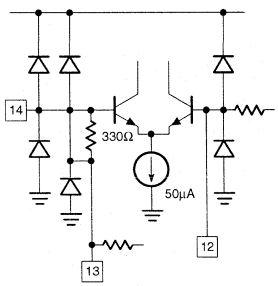
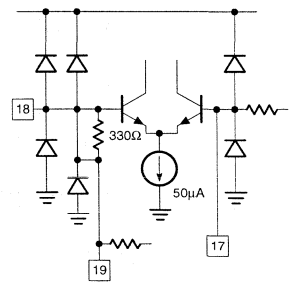
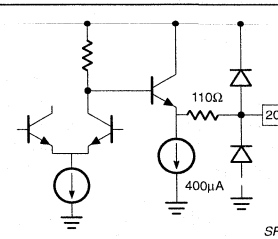
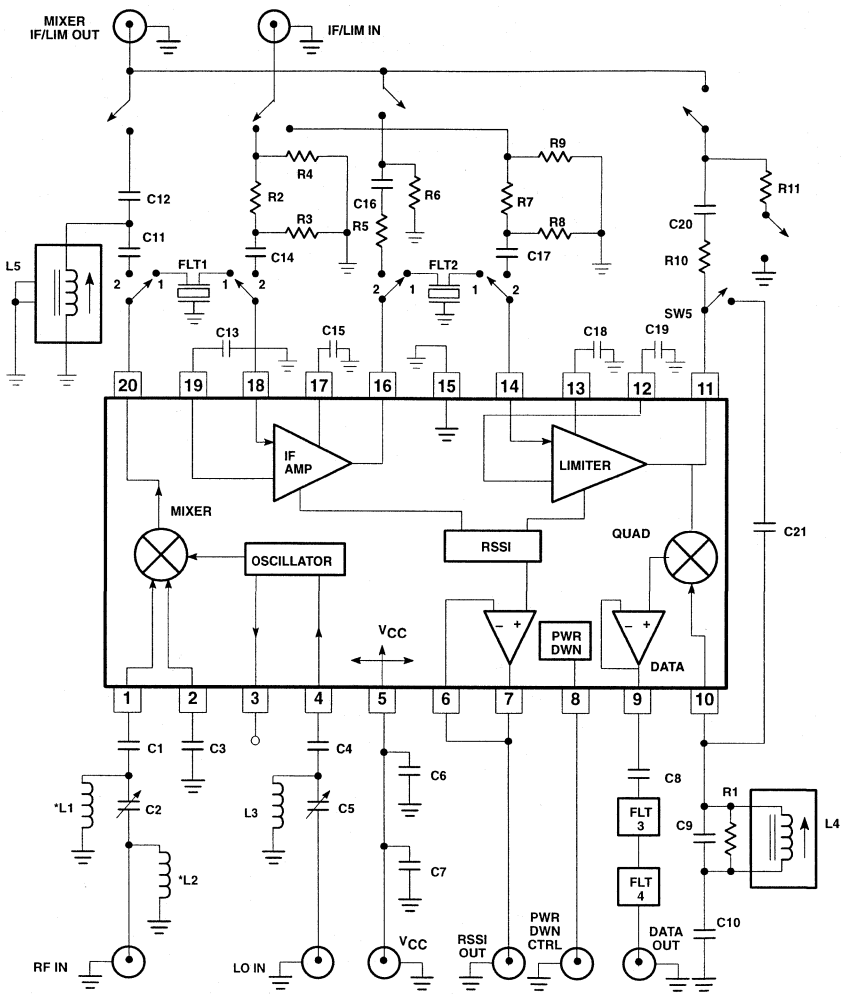
PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT	PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
11	LIMITER OUT	+1.35		16	IF AMP OUT	+1.22	
12	LIMITER DECOUP	+1.23		17	IF AMP DECOUP	+1.22	
13	LIMITER COUPLING	+1.23		18	IF AMP IN	+1.22	
14	LIMITER IN	+1.23		19	IF AMP DECOUP	+1.22	
15	GND	0		20	MIXER OUT	+1.03	

Figure 8. Pin Functions (cont.)



Automatic Test Circuit Component List

R1	8.2kΩ select	C1	0.1µF	C12	160pF select	L1	150nH select for input match
R2	6.42kΩ	C2	1–5pF select for input match	C13	1000pF	L2	22nH select for input match
R3	347.8Ω	C3	0.1µF	C14	0.1µF	L3	47nH select for input match
R4	49.9Ω	C4	0.1µF	C15	1000pF	L4	5.6µH select for input match
R5	1kΩ	C5	1–5pF select for input match	C16	0.1µF	L5	1.27–2.25µH select for mixer output match
R6	49.9Ω	C6	100pF	C17	0.1µF		
R7	6.42kΩ	*C7	6.8µF 10V	C18	1000pF	FLT1	10.7MHz (Murata SFE10.7MA5-A)
R8	347.8Ω	C8	1µF	C19	1000pF	FLT2	10.7MHz (Murata SFE10.7MA5-A)
R9	49.9Ω	C9	39pF select	C20	0.1µF	FLT3	"C" message weighted
R10	1kΩ	C10	0.1µF	C21	1pF	FLT4	Active de-emphasis
R11	49.9Ω	C11	0.1µF				

*NOTE: This value can be reduced when a battery is the power source.

SR00501

Figure 9. SA636 240.05MHz (RF) / 10.7MHz (IF) Test Circuit

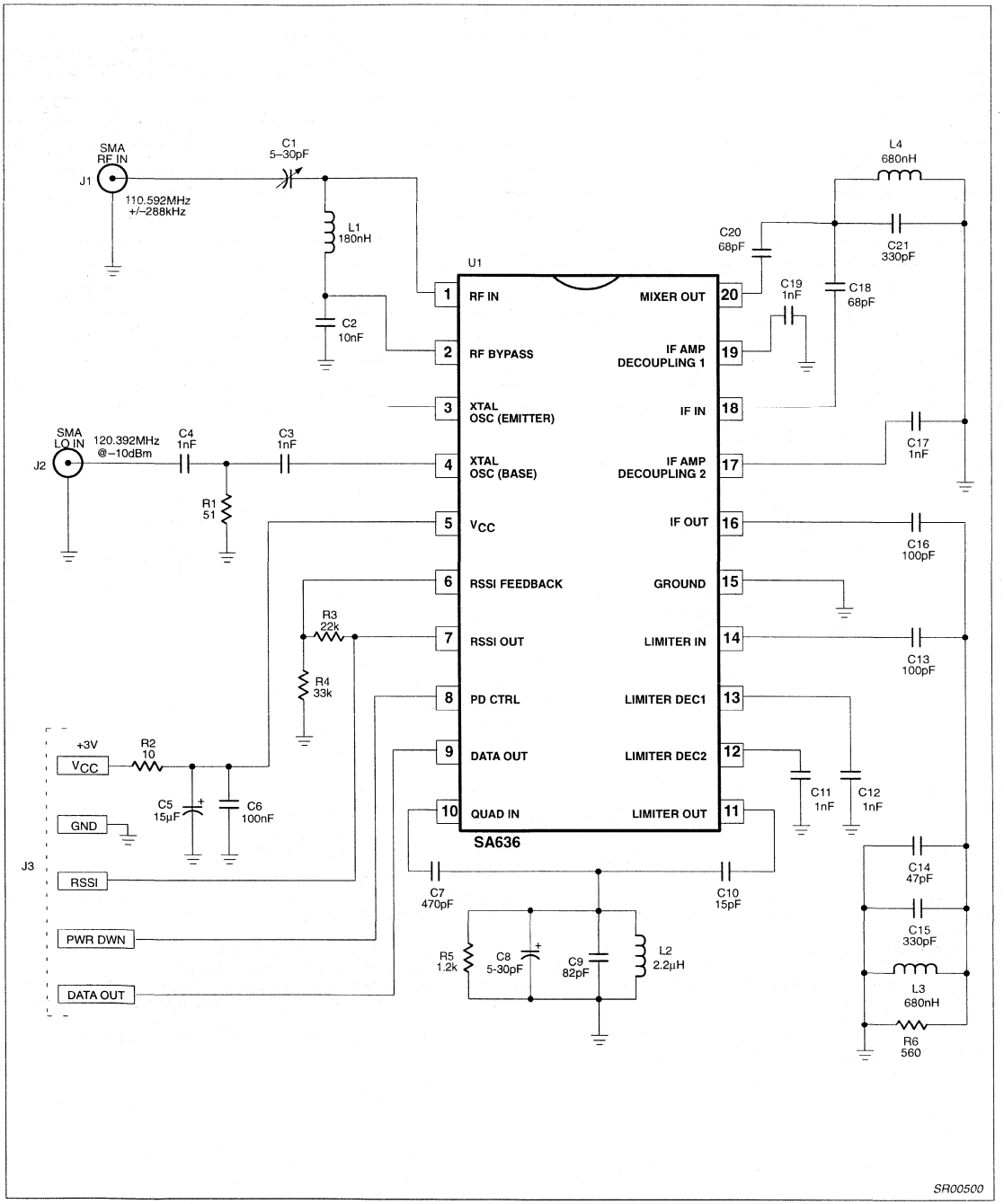


Figure 10. SA636 110.592MHz (RF) / 9.8MHz (IF) DECT Application Circuit

Table 1. DECT Application Circuit Electrical Characteristics

RF frequency = 110.592MHz; IF frequency = 9.8MHz; RF level = -45dBm; FM modulation = 100kHz with ±288kHz peak deviation.

SYMBOL	PARAMETER	TEST CONDITIONS	TYPICAL	UNITS
Mixer/Osc section (ext LO = 160mV$_{RMS}$)				
PG	Conversion power gain		13	dB
NF	Noise Figure at 110MHz		12	dB
IIP3	Third order input intercept	Matched f1 = 110.592; f2 = 110.892MHz	-15	dBm
R_{IN}	RF input resistance		690	Ω
C_{IN}	RF input capacitance		3.6	pF
IF section				
	IF amp gain	330Ω load	38	dB
	Limiter amp gain	330Ω load	54	dB
	Data level	R_{LOAD} = 3kΩ	130	mV$_{RMS}$
	3dB data bandwidth		700	kHz
RF/IF section (internal LO)				
	System RSSI output	RF level = -10dBm	1.4	V
	System S/N[1]	RF level = -83dBm	10	dB

NOTE:
1. 10dB S/N corresponds to BER = 10^{-3}.

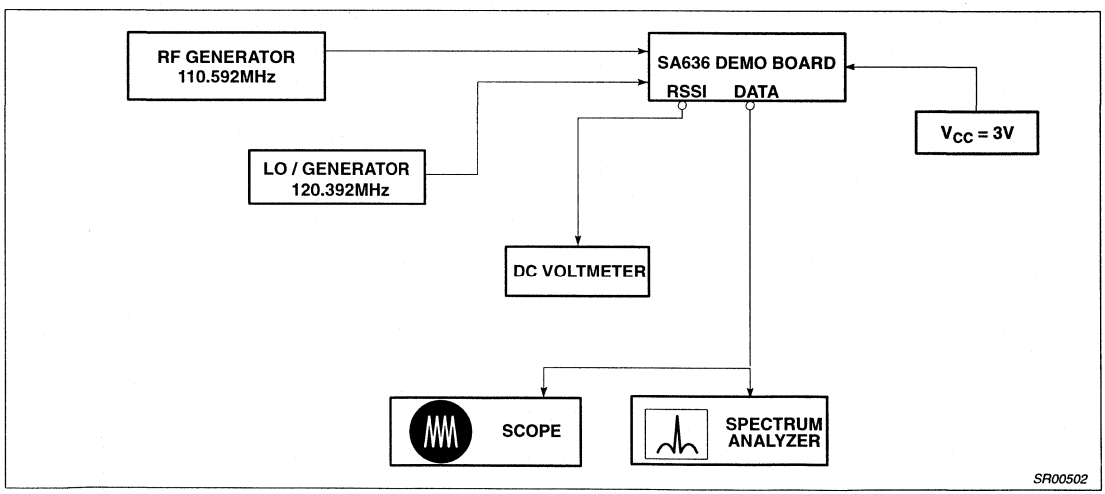
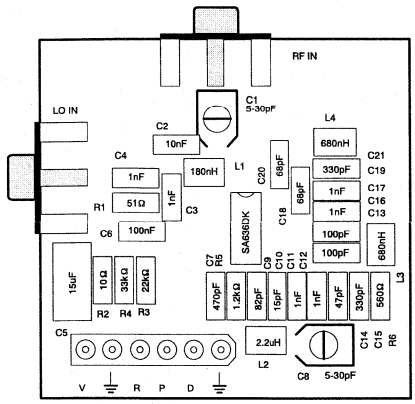
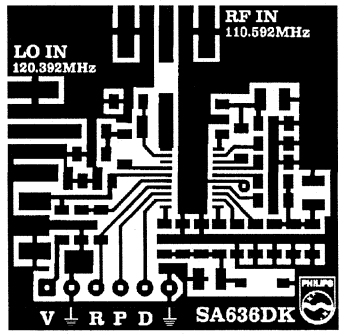


Figure 11. SA636 Application Circuit Test Set Up

NOTES:
1. RF generator: Set your RF generator at 110.592MHz, use a 100kHz modulation frequency and a ±288kHz deviation.
2. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
3. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 500mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
4. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 0.1µF bypass capacitor on the supply pin improves sensitivity.



TOP SILK SCREEN (SSOP)



TOP VIEW (SSOP)



BOTTOM VIEW (SSOP)

SR00503

Figure 12. SA636 Demoboard Layout (Not Actual Size)

CIRCUIT DESCRIPTION

The SA636 is an IF signal processing system suitable for second IF or single conversion systems with input frequency as high as 1GHz. The bandwidth of the IF amplifier is about 40MHz, with 38dB of gain from a 50Ω source. The bandwidth of the limiter is about 28MHz with about 54dB of gain from a 50Ω source. However, the gain/bandwidth distribution is optimized for 10.7MHz, 330Ω source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types, such as cordless and cellular hand-held phones.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 14dB, conversion gain of 11dB, and input third-order intercept of -16dBm. The oscillator will operate in excess of 1GHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

The output of the mixer is internally loaded with a 330Ω resistor permitting direct connection to a 10.7MHz ceramic filter for narrowband applications. The input resistance of the limiting IF amplifiers is also 330Ω. With most 10.7MHz ceramic filters and many crystal filters, no impedance matching network is necessary. For applications requiring wideband IF filtering, such as DECT, external LC filters are used (see Figure 10). To achieve optimum linearity of the log signal strength indicator, there must be a 6dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 6dB(v) insertion loss, a fixed or variable resistor can be added between the first IF output (Pin 16) and the interstage network.

The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

Overall, the IF section has a gain of 90dB. For operation at intermediate frequency at 10.7MHz. Special care must be given to layout, termination, and interstage loss to avoid instability.

The demodulated output (DATA) of the quadrature is a voltage output. This output is designed to handle a minimum bandwidth of 600kHz. This is designed to demodulate wideband data, such as in DECT applications.

A Receive Signal Strength Indicator (RSSI) completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPS or TACS cellular telephone, DECT and RCR-28 cordless telephone. This signal drives an internal op amp. The op amp is capable of rail-to-rail output. It can be used for gain, filtering, or 2nd-order temperature compensation of the RSSI, if needed.

NOTE: $dB(v) = 20\log V_{OUT}/V_{IN}$

Low-voltage digital IF receiver — SA637

DESCRIPTION

The SA637 is a low-voltage high performance monolithic digital system with high-speed RSSI incorporating a mixer, oscillator with buffered output, two limiting intermediate frequency amplifiers, fast logarithmic received signal strength indicator (RSSI), voltage regulator, RSSI op amp and power down pin. The SA637 is available in SSOP (shrink small outline package).

The SA637 was designed for portable digital communication applications and will function down to 2.7V. The limiter amplifier has differential outputs with 2MHz small signal bandwidth. The RSSI output has access to the feedback pin. This enables the designer to level adjust the outputs or add filtering.

FEATURES

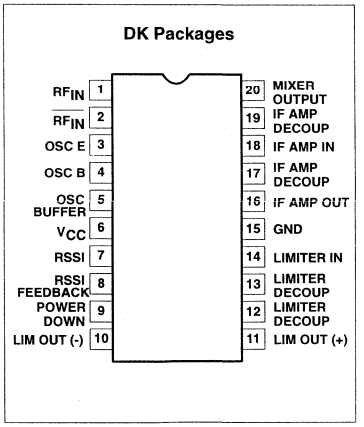
- V_{CC} = 2.7 to 5.5V
- Low power receiver (3.8mA @ 3V)
- Power down mode (I_{CC} = 110µA)
- Fast RSSI rise and fall times
- Extended RSSI range with temperature compensation
- RSSI op amp
- 2MHz limiter small signal bandwidth
- 455kHz filter matching (1.5kΩ)
- Differential limiter output
- Oscillator buffer
- SSOP-20 package

APPLICATIONS

- ADC (American Digital Cellular)
- Digital receiver systems
- Cellular radio

PIN CONFIGURATION

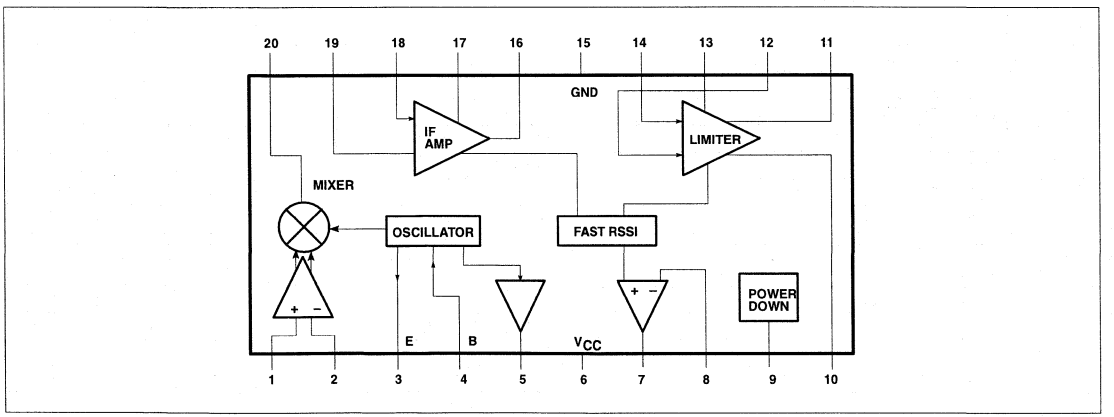
DK Packages



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Shrink Small Outline Package (Surface-mount)	-40 to +85°C	SA637DK	1563

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	-0.3 to +6.0	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{CC} + 0.3)	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range	-40 to +85	°C

NOTE: Thermal impedance (θ_{JA}) = 117°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		2.7		5.5	V
I_{CC}	DC current drain	Pin 9 = HIGH or OPEN		3.8	4.5	mA
		V_{CC} = 4.7V		4.4	5.5	mA
	Standby	Pin 9 = LOW		0.11	0.5	mA
	Input current	Pin 9 = LOW	-10		10	µA
		Pin 9 = HIGH	-10		10	µA
	Input level	Pin 9 = LOW	0		$0.3V_{CC}$	µA
		Pin 9 = HIGH	$0.7V_{CC}$		V_{CC}	µA
t_{ON}	Power up time	RSSI valid (10% to 90%)		10		µs
t_{OFF}	Power down time	RSSI invalid (90% to 10%)		5		µs

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +3V, unless otherwise stated. RF frequency = 90MHz; RF input step-up = +14.5dBV; IF frequency = 455kHz; RF level = -68dBm. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characteristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Mixer/Osc section						
f_{IN}	Input signal frequency			200		MHz
f_{OSC}	Crystal oscillator frequency			200		MHz
NF	Noise figure at 90MHz	Matched input and output		6.2		dB
TOI	Third-order input intercept point	Input matched to 50Ω source		-17		dBm
P1dB	Input 1dB compression point			-27		dBm
	Conversion power gain	Matched 50Ω		7		dB
R_{IN}	Mixer input resistance			2.5		kΩ
C_{IN}	Mixer input capacitance			2.2		pF
R_{OUT}	Mixer output resistance			1.87		kΩ
	Buffered LO output level	LO = 447mV_{P-P}, 1kΩ AC load	100	300	500	mV_{P-P}
IF section						
	IF amp power gain	50Ω source		36		dB
	Limiter power gain	50Ω source		60		dB
IF_{BW}	IF amp bandwidth			2.5		MHz

AC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
	RF RSSI output	RF level = -118dBm	.01	0.2	.65	V
		RF level = -68dBm	.4	0.9	1.7	V
		RF level = -28dBm	1.0	1.7	2.3	V
	RSSI range			90		dB
	RSSI accuracy			±1.5		dB
	RSSI ripple			30		mV_{P-P}
	RSSI speed Rise time	No interstage filter		2.5		µs
		With interstage filter		22		µs
	RSSI speed Fall time	No interstage filter		10		µs
		With interstage filter		50		µs
	IF input impedance			1.5		kΩ
	IF output impedance			1.5		kΩ
	Limiter input impedance			1.5		kΩ
	Limiter output impedance	(Pin 10, Pin 11)		200		Ω
	Limiter output signal level	(Pin 10, Pin 11) 1.5kΩ AC load		280		mV_{P-P}
	Limiter output DC level			1.27		V
	Differential output matching			±6		mV
	Differential output offset			±30		mV

CIRCUIT DESCRIPTION

Mixer

The mixer has a balanced input and is capable of being driven single-ended. The input impedance is 2.5kΩ in parallel with a 2.2pF cap at 90MHz RF. The mixer output can drive a 1500Ω ceramic filter at 455kHz or 600kHz directly without any matching required. The mixer conversion power gain is 7dB when both input and output are matched and optimum LO level is used to drive the internal mixer core.

Oscillator and Buffer

The on-board oscillator supplies the signal for the mixer down-conversion. The internally biased transistor can be configured as a Colpitts or Butler overtone crystal oscillator. The transistor's bias current can be increased if desired by adding a shunt resistor from Pin 3 to ground. The oscillator's buffered output (Pin 5) can be used as a feedback signal to lock the oscillator to an appropriate reference.

IF Amplifier and IF Limiter

The IF strip provides more than 95dB of power gain for the down converted signal. Its overall bandwidth is limited to 2MHz. The input and output impedance of the IF amplifier and the input impedance of the IF limiter are set to 1500Ω (match to 455kHz filter). A second filter is connected between the IF amplifier and the limiter for improved channel selectivity and reduced instability. This ceramic filter provides 3dB interstage insertion loss which results in optimal RSSI linearity. The overall gain can be reduced if desired by adding an external attenuator after the IF amplifier. The differential limiter outputs (Pins 10 and 11) are available for demodulator circuits.

RSSI

The received signal strength indicator provides a linear voltage indication of the received signal strength in dB for a range in excess of 90dB. The response time to a change in input signal is less than a few microseconds and the delay is kept to a minimum because of the use of a minimum phase shift circuit. Because of the speed of the RSSI circuit, the RSSI rise and fall time may, in practice, be dominated by the bandwidth of the external bandpass filter that is placed between the mixer and the IF, and the external filter placed between the IF amplifier and limiter. Since the RSSI function requires the signal to propagate through the whole IF strip, and the rise and fall time of the filters are inversely proportional to their bandwidth, there is a trade-off between channel selectivity and RSSI response. A possible solution is to use a second SA637 with wider band external filters for faster RSSI response.

The RSSI curve is temperature compensated and in addition is designed for improved consistency from unit to unit.

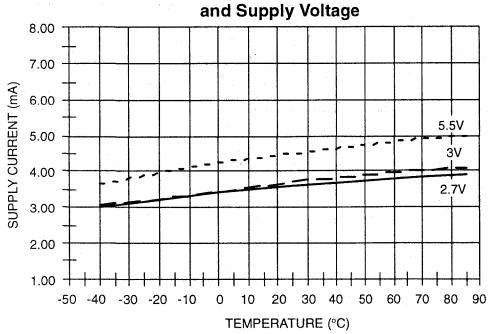
The RSSI circuit drives an on-chip low power op amp with rail-to-rail output which can be connected as a unity gain RSSI buffer or a gain stage or even a comparator.

DC Power Supply

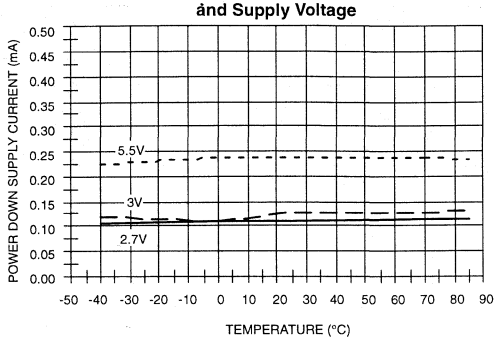
The IC is designed for operation between 2.7 and 5.5V. A power supply dependent biasing scheme is used in the mixers to benefit from the large headroom available at higher V_{CC}s.

PERFORMANCE CHARACTERISTICS

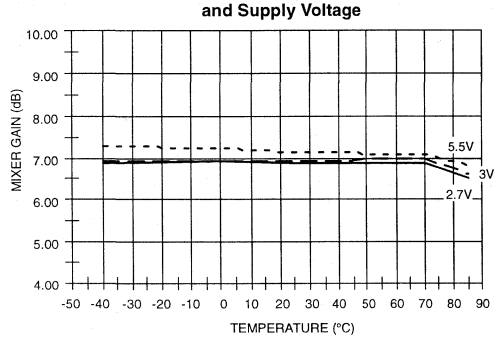
Supply Current vs Temperature and Supply Voltage



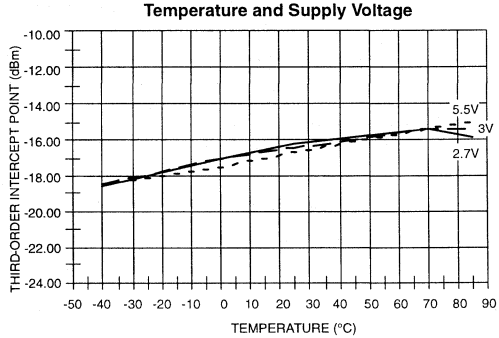
Power Down Supply Current vs Temperature and Supply Voltage



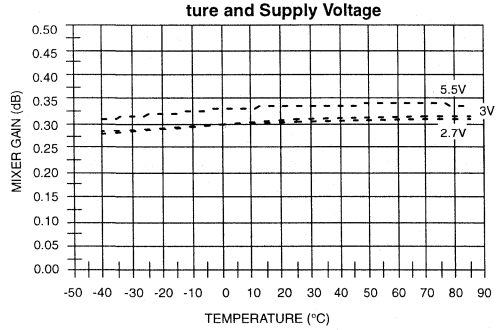
Mixer Power Gain vs Temperature and Supply Voltage



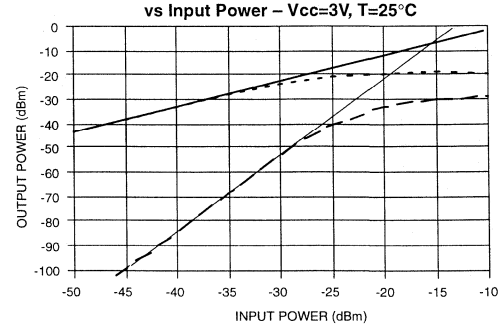
Mixer Third Order Input Intercept Point vs Temperature and Supply Voltage



Oscillator Buffer Output Level vs Temperature and Supply Voltage

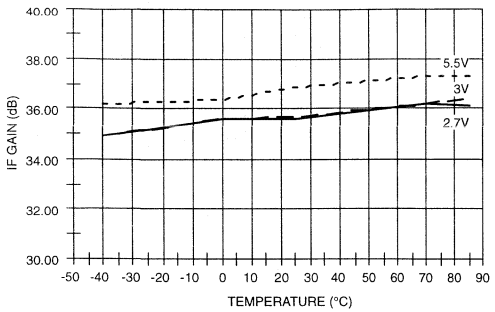


Mixer Third Order Intercept and Compression vs Input Power – Vcc=3V, T=25°C

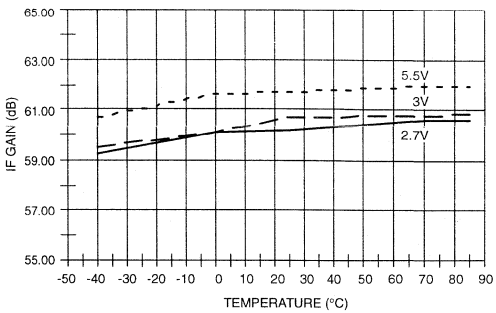


PERFORMANCE CHARACTERISTICS (cont.)

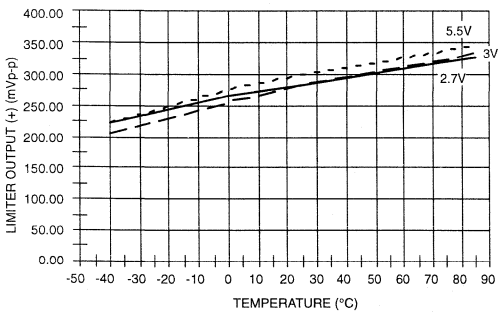
IF Power Gain vs Temperature and Supply Voltage



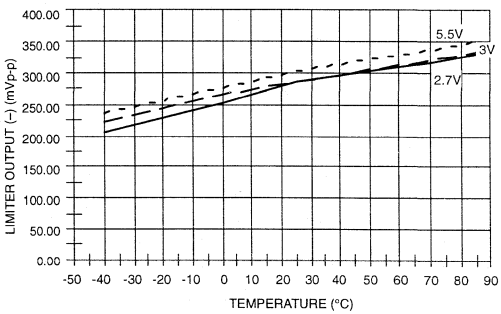
Limiter Power Gain vs Temperature and Supply Voltage



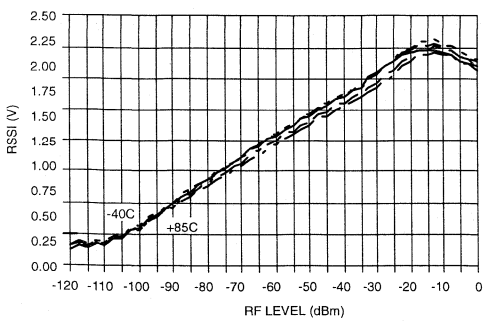
Limiter Output (+) Level vs Temperature and Supply Voltage



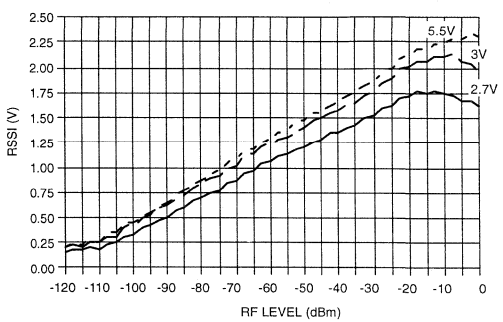
Limiter Output (–) Level vs Temperature and Supply Voltage



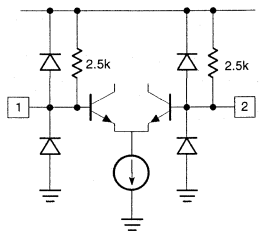
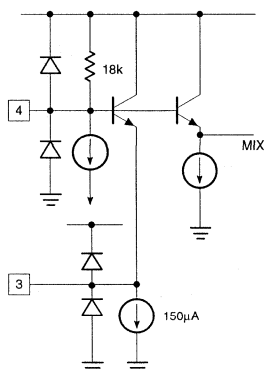
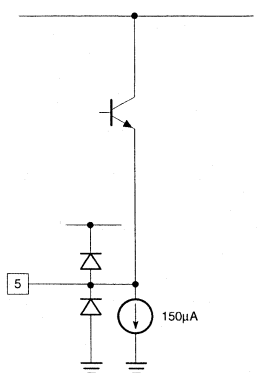
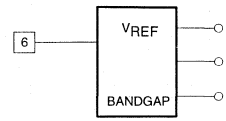
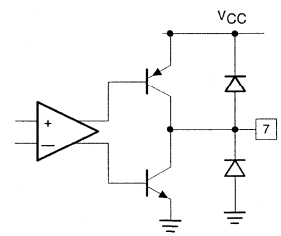
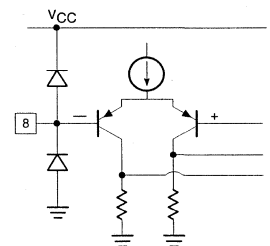
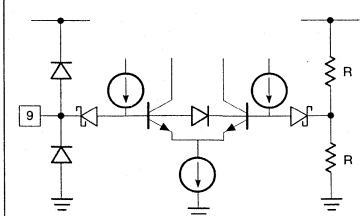
RSSI vs RF Level and Temperature – V_{CC} = 3V



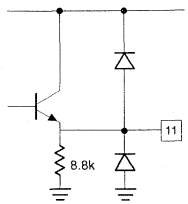
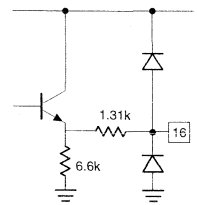
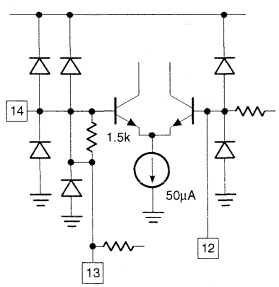
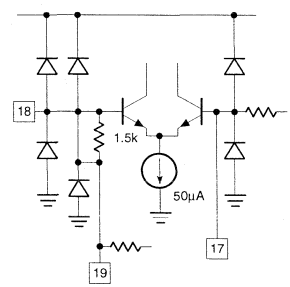
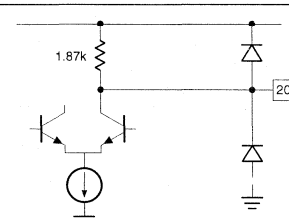
RSSI vs RF Level and Supply Voltage – Temperature = 25°C

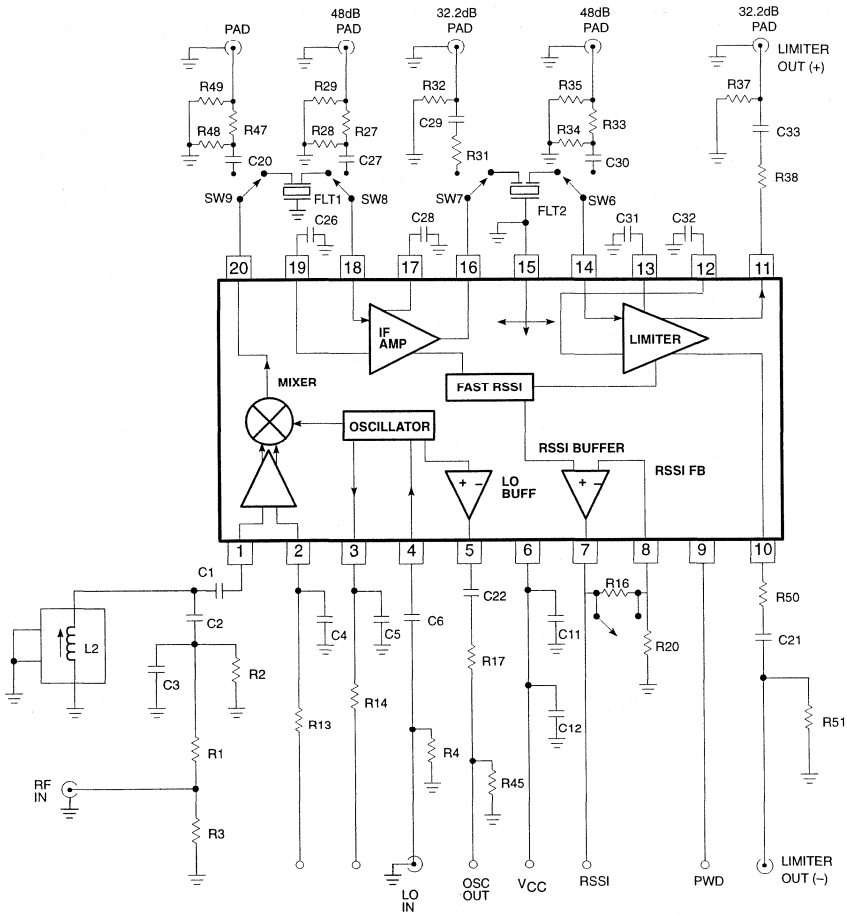


PIN FUNCTIONS

PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
1	RF IN	+1.40	
2	RF BYPASS	+1.40	
3	OSC E	+1.79	
4	OSC B	+2.56	
5	OSC BUFFER	+1.79	
6	V_{CC}	+3.00	
7	RSSI OUT	+0.20	
8	RSSI FEEDBACK	+0.20	
9	POWER DOWN	+2.00	

PIN FUNCTIONS (continued)

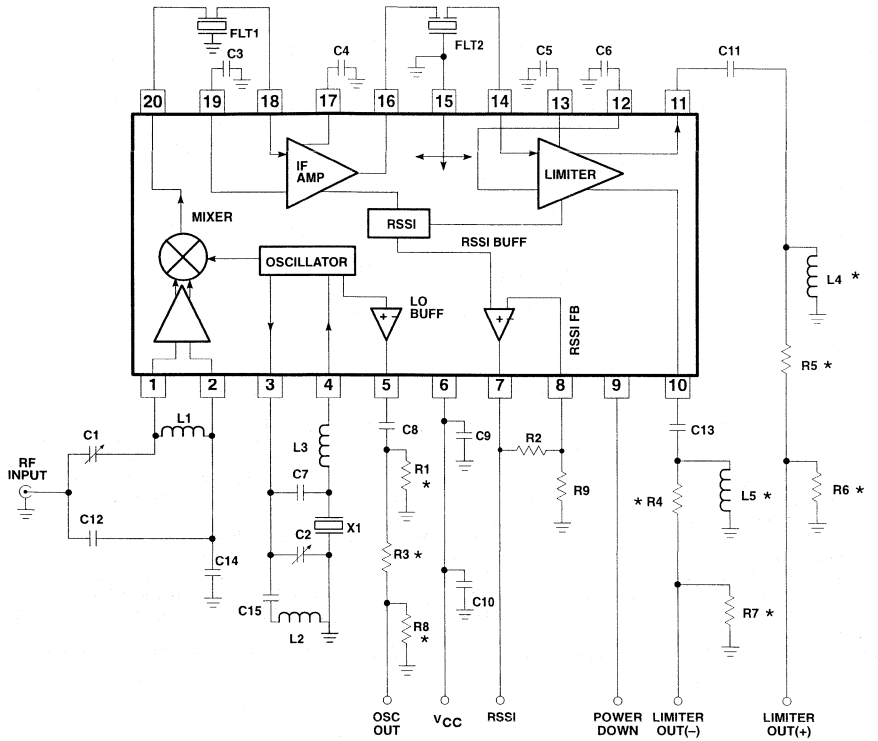
PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT	PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
10 11	LIMITER OUT	+1.25		16	IF AMP OUT	+1.28	
12	LIMITER DECOUP	+1.28		17	IF AMP DECOUP	+1.28	
13	LIMITER COUPLING	+1.28		18	IF AMP IN	+1.28	
14	LIMITER IN	+1.28		19	IF AMP DECOUP	+1.28	
15	GND	0		20	MIXER OUT	+2.03	



Automatic Test Circuit Component List

C1	10nF	C27	100nF	R4	49.9Ω	R32	49.9Ω	R32	49.9Ω
C2	91pF	C28	100nF	R13	10kΩ	R33	13.7kΩ	R50	1kΩ
C3	620pF	C29	100nF	R14	10kΩ	R34	1.68kΩ	R51	49.9Ω
C4	100nF	C30	100nF	R16	10kΩ	R35	49.9Ω	L2	62nH
C5	100nF	C31	100nF	R17	1kΩ	R38	1kΩ		
C6	10nF	C32	100nF	R20	10kΩ	R39	49.9Ω		
C11	100nF	C33	100nF	R27	13.7kΩ	R45	49.9Ω		
C20	100nF	R1	249Ω	R28	1.68kΩ	R47	2.43kΩ		
C21	100nF	R2	60.4Ω	R29	49.9Ω	R48	39.2kΩ		
C26	100nF	R3	60.4Ω	R31	1kΩ	R49	49.9Ω		

Figure 1. SA637 Automatic Test Circuit



Component List

C1	5-30pF	C9	0.1µF	R1	OPEN	L1	0.15µH PM20-R15M
C2	5-30pF	C10	1.0µF	R2	0Ω (short)	L2	0.15µH PM20-R15M
C3	0.1µF	C11	0.1µF	R3	1kΩ	L3	0.47µH PM20-R47M
C4	0.1µF	C12	68pF	R4	1.0kΩ	L4	OPEN
C5	0.1µF	C13	0.1µF	R5	2.0kΩ	L5	OPEN
C6	0.1µF	C14	0.1µF	R6	51Ω	FLT1	455kHz SFGCC 455BX-TC
C7	10pF	C15	1000pF	R7	100Ω	FLT2	455kHz SFGCC 455BX-TC
C8	0.1µF			R8	100Ω	X1	82.705MHz CTS XTAL 020-3249-042
				R9	OPEN		

* NOTE: These components are optional and depend on user matching requirements.
Pads are provided on the demo board.
R2 and R9 set the RSSI buffer gain. For unity gain short R2 (Pin 7 to Pin 8) and leave R9 open.

Figure 2. SA637 Application Circuit

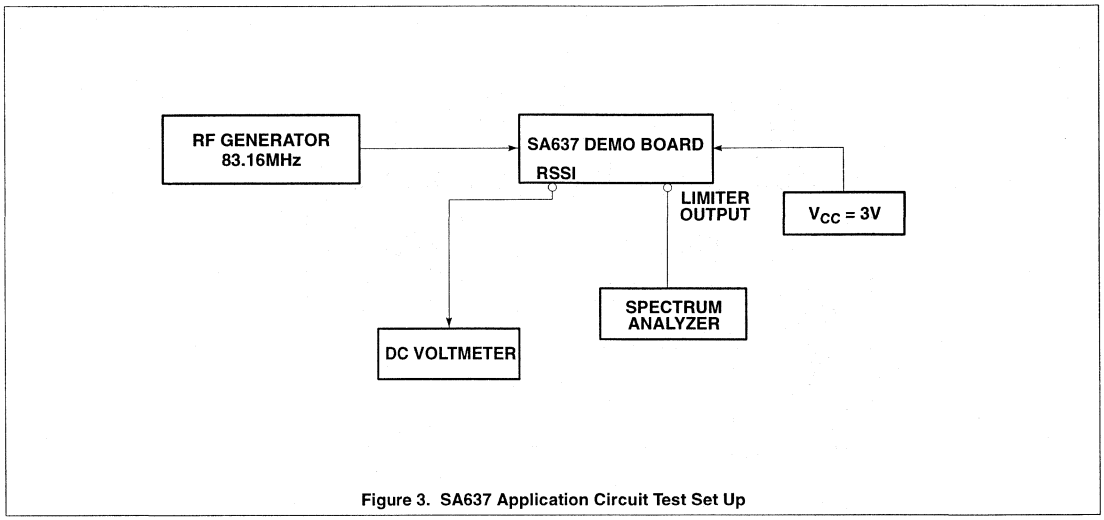
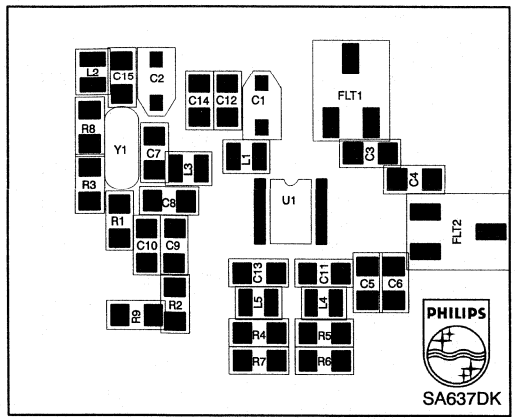
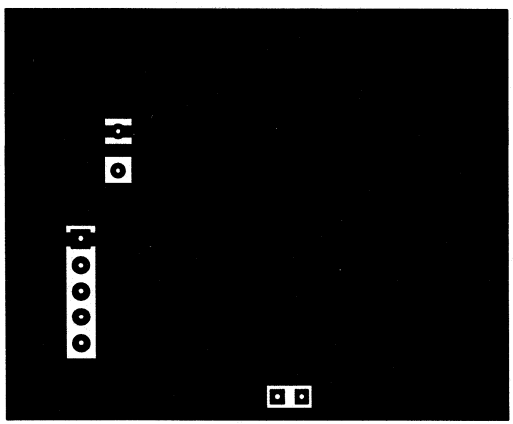


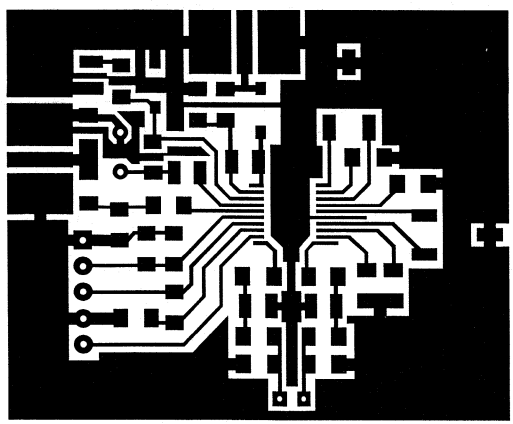
Figure 3. SA637 Application Circuit Test Set Up

NOTES:

1. Carrier-to-Noise (C/N): Connect a spectrum analyzer to Pin 10 or 11; set your RF generator to 83.16MHz or 455kHz above your LO frequency, modulation off; set the spectrum analyzer resolution bandwidth to 300Hz; and adjust your RF input level until the C/N = 26dB. Use video averaging. Assure that LIMOUT(+) and LIMOUT(–) are matched symetrically.
2. Ceramic filters: The ceramic filter can be SFGCC455BX-TC made by Murata which has 30kHz IF bandwidth.
3. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.45µV or -114dBm at the RF input.
4. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
5. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 500mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
6. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 0.1µF bypass capacitor on the supply pin improves sensitivity.


L2
C15
C2
C14
C12
C1
FLT1
R8
Y1
C7
L3
L1
C3
C4
R3
C8
U1
R1
FLT2
C10
C9
C13
C11
C5
C6
L5
L4
R9
R2
R4
R5
R7
R6
PHILIPS
SA637DK





Low voltage mixer FM IF system with filter amplifier and data switch

SA639

DESCRIPTION

The SA639 is a low-voltage high performance monolithic FM IF system with high-speed RSSI incorporating a mixer/oscillator, two wideband limiting intermediate frequency amplifiers, quadrature detector, logarithmic received signal strength indicator (RSSI), fast RSSI op amps, voltage regulator, wideband data output, post detection filter amplifier and data switch. The SA639 is available in 24-lead TSSOP (Thin shrink small outline package).

The SA639 was designed for high bandwidth portable communication applications and will function down to 2.7V. The RF section is similar to the famous NE605. The data output provides a minimum bandwidth of 1MHz to demodulate wideband data. The RSSI output is amplified and has access to the feedback pin. This enables the designer to level adjust the outputs or add filtering.

The post-detection amplifier may be used to realize a low pass filter function. A programmable data switch routes a portion of the data signal to an external integration circuit that generates a data comparator reference voltage.

SA639 incorporates a power down mode which powers down the device when Pin 8 is high. Power down logic levels are CMOS and TTL compatible with high input impedance.

PIN CONFIGURATION

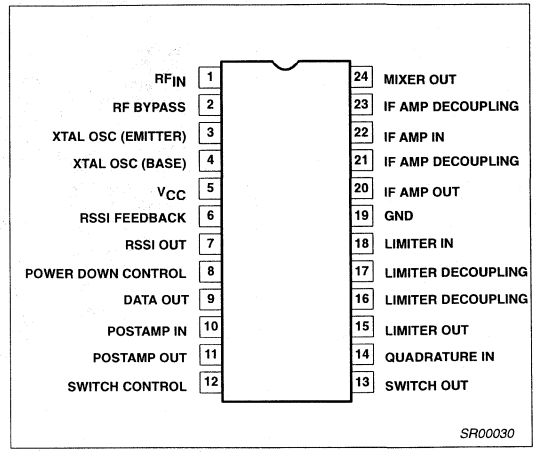


Figure 1. Pin Configuration

APPLICATIONS

- DECT (Digital European Cordless Telephone)
- FSK and ASK data receivers

FEATURES

- V_{CC} = 2.7 to 5.5V
- Low power consumption: 8.6mA typ at 3V
- Wideband data output (1MHz min.)
- Fast RSSI rise and fall times
- Mixer input to >500MHz
- Mixer conversion power gain of 9.2dB and noise figure of 11dB at 110MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator to 1GHz local oscillator can be injected)
- 92dB of IF Amp/Limiter power gain
- 25MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 80dB
- RSSI output internal op amp
- Post detection amplifier for filtering
- Programmable data switch
- Excellent sensitivity: 2.24μV into 50Ω matching network for 10dB SNR (Signal to Noise Ratio) with RF at 110MHz and IF at 9.8MHz
- ESD hardened
- Power down mode

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
24-Pin Plastic TSSOP (Thin Shrink Small Outline Package)	-40 to +85°C	SA639DH	SOT-355

BLOCK DIAGRAM

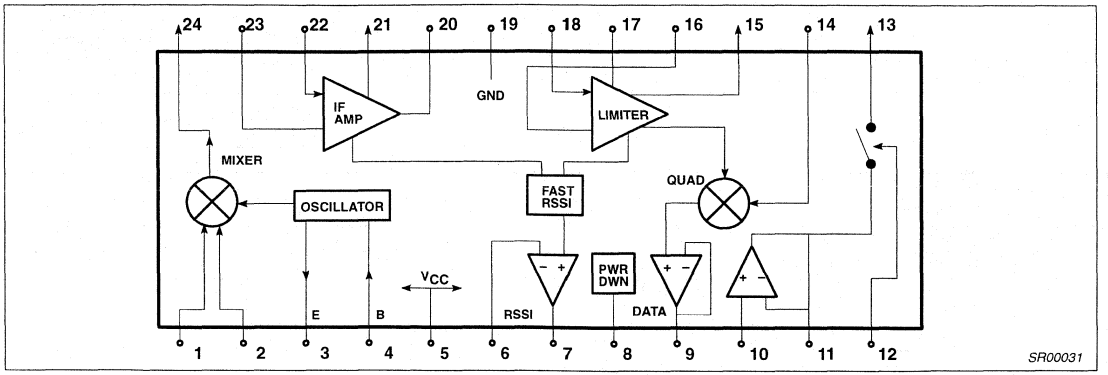


Figure 2. Block Diagram

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	-0.3 to 6	V
V_{IN}	Voltage applied to any other pin[1]	-0.3 to (V_{CC}+0.3)	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range SA639[2]	-40 to +85	°C

NOTE:
1. Except logic input pins (Pins 8 and 12) which can have 6V maximum.
2. θ_{JA} Thermal impedance (DH package) 117°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS SA639 MIN	-3σ	TYP	+3σ	MAX	UNITS
V_{CC}	Power supply voltage range		2.7		3.0		5.5	V
I_{CC}	DC current drain	Pin 8 = LOW, Pin 12 = HIGH		8.33	8.6	8.87	10	mA
I_{CC}	Standby	Pin 8 = HIGH, Pin 12 = HIGH		131.9	140	148.1	500	µA
	Input current	Pin 8 = LOW					10	µA
		Pin 8 = HIGH					4	
	Input level	Pin 8 = LOW	0				$0.3V_{CC}$	V
		Pin 8 = HIGH[NO TAG]	$0.7V_{CC}$				6	
t_{ON}	Power up time	RSSI valid (10% to 90%)			10			µs
t_{OFF}	Power down time	RSSI invalid (90% to 10%)			5			µs
	Power up settling time	Data output valid			100		200	µs
	Switch closed	Pin 12 = LOW, PIN 8 = LOW	0				$0.3\ V_{CC}$	V
	Switch open (output tri-state)	Pin 12 = HIGH	$0.7\ V_{CC}$				6	V
	Input current	Pin 12 = LOW					10	µA
		Pin 12 = HIGH					4	
	Switch activation time				0.5		1	µs

NOTE:
1. When the device is forced in power down mode via Pin 8, the Data Switch will output a voltage close to 1.6V and the state of the switch control input will have no effect.

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +3V, unless otherwise stated. RF frequency = 110.592MHz ;LO frequency = 120.392MHz; IF frequency = 9.8MHz; RF level = -45dBm; FM modulation = 576kHz with ±288kHz peak deviation, discriminator tank circuit Q=4. The parameters listed below are tested using automatic test equipment to assure consistent electrical characteristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNITS
			SA639					
			MIN	-3σ	TYP	+3σ	MAX	
Mixer/Osc section (ext LO = -14dBm)								
f_{IN}	Input signal frequency				500			MHz
f_{OSC}	External oscillator (buffer)		0.2		500			MHz
	Noise figure at 110MHz			10.4	11	11.6		dB
	Third-order input intercept point	Matched f1=110.592MHz; f2=110.852MHz		-11	-9.5	-8		dBm
	Conversion power gain		6	8.6	9.2	11.1		dB
	RF input resistance	Single-ended input			800			Ω
	RF input capacitance				3.5			pF
	Mixer output resistance	(Pin 24)			330			Ω
IF section								
	IF amp gain			38.86	40	41.14		dB
	Limiter gain			50.44	52	53.56		dB
	Input limiting -3dB	Test at Pin 22			–100			dBm
	IF input impedance				330			Ω
	IF output impedance				330			Ω
	Limiter input impedance				330			Ω
	Limiter output impedance				300			Ω
	Limiter output level with no load				130			mV_{RMS}
RF/IF section (ext LO = -14dBm)								
	Data level	R_L = 10kΩ, C_L = 30pF	260		360			mV_{P-P}
	Data bandwidth			2.1	2.4	2.7		MHz
S/N	Signal-to-noise ratio	No modulation for noise		56.1	60	63.9		dB
	AM rejection	80% AM 1kHz		34.8	36	37.2		dB
	RF RSSI output with buffer	RF level = -90dBm	0	0.232	0.4	0.568	0.75	V
		RF level = -45dBm	0.5	0.732	0.9	1.068	1.3	
		RF level = -10dBm	0.8	1.032	1.2	1.368	1.6	
	RF RSSI output rise time (10kHz pulse, w/ 9.8MHz filter) (no RSSI bypass capacitor)	IF frequency = 9.8MHz RF level = -45dBm			0.8			µs
		RF level = -28dBm			0.8			
	RF RSSI output fall time (10kHz pulse, w/ 9.8MHz filter) (no RSSI bypass capacitor)	IF frequency = 9.8MHz RF level = -45dBm			2.0			µs
		RF level = -28dBm			1.8			
	RSSI range				80			dB
	RSSI accuracy				±1.5			dB
	SINAD	RF level = -85dBm		9.45	12	14.55		dB
	S/N	RF level = -100dBm		5.8	10	14.2		dB

AC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS SA639 MIN	-3σ	TYP	+3σ	MAX	UNITS
Post detection filter amplifier								
	Amplifier 3dB bandwidth	AC coupled: R_L = 10kΩ, C_L = 30pF		3.85	4.75	5.65		MHz
	Amplifier gain	AC coupled: R_L = 10kΩ, $V_{OUT\ DC}$ = 1.6V		-0.39	-0.3	-0.21		dB
	Slew rate	AC coupled: R_L = 10kΩ, C_L = 30pF			14.0			V/μs
	Input resistance		300					kΩ
	Input capacitance						3	pF
	Output impedance				250		600	Ω
	Output load resistance	AC coupled	5					kΩ
	Output load capacitance[1]	AC coupled			30			pF
	DC output level[2]		1.5	1.682	1.7	1.718	1.9	V
Data switch								
	DC input voltage range[3]		1.2		1.6		2.0	V
	AC input swing				400			mV_{P-P}
	Input impedance		100					kΩ
	Input capacitance						5	pF
	Output load resistance				500			Ω
Through Mode (Pin 12 = LOW)								
	AC voltage gain[4]				-1.5			dB
	Output drive capability	Sink/source, $V_{OUT\ DC}$ = 1.6V	3					mA
	Slew rate	$V_{OUT\ DC}$ = 1.6V			>14.0			V/μs
	Static offset voltage[5]	$V_{IN\ DC}$ = 1.2 to 2.0V		-0.6	0.30	1.2	±5	mV
	Dynamic offset voltage[2, 6]	$V_{IN\ DC}$ = 1.4 to 2.0V; V_{CC} = 3.0 to 5.0V; RF level = -70 to -40 dBm	-7				+7	mV
		$V_{IN\ DC}$ = 1.4 to 2.0V; V_{CC} = 3.0 to 5.0V; RF level = -40 to -5 dBm	-10				+10	
Tri-State Mode (Pin 12 = HIGH)								
	Output leakage current	$V_{OUT\ DC}$ = 1.2 to 2.0V		9.5	20	30.5	100	nA

NOTES:
1. Includes filter feedback capacitance, comparator input capacitance. PCB stray capacitances and switch input capacitance.
2. Demodulator output DC coupled with Post Detection Filter Amplifier input and the demodulator tank exactly tuned to center frequency.
3. Includes DC offsets due to frequency offsets between Rx and Tx carrier and demodulator tank offset due to mis-tuning.
4. With a 400mV_{P-P} sinusoid at 600kHz driving Pin 10. Output load resistance 500Ω in series with 10nF.
5. With a DC input and capacitor in the RC load fully charged.
6. The switch is closed every 10ms for a duration of 40μs. The DC offset is determined by calculating the difference of 2 DC measurements, which are determined as follows: 1) The first DC value is measured at the integrating capacitor of the switch when the switch is in the closed position immediately before it opens. The value to be measured is in the middle of the peak-to-peak excursion of the superimposed sine-wave. (DClow + (DChigh – DClow)/2). 2) The second DC value (calculated as above) is measured at Pin 11 immediately after the switch opens, and is the DC value which gives the largest DC offset to the first DC measurement within a 400μs DECT burst. Minimum and maximum limits are not tested, however, they are guaranteed by design and characterization using an optimized layout and application circuit.
7. Standard deviations are measured based on application of 60 parts.

CIRCUIT DESCRIPTION

The SA639 is an IF signal processing system suitable for second IF or single conversion systems with input frequency as high as 1GHz. The bandwidth of the IF amplifier is about 40MHz, with 44dB(v) of gain from a 50Ω source. The bandwidth of the limiter is about 28MHz with about 58dB(v) of gain from a 50Ω source. However, the gain/bandwidth distribution is optimized for 9.8MHz, 330Ω source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types, such as digital cordless phones.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 11dB, conversion power gain of 9.2dB, and input third-order intercept of -9.5dBm. The oscillator will operate in excess of 1GHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

The output of the mixer is internally loaded with a 330Ω resistor permitting direct connection to a 330Ω ceramic filter. The input resistance of the limiting IF amplifiers is also 330Ω. With most 330Ω ceramic filters and many crystal filters, no impedance matching network is necessary. To achieve optimum linearity of the log signal strength indicator, there must be a 6dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 6dB(v) insertion loss, a fixed or variable resistor can be added between the first IF output (Pin 20) and the interstage network.

The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

Overall, the IF section has a gain of 90dB. For operation at intermediate frequency at 9.8MHz. Special care must be given to layout, termination, and interstage loss to avoid instability.

The demodulated output (DATA) of the quadrature is a low impedance voltage output. This output is designed to handle a minimum bandwidth of 1MHz. This is designed to demodulate wideband data, such as in DECT applications.

Post Detection Filter Amplifier

The filter amplifier may be used to realize a group delay optimized low pass filter for post detection. The filter amplifier can be configured for Sallen & Key low pass with Bessel characteristic and a 3dB cut frequency of about 800kHz.

The filter amplifier provides a gain of 0dB. The output impedance is less than 500Ω in order to reduce frequency response changes as a result of amplifier load variations. The filter amplifier has a 3dB bandwidth of at least 4 MHz in order to keep the amplifier's frequency response influence on the filter group delay characteristic at a minimum. At the center of the carrier it is mandatory to provide a filter output DC bias voltage of 1.6V in order to be within the input common mode range of the external data comparator. The filter output DC bias voltage specification holds for an exactly center tuned demodulator tank and for the demodulator output connected to the filter amplifier input.

Data Switch

The SA639 incorporates an active data switch used to derive the data comparator reference voltage by means of an external integration circuit. The data switch is typically closed for 10µs before and during reception of the synchronization word pattern, and is otherwise open. The external integration circuit is formed by an R/C low pass with a time constant of 5 to 10µs.

The active data switch provides excellent tracking behavior over a DC input range of 1.2 to 2.0V. For this range with an RC load (no static current drawn), the DC output voltage will not differ more than ±5mV from the input voltage. Since the active data switch is designed to behave like a non-linear charge pump (to allow fast tracking of the input signal without slew rate limitations under dynamic conditions of a 576kHz input signal with 400mV$_{P-P}$ and the RC load), the output signal will have a 340mV$_{P-P}$ output with a DC average that will not vary from the input DC average by more than ±10mV.

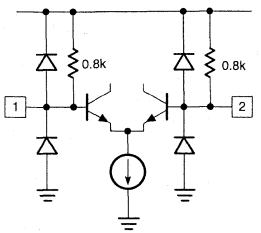
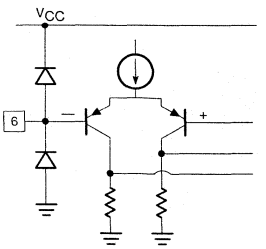
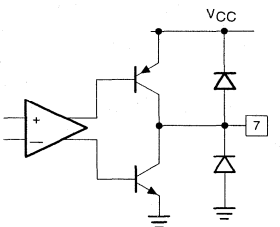
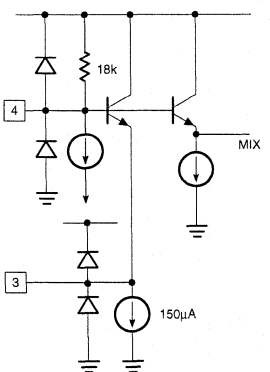
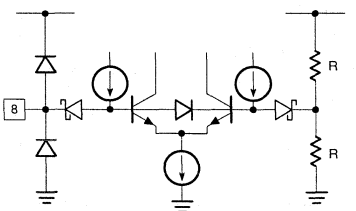
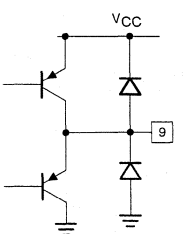
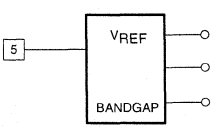
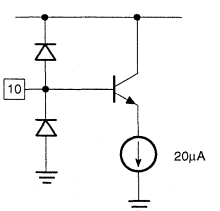
The data switch is able to sink/source 3mA from/to the external integration circuit in order to minimize the settling time after long power-down periods (DECT paging mode). In addition, during power-down conditions a reference voltage of approximately 1.6V will be used as the input to the switch. The switch will be in a low current mode to maintain the voltage on the external RC load. This will further reduce the settling time of the capacitor after power-up. It should be noted that during power-down the switch can only source and sink a trickle current (10µA). Thus, the user should make sure that other circuits (like the data comparator inputs) are not drawing current from the RC circuit.

The data switch provides a slew rate better than 1V/µs in order to track with system DC offset from receive slot to receive slot (DECT idle lock or active mode). When the data switch is opened the output is in a tri-state mode with a leakage current of less than 100nA. This reduces discharge of the external integration circuit. When powered-down, the data switch will output a reference of approximately 1.6V to maintain a charge on the external RC circuit.

A Receive Signal Strength Indicator (RSSI) completes the circuitry. The output range is greater than 80dB and is temperature compensated. This log signal strength indicator exceeds the criteria for DECT cordless telephone. This signal drives an internal op amp. The op amp is capable of rail-to-rail output. It can be used for gain, filtering, or 2nd-order temperature compensation of the RSSI, if needed.

NOTE: dB(v) = 20log V_{OUT}/V_{IN}

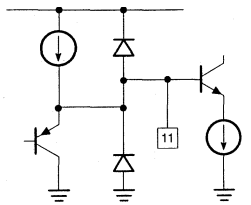
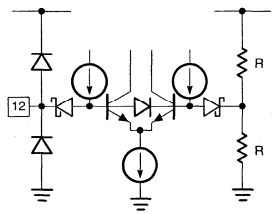
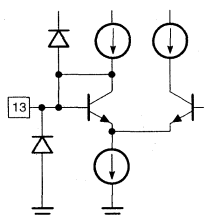
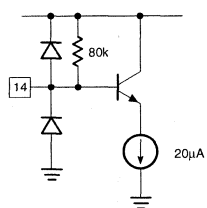
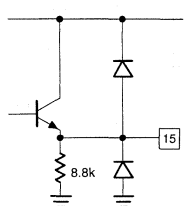
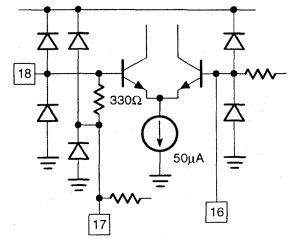
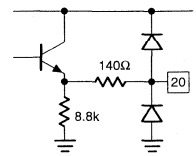
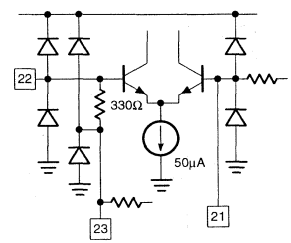
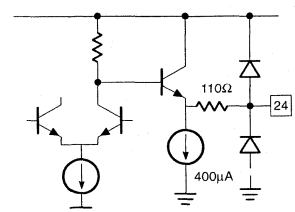
PIN FUNCTIONS All DC voltages measured with Pin 8 = Pin 12 = Pin 19 = 0V, Pin 5 = 3V and Pin 9 connected to Pin 10.

PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT	PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
1	RF IN	+1.07		6	RSSI FEEDBACK	+0.20	
2	RF BYPASS	+1.07		7	RSSI OUT	+0.20	
3	XTAL OSC	+1.57		8	POWER DOWN	0.00	
4	XTAL OSC	+2.32		9	DATA OUT	+1.7	
5	V_{CC}	+3.00		10	POST AMP IN	+1.70	

SR00032

Figure 3. Pin Functions

PIN FUNCTIONS (continued)

PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
11	POST AMP OUT	+1.70	
12	SWITCH CONTROL	0.00	
13	SWITCH OUT	+1.70	
14	QUAD IN	+3.00	
15	LIMITER OUT	+1.35	
16	LIMITER DECOUP	+1.23	
17	LIMITER COUPLING	+1.23	
18	LIMITER IN	+1.23	
19	GND	0	
20	IF AMP OUT	+1.22	
21	IF AMP DECOUP	+1.22	
22	IF AMP IN	+1.22	
23	IF AMP DECOUP	+1.22	
24	MIXER OUT	+1.03	

SR00033

Figure 4. Pin Functions (cont.)

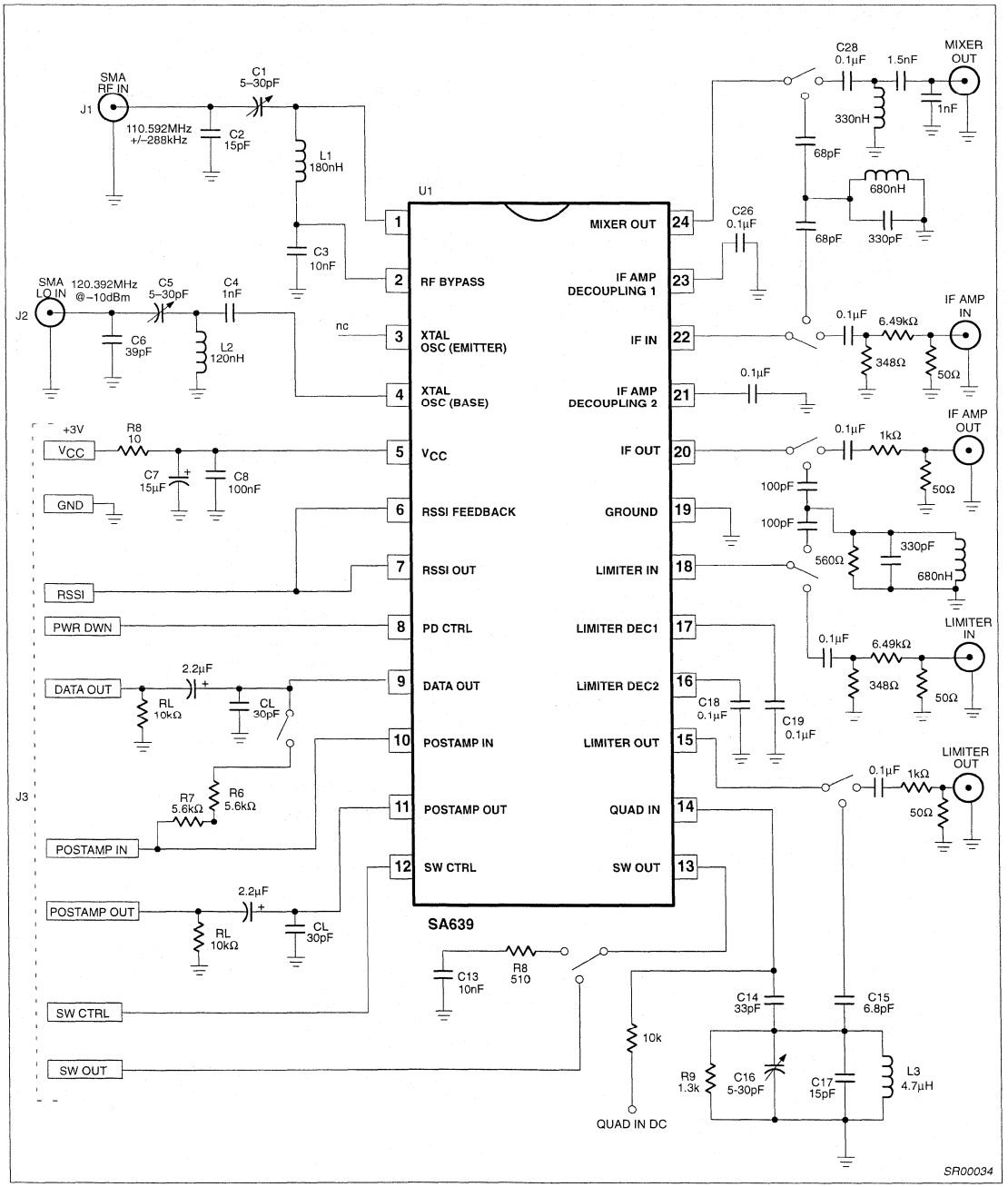


Figure 5. SA639 Test Circuit

TYPICAL PERFORMANCE CHARACTERISTICS

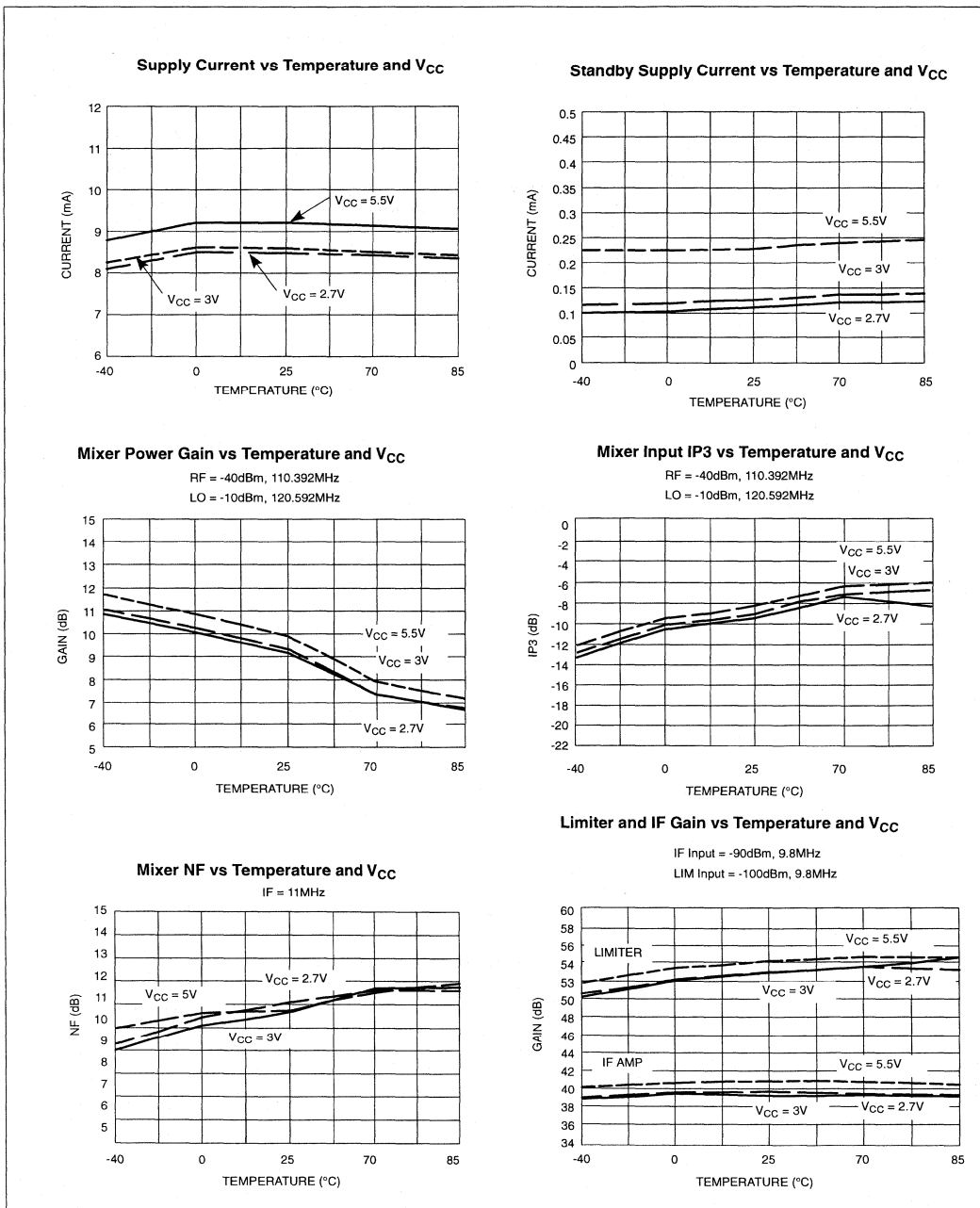


Figure 6. Typical Performance Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

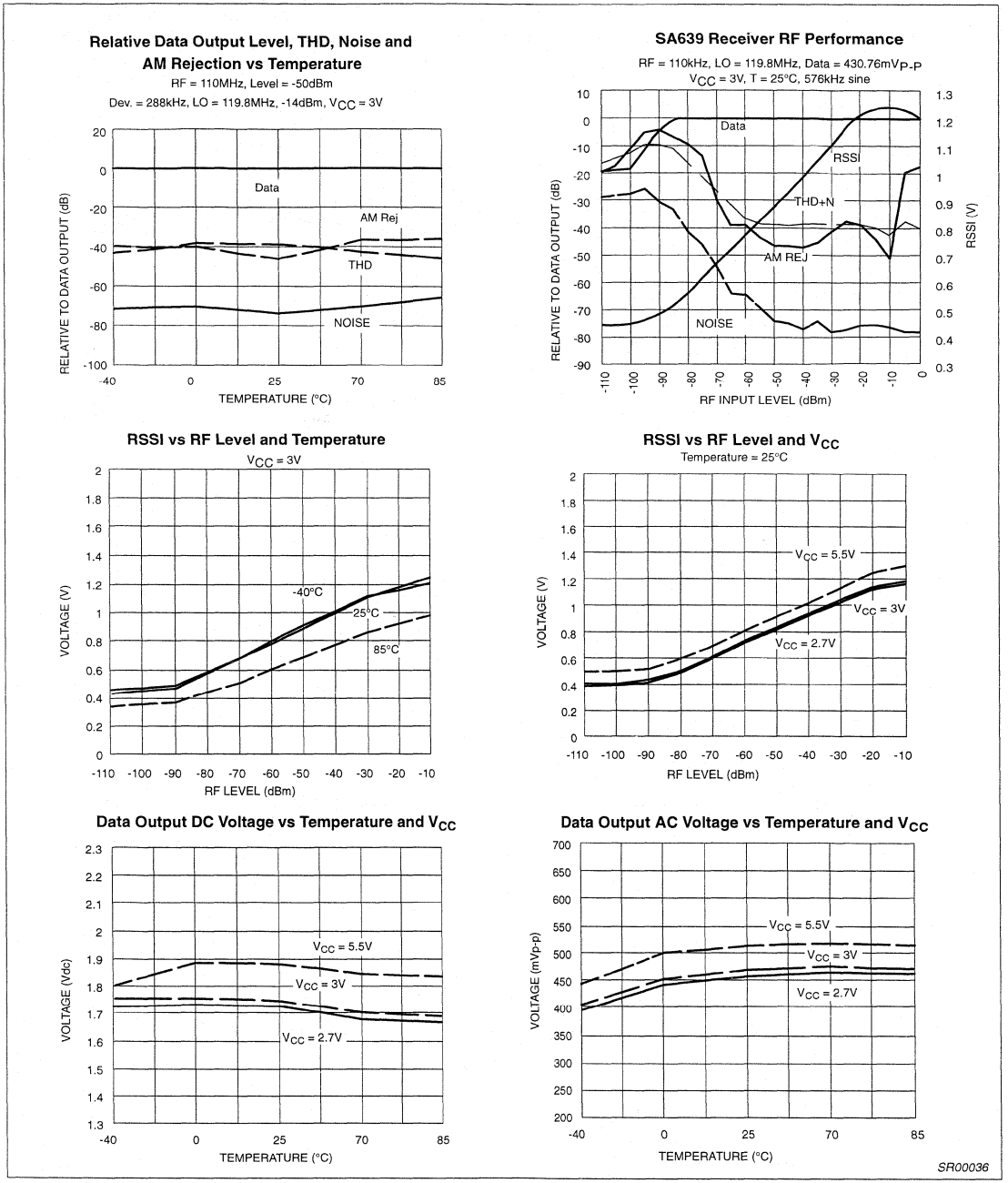
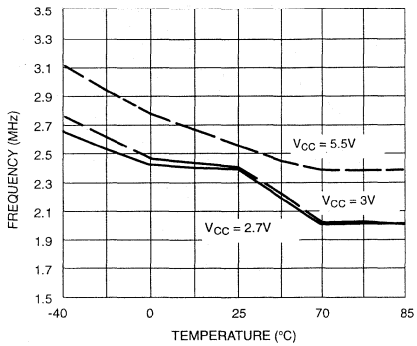


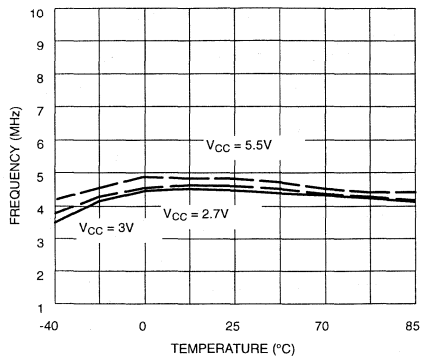
Figure 7. Typical Performance Characteristics (cont.)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

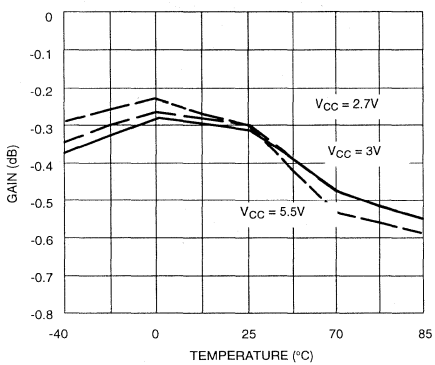
Data Output -3dB Bandwidth vs Temperature and V_{CC}



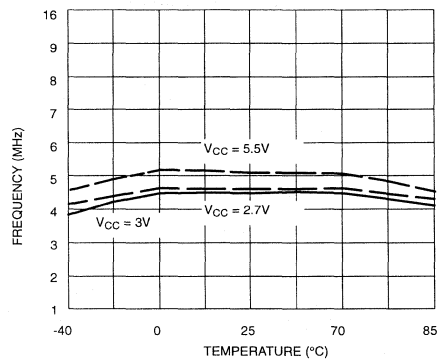
Switch -3dB Bandwidth vs Temperature and V_{CC}



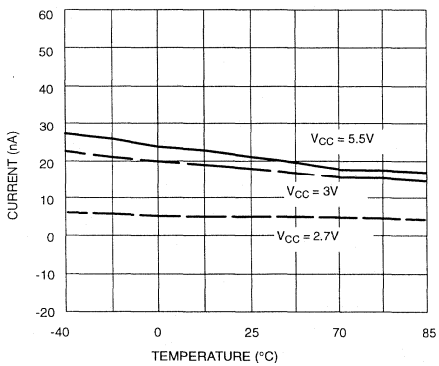
Post Detection Amplifier vs Temperature and V_{CC}



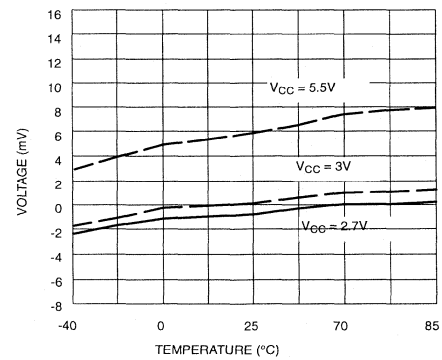
Post Detection Amplifier -3dB Bandwidth vs Temperature and V_{CC}



Switch Output Leakage Current vs Temperature and V_{CC}



Switch Output to Input Offset Voltage vs Temperature and V_{CC}



SR00037

Figure 8. Typical Performance Characteristics (cont.)

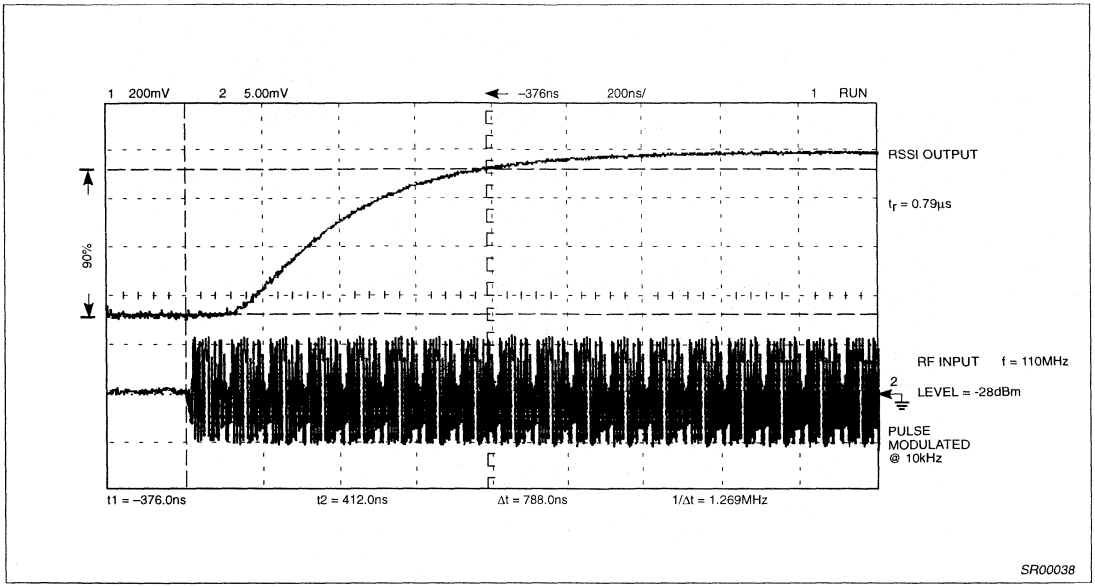


Figure 9. SA639 RSSI Rise Time

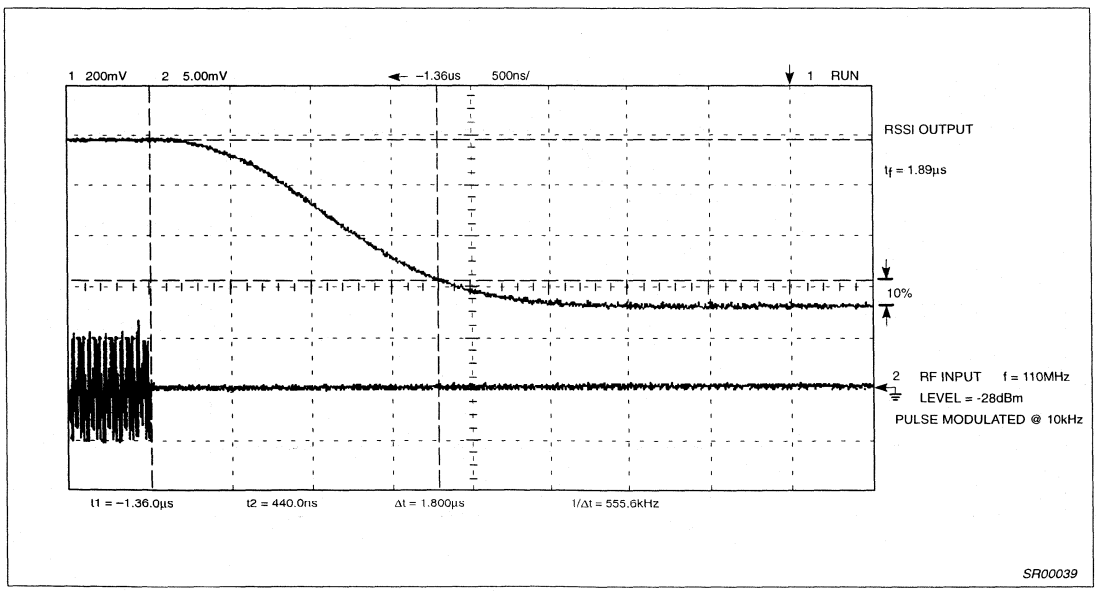


Figure 10. SA639 RSSI Fall Time

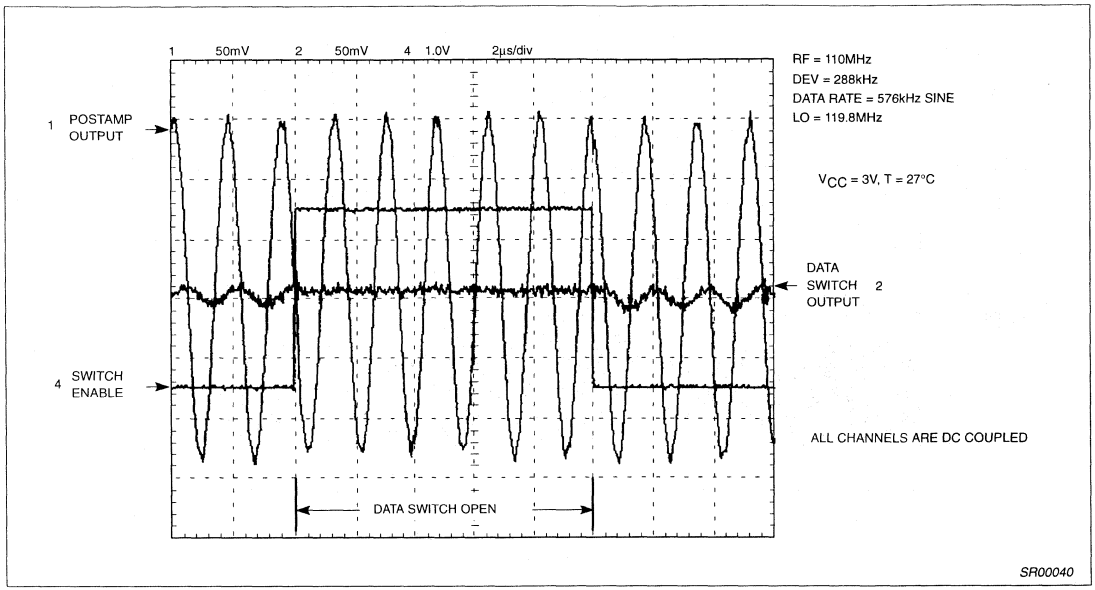


Figure 11. SA639 System Dynamic Response

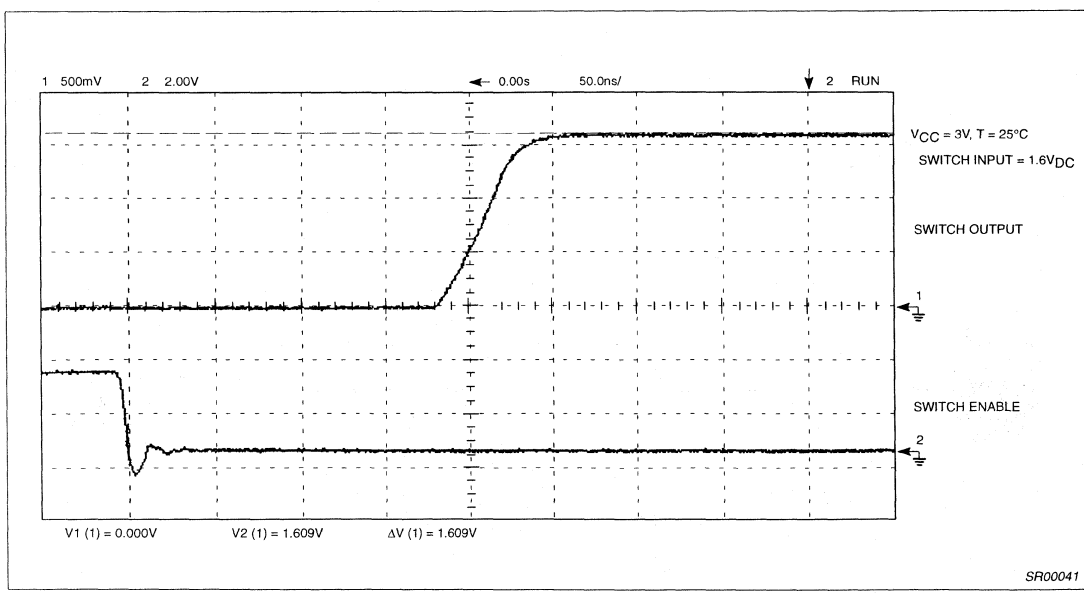


Figure 12. SA639 Data Switch Activation Time

Low-voltage digital IF receiver SA647

DESCRIPTION

The SA647 is a low-voltage high performance monolithic digital system with high-speed RSSI incorporating a mixer, oscillator with buffered output, two limiting intermediate frequency amplifiers, fast logarithmic received signal strength indicator (RSSI), voltage regulator, RSSI op amp and power down pin. The SA647 is available in TSSOP (thin shrink small outline package).

The SA647 was designed for portable digital communication applications and will function down to 2.7V. The limiter amplifier has differential outputs with 2MHz small signal bandwidth. The RSSI output has access to the feedback pin. This enables the designer to level adjust the outputs or add filtering.

FEATURES

- V_{CC} = 2.7 to 5.5V
- Low power receiver (5.3mA @ 3V)
- Power down mode (I_{CC} = 110µA)
- Fast RSSI rise and fall times
- Extended RSSI range with temperature compensation
- RSSI op amp
- 2MHz limiter small signal bandwidth
- Filter matching (1.5kΩ)
- Differential limiter output
- Oscillator buffer
- TSSOP-20 package

APPLICATIONS

- NADC (North American Digital Cellular)
- Digital receiver systems
- Cellular radio

PIN CONFIGURATION

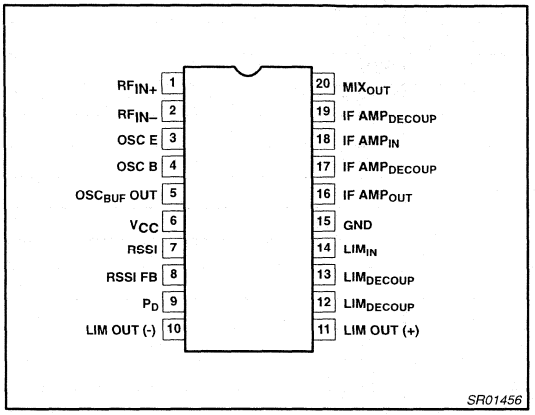


Figure 1. Pin Configuration

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Thin Shrink Small Outline Package (Surface-mount)	–40 to +85°C	SA647DH	SOT360–1

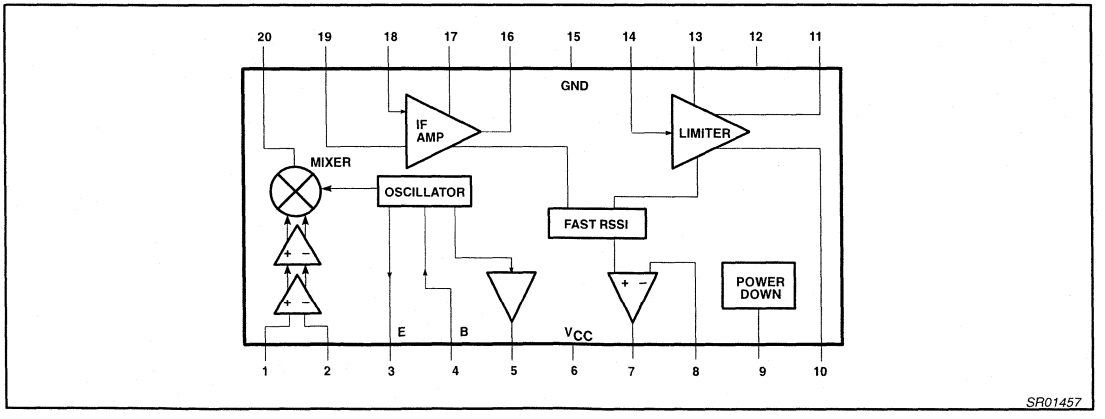


Figure 2. Block Diagram

PIN DESCRIPTION

PIN NO.	SYMBOL	FUNCTION
1	RF_{IN+}	RF input +
2	RF_{IN-}	RF input–decoupling
3	OSC_E	Oscillator emitter
4	OSC_B	Oscillator base (input)
5	$OSC_{BUF}OUT$	Oscillator buffer output
6	V_{CC}	Supply voltage
7	RSSI	RSSI output
8	RSSI FB	RSSI Feedback
9	P_D	Power Down
10	$LIM_{OUT(-)}$	Limiter output (neg)
11	$LIM_{OUT(+)}$	Limiter output (pos)
12	LIM_{DECOUP}	Limiter decoupling
13	LIM_{DECOUP}	Limiter decoupling
14	LIM_{IN}	Limiter input
15	GND	Ground
16	IF AMP_{OUT}	IF amplifier output
17	IF AMP_{DECOUP}	IF amplifier decoupling
18	IF AMP_{IN}	IF amplifier input
19	IF AMP_{DECOUP}	IF amplifier decoupling
20	MIX_{OUT}	Mixer output

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	-0.3 to +6.0	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{CC} + 0.3)	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range	-40 to +85	°C

NOTE: Thermal impedance (θ_{JA}) = 135°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3.0V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		2.7		5.5	V
I_{CC}	DC current drain		4	5.3	7	mA
	Standby	Pin 9 = LOW		0.11		mA
	Input current	Pin 9 = LOW	-10		10	µA
		Pin 9 = HIGH	-10		10	
	Input level	Pin 9 = LOW	0		0.3V_{CC}	V
		Pin 9 = HIGH	0.7 V_{CC}		V_{CC}	
τ_{on}	Power–up time	RSSI valid (10% to 90%)		10		µsec
τ_{off}	Power–down time	RSSI valid (90% to 10%)		5		µsec

AC ELECTRICAL CHARACTERISTICS

V_{CC} = +3.0V, Mixer input freq = 110.52MHz, LO input freq = 109.92MHz, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Mixer/Osc section						
f_{IN}	Input signal frequency				200	MHz
f_{OSC}	Crystal oscillator frequency				200	MHz
NF	Noise figure at 110.52MHz	Matched input and output 50Ω		4.5		dB
IIP3	Third-order input intercept point	Matched input and output to 50Ω		-29.5		dBm
G_{CP}	Conversion power gain	Matched input and output to 50Ω	17	20	23	dB
R_{IN}	Mixer input resistance	at 110.52 MHz		670		Ω
C_{IN}	Mixer input capacitance	at 110.52 MHz		3.0		pF
R_{OUT}	Mixer output resistance	at 600 kHz		1.5		kΩ
I_{SOL}	Mixer RF to LO isolation			32		dB
	Buffered LO output level, DC coupled	10kII3.9pF load	110	230	320	mV_{P-P}
	External input level	f = 110.52 MHz at Pin 4	250			mV_{P-P}
IF section						
	IF amp power gain	Matched input and output 50Ω	30	36		dB
	Limiter power gain		51	60		dB
IF_{BW}	IF amp bandwidth			2		MHz
	RSSI output	Input power level = -113dBm, Pin 1		0.30		V
		Input power level = -68dBm, Pin 1		1.00		V
		Input power level = -29dBm, Pin 1		1.55		V
	RSSI range			85		dB
	RSSI accuracy			±1.5		dB
	RSSI ripple			30		mV_{P-P}
	RSSI speed – (Rise Time) Input @ Pin 1	No filter		5		µs
	RSSI speed – (Fall time) Input @ Pin 1	No filter		25		µs
	IF input impedance			1.5		kΩ
	IF output impedance			1.5		kΩ
	Limiter input impedance			1.5		kΩ
	Limiter output impedance	(Pin 10, Pin 11)		230		Ω
	Limiter output (each pin)	Output load is 1.5K in parallel with 30 pF to GND each pin	240	350	420	mV_{P-P}
	Limiter output DC level			1.27		V
	Differential output matching			±5		mV
	Limiter output offset			0.09		V

CIRCUIT DESCRIPTION

Mixer

The mixer has a single–ended input. The input impedance is 670Ω in parallel with a 3.0pF cap at 110.52MHz RF. The mixer output can drive a 1500Ω ceramic filter without any matching required.

Oscillator and Buffer

The on-board oscillator supplies the signal for the mixer down-conversion. The internally biased transistor can be configured as a Colpitts or Butler overtone crystal oscillator. The transistor's bias current can be increased if desired by adding a shunt resistor from Pin 3 to ground. The oscillator's buffered output (Pin 5) can be used as a feedback signal to lock the oscillator to an appropriate reference.

IF Amplifier and IF Limiter

The IF strip provides more than 96dB of power gain for the down converted signal. Its bandwidth is 2MHz. The input and output impedance of the IF amplifier and the input impedance of the IF limiter are set to 1500Ω. A second filter is connected between the IF amplifier and the limiter for improved channel selectivity and reduced instability. The overall gain can be reduced if desired by adding an external attenuator after the IF amplifier The differential limiter outputs (Pins 10 and 11) are available for demodulator circuits.

RSSI

The received signal strength indicator provides a linear voltage indication of the received signal strength in dB for a typical range of 85dB. The response time to a change in input signal is less than a few microseconds and the delay is kept to a minimum because of the use of a minimum phase shift circuit. Because of the speed of the RSSI circuit, the RSSI rise and fall time will be dominated by the bandwidth of the external bandpass filter that is placed between the mixer and the IF. Since the RSSI function requires the signal to propagate through the whole IF strip, and the rise and fall time of the filters are inversely proportional to their bandwidth, there is a trade-off between channel selectivity and RSSI response. Therefore, it is recommended that all channel selection filters be placed before the IF strip, just after the mixer. This will make the delay of the RSSI independent of the mixer input signal amplitude. Also, a 6dB insertion loss between the IF and limiter sections (Pins 16 and 14) will give optimum flatness of RSSI versus mixer input signal.

The RSSI curve is temperature compensated and in addition is designed for improved consistency from unit to unit.

DC Power Supply

The IC is designed for operation between 2.7 and 5.5V. A power supply dependent biasing scheme is used in the mixers to benefit from the large headroom available at higher V_{CC}s.

PERFORMANCE CHARACTERISTICS

V_{CC} = +3.0V, Mixer input freq = 110.52MHz, LO input freq = 109.92MHz, T_A = 25°C; unless otherwise stated.

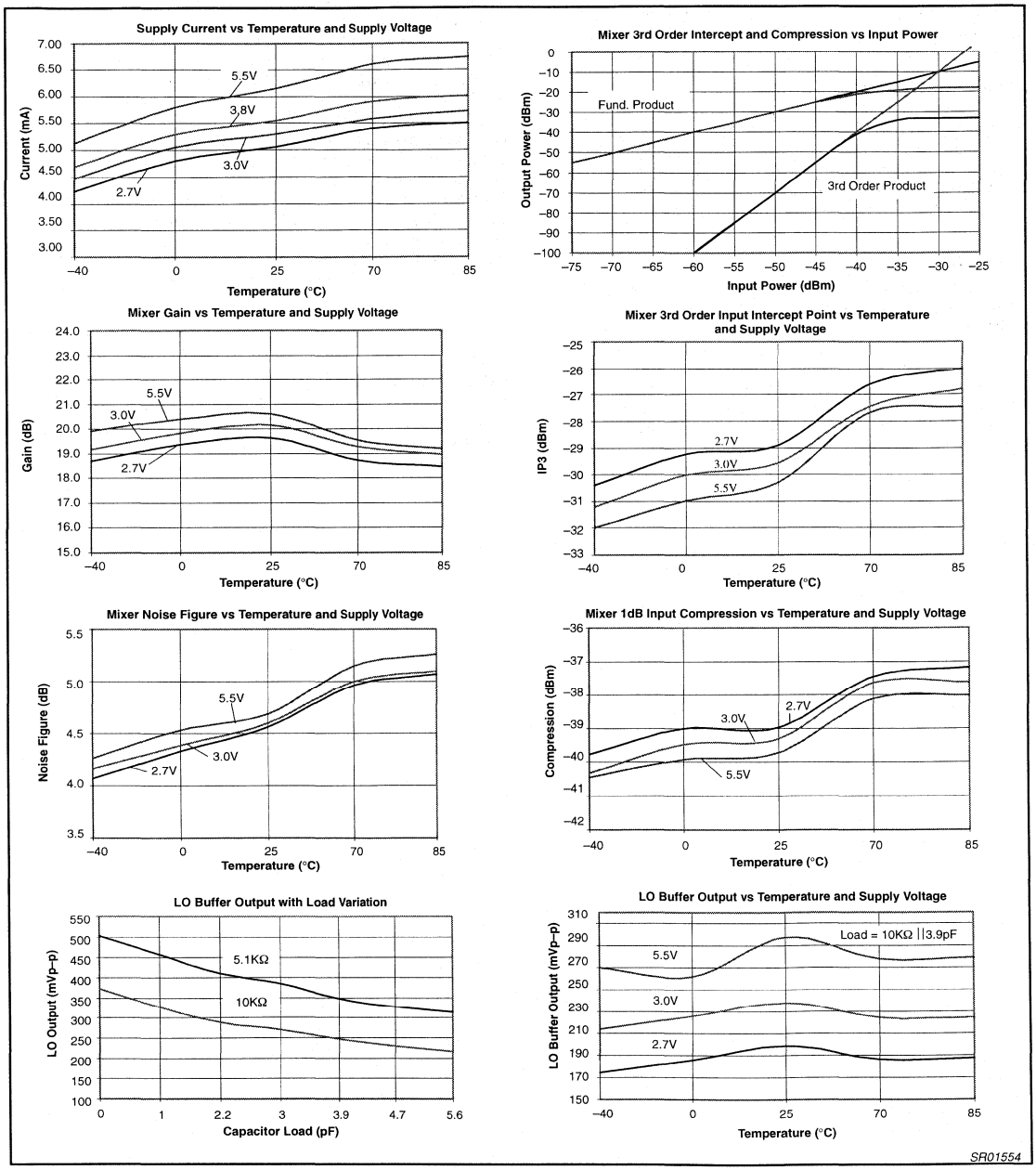


Figure 3.

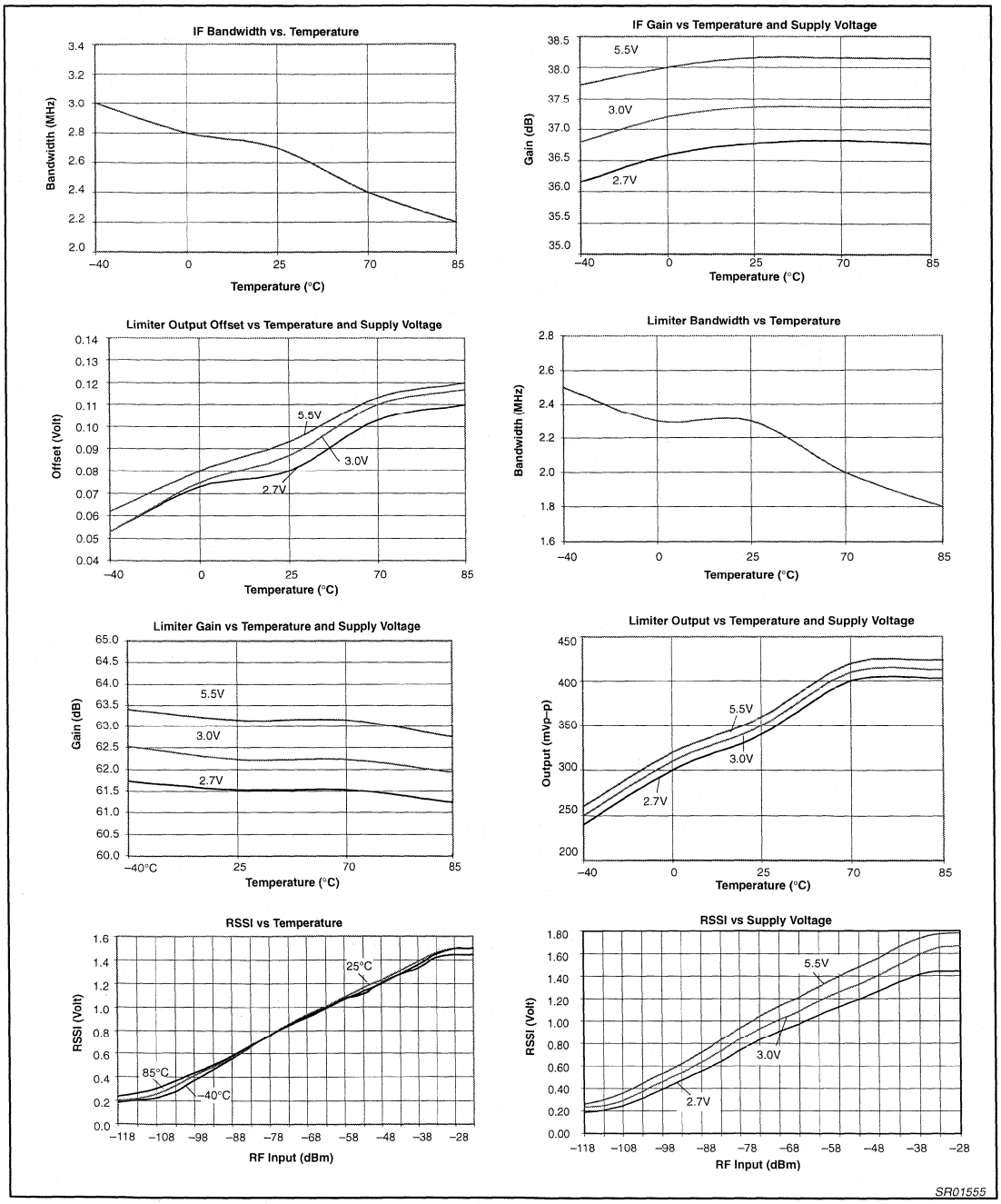
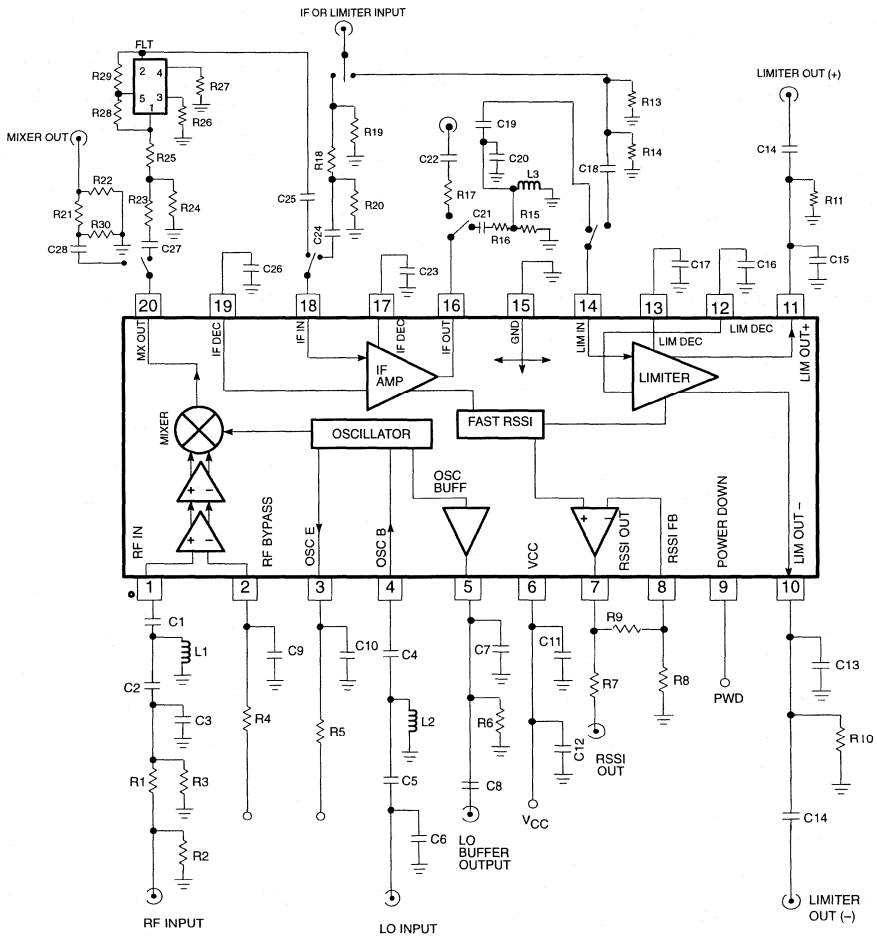

IF Bandwidth vs. Temperature
Bandwidth (MHz)
3.4
3.2
3.0
2.8
2.6
2.4
2.2
2.0
−40
0
25
70
85
Temperature (°C)
IF Gain vs Temperature and Supply Voltage
Gain (dB)
38.5
38.0
37.5
37.0
36.5
36.0
35.5
35.0
5.5V
3.0V
2.7V
−40
0
25
70
85
Temperature (°C)
Limiter Output Offset vs Temperature and Supply Voltage
Offset (Volt)
0.14
0.13
0.12
0.11
0.10
0.09
0.08
0.07
0.06
0.05
0.04
5.5V
3.0V
2.7V
−40
0
25
70
85
Temperature (°C)
Limiter Bandwidth vs Temperature
Bandwidth (MHz)
2.8
2.6
2.4
2.2
2.0
1.8
1.6
−40
0
25
70
85
Temperature (°C)
Limiter Gain vs Temperature and Supply Voltage
Gain (dB)
65.0
64.5
64.0
63.5
63.0
62.5
62.0
61.5
61.0
60.5
60.0
5.5V
3.0V
2.7V
−40°C
25
70
85
Temperature (°C)
Limiter Output vs Temperature and Supply Voltage
Output (mVp-p)
450
400
350
300
250
200
5.5V
3.0V
2.7V
−40
0
25
70
85
Temperature (°C)
RSSI vs Temperature
RSSI (Volt)
1.6
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0.0
25°C
85°C
−40°C
−118
−108
−98
−88
−78
−68
−58
−48
−38
−28
RF Input (dBm)
RSSI vs Supply Voltage
RSSI (Volt)
1.80
1.60
1.40
1.20
1.00
0.80
0.60
0.40
0.20
0.00
5.5V
3.0V
2.7V
−118
−108
−98
−88
−78
−68
−58
−48
−38
−28
RF Input (dBm)
SR01555

Figure 4.

GENERAL TEST CIRCUIT DESCRIPTION

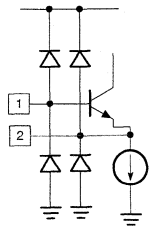
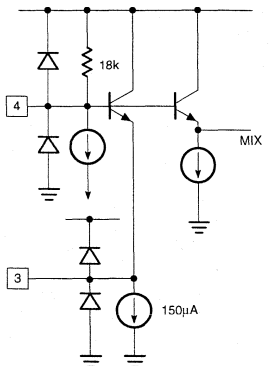
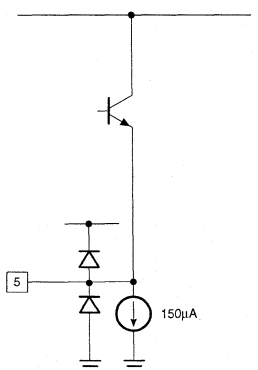


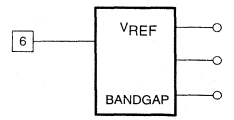
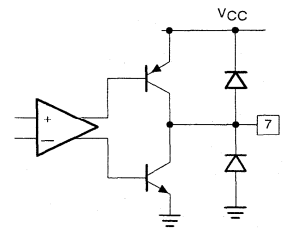
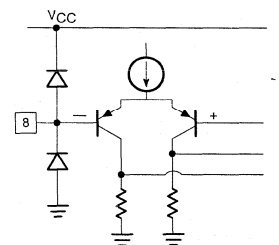
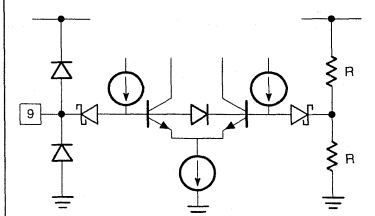
Automatic Test Circuit Component List

C1	0.01µF	C11	100nF	C21	0.01µF	R1	249Ω	R13	50Ω	R24	8.66Ω	L1	120nH
C2	12pF	C12	100nF	C22	0.1µF	R2	60.4Ω	R14	13.7Ω	R25	130Ω	L2	120nH
C3	39pF	C13	30pF	C23	100nF	R3	60.4Ω	R15	1.5KΩ	R26	182Ω	L3	56µH
C4	0.01µF	C14	0.1µF	C24	0.1µF	R4	10KΩ	R16	1.5KΩ	R27	182Ω	FLT	600kHz
C5	15pF	C15	30pF	C25	0.1µF	R5	10KΩ	R17	1KΩ	R28	10KΩ		
C6	39pF	C16	100nF	C26	100nF	R6	10KΩ	R18	13.7KΩ	R29	10KΩ		
C7	3.9pF	C17	100nF	C27	0.1µF	R7	10KΩ	R19	50KΩ	R30	3.92KΩ		
C8	0.1µF	C18	0.1µF	C28	0.1µF	R8	10KΩ	R20	1.69KΩ				
C9	100nF	C19	270pF			R9	10KΩ	R21	2.43KΩ				
C10	100nF	C20	1500pF			R10	1.5KΩ	R22	50Ω				
						R11	1.5KΩ	R23	130Ω				
						R12	1.69KΩ				

SR01476

Figure 5.

PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
1	RF IN	+1.40	
2	RF BYPASS	+1.40	
3	OSC E	+1.79	
4	OSC B	+2.56	
5	OSC BUFFER	+1.79	

PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
6	V_{CC}	+3.00	
7	RSSI OUT	+0.20	
8	RSSI FEEDBACK	+0.20	
9	POWER DOWN	+2.00	

SR00508

Figure 6.

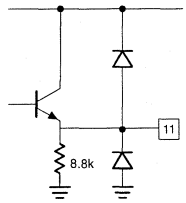
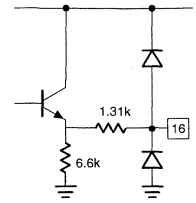
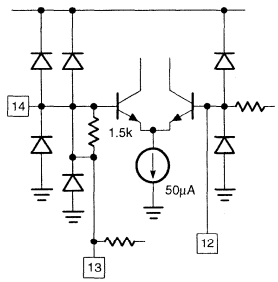
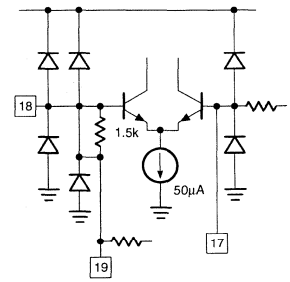
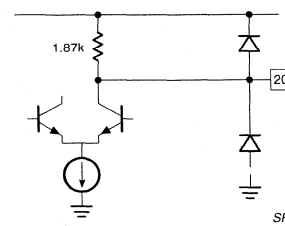
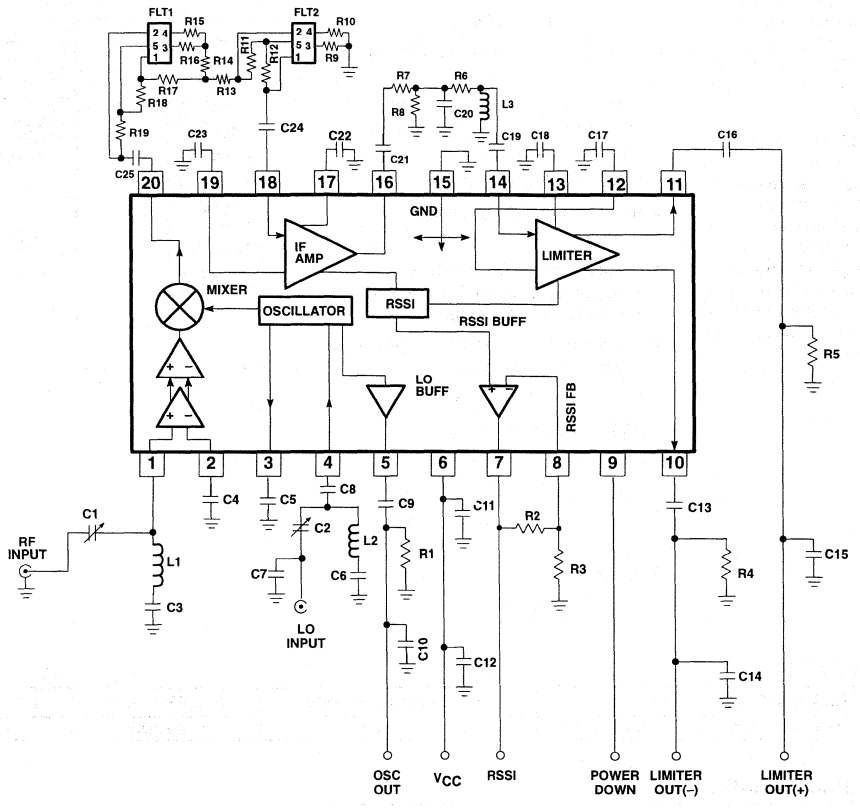
PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT	PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
10 11	LIMITER OUT	+1.25		16	IF AMP OUT	+1.28	
12	LIMITER DECOUP	+1.28		17	IF AMP DECOUP	+1.28	
13	LIMITER COUPLING	+1.28		18	IF AMP IN	+1.28	
14	LIMITER IN	+1.28		19	IF AMP DECOUP	+1.28	
15	GND	0		20	MIXER OUT	+2.03	

Figure 7.

GENERAL APPLICATIONS CIRCUIT



Component List

C1	5–30pF	C11	0.1μF	C21	10nF	R1	10KΩ	R13	240Ω	L1	180nH
C2	5–30pF	C12	6.8pF	C22	0.1μF	R2	0Ω (short)	R14	4.5KΩ	L2	180nH
C3	0.1μF	C13	0.1μF	C23	0.1μF	R3	OPEN	R15	180Ω	L3	56μH
C4	0.1μF	C14	30pF	C24	10nF	R4	5.1k	R16	180Ω	FLT1,2	600kHz
C5	0.1μF	C15	30pF	C25	10nF	R5	5.1k	R17	240Ω		
C6	0.1μF	C16	0.1μF			R6	0Ω (short)	R18	10KΩ		
C7	47pF	C17	0.1μF			R7	1.5KΩ	R19	10KΩ		
C8	1nF	C18	0.1μF			R8	1.5KΩ				
C9	10pF	C19	10nF			R9	180Ω				
C10	3.9pF	C20	1500pF			R10	180Ω				
						R11	10KΩ				
						R12	0KΩ				

NOTE: R2 and R3 set the RSSI buffer gain. For unity gain short R2 (Pin 7 to Pin 8) and leave R9 open.

SR01477

Figure 8.

Low-voltage mixer FM IF system — SA676

DESCRIPTION

The SA676 is a low-voltage monolithic FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, logarithmic received signal strength indicator (RSSI), voltage regulator and audio and RSSI op amps. The SA676 is available in a 20-pin SSOP (shrink small outline package).

The SA676 was designed for cordless telephone applications in which efficient and economic integrated solutions are required and yet high performance is desirable. Although the product is not targeted to meet the stringent specifications of high performance cellular equipment, it will exceed the needs for analog cordless phones. The minimal amount of external components and absence of any external adjustments makes for a very economical solution.

FEATURES

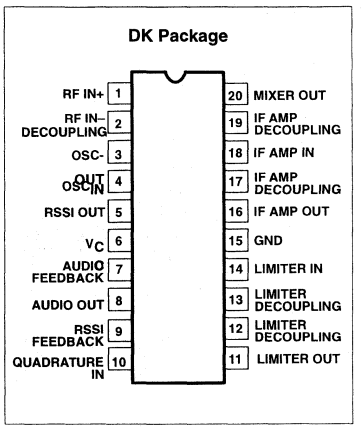
- Low power consumption: 3.5mA typical at 3V
- Mixer input to >100MHz
- Mixer conversion power gain of 17dB at 45MHz
- XTAL oscillator effective to 100MHz (L.C. oscillator or external oscillator can be used at higher frequencies)
- 102dB of IF Amp/Limiter gain
- 2MHz IF amp/limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a 70dB dynamic range
- Low external component count; suitable for crystal/ceramic/LC filters
- Audio output internal op amp
- RSSI output internal op amp
- Internal op amps with rail-to-rail outputs
- ESD protection: Human Body Model 2kV
  Robot Model 200V

APPLICATION

- Cordless phones

PIN CONFIGURATION

DK Package



ORDERING INFORMATION

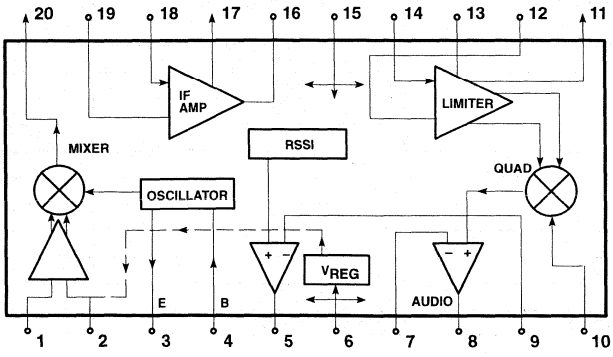
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Shrink Small Outline Package (Surface-mount)	-40 to +85°C	SA676DK	1563–

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	7	V
T_{STG}	Storage temperature range	–65 to +150	°C
T_A	Operating ambient temperature range	–40 to +85	°C
θ_{JA}	Thermal impedance DK package	117	°C/W

Low-voltage mixer FM IF system | SA676

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA676			
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		2.7		7.0	V
I_{CC}	DC current drain			3.5	5.0	mA

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +3V, unless otherwise stated. RF frequency = 45MHz; +14.5dBV RF input step-up; IF frequency = 455kHz; R17 = 2.4kΩ and R18 = 3.3kΩ; RF level = –45dBm; FM modulation = 1kHz with ±5kHz peak deviation. Audio output with de-emphasis filter and C-message weighted filter. Test circuit Figure NO TAG. The parameters listed below are tested using automatic test equipment to assure consistent electrical characteristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Mixer/Osc section (ext LO = 220mV$_{RMS}$)						
f_{IN}	Input signal frequency			100		MHz
f_{OSC}	Crystal oscillator frequency			100		MHz
	Noise figure at 45MHz			7.0		dB
	Third–order input intercept point (50Ω source)	f1 = 45.0; f2 = 45.06MHz Input RF level = –52dBm		–10		dBm
	Conversion power gain	Matched 14.5dBV step–up	10	17		dB
		50Ω source		+2.5		dB
	RF input resistance	Single–ended input		8		kΩ
	RF input capacitance			3.0	4.0	pF
	Mixer output resistance	(Pin 20)	1.25	1.5		kΩ
IF section						
	IF amp gain	50Ω source		44		dB
	Limiter gain	50Ω source		58		dB
	AM rejection	30% AM 1kHz		50		dB
	Audio level	Gain of two	60	120		mV
	SINAD sensitivity	IF level –110dBm		17		dB
THD	Total harmonic distortion			–55		dB

AC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
S/N	Signal–to–noise ratio	No modulation for noise		60		dB
	IF RSSI output, R_9 = 2kΩ[1]	IF level = –110dBm		0.5	.90	V
		IF level = –50dBm		1.7	2.2	V
	RSSI range			70		dB
	IF input impedance	Pin 18	1.3	1.5		kΩ
	IF output impedance	Pin 16		0.3		kΩ
	Limiter input impedance	Pin 14	1.3	1.5		kΩ
	Limiter output impedance	Pin 11		0.3		kΩ
	Limiter output voltage	Pin 11		130		mV_{RMS}
RF/IF section (int LO)						
	System SINAD sensitivity	RF level = –114dBm		12		dB

NOTE:
1. The generator source impedance is 50Ω, but the SA676 input impedance at Pin 18 is 1500Ω. As a result, IF level refers to the actual signal that enters the SA676 input (Pin 18) which is about 21dB less than the "available power" at the generator.

CIRCUIT DESCRIPTION

The SA676 is an IF signal processing system suitable for second IF systems with input frequency as high as 100MHz. The bandwidth of the IF amplifier and limiter is at least 2MHz with 90dB of gain. The gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 7.0dB, conversion gain of 17dB, and input third-order intercept of –10dBm. The oscillator will operate in excess of 100MHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations.

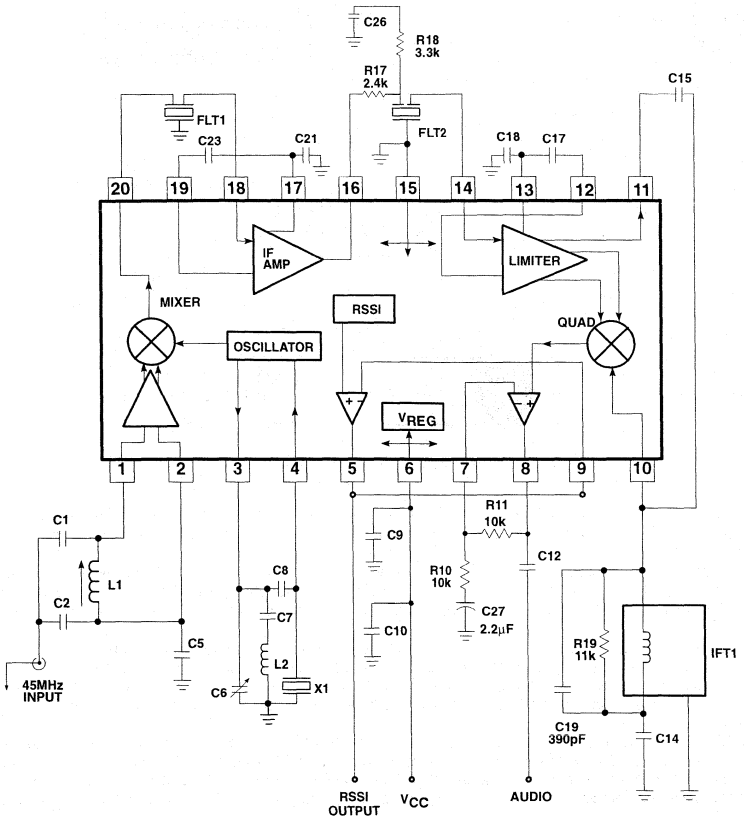
The output impedance of the mixer is a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. The IF amplifier has 44dB of gain and 5.5MHz bandwidth. The IF limiter has 58dB of gain and 4.5MHz bandwidth. To achieve optimum linearity of the log signal strength indicator, there must be a 12dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dB(v) insertion loss, a fixed or variable resistor or an L pad for simultaneous loss and impedance matching can be added between the first IF output (Pin 16) and the interstage network. The overall gain will then be 90dB with 2MHz bandwidth.

The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

The demodulated output of the quadrature drives an internal op amp. This op amp can be configured as a unity gain buffer, or for simultaneous gain, filtering, and 2nd-order temperature compensation if needed. It can drive an AC load as low as 10kΩ with a rail-to-rail output.

A log signal strength indicator completes the circuitry. The output range is greater than 70dB and is temperature compensated. This signal drives an internal op amp. The op amp is capable of rail-to-rail output. It can be used for gain, filtering, or 2nd-order temperature compensation of the RSSI, if needed.

NOTE: $dB(v) = 20\log V_{OUT}/V_{IN}$



SA676DK Demoboard
Application Component List

C1	51pF NPO Ceramic
C2	220pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	5-30pF trim cap
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	10µF Tantalum (minimum) *
C12	2.2µF ±10% Tantalum
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C19	390pF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C26	100nF ±10% Monolithic Ceramic
C27	2.2µF Tantalum
FLT 1	Ceramic Filter Murata SFG455A3 or equiv
FLT 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	330µH TOKO 303LN-1130
L1	330nH Coilcraft UNI-10/142-04J08S
L2	0.8µH nominal TOKO 292CNS-T1038Z
X1	44.545MHz Crystal ICM4712701
R5	Not Used in Application Board (see Note 8, pg 8)
R10	8.2k ±5% 1/4W Carbon Composition
R11	10k ±5% 1/4W Carbon Composition
R17	2.4k ±5% 1/4W Carbon Composition
R18	3.3k ±5% 1/4W Carbon Composition
R19	11k ±5% 1/4W Carbon Composition

* NOTE: This value can be reduced when a battery is the power source.

Figure 1. SA676 45MHz Application Circuit

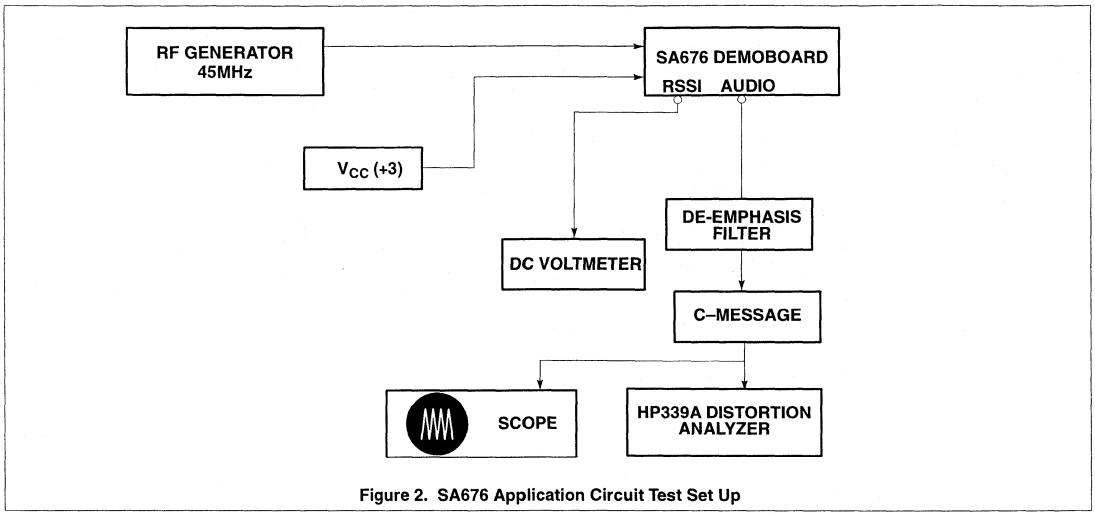


Figure 2. SA676 Application Circuit Test Set Up

NOTES:

1. C-message: The C-message and de-emphasis filter combination has a peak gain of 10 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339A analyzer. The de-emphasis filter has a fixed -6dB/Octave slope between 300Hz and 3kHz.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All specifications and testing are done with the wideband filter.
3. RF generator: Set your RF generator at 45.000MHz, use a 1kHz modulation frequency and a 6kHz deviation if you use 16kHz filters, or 8kHz if you use 30kHz filters.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.45μV or –114dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 500mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10-15μF or higher value tantalum capacitor on the supply line is essential. A low frequency ESR screening test on this capacitor will ensure consistent good sensitivity in production. A 0.1μF bypass capacitor on the supply pin, and grounded near the 44.545MHz oscillator improves sensitivity by 2-3dB.
8. R5 can be used to bias the oscillator transistor at a higher current for operation above 45MHz. Recommended value is 22kΩ, but should not be below 10kΩ.

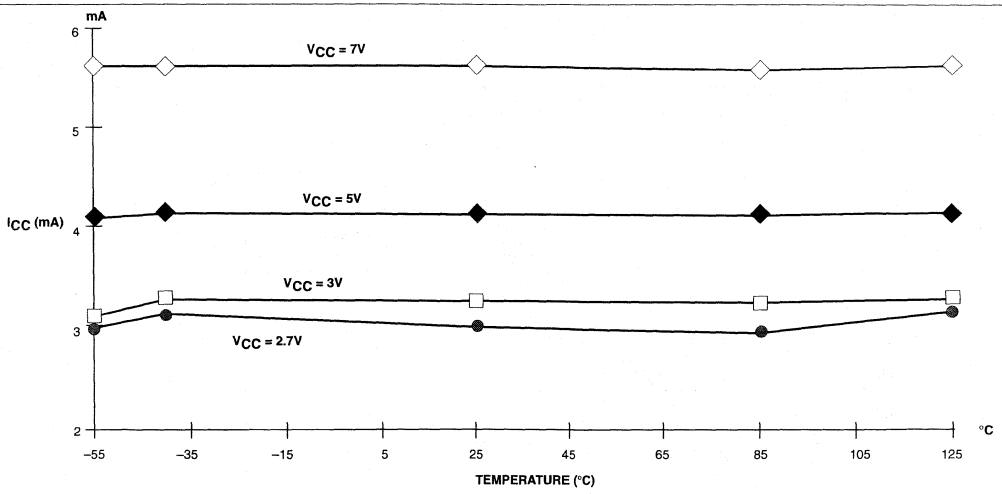


Figure 3. I_{CC} vs Temperature and Supply Voltage

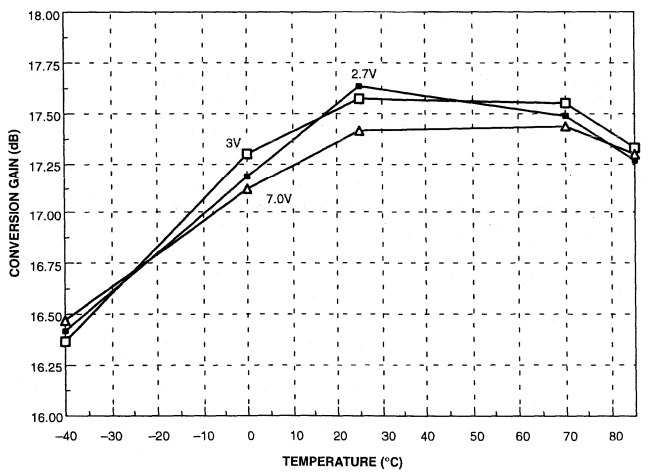


Figure 4. Conversion Gain vs Temperature and Supply Voltage

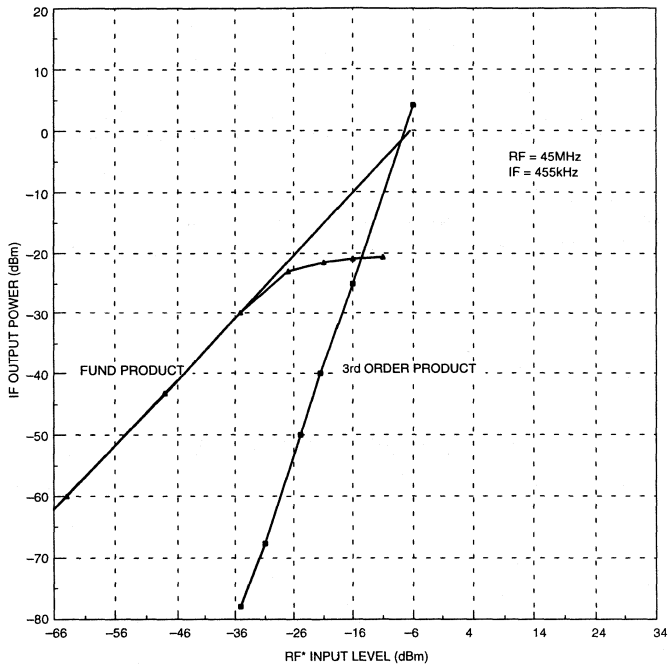


Figure 5. Mixer Third Order Intercept and Compression

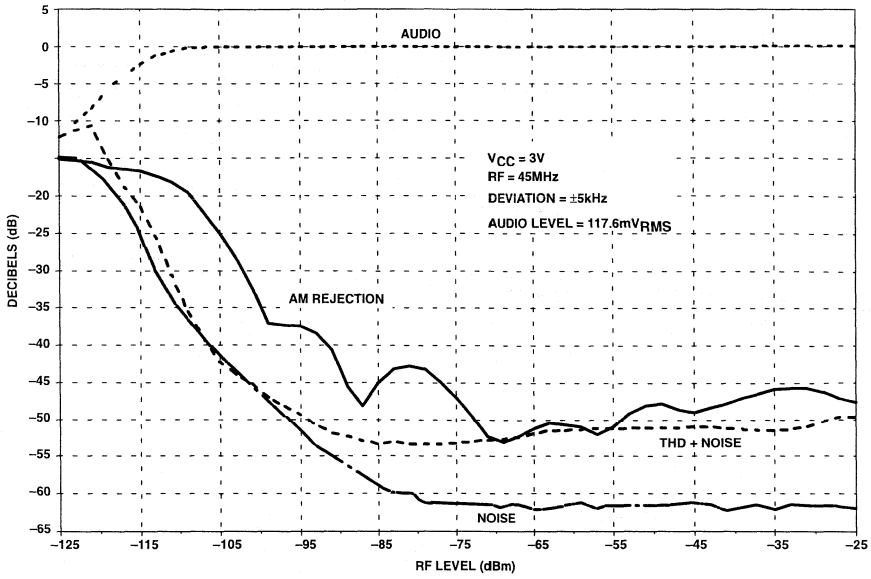


Figure 6. Sensitivity vs RF Level (+25°C)

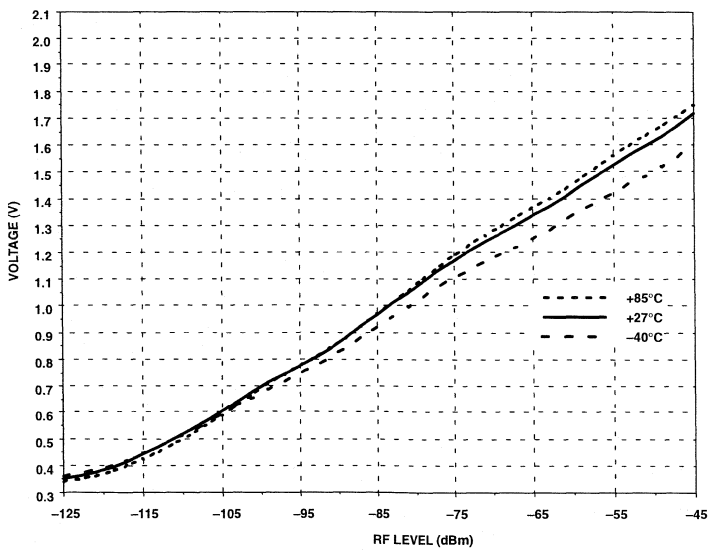


Figure 7. RSSI vs RF Level and Temperature - V_{CC} = 3V

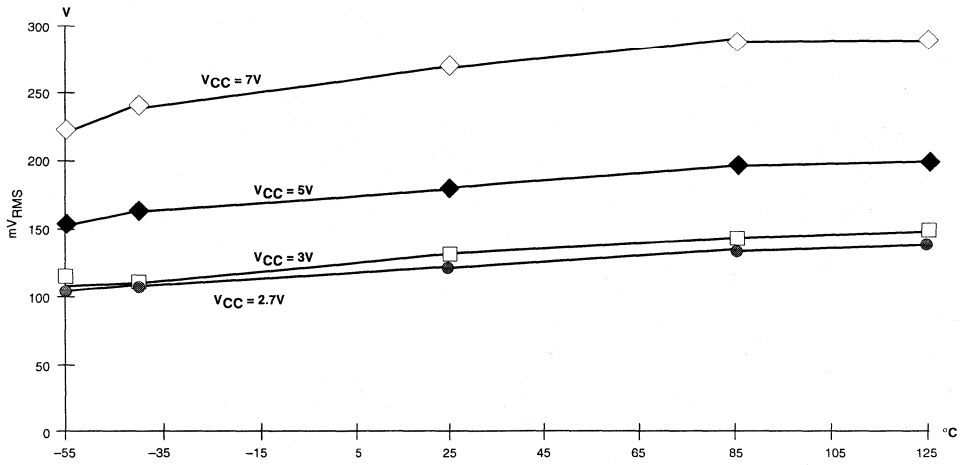


Figure 8. Audio Output vs Temperature and Supply Voltage

Divide by: 128/129-64/65 dual modulus low power ECL prescaler

SA701

DESCRIPTION

The SA701 is an advanced dual modulus (Divide By 128/129 or 64/65) low power ECL prescaler. The minimum supply voltage is 2.7V and is compatible with the CMOS UMA1005 synthesizer from Philips and other logic circuits. The low supply current allows application in battery operated low-power equipment. Maximum input signal frequency is 1.1GHz for cellular and other land mobile applications. There is no lower frequency limit due to a fully static design. The circuit is implemented in ECL technology on the QUBiC process. The circuit will be available in an 8-pin SO package with 150 mil package width and in 8-pin dual in-line plastic package, and is pin compatible with Fujitsu MB501, Plessey SP8704 and Motorola MC12022.

FEATURES

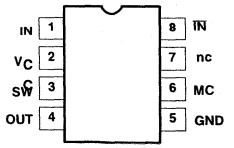
- Low voltage operation
- Low current consumption
- Operation up to 1.1GHz
- ESD hardened

APPLICATIONS

- Cellular phones
- Cordless phones
- RF LANs
- Test and measurement
- Military radio
- VHF/UHF mobile radio
- VHF/UHF hand-held radio

PIN CONFIGURATION

N, D Package



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA701N	0404B
8-Pin Plastic Small Outline (SO) package (Surface-mount)	-40 to +85°C	SA701D	0174C

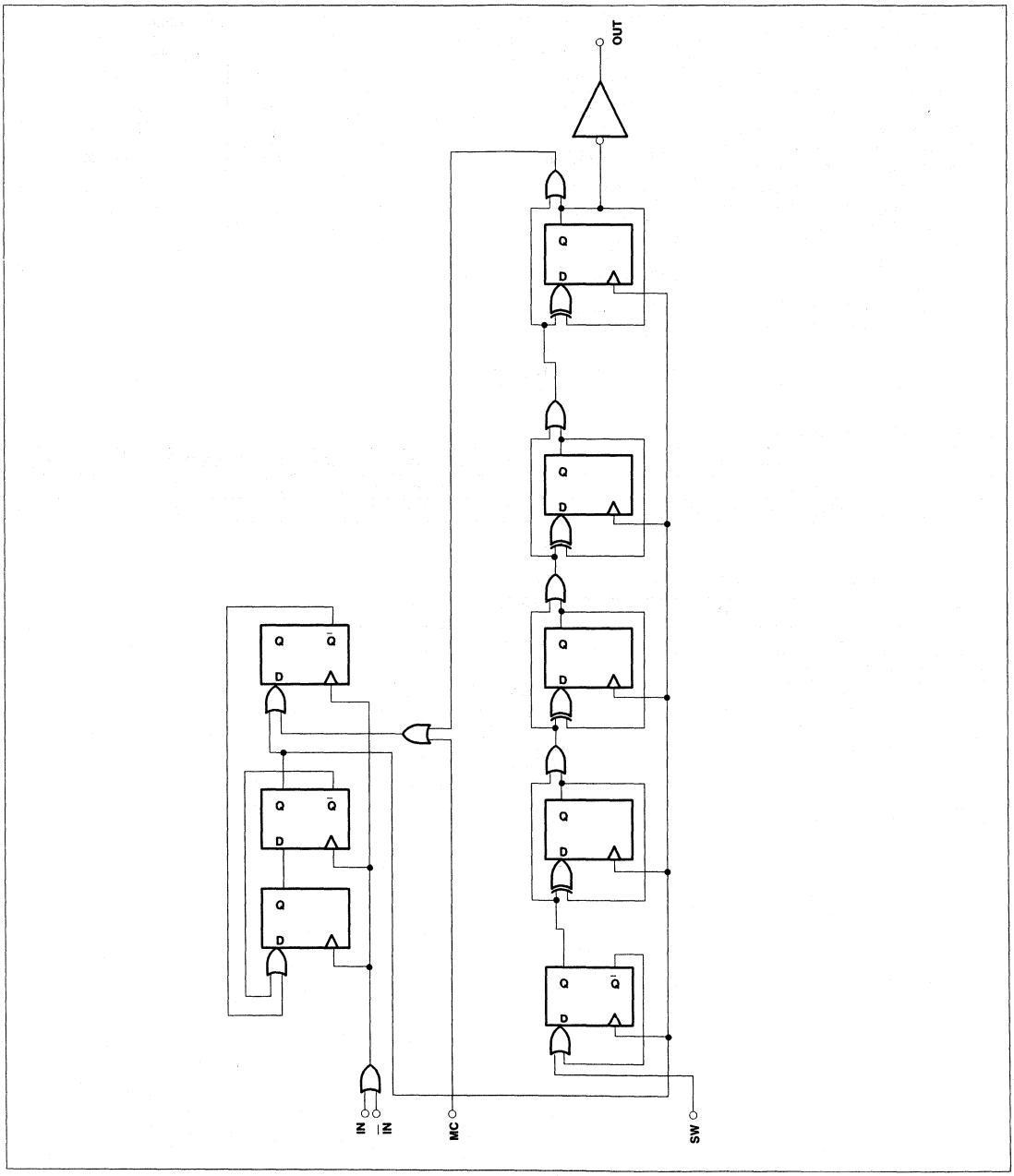
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	-0.3 to +7.0	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{CC} + 0.3)	V
I_O	Output current	10	mA
T_{STG}	Storage temperature range	-65 to +125	°C
T_A	Operating ambient temperature range	-55 to +125	°C
θ_{JA}	Thermal impedance D package N package	158 108	°C/W

Divide by: 128/129-64/65 dual modulus low power ECL prescaler

SA701

BLOCK DIAGRAM



Divide by: 128/129-64/65 dual modulus low power ECL prescaler

SA701

DC ELECTRICAL CHARACTERISTICS

The following DC specifications are valid for $T_A = 25°C$ and $V_{CC} = 3.0V$; unless otherwise stated. Test circuit Figure 1.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range	f_{IN} = 1GHz, input level = 0dBm	2.7		6.0	V
I_{CC}	Supply current	No load		4.5		mA
V_{OH}	Output high level	I_{OUT} = 1.2mA	V_{CC}-1.4			V
V_{OL}	Output low level			V_{CC}-2.6		V
V_{IH}	MC input high threshold		2.0		V_{CC}	V
V_{IL}	MC input low threshold		–0.3		0.8	V
V_{IH}	SW input high threshold		2.0		V_{CC}	V
V_{IL}	SW input low threshold		–0.3		0.8	V
I_{IH}	MC input high current	$V_{MC} = V_{CC} = 6V$		0.1	50	µA
I_{IL}	MC input low current	$V_{MC} = 0V$, $V_{CC} = 6V$	–100	–30		µA
I_{IH}	SW input high current	$V_{SW} = V_{CC} = 6V$		35	100	µA
I_{IL}	SW input low current	$V_{SW} = 0V$, $V_{CC} = 6V$	–50	–0.1		µA

AC ELECTRICAL CHARACTERISTICS

The following AC specifications are valid for $V_{CC} = 3.0V$, f_{IN} = 1GHz, input level = 0dBm, $T_A = 25°C$; unless otherwise stated. Test circuit Fig. 1.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{IN}	Input signal amplitude[1]	1000pF input coupling	0.05		2.0	V_{P-P}
f_{IN}	Input signal frequency	Direct coupled input[2]	0		1.1	GHz
		1000pF input coupling			1.1	GHz
R_{ID}	Differential input resistance	DC measurement		5		kΩ
V_O	Output voltage	$V_{CC} = 5.0V$		1.6		V_{P-P}
		$V_{CC} = 3.0V$		1.2		V_{P-P}
t_S	Modulus set-up time[1]				5	ns
t_H	Modulus hold time[1]				0	ns
t_{PD}	Propagation time			10		ns

NOTES:
1. Maximum limit is not tested, however, it is guaranteed by design and characterization.
2. For f_{IN} < 50MHz, minimum input slew rate of 32V/µs is required.

DESCRIPTION OF OPERATION

The SA701 comprises a frequency divider circuit implemented using a divide by 4 or 5 synchronous prescaler followed by a 5 stage synchronous counter, see BLOCK DIAGRAM. The normal operating mode is for SW (Modulus Set Switch) input to be set low and MC (Modulus Control) input to be set high in which case the circuit comprises a divide by 128. For divide by 129 the MC signal is forced low, causing the prescaler circuit to switch into divide by 5 operation for the last cycle of the synchronous counter. Similarly, for divide by 64 and 65 the SA701 will generate those respective moduli with the SW signal forced high, in which the fourth stage of the synchronous divider is bypassed. A truth table for the modulus values is given below:

Table 1.

Modulus	MC	SW
128	1	0
129	0	0
64	1	1
65	0	1

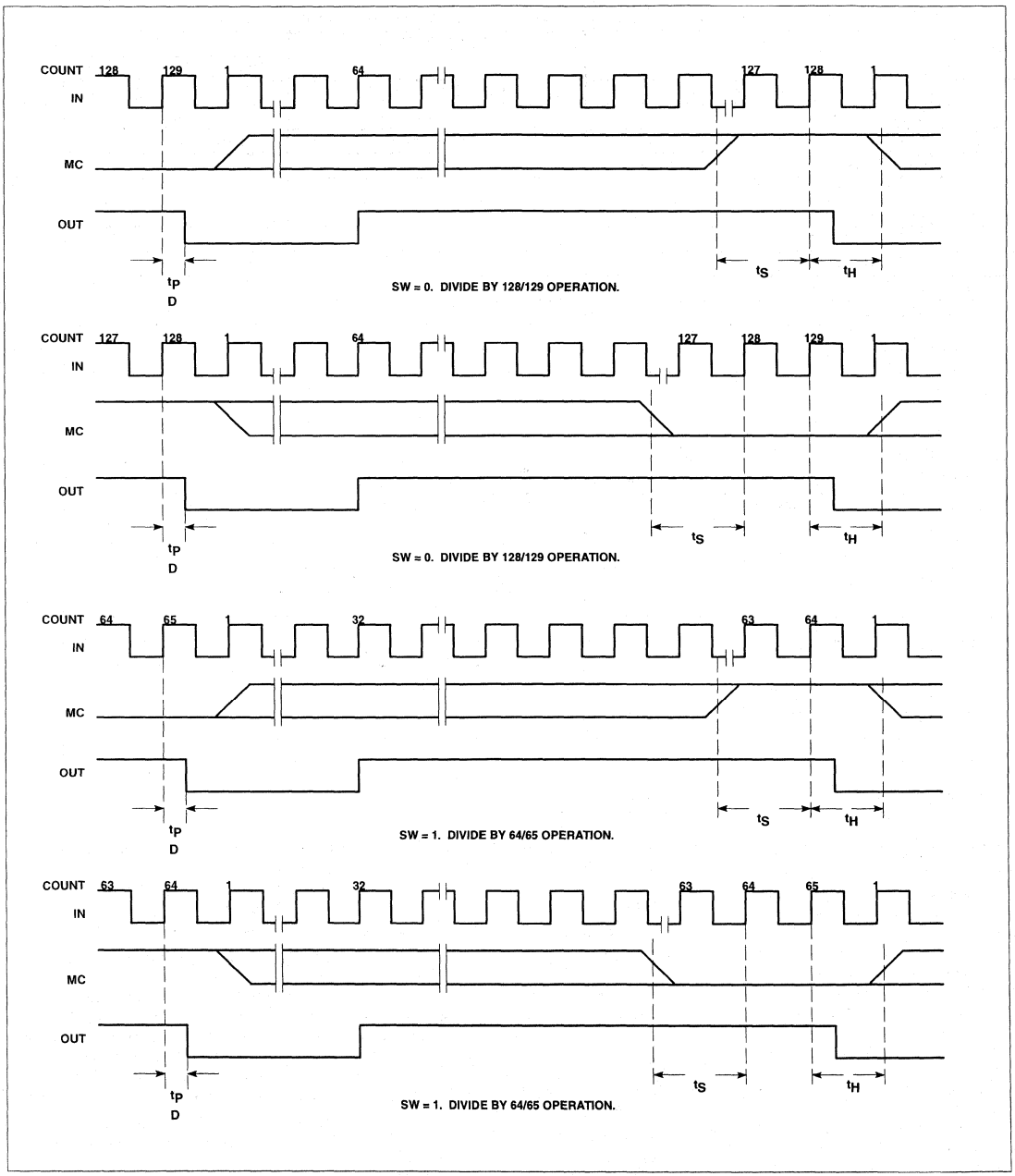
For minimization of propagation delay effects, the second divider circuit is synchronous to the divide by 4/5 stage output.

The prescaler input is positive edge sensitive, and the output at the final count is a falling edge with propagation delay t_{PD} relative to the input. The rising edge of the output occurs at the count 64 for modulus 128/129 or count 32 for modulus 64/65 with delay t_{PD}. The SW input is not designed for synchronous switching.

The MC and SW inputs are TTL compatible threshold inputs operating at a reduced input current. CMOS and low voltage interface capability are allowed. The SW input has an internal pull-down simplifying modulus group selection. With SW open the divide by 128/129 mode is selected and with SW connected to V_{CC} divide by 64/65 is selected.

The prescaler input is differential and ECL compatible. The output is single-ended ECL compatible.

AC TIMING CHARACTERISTICS



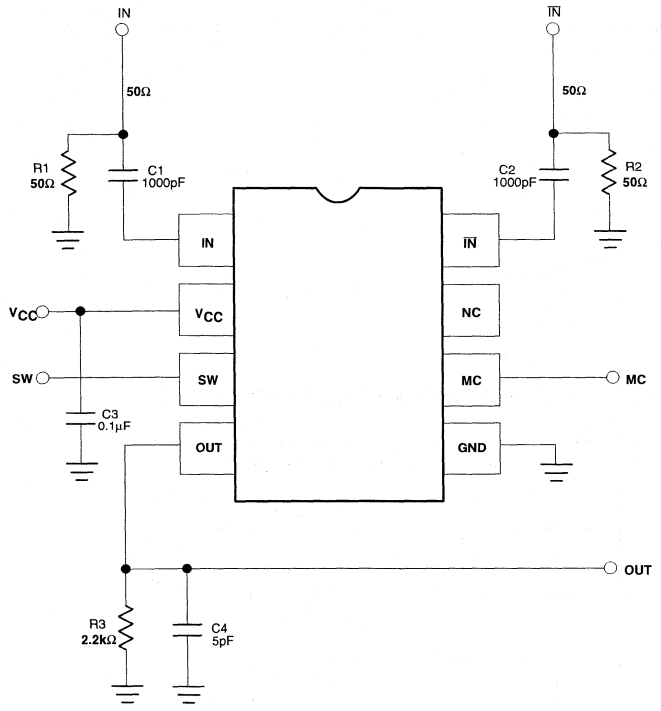


Figure 1. SA701 Test Circuit

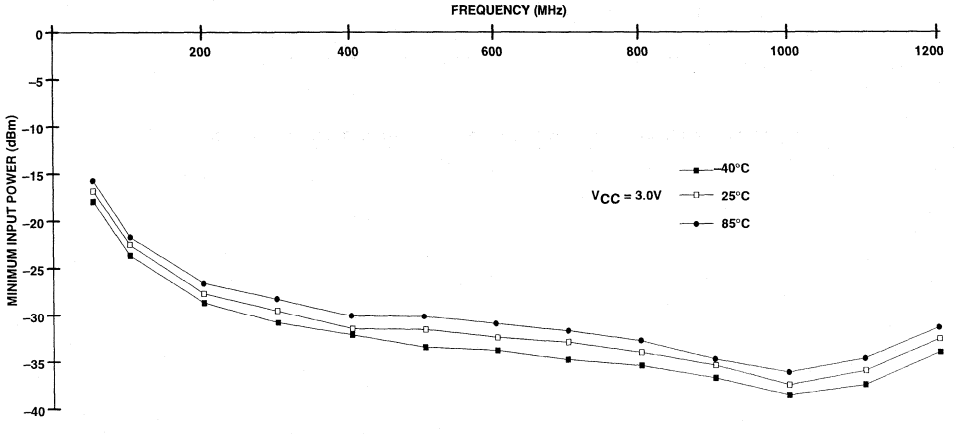


Figure 2. Minimum Input Power vs Frequency and Temperature

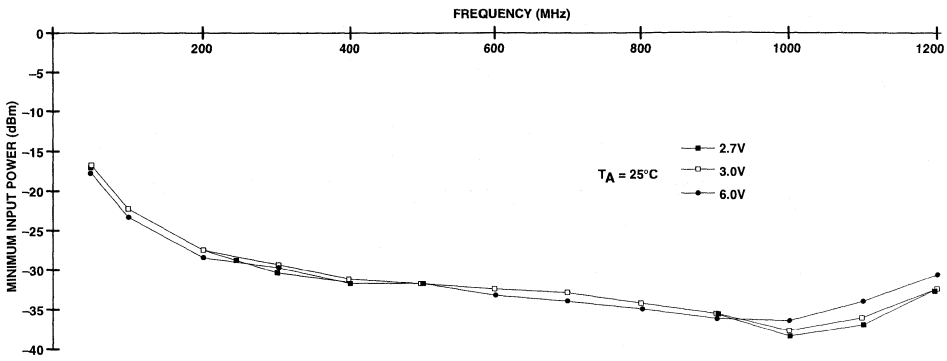


Figure 3. Minimum Input Power vs Frequency and V_{CC}

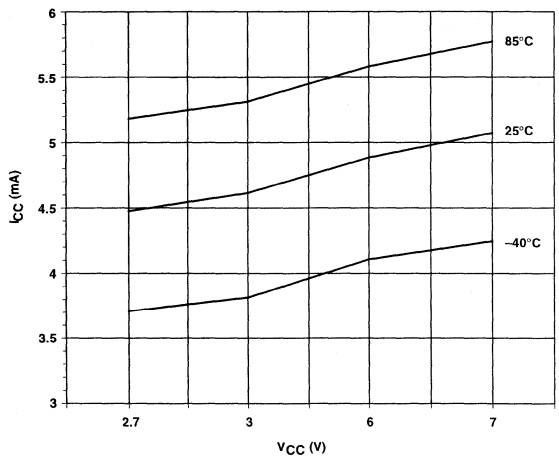


Figure 4. Supply Current vs Supply Voltage and Temperature With No Load

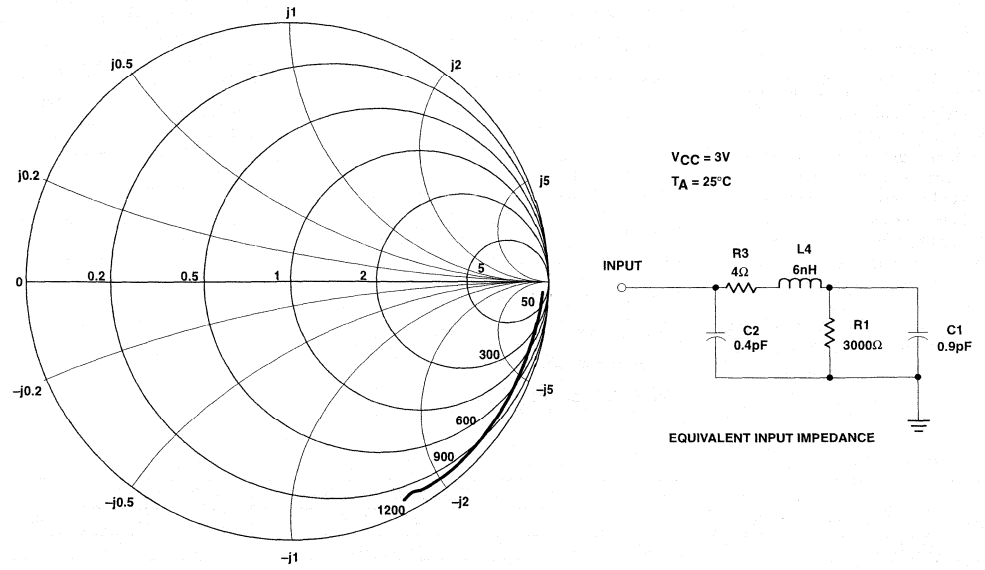


Figure 5. Typical N Package Input Impedance

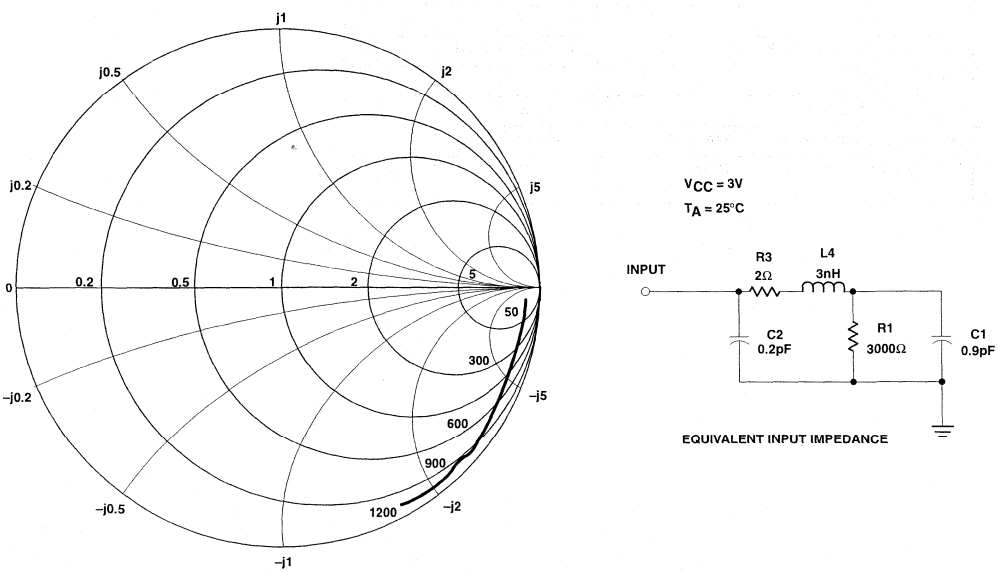


Figure 6. Typical D Package Input Impedance

Divide by: 64/65/72 triple modulus low power ECL prescaler

SA702

DESCRIPTION

The SA702 triple modulus (Divide By 64/65/72) low power ECL prescaler is used in synthesizer systems to achieve low phase lock time, broad operating range, high reference frequency and small frequency step sizes. The minimum supply voltage is 2.7V and is compatible with the CMOS UMA1005 synthesizer from Philips and other logic circuits. The low supply current allows application in battery operated low-power equipment. Maximum input signal frequency is 1.1GHz for cellular and other land mobile applications. There is no lower frequency limit due to a fully static design. The circuit is implemented in ECL technology on the QUBiC process. The circuit will be available in an 8-pin SO package with 150 mil package width and in 8-pin dual in-line plastic package.

FEATURES

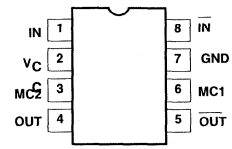
- Low voltage operation
- Low current consumption
- Operation up to 1.1GHz
- ESD hardened

APPLICATIONS

- Cellular phones
- Cordless phones
- RF LANs
- Test and measurement
- Military radio
- VHF/UHF mobile radio
- VHF/UHF hand-held radio

PIN CONFIGURATION

N, D Package



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA702N	0404B
8-Pin Plastic Small Outline (SO) package (Surface-mount)	-40 to +85°C	SA702D	0174C

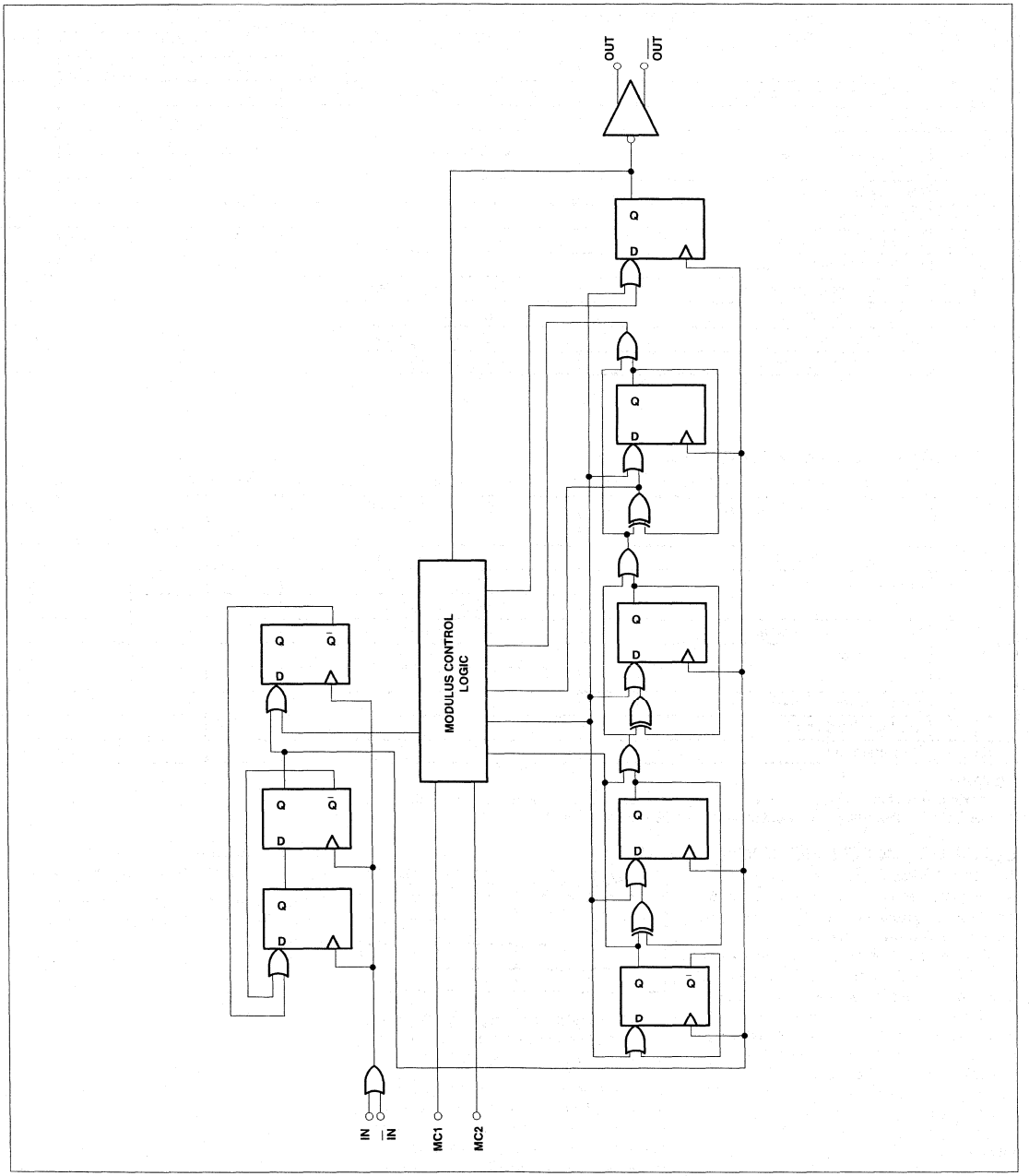
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	-0.3 to +7.0	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{CC} + 0.3)	V
I_O	Output current	10	mA
T_{STG}	Storage temperature range	-65 to +125	°C
T_A	Operating ambient temperature range	-55 to +125	°C
θ_{JA}	Thermal impedance D package N package	158 108	°C/W

Divide by: 64/65/72 triple modulus low power ECL prescaler

SA702

BLOCK DIAGRAM



Divide by: 64/65/72 triple modulus low power ECL prescaler

SA702

DC ELECTRICAL CHARACTERISTICS

The following DC specifications are valid for $T_A = 25°C$ and $V_{CC} = 3.0V$; unless otherwise stated. Test circuit Figure 1.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range	f_{IN} = 1GHz, input level = 0dBm	2.7		6.0	V
I_{CC}	Supply current	No load		4.5		mA
V_{OH}	Output high level	I_{OUT} = 1.2mA	V_{CC}-1.4			V
V_{OL}	Output low level			V_{CC}-2.6		V
V_{IH}	MC1 input high threshold		2.0		V_{CC}	V
V_{IL}	MC1 input low threshold		–0.3		0.8	V
V_{IH}	MC2 input high threshold		2.0		V_{CC}	V
V_{IL}	MC2 input low threshold		–0.3		0.8	V
I_{IH}	MC1 input high current	$V_{MC1} = V_{CC} = 6V$		0.1	50	µA
I_{IL}	MC1 input low current	$V_{MC1} = 0V$, $V_{CC} = 6V$	–100	–30		µA
I_{IH}	MC2 input high current	$V_{MC2} = V_{CC} = 6V$		0.1	50	µA
I_{IL}	MC2 input low current	$V_{MC2} = 0V$, $V_{CC} = 6V$	–100	–30		µA

AC ELECTRICAL CHARACTERISTICS

These AC specifications are valid for f_{IN} = 1GHz, input level = 0dBm, $V_{CC} = 3.0V$ and $T_A = 25°C$; unless otherwise stated. Test circuit Fig. 1.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{IN}	Input signal amplitude[1]	1000pF input coupling	0.05		2.0	V_{P-P}
f_{IN}	Input signal frequency	Direct coupled input[2]	0		1.1	GHz
		1000pF input coupling			1.1	GHz
R_{ID}	Differential input resistance	DC measurement		5		kΩ
V_O	Output voltage	$V_{CC} = 5.0V$		1.6		V_{P-P}
		$V_{CC} = 3.0V$		1.2		V_{P-P}
t_S	Modulus set-up time[1]				5	ns
t_H	Modulus hold time[1]				0	ns
t_{PD}	Propagation time			10		ns

NOTES:
1. Maximum limit is not tested, however, it is guaranteed by design and characterization.
2. For f_{IN} < 50MHz, minimum input slew rate of 32V/µs is required.

DESCRIPTION OF OPERATION

The SA702 comprises a frequency divider circuit implemented using a divide by 4 or 5 synchronous prescaler followed by a 5 stage synchronous counter, see BLOCK DIAGRAM. The normal operating mode is for MC1 (Modulus Control) to be set high and MC2 input to be set low in which case the circuit comprises a divide by 64. For divide by 65 the MC1 singal is forced low, causing the prescaler circuit to switch into divide by 5 operation for the last cycle of the synchronous counter. For divide by 72, MC2 is set high configuring the prescaler to divide by 4 and the counter to divide by 18. A truth table for the modulus values is given below:

Table 1.

Modulus	MC1	MC2
64	1	0
65	0	0
72	0	1
72	1	1

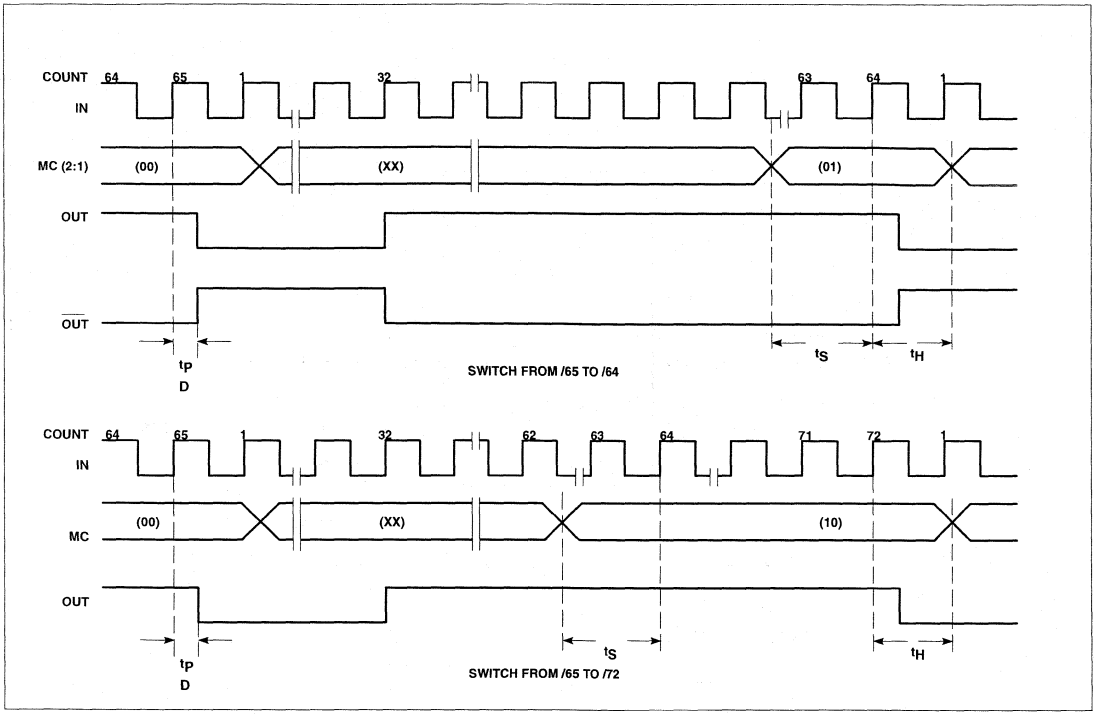
For minimization of propagation delay effects, the second divider circuit is synchronous to the divide by 4/5 stage output.

The prescaler input is positive edge sensitive, and the output at the final count is a falling edge with propagation delay t_{PD} relative to the input. The rising edge of the output occurs at the count 32 with delay t_{PD}.

The MC1 and MC2 inputs are TTL compatible threshold inputs operating at a reduced input current. CMOS and low voltage interface capability are allowed.

The prescaler input is differential and ECL compatible. The output is differential ECL compatible.

AC TIMING CHARACTERISTICS



Divide by: 64/65/72 triple modulus low power ECL prescaler

SA702

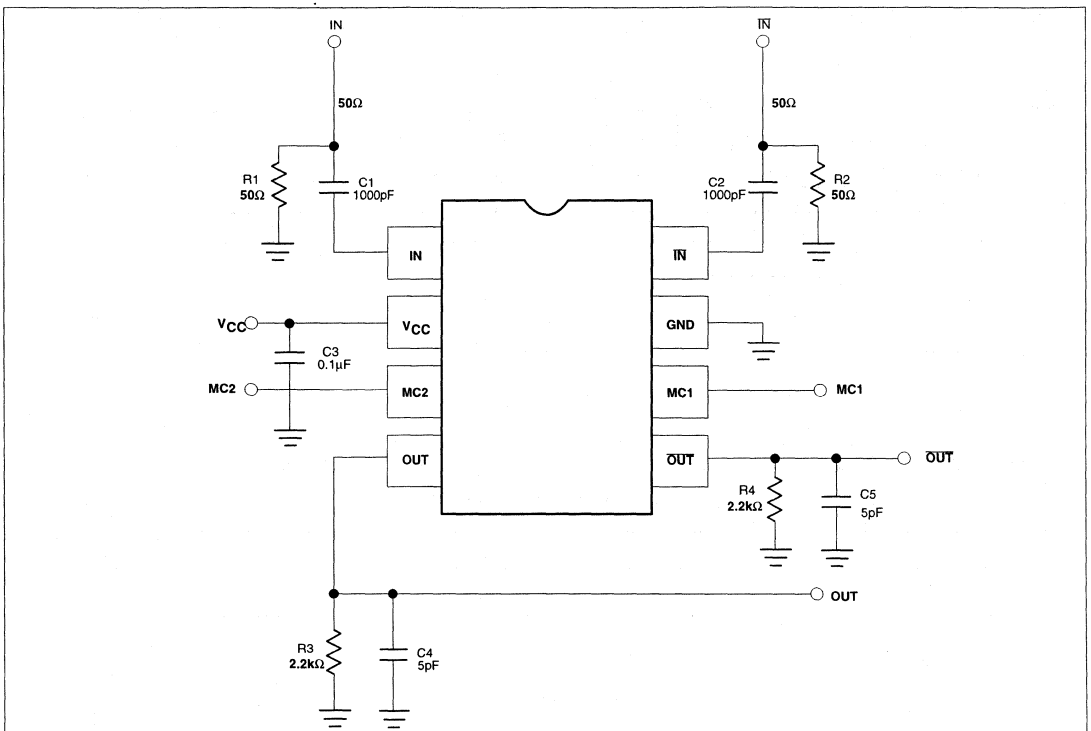


Figure 1. SA702 Test Circuit

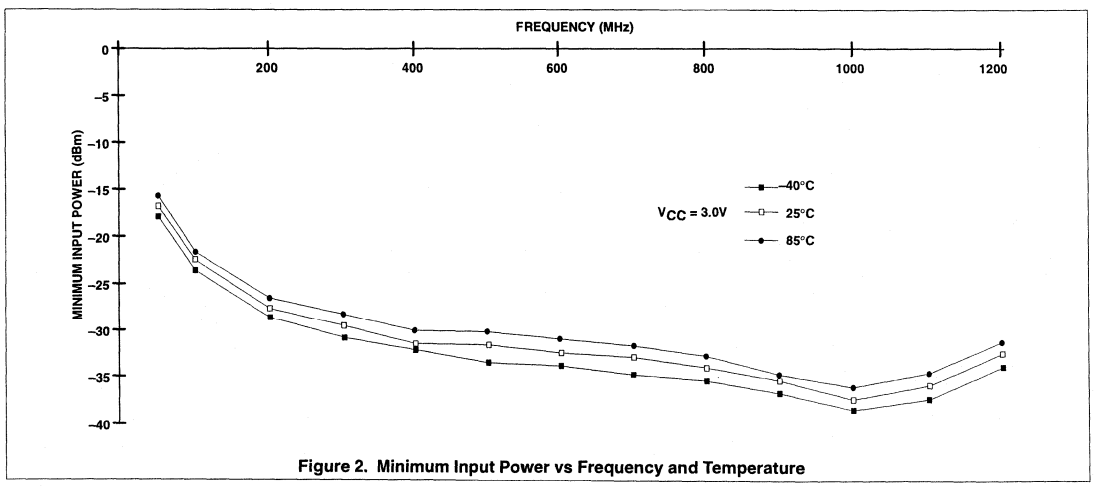


Figure 2. Minimum Input Power vs Frequency and Temperature

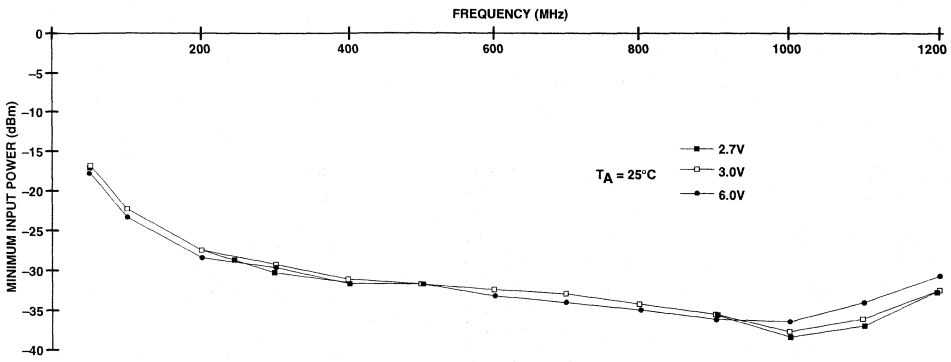


Figure 3. Minimum Input Power vs Frequency and V_{CC}

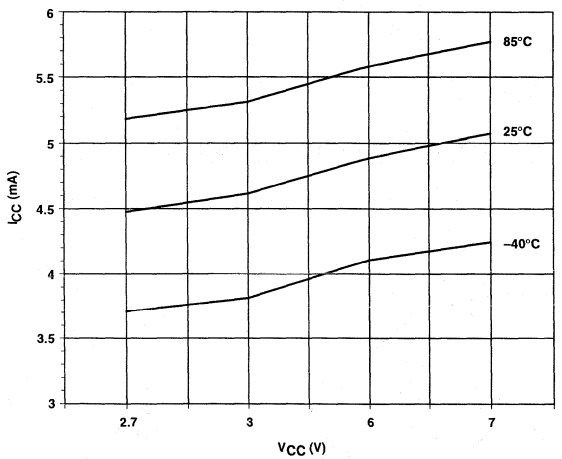
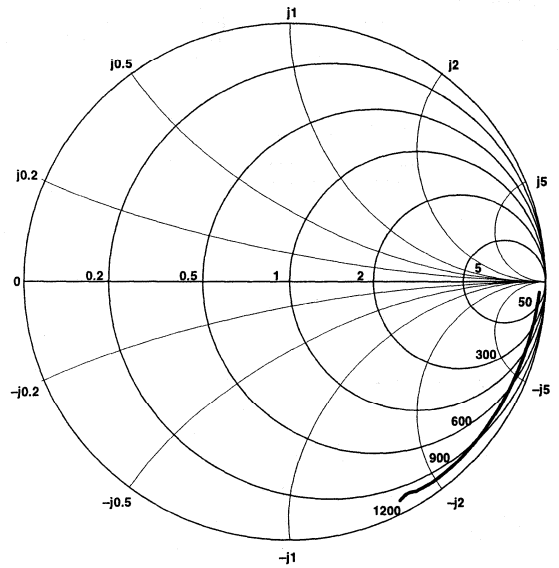


Figure 4. Supply Current vs Supply Voltage and Temperature With No Load



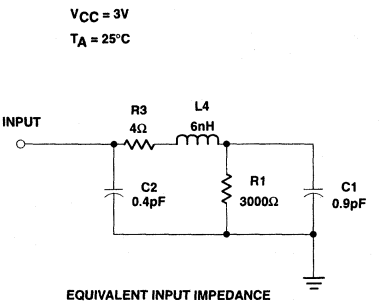
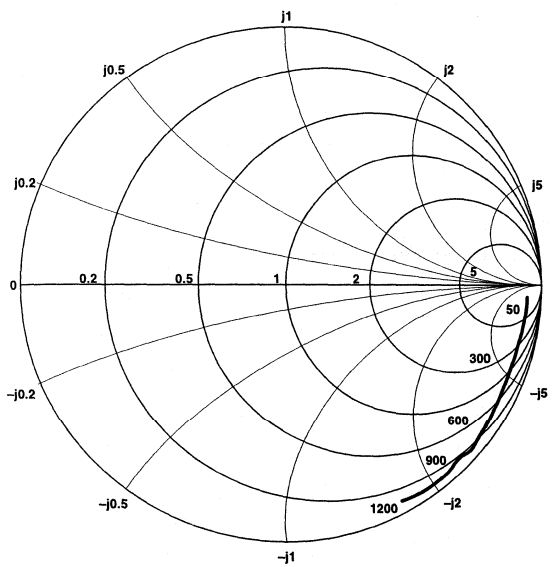


Figure 5. Typical N Package Input Impedance



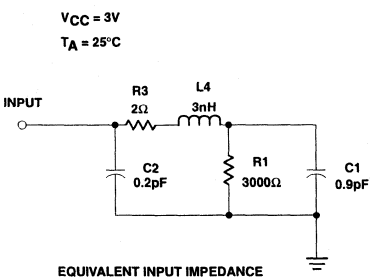


Figure 6. Typical D Package Input Impedance

Divide by: 128/129/144 triple modulus low power ECL prescaler

SA703

DESCRIPTION

The SA703 triple modulus (Divide By 128/129/144) low power ECL prescaler is used in synthesizer systems to achieve low phase lock time, broad operating range, high reference frequency and small frequency step sizes. The minimum supply voltage is 2.7V and is compatible with the UMA1005 synthesizer from Philips and other logic circuits. The low supply current allows application in battery operated low-power equipment. Maximum input signal frequency is 1.1GHz for cellular and other land mobile applications. There is no lower frequency limit due to a fully static design. The circuit is implemented in ECL technology on the QUBiC process. The circuit will be available in an 8-pin SO package with 150 mil package width and in 8-pin dual in-line plastic package.

FEATURES

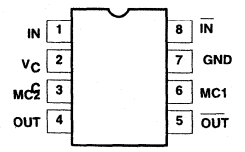
- Low voltage operation
- Low current consumption
- Operation up to 1.1GHz
- ESD hardened

APPLICATIONS

- Cellular phones
- Cordless phones
- RF LANs
- Test and measurement
- Military radio
- VHF/UHF mobile radio
- VHF/UHF hand-held radio

PIN CONFIGURATION

N, D Package



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA703N	0404B
8-Pin Plastic Small Outline (SO) package (Surface-mount)	-40 to +85°C	SA703D	0174C

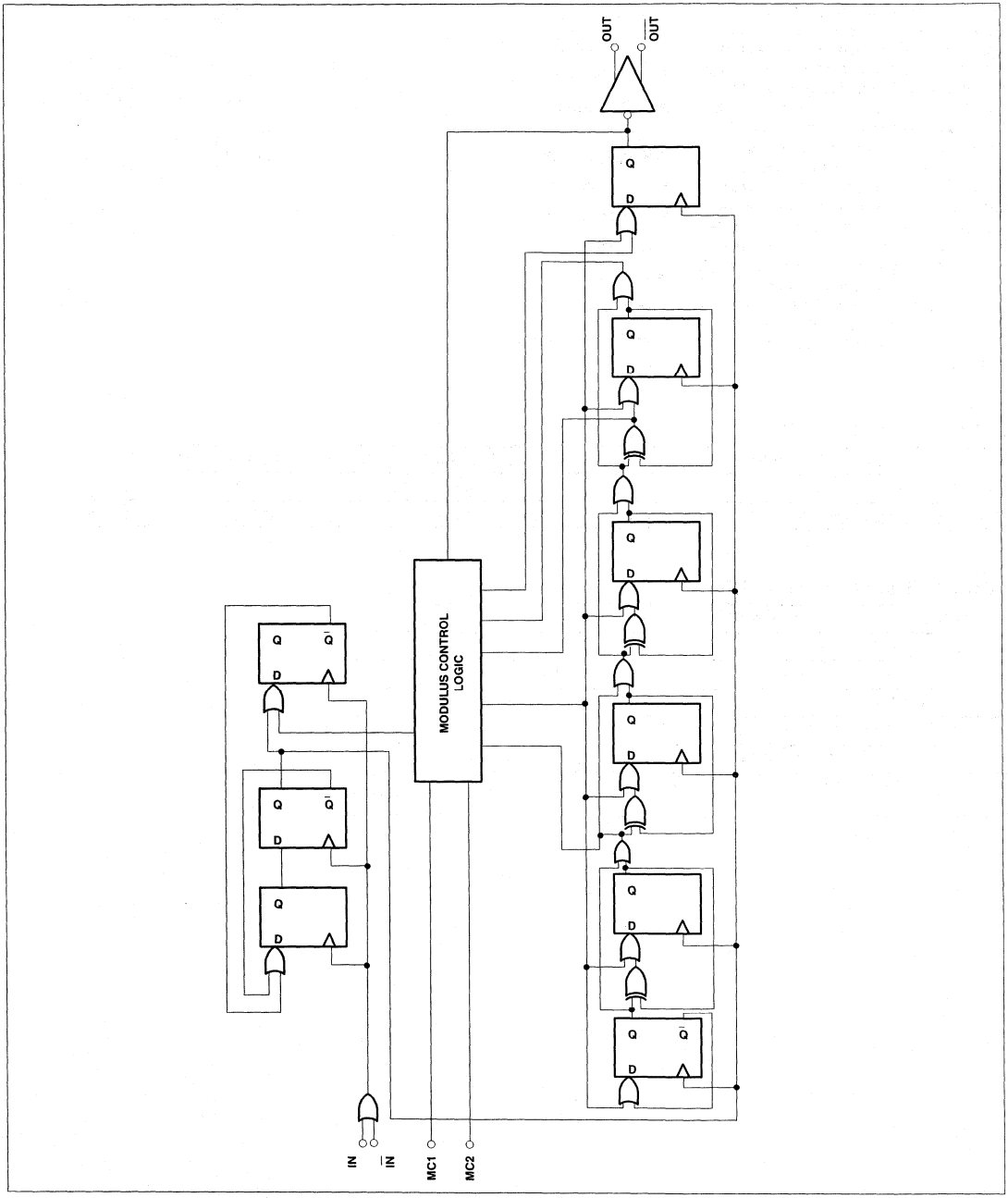
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	-0.3 to +7.0	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{CC} + 0.3)	V
I_O	Output current	10	mA
T_{STG}	Storage temperature range	-65 to +125	°C
T_A	Operating ambient temperature range	-55 to +125	°C
θ_{JA}	Thermal impedance D package N package	158 108	°C/W

Divide by: 128/129/144 triple modulus low power ECL prescaler

SA703

BLOCK DIAGRAM



Divide by: 128/129/144 triple modulus low power ECL prescaler

SA703

DC ELECTRICAL CHARACTERISTICS

The following DC specifications are valid for T_A = 25°C and V_{CC} = 3.0V; unless otherwise stated. Test circuit Figure 1.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range	f_{IN} = 1GHz, input level = 0dBm	2.7		6.0	V
I_{CC}	Supply current	No load		4.5		mA
V_{OH}	Output high level	I_{OUT} = 1.2mA	V_{CC}-1.4			V
V_{OL}	Output low level			V_{CC}-2.6		V
V_{IH}	MC1 input high threshold		2.0		V_{CC}	V
V_{IL}	MC1 input low threshold		–0.3		0.8	V
V_{IH}	MC2 input high threshold		2.0		V_{CC}	V
V_{IL}	MC2 input low threshold		–0.3		0.8	V
I_{IH}	MC1 input high current	V_{MC1} = V_{CC} = 6V		0.1	50	µA
I_{IL}	MC1 input low current	V_{MC1} = 0V, V_{CC} = 6V	–100	–30		µA
I_{IH}	MC2 input high current	V_{MC2} = V_{CC} = 6V		0.1	50	µA
I_{IL}	MC2 input low current	V_{MC2} = 0V, V_{CC} = 6V	–100	–30		µA

AC ELECTRICAL CHARACTERISTICS

These AC specifications are valid for V_{CC} = 3.0V, f_{IN} = 1GHz, input level = 0dBm, T_A = 25°C; unless otherwise stated. Test circuit Fig. 1.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{IN}	Input signal amplitude[1]	1000pF input coupling	0.05		2.0	V_{P-P}
f_{IN}	Input signal frequency	Direct coupled input[2]	0		1.1	GHz
		1000pF input coupling			1.1	GHz
R_{ID}	Differential input resistance	DC measurement		5		kΩ
V_O	Output voltage	V_{CC} = 5.0V		1.6		V_{P-P}
		V_{CC} = 3.0V		1.2		V_{P-P}
t_S	Modulus set-up time[1]				5	ns
t_H	Modulus hold time[1]				0	ns
t_{PD}	Propagation time			10		ns

NOTES:
1. Maximum limit is not tested, however, it is guaranteed by design and characterization.
2. For f_{IN} < 50MHz, minimum input slew rate of 32V/µs is required.

DESCRIPTION OF OPERATION

The SA703 comprises a frequency divider circuit implemented using a divide by 4 or 5 synchronous prescaler followed by a 5 stage synchronous counter, see BLOCK DIAGRAM. The normal operating mode is for MC1 (Modulus Control) to be set high and MC2 input to be set low in which case the circuit comprises a divide by 128. For divide by 129 the MC1 singal is forced low, causing the prescaler circuit to switch into divide by 5 operation for the last cycle of the synchronous counter. For divide by 144, MC2 is set high configuring the prescaler to divide by 4 and the counter to divide by 36. A truth table for the modulus values is given below:

Table 1.

Modulus	MC1	MC2
128	1	0
129	0	0
144	0	1
144	1	1

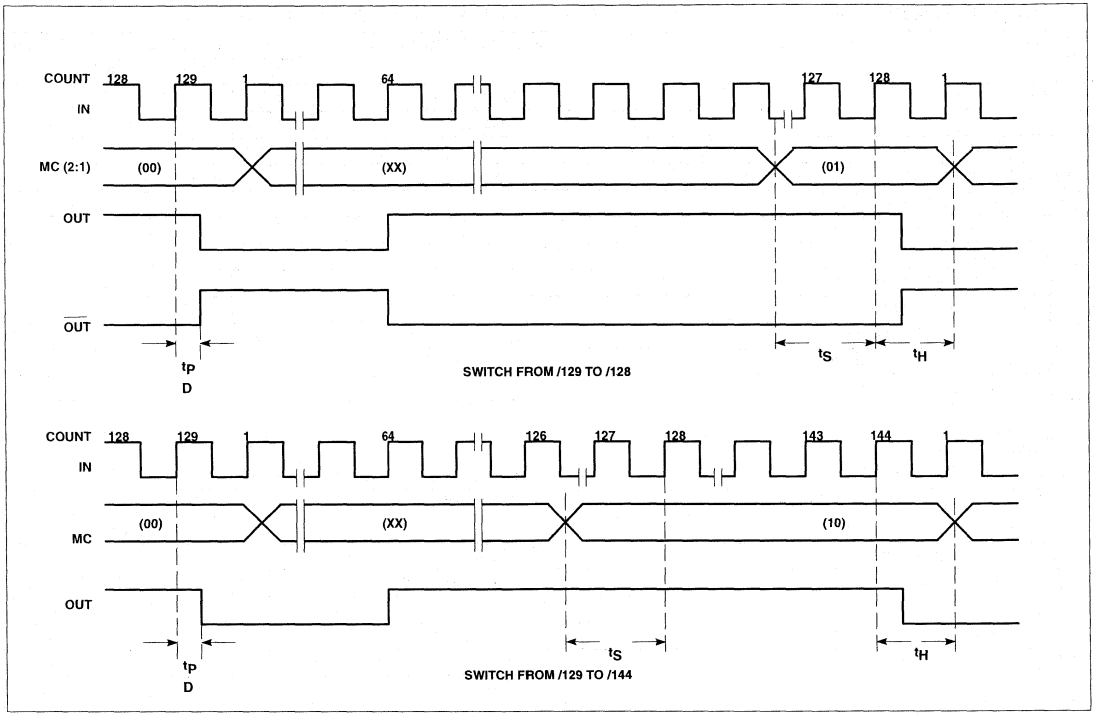
For minimization of propagation delay effects, the second divider circuit is synchronous to the divide by 4/5 stage output.

The prescaler input is positive edge sensitive, and the output at the final count is a falling edge with propagation delay t_{PD} relative to the input. The rising edge of the output occurs at the count 64 with delay t_{PD}.

The MC1 and MC2 inputs are TTL compatible threshold inputs operating at a reduced input current. CMOS and low voltage interface capability are allowed.

The prescaler input is differential and ECL compatible. The output is differential ECL compatible.

AC TIMING CHARACTERISTICS



Divide by: 128/129/144 triple modulus low power ECL prescaler

SA703

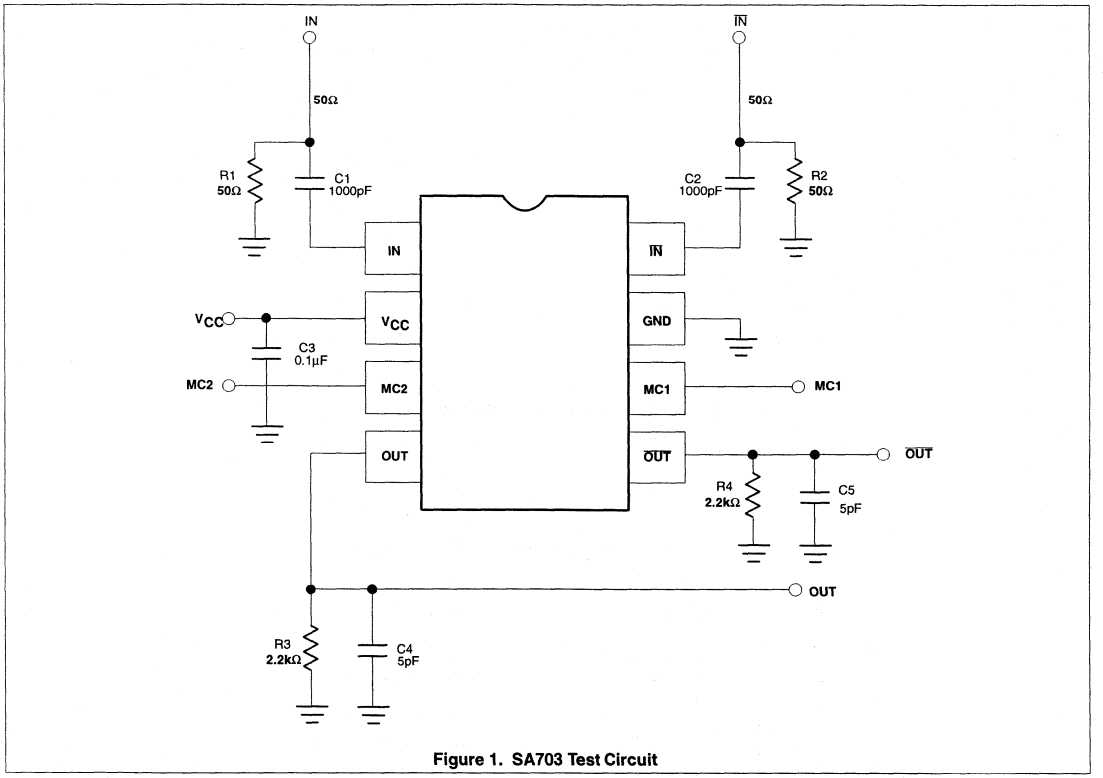


Figure 1. SA703 Test Circuit

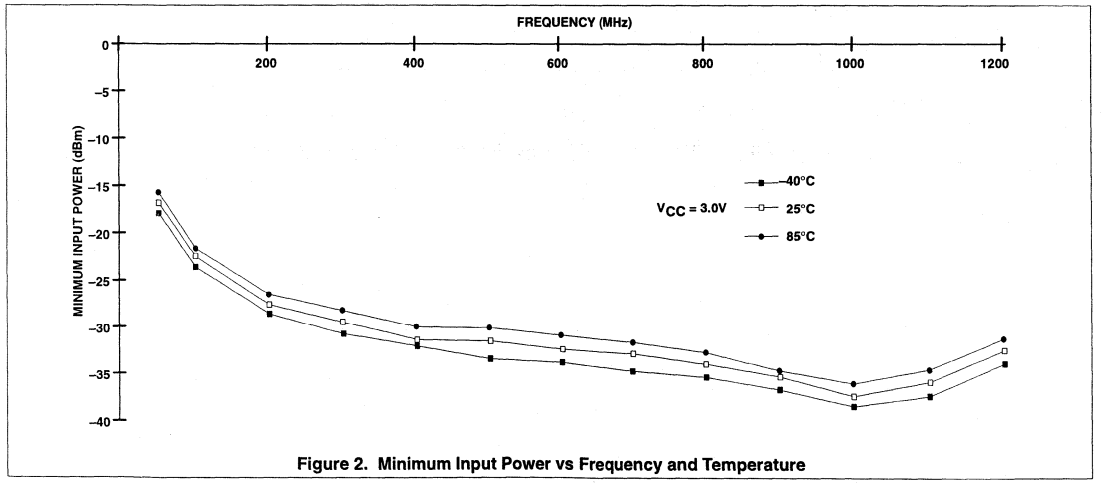


Figure 2. Minimum Input Power vs Frequency and Temperature

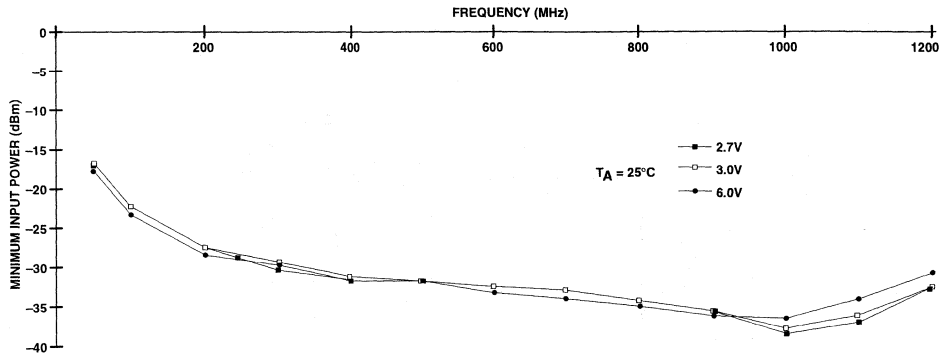


Figure 3. Minimum Input Power vs Frequency and V_{CC}

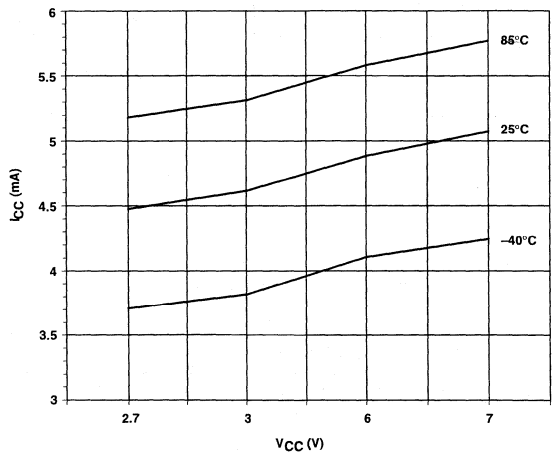
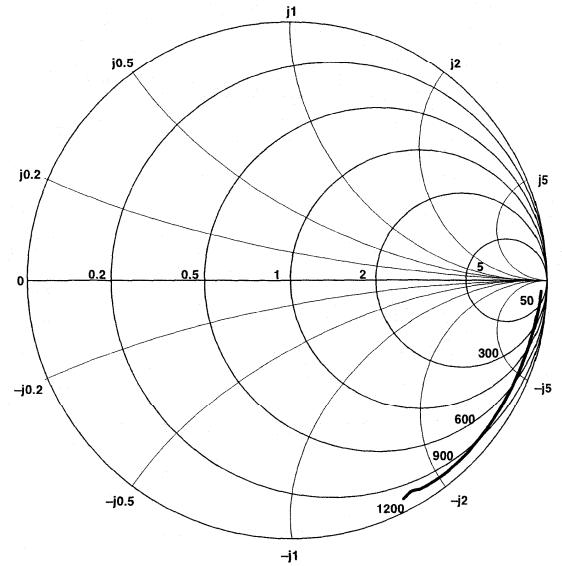


Figure 4. Supply Current vs Supply Voltage and Temperature With No Load



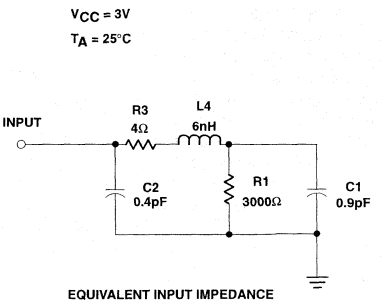
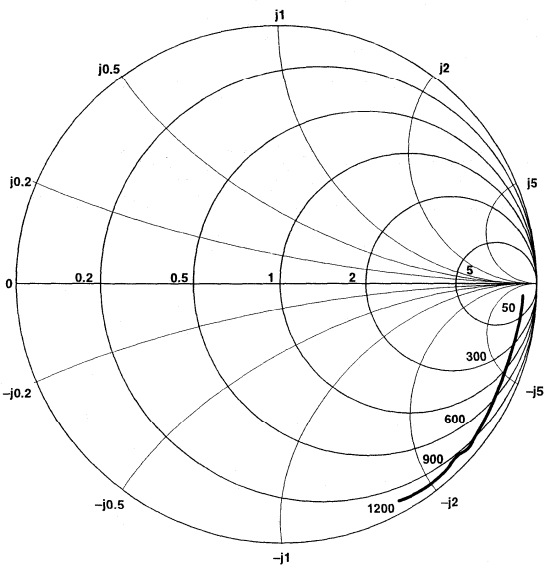


Figure 5. Typical N Package Input Impedance



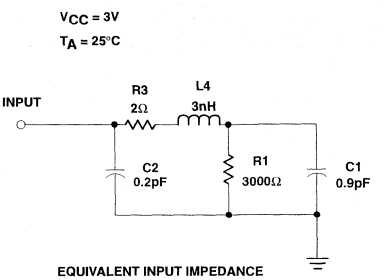


Figure 6. Typical D Package Input Impedance

I/Q transmit modulator SA900

DO NOT DISTRIBUTE WITHOUT ECN DATED AFTER Sept 16, 1997

DESCRIPTION

The SA900 is a monolithic high performance, multi-function transmit modulator for use in cellular radio applications, fabricated in QUBiC BiCMOS technology. The SA900 features both analog (AMPS) mode and complex, I/Q digital (NADC IS–136) mode quadrature modulation functions, a PLL synthesizer with VCO, crystal oscillator, programmable prescalers and Gilbert cell multiplier phase detector with programmable charge pump output. The DUALTX output can be used in DUAL mode cellular phone applications with the AMPS and NADC modulation being applied to the I/Q baseband inputs. The DUALTX output also provides 6-bit power control with 40dB of gain control in 0.63dB steps. In addition, buffered crystal oscillator programmable prescaler outputs are provided to support system clock reference needs. Programming of the SA900 functions are realized by a high speed 3-wire serial interface. The SA900 can be programmed into a sleep mode (low current mode providing crystal oscillator and Master Clock functions), a standby mode (providing crystal oscillator, Master Clock, System Clock 1 and Transmit LO buffer functions), and the AMPS mode and the DUAL mode configurations.

FEATURES

- V_{CC} = 4.0V
- Tx output frequency = 900MHz
- Direct modulation of RF
- DUAL mode, on-chip PA control
- I/Q modulator
- Single sideband quadrature LO generation with no external adjustments required
- On-chip crystal oscillator with 3 buffered outputs
- AMPS/TACS compatible
- On-chip VCO

PIN CONFIGURATION

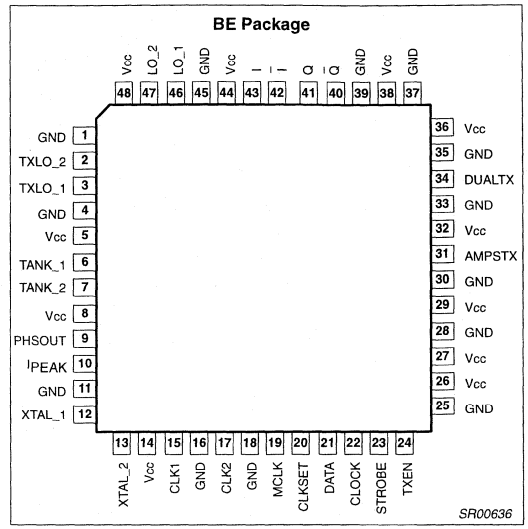


Figure 1. Pin Configuration

- Selective power-down
  - Low power AMPS/TACS mode
  - Low power dual mode NADC
- 48-Pin TQFP package

APPLICATIONS

- North American Digital Cellular (TDMA IS-136)

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
48-Pin Plastic Low Profile Quad Flat Package (LQFP)	-40 to +85°C	SA900BE	SOT313-2

BLOCK DIAGRAM

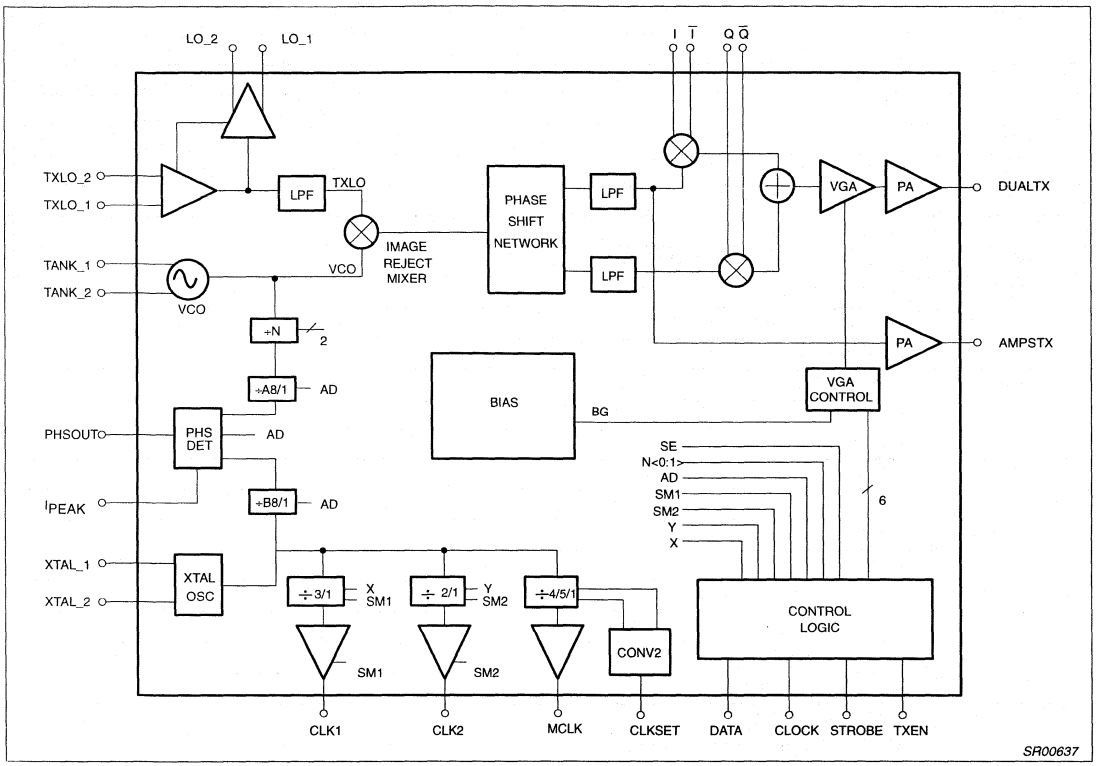


Figure 2. Block Diagram

PIN DESCRIPTIONS

Pin	Description
I	Non-inverting I Mod Signal
$\overline{I}$	Inverting I Mod Signal
TXLO_1/2	Second LO Input (differential/single-ended input)
DUALTX	RF output (850MHz) digital (DUAL) mode, complex modulated output
Q	Non-inverting Q Mod Signal
$\overline{Q}$	Inverting Q Mod Signal
CLK1	Buffered oscillator output (XO ÷3/÷1)
MCLK	Buffered oscillator output (XO ÷4/÷5/÷1)
CLK2	Buffered oscillator output (XO ÷2/÷1)
AMPSTX	RF output (850MHz) AMPS mode
V_{CC}	$+5V_{DC}$ power supply
GND	Ground
Data	Serial data input
Clock	Serial clock input
Strobe	Data strobe input
TXEN	AMPS and Dual Mode transmit enable
CLKSET	Program control pin for MCLK prescaler
XTAL1	Crystal oscillator base input
XTAL2	Crystal oscillator emitter output
PHSOUT	Phase comparator charge pump output
TANK_1	VCO differential tank
TANK_2	VCO differential tank
LO_1/2	Buffered differential TXLO output
I_{PEAK}	Phase comparator current programming

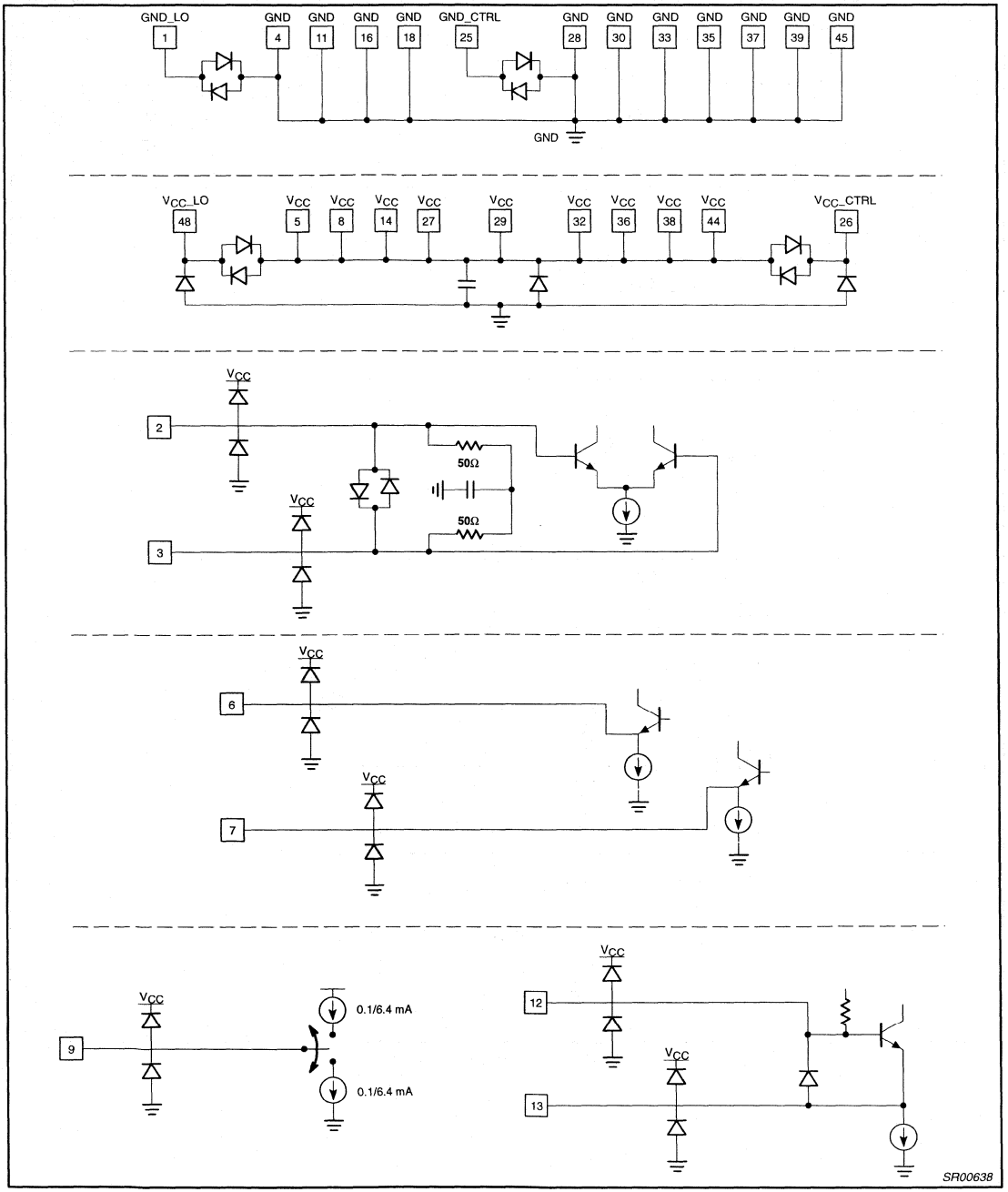


Figure 3. Pin Diagrams

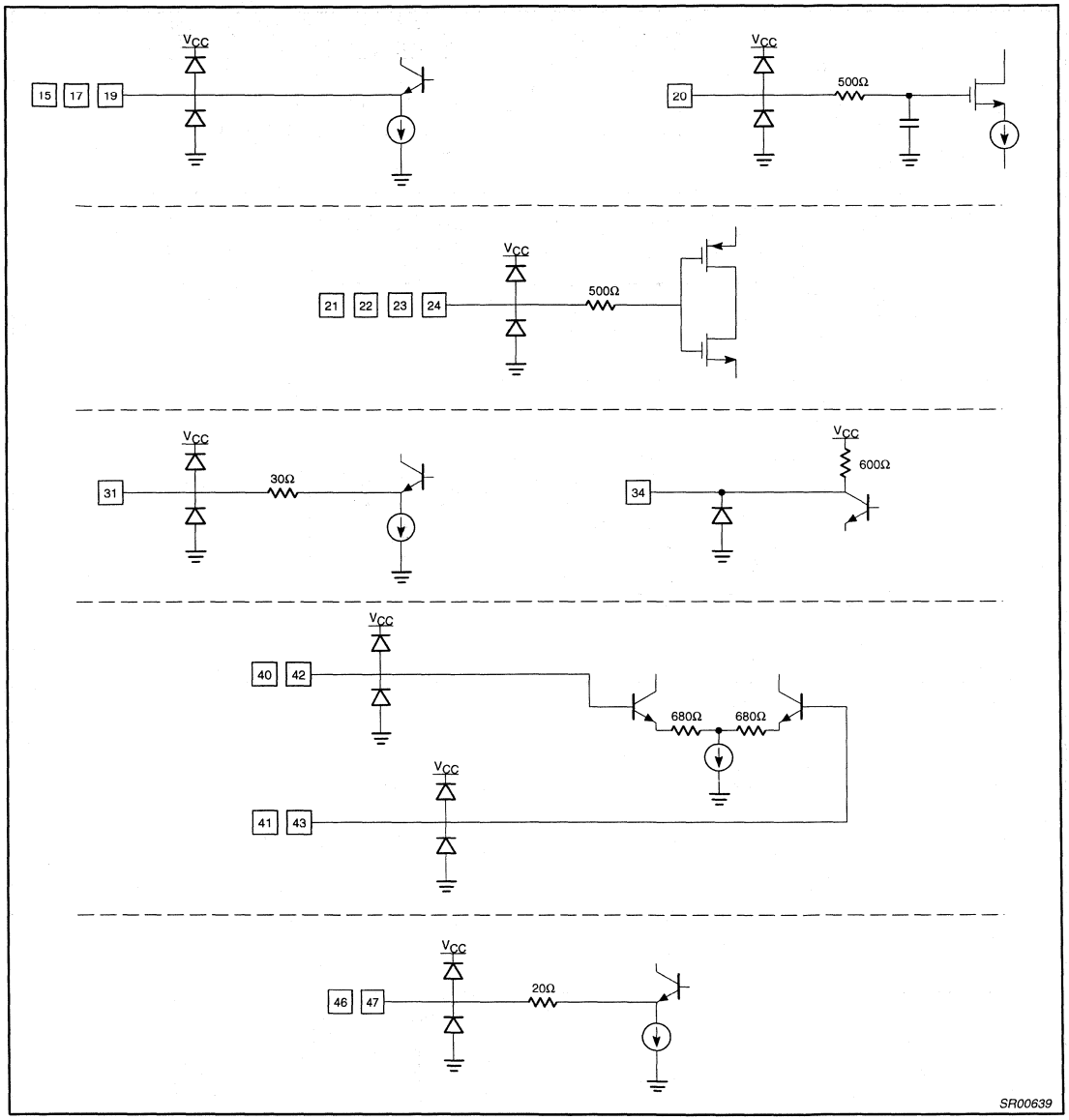


Figure 4. Pin Diagrams (cont.)

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	-0.3 to +6	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{CC} + 0.3)	V
P_D	Power dissipation, T_A = 25°C (still air)	600	mW
T_{JMAX}	Maximum operating junction temperature	150	°C
P_{MAX}	Maximum power input/output	+10	dBm
T_{STG}	Storage temperature range	–65 to +150	°C

NOTE:
1. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance, θ_{JA}.
   48-pin LQFP: θ_{JA} = 67°C/W

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	3.9 to 5.1	V
T_A	Operating ambient temperature range	-40 to +85	°C
T_J	Operating junction temperature	-40 to +105	°C

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +4.0V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{CC}	Power supply range		3.9		5.1	V
I_{CC}	Supply current	Sleep mode		3.1		mA
		Standby mode		8.2		
		AMPS mode		27.5		
		DUAL mode		64		
I / $\overline{I}$	In-phase differential baseband input	DC		0.5V_{CC}		V
Q / $\overline{Q}$	Quadraphase differential baseband input	DC		0.5V_{CC}		V
CLKSET	Divide by 4/5/1	÷ 4		V_{CC}		V
		÷ 5		0.5V_{CC}		
		÷ 1		0		
V_{IL}	Clock, data, strobe, TXEN	Input low	–0.3		0.3V_{CC}	V
V_{IH}	Clock, data, strobe, TXEN	Input high	0.7V_{CC}		V_{CC}+0.3	V

AC ELECTRICAL CHARACTERISTICS

V_{CC} = +4.0V, T_A = 25°C; TANK_1 = 120MHz @ 0 dBm; XO_REF = 30MHz @ –5 dBm; TxLO2 = –13 dBm, unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
TXLO_1/2	Transmit LO input (AC couple) (50Ω)	Input power	-13		-10[1]	dBm
		VSWR (50Ω)		2:1		
		Frequency range	900		1040	MHz
TANK_1/2	VCO tank differential inputs	Frequency range	90[1]	120	140[1]	MHz
PHSOUT	Phase detector charge pump output	Output level	0.5		V_{CC}–0.5	V
I_{PEAK}	PHSOUT programming	R_{SET} = 24kΩ, AD=0	200	300	400	µA
		R_{SET} = 24kΩ, AD=1	0.9	1.2	1.5	mA
XTAL_1	XO transistor base	XO frequency	10[1]	30	45[1]	MHz
		External drive	150[1]	350	500[1]	mV_{P-P}
CLK1	XO divide 3/1, power down SM1=0, 50% duty cycle	Frequency range	3.33[1]	30	45[1]	MHz
	÷3, X=1, ÷1, X=0	Output level, 5kΩ ll 7pF	0.7	1	1.4	V_{P-P}
CLK2	XO divide 2/1, power down SM2=0	Frequency range	5[1]	30	45[1]	MHz
	÷2, Y=1, ÷1, Y=0	Output level, 5kΩ ll 7pF	0.7	1	1.4	V_{P-P}
MCLK	XO divide 4/5/1, 50% duty cycle	Frequency range	2[1]		45[1]	MHz
	÷4, CLKSET = V_{CC}, ÷5, CLKSET = 0.5V_{CC}, ÷1, CLKSET = 0V	Output level, 5kΩ ll 7pF	0.7	1	1.4	V_{P-P}
CLOCK	Serial data clock input, 33% duty cycle	Max clock rate			10[1]	MHz
	Serial interface (CMOS levels)	Logic LOW			0.3V_{CC}[1]	V
	DATA, CLOCK, STROBE, TXEN	Logic HIGH	0.7V_{CC}			V
AMPSTX	AMPS output, SE=1, AD=0, TXEN=1 (AC couple)	Frequency range	820		860	MHz
		VSWR		2:1		
		Output level	–1.5	+2		dBm
	Spurious output	869 to 894MHz		-104		dBm
		824 to 849MHz		-47		dBc
		2 to 824MHz		-41		dBc
		849 to 869MHz		-41		dBc
		894MHz to 8.49GHz		-41		dBc
	TXLO and harmonics			-21		dBc
	Adjacent channel noise power	@30kHz		-95		dBc/Hz
	Alternate channel noise power	@60kHz		-101		dBc/Hz
	Broadband noise power	869 to 894MHz		-136		dBm/Hz
DUALTX	DUAL output, SE=1, AD=1, TXEN=1 (with external matching Figure 9)	Frequency range	820		920[2]	MHz
		VSWR		2:1		
		Output level (avg) (I and Q quad, 0dB VGA)	0	+2		dBm
		Gain flatness		1		dB

AC ELECTRICAL CHARACTERISTICS (continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
DUALTX (cont.)	Linearity (0dB VGA, I and Q inphase)	3rd order	-35	-42		dBc
		5th order		-55		dBc
		7th order		-65		dBc
	Carrier suppression (I and Q quadrature)	VGA = 0dB	-35	-45		dBc
	Carrier suppression (I and Q quadrature)	VGA = –40dB	-28	-33		dBc
	Sideband suppression	I and Q quadrature	-35	-45		dBc
	Spurious output	869 to 894MHz		–104		dBm
		824 to 849MHz		–47		dBc
		2 to 824MHz		–41		dBc
		849 to 869MHz		–41		dBc
		894MHz to 8.49GHz		–41		dBc
	TXLO and harmonics			–21		dBc
	Broadband noise (0dB VGA)	869 to 894MHz		–136		dBm/Hz
		935 to 960MHz		–136		dBm/Hz
	Adjacent channel noise power	@30kHz		–95		dBc/Hz
	Alternate channel noise power	@60kHz		–101		dBc/Hz
Q/$\overline{Q}$	Baseband quadrature differential input	Max frequency		0.8	2[1]	MHz
		Differential modulation level	0.6[1]	0.8	1.0[1]	V_{P-P}
		Differential input impedance	10[1]			kΩ
I/$\overline{I}$	Baseband inphase differential input	Max frequency		0.8	2[1]	MHz
		Differential modulation level	0.6[1]	0.8	1.0[1]	V_{P-P}
		Differential input impedance	10			kΩ
LO_1/2	Buffered TXLO differential outputs (AC coupled)	Frequency range	900		1040	MHz
		VSWR (single-ended)		2:1		
	Output impedance	single-ended		50		Ω
		differential		100		Ω
	Output level	single-ended, 50Ω	50	90		mV_{P-P}
		differential, 100Ω	100	180		mV_{P-P}

NOTES:
1. Guaranteed by design.
2. Needs a different matching component. Max test frequency is 850MHz with test circuit shown in Figure 11.

FUNCTIONAL DESCRIPTION

Dual Mode Operation

The SA900 transmit modulator provides direct single sideband quadrature modulation of the difference of the TXLO and VCO frequencies, while providing quadrature LO signals for the I/Q modulator. The quadrature LO signals are modulated with high linearity by the baseband inphase (I) and quadrature (Q) signals. The summed modulator output produces the lower sideband, while rejecting the upper sideband. The I and Q inputs also provide DC biasing for the modulator inputs. The summed output of the modulator goes to a variable gain amplifier (VGA) to control the output level, it has 40.0dB of attenuation control range, with 0.63dB steps. The power control function is programmed by means of a 6-bit word (see Table 3). The VGA output drives the power amp output stage to provide +2dBm average minimum power level (at 0dB power control) into 50Ω, in conjunction with external matching components on DUALTX. The AD (AMPS/DUAL) and the SE (synthesizer enable) bit control the power up/down of the DUAL mode function. The transition of the TXEN, from low to high turns on the modulator. The falling edge of the TXEN signal disables the synthesizer and modulator. The TXLO is a system supplied LO signal. The SA900 buffers the TXLO signal (LO_1/2) for use with the system synthesizer (such as the SA7025) to form the system LO synthesizer loop. The DUAL mode can also be used for AMPS operation. The AMPS and DUAL mode modulation is generated by the system DSP IC to provide the required I/Q baseband modulation for the SA900. The DUAL output provides low broadband noise output power (so that the receiver sensitivity is not degraded) and high linearity to meet cellular phone system needs. Table 1 provides the VGA power control limits.

The SA900 DUALTX output is externally matched with either a shunt inductor to V_{CC} and a series capacitor or a shunt inductor to V_{CC} and a series inductor. This matches the DUALTX output to 50Ω. Values of the matching components are dependent on PCB layout, typical values are shown in Figure 9.

Table 1. VGA Power Control Limits

VGA	Min.	Typ.	Max.	Relative VGA
0	0	0	0	0
1	-1	-.63	-.2	0
2	-1	-.63	-.2	1
3	-1	-.63	-.2	2
4	-1	-.63	-.2	3
5	-1	-.63	-.2	4
6	-1	-.63	-.2	5
7	-1	-.63	-.2	6
15	-6.6	-5	-3	7
23	-6.6	-5	-3	15
31	-6.6	-5	-3	23
39	-6.6	-5	-3	31
47	-6.6	-5	-3	39
55	-6.6	-5	-3	47
63	-6.6	-5	-3	55
63	-43.2	-40.4	-37.2	0

1. Guaranteed to be monotonic.

AMPS Mode Operation

The SA900 can be configured to operate in the AMPS mode, where FM modulation is applied to the SA900's VCO. For the AMPS mode, the VCO is configured with the proper synthesizer bandwidth to allow the application of the AMPS modulation to the VCO varactor tuned tank circuit. The modulated VCO signal is input into an image reject mixer along with the TXLO signal, where the upper sideband is rejected. This single sideband modulated signal then drives the AMPS output power amplifier. The PA provides +2dBm power level into 50Ω, with no external matching components required. The AD (AMPS/DUAL) and the SE (synthesizer enable) bit control the power up/down of the AMPS mode function. The transition of the TXEN signal from low to high turns on the modulator. The falling edge of TXEN signal disables the synthesizer and the modulator.

Synthesizer Operation

The SA900 synthesizer is comprised of the differential VCO circuit, with external tank components, the Gilbert cell multiplier phase detector with programmable charge pump current, crystal oscillator and programmable prescalers. The charge pump output drives an external second order loop filter. The output of the loop filter is used to provide the control voltage to the VCO tuning varactor to complete the PLL synthesizer. The synthesized VCO output frequency is mixed with the TXLO signal to generate the transmit LO from the lower sideband (the difference of the VCO and TXLO frequencies). The output of VCO is fed to a programmable /N prescaler with user selectable divides of 6, 7, 8 and 9 (all divides configured to provide 50% duty cycle). The output of the /N divider drives the A8/1 prescaler. The A8/1 divide is selected by the AD control bit (AD=1 for /1, and AD=0 for /8). The output of the divide A8/1 is fed into one input of the phase detector. The reference input for the phase comparator is generated from the crystal oscillator (XO) output from the B8/1 prescaler. The B8/1 divide is selected by the AD control bit (AD=0 for /8, and AD=1 for /1). The phase detector compares the prescaled XO reference phase to the VCO prescaled phase, to generate a charge pump output current proportional to the phase error. The phase detector, a Gilbert cell multiplier type, having a linear output from 0 to π ($\pi/2 \pm \pi/2$). The charge pump peak output current is programmable from 100μA for the AMPS mode (AD=0) to a maximum of 6.4mA for the DUAL mode (AD=1) by way of an external current setting resistor placed from I_{PEAK} to circuit ground. The typical loop filter network is shown in Figure 5. The charge pump current output is programmed by

$$AD = 0 \qquad I_{OUT} = 6 \cdot \left(\frac{1.25V}{R_{SET}}\right)$$

$$AD = 1 \qquad I_{OUT} = 24 \cdot \left(\frac{1.25V}{R_{SET}}\right)$$

where R_{SET} is placed between I_{PEAK} and GROUND.

The PLL frequency is determined by

$$VCO = XO \cdot N \cdot \frac{\left(\frac{A8}{1}\right)}{\left(\frac{B8}{1}\right)}$$

where N=6, 7, 8, 9 and A8/1 and B8/1 are controlled by the AD bit (AD=1 A8/1 and B8/1 are divide by 1, AD=0 A8/1 and B8/1 are divide 8).

Table 2. Data Word Format

Mnemonics	Bits	Function
A0	1 (MSB)	Address bit 0 (1)
A1	2	Address bit 1 (0)
A2	3	Address bit 2 (1)
A3	4	Address bit 4 (1)
PC0	5	Power control bit 0
PC1	6	Power control bit 1
PC2	7	Power control bit 2
PC3	8	Power control bit 3
PC4	9	Power control bit 4
PC5	10	Power control bit 5
N0	11	Divide N bit 0
N1	12	Divide N bit 1
AD	13	AMPS/DUAL mode select bit
SE	14	Synthesizer enable bit
NA	15	NA
SM1	16	Sleep mode 1 control bit
SM2	17	Sleep mode 2 control bit
X	18	Divide 3/1 control bit
Y	19	Divide 2/1 control bit
NA	20	NA
NA	21	NA
NA	22	NA
NA	23	NA
NA	24 (LSB)	NA

VCO Operation

The VCO is designed to operate from 90MHz to 140MHz. The VCO tank is configured using a parallel inductor and a dual common cathode tuning varactor diodes. DC blocking capacitors are used to isolate the varactor

control voltage from the VCO tank DC bias voltages. The VCO tuning voltage is generated from the output of the PLL loop filter. The VCO tank configuration is shown in Figure 6.

Crystal Oscillator (XO) Operation

For cellular radio applications, the SA900 will most likely utilize an external reference TCXO in order to provide the frequency stability necessary to operate to system requirements. The output of the system TCXO can be AC coupled to the XTAL_1 input. However, for applications that do not require such accuracy the XO circuit can be configured as a Colpitts type oscillator with the addition of two external capacitors along with the reference crystal and a trim capacitor as shown in Figure 7.

Programmable Clock Outputs

The SA900 generates three buffered XO outputs used for external reference signals. The XO feeds three sets of programmable prescalers, the prescaler outputs are buffered to provide the CLK1, CLK2 and MCLK signals. The CLK1 signal is a selectable divide 3/1 (X=1 divide 3, X=0 divide 1), 50% duty cycle, of the XO reference signal. The CLK2 signal is a selectable divide 2/1 (Y=1 divide 2, Y=0 divide 1), 50% duty cycle, of the XO reference signal. The MCLK signal is a selectable divide 4/5/1 (CLKSET = V_{CC} divide 4, CLKSET = $V_{CC}/2$ divide 5, and CLKSET = 0V divide 1), 50% duty cycle, of the XO reference signal. MCLK is externally set by means of the tri-level CLKSET input to provide a default master system clock prior to programming the SA900.

Programming Operation

The SA900 is configured by means of a 3-wire input (CLOCK, STROBE, DATA) to program the AMPS and DUAL modes, in addition there are two power saving modes of operation, SLEEP and STANDBY. The control logic section of the SA900 is designed using low power CMOS logic. During SLEEP mode only the circuitry required to provide a master clock (MCLK) to the digital portion of the system is enabled. During the STANDBY mode of operation MCLK, CLK1 and the TXLO and buffered LO outputs are powered on, which may be the case when the system is in the receive only mode. In the AMPS or DUAL operational modes all functions of the SA900 are powered on to support receive, transmit and system clock functions. The programming of the SA900 is identical to the programming format of the SA7025 low-voltage 1GHz fractional-N synthesizer, that can be used in conjunction with the SA900 to provide the cellular radio channel selection.

The programming data is structured as a 24 bit long serial data word; the word includes 4 address bits (dedicated 1 0 1 1) for chip select. Data bits are shifted in on the leading edge of the clock, with the least significant bit (LSB) first and the most significant bit (MSB) last. Table 2 shows data word format, the 15th and last 5 bits are not used. Figure 8 shows the chip timing diagram.

Address

A0	A1	A2	A3
1	0	1	1

Divide By N

N0	N1	Divide
0	0	6
1	0	7
0	1	8
1	1	9

AMPS/DUAL Mode

The A/D mode select enables or disables that portion of the circuitry used for either the AMPS or DUAL mode of operation.

AD	Mode
0	AMPS
1	DUAL

Synthesizer Enable

The SE bit turns on and off the synthesizer circuitry.

SE	Operation
0	Disabled
1	Enabled

Sleep Mode 1

The SM1 bit is used to power down the TXLO buffer, the divide 3/1 prescaler and the CLK1 output buffer.

SM1	Operation
0	Power down
1	Power up (STANDBY)

Sleep Mode 2

The SM2 bit is used to power down the divide 2/1 prescaler and the CLK2.

SM2	Operation
0	Power down
1	Power up (with SM1=1 normal operation)

Divide 3

X	Operation
0	Divide 1
1	Divide 3

Divide 2

Y	Operation
0	Divide 1
1	Divide 2

Table 3. Power Control

Attenuation (dB)	PC0 (0.6dB)	PC1 (1.3dB)	PC2 (2.5dB)	PC3 (5.0dB)	PC4 (10.0dB)	PC5 (20.0dB)
0	0	0	0	0	0	0
0.6	1	0	0	0	0	0
1.3	0	1	0	0	0	0
1.9	1	1	0	0	0	0
2.5	0	0	1	0	0	0
3.2	1	0	1	0	0	0
3.8	0	1	1	0	0	0
4.4	1	1	1	0	0	0
5.0	0	0	0	1	0	0
5.7	1	0	0	1	0	0
6.3	0	1	0	1	0	0
• • •						
23.3	1	0	1	0	0	1
• • •						
39.7	1	1	1	1	1	1

Component Designator	Value	
	DUAL Mode	AMPS Mode
R1	560Ω	560Ω
R2	1kΩ	5.6kΩ
C1	2.2nF	2.7μF
C2	No Load	.27μF
C3	33pF	6.8nF
R_{SET}	15kΩ	75kΩ

Typical Filter Network

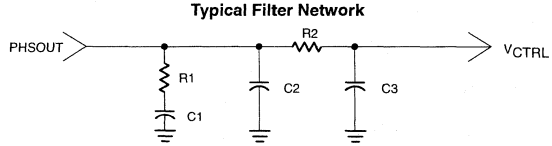


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Figure 5. PLL Loop Filter

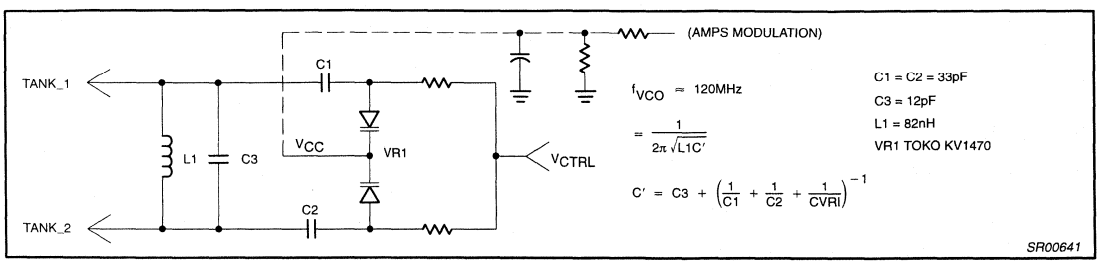

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Figure 6. VCO Tank Configuration

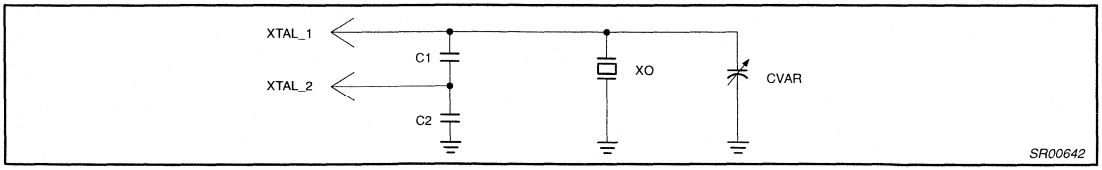


Figure 7. Crystal Oscillator Configuration

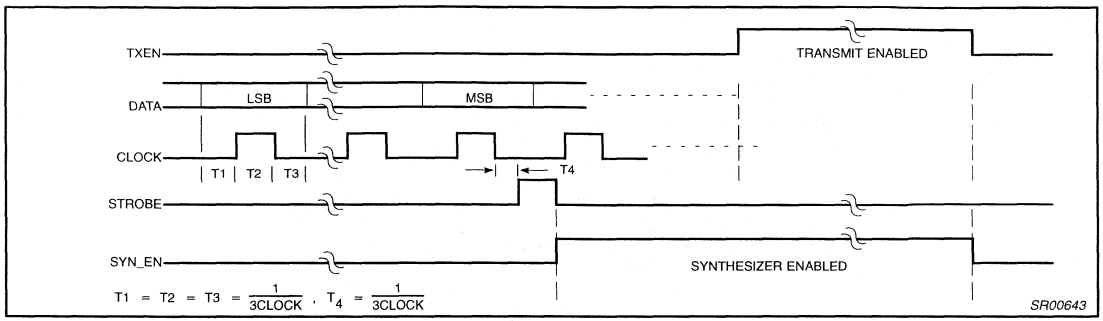


Figure 8. Chip Timing Diagram

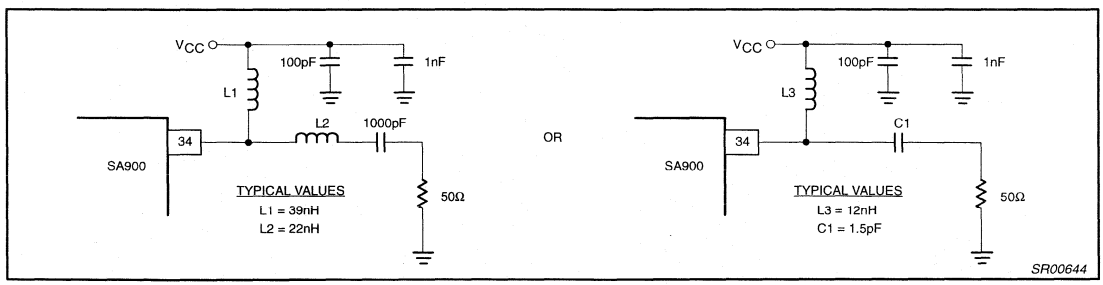


Figure 9. DUALTX Output Matching

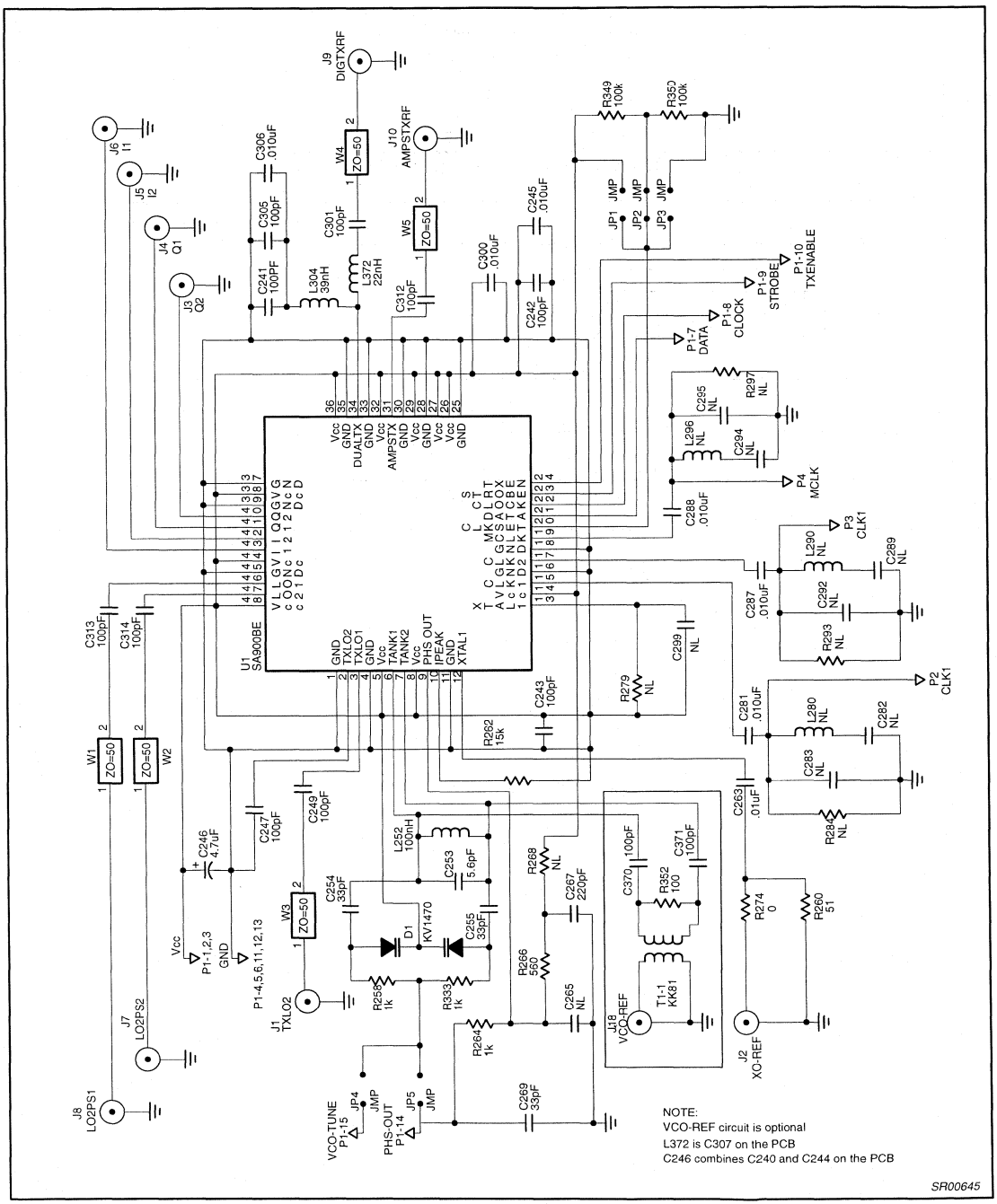


Figure 10. SA900 Application Circuit

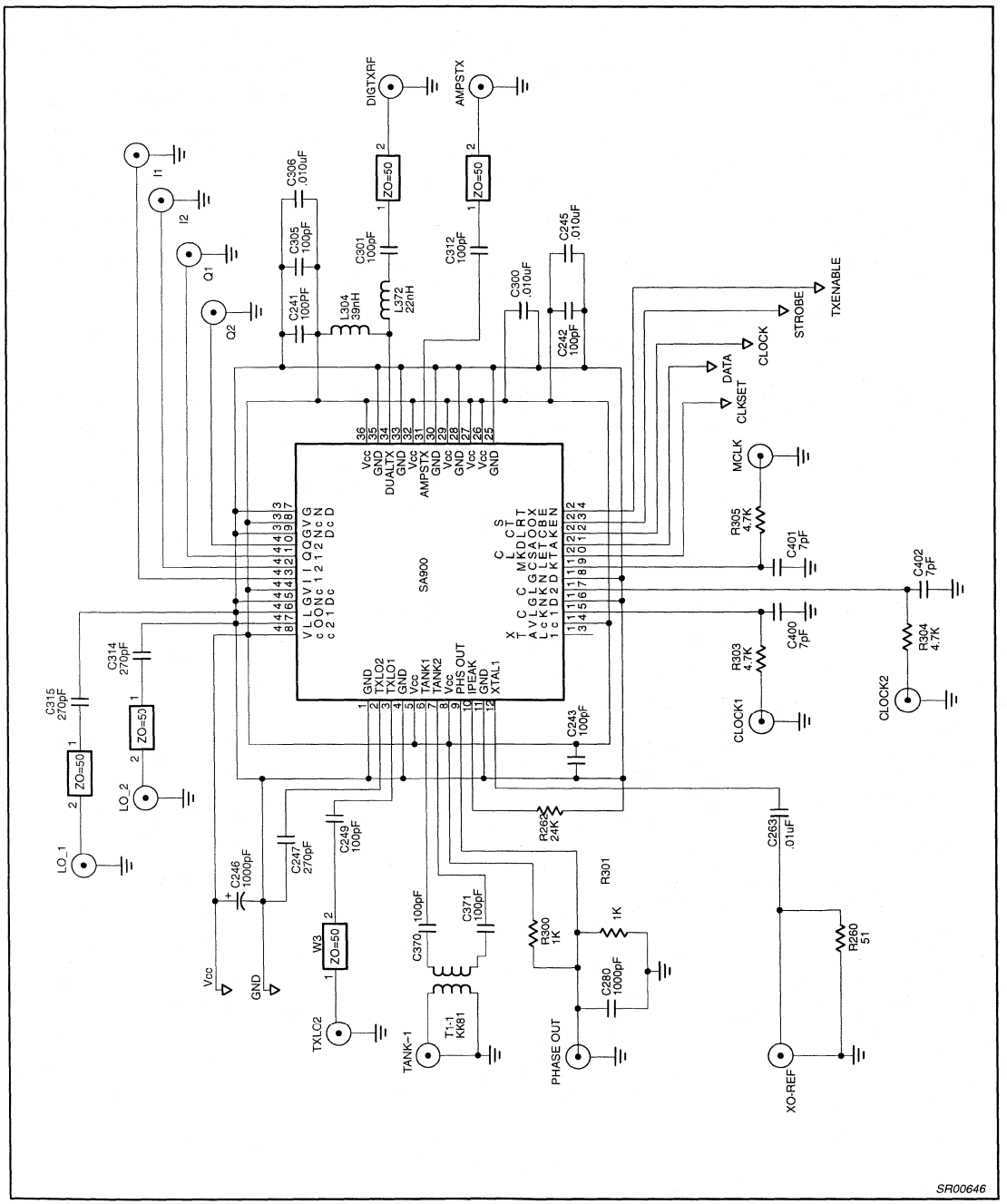
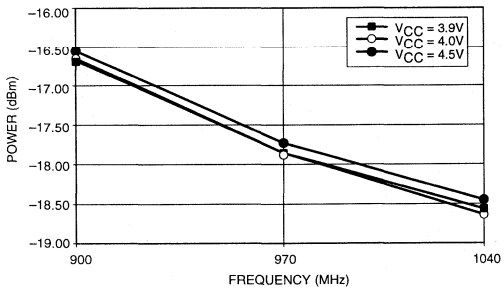
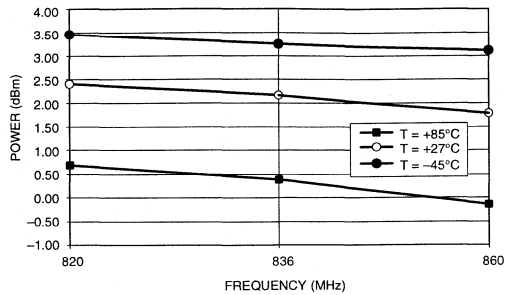


Figure 11. SA900 Test Circuit

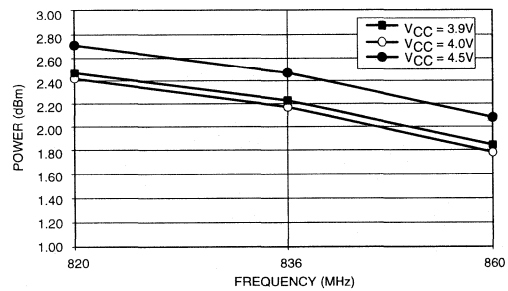
PERFORMANCE CHARACTERISTICS



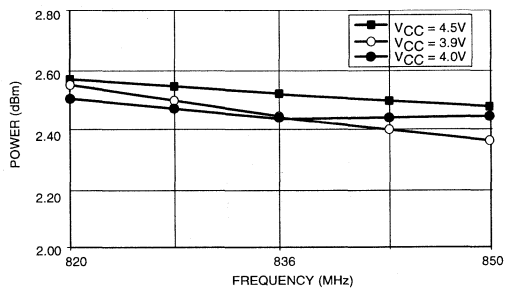
LO Buffer vs. Frequency (27°C, TXLO = –10dBm)



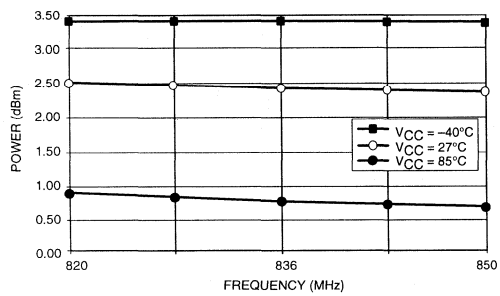
AMPTX vs. Frequency (V_{CC} = 4.0V, TXLO = –10dBm)



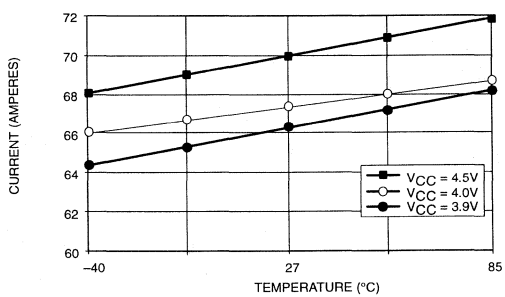
AMPTX vs. Frequency (27°C, TXLO = –10dBm)



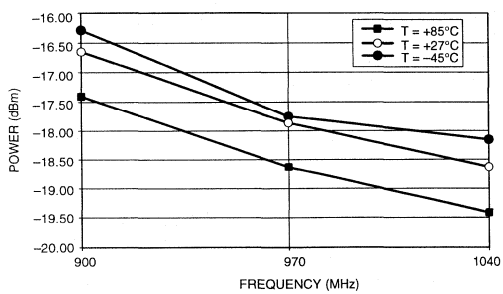
DUALTX vs. Frequency (TEMP 27°C, TXLO = –10dBm)



DUALTX vs. Frequency (V_{CC} = 4.0V, TXLO = –10dBm)



DUAL I_{CC} vs. Temperature



LO Buffer vs. Frequency (V_{CC} = 4.0V, TXLO = –10dBm)

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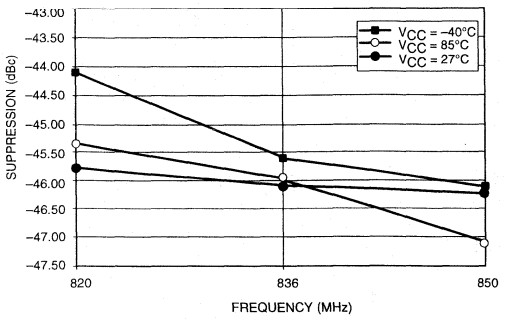
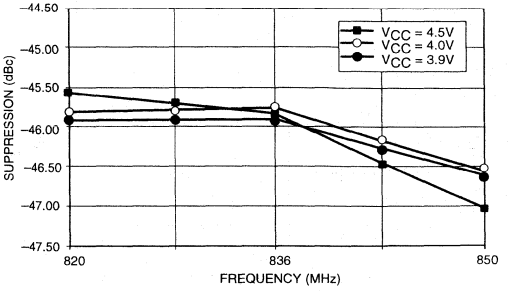
Figure 12. Performance Characteristics

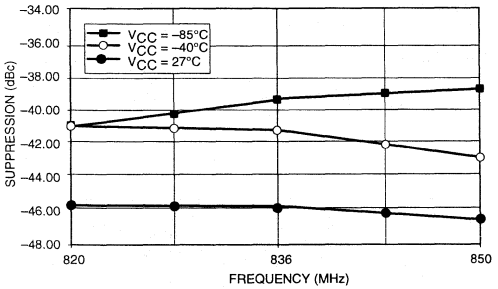
PERFORMANCE CHARACTERISTICS



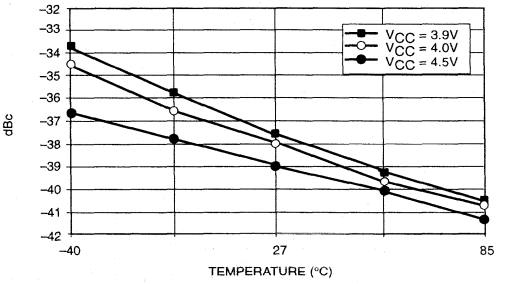
DUALTX Carrier Suppression vs. Frequency (V_{CC} = 4.0, TXLO = –10dBm Single Sideband Mode, With Respect to Lower Sideband)



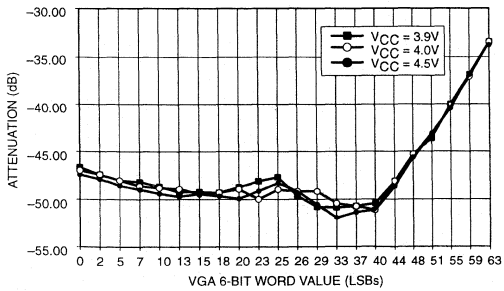
DUALTX Sideband Suppression vs. Frequency (Temperature = 27°C, TXLO = –10dBm Single Sideband Mode, With Respect to Lower Sideband)



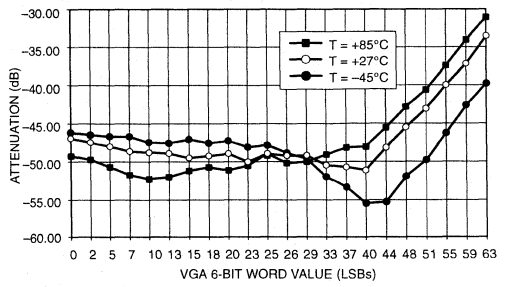
DUALTX Sideband Suppression vs Frequency (V_{CC} = 4.0V, TXLO = –10dBm Single Sideband Mode, With Respect to Lower Sideband)



DUALTX 3rd Order Products vs Temperature (TXLO = –10dBm, f = 836MHz, 0dB VGA I/Q Inphase)



DUALTX Carrier Suppression vs VGA Range (27°C, f = 836MHz, TXLO = –10dBm)

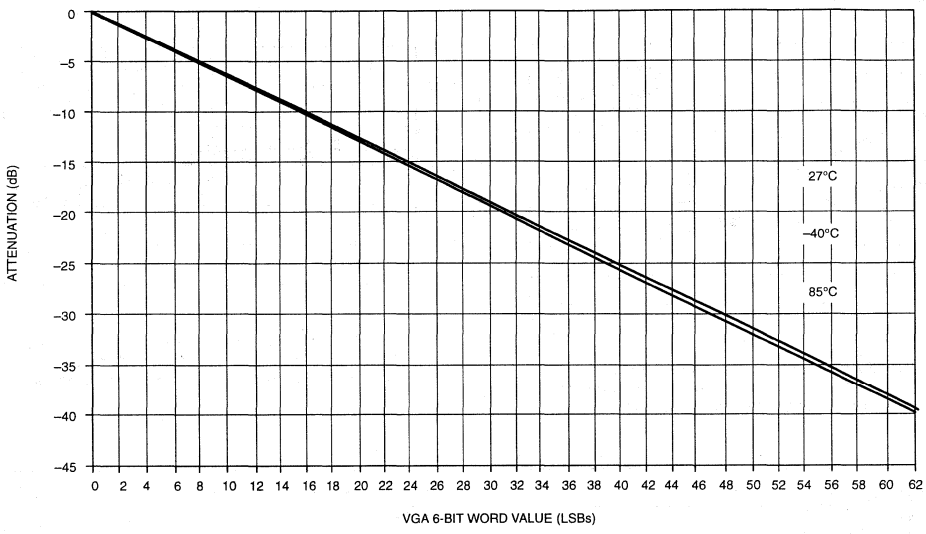


DUALTX Carrier Suppression vs VGA Range (V_{CC} = 4.0V, f = 836MHz, TXLO = –10dBm)

SR00648

Figure 13. Performance Characteristics

PERFORMANCE CHARACTERISTICS



DUALTX VGA Attenuation Profile vs. Temperature (V_{CC} = 4.0V, F = 836MHz)



DUALTX VGA Attenuation Profile vs. V_{CC} (T = 27°C, F = 836MHz)

SR00649

Figure 14. Performance Characteristics

Variable gain RF predriver amplifier SA910

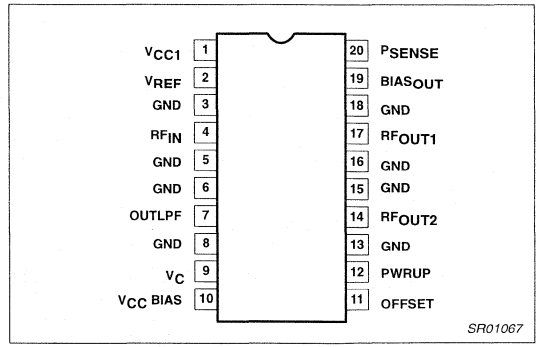
DESCRIPTION

The SA910 is a variable gain predriver amplifier designed for handheld analog cellular telephones. When used with a UHF power transistor, it forms a cost-effective, low-profile, surface mount power amplifier solution (1.2W maximum PAE > 50%). The SA910 integrates power detection and control circuitry that is stabilized over temperature and voltage. In power down mode, the SA910 draws less than 10μA of current. The SA910 is fabricated using Philips QUBiC BiCMOS process.

FEATURES

- MMIC BiCMOS predriver amplifier
- Low voltage 2.7 to 5.5V single supply operation
- 820 to 905MHz bandwidth
- High power gain >20dB
- High power output >23dBm (typical) @ 3V
- Efficiency = 35% (typical)
- Wide gain control range: >32dB
- Few external components required
- Integrated power detector and comparison gain control circuitry
- 50Ω input, open-collector output
- SSOP-20 package
- Integrated regulator with offset adjustment for biasing an external output stage

PIN CONFIGURATION



APPLICATIONS

- 900MHz analog cellular
- Handheld transmitting equipment in the 820 to 905MHz frequency range
- Cordless phone

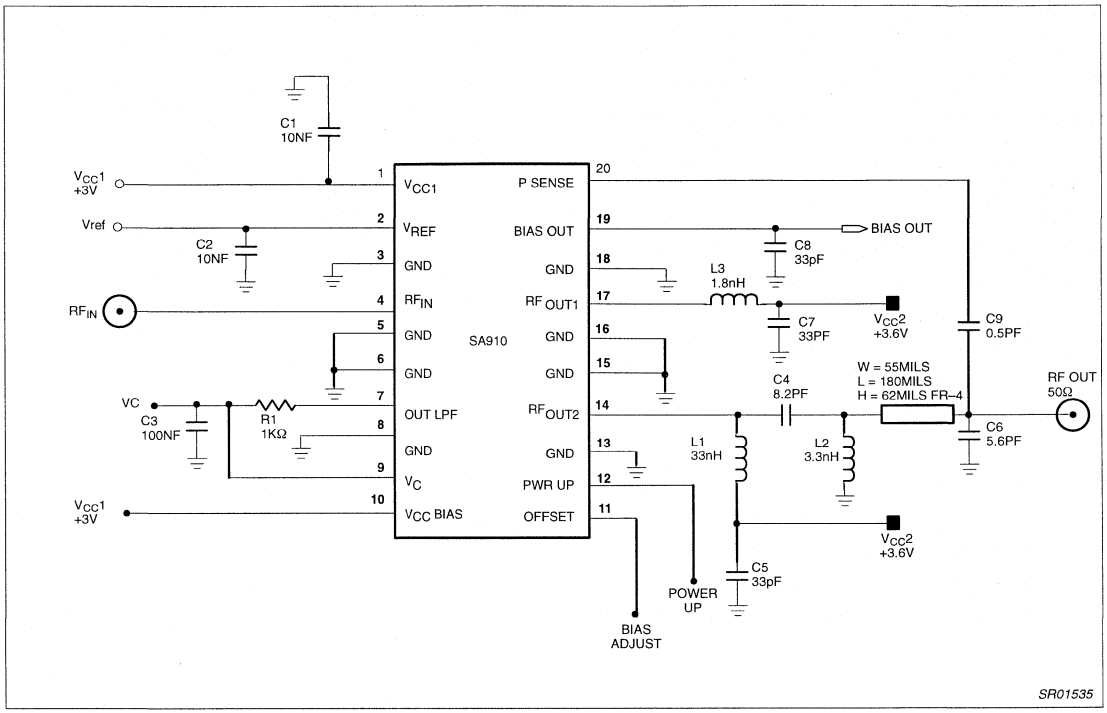
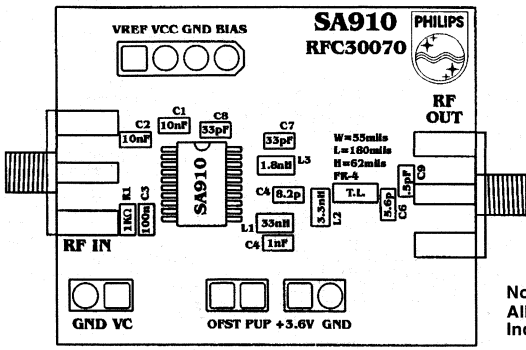


Figure 1. Application Diagram

ORDERING INFORMATION

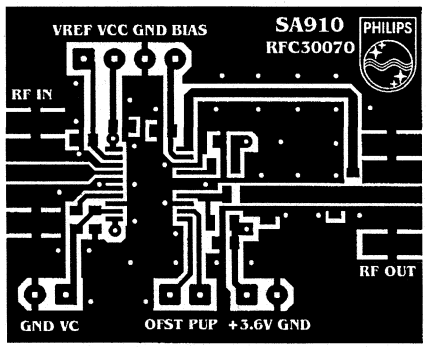
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic SSOP (Shrink Small Outline Package)	-40 to +85°C	SA910	SOT266-1

Components Layout

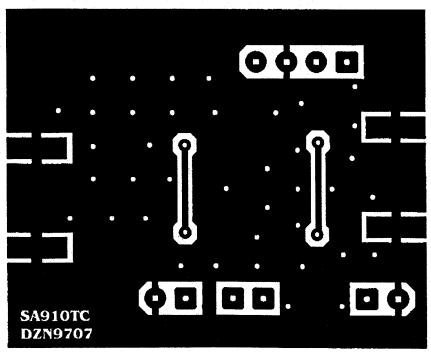


Notes:
All caps are MMC 0603,
Inductors: Toko LL2012

Top Layer



Bottom Layer



SR01547

Figure 2. Application Board Layout of SA910

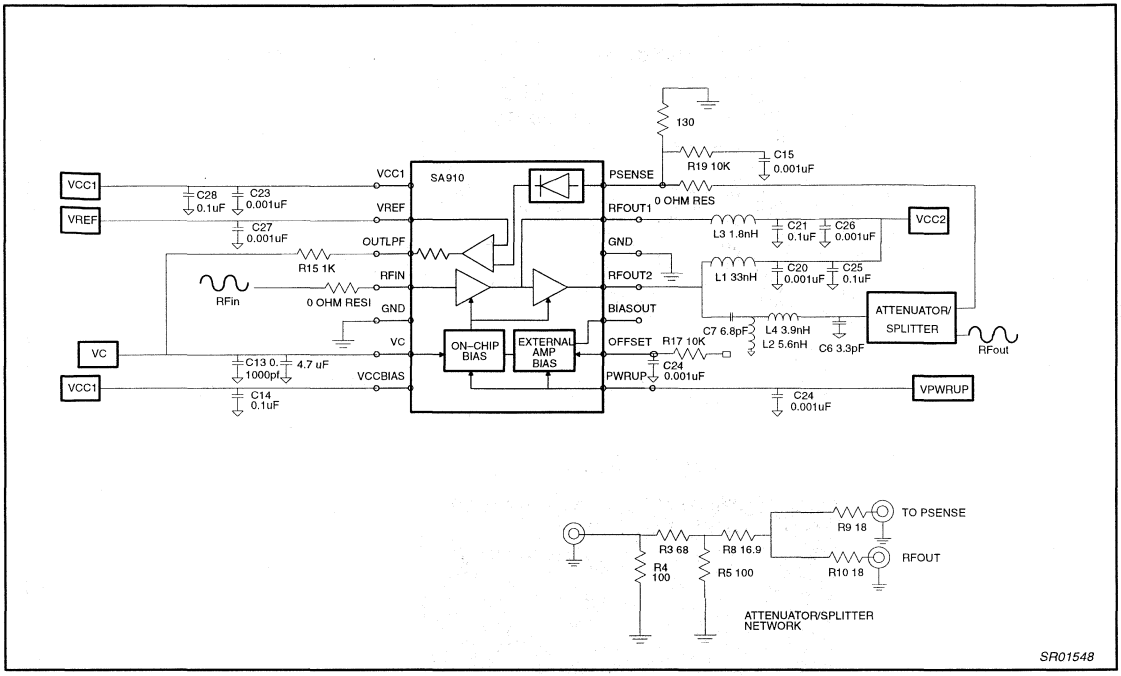


Figure 3. Test Circuit Used In Characterizing SA910

BLOCK DIAGRAM

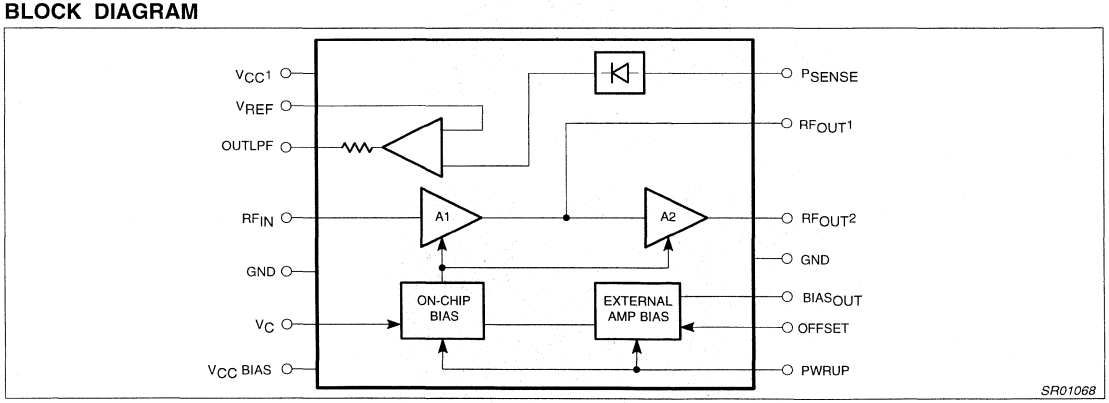


Figure 4. Block Diagram

PIN DESCRIPTIONS

Pin No.	Mnemonic	Function
1	V_{CC1}	Power supply for power sense loop and off-chip bias
2	V_{REF}	Power sense reference voltage input
3	GND	Ground
4	RF_{IN}	Pre-driver input
5	GND	Ground
6	GND	Ground
7	OUTLPF	Power sense detected output
8	GND	Ground
9	VC	Gain control input
10	V_{CC} BIAS	Power supply for on-chip bias
11	OFFSET	External power amp bias offset adjustment
12	PWRUP	Power-up input
13	GND	Ground
14	RF_{OUT2}	Pre-driver output (open collector)
15	GND	Ground
16	GND	Ground
17	RF_{OUT1}	Output of first stage (open collector)
18	GND	Ground
19	$BIAS_{OUT}$	Output to bias external power amplifier stage
20	P_{SENSE}	Power sense input

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC1}/V_{CC}BIAS	DC supply voltages	-0.3 to +6.0	V
	Voltage applied to any other pin[1]	-0.3 to (V_{CC1} + 0.3)	V
P_D	Power dissipation	1.0	W
P_{IN}	Input drive power	5	mW
P_{DET}	Input detect power	20	mW
P_L	Load power	500	mW
T_{STG}	Storage temperature range	-65 to +150	°C

NOTE:
1. Except RF_{OUT1} and RF_{OUT2} which can have 8V max.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC1}/V_{CC}BIAS	Supply voltage	3 to 3.6	V
T_A	Operating ambient temperature range	-40 to +85	°C

NOTE:
1. R_{th} = 75° c/w

AC ELECTRICAL CHARACTERISTICS

$V_{CC}1 = V_{CC}BIAS = +3V; V_{CC}(RF_{OUT}1, RF_{OUT}2) = 3.6V$; $T_A = 25°C$, $Z_S = Z_L = 50\Omega$; $V_C = 2V$; $RF_{IN} = 0dBm$ @ 830MHz; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
f_{RF}	Frequency range		820	830	905	MHz
P_L	Load power at RF_{OUT2}	Saturated[1]	21.5	24		dBm
S_{21}	Small signal gain	$RF_{in} = -20dBm$		31		dB
η	Power added efficiency	$P_L = 24dBm$		35		%
S_{11}	Input return loss	$RF_{in} = 0dBm$		–12		dB
G_C	Gain control range from $V_c = 0.7$ to 2V	dP/dV <120dB/V	32			dB
S_{12}	Reverse isolation			-40		dB
GOFF	Gain at RF_{OUT2} during power-down (RF_{IN} = -20dBm)			-30		dB
PSENSE	Power detector range			25		dB

NOTE:
1. Needs proper output matching.

DC ELECTRICAL CHARACTERISTICS

$V_{CC}1 = V_{CC}BIAS = +3V$, V_{CC} ($RF_{OUT}1$, $RF_{OUT}2$) = 3.6V; $T_A = 25°C$, $Z_S = Z_L = 50\Omega$, ; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNITS
			MIN	-3σ	TYP	+3σ	MAX	
V_{CC}	Power supply voltage range		2.7		3.0		5.5	V
I_{CC}	Total DC current from all V_{CC}	Pin 12 = HIGH; Pin 9 > V_{BE}			210		300	mA
I_{ZB}	I_{CC} under zero bias mode	Pin 12 = HIGH; Pin 9 < V_{BE}					0.7	mA
I_{OFF}	Powerdown current	Pin 12 = LOW					10	µA
I_{PU}	Input current to PWRUP	Pin 12 = HIGH					100	µA
		Pin 12 = LOW					10	
V_{PU}	Input level for PWRUP (Pin 12)	Pin 12 = LOW	0				$0.3V_{CC}$	V
		Pin 12 = HIGH	$0.7V_{CC}$				V_{CC}	V
I_{REF}	Input current to V_{REF} (Pin 2)						1	µA
V_{REF}	Power control reference voltage (Pin 1)		0				2.0	V
V_{BIAS}	$Bias_{OUT}$ voltage (Pin 19) (unadjusted)	$V_C = 2.0V$			0.68			V
I_{BIAS}	DC current available @ Bias-OUT (Pin 19)		30					mA
V_C	Control voltage (Pin 9) range		0				2	V

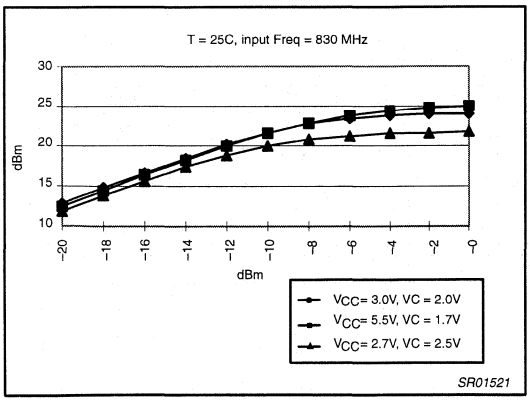


Figure 5. Output Power VS Input Power

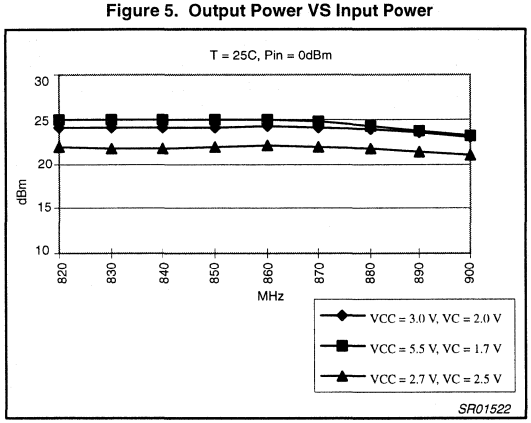


Figure 6. Output Power VS Input Frequency

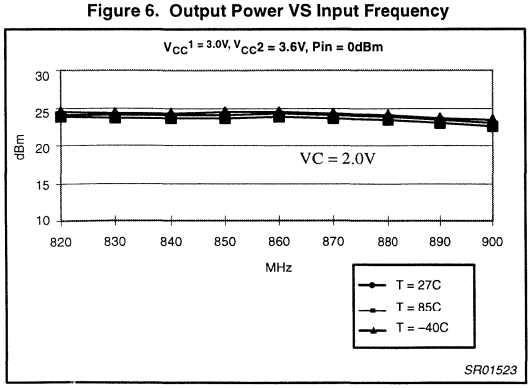


Figure 7. Output Power VS Input Frequency

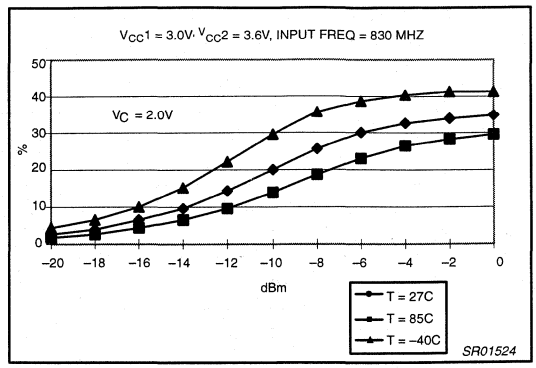


Figure 8. PAE VS Input Power

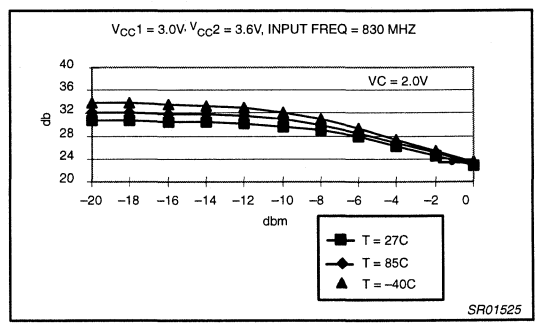


Figure 9. Signal Gain VS Input Power

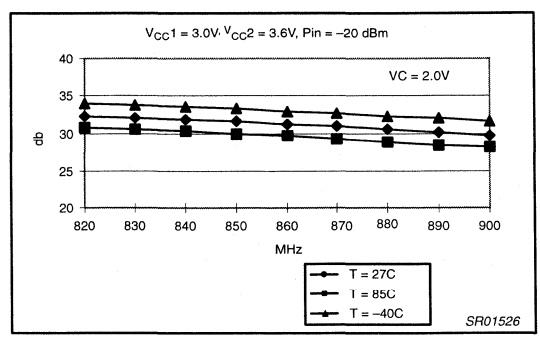


Figure 10. Signal Gain VS Input Frequency

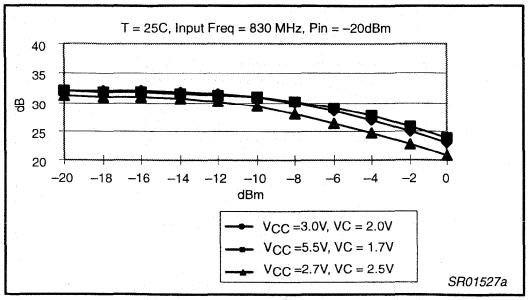


Figure 11. Signal Gain VS Input Power

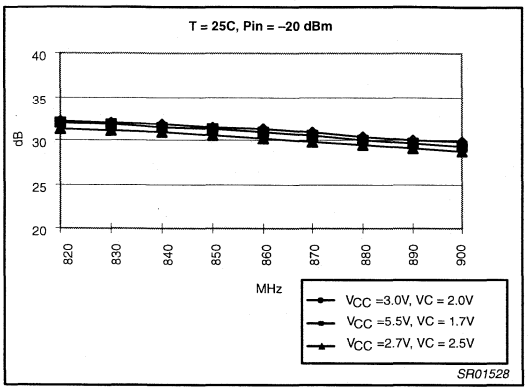


Figure 12. Signal Gain VS Input Frequency

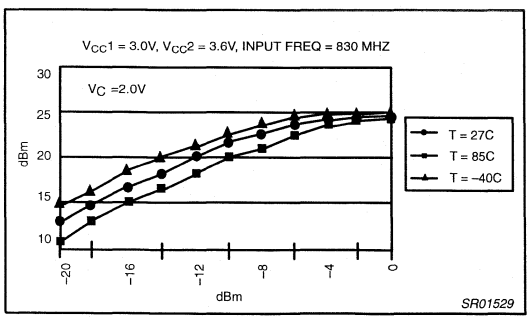


Figure 13. Output Power VS Input Power

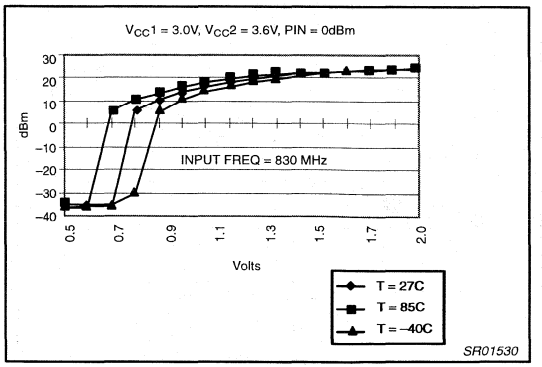


Figure 14. Output Power VS VC

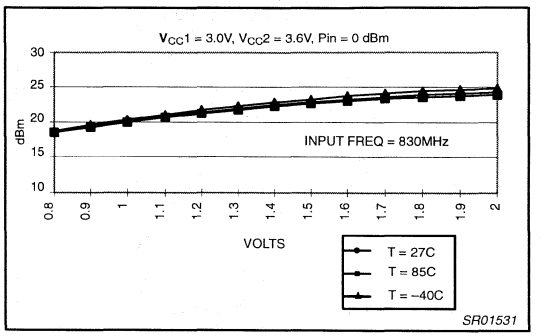


Figure 15. Output Power VS VREF (Closed Loop)

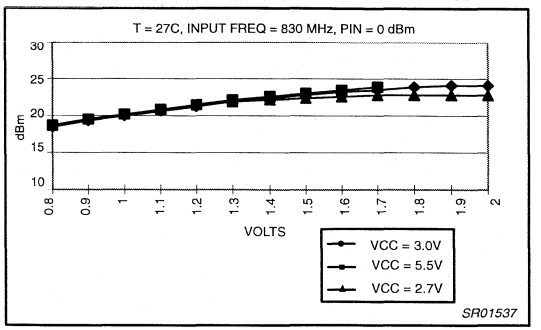


Figure 16. Output Power VS VREF (Closed Loop)

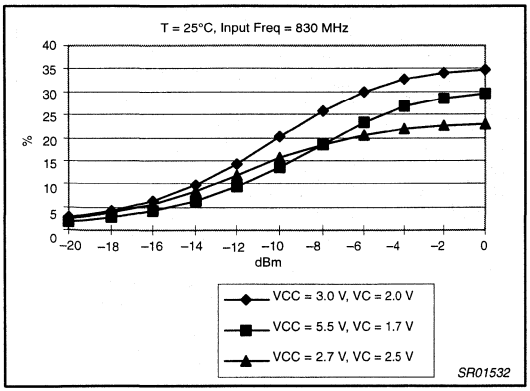


Figure 17. PAE VS Input Power

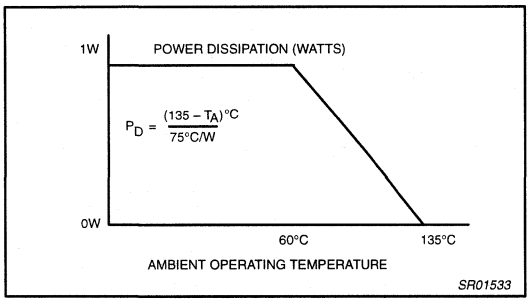


Figure 18. Power De–Rating Curve

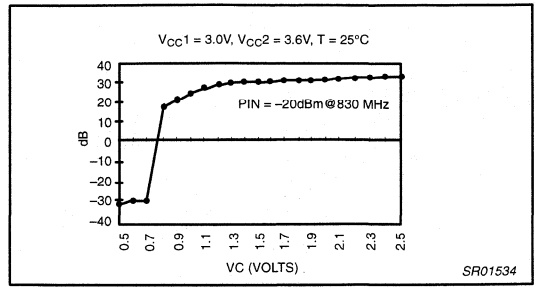


Figure 19. Small Signal Gain VS V_C

Low voltage GSM front-end transceiver — SA1620

DESCRIPTION

The SA1620 is a combined receive (Rx) and transmit (Tx) front-end for GSM cellular telephones. The receive path contains two low noise amplifiers (LNA1 and LNA2) with four switchable attenuation steps. A Gilbert Cell mixer in the receive path down-converts the RF signal to a first IF of 70 to 500 MHz. A second Gilbert Cell in the transmit path transposes a GMSK or phase modulated IF to RF by image reject mixing and has a fixed IF of 400 MHz. A buffered LO signal is fed to Rx and Tx mixers. Rx or Tx path or the entire circuit may be powered-down.

FEATURES

- Excellent noise figure: <2dB for the LNAs at 950MHz
- LNAs matched to 50Ω with external matching components
- LNAs with gain control, 59dB dynamic range in four discrete steps
- LNA gain stability ±0.5dB within -40 to 85°C
- Feedthrough attenuation LNA1 to Rx mixer ≥ 35dB
- Tx power adjustable from -3 to +12dBm by external resistor
- Direct supply: 2.7V to 5.5V
- Battery supply voltage V_{BATT} = 3.3V to 7.5V or direct supply
- Two DC regulators programmable for 3.0V, 3.4V, 3.7V or 5.1V
- Low current consumption: 28mA for Rx or 59mA for Tx
- Fully compatible with SA1638 GSM IF Digital I/Q circuit

APPLICATIONS

- 900MHz front end for GSM hand-held units
- Portable radio, TDMA systems

PIN CONFIGURATION

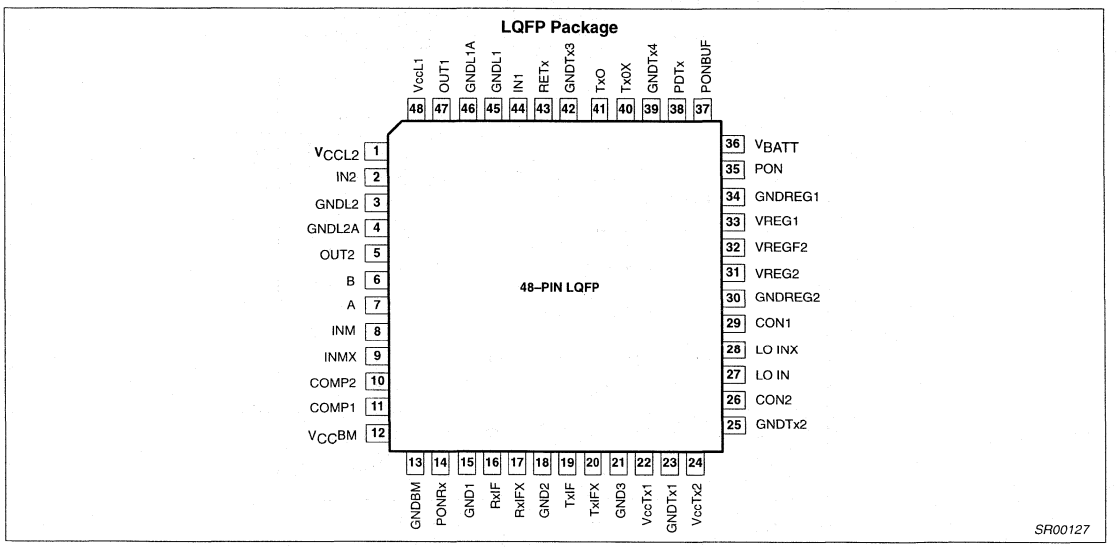


Figure 1. Pin Configuration

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
48-Pin Thin Quad Flat Pack (TQFP)	-40 to +85°C	SA1620BE	SOT313-2

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CCXX}	Supply voltages	2.7 to 5.5	V
V_{BATT}	Battery voltage	3.3 to 7.5	V
T_A	Operating ambient temperature range	-40 to +85	°C

BLOCK DIAGRAM

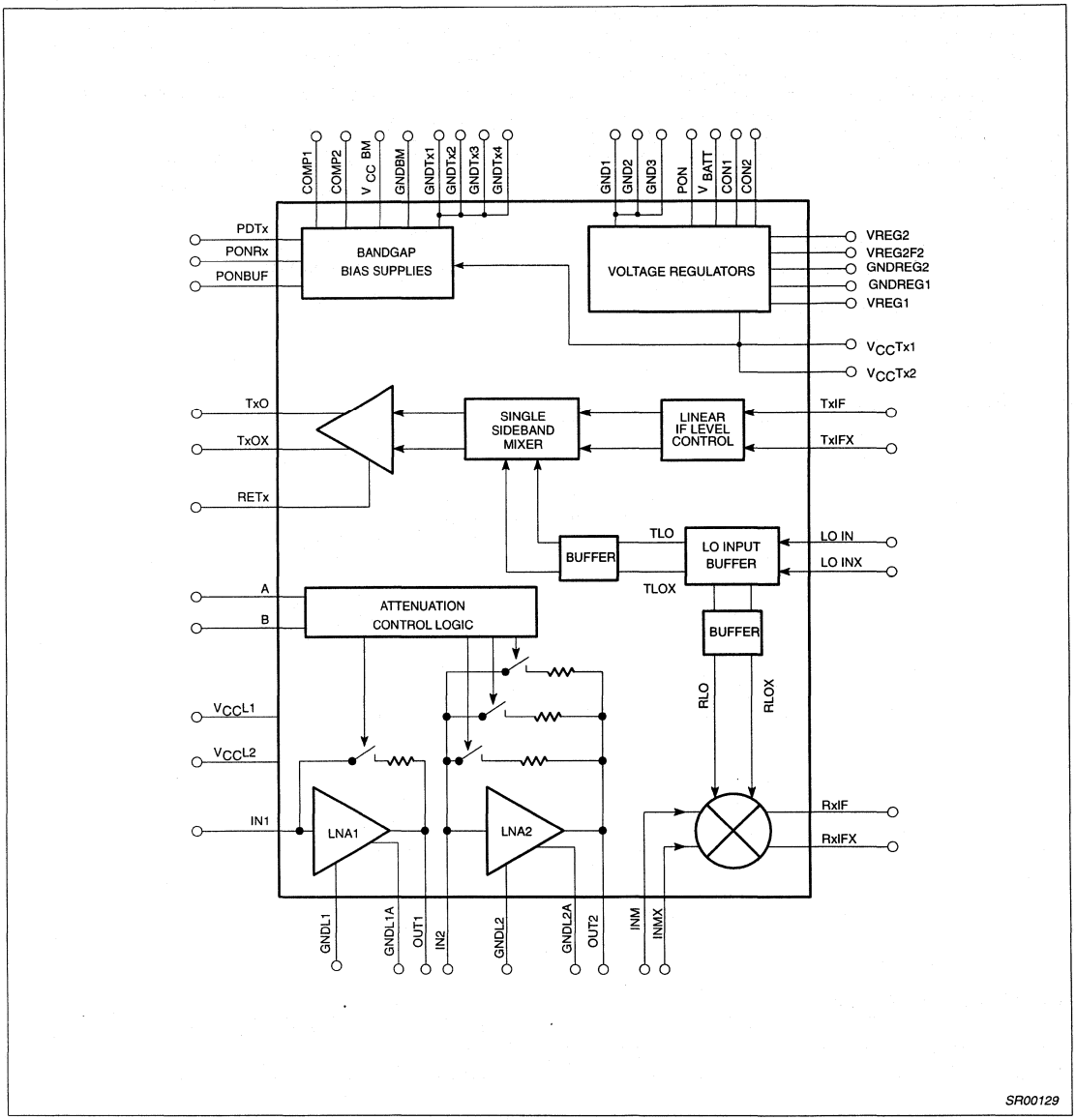


Figure 2. Block Diagram

PIN DESCRIPTIONS

Pin No.	Pin Name	Description
DC Regulators		
15	GND1	Ground of regulator supply
18	GND2	Ground of regulator supply
21	GND3	Ground of regulator supply
26	CON2	Control 2, voltage select for regulator 1 and 2
29	CON1	Control 1, voltage select for regulator 1 and 2
30	GNDREG2	Ground of regulator 2
31	VREG2	Output of regulator 2
32	VREG2F2	Feedback of regulator 2
33	VREG1	Output of regulator 1
34	GNDREG1	Ground of regulator 1
35	PON	Power-on input of regulators
36	V_{BATT}	Input of regulator 1 and 2
Rx Path		
1	$V_{CC}L2$	Positive supply for LNA2
2	IN2	Input LNA2
3	GNDL2	Ground L2 for LNA2
4	GNDL2A	Ground L2A for LNA2
5	OUT2	Output LNA2
6	B	Attenuation select B for LNA1 and LNA2
7	A	Attenuation select A for LNA1 and LNA2
8	INM	RF input for Rx mixer, open emitter
9	INMX	Inverse RF input for Rx mixer, open emitter
10	COMP2	Capacitor for bias stabilization
11	COMP1	Capacitor for bias stabilization
12	$V_{CC}BM$	V_{CC} for Rx Bias and Rx mixer
13	GNDBM	Ground for Rx Bias and Rx mixer
14	PONRx	Power on input for Rx bias supply
16	RxIF	IF output, open collector
17	RxIFX	Inverse IF output, open collector
44	IN1	Input to LNA1
45	GNDL1	Ground L1 for LNA1
46	GNDL1A	Ground L1A for LNA1
47	OUT1	Output LNA1
48	$V_{CC}L1$	Positive supply for LNA1
Tx Path		
19	TxIF	IF input for Tx
20	TxIFX	Inverse IF input for Tx
22	$V_{CC}Tx1$	Positive supply for Tx input
23	GNDTx1	Ground for Tx input
24	$V_{CC}Tx2$	Positive supply for LO and Tx input
25	GNDTx2	Ground for LO and Tx input
38	PDTx	Power down Tx input
39	GNDTx4	Ground for Tx output
40	TxOX	Inverse Tx output, open collector
41	TxO	Tx output, open collector
42	GNDTx3	Ground 1 for Tx output side
43	RETx	Reference resistor for Tx output current
Elements for Tx and Rx Path		
27	LO IN	Input for Local Oscillator signal
28	LO INX	Inverse input for LO or AC ground
37	PONBUF	Power on first stage LO input buffer and bias

NOTES:

1. Device is ESD sensitive. There are no ESD protection diodes at Pins 16, 17, 40 and 41. Thus, open-collector outputs may have increased DC voltage or higher AC peak voltage.
2. Pins 15, 18 and 21 are connected to each other and to a separate ground in REG1 and REG2.
3. Pins 23, 25, 42 and 39 are connected to each other and to the Tx path, LO buffer and associated bias supplies.
4. Pins 22 and 24 are connected to each other providing a sense input. They are also connected to the Tx path, LO buffer and associated bias supplies.
5. Pins 30 and 34 are not internally connected. They must be connected to external grounds.
6. Pins 48, 1, and 12 are not internally connected and have no ESD protection diodes between them. Power may be saved by connecting $V_{CC}L1$ and IN1 or $V_{CC}L2$ and IN2 to ground if LNA1 or LNA2 is not needed.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CCXX}	Supply voltages	-0.3 to +6.0	V
V_{BATT}	Battery voltage	-0.3 to +8.0	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{CCXX}+0.3)	V
ΔV	V_{CC}Tx1,2 pins to V_{CC}BM	-0.3 to +1	V
ΔVG	Any GND pin to any other GND pin	0	V
P_D	Power dissipation, T_A = 25°C (still air)	800	mW
T_{JMAX}	Maximum operating junction temperature	150	°C
P_{MAX}	Maximum power input/output	+20	dBm
T_{STG}	Storage temperature range	–65 to +150	°C
V_{TXO}, V_{TXOX}	Positive RF peak voltage at Tx outputs	6	V
V_{RXIF}, V_{RXIFX}	Positive IF peak voltage at Rx mixer outputs	6	V

NOTE:
1. Maximum junction temperature is determined by the power dissipation is determined by the operating ambient temperature and the thermal resistance, θ_{JA}. 48-pin TQFP: θ_{JA} = 67°C/W.

DC REGULATORS

Two low drop regulators (REG1 and REG2) are included on the chip and may be used to deliver the supply voltage of the main circuitry (e.g., 3V) out of the battery (at V_{BATT} = 3.3 to 7.5V) as shown in Figure 4 and in Table 1.

REG1 is intended to supply, at least, the internal functions of the SA1620. Both regulators may also be used for external circuitry. For this application, different voltages may be programmed as shown in Table 1.

The transmitter supply pins (V_{CC}Tx1,2) also operate as a sensor connection in the feedback loop of REG1 and must be externally connected to pin VREG1. For REG2, the sensor pin VREGF2 must be connected to VREG2.

All ground pins are internally bonded to the header except for pins GNDL1, GNDREG1 and GNDREG2.

When both regulators are not used, connect pins V_{BATT}, PON, CON1, CON2, VREG1, VREG2 and VREG2F2 to ground.

Table 1. DC Reg Output Voltage Control Pins

CON1	CON2	VREG1	VREG2	UNITS
L	L	3 ±5%	3 ±5%	V
L	H	3.4 ±5%	3.4 ±5%	V
H	L	3.7 ±5%	3.7 ±5%	V
H	H	5.1 ±5%	5.1 ±10%	V

NOTES:
1. Logic levels at CON1 and CON2:
   H – Open circuit. Pin must not be connected externally.
   Logic high level supplied on chip.
   L – Connected to ground.
2. Currents at CON1 and CON2:
   H – 0µA
   L (PON = H) – 50µA
   L (PON = L) – <1µA

Table 2. DC Regulators

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{BATT}	Common positive input voltage at both regulators		VREG1+0.3			V
VREG1, VREG2	Output voltages of regulators 1 and 2	V_{BATT} = 3.3V	2.85	3	3.15	V
I_{INT1}	Internal current of REG1 in power-on mode			4 + I_{VREG1}/10		mA
I_{INT2}	Internal current of REG2 in power-on mode			2.5 + I_{VREG2}/10		mA
I_{INT01}, I_{INT02}	Internal current in power-down mode			<15		µA
$I_{VREG1MAX}$[5]	Max output current at VREG1				100	mA
$I_{VREG2MAX}$[5]	Max output current at VREG2				30	mA
BW[6]	V_{BATT} = 3.3V, I_{REG1} = 0.1mA			0.03		kHz
	V_{BATT} = 3.3V, I_{REG1} = 100mA			60		
	V_{BATT} = 7.5V, I_{REG1} = 100mA			80		
F_{REG}[7]	f ≤100kHz			≤–61		dB
	f 10MHz			≤–32		
	f 100MHz			≤–37		
	f 400MHz			≤–48		

NOTES:
1. Power-on pin of Regulator 1 and 2: PON
2. Input currents at PON: <1µA. There are no pull-up or pull-down resistors.
3. Feedthrough attenuation from the logic input PON to the outputs VREG1 and VREG2: ≥40dB.
4. Recommended load capacitors: C529 = C530 = 1µF to ground with series resistance ≤0.1Ω. See Figure 4. Additional optional capacitor ≤1000µF with series resistance ≤5Ω.
5. At $T_j \geq 150°C$ a thermal switch reduces the output current.
6. Typical open loop bandwidths of regulator 1 at V_{REG1} = 3V and C529 = 1µF.
7. Feedthrough attenuation (at the indicated frequency f) from the input V_{BATT} to the outputs V_{REG1} and V_{REG2} at V_{BATT} = 3.3V, (CON1=CON2=L)

DC ELECTRICAL CHARACTERISTICS

V_{CCxxx} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Transmitter						
I_{VCC}	Total supply current	Transmit mode R_{546} = 240Ω		59	90	mA
R1	External resistor[1]			240		Ω
V_{R1}	Internal supply at pin RETx	V_{CC}Tx1,2 = 2.7V		0.43		V
		V_{CC}Tx1,2 = 5.5V		0.45		
I_{R1}	Current at pin RETx	R546 = 240Ω, V_{CC}Tx1,2 = 2.7V		1.7		mA
		R546 = 240Ω, V_{CC}Tx1,2 = 5.5V		1.8		
Low noise amplifiers						
I_{VCC}L1	Current at pin V_{CC}L1	G1hi mode	2.5	3.5	5	mA
I_{VCC}L2	Current at pin V_{CC}L2	G2hi mode	2.5	3.5	5	mA
Receiver						
I_{VCC}	Total supply current	Receive mode R_{546} = 240Ω		28	39	mA
Regulators						
Vreg1	Voltage @ 100mA load	Con1 Con2				
		L L	2.85	3.0	3.15	V
		L H	3.23	3.4	3.57	V
		H L	3.515	3.7	3.885	V
		H H	4.61	5.1	5.61	V
Vreg2	Voltage @ 30mA load	Con1 Con2				
		L L	2.85	3.0	3.15	V
		L H	3.23	3.4	3.57	V
		H L	3.515	3.7	3.885	V
		H H	4.61	5.1	5.61	V
Logic levels[2]						
V_{IH}	Logic 1 level	P_{ON}BUF, PDTx, P_{ON}Rx, A, B	2.0		V_{CCBM}[3]	V
V_{IH}	Logic 1 level	P_{ON}	2.0		V_{BATT}	V
V_{IL}	Logic 0 level		0		0.8	V
I_I	Input logic current				1	µA
C_{Ia}	Input logic capacitance			1.7		pF

NOTES:

1. The output current I_{TXO} + I_{TXOX} is adjustable by the external resistor R546. I_{TXO} + I_{TXOX} = 10 * I_{R546}, I_{R546} = V_{R1}/R546,
2. Thresholds are independent of supply voltages. Thus the SA1620 is compatible with SA1638 and with the power down inputs of usual external voltage regulators.
3. P_{ON} logic 1 max is V_{BATT}.

AC ELECTRICAL CHARACTERISTICS

V_{CCXX} = +3V, T_A = 25°C; RF = 940MHZ; IF=400MHz, f_{LO}=RF + IF; LO = –15dBm; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS[1]					UNITS
			MIN[1]	-3σ	TYP	3σ	MAX[1]	
Low Noise Amplifier LNA1[2]								
S_{21}	Gain	G1hi mode		9.4	10	10.6		dB
		G1hi mode, RF = 1800MHz			–2.5			
		G1lo mode		–13	–12	–11		
	IP3	G1lo mode			28			
$\Delta S_{21}/\Delta T$	Gain temperature sensitivity	G1hi mode			0.003			dB/°C
		G1lo mode			0.0140			
$\Delta S_{21}/\Delta V_{CCL1}$	Gain/voltage sensitivity				0.1			dB/V
$\Delta S_{21}/\Delta f$	Gain frequency variation				0.01			dB/MHz
S_{12}	Reverse isolation	G1hi mode			–19			dB
S_{11}	Input match[3]	50Ω			–11			dB
S_{22}	Output match[3]	50Ω			–14			dB
P_{-1dB}	Input 1dB gain compression	G1hi mode		–15.5	–14	–12.5		dBm
IIP3	Input third order intercept			–5.5	–4	–2.5		dBm
IIP3/Δt	Input third order intercept				0.011			dB/°C
NF	Noise figure				1.9			dB
t_{ON}	Turn-on time				7			µs
t_{OFF}	Turn-off time				0.5			µs
Low Noise Amplifier LNA2[2]								
S_{21}	Gain	G2hi mode		9	10	11		dB
		G2hi mode, RF = 1800MHz			–1.5			dB
		G2lo1 mode		–8.5	–7.5	–6.5		dB
		G2lo2 mode		–22.5	–21.5	–20.5		
		G2lo3 mode		–30	–28.5	–27		
	IP3	G2lo1 mode			18			
		G2lo2 mode			20			
		G2lo3 mode			25			
$\Delta S_{21}/\Delta T$	Gain temperature sensitivity	G2hi mode			0.003			dB/°C
		G2lo1,2,3 modes			0.014			
$\Delta S_{21}/\Delta V_{CCL2}$	Gain/voltage sensitivity				0.1			dB/V
$\Delta S_{21}/\Delta f$	Gain frequency variation				0.01			dB/MHz
S_{12}	Reverse isolation	G2hi mode			–24			dB
S_{11}	Input match[3]	50Ω			–13			dB
S_{22}	Output match[3]	50Ω			–15			dB
P_{-1dB}	Input 1dB gain compression	G2hi mode		–18	–16	–14		dBm
IIP3	Input third order intercept			–8	–6	–4		dBm
IIP3/Δt	Input third order intercept				0.019			dB/°C
NF	Noise figure				2			dB
t_{ON}	Turn-on time				7			µs
t_{OFF}	Turn-off time				0.5			µs

AC ELECTRICAL CHARACTERISTICS (continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS[1]					UNITS
			MIN[1]	-3σ	TYP	3σ	MAX[1]	
Rx Mixer								
PG_C	Power conversion gain[5]			7.5	+8.5	9.5		dB
		RF = 1800MHz			–4			
S_{11}	Mixer input match at ports INM and INMX[4]				–13			dB
NF_M	SSB combined noise figure				10			dB
P_{-1dB}	Input 1dB compression				–7.3			dBm
IIP3	Input third order intercept			0	2	4		dBm
IIP3/Δt	Input third order intercept				0.005			dB/°C
IIP2	Input second order intercept				19			dBm
G_{RFM-IF}	RF feedthrough	400MHz			–26			dB
$G_{LOfloor}$	LO floor feedthrough	400MHz			–30			dB
G_{LO-IF}	LO feedthrough to IF	1.3GHz			–16			dB
G_{LO-RFM}	LO to mixer input feedthrough	1.3GHz			–50			dBm
G_{LO-RF1}	LO to RF LNA1 input feedthrough	1.3GHz			–65			dBm
G_{LNA1-2}	LNA1 output to LNA2 input feedthrough	400MHz 1290-1760MHz			–41 –26			dB
G_{LNA2-M}	LNA2 output to mixer input feedthrough	1290-1760MHz			–23			dB
G_{LNA1-M}	LNA1 output to mixer input feedthrough	400MHz 1290-1760MHz			–50 –35			dB
Receiver [6]								
	Cascaded gain	A,B Logic Level						
		H,H	23.5	26.5	28.5	30.5	33.5	dB
		H,L	6	9	11	13	16	dB
		L,H	–8	–5	–3	–1	+2	dB
		L,L	–41	–36	–32	+28	–23	dB
	Input IP3 @ RFin=–40dBm	H,H		–20	–18	–16		dBm
LO input								
Z_{IN}	Input impedance (each single-ended input)	1.3GHz			35-j97			Ω
P_{IN}	Input power		–25[7]		–15			dBm
A_{SAT}	Transistor saturation limit, max input amplitude				500			mV
Tx IF input								
$\|Z_{IN}\|$	Input impedance	400MHz			2			kΩ
P_{IN}	Input power				–20			dBm
Tx RF output								
P_{OUT}	R546 = 240Ω, V_{CC}Tx1,2 = 3V		5	7.5	8.5	9.5		dBm

NOTES:

1. Due to our automatic test equipment accuracy and repeatability test limits may not reflect the ultimate device performance. Standard deviations are calculated from characterization data.
2. If the LNA1 is not needed, connect pin V_{CC}L1 and IN1 to GND. If the LNA2 is not needed, connect pin V_{CC}L2 and IN2 to GND.
3. Simple L/C elements are needed to achieve specified return loss.
4. The mixer RF inputs (emitters of a Gilbert Cell) may be driven by a symmetrical matching network.
5. Input symmetry suppression is such that the product 6*RF–4*LO is to be suppressed by at least 66dB relative to the wanted IF output when the input to the mixer is at –32dBm.
6. LNA1, LNA2, and the mixer are cascaded. 0 db insertion loss between LNA1 out to LNA2 in and LNA2 out to mixer in.
7. Lowering the LO input power (P_{IN}) from TYP to MIN will lower the mixer gain (PG_C) by 1 dB.

Table 3. Power-Down and Tx/Rx Control Logic

No.	PONBUF	PDTX	PONRX	MODE	RESULT
1	H	H	L	Standby	LO buffer active, Tx and Rx path inactive
2	H	L	L	Transmit	LO buffer active, Tx path active, Rx path inactive (LNAs + mixer)
3	H	H	H	Receive	Tx path inactive, LO buffer and Rx path active (LNAs + mixer)
4	H	L	H	Calibrate	Tx path and Rx LNAs inactive, LO buffer and Rx mixer active
5	L	x	x	Power-Down	Tx- and Rx-path, LO buffers and Bias inactive

NOTES:
1. Logic levels of PONBUF, PDTx and PONRx: TTL, see DC Electrical Characteristics.
2. Logic levels / polarities are compatible with Philips Semiconductors Power Amp Controller PCA5075 and synthesizers UMA1019 or SA8025.
3. First stage of LO buffer and parts of bias supply are powered on by PONBUF.
4. Tx- or Rx-paths may be activated for special timeslots. Lines 1 and 4 show options to support DC offset calibrations at baseband mixers, following in the receiver chain (SA1638).

Table 4. Gain Control Logic for LNA1 and LNA2

INPUT		ATTENUATION STEP	GAIN		POWER CONSUMPTION	
a	b		LNA1	LNA2	LNA1	LNA2
H	H	0	G1hi	G2hi	on	on
H	L	1	G1hi	G2lo1	on	off
L	H	2	G1hi	G2lo2	on	off
L	L	3	G1lo	G2lo3	off	off

NOTES:
1. Logic levels of a and b: TTL
2. For values of G1hi and G1lo, G2hi, G2lo1, G2lo2 and G2lo3 see LNA1 and LNA2 AC Electrical Characteristics.

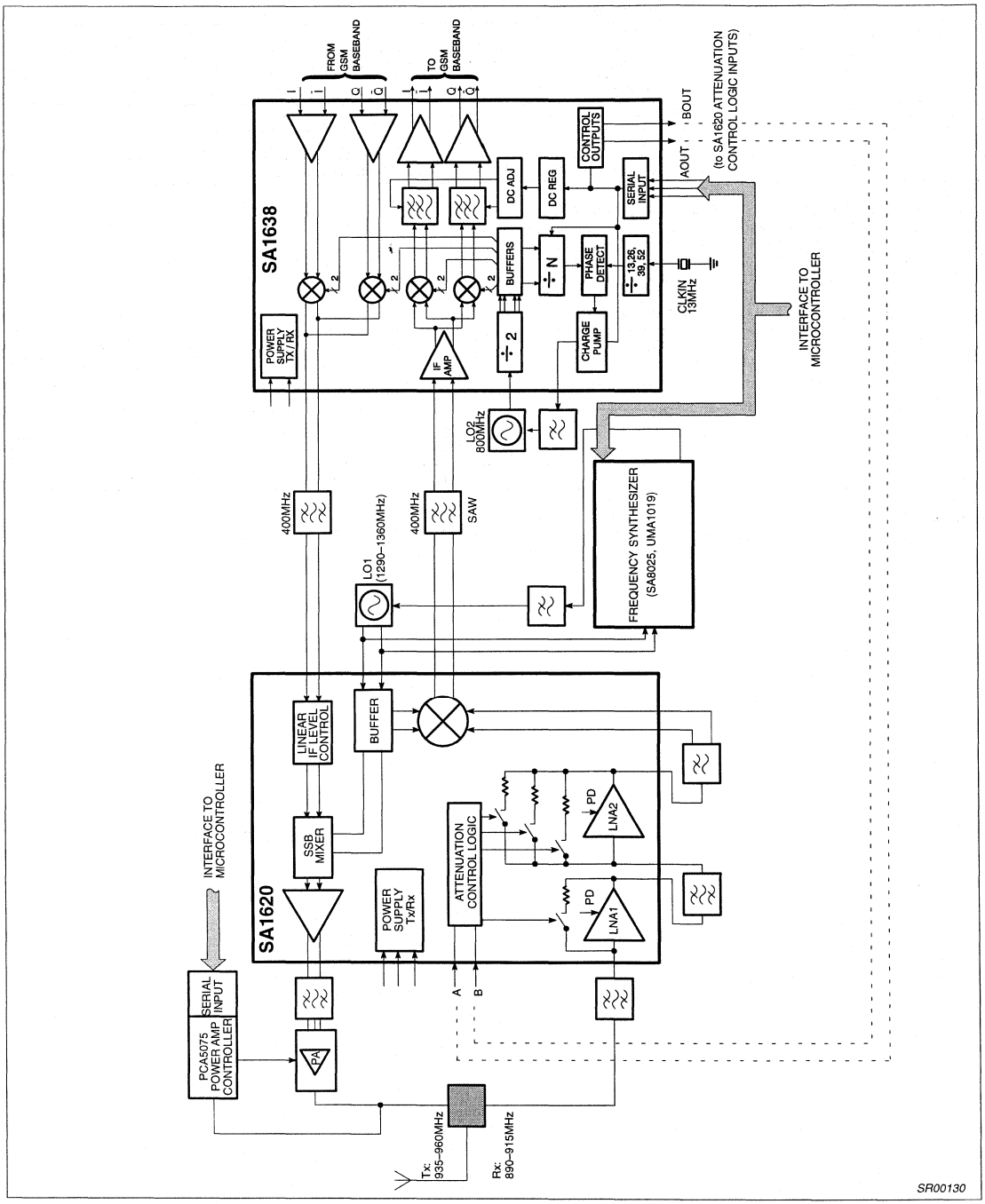

FROM GSM BASEBAND
TO GSM BASEBAND
SA1638
POWER SUPPLY TX/RX
IF AMP
÷ 2
BUFFERS
÷ N
DC ADJ
DC REG
CONTROL OUTPUTS
SERIAL INPUT
PHASE DETECT
÷ 13,26, 39, 52
CHARGE PUMP
AOUT
BOUT
(to SA1620 ATTENUATION CONTROL LOGIC INPUTS)
CLKIN 13MHz
INTERFACE TO MICROCONTROLLER
LO2 800MHz
400MHz
SAW
LO1 (1290–1360MHz)
FREQUENCY SYNTHESIZER (SA8025, UMA1019)
SA1620
LINEAR IF LEVEL CONTROL
BUFFER
SSB MIXER
ATTENUATION CONTROL LOGIC
POWER SUPPLY Tx/Rx
PD
LNA2
LNA1
A
B
INTERFACE TO MICROCONTROLLER
SERIAL INPUT
PCA5075 POWER AMP CONTROLLER
PA
Tx: 935–960MHz
Rx: 890–915MHz
SR00130

Figure 3.

Overview of Dual GSM/PCN Architecture

The SA1620 RF front-end and SA1638 IF transceivers form a dual conversion architecture which uses a common IF and standard I/Q baseband interface for both transmit and receive paths. This approach avoids the screening difficulties of direct modulation in the transmit direction and the mass production and practical performance issues related to direct conversion in the receive direction. The time division multiplex nature of the GSM system permits integration of the transmit and receive functions together on the one RF and one IF chips. This simplifies the distribution of local oscillator signals, maximizes circuitry commonality, and reduces power consumption.

The SA1620 and SA1638 allow considerable flexibility to optimize the transceiver design for particular price/size/performance requirements, through choice of appropriate RF and IF filters. The receive IF may be chosen freely in the range 70–500MHz, while the transmit IF is fixed to 400 MHz. The comparison frequency of the SA1638 PLL is high in order to provide fast switching time.

With suitable choice of the IF, an identical SA1638 IF receiver design can be used for both 900MHz GSM and 1800MHz PCN (DCS1800) equipment.

General Benefits/Advantages

- 2.7V operation. Compatible with 3V digital technology and portable applications. (Higher voltage operation also possible, if desired.)
- Excellent dynamic range. The availability of two LNAs allows flexibility in receiver dynamic design for portable and mobile GSM spec. applications with appropriate filters. If for a particular application a GaAs or discrete front-end is desired, one of the LNAs can be left unpowered. The placing of the AGC gains switches at the front means that for most of the time some attenuation will be inserted, further increasing typical dynamic performance beyond that specified by GSM.
- High power transmit output driver, delivering +8.5dBm output. This is sufficient to drive a filter and power amplifier input, without a driver amplifier. To avoid unnecessary current consumption the output power can be reduced, if not required, by appropriate choice of an external resistor.
- DC offsets generated in the receive channel are independent of the AGC setting, and correctable by software to prevent erosion of signal handling dynamic range by DC offsets. Independence of DC from AGC setting is achieved by putting the gain switches in the RF front-end.
- Minimal high-quality filter requirements. As a result of the integration in the SA1638 of high quality channel selectivity filters, only sufficient filtering is needed in the receive path to provide blocking protection for the second mixers. This reduces receiver cost and size.
- Operation at a high IF allows RF image reject filters to be relaxed. For example, at a 400MHz IF, the natural gain roll-off in the LNAs and mixer suppresses the image signal in the 1800MHz band by typically 28dB below the desired 900MHz band signal.

Receive Path

Multiple LNAs allow the flexibility to exploit the best choice of currently available filters (on performance, size, or cost grounds). This approach is preferable to a single high-gain stage as the stray cross-coupling effects between pins remain manageable. In a single stage amplifier this would limit the amount of rejection of out-of-band signals that could be achieved, and would also limit the amount of AGC attenuation that could be practically implemented.

The LNAs are powered up only when PONBUF, PDTx and PONRx are high, to allow a high degree of battery economy. If greater sensitivity is required for an application, an external preamplifier circuit can be used instead of LNA1, and LNA1 left unconnected.

A special mode is provided with just the IF output related circuitry active in order to allow calibration of the DC offset at the SA1638 baseband receive outputs. This offset contains a contribution due to coupling effects between the second local oscillator and the IF circuitry, and therefore the receiver is set up in the receive state (but with incoming signals excluded) to allow accurate offset calibration.

Gain Control

Gain control is implemented in the SA1620 RF front-end. This avoids the disruption of the DC offset at the baseband IQ outputs that is typically caused by changes in the AGC. The SA1620 and SA1638 are designed so that the GSM dynamic range requirements can be met with the AGC remaining on the maximum gain setting.

These gain steps scale the dynamic range of the received signal (e.g., 90dB for GSM) into the dynamic range of the baseband processing device.

The absolute gain tolerances may be measured together with the attenuation tolerances of external filters during production of the receiver equipment. After software calibration switching from one dynamic range to another will cause only minor errors.

Tx Path

TXIF and TXIFX are differential IF inputs for phase modulated signals (e.g., GMSK). There is an IF level control loop which provides a constant amplitude to an image reject up mixer. Thus, this mixer operates linearly in the IF path, independent of IF level tolerances.

The single sideband up mixer is sufficient in quadrature to achieve the typical performance indicated in Table 6 over an IF range of 250 to 500MHz. The mixer is operating in switching mode by well matched 0° and 90° LO signals, optimized for 1.1 to 1.5GHz.

The Tx output stage operates in switching mode. Thus, parasitic AM at the IF is not transferred. The outputs TXO and TXOX may be used symmetrically or single-ended. Some spurious emissions will be very low when a symmetrical output signal is used.

$$P_{OUT} = R_e \; 6.25V \; (Z_{Pin\,40} \pm Z_{Pin\,41}) \; (I_{R546})^2$$

according to Figure 4 and $I_{R546} \quad \frac{V_{R546}}{R_{546}}$ according to DC Electrical Characteristics. P_{OUT} is adjustable with R546 and is accurate to within ±1dB over the full voltage range 2.7 to 5.5V, and ±0.5dB from a given supply voltage. The absolute limit of the negative peak voltage swing at pins TxO and TxOX is $V_{SAT} = V_{CC}Tx1,2 - 1V$. The absolute limit of the positive peak voltage is +6V.

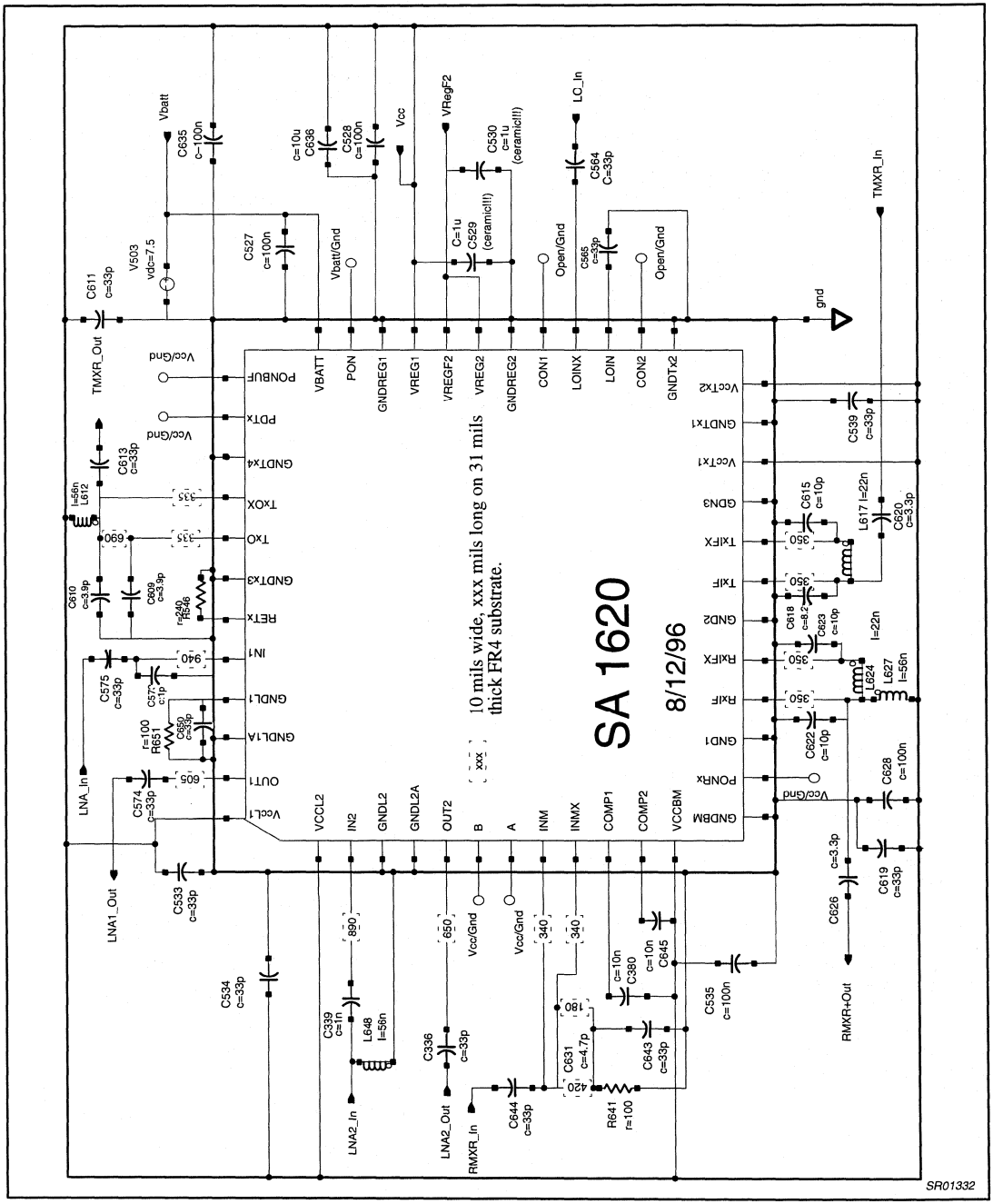


Figure 4. Application Circuit

APPLICATION CIRCUIT

LNA

Impedance Match: Intrinsic return losses at the input and output ports are 7dB and 11dB, respectively. However, since long and narrow traces are always needed to fan out the pins, the user can adjust the traces' dimensions so that only one shunt capacitor at the input is required to achieve excellent impedance match for both ports. If the user wants to skip the input matching network for simplicity, then roughly 0.7dB gain would be lost, although it benefits the system IP3.

Noise Match: The LNA1 and LNA2 can achieve 1.9dB and 2.0dB noise figure, respectively, when S11 = –11dB. Further improvement in S_{11} will slightly decrease NF and increase S_{21}.

Gain Control: The LNA1 can be switched to the attenuation mode, while LNA2 has three attenuation modes to choose from. When gain and loss modes from two LNAs are combined, there will be a total dynamic range of 59dB in the RF block; 3.0V operation is preferred to achieve better IP3 for both LNA1 and LNA2.

Temperature Compensation: Both LNAs have a built–in temperature compensation scheme to reduce the gain drift rate to 0.003dB/°C from –40°C to +85°C.

Supply Voltage Compensation: Unique circuitry provides gain stabilization over wide supply voltage range. The gain changes no more than 0.5dB when V_{CC} increases from 2.7V to 5.5V.

Mixer

Mixer Input Match: The mixer is configured for best gain, noise figure and spurious response. The user must supply an external, patented resonant balun to provide the differential drive as well as the impedance match (embedded in). Because the mixer consists of two single–balance mixers, whose inputs are connected in parallel instead of in series, the differential and common–mode impedances are equal.

Output Match: The mixer output circuit also features an external, patented resonant balun to optimize the conversion gain and noise figure. The principal IF operating frequency is 400 MHz.

LO Drive: The internal buffer only requires –15dBm from an external source. Furthermore, the transmitter incorporates an integrated SSB upconverter that consists of narrowband phase shifters at 1300MHz (LO side) and 400MHz (IF side), so the LO frequency is recommended to be the receiver band plus 400MHz. Additionally, the LO leakage at the input of LNA1 is extremely low, which can greatly alleviate the LO re–radiation problem.

Outband Blocking: For optimum performance, passive R/C network is added at each input of the mixer. The resistors degenerate the noise conversion gain, while the capacitors preserve the gain and noise figure at RF frequencies.

Noise Figure and IP3: The resonant balun is superior to the conventional balun in terms of insertion loss, size and cost. As a result, the user can expect excellent SSB noise figure and gain which is 10dB and 8.5dB, respectively, at 400MHz IF. And the associated input IP3 is 2dBm typically. In the meantime, due to the internal LO buffer, the noise figure and IP3 are not sensitive to the LO levels. As discussed in the LNA Impedance Match session, a better system IP3 can be achieved (if necessary) through LNAs' gain reduction.

Transmitter

The resonant balun is applied again to maximize the gain and output power, for a given bias current. Typical output power is 8.5dBm when the input level exceeds –25dBm.

LO Input

The LO input is used in Tx- and in Rx-mode.

Only one synthesizer PLL is necessary to supply the LO input with different frequencies in Tx and Rx timeslots.

The LO input buffer should only be set in power-down mode together with the PLL. As further buffering is included on chip there will be no influence on the PLL in active mode when the SA1620 Rx- or Tx-path is power On or Off. Current consumption can thus be saved by powering on the Rx- and Tx-circuitry just before it is required, without disruption of the LO circuitry. LO input pins LO IN and LO INX may be used single-ended or symmetrically.

Table 5. GSM/DSC1800 Frequency Specification

(GSM 05.05, Version 4.2.0, April 1992) Mobile Stations Frequency Bands

	GSM	EGSM	DCS1800	Unit
Tx	890 to 915	880.2 to 915	1710 to 1785	MHz
Rx	935 to 960	925.2 to 960	1805 to 1880	MHz

Table 6. Measured Tx Output Frequency and Tx Mixer Products

IF=400MHz, symmetrical load at pins TxO, TxOX.

No.	SPECTRAL LINE f=n*IF+m*LO MHz					RELATIVE POWER OF SPECTRAL LINE			REMARKS
	LO = 1280MHz	LO = 1300MHz	LO = 1315MHz	Order					
				n	m	min dBc	typ dBc	max dBc	
1	80	100	115	–3	1		–70		
2	160	200	230	–6	2		–76		
3	320	300	285	4	–1		–60		
4	400	400	400	1	0		–46		IF
5	480	500	515	–2	1		–31		
6	560	600	630	–5	2		–62		
7	720	700	685	5	–1		–56		
8	800	800	800	2	0		–37		Note 2
9	880	900	915	–1	1		0		Note 1
10	960	1000	1030	–4	2		–46		Note 3
11	1020	1100	1185	6	–1		–63		
12	1200	1200	1200	3	0		–60		
13	1280	1300	1315	0	1		–32		LO
14	1360	1400	1430	–3	2		–46		
15	1440	1500	1545	–6	3		–64		
16	1600	1600	1600	4	0		–75		
17	1680	1700	1715	1	1		–50		Notes 4 and 5
18	1760	1800	1830	–2	2		–34		Note 3
19	1840	1900	1945	–5	3		–68		Note 3
20	2000	2000	2000	5	0		–77		
21	2080	2100	2115	2	1		–74		
22	2160	2200	2230	–1	2		–67		
23	2240	2300	2345	–4	3		–59		
24	2400	2400	2400	6	0		–75		
25	2480	2500	2515	3	1		–76		
26	2560	2600	2630	0	2		–70		2LO

NOTES:
1. Desired Tx output frequency LO–IF corresponding to EGSM Tx band in Table 5.
2. (LO+IF)–(LO–IF) = 2 * IF
3. See Rx bands in Table 5.
4. LO+IF = mixer image frequency
5. See Tx bands in Table 5.

Table 7. Measured Tx Output Noise Floor

Frequency MHz		dBc/Hz			REMARKS
		MIN	TYP	MAX	
< 860			–135		
860 to 880			–134		
880.2 to 890			–133		EGSM TX extension
890 to 915			–133		GSM TX
915 to 925			–133		
925.2 to 935			–134		EGSM RX extension
935 to 960			–135		GSM RX
960 to 1000			–135		
1000 to 1710			–135		
1710 to 1785			–146		DCS1800 TX
1785 to 1805			–145		
1805 to 1880			–144		DCS1800 RX
1880 to 12750			–147		
Adjacent Channel			–130		

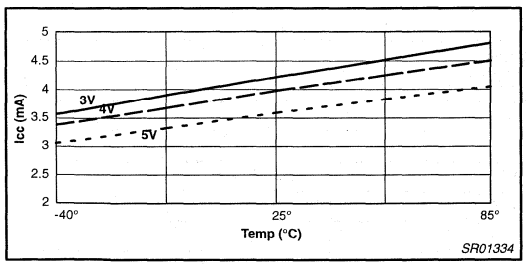


Figure 5. LNA1_ICC vs. Temp

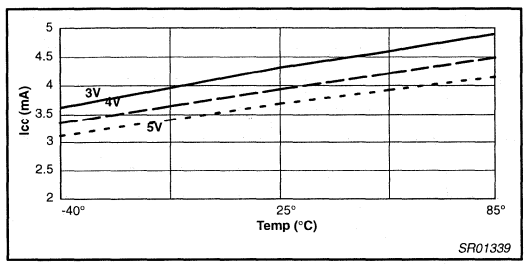


Figure 6. LNA_2 ICC vs. Temp

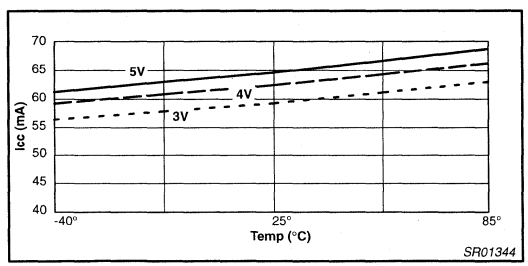


Figure 7. Transmit_ICC vs. Temp

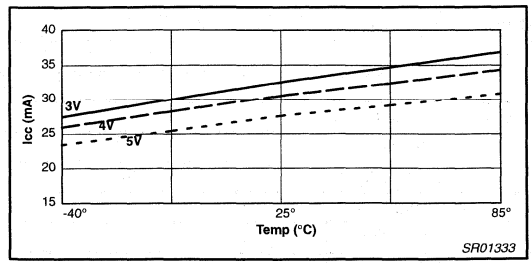


Figure 8. Receive ICC vs. Temp

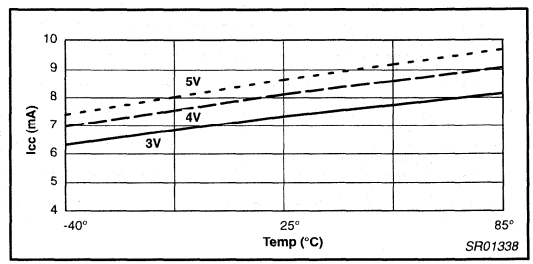


Figure 9. Standby_ICC vs. Temp

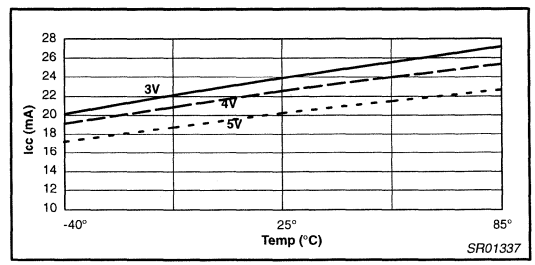


Figure 10. Calibrate_ICC vs. Temp

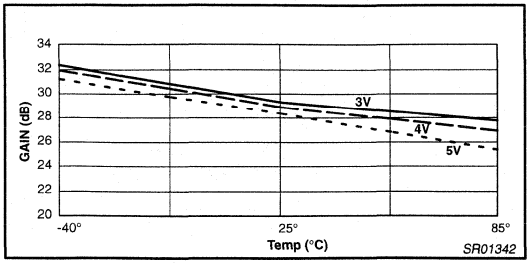


Figure 11. Receive_Gain Mode1 vs. Temp

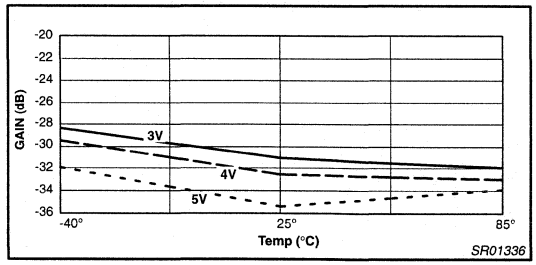


Figure 14. Receive_Gain_Mode4 vs. Temp

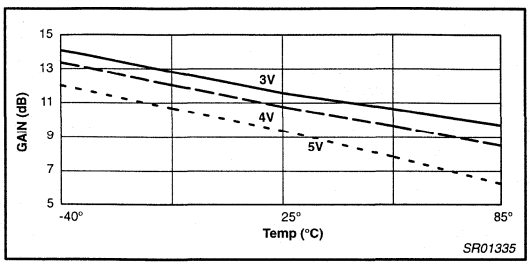


Figure 12. Receive_Gain_Mode2 vs. Temp

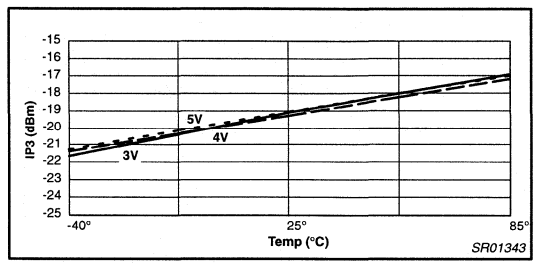


Figure 15. Receive IIP3 vs. Temp

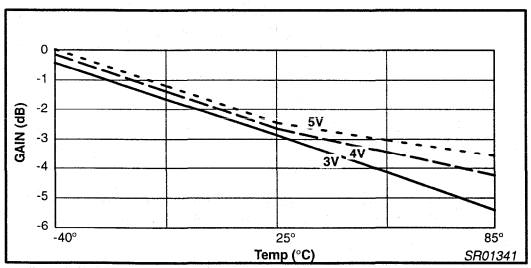


Figure 13. Receive_Gain_Mode3 vs. Temp

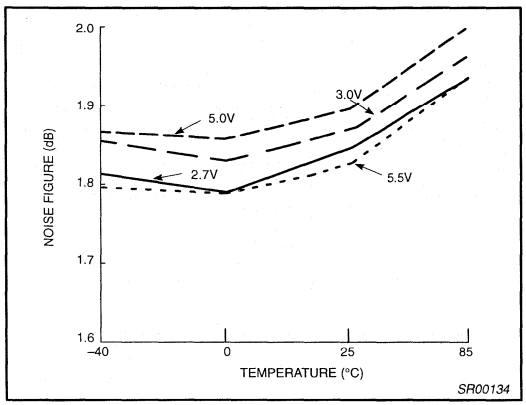


Figure 16. Receive LNA1 Noise Figure

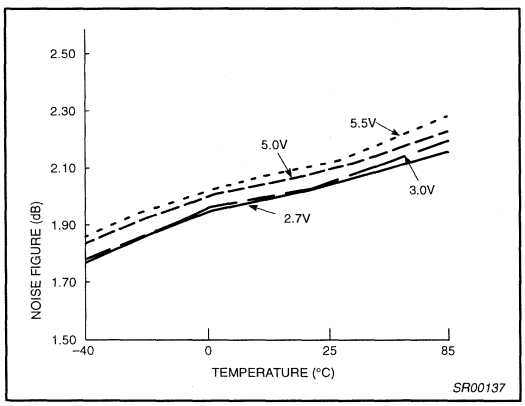


Figure 17. Receive LNA2 Noise Figure

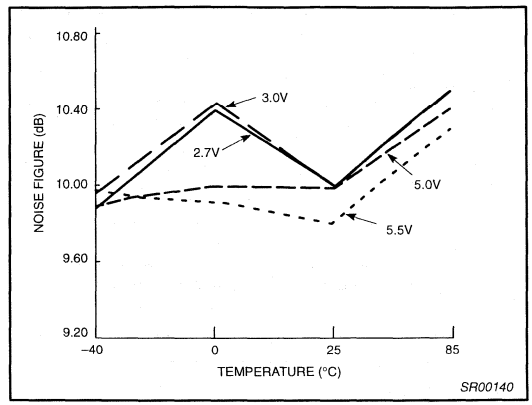


Figure 18. Receive Mixer Noise Figure

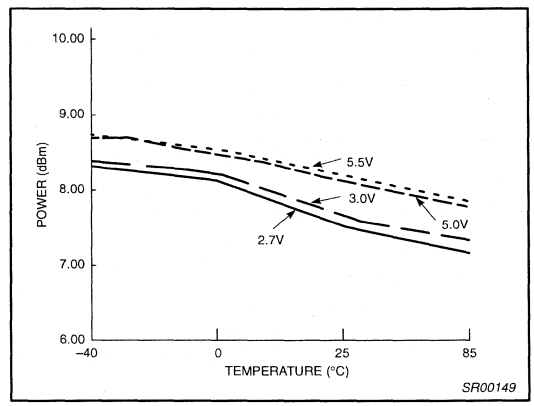


Figure 19. Transmit Power @ -25dBm

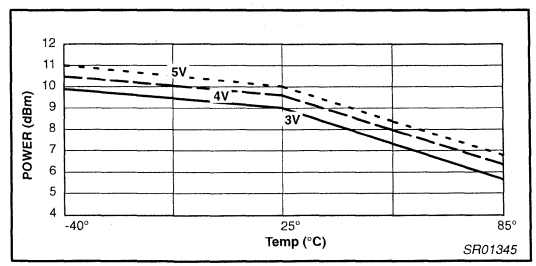


Figure 20. Transmit_Power @ –20 dBm Input

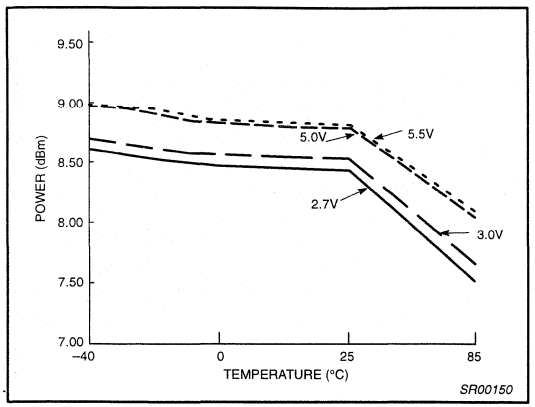


Figure 21. Transmit Power @ -15dBm

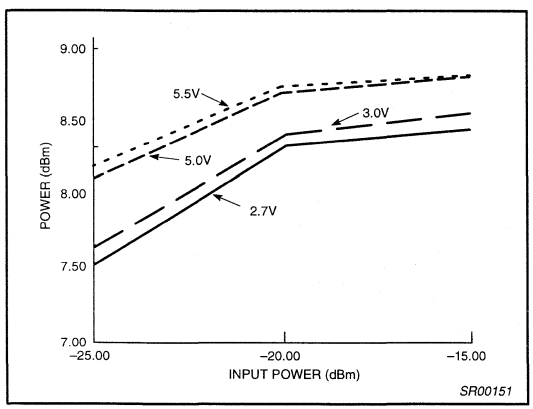


Figure 22. Transmit Power @ 25°C

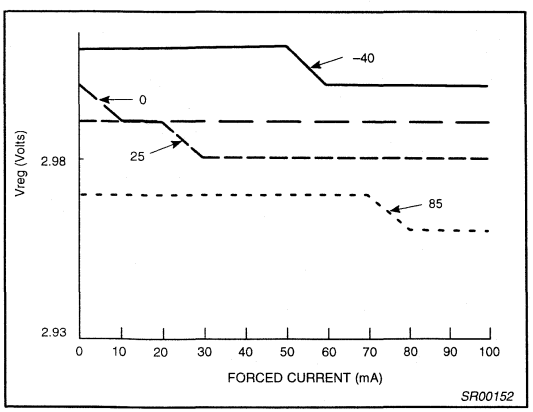


Figure 23. Regulator 1 Load Regulation (V_{BATT} = 3.5V)

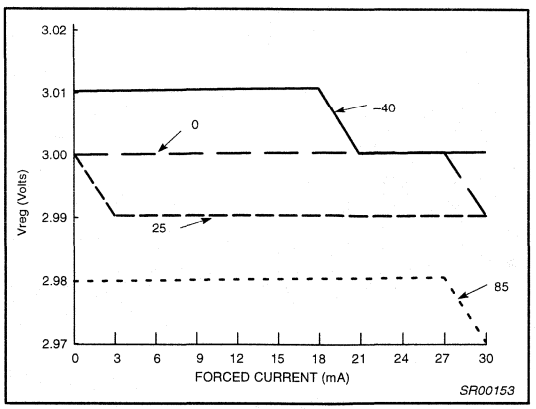


Figure 24. Regulator 2 Load Regulation (V_{BATT} = 3.5V)

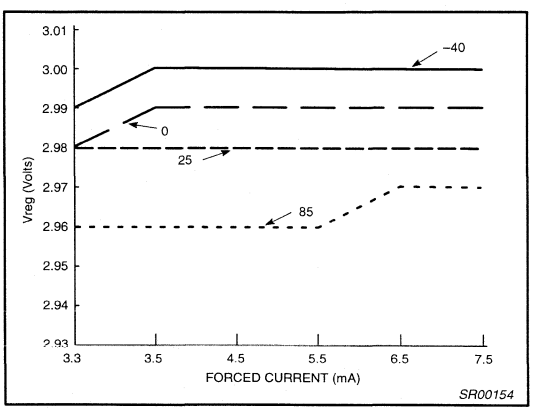


Figure 25. Regulator 1 Line Regulation @ 100mA Load

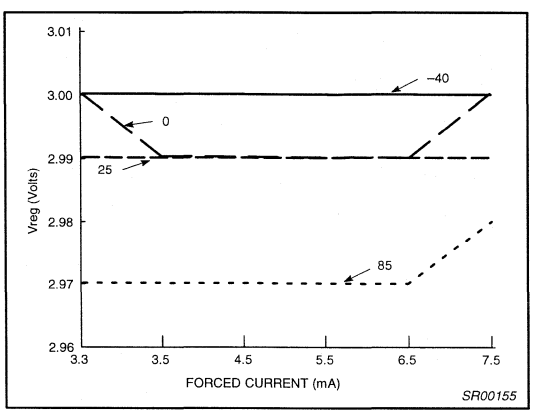


Figure 26. Regulator 2 Line Regulation @ 30mA Load

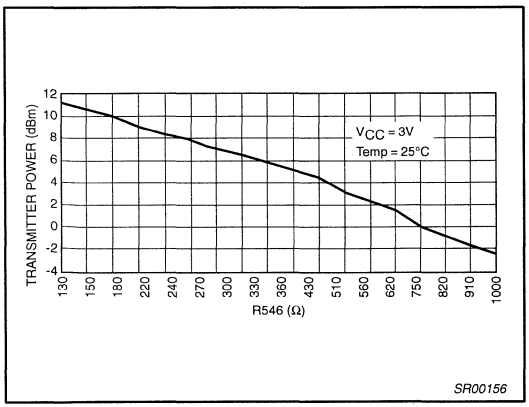


Figure 27. Transmit Output Power vs R(546) @ V_{CC} = 3V

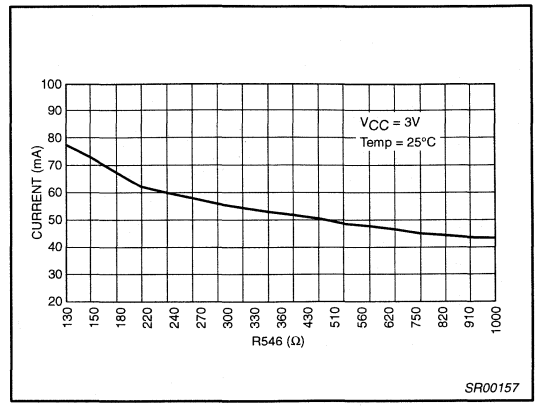
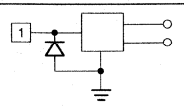
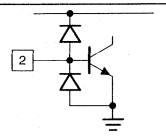
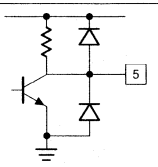
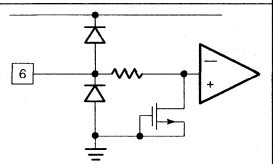
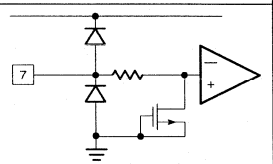
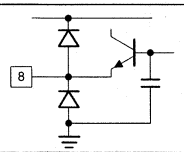
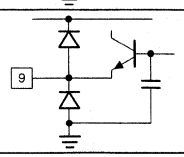
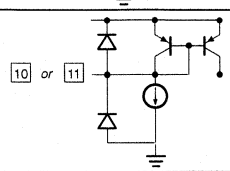


Figure 28. Transmit Mode Current vs R(546) @ V_{CC} = 3V

PIN FUNCTIONS

PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
1	V_{CC}	3.0	
2	IN2	0.8	
3	GNDL2	0.0	
4	GNDL2a	0.0	
5	OUT2	2.2	
6	B CMOS INPUT		
7	A CMOS INPUT		
8	INM	0.4	
9	INMX	0.4	
10	COMP2	2.2	
11	COMP1	2.2	

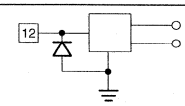
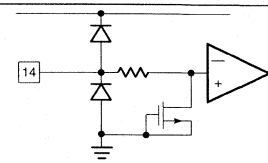
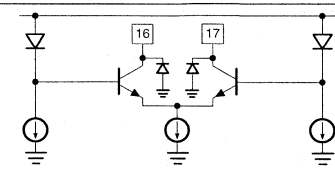
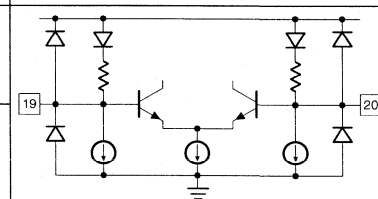
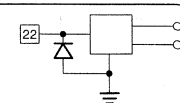
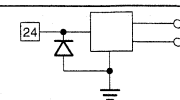
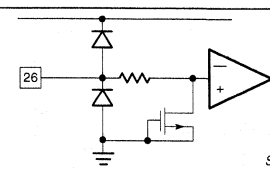
PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
12	V_{CC}BM	3.0	
13	GND	0.0	
14	POnRx CMOS INPUT		
15	GND	0.0	
16	Rxif	3.0	
17	RxifX	3.0	
18	GND	0.0	
19	Txif	2.2	
20	TxifX	2.2	
21	GND	0.0	
22	V_{CC}Tx	3.0	
23	GND	0.0	
24	V_{CC}Tx	3.0	
25	GND	0.0	
26	CON2 CMOS INPUT		

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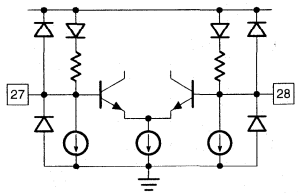
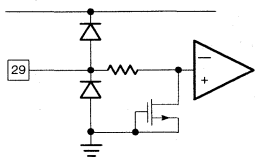
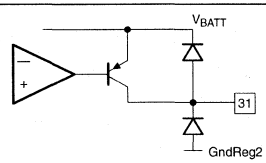
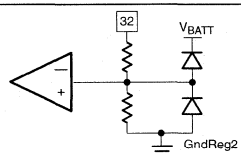
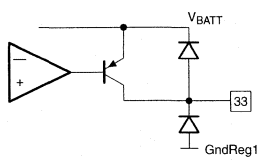
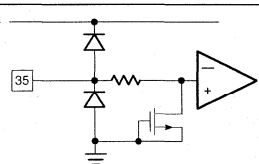
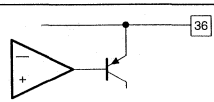
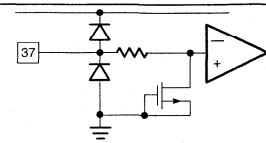
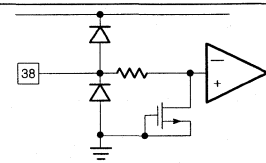
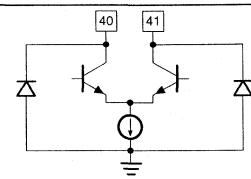
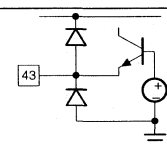
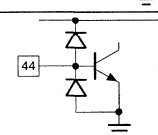
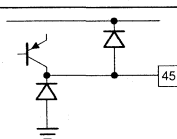
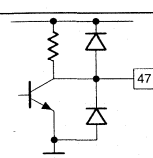
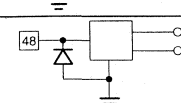
Figure 29. Pin Functions

PIN FUNCTIONS (continued)

PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
27	LOin	2.2	
28	LOinX	2.2	
29	CON1 CMOS INPUT		
30	GndReg1	0.0	
31	VReg2	3.0	
32	VRegF2	3.0	
33	VReg1	3.0	
34	GndReg1	0.0	
35	POn CMOS INPUT		
36	V_{BATT}	3.0	

PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
37	POnBuf CMOS INPUT		
38	PDTx CMOS INPUT		
39	GndTx	0.0	
40	TxOx	3.0	
41	TxO	3.0	
42	GndTx	0.0	
43	RETx	0.4	
44	IN1	0.8	
45	GndL1	0.0	
46	GndTx	0.0	
47	OUT1	2.2	
48	$V_{CC}L1$	3.0	

SR00163

Figure 29. Pin Functions (continued)

IF quadrature transceiver SA1630

DESCRIPTION

The SA1630 is a 70–400 MHz I/Q transceiver for wireless LAN. The Receive Path contains a digitally gain controlled linear IF amplifier, a pair of quadrature down conversion mixers and a pair of baseband amplifiers. The transmit path contains a pair of quadrature up conversion mixers that transposes a quadrature baseband input signal up to IF frequency. An external VCO signal is divided internally and provides quadrature local oscillator signals for the mixers. Another divider chain, reference divider and phase detector are provided to avoid the need for an external synthesizer. To keep power consumption to a minimum the transmit, receive and local oscillator functions can be powered down under digital control.

FEATURES

- Low supply voltage operation of 2.7V for main chip and 2.9V for charge pump.
- Low current consumption: 33.5 mA in RX, 26.5 mA in TX, typical at 3V.
- Flexible power up/down options.
- Optional 2.5V regulated reference voltage available during transmit.
- Input IF frequency range of 70–400 MHz.
- Internal IF PLL for synthesizing the local IF oscillator signal.
- Bandwidth of baseband Tx inputs is 20 MHz and that of baseband Rx outputs is 8.5MHz.
- Designed for IEEE 802.11 wireless LAN using Direct Sequence Spread Spectrum modulation.
- Control registers power up in a default state.
- Only a standard reference input frequency required, choice of 8, 11, 22 or 44 MHz.
- Digital gain control of 70 dB in steps of 2 dB.
- Rx Baseband amplifiers are capable of driving 1kΩ ||15pF
- Rx Baseband o/p's clamp symmetrically, above 1Vp–p in order to prevent dc bias shift under overdrive conditions.
- Package: LQFP–48, PCMCIA compatible

APPLICATIONS

- IF circuitry for IEEE 802.11 DSSS wireless LAN.
- Applications for high speed wireless data.

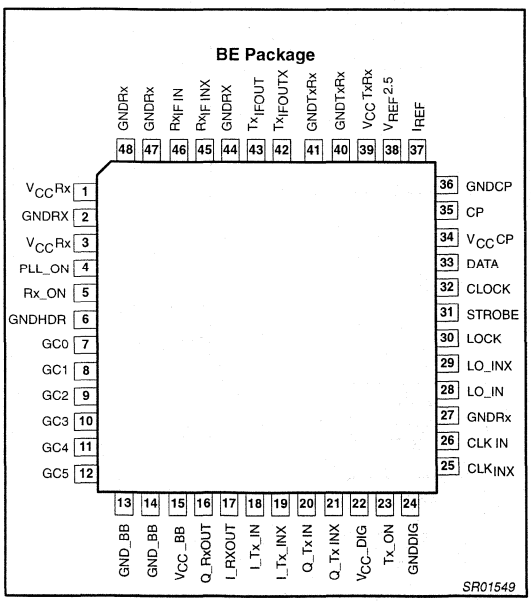


Figure 1. Pin Configuration

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
48–Pin Plastic Low Profile Quad Flat package	–40 to +85°C	SA1630BE	SOT313–2

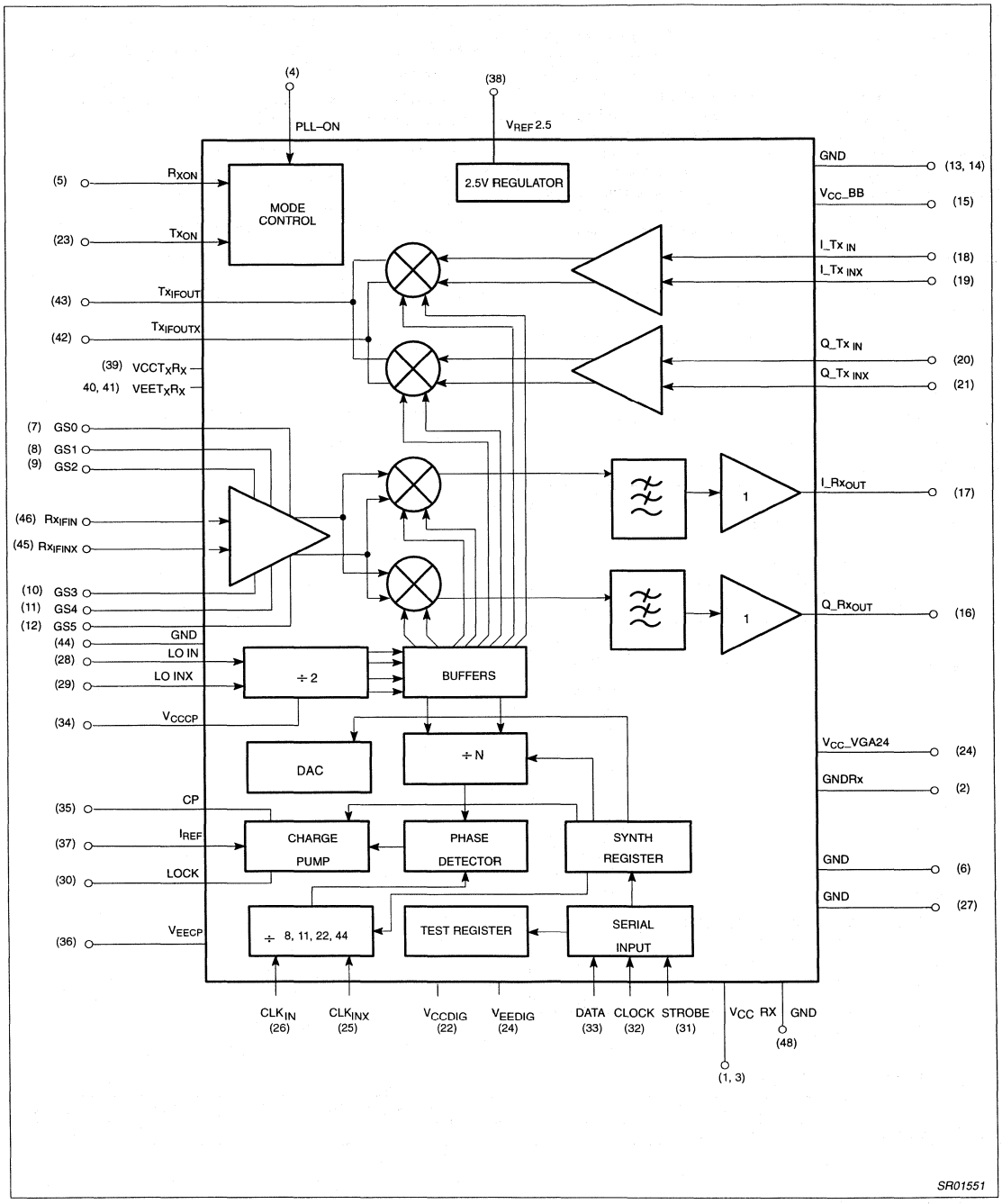


Figure 2. Block Diagram

PIN DESCRIPTIONS

Pin No.	Pin Name	Description
1, 3	V_{CC}Rx	Supply Pin for Rx section (IF circuits)
2, 27, 44,47, 48	GNDRx	Ground pins for Rx section (IF circuits)
4	PLL_ON	One of the three digital CMOS logic control inputs to the mode control section
5	Rx_ON	One of the three digital CMOS logic control inputs to the mode control section
6	GNDHDR	Substrate ground
7	GCO	Control bit 0 for IF VGA gain control, CMOS input
8	GC1	Control bit 1 for IF VGA gain control, CMOS input
9	GC2	Control bit 2 for IF VGA gain control, CMOS input
10	GC3	Control bit 3 for IF VGA gain control, CMOS input
11	GC4	Control bit 4 for IF VGA gain control, CMOS input
12	GC5	Control bit 5 for IF VGA gain control, CMOS input
13, 14	GND_BB	Ground pin for Rx baseband circuits
15	GND_BB	Supply Pin for Rx Baseband circuits
16	Q_RXOUT	Quadrature–phase Rx baseband output, single–ended
17	I_RxOUT	In–phase Rx baseband output, single–ended
18	I_Tx IN	In–phase differential Tx baseband input, positive
19	I_Tx INX	In–phase differential Tx baseband input, negative
20	Q_Tx IN	Quadrature differential Tx baseband input, positive
21	Q_Tx INX	Quadrature differential Tx baseband input, negative
22	V_{CC}_DIG	Supply for digital circuits
23	Tx_ON	One of the Three digital CMOS logic control inputs to the mode control section
24	GNDDIG	Digital ground
25	CLK INX	Differential reference input for synthesizer, negative
26	CLK IN	Differential reference input for synthesizer, positive
28	LO_IN	Differential LO input,positive
29	LO INX	Differential LO input, negative
30	LOCK	Test control output and synthesizer lock indicator
31	STROBE	Serial bus strobe input
32	CLOCK	Serial bus clock input
33	DATA	Serial bus data input
34	V_{CC}CP	Supply for charge pump circuits
35	CP	Charge pump output
36	GNDCP	Ground for charge pump circuits
37	I_{REF}	Ground for charge pump circuits
38	V_{REF}2.5	Reference voltage of 2.5V available for external use
39	V_{CC}TxRx	Supply pin used by Tx circuits
40,41	GNDTxRx	Ground pins used by Tx circuits
42	TxIFOUTX	Differential transmitter IF output (open collector), positive
43	TxIFOUT	Differential transmitter IF output (open collector), negative
45	RxIF INX	Differential receiver IF input, negative
46	RxIF IN	Differential receiver IF input, positive

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CCXX}	Supply voltages	-0.3 to +6.0	V
V_{IN}	Voltage applied to any other pin	-0.3 to V_{CCXX}+0.3	V
ΔVG	Any GND pin to any other GND pin	0	V
P_D	Power dissipation, T_A = 25°C (still air)	300	mW
T_{JMAX}	Maximum operating junction temperature	150	°C
P_{MAX}	Maximum power input/output	+20	dBm
T_{STG}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CCXXXX}	Supply voltages:	2.7 to 3.6	V
V_{CC}CP	Charge pump supply voltage	2.9 to 3.6	V
T_A	Operating ambient temperature range	-40 to +85	°C

MODE CONTROL

NO:	PLL_ON	RX_ON	TX_ON	STATE DESCRIPTION	MODE	2.5V REF
1	0	X	X	SLEEP mode	SLEEP	Off
2	1	0	1	Synthesizer ON, Rx STDBY, Tx OFF	WAIT	Off
3	1	1	1	Synthesizer ON, Rx STDBY, Tx ON	TRANSMIT	On
4	1	1	0	Synthesizer ON, Rx ON, Tx OFF	RECEIVE	Off
5	1	0	0	Synthesizer ON, Rx OFF, Tx ON	TRANSMIT	Off

'0' – LOGIC LOW
'1' – LOGIC HIGH
'X' – DON'T CARE

1. Sleep mode (PLL OFF, Rx OFF, Tx OFF)

In this mode everything is switched off except the 3–wire digital bus. As long as the digital supply is still on, the programmed values are active and the 3–wire bus will continue to be programmable.

2. Wait Mode (Tx Off, Rx Standby)

PLL is on. Receiver is in the reduced current standby mode and the transmitter is completely switched off. This mode maybe useful if the PLL is to be kept on and is waiting for a quick turn–on to either transmit or receive modes, especially when Rx outputs are AC coupled.

3. Transmit mode (Rx standby)

The PLL and transmitter are on. The receive section is in a reduced current mode wherein most of the Rx circuitry is powered down except for the bias and baseband circuits needed to hold the baseband output voltages in the active state. This mode is useful if the Rx baseband outputs are AC coupled via a large capacitor and the application demands quick turn–on for the Rx, from Tx.

4. Receive Mode (Tx Off)

The Transmitter is completely shut–off. The PLL and receiver sections are operating.

5. Transmit Mode (Rx OFF)

PLL and Transmit sections are on. However, the Receiver is completely shut–down. This mode is useful if the Rx baseband outputs are DC coupled to the external world.

RX VGA CONTROL TABLE

GC5	GC4	GC3	GC2	GC1	GC0	DECIMAL NUMBER	REDUCTION FROM Gmax
0	0	0	0	0	0	0	0
0	0	0	0	0	1	1	–2
0	0	0	0	1	0	2	–4
0	0	0	0	1	1	3	–6
0	0	0	1	0	0	4	–8
0	0	0	1	0	1	5	–10
0	0	0	1	1	0	6	–12
0	0	0	1	1	1	7	–14
0	0	1	0	0	0	8	–16
0	0	1	0	0	1	9	–18
0	0	1	0	1	0	10	–20
0	0	1	0	1	1	11	–22
0	0	1	1	0	0	12	–24
0	0	1	1	0	1	13	–26
0	0	1	1	1	0	14	–28
0	0	1	1	1	1	15	–30
0	1	0	1	1	1	23	–32
0	1	1	0	0	0	24	–34
0	1	1	0	0	1	25	–36
0	1	1	0	1	0	26	–38
0	1	1	0	1	1	27	–40
0	1	1	1	0	0	28	–42
0	1	1	1	0	1	29	–44
0	1	1	1	1	0	30	–46
0	1	1	1	1	1	31	–48
1	1	0	1	0	0	52	–50
1	1	0	1	0	1	53	–52
1	1	0	1	1	0	54	–54
1	1	0	1	1	1	55	–56
1	1	1	0	0	0	56	–58
1	1	1	0	0	1	57	–60
1	1	1	0	1	0	58	–62
1	1	1	0	1	1	59	–64
1	1	1	1	0	0	60	–66
1	1	1	1	0	1	61	–68
1	1	1	1	1	0	62	–70

DC ELECTRICAL CHARACTERISTICS

$V_{CC}XXX$=+3V; $V_{EE}XXX$ = 0V; TA=25°C, unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNITS
			MIN	**TYP**	MAX	
I_{CC-4}	Supply Current, Receive (mode #4)	PLL_ON=Rx_ON=Hi Tx_ON = Low		33.5	tbd	mA
I_{CC-2}	Supply Current, Wait (mode #2)	Wait mode (2) PLL_ON = Hi Tx_ON = Hi Rx_ON = Low		17	tbd	mA
I_{CC-3}	Supply Current, Transmit (mode #3)	PLL_ON = TX_ON = Hi RX_ON = Hi		26.5	tbd	mA
I_{CC-1}	Supply Current, Sleep mode (mode #1)	PLL_ON = Low RX_ON = DC TX_ON = DC		.068	tbd	mA
V_{REF}_2.5	Reference voltage (mode 3, enabled)	Load = 1.5mA		2.5		V
Z_{OUT}_V_{REF}	Output impedance of reference voltage	ΔI tbd		tbd		Ω
CMOS LOGIC INPUTS (DATA, CLOCK, STROBE)						
V_{IH}	Input logic 1 level		2.0		V_{CCD}	V
V_{IL}	Input logic 0 level		0		0.8	V
I_I	Input logic current				1	µA
C_I	Input logic capacitance				4	pF
CMOS Logic output (LOCK)						
V_{OH}	Output logic 1 level	I_O = –2mA	V_{CCD}–0.4			V
V_{OL}	Output logic 0 level	I_O = 2mA			0.4	V
CMOS Logic Inputs (PLL_ON, RX_ON, TX_ON)						
V_{IH}	Input logic 1 level		2.0		V_{CCTXRX}	V
V_{IL}	Input logic 0 level		0		0.8	V
I_I	Input logic current				1	µA

AC ELECTRICAL CHARACTERISTICS IF TRANSMIT MODULATOR

(Mode #3, Tx ON Rx Standby) $V_{CC}XXX$ = +3V; GNDXXX = 0V; LO_in = 100 mV peak at 704 MHz, CLKin = 100mV peak at 22 MHz, T_{amb} = 25°C, unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNITS
			MIN	**TYP**	MAX	
BW[4,5]	Input modulation bandwidth	500 ohms source impedance	22			MHz
V_{IN}	Input signal amplitude, Differential[1]	Vcm range		1		Vpp
THD	Total harmonic distortion[1]	Input signal amplitude[1] = 1 V_{PP}, 11 MHz		tbd		dBc
R_{INTx}	Input resistance	Between pins I_T_XIN, I_T_XINX Q_T_XIN, Q_T_XINX		98		kΩ
C_{INTx}	Input Capacitance	Between pins I_T_XIN, I_T_XINX Q_T_XIN, Q_T_XINX			2	pF
	Output saturation limit	ITxIn = ITxinX = QTxin = QTxinX = $V_{CC}/2$	V_{CC}–0.3			V
	Mean output current	At T_XIF_{OUT} and T_XIF_{OUTX}		2		mA
	Output current DC offset	Mismatch at T_XIF_{OUT} and T_XIF_{OUTX}			20	µA
	Output Current[1,2]	At T_XIF_{OUT} and T_XIF_{OUTX}		0.475		mA rms
	Output differential voltage[1,2]	400 Ω tuned load[2]		190		mV rms
f_{LO-IF}	LO feedthrough[1,3]	Differential output		tbd	–30	dBc
	SSB Suppression [1,3]	f_{OUT} = 352 MHz	35	tbd		dBc
	Spot Noise[4] (Output Spectrum)	offset F1 (tbd) offset (tbd)		tbd tbd		dBc/Hz
∠G[4]	Gain stability				2.0	dB
t_{ON}[4]	Turn–on time	T_X_ON, R_X_ON transition to transmit signal at 90% level			2	µs
T_{OFF}[4]	Turn–off time	T_X_ON, R_X_ON transition to transmit signal at 10% level			2	µs

NOTES:

1. I_TxIN = 0.25 Sin wmt, I_TxINX = 0.25 Sin wmt, Q_TxIN = 0.25 Sin (wmt–90), Q_TxINX = 0.25 Sin (wmt–90). The output spectrum will be a SSB one. The tone is at a frequency of 1 MHz.
2. The output current in each arm is the same but 180 degrees out of phase with each other. Also the tuned load of 400 ohms differential, is assumed. The power delivered to 400 ohms will be –10.4 dBm (typ.). The output current measurement is indirect based on output power measurement.
3. This is measured with respect to the SSB output.
4. Guaranteed by design and or characterization but not final tested.
5. The input bandwidth will be tested by measuring the output THD and signal level using a DSB spectrum where I = Q and the signal is a tone at 22 MHz.

AC ELECTRICAL CHARACTERISTICS IF RECEIVER DEMODULATOR

(Mode #4, Rx_ON, Tx_OFF) $V_{CC}XXX$ = +3V = GNDXXX = 0V; LO IN = 100 mV_{peak} at 704 MHz, CLKIN = 100mV_{peak}, at 22 MHz, Ta = 25°C, unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNITS
			MIN	**TYP**	MAX	
RInRx	Differential input impedance	f_{IN} = 400 MHz		tbd		kΩ
VG	Voltage gain	AGC at maximum gain	tbd	83		dB
NF[1]	Input noise figure[6]	VGA at maximum gain		7.5		dB
	AGC range			70		dB
	AGC step size			2		dB
	AGC differential error				1	dB
	AGC settling time	any AGC step			200	nS
	Channel matching gain phase			0.2 1.0		dB deg
	Output voltage swing	V_{CC} = 3V, into Load[8]	1			Vpp
	Output common mode voltage			1.9		V
	Output impedance			7		Ω
THD[9]	Total Harmonic Distortion	Max. Gain, rated output at 1 MHz		3		%
BW	Rx Bandwidth	3dB dropin gain	7	8.5	10	MHz
t_{ON}[4]	Turn–on time	R_X_ON, T_X_ON transition to baseband signal out			2	µs
t_{OFF}[4]	Turn–off time	R_X_ON, T_X_ON transition to no baseband signal out			2	µs

NOTES:

1. The Receive input is to be differential (using a balun or a differential source such as a differential SAW filter) and matched to external generator's impedance (ex: 50 ohms). The balun may or may not provide any impedance transformation depending on availability. An external L–C matching circuit can provide the rest of the impedance transformation as well absorb the input capacitance of the receiver input. Such a differential input scheme is mandatory to avoid pickup, and keep the noise figure low. A shunt resistor across the input (value TBD) will be used to set the input impedance as a compromise between the matching ease in production versus the noise figure of the receiver.
2. The system board layout has to keep the isolation between the receive inputs and the LO signal as high as possible. Otherwise the LO leakage will overload the receiver.
3. The load is 1000 ohms in parallel with 15pF of capacitor.
4. THD is total harmonic distortion. Since 3rd harmonic will dominate we will just measure this one.

AC ELECTRICAL CHARACTERISTICS IF SYNTHESIZER

$V_{CC}XXX$ = RX_ON = TX_ON = PLL_ON = +3V TO +5V, $V_{EE}XXX$ = 0V; LO_IN = 100 mV_{peak} at 704 MHz, CLKIN = 100mV_{peak} at 22 MHz, Ta = 25°C, unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNITS
			MIN	**TYP**	MAX.	
f_{LO}	Local oscillator input frequency range		140		800	MHz
Z_{LOIN}	Differential input impedance	Between LO_IN and LO_INX		276 0.6		Ω pF
	LO input sensitivity	Single ended Referred to 50Ω	tbd		tbd	mVpp
	Programmable divider: division range step size		64	 1	511	
f_{CLK}	Reference clock frequency			8, 11, 22 or 44		MHz
Z_{CLKIN}	Differential input impedance	Between Clk_{IN} and Clk_{INX}		10 1.0		kΩ pF
	CLK input sensitivity	Referred to 50Ω	50	200	400	mVpk
f_C	Phase detector comparison frequency			1		MHz
I_{REF}	Charge pump reference current			31.25		µA
$\|I_{CP}\|$	Charge pump output current: C0...C2 = 000 C0...C2 = 111 step size	I_{REF} = 31.25 µA $V_{CP} = V_{CC}CP/2$		0.200 0.400 0.029		mA mA mA
$\frac{\angle I_{CP}}{I_{CP}}$	Relative output current variation[1]	I_{REF} = 31.25 µA		1.3	±10	%
$\angle I_{CP\_M}$	Output current matching[2]	I_{REF} = 31.25 µA $V_{CP} = V_{CC}CP/2$			±12	%
	Output current tolerance with programmed step with temperature with output voltage	CP between 0.8 V and V_{CC} CP = 0.8V		±10 ±10 ±5		%
Serial Interface[4]						
f_{CLOCK}	Clock frequency				10^5	MHz
t_{SU}	Set–up time; DATA to clock, CLOCK to STROBE		30			ns
t_H	Hold time: CLOCK to DATA		30			ns
t_W	Pulse width: CLOCK		30			ns
	Pulse width: STROBE		30			ns

NOTES:

1. The relative output current variation is defined thus: $\frac{\Delta I_{OUT}}{I_{OUT}} = 2 \cdot \frac{(I_2 - I_1)}{I(I_2 + 1_1)}$; WITH V_1 = 0.3V, V_2 = $V_{CC}CP$ – 0.3V (see Figure 3).
2. The output current matching is measured when both (positive current and negative current) sections of the output charge pumps are on
3. As soon as $P_{ON}PLL$ is set to LO, the phase detector is reset and no charge pumps pulses are generated.
4. Guaranteed by design.
5. Minimum frequency is guaranteed by design.

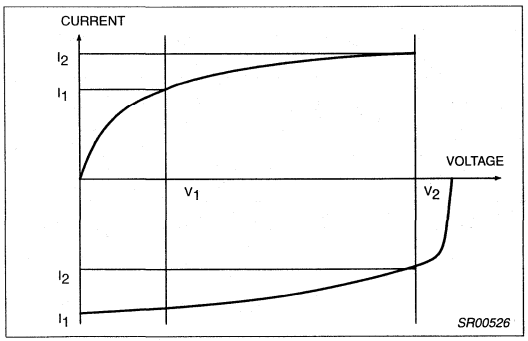


Figure 3. Relative Output Current Variation

APPLICATION DESCRIPTION

General

The 1630 performs the IF modulator and demodulator functionality for high–speed wireless data transceivers. The design is optimized for IEEE 802.11 wireless LAN using 11 chips/symbol Direct Sequence Spread Spectrum.

Transmitter

The IF quadrature transmitter baseband modulator input is driven differentially by the D/A converters in the DSP chip. The baseband signals are DC coupled for fast turn–on and turn–off and for constant carrier testing. The typical common–mode input voltage is VCC/2.

The open collector outputs of the mixers are biased by two choke coils, which are part of an LC tank. The LC tank matches the output impedance of the mixers to the input impedance of the upconverter chip (or any filter in between) and suppresses IF harmonics.

An optional 2.5V reference is available during mode (3), the transmit mode with Rx in standby. This reference can be enabled or disabled via the 3 wire bus (in this mode). This voltage is provided for use by an external current DAC if needed.

Receiver

The receiver part of the SA1630 consists of an IF Variable gain amplifier, a quadrature demodulator and a pair of baseband amplifiers. The IF amplifier has its gain controlled by the DSP chip. This ensures linear operation of the receiver chain over a wide dynamic range of input signals. Linear operation is essential for resolving echo's due to multipath reception.

The digital controlled AGC is meant for fast level training for the receiver.

The high gain receiver, which is distributed between the IF and baseband part facilitates interfacing with the RF front–end chip, which normally have moderate gains (up to 20 dB), and SAW IF filters, which mostly have considerable loss (up to 8 dB) without external amplifiers.

The baseband amplifiers have a high drive capability (1 Vpp into 1kΩ, 15 pF for VCC = 3V) that facilitates direct interfacing to the A/D converter without active external elements.

The baseband amplifiers can interface directly to the Track/Hold switch/capacitor combination with capacitance values up to 15 pF. When sampled at 22MHz the output can settle to within 1/4 LSB when swinging 1V p–p.

The chip has a unique mode in which the Rx is on standby while the Tx is ON. In this mode the Rx Baseband circuits are idling at reduced currents and all Rx I/O outputs retain their DC bias unchanged from their values when the Rx was fully ON. This mode is very essential if ac coupling through a large capacitor, such as, 10nF is used. From this mode the chip can quickly be switched to the Rx ON mode (Tx OFF) without worrying about charging/discharging the large AC coupling capacitor.

The VGA can be programmed in 2 ways: 1) Directly programming external control bins. 2) programming over the serial 3–wire bus. The former method can switch gain in less than 200 ns.

The Rx baseband section also incorporates simple low pass active filters of the Sallen key type. The Rx bandwidth is mainly set by these filters. The function of these filters is twofold: 1) attenuate high frequency signals from the Rx mixers. 2) act as anti–aliasing filters for any A to D converters following this chip.

IF synthesizer

The SA1630 has an integrated synthesizer that uses an external VCO operating on twice the IF frequency. It is internally divided by 2 for obtaining quadrature signals. The divided VCO signal is not externally available. This minimizes the LO feedthrough to the IF input port and hence minimizes output dc glitches when the IF gain is switched.

The PLL reference clock is derived from the 22 MHz DSP clock. The available divider ratios facilitate both 1 and 2 MHz phase comparison frequency from a 22 MHz and an optional 44 MHz clock respectively. In essence the reference divider will have programmable dividers ratios of 8, 11, 22 and 44.

The VCO shall be fed from a stabilized supply. Such a stabilized supply is necessary in order to prevent oscillator jitters due to Rx/Tx switching. The effect of oscillator jitters is further minimized when using a high PLL loop bandwidth, which on its turn requires a high phase comparison frequency (1 MHz, preferably 2 MHz).

Serial Programming Input

The serial input is a 3–wire input (CLOCK, STROBE, DATA) to program the counter ratios, charge pump current, status– and DC–offset register, mode select and test register. The programming data is structured into two 21–bit words; each word includes 4 chip address bits and 1 subaddress bit. Figure 2 shows the timing diagram of the serial input. When the STROBE = L, the clock driver is enabled and on the positive edges of the CLOCK the signal on DATA input is clocked into a shift register. When the STROBE = H, the clock is disabled and the data in the shift register remains stable. Depending on the value of the subaddress bit the data is latched into different working registers. Table 3 shows the contents of each word.

Default States

Upon power up (V_{CC}DIG is applied) a reset signal is generated, which sets all registers to a default state. The logic level at the STROBE pin should be low during power up to guarantee a proper reset. These default states are shown in Table

Reference Divider

The reference divider can be programmed to four different division ratios (:8, :11, :22, :44), see registers r0, r1; default setting: divide by 22.

Main Divider

The external VCO signal, applied to the LO_{IN} and $LO_{IN}X$ inputs, is divided by two and then fed to the main divider (:N). The main divider is a programmable 9 bit divider, the minimum division ratio is divide by 64. The division ratio is binary coded and set in the registers n0 to n8. The default setting is a divide by 352.

At the completion of a main divider cycle, a main divider output is generated which will drive the phase detector.

Phase Detector

The phase detector is a D-type flip-flop phase and frequency detector shown in Figure NO TAG. The flip-flops are set by the negative edges of the output signals of the dividers. The rising edge of the signal L will reset the flip-flops after both flip-flops have been set. Around zero phase error this has the effect of delaying the reset for 1 reference input cycle. This avoids non-linearity or deadband around zero phase error. The flip-flops drive on-chip charge pumps. A source current from the charge pump acts to increase the VCO frequency; a sink current acts to decrease the VCO frequency.

Current Setting

The charge pump current is defined by the current set between the pin I_{REF} and V_{EE}CP. The current value to be set there is 31.2µA. This current can be set by an external resistor to be connected between the pin I_{REF} and V_{EE}CP. The typical value R_{EXT} (current setting resistor) can be calculated with the formula

$$R_{EXT} = \frac{V_{CC}CP - 1.6V}{31.2\mu A} \quad (44.87K \text{ for } 3V)$$

The current can be set to zero by connecting the pin I_{REF} to V_{CC}CP.

Charge Pumps

The charge pumps at pin CP are driven by the phase detector and the current value is determined by the binary value of the charge pumps register CN = c2, c1, c0, default .4mA. The active charge pump current is typically:

$$|I_{CP}| = (c0 + 2c1 + 4c2) \cdot 29\mu A + 200\mu A$$

Lock Detect

The output LOCK is H when the phase detector indicates a lock condition. This condition is defined as a phase difference of less than ±1 cycle on the reference input CLK_{IN}, $CLK_{IN}X$.

Test Modes (Synthesizer, Transmit Mixer)

The LOCK output is selectable as a test output. Bits x0, x1 control the selection, the default setting is normal lock output as described in the Lock detect section. The selection of a Bit x0, x1 combination has a twofold effect: First it routes a divider output signal to the LOCK pin, second it disables mixer stages in the transmit path. Setting x0,1 = 11 disables both transmit path mixers. This mode can be used to prevent the transmitter from producing an IF output signal even if the transmit part is powered on. This can be used to simplify the control timing while commanding the transmit and receive simultaneously without the transmit part causing interference.

Table 1. Test Modes

x0	x1	Synthesizer Signal at LOCK Pin	Transmit Mixer	
			Q-mixer	I-mixer
0	0	normal lock detect	on	on
1	0	CLK_{IN} divided by reference divider ratio	off	on
0	1	$LO_{IN} \div 2$ * (main divider ratio)	on	off
1	1	main divider output, that goes to the phase detector	off	off

Table 2. Definition of SA1630 Serial Registers

First data word: (shown with default values)

Address SA1630				Sub Adr	N-Divider									Reference Divider		Charge-Pump			Test	
MSB																				LSB
a0	a1	a2	a3	sa	n0	n1	n2	n3	n4	n5	n6	n7	n8	r0	r1	c0	c1	c2	x0	x1
1	1	1	0	0	1	0	1	1	0	0	0	0	0	1	0	1	1	1	0	0

Address:	4 bits, a0...a3, fixed to 1110
Sub:Address:	1 bit, sa, fixed to 0 for first data word
N-Divider:	9 bits, n0...n8, values 64 (00100 0000) to 511 (11111 1111) allowed for IF choice, default 352 (assuming LO input frequency is 704 MHz).
Reference Divider Register:	2 bits, r0...r1, 00 = /8, 01 = 11, 10 = /22, 11 = /44. Default: 10
Charge-Pump Register:	3 bits, c0...c2, Binary setting factor for charge pumps, values 000 = minimum current to 111 = maximum current, default is maximum charge pump current (111)
Test Register:	2 bits, x0...x1, default 00, see functional description for details

Second data word: (shown with default values)

Address SA1630				Sub Adr	LLL Mode Control		I Offset Register			Q Offset Register			VGA Gain Control						Misc Control bits	
MSB																				LSB
a0	a1	a2	a3	sa	s0	s1	i0	i1	i2	q0	q1	q2	b0	b1	b2	b3	b4	b5	bc	vc
1	1	1	0	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1

Address:	4 bits, a0...a3, fixed to 1110
Sub:Address:	1 bit, sa, fixed to 1 for second data word
LLL Mode control:	2 bits, s0, s1 Not used, always set to 0, 0
I Offset Register:	3 bits, i0...i2 .10 Not used, always set to 0, 0, 0
Q Offset Register:	3 bits, q0...q2. q0. Currently not being used, always set to 0, 0, 0
VGA Gain Control	6 bits, b0...b5. 000 000 corresponds to maximum gain and 111 111 to minimum gain in 2 dB increments. Check control table contained elsewhere in this document.
VGA Control Enable	1 bit, bc. When bc=0 the VGA is controlled by external pins. When bc=1 then bits b0...b5 control the VGA. Default bc=0, control by external pins
Regulator Disable	1 bit, s0. When s0=0 the 2.5V reference output is completely powered down. When S0=1 the reference voltage is enabled (provided Tx_ON=HIGH). Default: s0 = 1, enable the 2.5 reference.

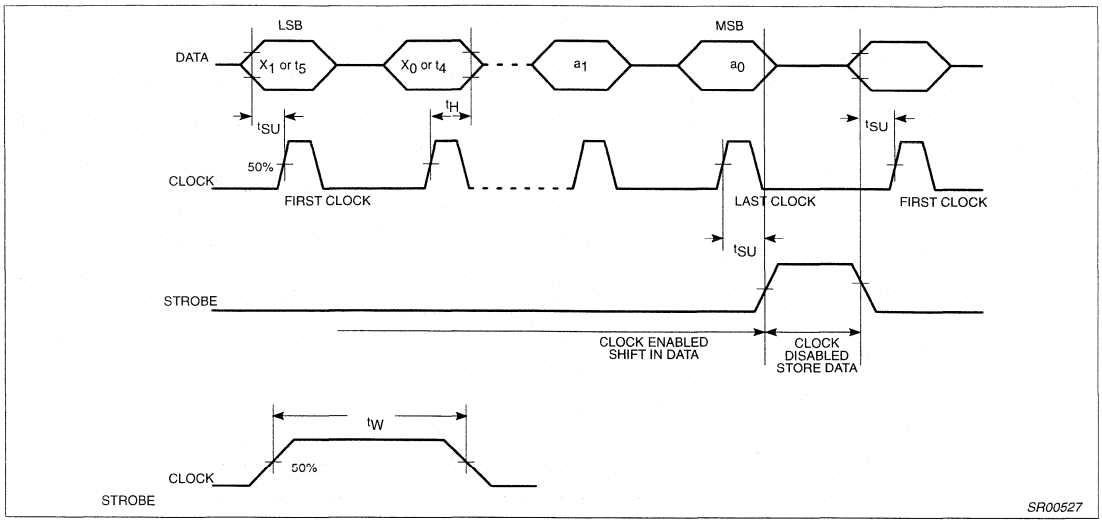


Figure 4. Serial Input Timing Sequence

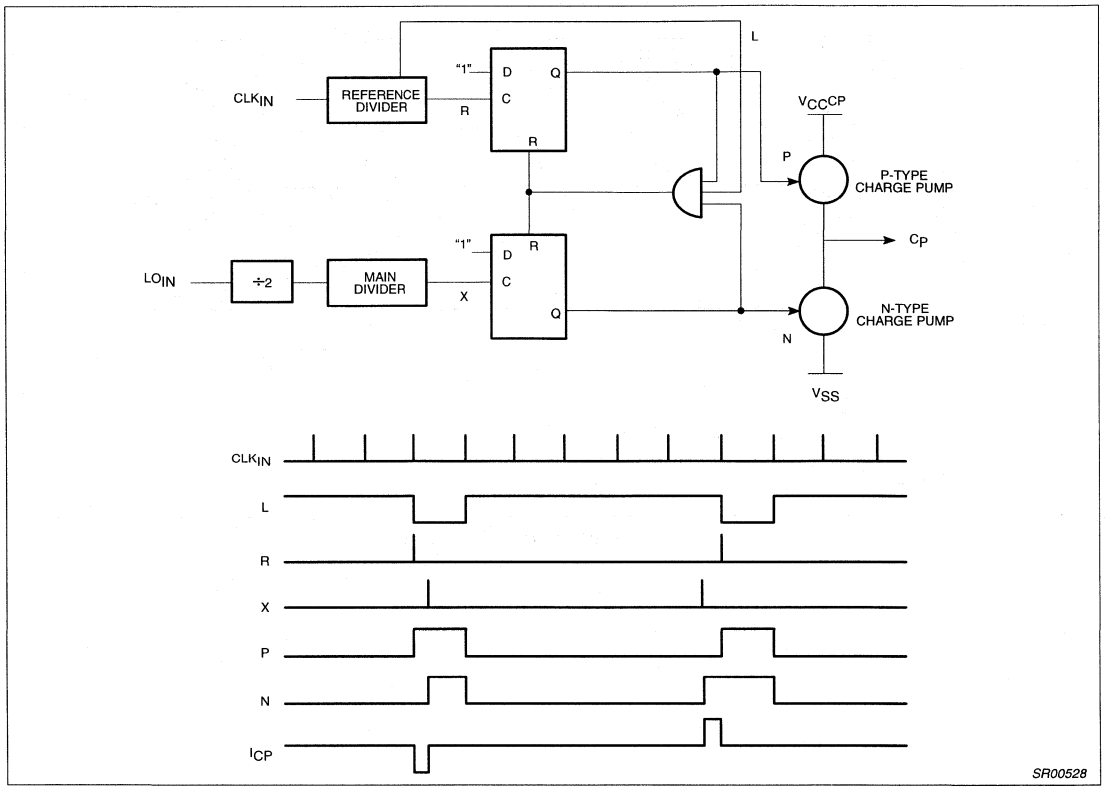


Figure 5. Phase Detector Structure with Timing

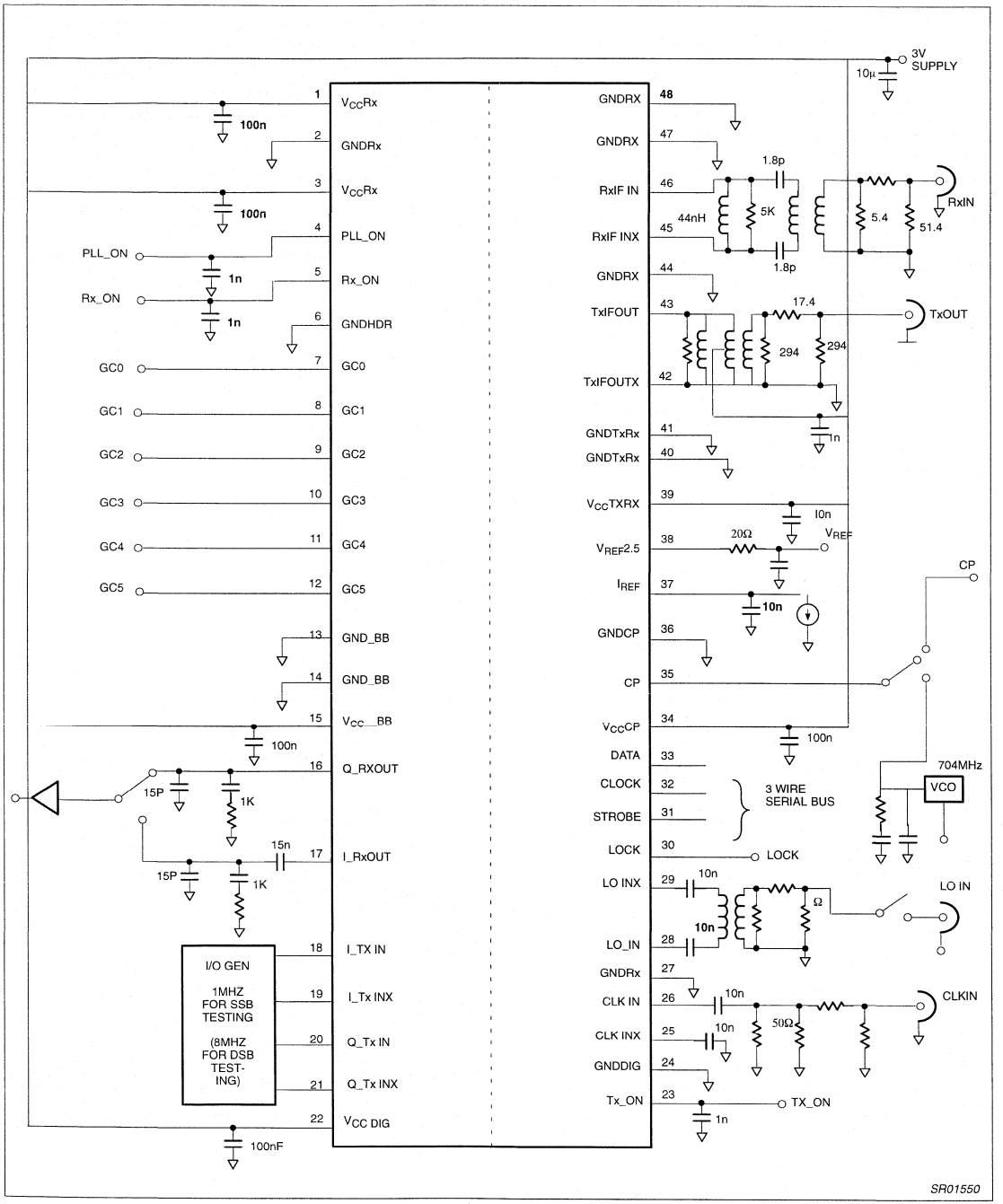


Figure 6. Typical SA1630 Test Circuit

Low voltage IF I/Q transceiver SA1638

DESCRIPTION

The SA1638 is a combined Rx and Tx IF I/Q circuit. The receive path contains an IF amplifier, a pair of quadrature down-mixers, and a pair of baseband filters and amplifiers. A second pair of mixers in the transmit path transposes a quadrature baseband input up to the IF frequency. An external VCO signal is divided down internally and buffered to provide quadrature local oscillator signals for the mixers. A further divider chain, reference divider and phase detector are provided to avoid the need for an external IF synthesizer. Rx or Tx path or the entire circuit may be powered down by logic inputs. On-board voltage regulators are provided to allow direct connection to a battery supply.

FEATURES

- Direct supply: 3.3V to 7.5V
- Two DC regulators giving 3.0V output
- Low current consumption: 18mA for Rx or 22mA for Tx
- Input/output IF frequency from 70-400 MHz
- Internal IF PLL for synthesizing the local oscillator signal
- High performance on-board integrated receive filters with bandwidth tunable between 50-850 kHz
- Switchable alternative bandwidth setting available to allow channel bandwidth flexibility in operation
- Designed for a widely used I and Q baseband GSM interface
- Control registers power up in a default state
- Optional DC offset trim capability to <200mV
- Only a standard reference input frequency required, choice of 13, 26, 39 or 52MHz
- Fully compatible with SA1620 GSM RF front-end (see Figure 9)

APPLICATIONS

- IF circuitry for GSM 900MHz hand-held units
- IF circuitry for PCN (DCS1800) hand-held units
- Quadrature up and down mixer stage

PIN CONFIGURATION

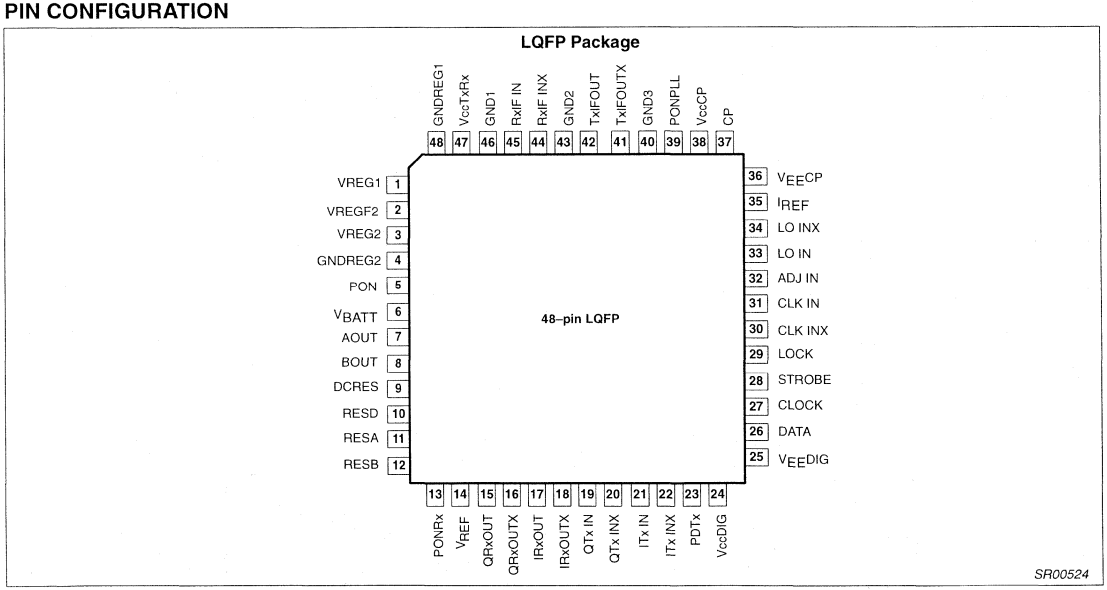


Figure 1. SA1638 Pin Configuration

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
48-Pin Thin Quad Flat Pack (LQFP)	-40 to +85°C	SA1638BE	SOT313-2

BLOCK DIAGRAM

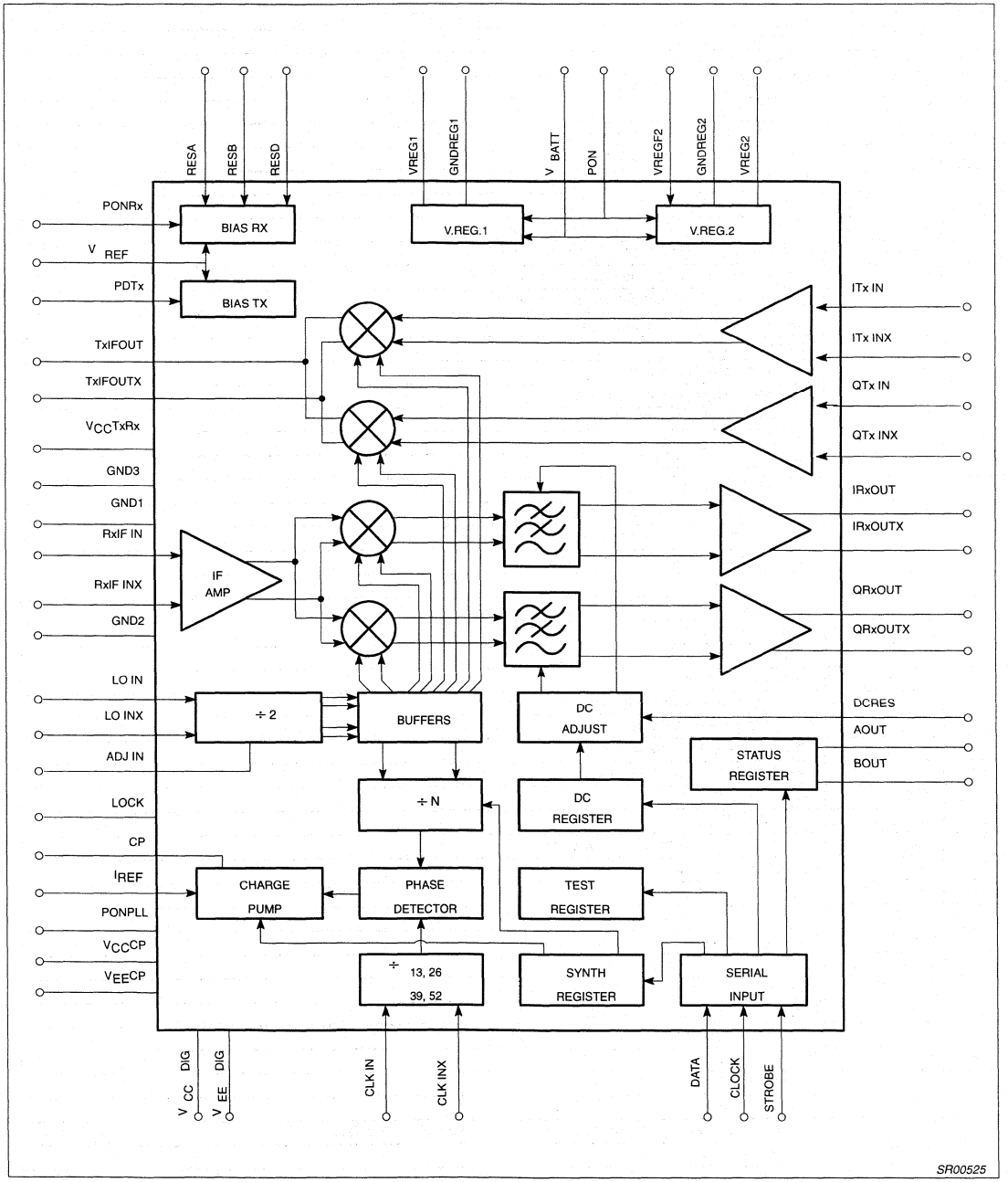


Figure 2. SA1638 Block Diagram

PIN DESCRIPTIONS

Pin No.	Pin Name	Description
1	VREG1	Output voltage of regulator 1
2	VREGF2	Feedback of regulator 2
3	VREG2	Output voltage of regulator 2
4	GNDREG2	Ground of regulator 2
5	PON	Power-on input for voltage regulators 1 and 2 (active high)
6	V_{BATT}	Input voltage for regulators 1 and 2
7	AOUT	Programmable logic output (see Figure 9)
8	BOUT	Programmable logic output (see Figure 9)
9	DCRES	Reference current setting resistor for DC offset circuit
10	RESD	Additional external current defining resistor for filters
11	RESA	Principal external current defining resistor for filters
12	RESB	Principal external current defining resistor for filters
13	PONRx	Power-on input for Rx (active high)
14	V_{REF}	Reference voltage
15	QRxOUT	Differential receive baseband output
16	QRxOUTX	Differential receive baseband output
17	IRxOUT	Differential receive baseband output
18	IRxOUTX	Differential receive baseband output
19	QTx IN	Differential transmit baseband input
20	QTx INX	Differential transmit baseband input
21	ITx IN	Differential transmit baseband input
22	ITx INX	Differential transmit baseband input
23	PDTx	Power-on for transmitter (active low)
24	V_{CC}DIG	Digital circuit supply
25	V_{EE}DIG	Digital ground
26	DATA	Serial bus data input
27	CLOCK	Serial bus clock input
28	STROBE	Serial bus strobe input
29	LOCK	Test control/synthesizer lock indicator
30	CLK INX	Differential reference divider input
31	CLK IN	Differential reference divider input
32	ADJ IN	Used for test only. Do not connect
33	LO IN	Differential LO input
34	LO INX	Differential LO input
35	I_{REF}	Reference current setting for charge pump
36	V_{EE}CP	Charge pump ground
37	CP	Charge pump output
38	V_{CC}CP	Charge pump circuit supply
39	POnPLL	Power-on input for synthesizer circuits (active high)
40	GND3	Ground (internal connection to GND1 and GND2)
41	TxIFOUTX	Differential transmit IFoutput (open collector)
42	TxIFOUT	Differential transmit IFoutput (open collector)
43	GND2	Ground (internal connection to GND1 and GND3)
44	RxIF INX	Differential receive IF input
45	RxIF IN	Differential receive IF input
46	GND1	Ground (internal connection to GND2 and GND3)
47	V_{CC}TxRx	Transmit and receive circuits supply voltage (also feedback of Regulator 1)
48	GNDREG1	Ground of regulator 1
NOTE: There are no ESD protection diodes at Pins 41 and 42. Thus, open collector outputs may have increased DC voltage or higher AC peak voltage.		

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
$V_{CC}XXX$	Supply voltages: $V_{CC}TxRx$, $V_{CC}DIG$, $V_{CC}CP$	-0.3 to +6.0	V
V_{BATT}	Battery voltage	-0.3 to +8.0	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{CCXXX}+0.3)	V
ΔVG	Any GND pin to any other GND pin	0	V
P_D	Power dissipation, T_A = 25°C (still air)	300	mW
T_{JMAX}	Maximum operating junction temperature	150	°C
P_{MAX}	Maximum power input/output	+20	dBm
T_{STG}	Storage temperature range	–65 to +150	°C

NOTE:
1. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance, θ_{JA}. 48-pin LQFP: θ_{JA} = 67°C/W.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
$V_{CC}XXX$	Supply voltages: $V_{CC}TxRx$, $V_{CC}DIG$	2.7 to 5.5	V
$V_{CC}CP$	Charge pump supply voltage	2.9 to 5.5	V
V_{BATT}	Battery voltage	3.3 to 7.5	V
T_A	Operating ambient temperature range	-40 to +85	°C

Voltage Regulators

T_A = 25°C, P_{ON} = 3V, $P_{ON}RX$ = 0V, PDTX = 3V, $P_{ON}PLL$ = 0V, V_{BATT} = 3.3V, $I_{OUT}1$ = $I_{OUT}2$ = 15mA, $V_{REG}1$ connected to $V_{CC}TxRx$, $V_{REG}2$ connected to $V_{REG}F2$; $V_{CC}DIG$ = $V_{CC}CP$ = 3V; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNITS
			Min	–3σ	Typ	+3σ	Max	
$V_{REG}1$, $V_{REG}2$	Nominal V_{OUT}		2.85	2.93	3.00	3.07	3.15	V
V_{BATT}			3.3				7.5	V
$I_{OUT}1$, $I_{OUT}2$	Maximum output current for each regulator[1]						30	mA
I_{BATT}	Supply current for both regulators	I_{LOAD} = 0mA		4.3	5	5.7	7	mA
$I_{BATT\ PD}$	Power-down supply current	P_{ON} = 0V, I_{LOAD} = 0mA		7.7	9	10.3	15	µA
$C_{REG}1^2$	$V_{REG}1$ cap load		0.1				1000	µF
$C_{REG}2^2$	$V_{REG}2$ cap load		0.1				500	µF
LINEREG	Line regulation	DC, V_{BATT} = 3.3V to 7.5V	–0.4	–0.2	0.001	0.2	0.4	%
LOADREG	Load regulation	I_{LOAD} = 15mA to 30mA	–5	–0.37	-0.17	0.03	5	%
BW	Bandwidth		100					kHz
F_{PON}	Feedthrough attenuation from P_{ON} to each regulator				≤ -40			dB
F_{REG}	Feedthrough attenuation from V_{BATT} to each regulator	f ≤ 100kHz f = 10MHz f = 100MHz f = 400MHz			≤ -61 ≤ -32 ≤ -37 ≤ -48			dB
t_{ON}	Turn ON time				10			µs

NOTES:
1. At $T_j \geq$ 150°C a thermal switch reduces the output current to avoid damage.
2. Recommended load capacitors: In every case $C_{REG}1$ = $C_{REG}2$ = 100nF to ground with series resistance ≤0.1Ω. Additional capacitor optional ≤1000µF with series resistance ≤5Ω. The low series resistance is very important to ensure regulator stability.
3. Standard deviations are based on the characterization results of 90 ICs.

DC ELECTRICAL CHARACTERISTICS

V_{CC}TxRx=V_{CC}DIG=V_{CC}CP=PONRx=PONPLL= +3V; V_{EE}DIG = V_{EE}CP=GND1=GND2=GND3=PDTx = 0V; T_A = 25°C, unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNITS
			MIN	–3σ	TYP	+3σ	MAX	
I_{CC}	Supply current							mA
	Rx and IF synthesizer active	PONRx = PONPLL = PDTx = Hi		14.4	16	17.6	20	
	Tx and IF synthesizer active	PONRx = PDTx = Low; PONPLL = Hi		17.4	19.5	21.6	24	
	Power-down mode	PONRx = PONPLL = Low; PDTx = Hi			0.068			
V_{REF}	Reference voltage	Generated internally		1.39	1.57	1.75		V
IV_{REF}	V_{REF} I_{SINK} I_{SOURCE}				5 5			µA
I_{OUT}	DC output current	At pins TxIFOUT and TxIFOUTX	1.5	1.86	2.0	2.14	2.7	mA
Digital inputs (P_{ON})								
V_{IH}	High level input voltage range		2.0				V_{BATT}	V
V_{IL}	Low level input voltage range		0				0.8	V
Digital inputs (PDTx, P_{ON}Rx, P_{ON}PLL, P_{ON})								
V_{IH}	High level input voltage range		2.0				V_{CC}TxRx	V
V_{IL}	Low level input voltage range		0				0.8	V
Digital inputs (Clock, Data, Strobe)								
V_{IH}	High level input voltage range		2.0				V_{CC}Dig	V
V_{IL}	Low level input voltage range		0				0.8	V
Digital outputs (LOCK, AOUT, BOUT)								
V_{OH}	Output voltage HIGH	I_O = -2mA	V_{CC}DIG–0.4					V
V_{OL}	Output voltage LOW	I_O = 2mA					0.4	V

AC ELECTRICAL CHARACTERISTICS

V_{CC}TxRx=V_{CC}DIG=V_{CC}CP=PONRx=PONPLL= +3V; V_{EE}DIG = V_{EE}CP=GND1=GND2=GND3=PDTx = 0V; LO_{IN} = 100mV_{PEAK}, 800MHz; CLK_{IN} = 100mV_{PEAK}, 52MHz; serial registers programmed with default values; T_A = 25°C unless otherwise stated. Test Circuit Figure 8.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNITS
			MIN	–3σ	TYP	+3σ	MAX	
IF Transmit Modulator								
BW	Input modulation bandwidth	200Ω source impedance		0.82	0.94	1.06		MHz
V_{COM}	Common mode range for baseband inputs	DC at pins ITxIN, ITxINx, QTxIN, QTxINx	1		1.5		2	V
V_{IN}	Peak input signal amplitude	Centered on V_{COM}			0.75			V
	Third harmonic distortion[1]	| ITxIn | = | ITxInX | = | QTxIn | = | QTxInX | = 0.75V_{PEAK}; fin = 20kHz		-61	-57	-53	-40	dB
R_{INTx}	Input resistance	Between pins: ITxIn and ITxInX or QTxIn and QTxInX	112					kΩ
C_{INTx}	Input capacitance	At ITxIn, ITxInX, QTxIn, QTxInX					10	pF
	Output saturation limit						V_{CC}TxRx-0.3	V
I_{OUT}	RMS output current	| ITxIn | = | ITxInX | = | QTxIn | = | QTxInX | = 0.75V_{PEAK}	0.6	0.73	0.82	0.91	1.08	mA
S_{LO}	LO suppression[1]	| ITxIn | = | ITxInX | = | QTxIn | = | QTxInX | = 0.75V_{PEAK}; fin = 20k	+30		+43			dB
SSB	Sideband suppression[1]	| ITxIn | = | ITxInX | = | QTxIn | = | QTxInX | = 0.75V_{PEAK}; fin = 20k	+35		+50			dB

AC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNITS
			MIN	−3σ	TYP	+3σ	MAX	
IF Transmit Modulator (continued)								
	Noise density at 600kHz	|ITxInI = |ITxInX| = |QTxInI = |QTxInX| = 0.75V_{PEAK}		-130	-129	-128		dBc/Hz
	Noise density at 10MHz			-133	-131	-129		
t_{ON}	Turn ON time	PdTx = LO, transmit signal to 90%			5			µs
t_{OFF}	Turn OFF time	PdTx = HI, transmit signal to 10%			5			µs
IF Receiver (R = 36kΩ between pins RESA and RESB)								
RInRx	Differential input impedance	f_{IN} = 400MHz			5 || 0.6			kΩ || pF
ROutRx	Output impedance				1			kΩ
	Output common mode voltage				V_{REF}			V
f3dB	Low pass filter -3dB bandwidth		70		83		90	kHz
	Low pass filter attenuation: 200kHz 400kHz 600kHz 6.5MHz 13.0MHz		 6.5 30	 8.9 38.1	 10.7 45 70 >80 >80	 12.5 51.9		dB
VG	Voltage gain	Differential output PD into GSM baseband relative to 1200Ω source EMF	43	49.4	51	52.7	58	dB
NF	Noise figure[8]	1200Ω source and external matching resistor and inductor		5.7	7.0	8.3		dB
	Channel matching: Gain Phase	f_{IN} = 400.005MHz	-1.5		 -0.26 0.0		1.5	 dB degrees
	Output DC offset[2]	Differential, DCRES=562kΩ	-60		-25		60	mV
I_{OUT}	Output drive current at each pin	Source (Sink)			10 (700)			µA
V_{OUT}	Minimum differential output swing				2.0			V
P_{-1dB}	Input 1dB compression point: In band 200kHz 400kHz 600kHz	1200Ω source EMF	 -59 -54	 -55.3 -49.3	 -53 -47 -47 -47	 -50.7 -44.8	 -47 -40	dBV
t_{ON}	Turn ON time[3]	POnRx = HI, to baseband signal out			2			µs
t_{OFF}	Turn OFF time	POnRx = LO, to no baseband signal out			2			µs
IF Synthesizer								
f_{LO}	Local oscillator input frequency range[9]		140				800	MHz
Z_{LOIN}	Differential input impedance	Between pins LO_{IN} and $LO_{IN}X$, f_{IN} = 800MHz			276 || 0.6			Ω || pF
V_{LOIN}	LO peak input voltage range	Single-ended Referred to 50Ω	50				100	mV
	Programmable divider: Division range Step size		64		 1		511	
f_{CLKIN}	Reference clock input frequency	V_{CLKIN} = 100mV_{PEAK}					52	MHz
Z_{CLKIN}	Differential input impedance	Between pins ClkIn and ClkInX			10 || 1.0			kΩ || pF
V_{CLKIN}	CLK_{IN} peak input voltage range	Single-ended, referred to 50Ω	50				400	mV
I_{REF}	Charge pump input reference current				31.2			µA
$\|I_{CP}\|$	Charge pump output current: c0...c2 = 000 c0...c2 = 111 Step size	I_{REF} =31.2µA, V_{CP} = V_{CC}CP/2	 0.425 0.85 0.045	 0.487 0.979 0.062	 0.5 1.0 0.071	 0.513 1.021 0.08	 0.575 1.15 0.105	mA

AC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNITS
			MIN	–3σ	TYP	+3σ	MAX	
IF Synthesizer (cont.)								
$\frac{\Delta I_{CP}}{I_{CP}}$	Relative output current variation[4]	I_{REF} =31.2µA		0.1	1.3	2.5	±10	%
ΔI_{CP_M}	Output current matching[5]	I_{REF} =31.2µA, $V_{CP} = V_{CC}CP/2$					±12	%
$\lvert I_{CP\_L} \rvert$	Output leakage current	V_{CP} = 0.3V to V_{CC}CP-0.3V		-0.02	0.1	0.22	±15	nA
t_{ON}	Turn ON time	POnPLL = HI, to full charge pump current			15			µs
t_{OFF}	Turn OFF time[6]	POnPLL = LO, to I_{CC}CP, I_{CC}DIG <5% of operational supply current			15			µs
Serial Interface[7]								
f_{CLOCK}	Clock frequency						10	MHz
t_{SU}	Set-up time: DATA to CLOCK, CLOCK to STROBE		30					ns
t_H	Hold time: CLOCK to DATA		30					ns
t_W	Pulse width: CLOCK		30					ns
	Pulse width: STROBE		30					

NOTES:
1. Parameter measured relative to modulation sideband amplitude.
2. After programming the DC offset register for minimum offset. DCRES = 562kΩ.
3. The turn on time relates only to the power up time of the circuit. The settling time of the integrated baseband filters has to be added (for GSM–mode = 8µs with filter bandwidth setting resistor = 36kΩ).
4. The relative output current variation is defined thus: $\frac{\Delta I_{OUT}}{I_{OUT}} = 2 \cdot \frac{(I_2 - I_1)}{\lvert(I_2 + I_1)\rvert}$; with V_1 = 0.3V, $V_2 = V_{CC}CP - 0.3V$ (see Figure 3).
5. The output current matching is measured when both (positive current and negative current) sections of the output charge pumps are on.
6. As soon as P_{ON}PLL is set to LO, the phase detector is reset and no charge pumps pulses are generated.
7. Guaranteed by design.
8. $NF = \left[20 \log \left(\frac{E_{no}}{\sqrt{4kTR}} \right) \right] - VG$ where, E_{no} is the output noise voltage measured in a 1Hz bandwidth, R = 1200Ω, VG = gain in dB.
9. Minimium frequency is guaranteed by design.

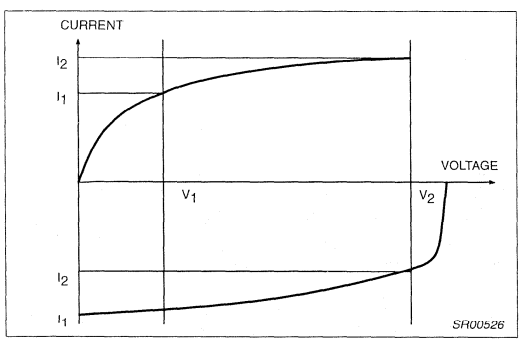


Figure 3. Relative Output Current Variation

FUNCTIONAL DESCRIPTION

Serial Programming Input

The serial input is a 3-wire input (CLOCK, STROBE, DATA) to program the counter ratios, charge pump current, status- and DC-offset register, mode select and test register. The programming data is structured into two 21-bit words; each word includes 4 chip address bits and 1 subaddress bit. Figure 2 shows the timing diagram of the serial input. When the STROBE = L, the clock driver is enabled and on the positive edges of the CLOCK the signal on DATA input is clocked into a shift register. When the STROBE = H, the clock is disabled and the data in the shift register remains stable. Depending on the value of the subaddress bit the data is latched into different working registers. Table 3 shows the contents of each word.

Default States

Upon power up (V_{CC}DIG is applied) a reset signal is generated, which sets all registers to a default state. The logic level at the STROBE pin should be low during power up to guarantee a proper reset. These default states are shown in Table 3.

Reference Divider

The reference divider can be programmed to four different division ratios (:13, :26, :39, :52), see registers r0, r1; default setting: divide by 13.

Main Divider

The external VCO signal, applied to the LO_{IN} and $LO_{IN}X$ inputs, is divided by two and then fed to the main divider (:N). The main divider is a programmable 9 bit divider, the minimum division ratio is

divide by 64. The division ratio is binary coded and set in the registers n0 to n8. The default setting is a divide by 400.

At the completion of a main divider cycle, a main divider output is generated which will drive the phase detector.

Phase Detector

The phase detector is a D-type flip-flop phase and frequency detector shown in Figure 5. The flip-flops are set by the negative edges of the output signals of the dividers. The rising edge of the signal L will reset the flip-flops after both flip-flops have been set. Around zero phase error this has the effect of delaying the reset for 1 reference input cycle. This avoids non-linearity or deadband around zero phase error. The flip-flops drive on-chip charge pumps. A source current from the charge pump acts to increase the VCO frequency; a sink current acts to decrease the VCO frequency.

Current Setting

The charge pump current is defined by the current set between the pin I_{REF} and $V_{EE}CP$. The current value to be set there is 31.2µA. This current can be set by an external resistor to be connected between the pin I_{REF} and $V_{EE}CP$. The typical value R_{EXT} (current setting resistor) can be calculated with the formula

$$R_{EXT} = \frac{V_{CC}CP - 1.4V}{31.2\mu A}$$

The current can be set to zero by connecting the pin I_{REF} to $V_{CC}CP$.

Charge Pumps

The charge pumps at pin CP are driven by the phase dectector and the current value is determined by the binary value of the charge pumps register CN = c2, c1, c0, default 1mA. The active charge pump current is typically:

$$|I_{CP}| = (c0 + 2c1 + 4c2) \cdot 71\mu A + 500\mu A$$

Lock Detect

The output LOCK is H when the phase detector indicates a lock condition. This condition is defined as a phase difference of less than ±1 cycle on the reference input CLK_{IN}, $CLK_{IN}X$.

Test Modes (Synthesizer, Transmit Mixer)

The LOCK output is selectable as a test output. Bits x0, x1 control the selection, the default setting is normal lock output as described in the Lock detect section. The selection of a Bit x0, x1 combination has a twofold effect: First it routes a divider output signal to the LOCK pin, second it disables mixer stages in the transmit path. Setting x0,1 = 11 disables both transmit path mixers. This mode can be used to prevent the transmitter from producing an IF output signal even if the transmit part is powered on (PDTx = 0V). This can be used to simplify the control timing while commanding the transmit and receive simultaneously without the transmit part causing interference.

Table 1. Test Modes

x0	x1	Synthesizer Signal at LOCK Pin	Transmit Mixer	
			Q-mixer	I-mixer
0	0	normal lock detect	on	on
1	0	CLK_{IN} divided by reference divider ratio	off	on
0	1	LO_{IN} ÷ 2 * (main divider ratio)	on	off
1	1	main divider output, that goes to the phase detector	off	off

Status Register

The s0 and s1 status bits determine the values of the logic output pins A_{OUT} and B_{OUT}. These outputs can be connected to the AGC control inputs A and B of the SA1620. (See Figure 9)

DC Offset Register

Registers i0 to i3 and q0 to q3 control a correction to the output DC offset of the I and Q channels of the receiver. The polarity of the DC offset correction in the I and Q channels are determined by i0 and q0, respectively. The other bits set the magnitude of the offset correction. The step size of the two offset correction DACs is fixed by an external resistor between the DCRES pin and ground. A value of 120kΩ will give a step size of 200mV.

Mode Select Register

t0: switches the RX IF gain.

t0 = 0 no attenuation

t0 = 1 10dB attenuation

The attenuation switch is included between the IF amplifier and the I and Q mixers, thereby influencing the noise figure negligibly. The purpose of this switch is to provide another AGC step which does not influence the receiver noise figure. Please note that this gain change will influence the DC offset of the I and Q mixers.

t1 = 0 test mode only, always to be set to 0.

t2, t3 sets the mode of the level locked loop (LLL)

The LLL is a circuit which processes the LO input signal in order to provide an LO signal with a perfect 50% duty cycle, which determines the precision of the 90° shift of the I and Q mixing signals generated by the ÷2 divider. For an external tuning of the 90° phase shift of the I and Q mixing signals, a trimming resistor may be connected (but is not required) between the ADJ_{IN} pin and ground, and the LLL has to be put in one of the following modes:

Table 2. Mode Select Register

t2	t3	LLL Status
0	0	LLL on (no external tune, monitor performance, default)
0	1	LLL on (with medium external tune)
1	0	LLL off (tune externally)
1	1	LLL on (with fine external tune)

t4 selects the bandwidth of the RC low pass filters at the I, Q Rx mixer outputs

t4 = 0 cutt-off frequency (-3dB) 110kHz

t4 = 1 cutt-off frequency (-3dB) 792kHz

t5 selects the bandwidth of the integrated 5th-order gyrator filters. The filters are tuneable over a range of 50kHz to 1MHz with external resistors. The -3dB bandwidth is inversely proportional to the value of the external resistor.

With

t5, two external resistor values are selectable.

t5 = 0 the resistance between the pins RESA and RESB determines the cutoff frequency. For GSM a nominal bandwidth of 80kHz is chosen when the external resistor is 36kΩ.

t5 = 1 a second resistor between the pins RESB and RESD is connected in parallel to the first external resistor, thus increasing the filter bandwidth. The relative amplification is decreased in this mode.

The overall filter response in the receive section is the sum of the filter responses of the passive RC low-pass filter and the active gyrator filter.

Power Down Modes

There are 4 power-on pins in the SA1638: P_{ON}, P_{ON}Rx, PDTx, P_{ON}PLL.

P_{ON} = H powers up both voltage regulators $V_{REG}1$ and $V_{REG}2$. P_{ON} should be set to L, if these internal voltage regulators are not to be used.

P_{ON}Rx = H powers up the receiver part.

PDTx = L powers up the transmitter part.

P_{ON}PLL = H powers up the synthesizer part. As it also powers up the first divide by 2 stage for generating the 0/90 degree phase shifted signals for the transmit and receive mixers, it also has to be set H if either the transmit part or the receive part is used. P_{ON}PLL = L powers down the dividers, resets the phase detector and disconnects the current setting pin I_{REF}. In P_{ON}PLL = L mode, the values in the serial input registers are still kept and the part still can be reprogrammed as long as V_{CC}DIG is present.

Table 3. Definition of SA1638 Serial Registers

First data word: (shown with default values)

Address SA1638				Sub Adr	N-Divider									Ref ÷ Reg		Charge-Pump			Reg Test	
MSB																				LSB
a0	a1	a2	a3	sa	n0	n1	n2	n3	n4	n5	n6	n7	n8	r0	r1	c0	c1	c2	x0	x1
1	1	1	0	0	1	1	0	0	1	0	0	0	0	0	0	1	1	1	0	0

Address:	4 bits, a0...a3, fixed to 1110
Sub:Address:	1 bit, sa, fixed to 0 for first data word
N-Divider:	9 bits, n0...n8, values 64 (00100 0000) to 511 (111111111) allowed for IF-choice, default 400
Reference Divider Register:	2 bits, r0...r1, 00 = ÷13, 01 = ÷26, 10 = ÷39, 11 = ÷52. Default: 00
Charge-Pump Register:	3 bits, c0...c2, Binary current setting factor for charge pumps, values 000 = minimum current to 111 = maximum current, default maximum charge pump current
Test Register:	2 bits, x0...x1, default 00, see Functional Description

Second data word: (shown with default values)

Address SA1638				Sub Adr	Status Reg		DC Offset Register								Mode Select Register					
							Q-Channel				I-Channel									
MSB																				LSB
a0	a1	a2	a3	sa	s0	s1	q0	q1	q2	q3	i0	i1	i2	i3	t0	t1	t2	t3	t4	t5
1	1	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Address:	4 bits, a0...a3, fixed to 1110
Sub:Address:	1 bit, sa, fixed to 1 for second data word
Status Register:	2 bits, s0 sets pin A_{OUT}, s1 sets pin B_{OUT}, see Functional Description
DC Offset Register:	4 bits per channel, i0...i3 and q0...q3, no correction as default i0 and q0 switches offset polarity, 0 to lower voltage, 1 to higher voltage il...i3 and q1...q3, 000 no correction to 111 max. correction enabled
Mode Select Register:	6 bits, t0...t5, 000000 = normal GSM-Operation as default, see Functional Description

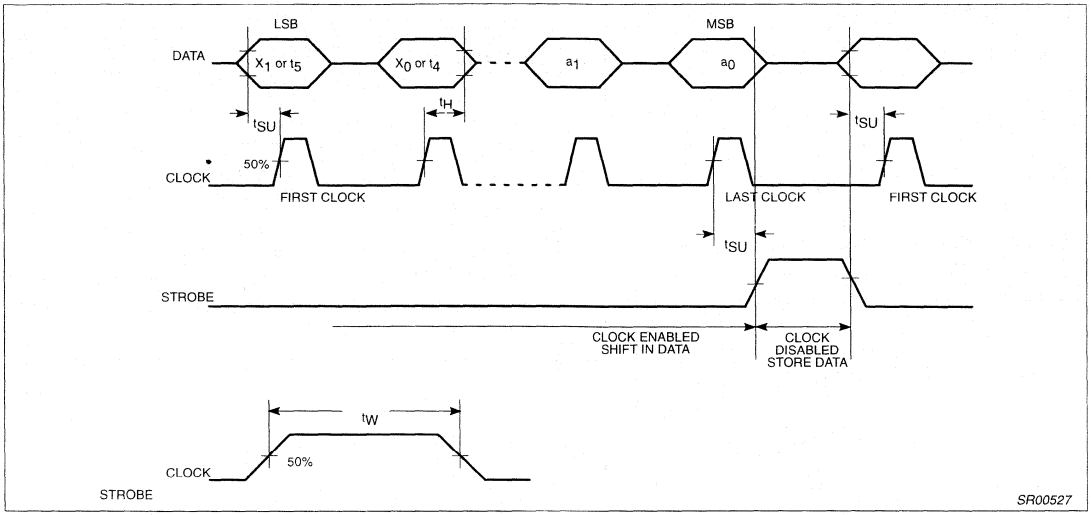


Figure 4. Serial Input Timing Sequence

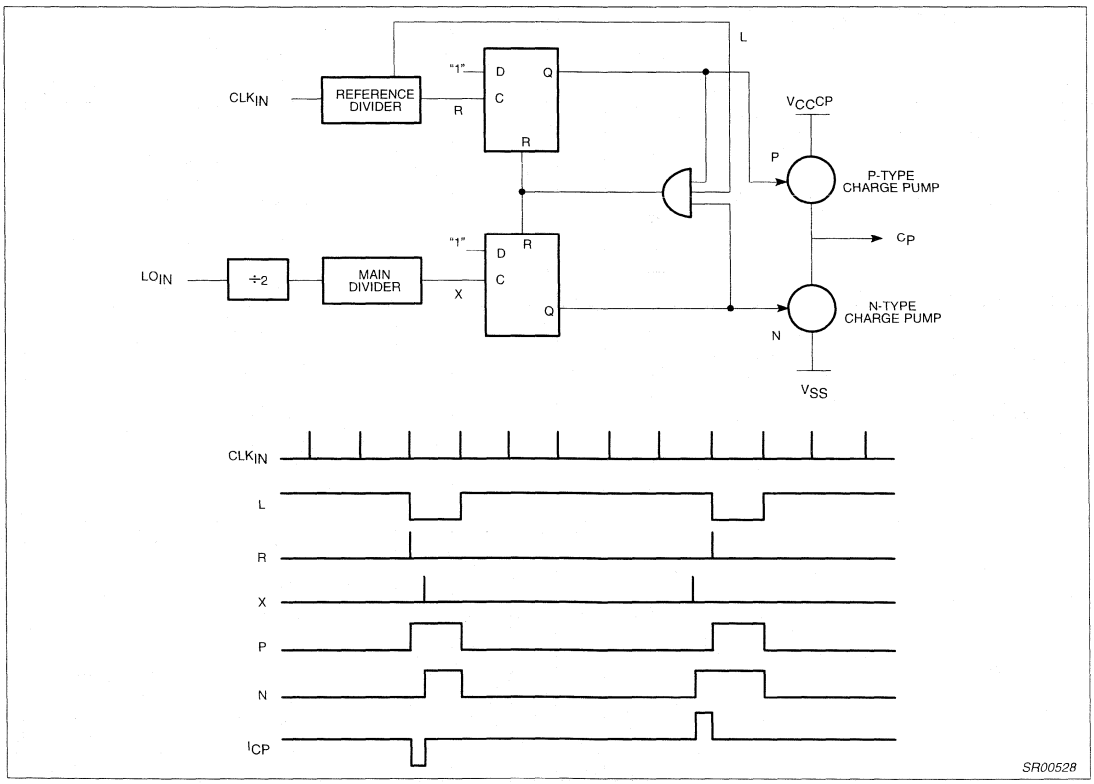


Figure 5. Phase Detector Structure with Timing

PIN FUNCTIONS

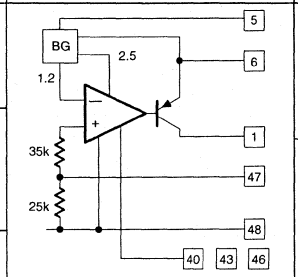
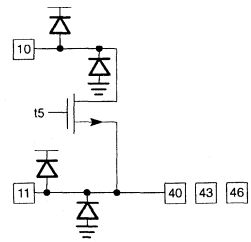
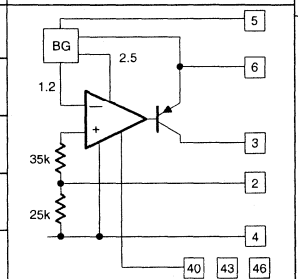
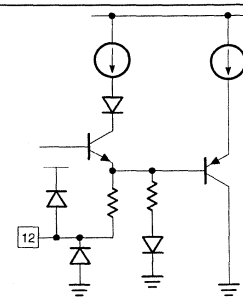
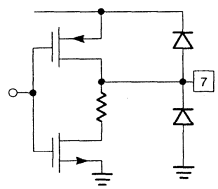
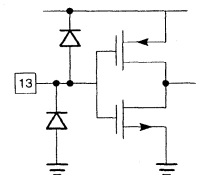
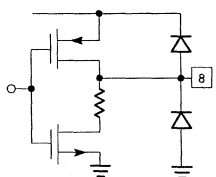
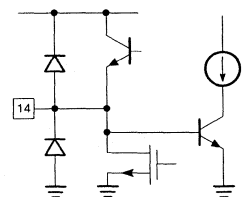
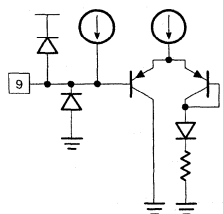
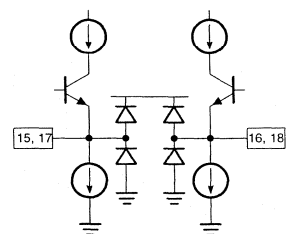
PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT	PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
47	$V_{CC}TxRx$	3.0		10	RES_D	0.05	
48	$GND_{REG}1$	0.0		11	RES_A	0.00	
1	$V_{REG}1$	3.0					
2	$V_{REG}F2$	3.0		12	RES_B	0.05	
3	$V_{REG}2$	3.0					
4	$GND_{REG}2$	0.0					
5	P_{ON}	3.3					
6	V_{BATT}	3.3					
7	A_{OUT}	3.0		13	$P_{ON}Rx$	3.0	
8	B_{OUT}	3.0		14	V_{REF}	1.5	
9	DC_{RES}	1.6		15	QRX_{OUT}	1.5	
				16	$QRX_{OUT}X$	1.5	
				17	IRX_{OUT}	1.5	
				18	$IRX_{OUT}X$	1.5	

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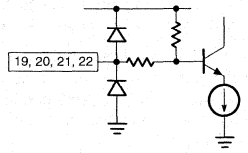
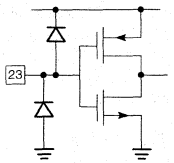
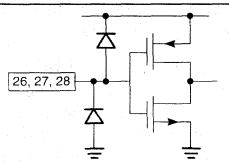
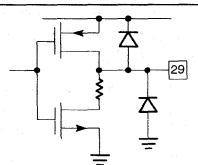
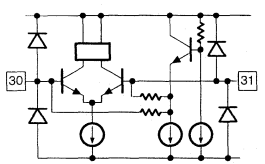
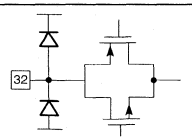
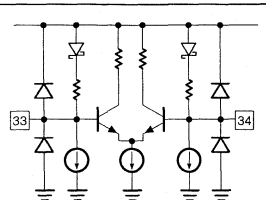
Figure 6. Pin Functions

PIN FUNCTIONS (continued)

PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
19	QTX_{IN}	1.5	
20	$QTX_{IN}X$	1.5	
21	ITX_{IN}	1.5	
22	$ITX_{IN}X$	1.5	
23	PdTx	0.0	
24	$V_{CC}DIG$	3.0	
25	$V_{EE}DIG$	3.0	
26	DATA		
27	CLOCK		
28	STROBE		
29	LOCK		
30	CLK_{IN}	2.0	
31	$CLK_{IN}X$	2.0	
32	ADJ_{IN}	2.0	
33	LO_{IN}	2.0	
34	$LO_{IN}X$	2.0	

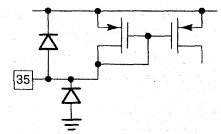
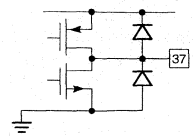
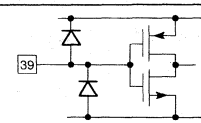
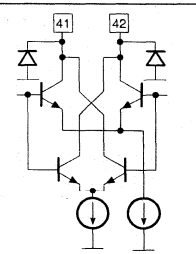
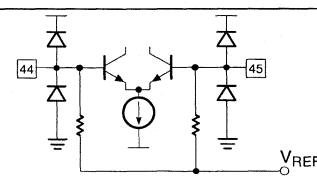
PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
35	I_{REF}	1.6	
36	$V_{EE}CP$	0.0	
37	CP		
38	$V_{CC}CP$	3.0	
39	$P_{ON}PLL$	3.0	
40	GND3	0.0	
41	$TXIF_{OUT}X$	OPEN COLLECTOR	
42	$TXIF_{OUT}X$	OPEN COLLECTOR	
43	GND2	0.0	
44	$RxIF_{IN}X$	1.5	
45	$RxIF_{IN}$	1.5	
46	GND1	0.0	
47	$V_{CC}TxRx$	3.0	
48	$GND_{REG}1$	0.0	

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Figure 7. Pin Functions (cont.)

Overview of Dual GSM/PCN Architecture

The SA1620 RF front-end and SA1638 IF transceivers form a dual conversion architecture which uses a common IF and standard I/Q baseband interface for both transmit and receive paths. The time division multiplex nature of the GSM system permits integration of the transmit and receive functions together on the one RF and one IF chips. This simplifies the distribution of local oscillator signals, maximizes circuitry commonality, and reduces power consumption.

The SA1620 and SA1638 allow considerable flexibility to optimize the transceiver design for particular price/size/performance requirements, through choice of appropriate RF and IF filters. The IF may be chosen freely in the range 70–400 MHz. The same IF can be used in the transmit and receive directions. Alternately, different IFs can be used if the SA1638 synthesizer frequency is switched between transmit and receive timeslots. The comparison frequency of the SA1638 PLL is high in order to provide fast switching time.

With suitable choice of the IF, an identical SA1638 IF receiver design can be used for both 900MHz GSM and 1800MHz PCN (DCS1800) equipment.

General Benefits/Advantages

- 2.7V operation. Compatible with 3V digital technology and portable applications. (Higher voltage operation also possible, if desired.)
- Excellent dynamic range. The availability of two LNAs in the SA1620 allows flexibility in receiver dynamic design for portable and mobile GSM spec. applications with appropriate filters. If for a particular application a GaAs or discrete front-end is desired, one of the LNAs can be left unpowered. Placing the AGC gain switches at the front results in some attenuation most of the time, further increasing typical dynamic performance beyond that specified by GSM.
- High power transmit output driver, delivering +7.5dBm output. This is sufficient to drive a filter and power amplifier input, without a driver amplifier. To avoid unnecessary current consumption, the output power can be reduced to an appropriate level by choice of an external resistor.
- DC offsets generated in the receive channel are independent of the LNA AGC setting, and correctable by software to prevent erosion of signal handling dynamic range by DC offsets.
- Minimal high-quality filter requirements. As a result of the integration in the SA1638 of high quality channel selectivity filters, only sufficient filtering is needed in the receive path to provide blocking protection for the second mixers. This reduces receiver cost and size.
- Operation at a high IF allows RF image reject filter requirements to be relaxed. For example, at a 400MHz IF, the natural gain roll-off in the SA1620 LNAs and mixer suppresses the image signal in the 1800MHz band by typically 28dB below the desired 900MHz band signal.

DC Offset Correction

DC offset correction is provided by two DACs each feeding into one of the two Rx channels. The step size of both DACs is set by the value of the external resistor between DCRES and ground. Thus any original offset less than 1.5V magnitude in either channel can be reduced to the specified level by selecting the appropriate DAC setting via the serial interface.

Integrated Receive Filters

The low-pass characteristics of the Rx channel are determined by two low-pass responses. The first of these is a passive filter at the output of the quadrature mixers and the second is the low-pass filters which follow the post-mixer amplifiers. These specifications refer only to the response of the default state, but this may be switched by the control register to an alternative setting with a nominal 3dB point of 792kHz.

The corner frequency of the low pass filters can be adjusted over a wide range by varying the value of the external resistor between RESA and RESB. The range of feasible corner frequencies extends at least between 50kHz and 500kHz.

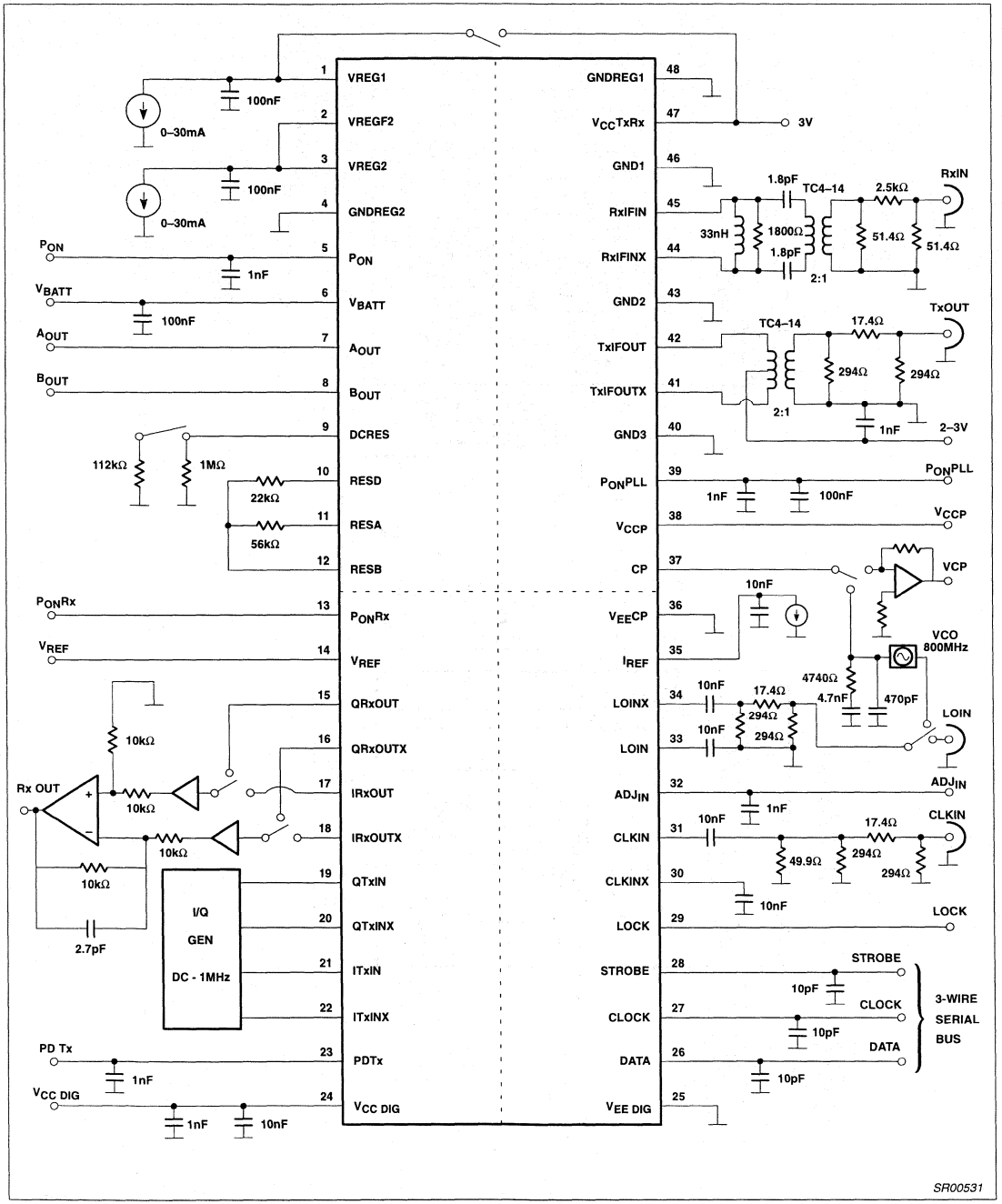


Figure 8. SA1638 Test Circuit

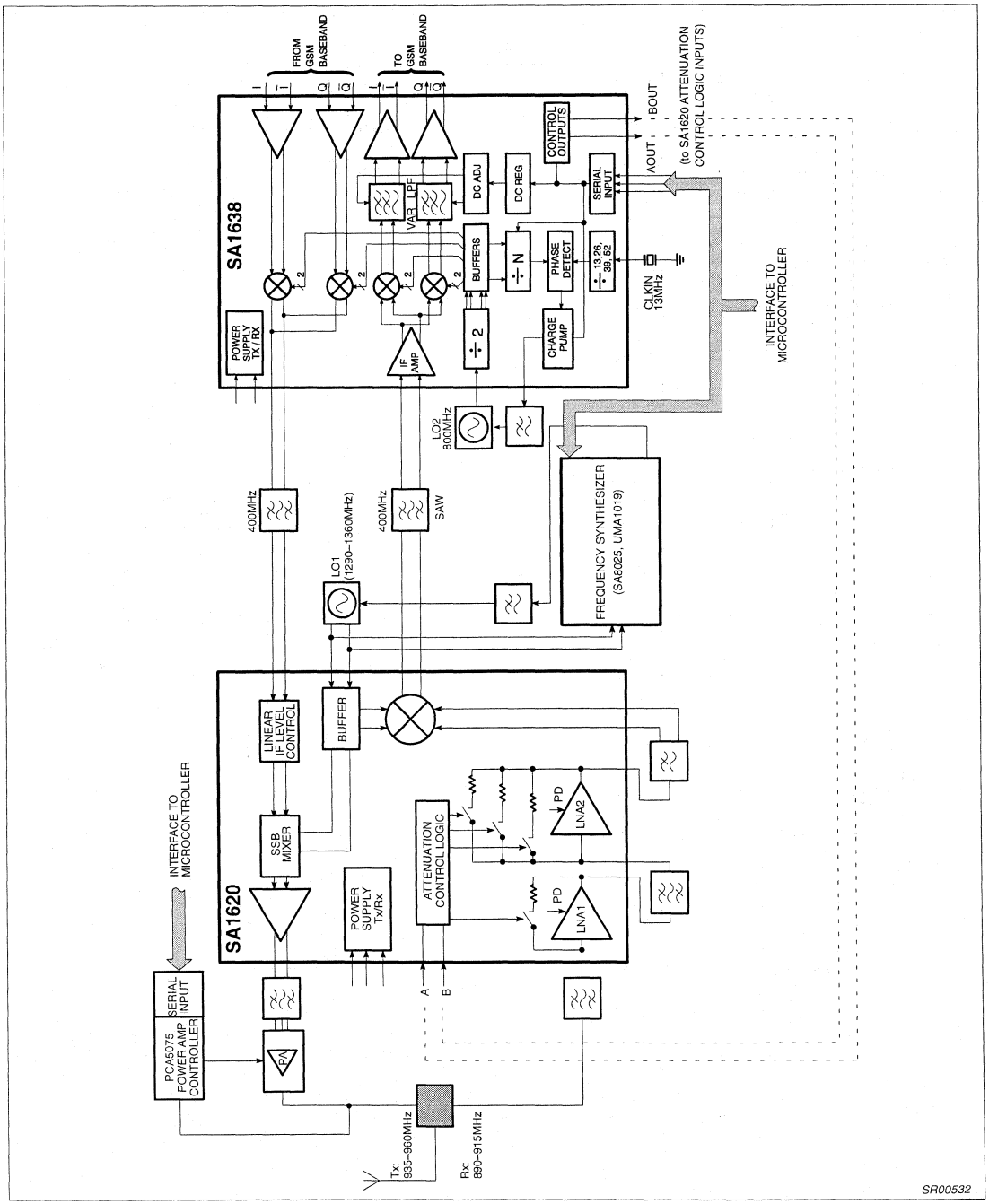


Figure 9. SA1620 / SA1638 System Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

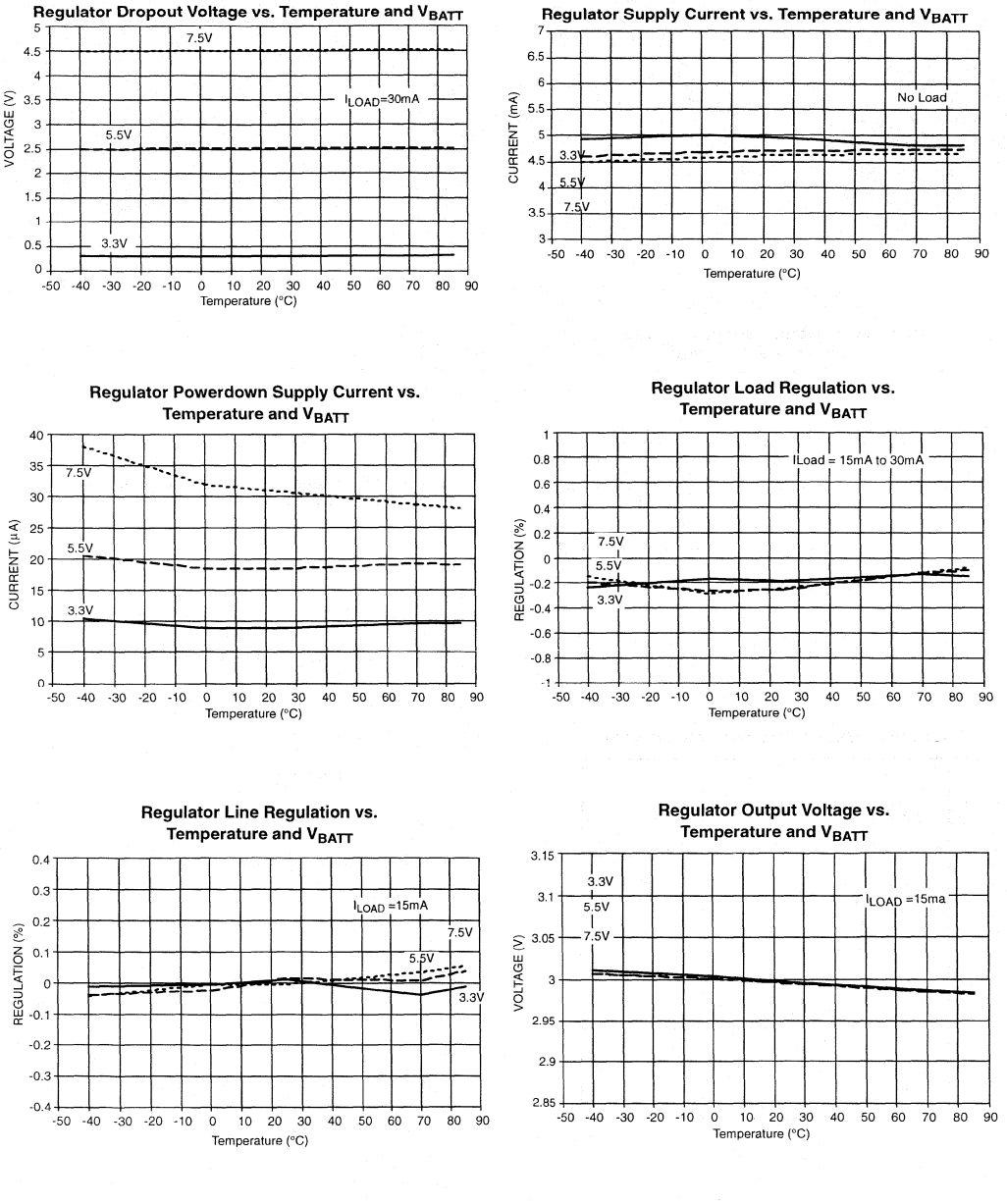
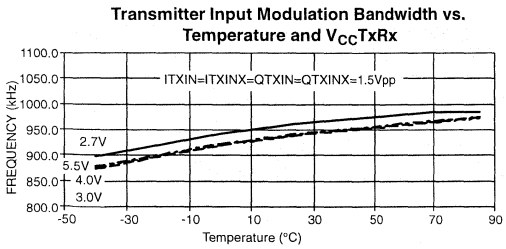
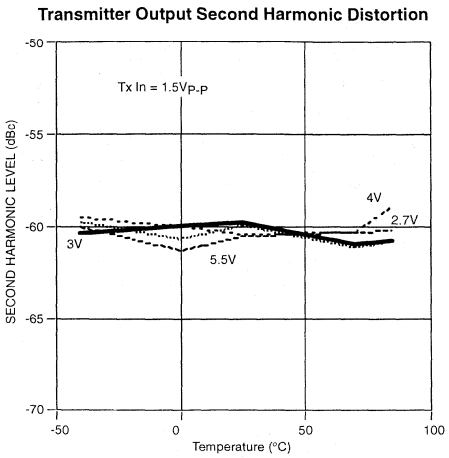
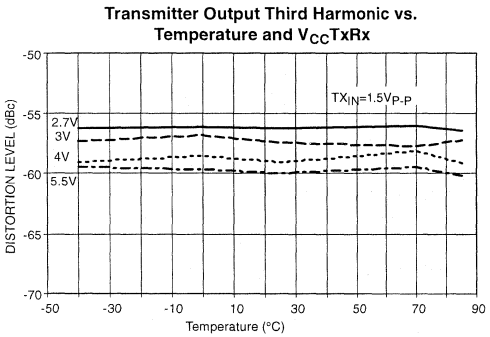


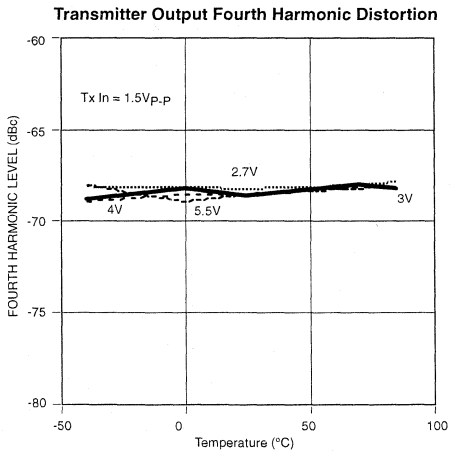
Figure 10. Typical Performance Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (continued)









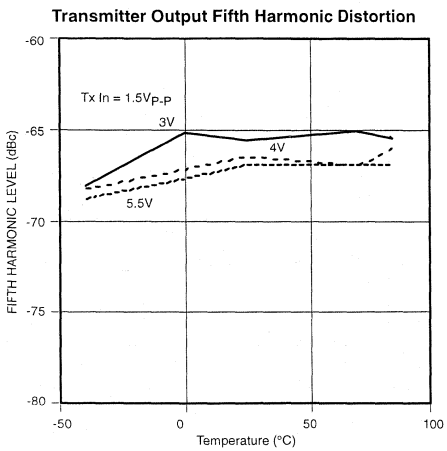


Figure 11. Typical Performance Characteristics (continued)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

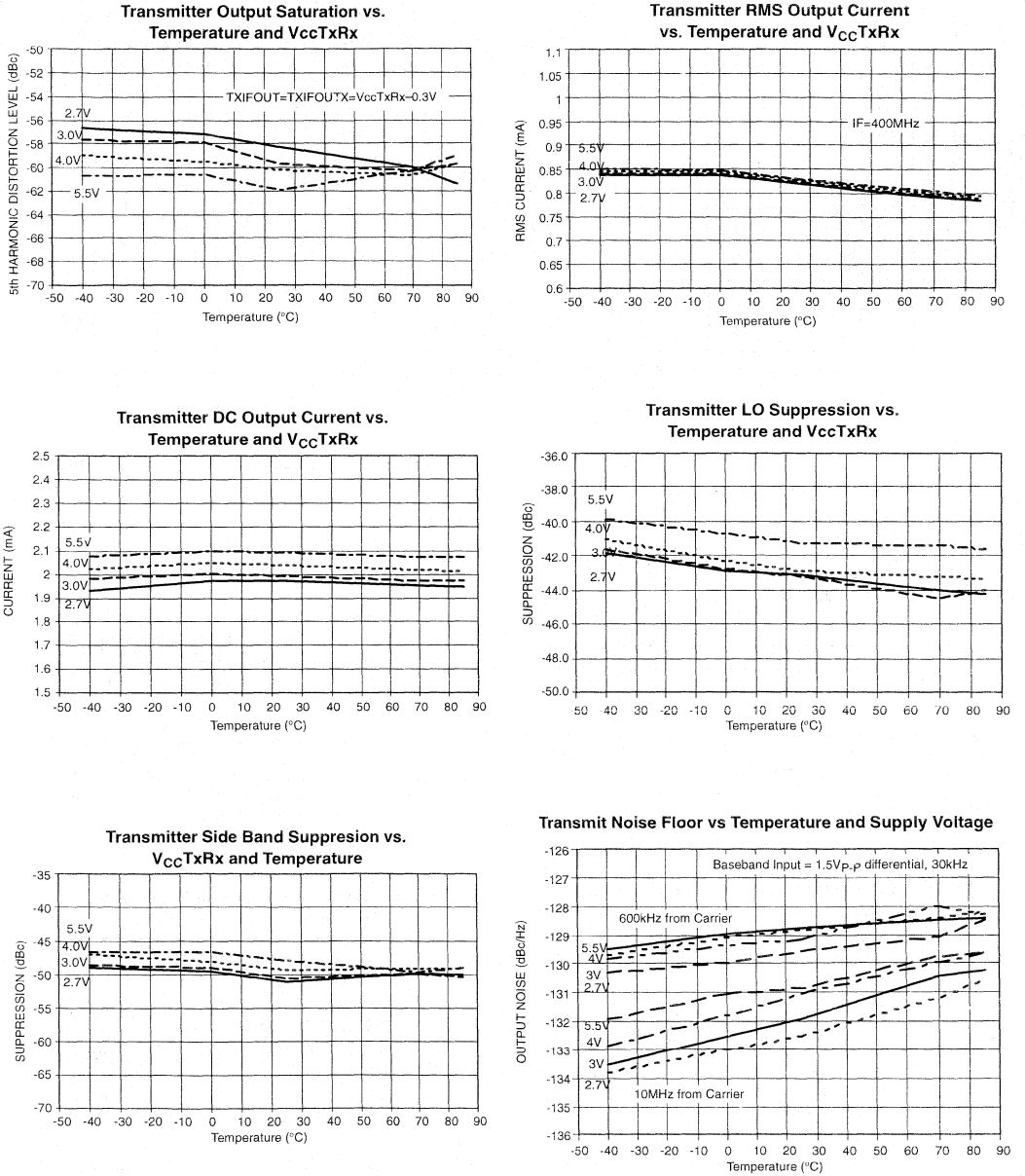
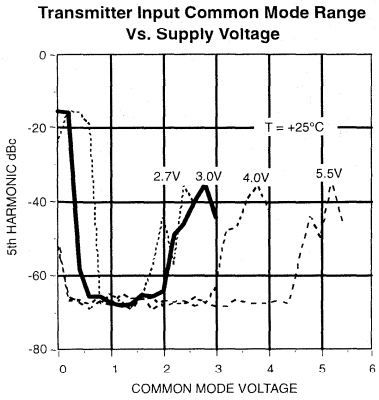
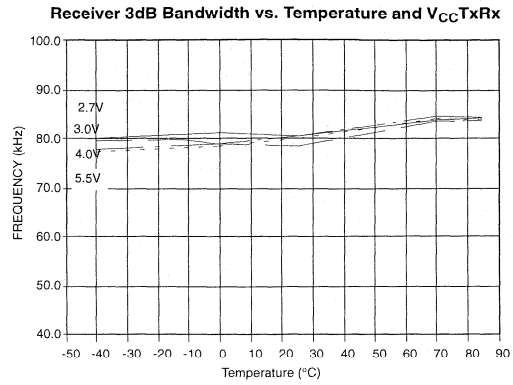
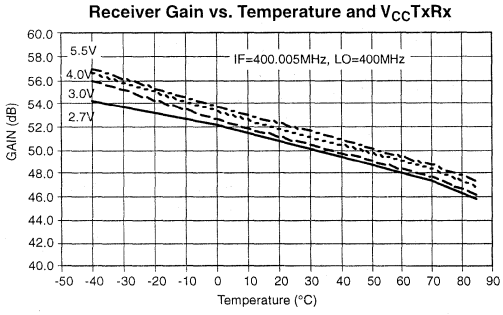


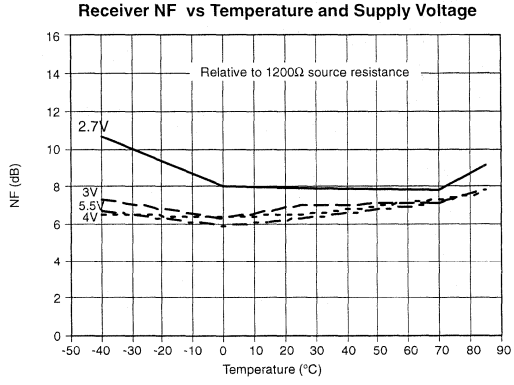
Figure 12. Typical Performance Characteristics (continued)

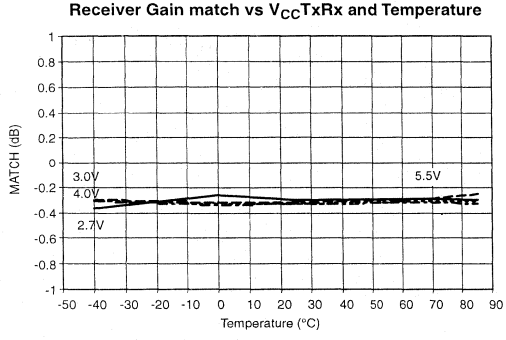
TYPICAL PERFORMANCE CHARACTERISTICS (continued)











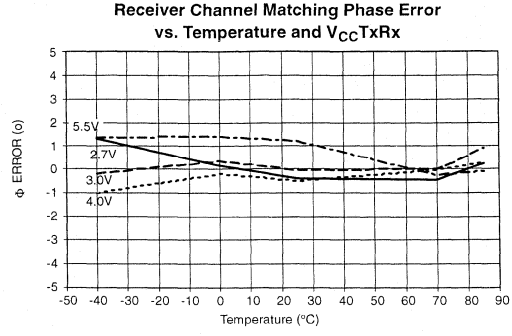


Figure 13. Typical Performance Characteristics (continued)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

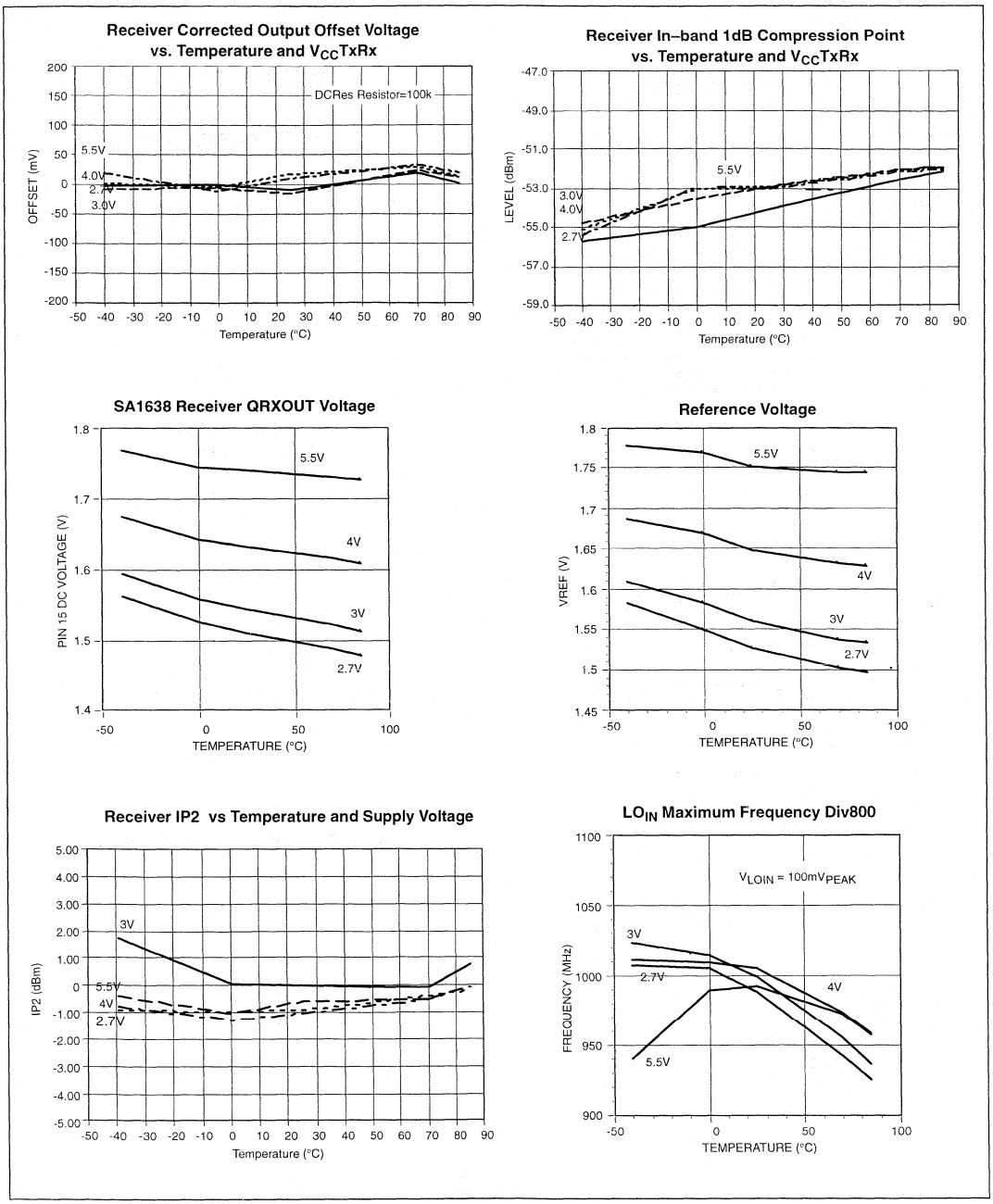


Figure 14. Typical Performance Characteristics (continued)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

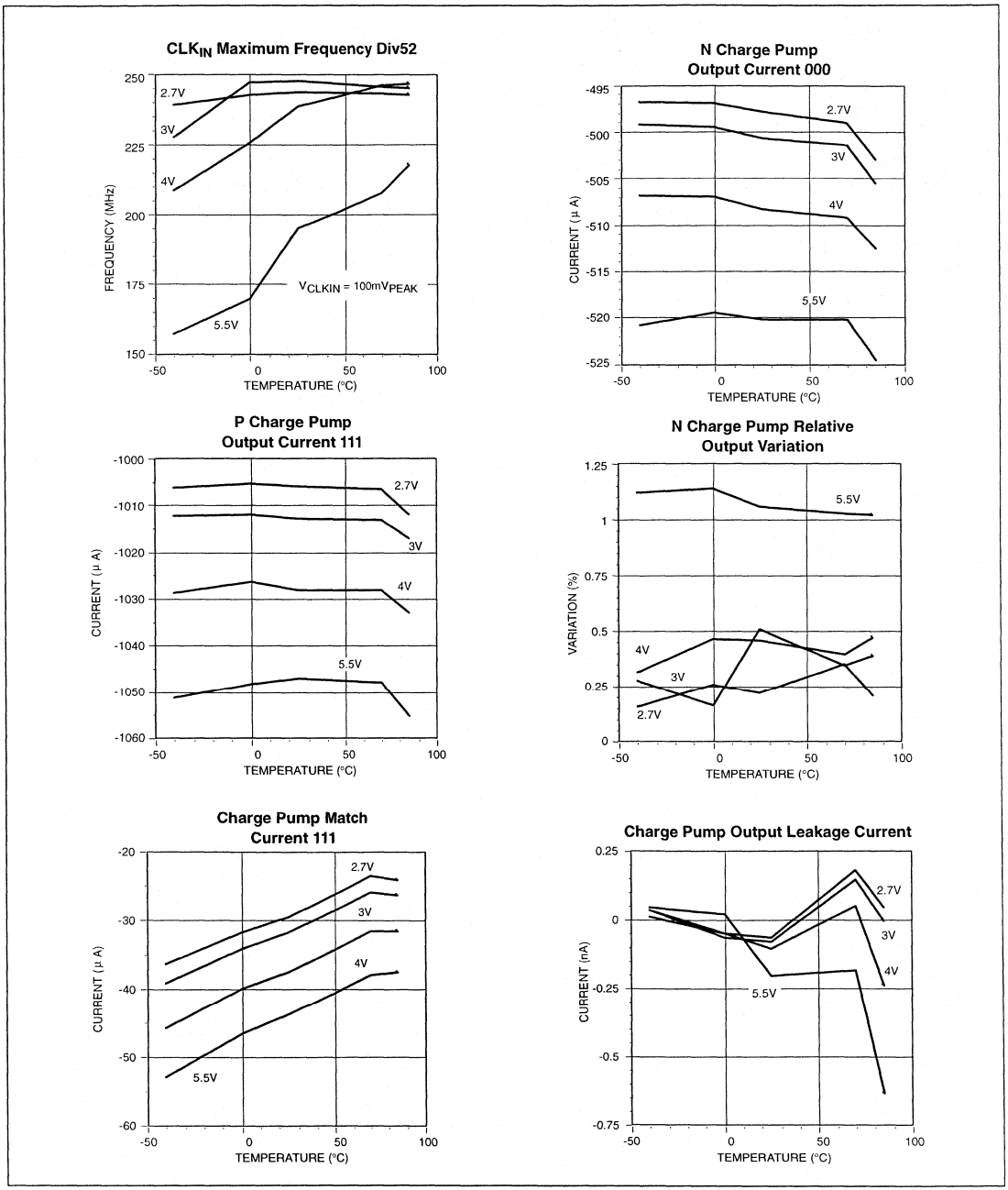


Figure 15. Typical Performance Characteristics (continued)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

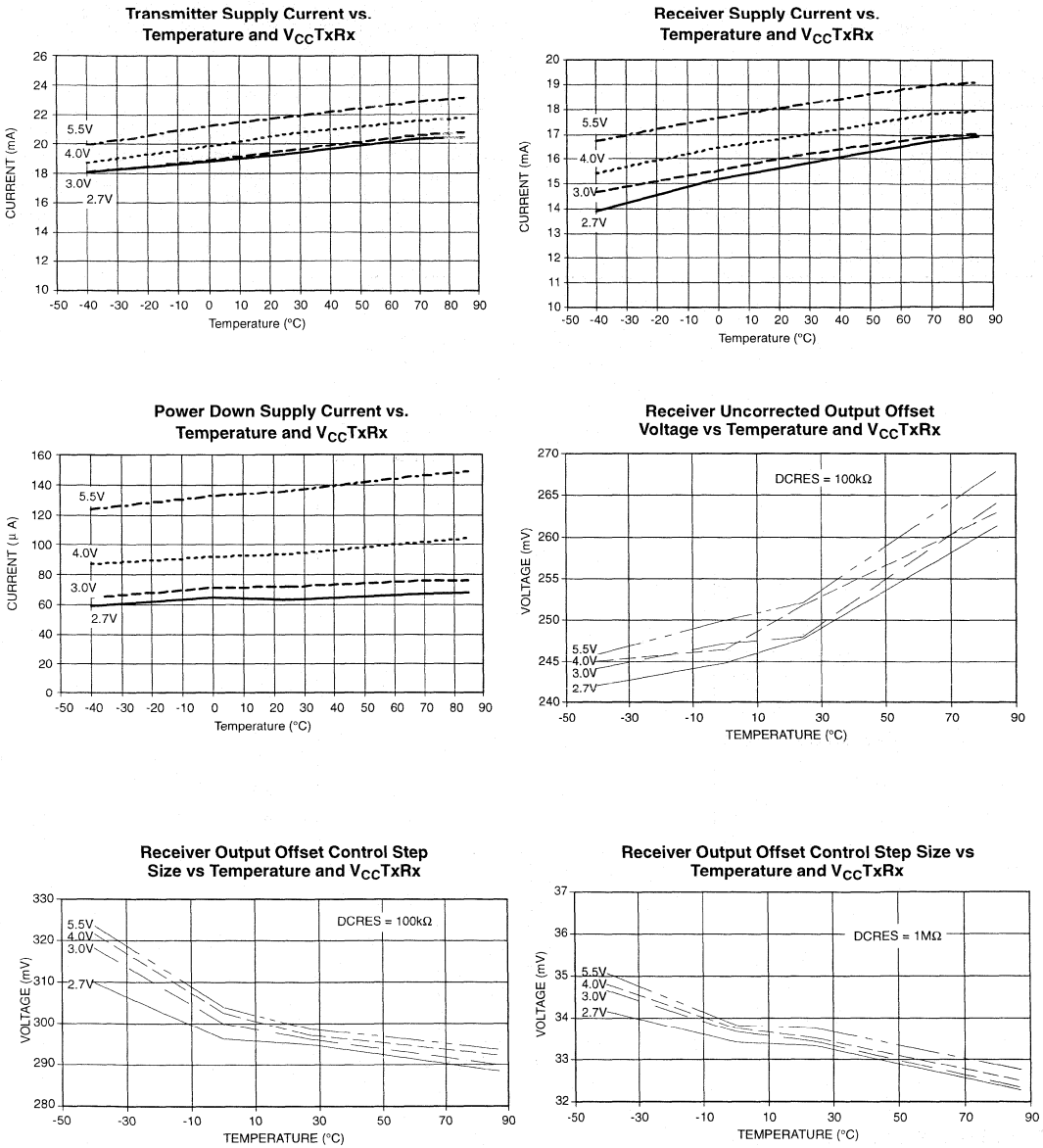


Figure 16. Typical Performance Characteristics (continued)

PCS/Cellular dual–band RF front–end SA1920

DESCRIPTION

The SA1920 is an integrated dual–band RF front–end circuit for cellular phones operating in dual–mode (analog and digital) in the 800 MHz band (Low–band) and single–mode (digital) in the PCS–1900 MHz (High–band).

Low Band	High Band
AMPS/DAMPS 800 MHz	"DAMPS" PCS–1900

For each application, the principal functions of the circuit are:

–Low noise amplifier

–RF mixer (Image Rejection Configuration for High–band)

–IF amplifier

The circuits for both bands shall be separated (i.e., unique RF inputs, LNAs, inter–stage filters, mixers, and IF amplifiers) with common control circuitry. The SA1920 has six dedicated control logic pins: High–band/Low–band Selection, Synthesizer On, Receiver On, Transmitter On, Strong Signal Indication, and Frequency Doubler On.

GENERAL

The SA1920 chip shall be delivered in a plastic surface mount package, LQFP–48. The maximum distance from the highest pin to the seating plane should be 0.1 mm. The seating plane is determined by the three lowest pin tips.

PIN CONFIGURATION

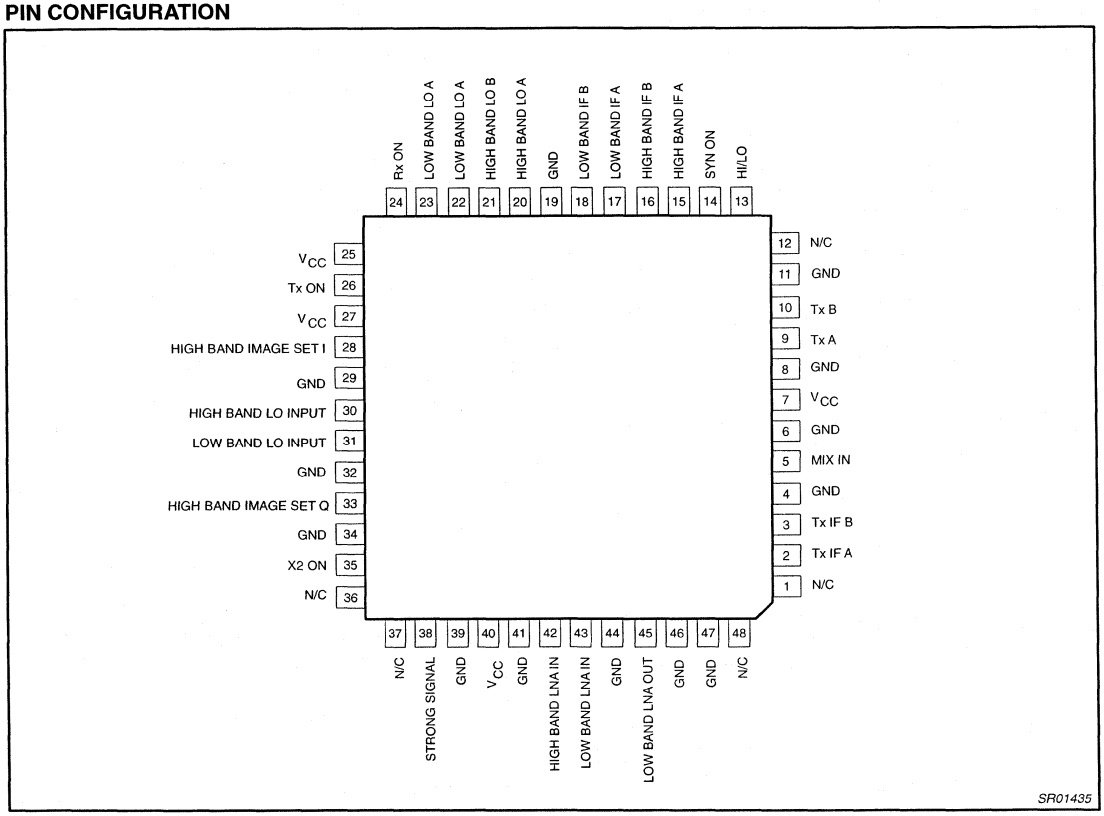


Figure 1. Pin Configuration

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SA1920	LQFP48	Plastic low profile quad flat package; 48 leads; body 7x7x1.4 mm	SOT313-2

PIN DESCRIPTIONS

PIN NO.	PIN NAME	DESCRIPTION
1	N/C	No Connection
2	Tx IF A	Transmit IF A
3	Tx IF B	Transmit IF B
4	GND	Ground
5	MIX IN	Low Band Mixer Input
6	GND	Ground
7	V_{CC}	V_{CC}
8	GND	Ground
9	Tx A	Transmit Signal A
10	Tx B	Transmit Signal B
11	GND	Ground
12	N/C	No Connection
13	HI/LO	High Band/Low Band Control
14	SYN ON	LO Buffer Power Control
15	HIGH BAND IF A	High Band IF A
16	HIGH BAND IF B	High Band IF B
17	LOW BAND IF A	Low Band IF A
18	LOW BAND IF B	Low Band IF B
19	GND	Ground
20	HIGH BAND LO A	High Band LO Output
21	HIGH BAND LO B	High Band LO Output
22	LOW BAND LO A	Low Band LO Output
23	LOW BAND LO B	Low Band LO Output
24	Rx ON	LNA/Mixer Power Control
25	V_{CC}	V_{CC}
26	Tx ON	Tx Mixer/Driver Power
27	V_{CC}	V_{CC}
28	HIGH BAND IMAGE SET I	High Band Image Set I
29	GND	Ground
30	HIGH BAND LO INPUT	High Band LO Connection
31	LOW BAND LO INPUT	Low Band LO Connection
32	GND	Ground
33	HIGH BAND IMAGE SET Q	High Band Image Set Q
34	GND	Ground
35	X2 ON	Freq. Doubler Power Control
36	N/C	No Connection
37	N/C	No Connection
38	STRONG SIGNAL	Strong Signal Detection
39	GND	Ground
40	V_{CC}	V_{CC}
41	GND	Ground
42	HIGH BAND LNA IN	High Band LNA Input
43	LOW BAND LNA IN	Low Band LNA Input
44	GND	Ground
45	LOW BAND LNA OUT	Low Band LNA Output
46	GND	Ground
47	GND	Ground
48	N/C	No Connection

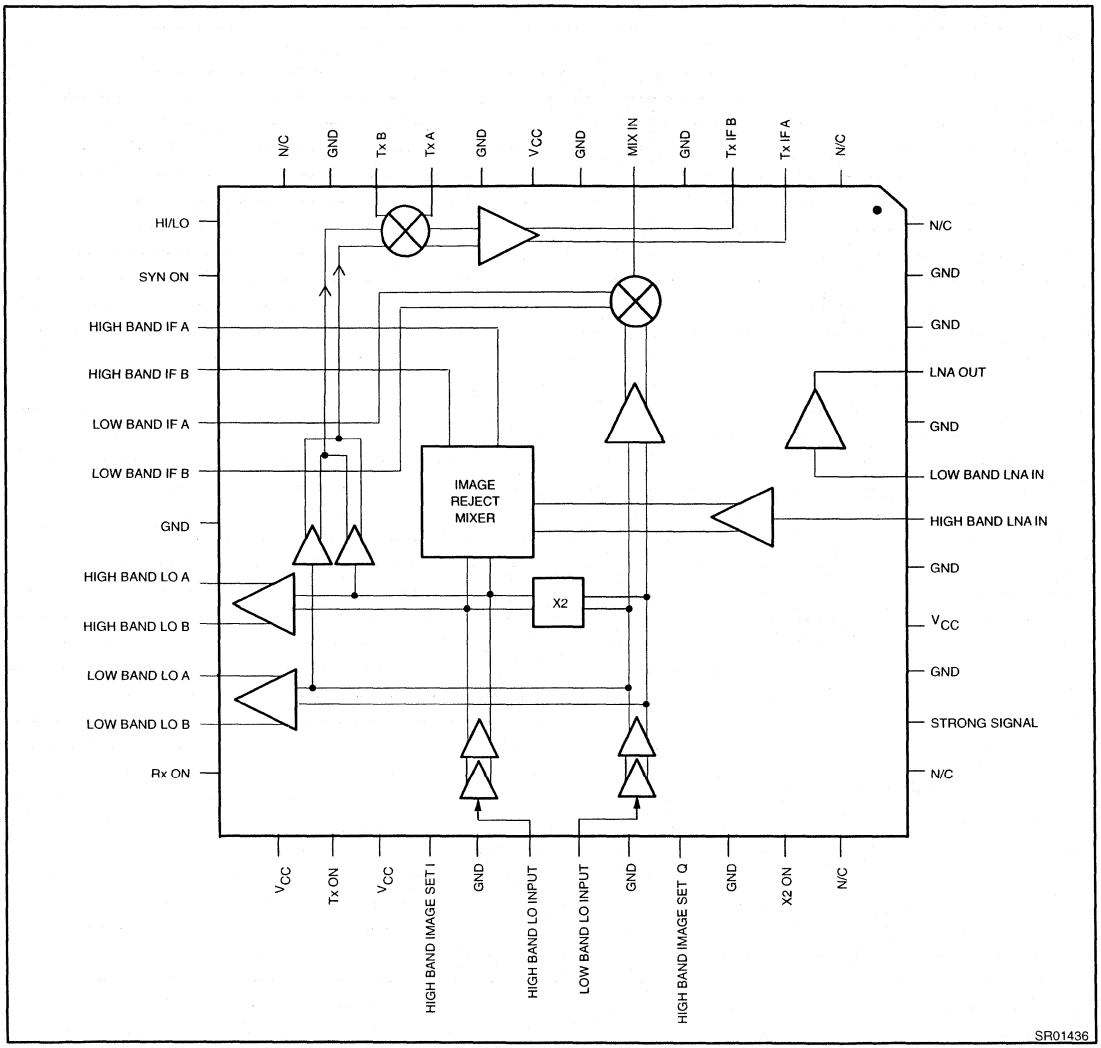


Figure 2. Block Diagram

NOTES:

1. RF inputs are specified as single–ended. The IF and LO outputs are differential.

POWER DOWN CONTROL

For **Applications Not Using a Frequency Doubler**, each state is defined as follows:

		DOUBLER	LO BUFFER		LNA		MIXER		T_X MIXER DRIVER	
Control State (Hi/Lo, Syn On, Rx On, Tx On, Strong Signal, X2 ON)			High Band	Low Band	High Band	Low Band	High Band	Low Band	High Band	Low Band
x000xx	Sleep	Off	Off	Off	Off	Off	Off	Off	Off	Off
010000	Low–Band LO Buffer on	Off	Off	On	Off	Off	Off	Off	Off	Off
011000	Low–Band Receive Normal	Off	Off	On	Off	On	Off	On	Off	Off
011010	Low–Band receive Strong Signal	Off	Off	On	Off	Off	Off	On	Off	Off
011100	Low–Band Transmit (Analog)	Off	Off	On	Off	On High Bias	Off	On	Off	On
010100	N/A	Off	Off	On	Off	Off	Off	Off	Off	On
110000	High–Band LO Buffer On	Off	On	Off	Off	Off	Off	Off	Off	Off
111000	High–Band Receive Normal	Off	On	Off	On	Off	On	Off	Off	Off
111010	High–Band Receive Strong Signal	Off	On	Off	Off	Off	On	Off	Off	Off
110100	N/A	Off	On	Off	Off	Off	Off	Off	On	Off

For **Applications Using a Frequency Doubler**, each state is defined as follows:

		DOUBLER	LO BUFFER		LNA		MIXER		T_X MIXER DRIVER	
Control State (Hi/Lo, Syn On, Rx On, Tx On, Strong Signal, X2 ON)			High Band	Low Band	High Band	Low Band	High Band	Low Band	High Band	Low Band
x000xx	Sleep	Off	Off	Off	Off	Off	Off	Off	Off	Off
010000	Transmit (Low and High Band)	Off	Off	On	Off	Off	Off	Off	Off	Off
011000	Low–Band Receive Normal	Off	Off	On	Off	On	Off	On	Off	Off
011010	Low–Band Receive Strong Signal	Off	Off	On	Off	Off	Off	On	Off	Off
011110	Low–Band Transmit (Analog only)	Off	Off	On	Off	On High Bias	Off	On	Off	Off
010100	Low–Band Transmit (GSM)	Off	Off	On	Off	Off	Off	Off	Off	On
010001	Transmit (Low and High Band)	On	Off	On	Off	Off	Off	Off	Off	Off
011001	Low–Band Receive Normal	On	Off	On	Off	On	Off	On	Off	Off
011011	Low–Band Receive Strong Signal	On	Off	On	Off	Off	Off	On	Off	Off
011111	Low–Band Transmit(Analog only)	On	Off	On	Off	On High Bias	Off	On	Off	Off
111001	High–Band Receive Normal	On	Off	On	On	Off	On	Off	Off	Off
111011	High–Band Receive Strong Signal	On	Off	On	Off	Off	On	Off	Off	Off
110101	High–Band Transmit (GSM)	On	Off	On	Off	Off	Off	Off	On	Off

NOTE:
"0" is low logic state; "1" is high logic state.

ABSOLUTE MAXIMUM RATINGS

QUANTITY	SYMBOL	VALUE	UNIT
Input supply voltage at pin XX	V_{CC}	4.75	V
Power dissipation	P_D	150	mW
Input power at all ports	P_{IN}	+20	dBm
Operating temperature range (pin temp)	T_O	–40 to+85	°C
Storage temperature range	T_{srg}	–65 to +125	°C

DC ELECTRICAL

CHARACTERISTICS

Unless otherwise specified, all Input/Output ports are single–ended.

DC PARAMETERS

V_{CC} = +3.75, T_A = –40 to +85°C unless otherwise noted

QUANTITY	CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
DC Supply voltage		V_{CC}	3.6	3.75	3.9	V
Current Consumption: Sleep Mode	X000XX	I_{CC}			0.100	mA
Low Band Receive Normal	011000	I_{CC}		11.3		mA
Low Band Receive Strong	011010	I_{CC}		8.4		mA
Low Band Transmit (Analog)	011110	I_{CC}		16.7		mA
Low Band Transmit (GSM)	010100	I_{CC}		15.7		mA
High Band Receive Normal	111000	I_{CC}		41.1		mA
High Band Receive Strong	111010	I_{CC}		37.3		mA
High Band Transmit (GSM)	110100	I_{CC}		21.3		mA
Frequency Doubler				8.8		mA
Logic Low Input			0		0.5	V
Logic High Input			1.9		4.0	V

AC ELECTRICAL CHARACTERISTICS

Low–Band, Dual Mode of Operation

All specifications apply for an IF output terminated into a 1kΩ load.
All specifications are over the temperature range of –40 to +85°C.

PARAMETERS	MIN.	TYP	MAX	UNITS	NOTES
RF Input Frequency Range	869		960	MHz	
IF Frequency		110.52		MHz	
LO Frequency	910		1060	MHz	
Power Gain	20.0		24.0	dB	
Power Gain Reduction (Strong Signal Mode–LNA Off)	15	25	45	dB	
Noise Figure			4.5	dB	
Noise Figure T_A=+15 to +45°C			4.0	dB	
LNA Gain		16		dB	
LNA IIP3		–6		dBm	
LNA Noise Figure		1.8		dB	
Mixer Gain		10		dB	
Mixer IIP3		5		dBm	
Mixer Noise Figure		10.5		dB	
Input Impedance, RF Port		50		Ω	
Output Impedance, LNA		50		Ω	
Input Impedance, Mixer		50		Ω	
Return Loss at LNA and Mixer Inputs			–10	dB	
Return Loss at LNA Output			–10	dB	
LO leakage at RF Port			–27	dBm	4
1 dB RF Input Compression Point (filtered)		–14		dBm	2
1 dB RF Input Compression Point (unfiltered)		–25		dBm	1
IP3 (3RD Order Intermodulation Product) Referred to the RF Input Port T_A=+15 to +45°C		–9		dBm	1,2
LO Input Power	–7	–5	–3	dBm	3
Turn ON/OFF Time			500	µsec	

NOTES:
1. The jamming signal will be inside the pass–band of the inter–stage filter.
2. In analog mode, T_X is on (Δf=–45 MHz). The inter–stage filter shall provide 20 dB of rejection.
3. The mixer will be run with an external VCO for the LO drive.
4. With external oscillator.

Low–Band LO Buffer

All specifications are over the temperature range of –40 to +85°C

PARAMETERS		MIN.	TYP.	MAX.	UNITS	NOTES
LO Frequency Range		900		1060	MHz	1
Output Power		–11		–8	dBm	
Differential Output Impedance			100		Ω	
Harmonic Content				–20	dBc	
Input Power		–7	–5	–3	dBm	
Input Impedance			50		Ω	
Turn On/Off Time				30	µsec	

NOTES:
1. Maximum 75 MHz in a specific application (Phase–locked); however, the buffer must be capable of accommodating a capture range from 900 MHz to 1100 MHz.

High–Band, Single Mode of Operation
LNA and Image Reject Mixer

All specifications apply for an IF output terminated into a 1kΩ load.
All specifications are over the temperature range of –40 to +85°C.

PARAMETERS	MIN.	TYP.	MAX.	UNITS	NOTES
RF Input Frequency Range	1930		1990	MHz	
IF Frequency		110.52		MHz	
LO Frequency	2030		2110	MHz	
Power Gain	20		24	dB	1
Power Gain Reduction (Strong Signal Mode – LNA Off)	15	25	60	dB	
Noise Figure			5.5	dB	
Noise Figure T_A=+15 to +45°C		4.5		dB	
Input Impedance, RF Port		50		Ω	
Return Loss at Inputs			–10	dB	
LO leakage at RF Port			–27	dBm	4
1 dB RF Input Compression Point		–24		dBm	2
IP3 (3RD Order Intermodulation Product) Referred to the RF Input Port T_A=+15 to +45°C		–12		dBm	2
(2 x LO) – (2 x RF) Spur Performance –50 dBm IN Referred to RF Input Port Measure at LO = 2040 MHz and RF = 1985 MHz		–67		dBc	2
(3 x LO) – (3 x RF) Spur Performance. –50 dBm IN Referred to RF Input Port. Measure at LO = 2040 MHz and RF = 2003 MHz.	–65			dBc	2
Image rejection, $f_{RX}+2f_{IF}$ or $f_{RX}-2f_{IF}$ Referred to the RF Input Port	30	35		dB	
LO Input Power	–7	–5	–3	dBm	3
Turn ON/OFF Time			30	µsec	

NOTES:
1. Performance shall be maintained when used with a single–endedRF input configuration.
2. The jamming signal will be inside the input frequency range.
3. The mixer will be run with an external VCO.
4. With an external oscillator.

High–Band LO Buffer

All specifications are over the temperature range of –40 to +85°C.

PARAMETERS	MIN.	TYP.	MAX.	UNITS	NOTES
VCO Frequency Range	2030		2110	MHz	1
Output Power (differential)	–11		–8	dBm	
Differential Output Impedance		100		Ω	
Harmonic Content			–20	dBc	
Input Power	–7	–5	–3	dBm	
Input Impedance		50		Ω	
Turn On/Off Time			30	µsec	

NOTES:
1. Maximum 60 MHz in a specific application (Phase–locked); however, the buffer must be capable of accommodating a capture range from 2000 MHz to 2140 MHz.

Frequency Doubler

All specifications are over the temperature range of –40 to +85°C.

PARAMETERS	MIN.	TYP.	MAX.	UNITS	NOTES
Output Frequency Range	2030		2110	MHz	
Output Power	–11		–8	dBm	
Differential Output Impedance		100		Ω	
Harmonic Content (3F, 4F, etc.)			–20	dBc	
Subharmonic Content (F_i)			–20	dBc	
Non–Harmonic Content			–80	dBc	
Turn On/Off Time			30	µsec	
Phase Noise Degradation, Δ f = 30kHz		6		dB	

Transmit Section

All specifications are over the temperature range of –40 to +85°C.

PARAMETERS	MIN.	TYP.	MAX.	UNITS	NOTES
T_X Mixer Input Frequency	824		1910	MHz	
T_X RF Input Impedance, Balanced		200		Ω	
Return Loss at Input		–10		dB	
T_X Mixer Output Frequency	70		200	MHz	
T_X IF Load Impedance		1000		Ω	
Maximum T_X IF Load Capacitance			2	pF	
Conversion Power Gain		17		dB	1
1 dB Input Compression Point		–17		dBm	
IIP2		20		dBm	
IIP3		–9		dBm	
Noise Figure (double sideband)		10		dB	
Reverse Isolation T_{XIN}–LO_{IN}	40			dB	
Isolation LO_{IN}–T_{XIN}	40			dB	

NOTES:
1. From 200Ω input to a 1kΩ output.

Satellite/Cellular dual–band RF front–end SA1921

DESCRIPTION

The SA1921 is an integrated dual–band RF front–end circuit for cellular phones operating in the 900 MHz band and 1550 MHz band.

Low Band	High Band
GSM 900 MHz	Satellite 1550 MHz

For each application, the principal functions of the circuit are:

–Low noise amplifier

–RF mixer (Image Rejection Configuration for High–band)

–IF amplifier

The circuits for both bands shall be separated (i.e., unique RF inputs, LNAs, inter–stage filters, mixers, and IF amplifiers) with common control circuitry. The SA1921 has six dedicated control logic pins: High–band/Low–band Selection, Synthesizer On, Receiver On, Transmitter On, Strong Signal Indication, and Frequency Doubler On.

GENERAL

The SA1921 chip shall be delivered in a plastic surface mount package, LQFP–48. The maximum distance from the highest pin to the seating plane should be 0.1 mm. The seating plane is determined by the three lowest pin tips.

PIN CONFIGURATION

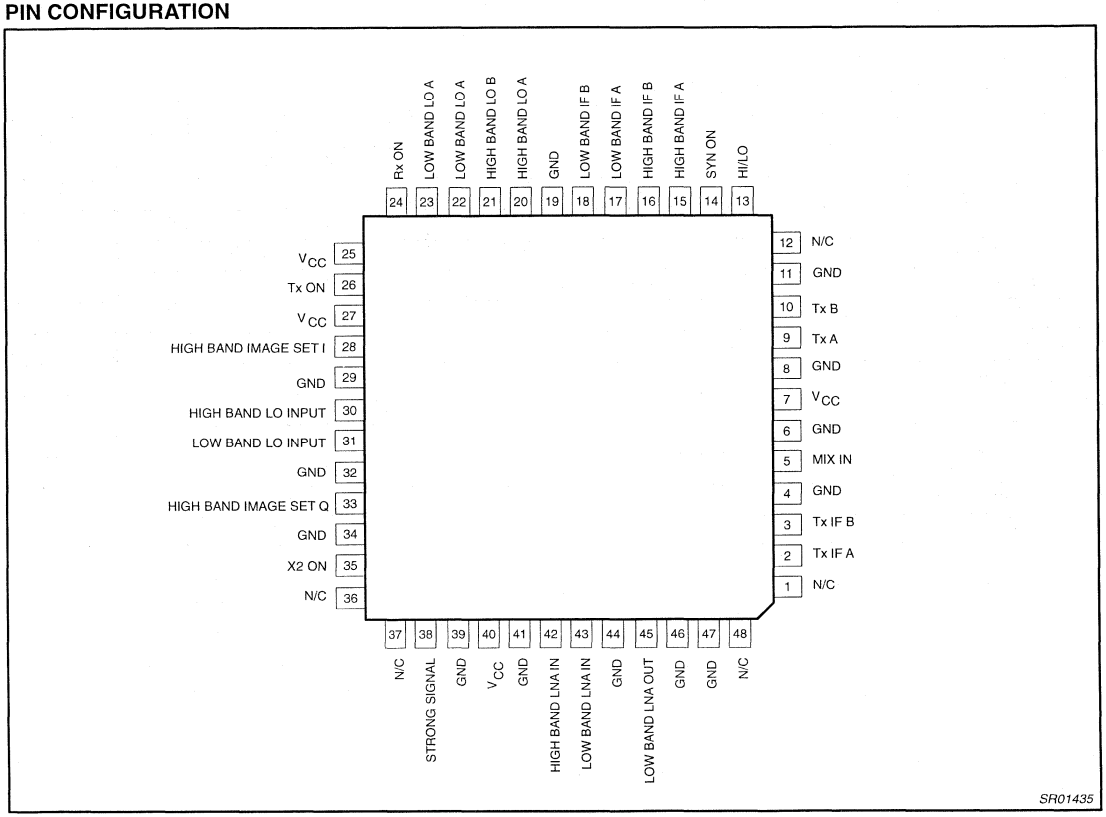


Figure 1. Pin Configuration

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SA1921	LQFP48	Plastic low profile quad flat package; 48 leads; body 7x7x1.4 mm	SOT313-2

PIN DESCRIPTIONS

PIN NO.	PIN NAME	DESCRIPTION
1	N/C	No Connection
2	Tx IF A	Transmit IF A
3	Tx IF B	Transmit IF B
4	GND	Ground
5	MIX IN	Low Band Mixer Input
6	GND	Ground
7	V_{CC}	V_{CC}
8	GND	Ground
9	Tx A	Transmit Signal A
10	Tx B	Transmit Signal B
11	GND	Ground
12	N/C	No Connection
13	HI/LO	High Band/Low Band Control
14	SYN ON	LO Buffer Power Control
15	HIGH BAND IF A	High Band IF A
16	HIGH BAND IF B	High Band IF B
17	LOW BAND IF A	Low Band IF A
18	LOW BAND IF B	Low Band IF B
19	GND	Ground
20	HIGH BAND LO A	High Band LO Output
21	HIGH BAND LO B	High Band LO Output
22	LOW BAND LO A	Low Band LO Output
23	LOW BAND LO B	Low Band LO Output
24	Rx ON	LNA/Mixer Power Control
25	V_{CC}	V_{CC}
26	Tx ON	Tx Mixer/Driver Power
27	V_{CC}	V_{CC}
28	HIGH BAND IMAGE SET I	High Band Image Set I
29	GND	Ground
30	HIGH BAND LO INPUT	High Band LO Connection
31	LOW BAND LO INPUT	Low Band LO Connection
32	GND	Ground
33	HIGH BAND IMAGE SET Q	High Band Image Set Q
34	GND	Ground
35	X2 ON	Freq. Doubler Power Control
36	N/C	No Connection
37	N/C	No Connection
38	STRONG SIGNAL	Strong Signal Detection
39	GND	Ground
40	V_{CC}	V_{CC}
41	GND	Ground
42	HIGH BAND LNA IN	High Band LNA Input
43	LOW BAND LNA IN	Low Band LNA Input
44	GND	Ground
45	LOW BAND LNA OUT	Low Band LNA Output
46	GND	Ground
47	GND	Ground
48	N/C	No Connection

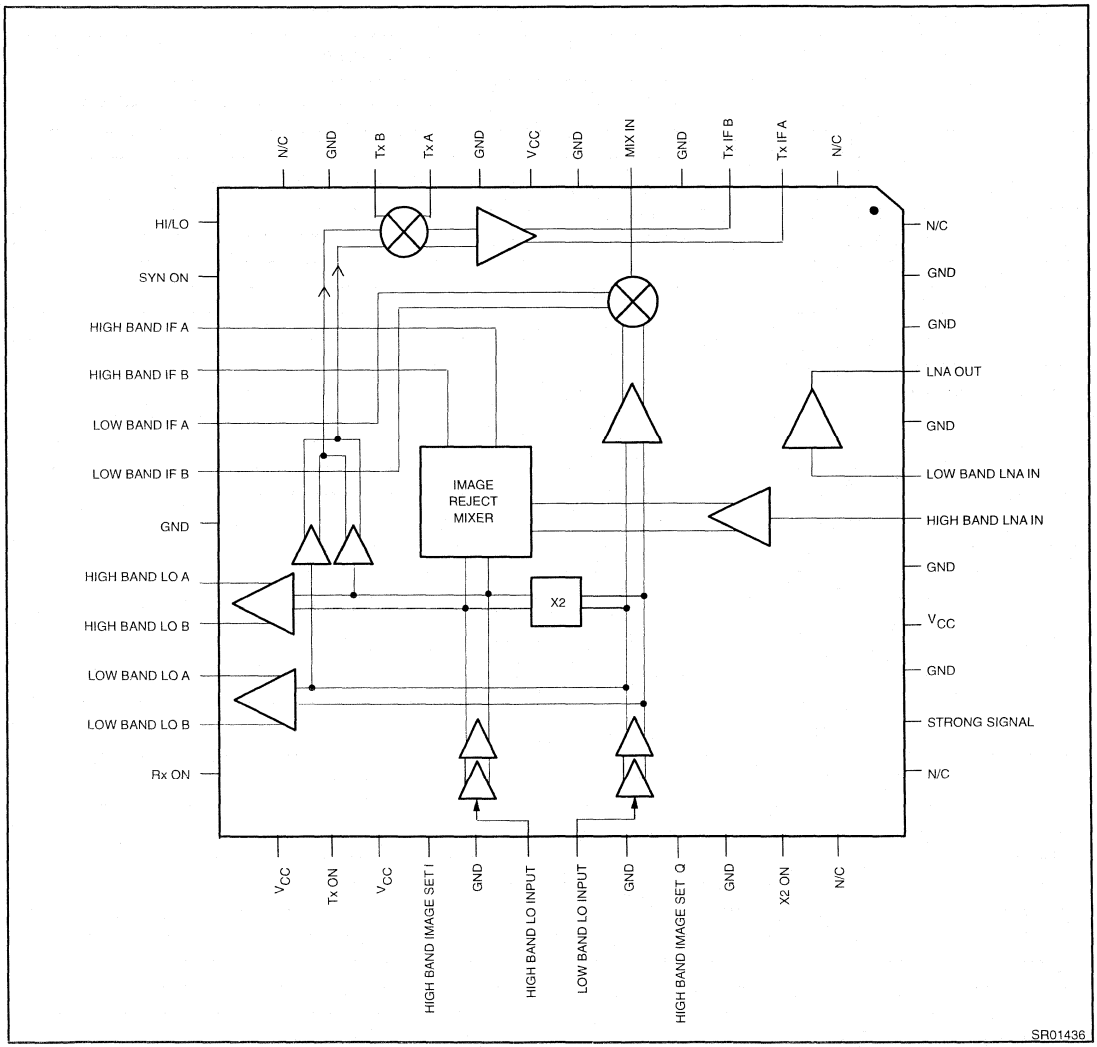


Figure 2. Block Diagram

NOTES:

1. RF inputs are specified as single–ended. The IF and LO outputs are differential.

POWER DOWN CONTROL

For **Applications Not Using a Frequency Doubler**, each state is defined as follows:

		DOUBLER	LO BUFFER		LNA		MIXER		T_X MIXER DRIVER	
Control State (Hi/Lo, Syn On, Rx On, Tx On, Strong Signal, X2 ON)			High Band	Low Band	High Band	Low Band	High Band	Low Band	High Band	Low Band
x000xx	Sleep	Off	Off	Off	Off	Off	Off	Off	Off	Off
010000	Low–Band LO Buffer on	Off	Off	On	Off	Off	Off	Off	Off	Off
011000	Low–Band Receive Normal	Off	Off	On	Off	On	Off	On	Off	Off
011010	Low–Band receive Strong Signal	Off	Off	On	Off	Off	Off	On	Off	Off
011100	Low–Band Transmit (Analog)	Off	Off	On	Off	On High Bias	Off	On	Off	On
010100	N/A	Off	Off	On	Off	Off	Off	Off	Off	On
110000	High–Band LO Buffer On	Off	On	Off	Off	Off	Off	Off	Off	Off
111000	High–Band Receive Normal	Off	On	Off	On	Off	On	Off	Off	Off
111010	High–Band Receive Strong Signal	Off	On	Off	Off	Off	On	Off	Off	Off
110100	N/A	Off	On	Off	Off	Off	Off	Off	On	Off

For **Applications Using a Frequency Doubler**, each state is defined as follows:

		DOUBLER	LO BUFFER		LNA		MIXER		T_X MIXER DRIVER	
Control State (Hi/Lo, Syn On, Rx On, Tx On, Strong Signal, X2 ON)			High Band	Low Band	High Band	Low Band	High Band	Low Band	High Band	Low Band
x000xx	Sleep	Off	Off	Off	Off	Off	Off	Off	Off	Off
010000	Transmit (Low and High Band)	Off	Off	On	Off	Off	Off	Off	Off	Off
011000	Low–Band Receive Normal	Off	Off	On	Off	On	Off	On	Off	Off
011010	Low–Band Receive Strong Signal	Off	Off	On	Off	Off	Off	On	Off	Off
011110	Low–Band Transmit (Analog only)	Off	Off	On	Off	On High Bias	Off	On	Off	Off
010100	Low–Band Transmit (GSM)	Off	Off	On	Off	Off	Off	Off	Off	On
010001	Transmit (Low and High Band)	On	Off	On	Off	Off	Off	Off	Off	Off
011001	Low–Band Receive Normal	On	Off	On	Off	On	Off	On	Off	Off
011011	Low–Band Receive Strong Signal	On	Off	On	Off	Off	Off	On	Off	Off
011111	Low–Band Transmit(Analog only)	On	Off	On	Off	On High Bias	Off	On	Off	Off
111001	High–Band Receive Normal	On	Off	On	On	Off	On	Off	Off	Off
111011	High–Band Receive Strong Signal	On	Off	On	Off	Off	On	Off	Off	Off
110101	High–Band Transmit (GSM)	On	Off	On	Off	Off	Off	Off	On	Off

NOTE:
"0" is low logic state; "1" is high logic state.

ABSOLUTE MAXIMUM RATINGS

QUANTITY	SYMBOL	VALUE	UNIT
Input supply voltage at pin XX	V_{CC}	4.75	V
Power dissipation	P_D	150	mW
Input power at all ports	P_{IN}	+20	dBm
Operating temperature range (pin temp)	T_O	–40 to+85	°C
Storage temperature range	T_{srg}	–65 to +125	°C

DC ELECTRICAL

CHARACTERISTICS

Unless otherwise specified, all Input/Output ports are single–ended.

DC PARAMETERS

V_{CC} = +3.75, T_A = –40 to +85°C unless otherwise noted

QUANTITY	CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
DC Supply voltage		V_{CC}	3.6	3.75	3.9	V
Current Consumption: Sleep Mode	X000XX	I_{CC}			0.100	mA
Low Band Receive Normal	011000	I_{CC}		11.3		mA
Low Band Receive Strong	011010	I_{CC}		8.4		mA
Low Band Transmit (Analog)	011110	I_{CC}		16.7		mA
Low Band Transmit (GSM)	010100	I_{CC}		15.7		mA
High Band Receive Normal	111000	I_{CC}		38.6		mA
High Band Receive Strong	111010	I_{CC}		34.7		mA
High Band Transmit (GSM)	110100	I_{CC}		18.8		mA
Frequency Doubler				8.8		mA
Logic Low Input			0		0.5	V
Logic High Input			1.9		4.0	V

AC ELECTRICAL CHARACTERISTICS

Low–Band, Dual Mode of Operation

All specifications apply for an IF output terminated into a 1kΩ load.
All specifications are over the temperature range of –40 to +85°C.

PARAMETERS	MIN.	TYP	MAX	UNITS	NOTES
RF Input Frequency Range	935		960	MHz	
IF Frequency		163		MHz	
LO Frequency	772		998	MHz	
Power Gain	20.0		24.0	dB	
Power Gain Reduction (Strong Signal Mode–LNA Off)	15	25	45	dB	
Noise Figure			4.5	dB	
Noise Figure T_A=+15 to +45°C			4.0	dB	
LNA Gain		16		dB	
LNA IIP3		–6		dBm	
LNA Noise Figure		1.8		dB	
Mixer Gain		10		dB	
Mixer IIP3		5		dBm	
Mixer Noise Figure		10.5		dB	
Input Impedance, RF Port		50		Ω	
Output Impedance, LNA		50		Ω	
Input Impedance, Mixer		50		Ω	
Return Loss at LNA and Mixer Inputs			–10	dB	
Return Loss at LNA Output			–10	dB	
LO leakage at RF Port			–27	dBm	4
1 dB RF Input Compression Point (filtered)		–14		dBm	2
1 dB RF Input Compression Point (unfiltered)		–25		dBm	1
IP3 (3RD Order Intermodulation Product) Referred to the RF Input Port T_A=+15 to +45°C		–9		dBm	1,2
LO Input Power	–7	–5	–3	dBm	3
Turn ON/OFF Time			50	µsec	

NOTES:
1. The jamming signal will be inside the pass–band of the inter–stage filter.
2. In analog mode, T_X is on (Δf=–45 MHz). The inter–stage filter shall provide 20 dB of rejection.
3. The mixer will be run with an external VCO for the LO drive.
4. With external oscillator.

Low–Band LO Buffer

All specifications are over the temperature range of –40 to +85°C

PARAMETERS		MIN.	TYP.	MAX.	UNITS	NOTES
LO Frequency Range		750		1000	MHz	
Output Power		–11		–8	dBm	
Differential Output Impedance			100		Ω	
Harmonic Content				–20	dBc	
Input Power		–7	–5	–3	dBm	
Input Impedance			50		Ω	
Turn On/Off Time				30	µsec	

High–Band, Single Mode of Operation
LNA and Image Reject Mixer

All specifications apply for an IF output terminated into a 1kΩ load.
All specifications are over the temperature range of –40 to +85°C.

PARAMETERS	MIN.	TYP.	MAX.	UNITS	NOTES
RF Input Frequency Range	1525		1559	MHz	
IF Frequency		163		MHz	
LO Frequency	1688		1722	MHz	
Power Gain	20		24	dB	1
Power Gain Reduction (Strong Signal Mode – LNA Off)	15	25	60	dB	
Noise Figure			5.5	dB	
Noise Figure T_A=+15 to +45°C		4.5		dB	
Input Impedance, RF Port		50		Ω	
Return Loss at Inputs			–10	dB	
LO leakage at RF Port			–27	dBm	4
1 dB RF Input Compression Point		–24		dBm	2
IP3 (3RD Order Intermodulation Product) Referred to the RF Input Port T_A=+15 to +45°C		–12		dBm	2
(2 x LO) – (2 x RF) Spur Performance –50 dBm IN Referred to RF Input Port Measure at LO = 2040 MHz and RF = 1985 MHz		–67		dBc	2
(3 x LO) – (3 x RF) Spur Performance. –50 dBm IN Referred to RF Input Port. Measure at LO = 2040 MHz and RF = 2003 MHz.	–65			dBc	2
Image rejection, $f_{RX}+2f_{IF}$ or $f_{RX}-2f_{IF}$ Referred to the RF Input Port	30	35		dB	
LO Input Power	–7	–5	–3	dBm	3
Turn ON/OFF Time			30	µsec	

NOTES:
1. Performance shall be maintained when used with a single–endedRF input configuration.
2. The jamming signal will be inside the input frequency range.
3. The mixer will be run with an external VCO.
4. With an external oscillator.

High–Band LO Buffer

All specifications are over the temperature range of –40 to +85°C.

PARAMETERS	MIN.	TYP.	MAX.	UNITS	NOTES
VCO Frequency Range	1650		1750	MHz	
Output Power (differential)	–11		–8	dBm	
Differential Output Impedance		100		Ω	
Harmonic Content			–20	dBc	
Input Power	–7	–5	–3	dBm	
Input Impedance		50		Ω	
Turn On/Off Time			30	µsec	

Frequency Doubler

All specifications are over the temperature range of –40 to +85°C.

PARAMETERS	MIN.	TYP.	MAX.	UNITS	NOTES
Output Frequency Range	1650		1750	MHz	
Output Power	–11		–8	dBm	
Differential Output Impedance		100		Ω	
Harmonic Content (3F, 4F, etc.)			–20	dBc	
Subharmonic Content (F_i)			–20	dBc	
Non–Harmonic Content			–80	dBc	
Turn On/Off Time			30	μsec	
Phase Noise Degradation, Δ f = 30kHz		6		dB	

Transmit Section

All specifications are over the temperature range of –40 to +85°C.

PARAMETERS	MIN.	TYP.	MAX.	UNITS	NOTES
T_X Mixer Input Frequency	824		1660.5	MHz	
Tx Mixer LO Input Frequency	773		1725.5	MHz	
T_X RF Input Impedance, Balanced		200		Ω	
Return Loss at Input	–10			dB	
T_X Mixer Output Frequency	25		210	MHz	
T_X IF Load Impedance		1000		Ω	
Maximum T_X IF Load Capacitance			2	pF	
Conversion Power Gain		17		dB	1
1 dB Input Compression Point		–17		dBm	
IIP2		20		dBm	
IIP3		–9		dBm	
Noise Figure (double sideband)		10		dB	
Reverse Isolation T_{XIN}–LO_{IN}	40			dB	
Isolation LO_{IN}–T_{XIN}	40			dB	

NOTES:
1. From 200Ω input to a 1kΩ output.

2.45GHz RF power amplifier and T/R switch SA2410

DESCRIPTION

The SA2410 is a GaAs monolithic power amplifier with an integrated T/R switch designed to meet requirements for 802.11 (WLAN). The SA2410 uses an on–chip 4 GHz oscillator to generate the negative bias, thus eliminating the need for a negative supply. It operates from 3V to 5.5V and consumes 125 mA with an output power of 18.5 dB (typ). It is suitable for other 2.45 GHz ISM band applications.

FEATURES

- V_{CC}=3V–5.5V
- No negative bias needed
- I_{CC}=125mA (typ) @ 3.3V
- P_{OUT}=18.5 dB(typ)
  IM3<–30dBc
  IM5<–50dBc
- Gain=29dB (typ)
- Attenuation range=16dB (typ)
- LQFP–32 package

APPLICATIONS

- 802.11 WLAN
- 2.4–2.5 GHz ISM BAND

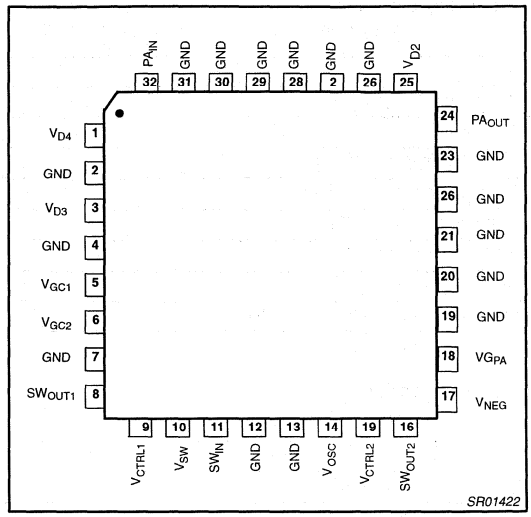


Figure 1. Pin Configuration

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
32–Pin Plastic Thin Quad Flat Package	–40° C+85°C	SA2410	SOT401–1

GENERAL SPECIFICATIONS

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T	Temperature		–40		+85	C
V_{CC}	Supply V		3		5.5	V
I_{CC}	Supply I	3.3 volts		125		mA
Power Amplifier						
f_{RF}	Frequency Range		2.4		2.5	GHz
IM3	IM3 2 tones		30			dBc
IM5	IM5 2 tones		50			dBc
T_{on}	Transmit power on	Including neg. supply			2	µs
T_{off}	Xmit power down				2	µs
Gain	Small signal gain			29		dB
P_{out}	Output power	IM3=30dBc IM5=50dBc 125mA@3.3 volts	17.5	18.5		dBm
Eff.	Efficiency			25		%
Δ Gt1	Gain variation with temp	–40 to +85°C		±3.5		dB
Δ Gt2	Gain variation with temp	0–70°C		±2.0		dB
Δ Gr	Ripple	2.45±0.05 GHz		±1		dB
Δ Gvd	Gain variation with supply	3.3 volts±0.3 V		0.5		dB

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Negative voltage supply						
t_{on}	Power on time		10		100	nS
	4 GHz spur	Xmit Mode		TBD		dBm
Linear Gain Control						
Symbol	**Parameter**	**Condition**	**Min**	**Typ**	**Max**	**Unit**
V_{GC}	Gain control voltage			TBD		Volt
C_{GC}	Input C at gain pin			TBD		pF
G_{CR}	Attenuation range			16		dB
Transmit/receive switch						
Symbol	**Parameter**	**Condition**	**Min**	**Typ**	**Max**	**Unit**
L_{tx}	Insertion loss T_x			1.3	2	dB
L_{rx}	Insertion loss R_x			1.3	2	dB
t_{sw}	Switch response time				400	nS
ISO_{PA}	Isolation switch to PA		30			dB
Z_{in}	Input impedance			50		Ω
Z_{out}	Output impedance			50		Ω
ISO_{SW}	Switch Isolation		17	19		dB

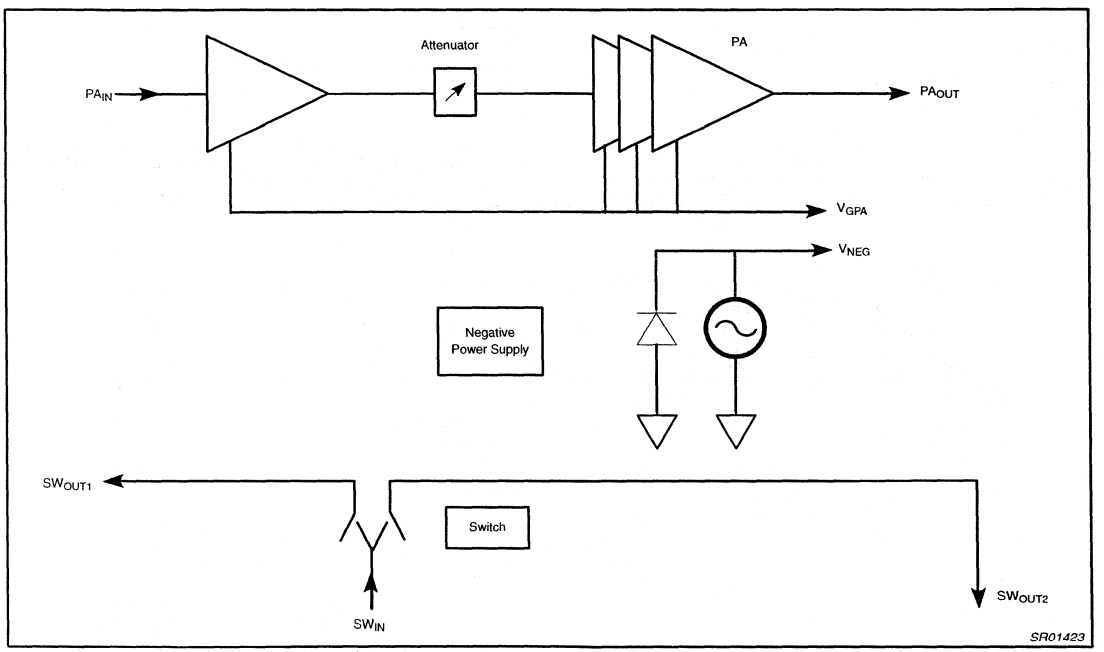


Figure 2. Block Diagram

Low voltage RF transceiver — 2.45 GHz SA2420

DESCRIPTION

The SA2420 transceiver is a combined low-noise amplifier, receive mixer, transmit mixer and LO buffer IC designed for high-performance low-power communication systems for 2.4-2.5GHz applications. The LNA has a 2.5dB noise figure at 2.45GHz with 14dB gain and an IP3 intercept of -3dBm at the input. The gain is stabilized by on-chip compensation to vary less than ±0.2dB over the -40 to +85°C temperature range. The wide-dynamic-range receive mixer has a 10.9dB noise figure and an input IP3 of +2.8dBm at 2.45GHz. The nominal current drawn from a single 3V supply is 37mA in transmit mode and 22mA in receive mode.

FEATURES

- Low current consumption: 37mA nominal transmit mode and 22mA nominal receive mode
- Fabricated on a high volume, rugged BiCMOS technology
- High system power gain: 22.5dB (LNA + Mixer) at 2.45GHz
- TSSOP24 package
- Excellent gain stability versus temperature and supply voltage
- -10dBm LO input power can be used to drive the mixer
- Operates with either full or half frequency LO
- Wide IF range: 50–500MHz

PIN CONFIGURATION

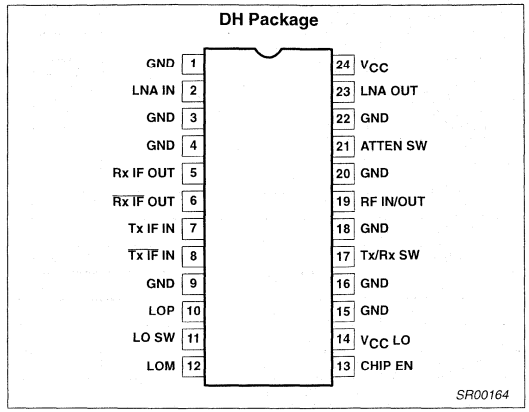


Figure 1. Pin Configuration

APPLICATIONS

- 2.45GHz WLAN front-end (802.11, ISM)

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
24-Pin Plastic Thin Shrink Small Outline Package (Surface-mount, TSSOP)	-40 to +85°C	SA2420DH	SOT355-1

BLOCK DIAGRAM

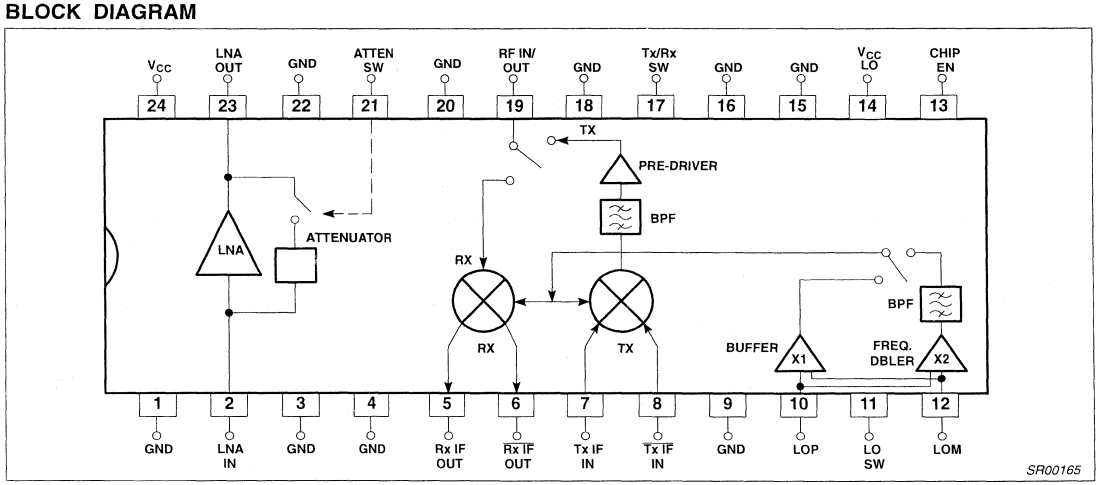


Figure 2. SA2420 Block Diagram

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	-0.3 to +6	V
V_{IN}	Voltage applied to any pin	-0.3 to (V_{CC} + 0.3)	V
P_D	Power dissipation, T_A = 25°C (still air) 24-Pin Plastic TSSOP	555	mW
T_{JMAX}	Maximum operating junction temperature	150	°C
P_{MAX}	Maximum power (RF/IF/LO pins)	+20	dBm
T_{STG}	Storage temperature range	–65 to +150	°C

NOTE:
1. Transients exceeding these conditions may damage the product.
2. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance, and absolute maximum ratings may impact product reliability θ_{JA}: 24-Pin TSSOP = 117°C/W
3. IC is protected for ESD voltages for 2000V, excepts pins 10 and 12, which are protected up to 500V.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	2.7 to 5.5	V
T_A	Operating ambient temperature range	-40 to +85	°C
T_J	Operating junction temperature	-40 to +105	°C

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNITS
			MIN	-4σ	TYP	+4σ	MAX	
I_{CCTX}	Supply current, Transmit	LO mode = Hi	25		37		45	mA
I_{CCRX}	Supply current, Receive	LO mode = Hi	15		22		28	mA
$I_{CC\ OFF}$	Power down mode (Tx/Rx SW = Low)	LO mode = Hi, LNA gain = Hi			0		10	µA
V_{LNA-IN}	LNA input voltage	Receive mode			0.855			V
$I_{LNA-OUT}$	LNA output bias current	Receive mode			4.0			mA
$V_{LO\ 2.1\ GHz}$	LO buffer DC input voltage	LO mode = Hi			2.1			V
$V_{LO\ 1.05\ GHz}$	LO buffer DC input voltage	LO mode = Low			2.1			V
$V_{TX\ IF}$	Tx Mixer input voltage	Transmit mode			1.7			V
$V_{TX\ IFB}$	Tx Mixer input voltage	Transmit mode			1.7			V

AC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; LO_{IN} = -10dBm @ 2.1GHz; f_{RF} = 2.45GHz; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNITS
			MIN	-4σ	TYP	+4σ	MAX	
Low Noise Amplifier (In = Pin 2; Out = 23)								
S_{21}	Amplifier gain	LNA gain = Hi		12.7	14.0	15.3		dB
$\Delta S_{21}/\Delta T$	Gain temperature sensitivity	LNA gain = Hi			-0.002			dB/°C
$\Delta S_{21}/\Delta V_{CC}$	Gain V_{CC} drift	LNA gain = Hi			0.3			dB/V
S_{12}	Amplifier reverse isolation	LNA gain = Hi			-22			dB
S_{11}	Amplifier input match[1]	LNA gain = Hi			-8			dB
S_{22}	Amplifier output match[1]	LNA gain = Hi			-8			dB
ISO	Isolation: LO_1 to LNA_{IN}	LO mode = Hi, LNA gain = Hi			-45			dB
P_{-1dB}	Amplifier input 1dB gain compression	LNA gain = Hi			-15			dBm
IP3	Amplifier input third order intercept	$f_1 - f_2$ = 1MHz, LNA gain = Hi			-3			dBm
NF	Amplifier noise figure (50Ω)	LNA gain = Hi		2.3	2.5	2.7		dB
LNA High Overload Mode								
S_{21}	Amplifier gain	LNA gain = Low		−14.0	-13.3	−12.0		dB
$\Delta S_{21}/\Delta T$	Gain temperature sensitivity	LNA gain = Low			-0.01			dB/°C
$\Delta S_{21}/\Delta V_{CC}$	Gain V_{CC} drift	LNA gain = Low			0.3			dB/V
S_{12}	Amplifier reverse isolation	LNA gain = Low			-16			dB
S_{11}	Amplifier input match[1]	LNA gain = Low			-8			dB
S_{22}	Amplifier output match[1]	LNA gain = Low			-8			dB
ISO	Isolation: LO_1 to LNA_{IN}	LO mode = Hi, LNA gain = Low			-45			dB
P_{-1dB}	Amplifier input 1dB gain compression	LNA gain = Low			+6			dBm
IP3	Amplifier input third order intercept	$f_1 - f_2$ = 1MHz, LNA gain = Low			17			dBm
NF	Amplifier noise figure (50Ω)	LNA gain = Low			17			dB
Rx Mixer (RF = Pin 19, IF = Pins 5 and 6, LO = Pin 10 or 12, P_{LO} = -10dBm)								
PG_C	Power conversion gain into 50Ω : matched to 50Ω using external balun circuitry.	f_S = 2.45GHz, f_{LO} = 2.1GHz, f_{IF} = 350MHz		7.9	8.5	9.1		dB
$\Delta G_C/\Delta T$	Gain temperature drift				-0.016			dB/°C
$\Delta G_C/\Delta V_{CC}$	Gain V_{CC} drift				0.34			dB/V
S_{11-RF}	Input match at RF (2.45GHz)[1]				-15			dB
NF_M	SSB noise figure (2.45GHz) (50Ω)			10.2	10.9	11.6		dB
P_{-1dB}	Mixer input 1dB gain compression			−11.4	-10.3	−9.2		dBm
IP3	Input third order intercept	$f_1 - f_2$ = 1MHz		1.7	2.8	3.9		dBm
f_{RF}	RF frequency range[3]		2.4		2.45		2.5	GHz
f_{IF}	IF frequency range[3]		300		350		400	MHz

AC ELECTRICAL CHARACTERISTICS (continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNITS
			MIN	-4σ	TYP	+4σ	MAX	
Rx Mixer Spurious Components (P_{IN} = P_{-1dB})								
P_{RF-IF}	RF feedthrough to IF	C_L = 2pF per side			-35			dBc
P_{LO-IF}	LO feedthrough to IF	C_L = 2pF per side			-35			dBc
Tx Mixer (RF = Pin 19, IF = Pins 7 and 8, LO = Pin 10 or 12, P_{LO} = -10dBm)								
PG_C	Power conversion gain: R_L = 50Ω R_S = 50Ω	f_S = 2.45GHz, f_{LO} = 2.1GHz, f_{IF} = 350MHz		15.0	17	19.9		dB
$\Delta G_C/\Delta T$	Gain temperature drift				-0.032			dB/°C
$\Delta G_C/\Delta V_{CC}$	Gain voltage drift				0.4			dB/V
S_{11-RF}	Output match at RF (2.45GHz)[1]				-10			dB
NF_M	SSB noise figure (2.45GHz) (50Ω)				13.2			dB
P_{-1dB}	Output 1dB gain compression			1.5	2.9	4.3		dBm
IP3	Output third order intercept	$f_1 - f_2$ = 1MHz		10.1	+11.5	12.9		dBm
f_{RF}	RF frequency range[3]		2.4		2.45		2.5	GHz
f_{IF}	IF frequency range[3]		300		350		400	MHz
Tx Mixer Spurious Components (P_{OUT} = P_{-1dB})								
P_{IF-RF}	IF feedthrough to RF				-29			dBc
P_{LO-RF}	LO feedthrough to RF				-20			dBc
P_{2LO-RF}	2*LO feedthrough to RF				-25			dBc
$P_{IMAGE-RF}$	Image feedthrough to RF				-0			dBc
LO Buffer: Full and Half Frequency inputs								
P_{LO}	LO drive level (see figure 16)		-10		-7		5	dBm
S_{11-LO1}	Mixer input match (LO = 2.1GHz)	LO mode = Hi			-10			dB
S_{11-LO2}	Mixer input match (LO = 1.05GHz)	LO mode = Low			-10			dB
f_{LO2G}	LO2G frequency range[3]	LO mode = Hi	1.9		2.1		2.3	GHz
f_{LO1G}	LO1G frequency range[3]	LO mode = Low	0.85		1.05		1.25	GHz
Switching[2]								
t_{Rx-Tx}	Receive-to-transmit switching time				1			µs
t_{Tx-Rx}	Transmit-to-Receive switching time				1			µs
$t_{POWER\ UP}$	Chip enable time				1			µs
$t_{PWR\ DWN}$	Chip disable time				1			µs

NOTES:
1. With simple external matching
2. With 50pF coupling capacitors on all RF and IF parts
3. This part has been optimized for the frequency range at 2.4–2.5 GHz. Operation outside this frequency range may yield performance other than specified in this datasheet.

Table 1. Truth Table

Chip-En	TxRx-SW	LNA-SW	LO-SW	Mode	LNA Gain	LO Freq. (Typ)
0	X	X	X	Sleep	N/S	N/S
1	0	1	1	Receive	+14dB	2.1GHz
1	0	0	1	Receive	-8dB	2.1GHz
1	0	1	0	Receive	+14dB	1.05GHz
1	0	0	0	Receive	-8dB	1.05GHz
1	1	X	1	Transmit	N/S	2.1GHz
1	1	X	0	Transmit	N/S	1.05GHz

FUNCTIONAL DESCRIPTION

The SA2420 is a 2.45GHz transceiver front-end available in the TSSOP-24 package. This integrated circuit (IC) consists of a low noise amplifier (LNA) and up- and down-converters. The injection of the local oscillator (LO) signal has two options: 1) direct injection of the LO signal at approximately 2GHz, or 2) injection of an LO signal at approximately 1GHz through an on-chip doubler. The SA2420 functions with a supply voltage range of 3 – 5 V (nominally). There is an enable/disable switch available to power up/down the entire chip in 1µs, typically. This transceiver has several unique features.

The LNA has two operating modes: 1) high gain mode with a gain = +14dB; and 2) low gain mode with a gain <-10dB. The switch for this option is internal and is controlled externally by high and low logic to the pin. When the LNA is switched into the attenuation mode, active matching circuitry (on-chip) is switched in (reducing the number of off-chip components required). To reduce power consumption when the chip is transmitting, the LNA is automatically switched into a "sleep" mode (internally) without the use of external circuitry.

The up and down frequency converters are single-ended at the RF port of the mixers. The up and down converters share the same (RF) pin and use an internal switch for transmitting (up-converting) or receiving (down-converting) modes. The switch is controlled externally by high and low logic states. The RF port is matched to 50Ω and has an input IP3 of +2.8dBm (mixer only). The down-convert mixer is buffered and has open collectors at the pins to allow for matching to common SAW filters. The up-convert mixer has differential inputs (IF port) and single-ended output (RF port), with an input pin to output pin gain of 17dB. The output of the up-converter is designed for a power level = +3dBm (P_{-1dB}). The mixers are fed by the two LO options.

The available LO options are: direct injection (2.1GHz at the pin) or through an on-chip doubler. The doubler has a simple LC bandpass filter (internal) at its output which passes the second harmonic to the mixers. Through an internal switch (controlled externally), either LO can be used depending on the designer's application. If an application requires the use of a 1.05GHz VCO, then the doubler option would be used to double the frequency (2 × 1.05GHz = 2.1GHz) before being injected into the mixers. For a 2.1GHz VCO, the direct option would be used. With this option, the signal passes through an on-chip buffer and is then injected into the mixers.

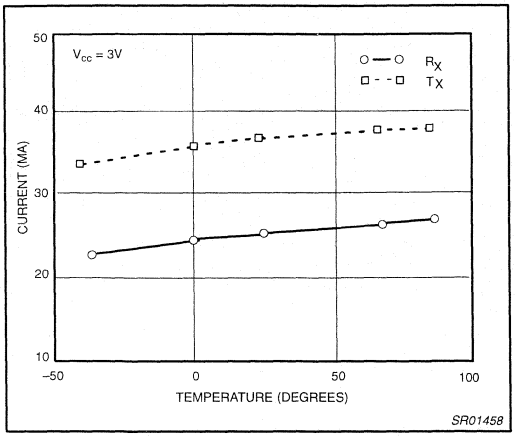


Figure 3. Rx & Tx Currents VS Temperature

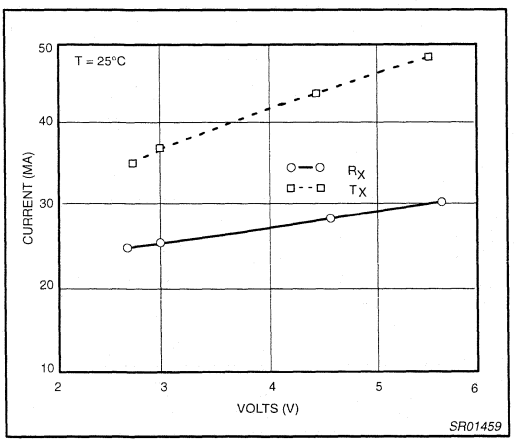


Figure 4. Rx & Tx Currents VS Voltage Supply

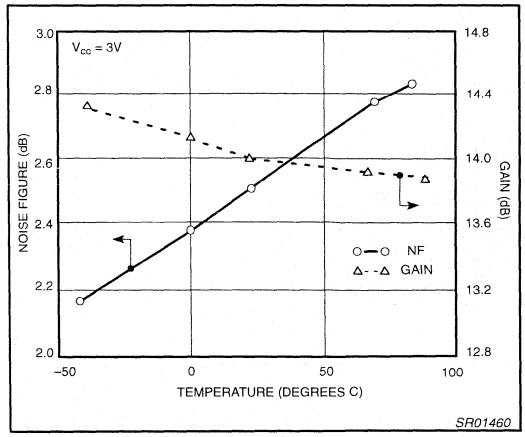


Figure 5. LNA Gain & 50Ω NF VS Temperature

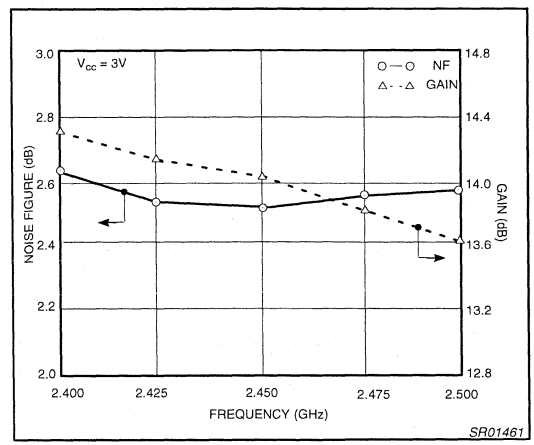


Figure 6. LNA Gain & 50Ω NF VS Frequency

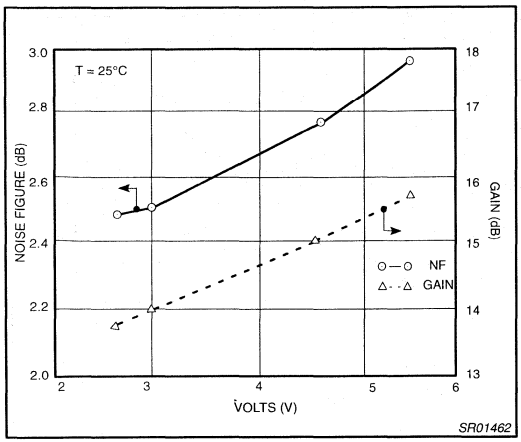


Figure 7. LNA Gain & 50Ω NF VS Supply Voltage

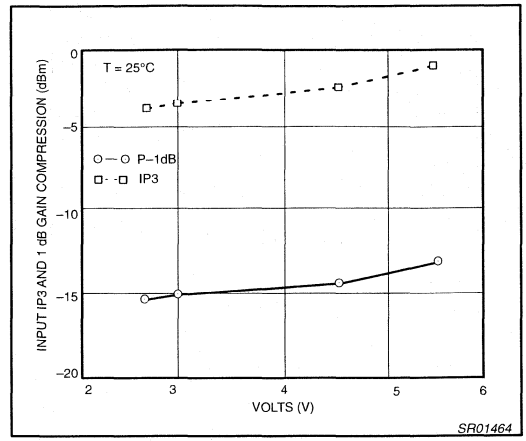


Figure 9. LNA Input IP3 and P–1dB VS Supply Voltage

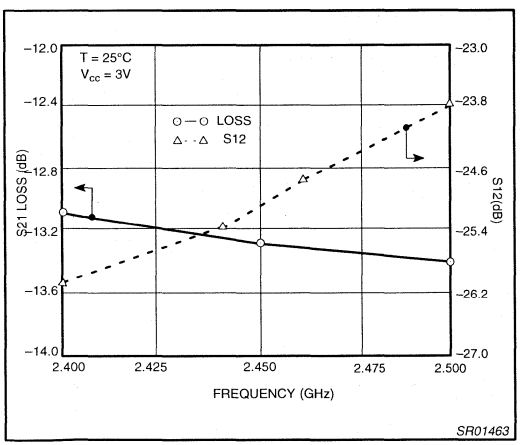


Figure 8. LNA Loss Mode & S12 VS Frequency

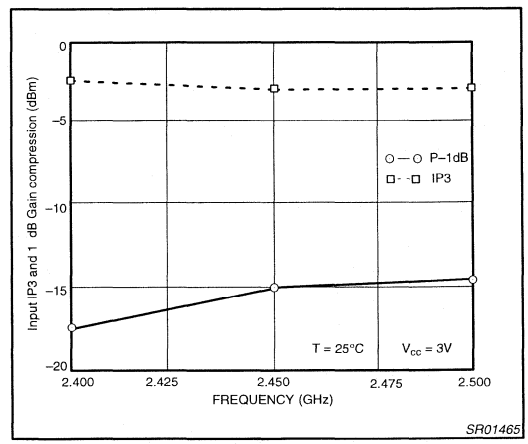


Figure 10. LNA Input IP3 and P–1dB VS Frequency

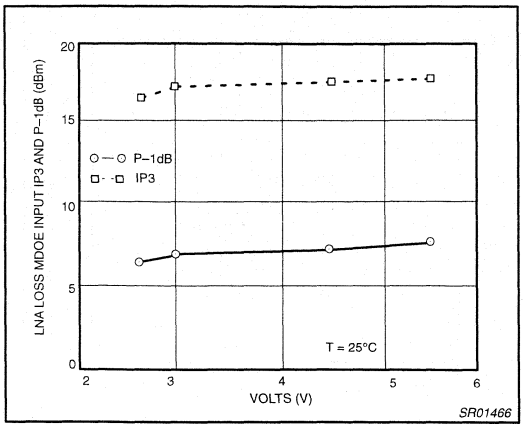


Figure 11. LNA Loss Mode Input IP3 and P–1dB VS Voltage

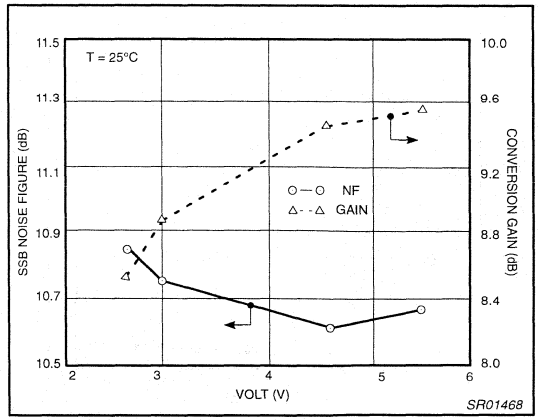


Figure 13. Rx Mixer Conv. Gain & SSB NF VS Supply Voltage

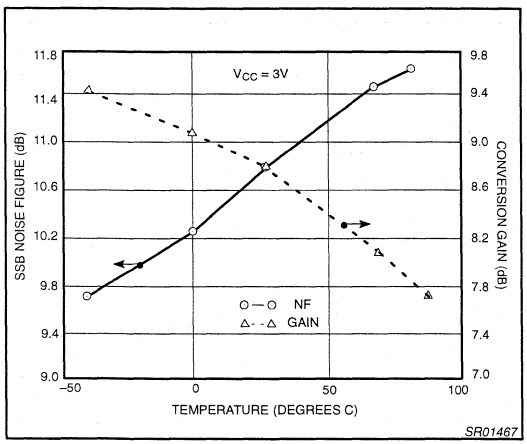


Figure 12. Rx Mixer Conv. Gain & SSB NF VS Temperature

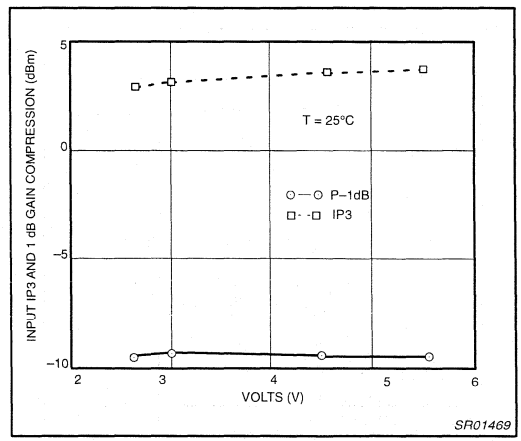


Figure 14. Rx Mixer Input IP3 and P–1dB VS Supply Voltage

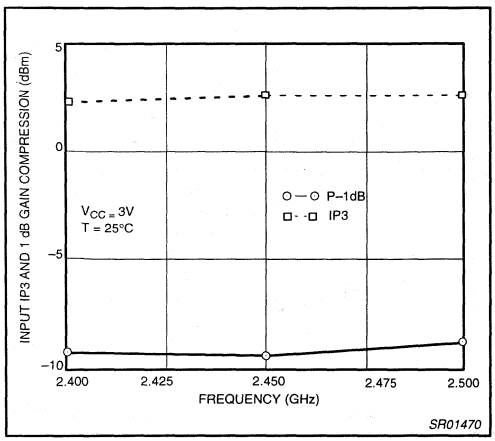


Figure 15. Rx Mixer Output IP3 and P–1dB VS Frequency

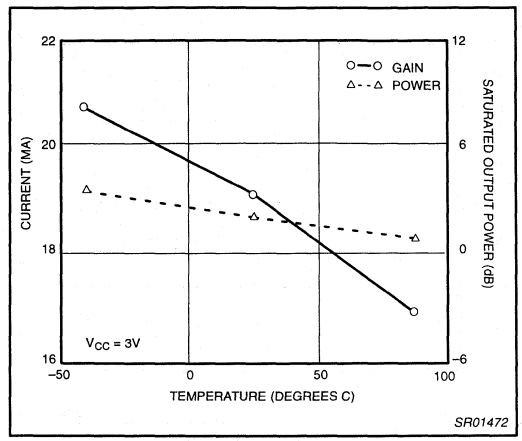


Figure 17. Tx Mx conv. Gain and Output Pwr VS Temp.

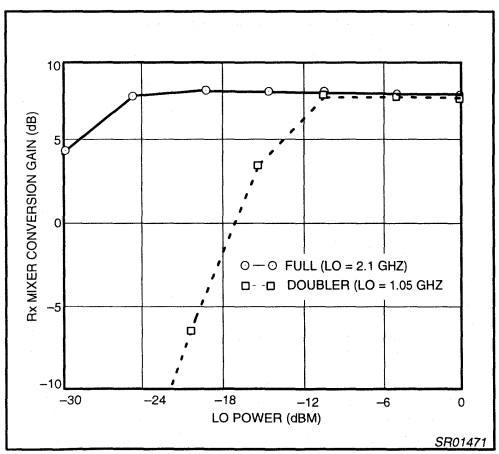


Figure 16. Rx Mixer Conversion Gain VS LO Power

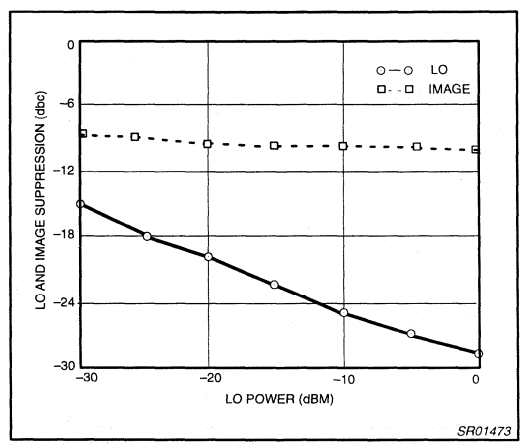


Figure 18. Tx Mixer LO and Image Suppression

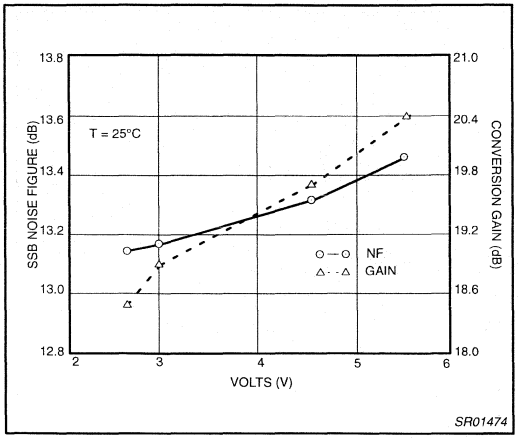


Figure 19. Tx Mixer Gain & NF VS Supply Voltage

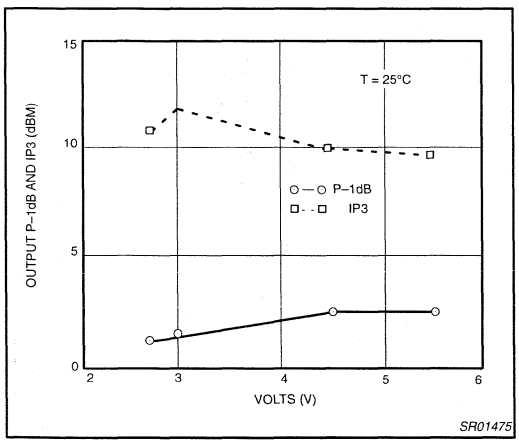


Figure 20. Tx Mixer Output P–1dB and IP3 Vs Voltage

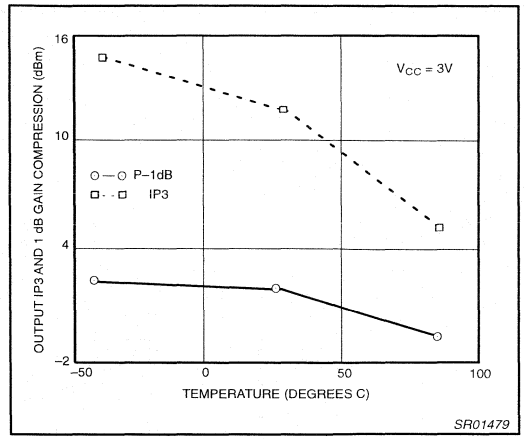


Figure 21. Tx Mixer Output IP3 and P–1dB VS Temperature

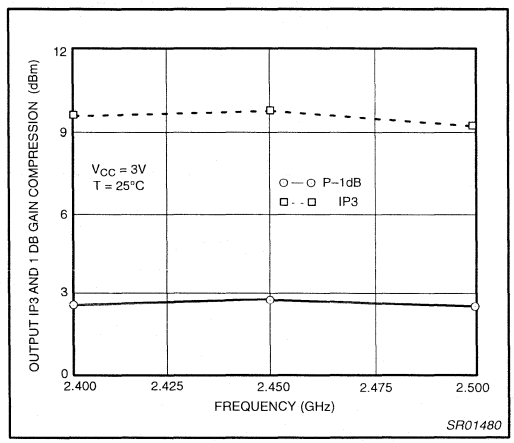


Figure 22. Tx Mixer Output IP3 and P–1dB VS Frequency

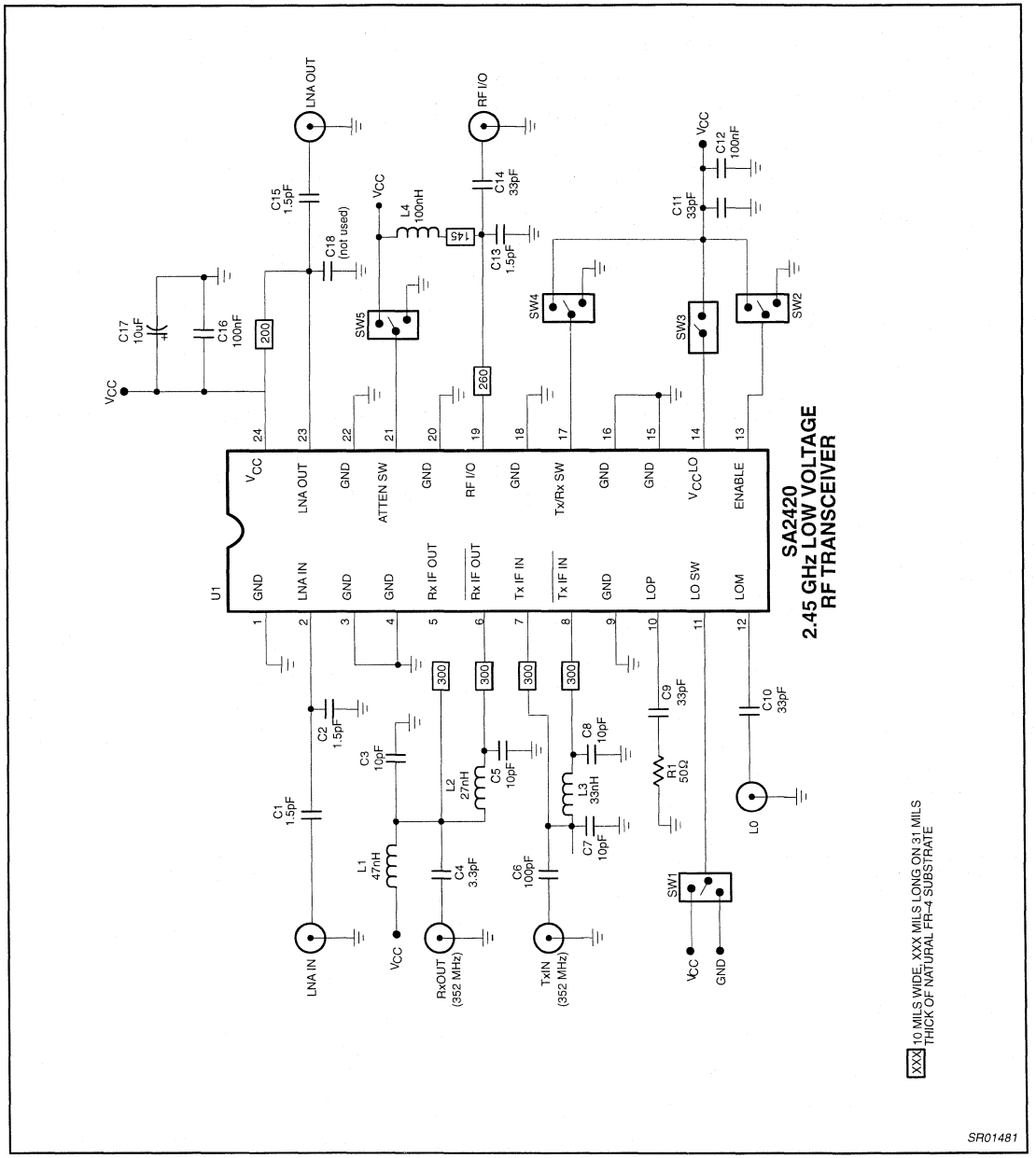
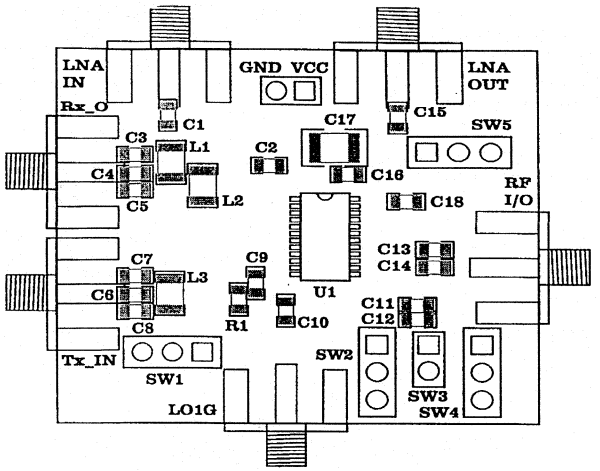
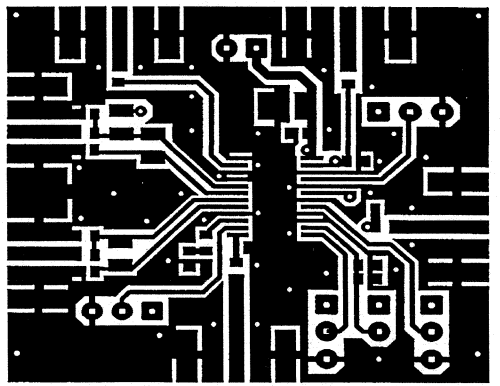
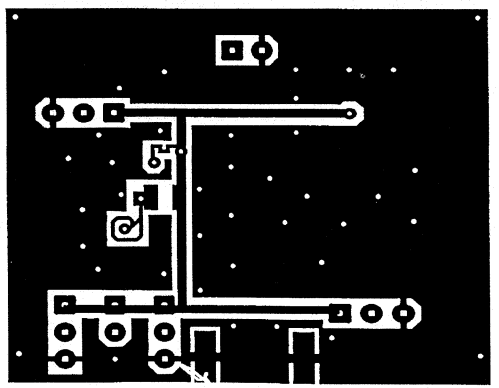

SA2420
2.45 GHz LOW VOLTAGE
RF TRANSCEIVER
U1
VCC
LNA OUT
GND
ATTEN SW
GND
RF I/O
GND
Tx/Rx SW
GND
GND
VCC LO
ENABLE
GND
LNA IN
GND
GND
Rx IF OUT
Rx IF OUT
Tx IF IN
Tx IF IN
GND
LOP
LO SW
LOM
LNA OUT
RF I/O
VCC
C12 100nF
C11 33pF
C15 1.5pF
C18 (not used)
L4 100nH
C14 33pF
C13 1.5pF
C17 10uF
C16 100nF
200
145
260
SW5
SW4
SW3
SW2
C2 1.5pF
C3 10pF
C1 1.5pF
L2 27nH
C5 10pF
C8 10pF
L3 33nH
C9 33pF
C10 33pF
R1 50Ω
L1 47nH
C4 3.3pF
C6 100pF
C7 10pF
SW1
LO
LNA IN
VCC
RxOUT (352 MHz)
TxIN (352 MHz)
VCC
GND
XXX 10 MILS WIDE, XXX MILS LONG ON 31 MILS THICK OF NATURAL FR-4 SUBSTRATE
SR01481

Figure 23.







SR01485

Figure 24. SA2420 RF Transciever

RF dual gain-stage | SA5200

DESCRIPTION

The SA5200 is a dual amplifier with DC to 1200MHz response. Low noise (NF = 3.6dB) makes this part ideal for RF front-ends, and a simple power-down mode saves current for battery operated equipment. Inputs and outputs are matched to 50Ω.

The enable pin allows the designer the ability to turn the amplifiers on or off, allowing the part to act as an amplifier as well as an attenuator. This is very useful for front-end buffering in receiver applications.

FEATURES

- Dual amplifiers
- DC - 1200MHz operation
- Low DC power consumption (4.2mA per amplifier @ V_{CC} = 5V)
- Power-Down Mode (I_{CC} = 95μA typical)
- 3.6dB noise figure at 900MHz
- Unconditionally stable
- Fully ESD protected
- Low cost

PIN CONFIGURATION

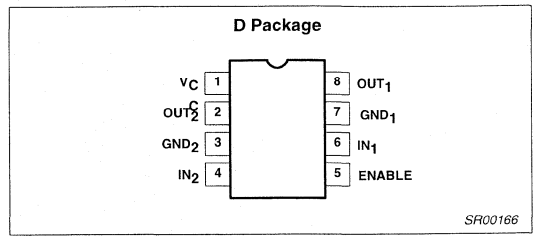


Figure 1. Pin Configuration

- Supply voltage 4-9V
- Gain S_{21} = 7dB at f = 1GHz
- Input and output match S_{11}, S_{22} typically <–14dB

APPLICATIONS

- Cellular radios
- RF IF strips
- Portable equipment

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Small Outline (Surface–mount)	–40-+85°C	SA5200D	SOT96-1

BLOCK DIAGRAM

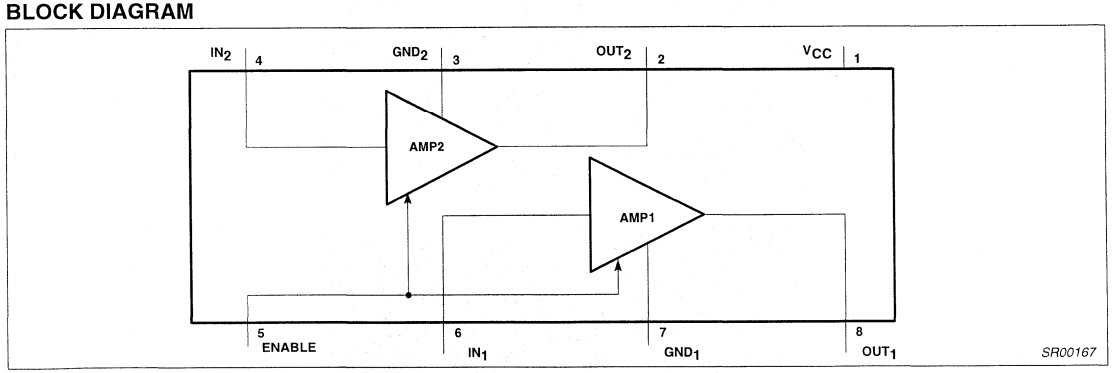


Figure 2. Block Diagram

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	4.0 to 9.0	V
T_A	Operating ambient temperature range SA Grade	-40 to +85	°C
T_J	Operating junction temperature SA Grade	-40 to +105	°C

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage[1]	-0.5 to +9	V
P_D	Power dissipation, T_A = 25°C (still air)[2] 8-Pin Plastic SO	780	mW
T_{JMAX}	Maximum operating junction temperature	150	°C
P_{MAX}	Maximum power input/output	+20	dBm
T_{STG}	Storage temperature range	–65 to +150	°C

NOTE:
1. Transients exceeding 10.5V on V_{CC} pin may damage product.
2. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance, θ_{JA}:
   8-Pin SO: θ_{JA} = 158°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +5V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{CC}	Supply voltage		4	5.0	9.0	V
I_{CC}	Total supply current	V_{CC} = 5V, ENABLE = High	6.4	8.4	10.4	mA
		V_{CC} = 5V, ENABLE = Low		95	255	µA
		V_{CC} = 9V, ENABLE = High		17.8	22.2	mA
		V_{CC} = 9V, ENABLE = Low		320	960	µA
V_T	TTL/CMOS logic threshold voltage[1]			1.25		V
V_{IH}	Logic 1 level	Power-up mode	2.0		V_{CC}	V
V_{IL}	Logic 0 level	Power-down mode	-0.3		0.8	V
I_{IL}	Enable input current	Enable = 0.4V	-1	0	1	µA
I_{IH}	Enable input current	Enable = 2.4V	-1	0	1	µA
$V_{IDC,ODC}$	Input and output DC levels		0.6	0.83	1.0	V

NOTE:
1. The ENABLE input must be connected to a valid logic level for proper operation of the SA5200.

AC ELECTRICAL CHARACTERISTICS[1]

V_{CC} = +5V, T_A = 25°C, either amplifier, enable = 5V; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
S21	Insertion gain	f = 100MHz	9.2	11	13.2	dB
		f = 900MHz	5.2	7.5		
S22	Output return loss	f = 900MHz		–14.3		dB
S12	Reverse isolation	f = 900MHz		–17.9		dB
S11	Input return loss	f = 900MHz		–16.5		dB
P-1	Output 1dB compression point	f = 900MHz		–4.3		dBm
NF	Noise figure in 50Ω	f = 900MHz		3.6		dB
IP_2	Input second-order intercept point	f = 900MHz		+4.3		dBm
IP_3	Input third-order intercept point	f = 900MHz		–1.8		dBm
ISOL	Amplifier-to-amplifier isolation[2]	f = 900MHz		–25		dB
P_{OUT}	Saturated output power	f = 900MHz		–1.7		dBm
S21	Insertion gain when disabled	f = 100MHz		–13		dB
		f = 900MHz		–13.5		

NOTE:
1. All measurements include the effects of the SA5200 Evaluation Board (see Figure 4). Measurement system impedance is 50Ω.
2. Input applied to one amplifier, output taken at the other output. All ports terminated into 50Ω.

APPLICATIONS

SA5200 is a user-friendly, wide-band, unconditionally stable, low power dual gain amplifier circuit. There are several advantages to using the SA5200 as a high frequency gain block instead of a discrete implementation. First is the simplicity of use. The SA5200 does not need any external biasing components. Due to the higher level of integration and small footprint (SO8) package it occupies less space on the printed circuit board and reduces the manufacturing cost of the system. Also the higher level of integration improves the reliability of the amplifier over a discrete implementation with several components. The power down mode in the SA5200 helps reduce power consumption in applications where the amplifiers can be disabled. And last but not the least is the impedance matching at inputs and outputs. Only those who have toiled through discrete transistor implementations for 50Ω input and output impedance matching can truly appreciate the elegance and simplicity of the SA5200 input and output impedance matching to 50Ω.

A simplified equivalent schematic is shown in 3. Each amplifier is composed of an NPN transistor with an Ft of 13GHz in a classical series-shunt feedback configuration. The two wideband amplifiers are biased from the same bias generator. In normal operation each amplifier consumes about 4mA of quiescent current (at V_{CC} = 5V). In the disable mode the device consumes about 90µA of current, most of it is in the TTL enable buffer and the bias generator. The input impedance of the amplifiers is 50Ω. The amplifiers have typical gain of 11dB at 100MHz and 7dB of gain at 1.2GHz.

It can be seen from 3 that any inductance between Pin 7, 3 and the ground plane will reduce the gain of the amplifiers at higher frequencies. Thus proper grounding of Pins 7 and 3 is essential for maximum gain and increased frequency response. 4 shows the printed circuit board layout and the component placement for the SA5200 evaluation board. The AC coupling capacitors should be selected such that at they are shorts at the desired frequency of operation. Since most low-cost large value surface mount capacitors cease to be simply capacitors in the UHF range and exhibit an inductive behavior, it is recommended that high frequency chip capacitors be utilized in the circuit. A good power supply bypass is also essential for the performance of the amplifier and should be as close to the device as practical.

5 shows the typical frequency response of the two channels of SA5200. The low frequency gain is about 11dB at 100MHz and slowly drops off to 10dB at 500MHz. The gain is about 8dB at 900MHz and 7dB at 1.2 GHz which is typical of SA5200 with a good printed circuit board layout. It can also be seen that both channels have a very well matched frequency response and matched gain to within 0.1dB at 100MHz and 0.2dB at 900MHz.

SA5200 finds applications in many areas of RF communications. It is an ideal gain block for high performance, low cost, low power RF communications transceivers. A typical radio transceiver front-end is shown in 6. This could be the front-end of a cellular phone, a VHF/ UHF hand-held transceiver, UHF cordless telephone or a spread spectrum system. The SA5200 can be used in the receiver path of most systems as an LNA and pre-amplifier. The bandpass filter between the two amplifiers also minimize the noise into the first mixer. In the transmitter path, SA5200 can be used as a buffer to the VCO and isolate the VCO from any load variations due to the power level changes in the power amplifier. This improves the stability of the VCOs. The SA5200 can also be used as a pre-driver to the power amplifier modules.

The two amplifiers in SA5200 can be easily cascaded to have a 13dB gain block at 900MHz. At 100MHz the gain will be 22dB and a noise figure of about 5.5dB. The SA5200 can be operated at a higher voltage up to 9V for much improved 1dB output compression point and higher 3rd order intercept point.

Several stages of SA5200 can also be cascaded and be used as an IF amplifier strip for DBS/TV/GPS receivers. 7 shows a 60dB gain IF strip at 180MHz. The noise figure for the cascaded amplifier chain is given by equation 1.

NF (total) = NF1 + NF2/G1 + NF3/G1*G2 + NF4/G1*G2*G3 + ... (Equation. 1)

NOTE: The noise figure and gain should not be in dB in the above equation.

Since the noise figure for each stage is about 3.6dB and the gain is about 11dB, the noise figure for the 60dB gain IF strip will be about 6.4dB.

In applications where a single amplifier is required with a 7.5dB gain at 900MHz and current consumption is of paramount importance (battery powered receivers), the amplifier A1 can be used and amplifier A2 can be disabled by leaving GND2 (Pin 3) unconnected. This will reduce the total current consumption for the IC to a meager 4mA.

The ENABLE pin is useful for Time-Division-Duplex systems where the receiver can be disabled for a period of time. In this case the overall system supply current will be decreased by 8mA.

The ENABLE pin can also be used to improve the system dynamic range. For input levels that are extremely high, the SA5200 can be disabled. In this case the input signal is attenuated by 13dB. This prevents the system from being overloaded as well as improves the system's overall dynamic range. In the disabled condition the SA5200 IP_3 increases to nearly +20dBm.

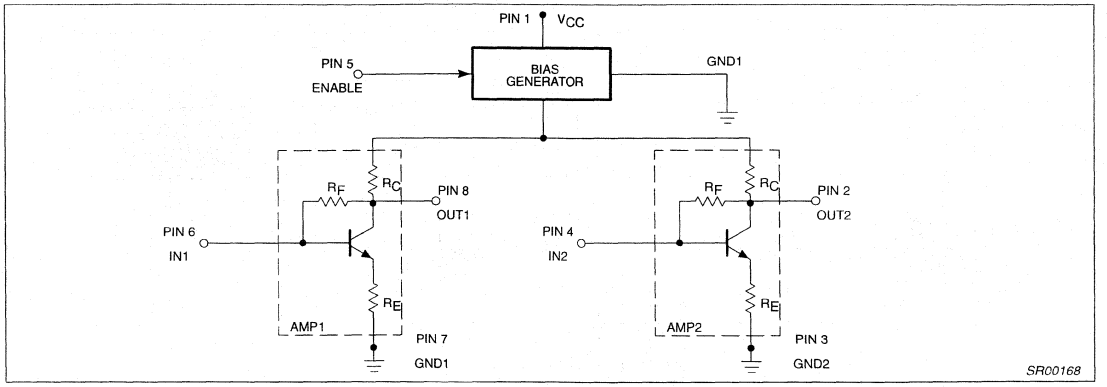


Figure 3. Simplified Equivalent Schematic of SA5200

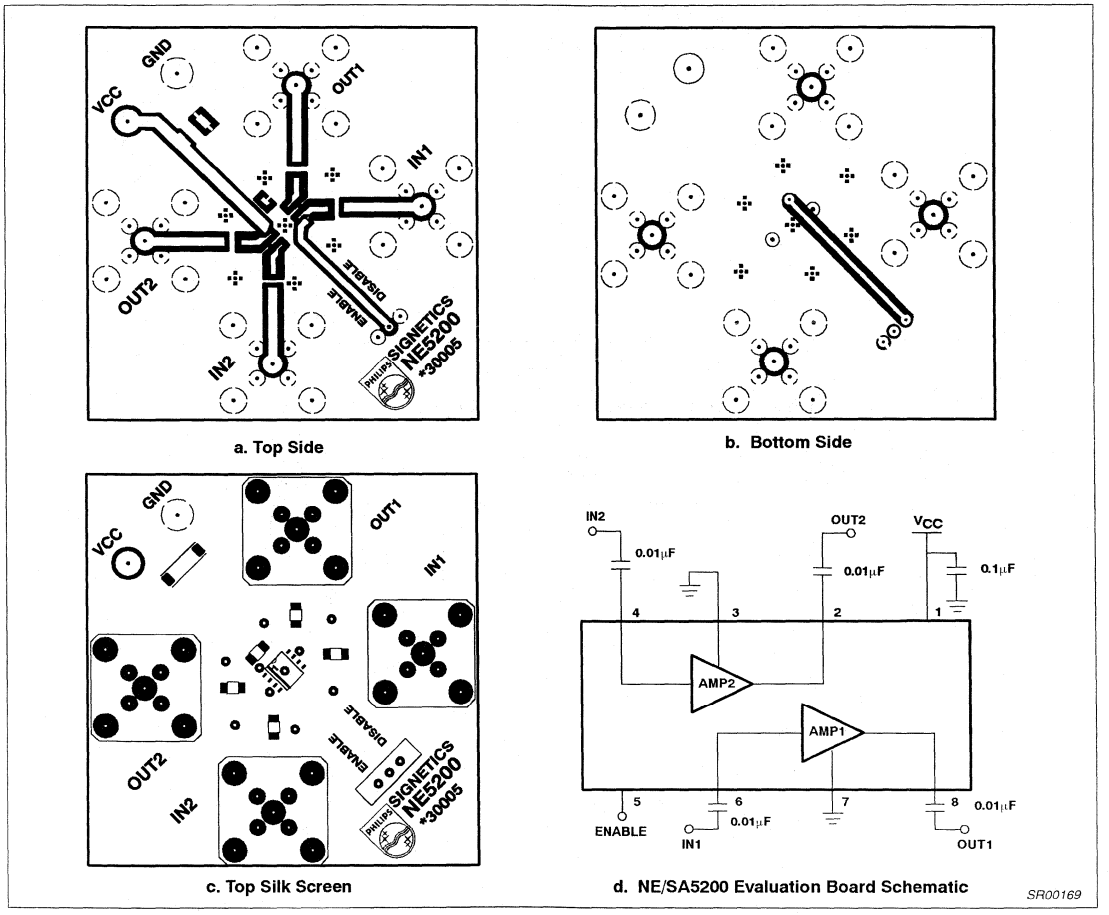


Figure 4. Printed Circuit Board Layout of the SA5200 Evaluation Board

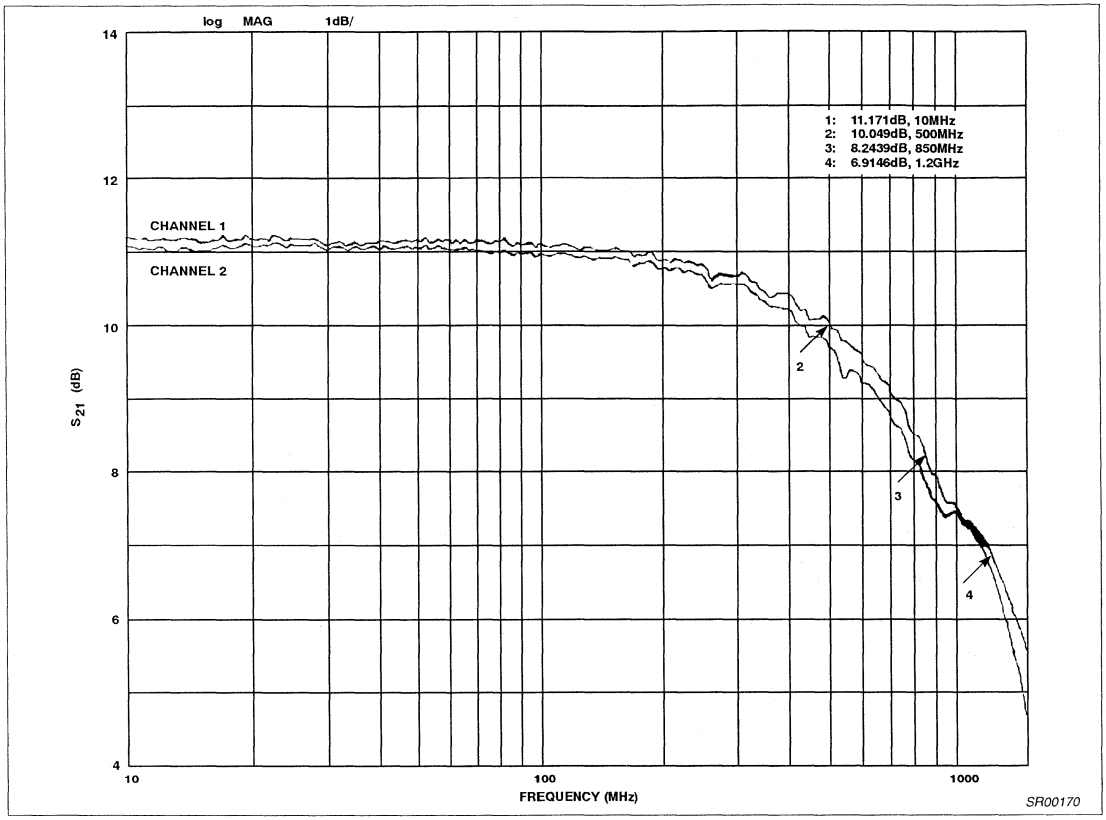


Figure 5. Typical Frequency Response of SA5200 in a 50Ω System

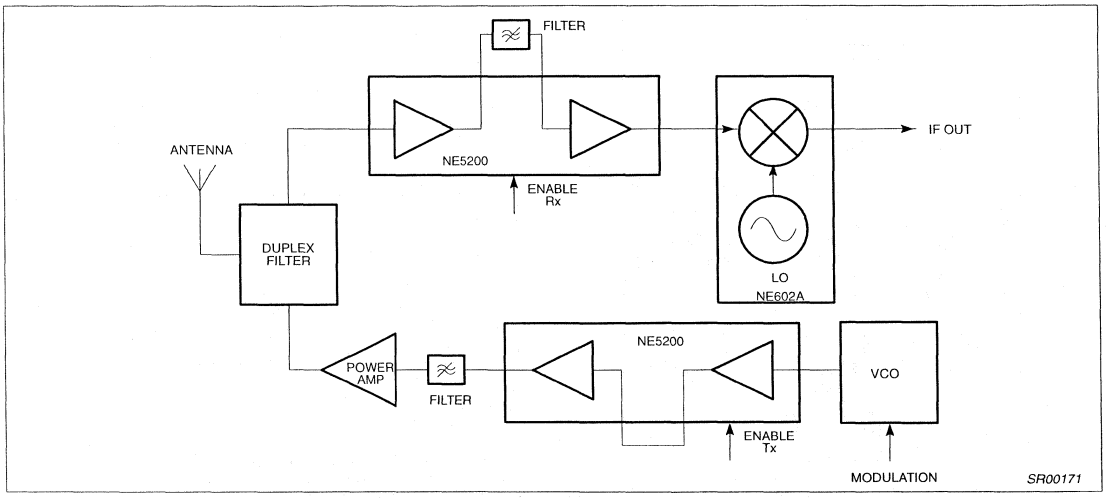


Figure 6. Typical Radio Transceiver Front-End

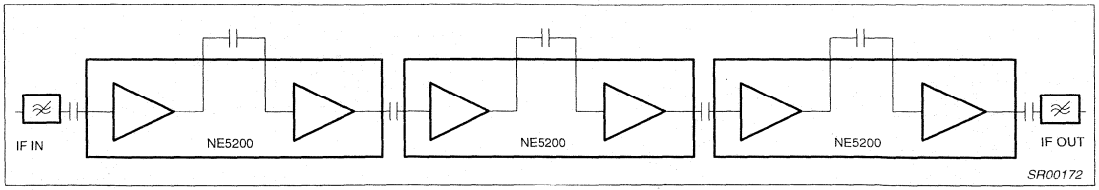


Figure 7. 60dB IF Gain Block for 100-300MHz IF for GPS/DBS Systems

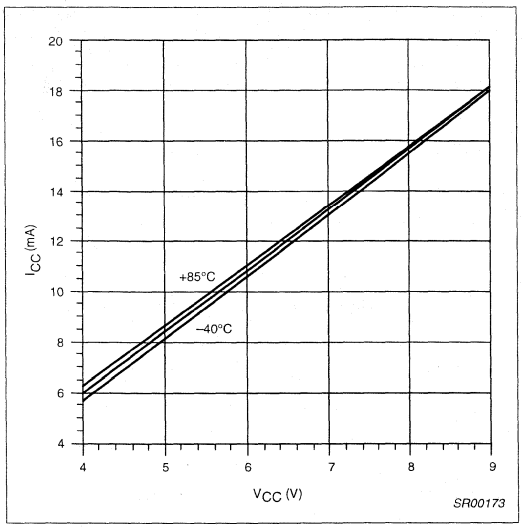


Figure 8. Supply Current vs Supply Voltage and Temperature

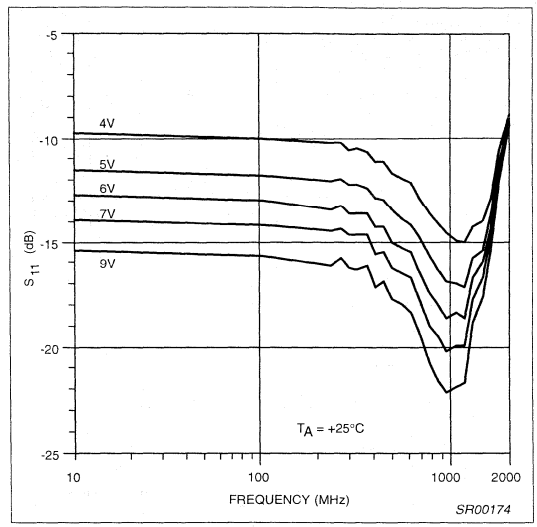


Figure 10. Input Match vs Frequency and V_{CC}

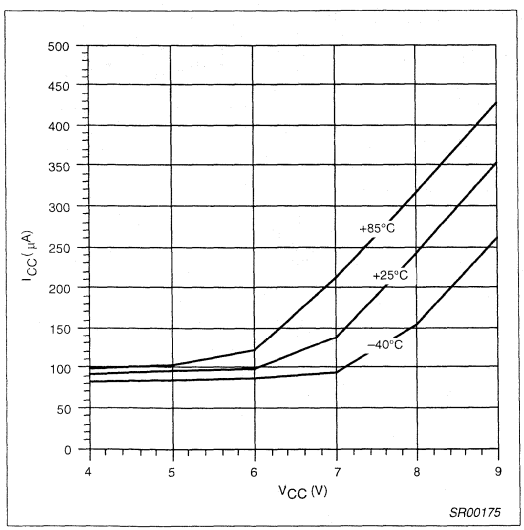


Figure 9. Disabled Supply Current vs V_{CC} and Temperature

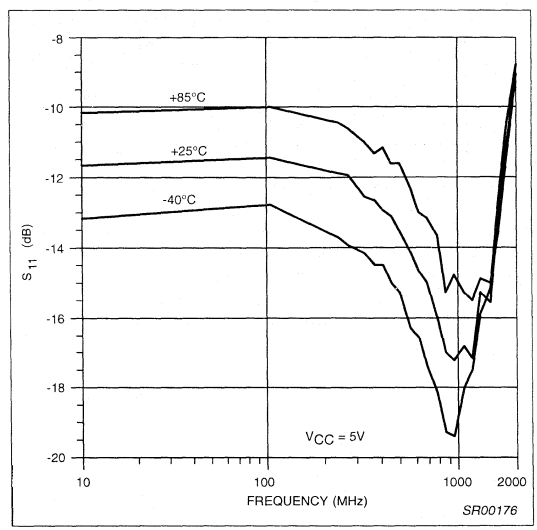


Figure 11. Input Match vs Frequency and Temperature

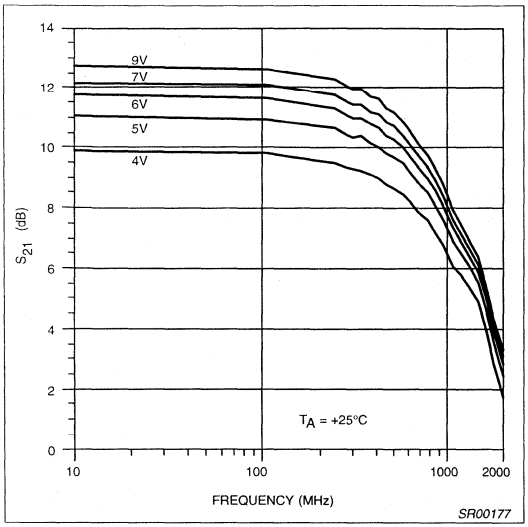


Figure 12. Insertion Gain vs Frequency and V_{CC}

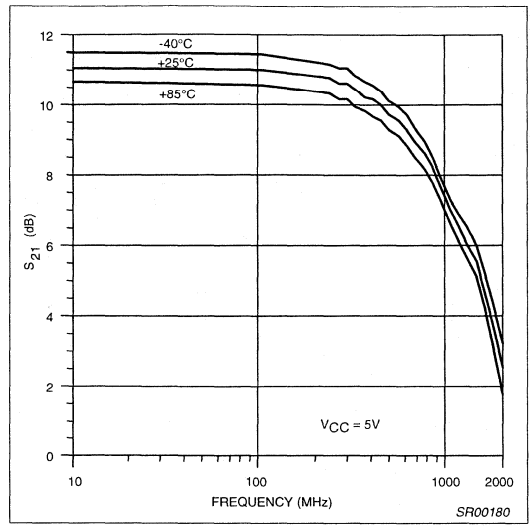


Figure 14. Insertion Gain vs Frequency and Temperature

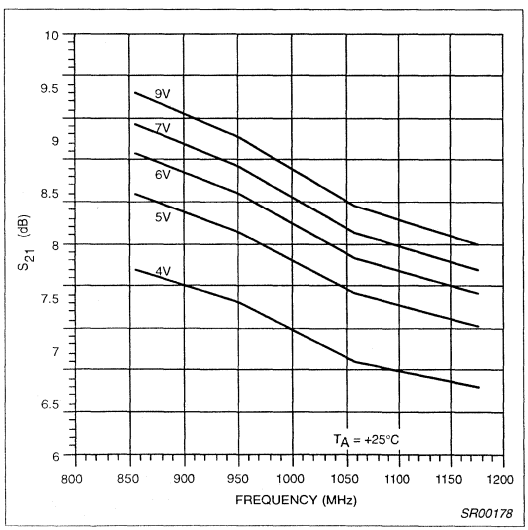


Figure 13. Insertion Gain vs Frequency and V_{CC} — Expanded Detail —

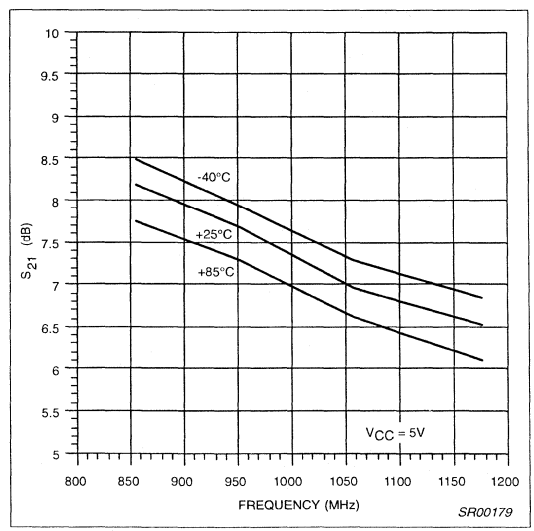


Figure 15. Insertion Gain vs Frequency and Temperature – Expanded Detail –

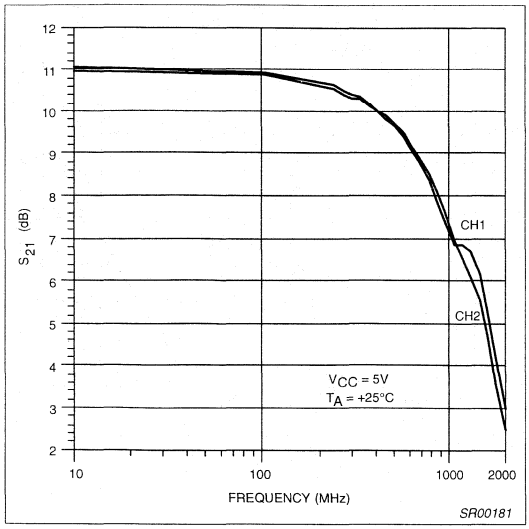


Figure 16. Insertion Gain Matching (CH1 vs CH2) vs Frequency

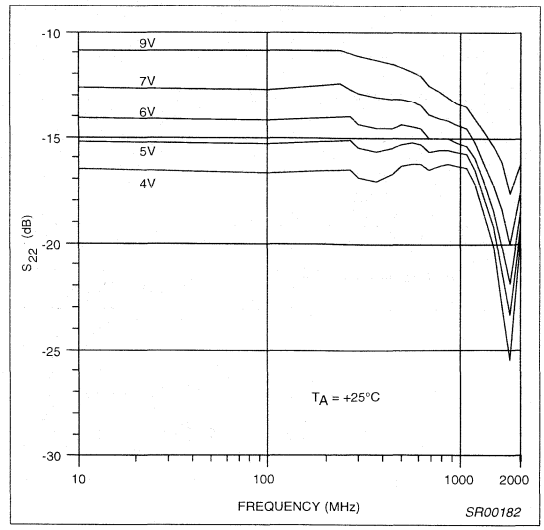


Figure 18. Output Match vs Frequency and V_{CC}

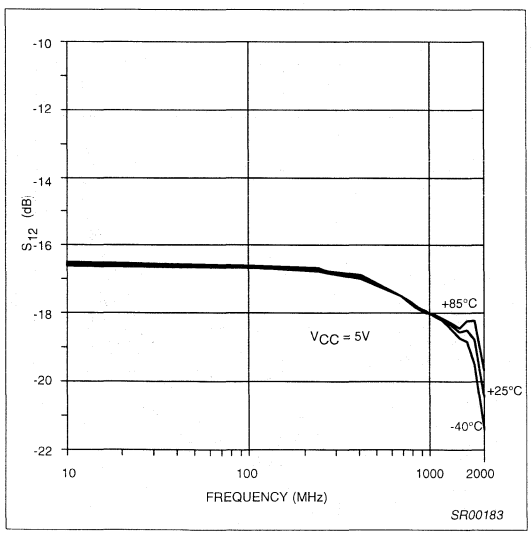


Figure 17. Reverse Insertion Gain vs Frequency and Temperature

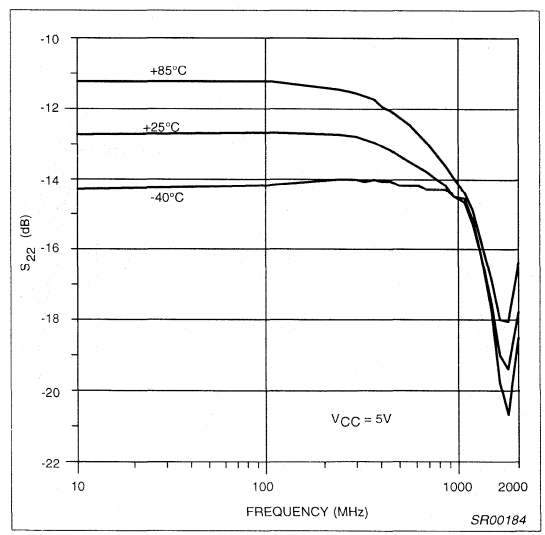


Figure 19. Output Match vs Frequency and Temperature

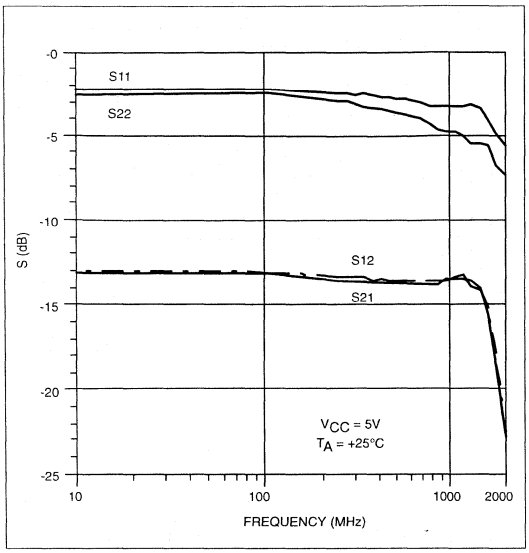


Figure 20. S-parameters vs Frequency for Disabled Amplifier

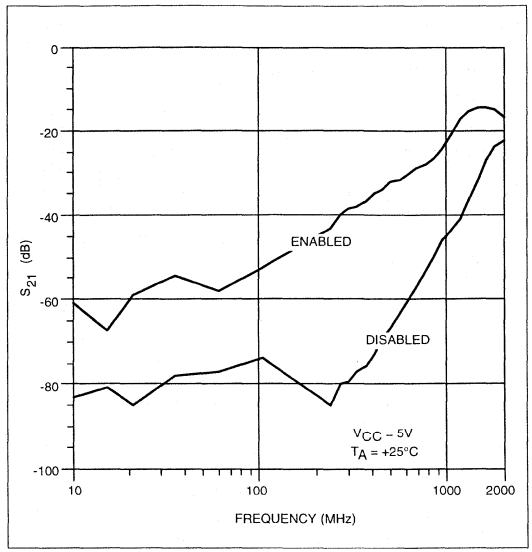


Figure 22. CH1 Input to CH2 Output Isolation vs Frequency

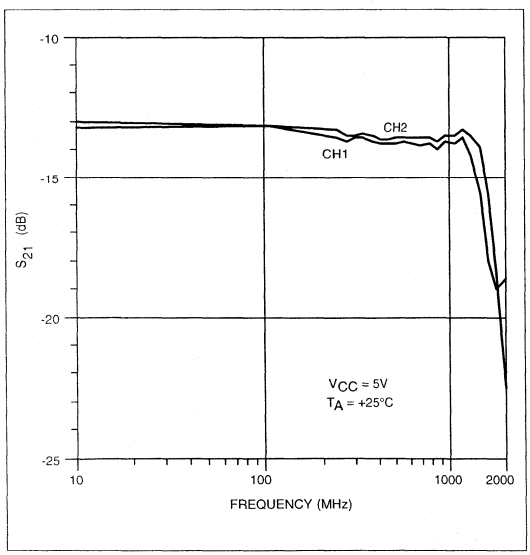


Figure 21. Insertion Gain Matching Disabled (CH1 vs CH2) vs Frequency

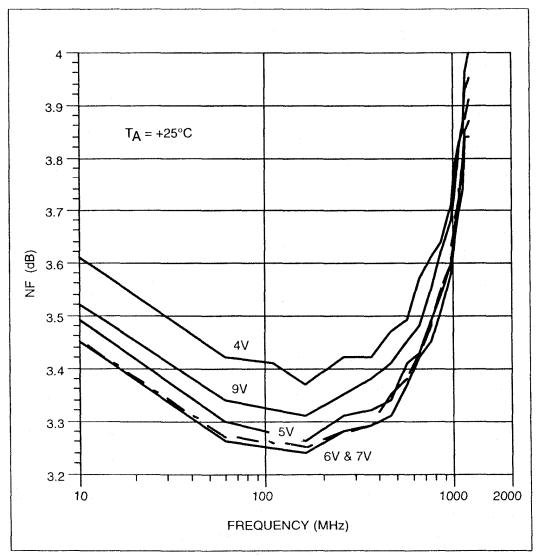


Figure 23. Noise Figure vs Frequency and V_{CC} in a 50Ω System

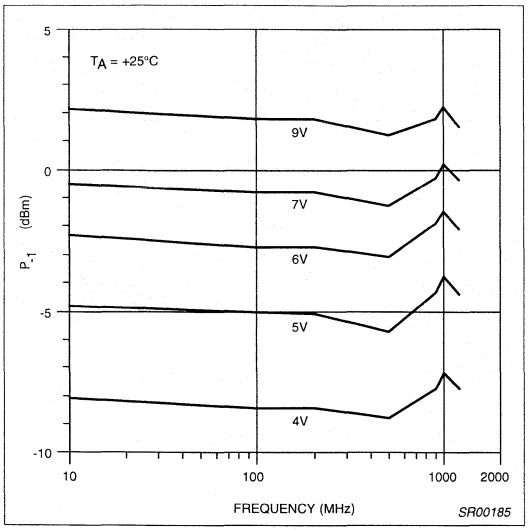


Figure 24. 1dB Output Compression Point vs Frequency and V_{CC}

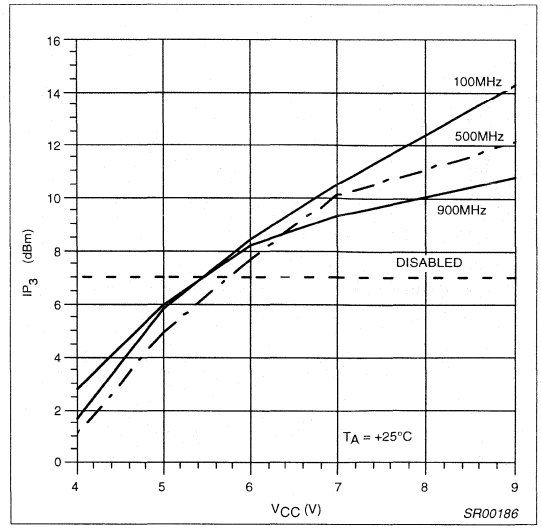


Figure 26. Third-Order Output Intercept vs Frequency and V_{CC}

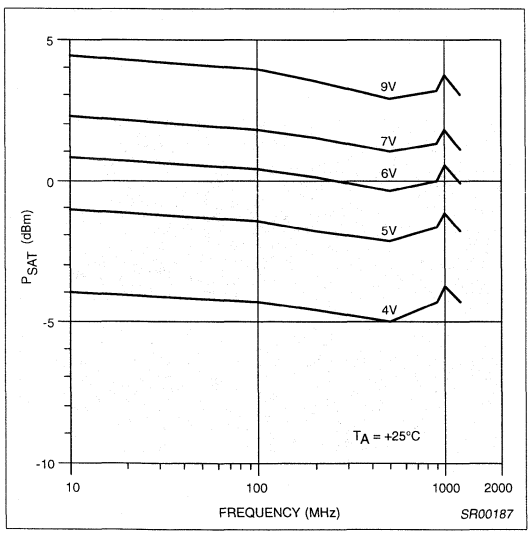


Figure 25. Saturated Output Power vs Frequency and V_{CC}

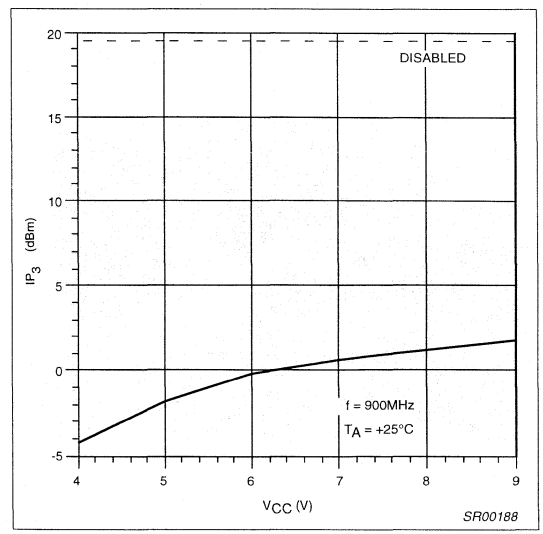


Figure 27. Third-Order Input Intercept vs Frequency and V_{CC}

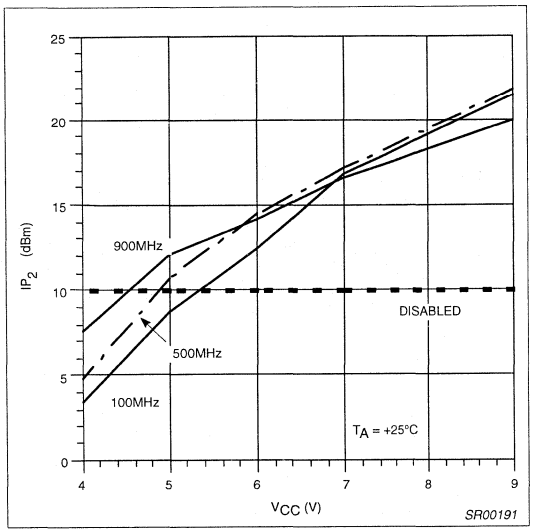


Figure 28. Second-Order Cutput Intercept vs Frequency and V_{CC}

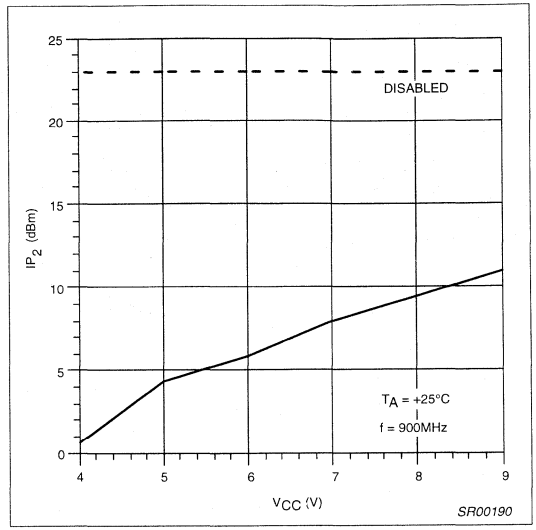


Figure 30. Second-Order Input Intercept vs Frequency and V_{CC}

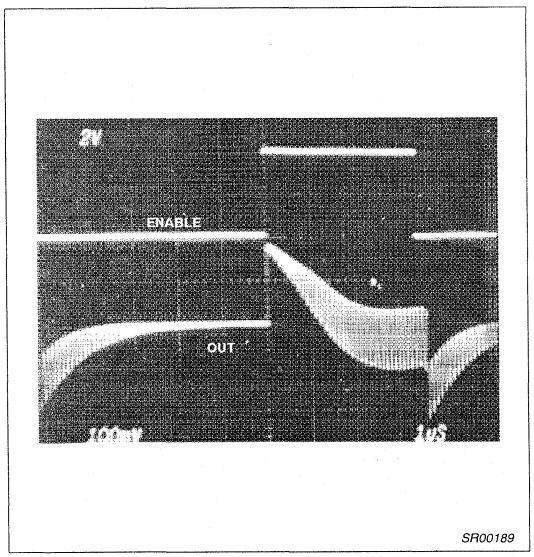


Figure 29. Switching Speed; f_{IN} = 10MHz at –26dBm, V_{DD} = 5V, Coupling Capacitors Set to 0.01µF

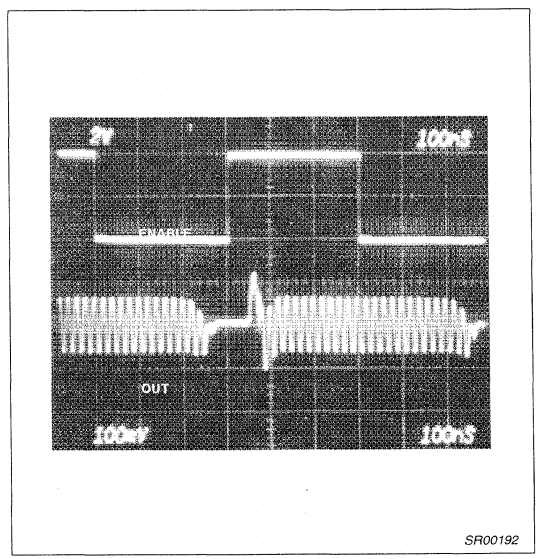


Figure 31. Switching Speed; f_{IN} = 50MHz at –26dBm, V_{DD} = 5V, Coupling Capacitors Set to 100pF

Wide-band high-frequency amplifier SA5204A

DESCRIPTION

The SA5204A family of wideband amplifiers replaces the SA5204 family. The 'A' parts are fabricated on a rugged 2μm bipolar process featuring excellent statistical process control. Electrical performance is nomically identical to the original parts.

The SA5204A is a high-frequency amplifier with a fixed insertion gain of 20dB. The gain is flat to ±0.5dB from DC to 200MHz. The -3dB bandwidth is greater than 350MHz. This performance makes the amplifier ideal for cable TV applications. The SA5204A operates with a single supply of 6V, and only draws 25mA of supply current, which is much less than comparable hybrid parts. The noise figure is 4.8dB in a 75Ω system and 6dB in a 50Ω system.

The SA5204A is a relaxed version of the SA5205. Minimum guaranteed bandwidth is relaxed to 350MHz and the "S" parameter Min/Max limits are specified as typicals only.

Until now, most RF or high-frequency designers had to settle for discrete or hybrid solutions to their amplification problems. Most of these solutions required trade-offs that the designer had to accept in order to use high-frequency gain stages. These include high power consumption, large component count, transformers, large packages with heat sinks, and high part cost. The SA5204A solves these problems by incorporating a wideband amplifier on a single monolithic chip.

The part is well matched to 50 or 75Ω input and output impedances. The standing wave ratios in 50 and 75Ω systems do not exceed 1.5 on either the input or output over the entire DC to 350MHz operating range.

Since the part is a small, monolithic IC die, problems such as stray capacitance are minimized. The die size is small enough to fit into a very cost-effective 8-pin small-outline (SO) package to further reduce parasitic effects.

No external components are needed other than AC-coupling capacitors because the SA5204A is internally compensated and matched to 50 and 75Ω. The amplifier has very good distortion specifications, with second and third-order intermodulation intercepts of +24dBm and +17dBm, respectively, at 100MHz.

The part is well matched for 50Ω test equipment such as signal generators, oscilloscopes, frequency counters, and all kinds of signal analyzers. Other applications at 50Ω include mobile radio, CB radio, and data/video transmission in fiber optics, as well as broadband LANs and telecom systems. A gain greater than 20dB can be achieved by cascading additional SA5204As in series as required, without any degradation in amplifier stability.

PIN CONFIGURATION

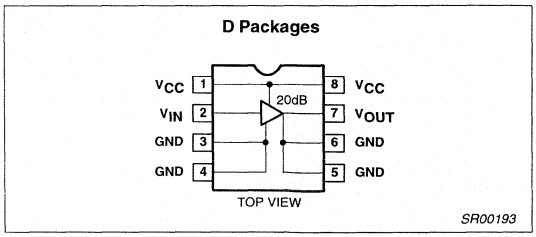


Figure 1. Pin Configuration

FEATURES

- Bandwidth (min.)
  200 MHz, ±0.5dB
  350 MHz, -3dB
- 20dB insertion gain
- 4.8dB (6dB) noise figure Z_O=75Ω (Z_O=50Ω)
- No external components required
- Input and output impedances matched to 50/75Ω systems
- Surface-mount package available
- Cascadable
- 2000V ESD protection

APPLICATIONS

- Antenna amplifiers
- Amplified splitters
- Signal generators
- Frequency counters
- Oscilloscopes
- Signal analyzers
- Broadband LANs
- Networks
- Modems
- Mobile radio
- Security systems
- Telecommunications

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Small Outline (SO) package	–40 to +85°C	SA5204AD	SOT96-1

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	9	V
V_{IN}	AC input voltage	5	V_{P-P}
T_A	Operating ambient temperature range SA grade	 –40 to +85	 °C
P_{DMAX}	Maximum power dissipation[1, 2] T_A=25°C(still–air) D package	 780	 mW
T_J	Junction temperature	150	°C
T_{STG}	Storage temperature range	–55 to +150	°C
T_{SOLD}	Lead temperature (soldering 60s)	300	°C

NOTES:
1. Derate above 25°C, at the following rates
   D package at 6.2mW/°C
2. See "Power Dissipation Considerations" section.

EQUIVALENT SCHEMATIC

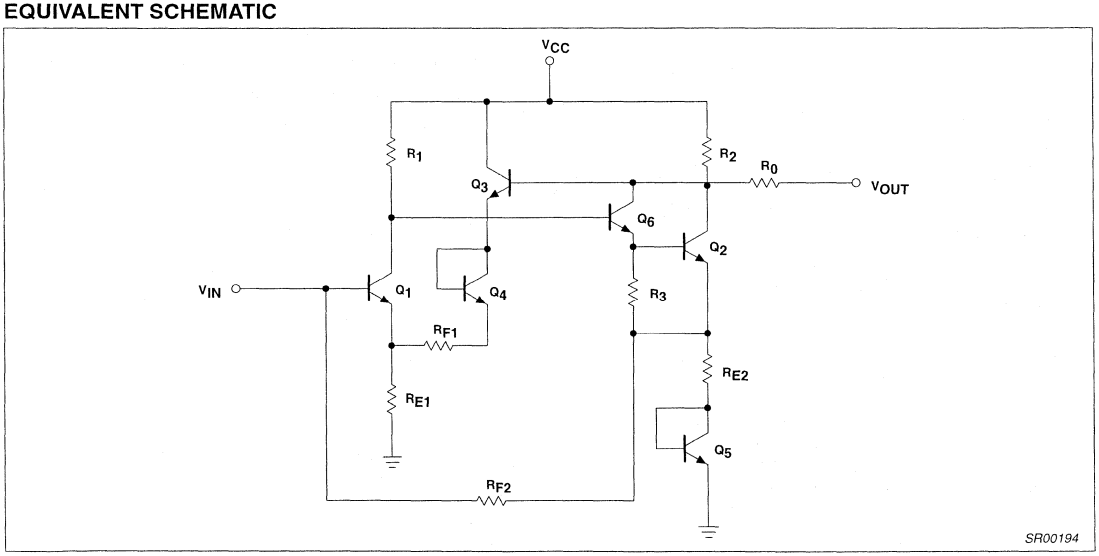


Figure 2. Equivalent Schematic

DC ELECTRICAL CHARACTERISTICS

V_{CC}=6V, Z_S=Z_L=Z_O=50Ω and T_A=25°C, in all packages, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Operating supply voltage range	Over temperature	5		8	V
I_{CC}	Supply current	Over temperature	19	25	33	mA
S21	Insertion gain	f=100MHz, over temperature	16	19	22	dB
S11	Input return loss	f=100MHz		25		dB
		DC –550MHz		12		
S22	Output return loss	f=100MHz		27		dB
		DC –550MHz		12		
S12	Isolation	f=100MHz		–25		dB
		DC –550MHz		–18		
BW	Bandwidth	±0.5dB	200	350		MHz
BW	Bandwidth	–3dB	350	550		MHz
	Noise figure (75Ω)	f=100MHz		4.8		dB
	Noise figure (50Ω)	f=100MHz		6.0		dB
	Saturated output power	f=100MHz		+7.0		dBm
	1dB gain compression	f=100MHz		+4.0		dBm
	Third–order intermodulation intercept (output)	f=100MHz		+17		dBm
	Second–order intermodulation intercept (output)	f=100MHz		+24		dBm
t_R	Rise time			500		ps
t_P	Propagation delay			500		ps

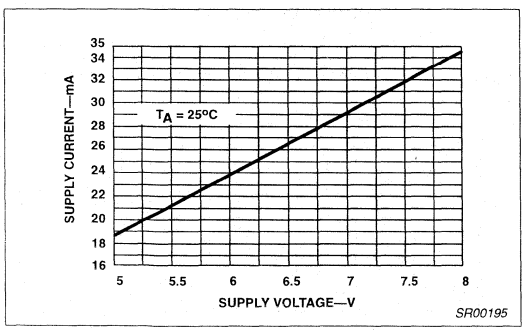


Figure 3. Supply Current vs Supply Voltage

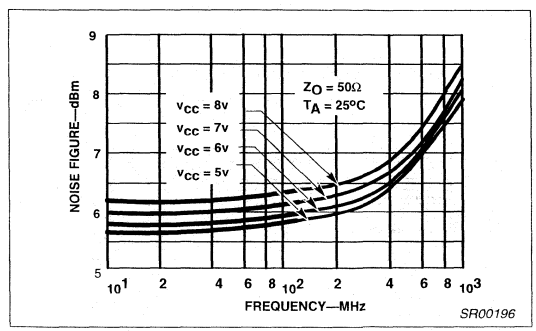


Figure 4. Noise Figure vs Frequency

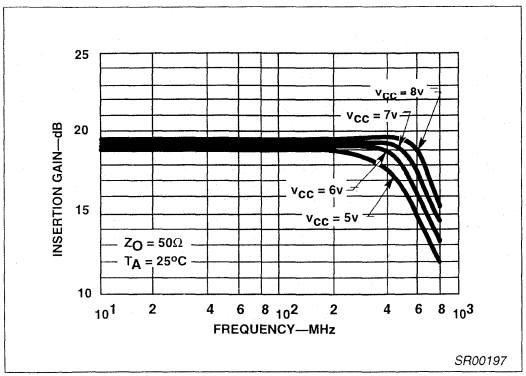


Figure 5. Insertion Gain vs Frequency (S_{21})

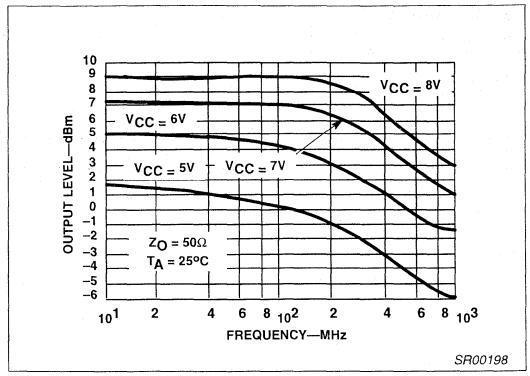


Figure 8. 1dB Gain Compression vs Frequency

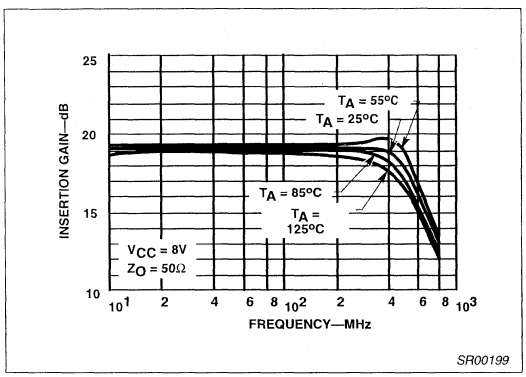


Figure 6. Insertion Gain vs Frequency (S_{21})

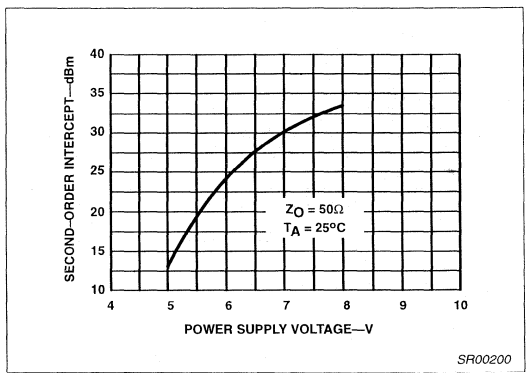


Figure 9. Second-Order Output Intercept vs Supply Voltage

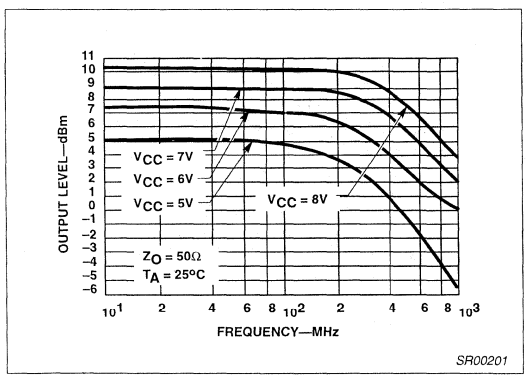


Figure 7. Saturated Output Power vs Frequency

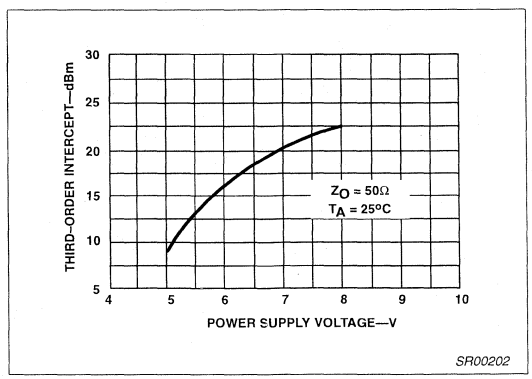


Figure 10. Third-Order Intercept vs Supply Voltage

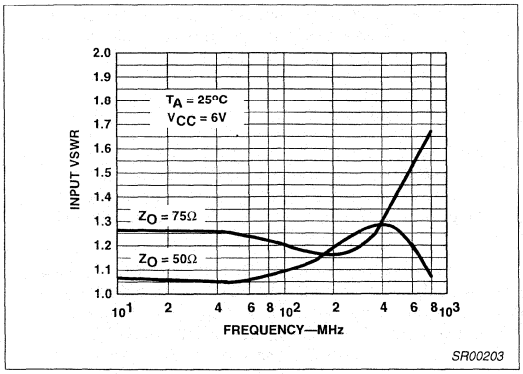


Figure 11. Input VSWR vs Frequency

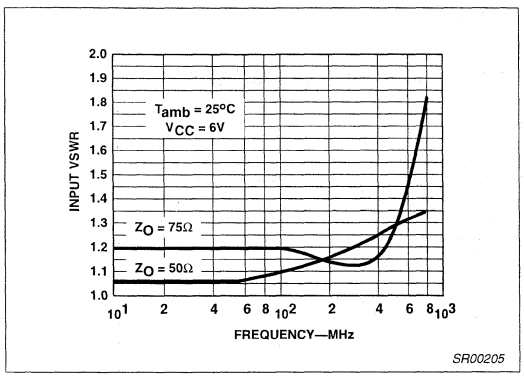


Figure 12. Output VSWR vs Frequency

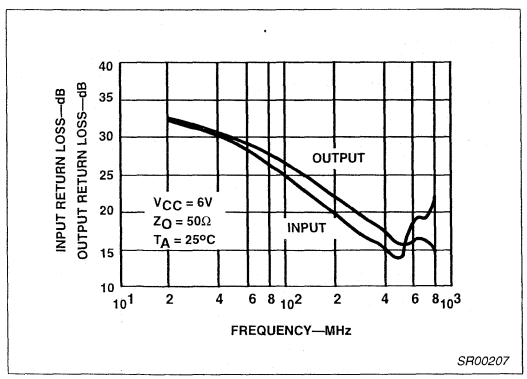


Figure 13. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

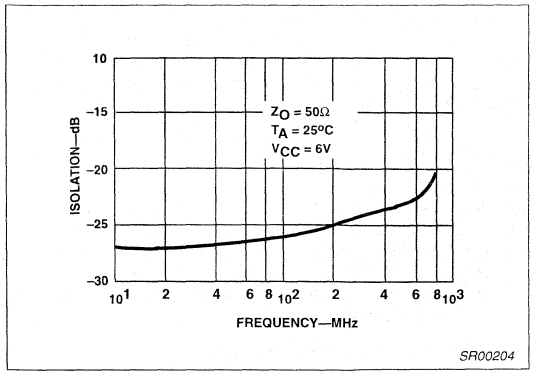


Figure 14. Isolation vs Frequency (S_{12})

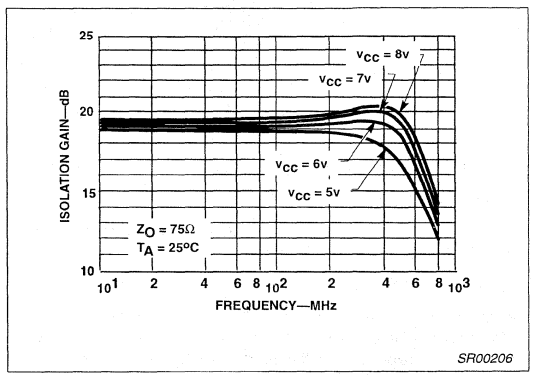


Figure 15. Insertion Gain vs Frequency (S_{21})

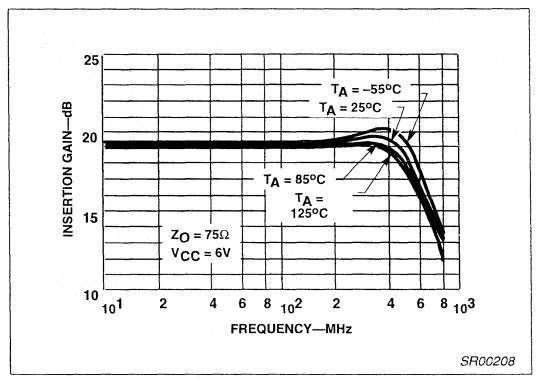


Figure 16. Insertion Gain vs Frequency (S_{21})

THEORY OF OPERATION

The design is based on the use of multiple feedback loops to provide wide-band gain together with good noise figure and terminal impedance matches. Referring to the circuit schematic in Figure 17, the gain is set primarily by the equation:

$$\frac{V_{OUT}}{V_{IN}} = (R_{F1} + R_{E1}) / R_{E1} \quad (1)$$

which is series-shunt feedback. There is also shunt-series feedback due to R_{F2} and R_{E2} which aids in producing wide-band terminal impedances without the need for low value input shunting resistors that would degrade the noise figure. For optimum noise performance, R_{E1} and the base resistance of Q_1 are kept as low as possible, while R_{F2} is maximized.

The noise figure is given by the following equation:

$$NF = 10Log\left[1 + \frac{\left[r_b + R_{E1} + \frac{KT}{2qI_{C1}}\right]}{R_O}\right] dB \quad (2)$$

where I_{C1}=5.5mA, R_{E1}=12Ω, r_b=130Ω, KT/q=26mV at 25°C and R_0=50 for a 50Ω system and 75 for a 75Ω system.

The DC input voltage level V_{IN} can be determined by the equation:

$$V_{IN}=V_{BE1}+(I_{C1}+I_{C3})\ R_{E1}(3)$$

where R_{E1}=12Ω, V_{BE}=0.8V, I_{C1}=5mA and I_{C3}=7mA (currents rated at V_{CC}=6V).

Under the above conditions, V_{IN} is approximately equal to 1V.

Level shifting is achieved by emitter-follower Q_3 and diode Q_4, which provide shunt feedback to the emitter of Q_1 via R_{F1}. The use of an emitter-follower buffer in this feedback loop essentially eliminates problems of shunt-feedback loading on the output. The value of R_{F1}=140Ω is chosen to give the desired nominal gain. The DC output voltage V_{OUT} can be determined by:

$$V_{OUT}=V_{CC}-(I_{C2}+I_{C6})R2,(4)$$

where V_{CC}=6V, R_2=225Ω, I_{C2}=8mA and I_{C6}=5mA.

From here, it can be seen that the output voltage is approximately 3.1V to give relatively equal positive and negative output swings. Diode Q_5 is included for bias purposes to allow direct coupling of R_{F2} to the base of Q_1. The dual feedback loops stabilize the DC operating point of the amplifier.

The output stage is a Darlington pair (Q_6 and Q_2) which increases the DC bias voltage on the input stage (Q_1) to a more desirable value, and also increases the feedback loop gain. Resistor R_0 optimizes the output VSWR (Voltage Standing Wave Ratio). Inductors L_1 and L_2 are bondwire and lead inductances which are roughly 3nH. These improve the high-frequency impedance matches at input and output by partially resonating with 0.5pF of pad and package capacitance.

POWER DISSIPATION CONSIDERATIONS

When using the part at elevated temperature, the engineer should consider the power dissipation capabilities.

At the nominal supply voltage of 6V, the typical supply current is 25mA (32mA max). For operation at supply voltages other than 6V, see Figure 3 for I_{CC} versus V_{CC} curves. The supply current is inversely proportional to temperature and varies no more than 1mA between 25°C and either temperature extreme. The change is 0.1% per °C over the range.

The recommended operating temperature ranges are air-mount specifications. Better heat-sinking benefits can be realized by mounting the SO package body against the PC board plane.

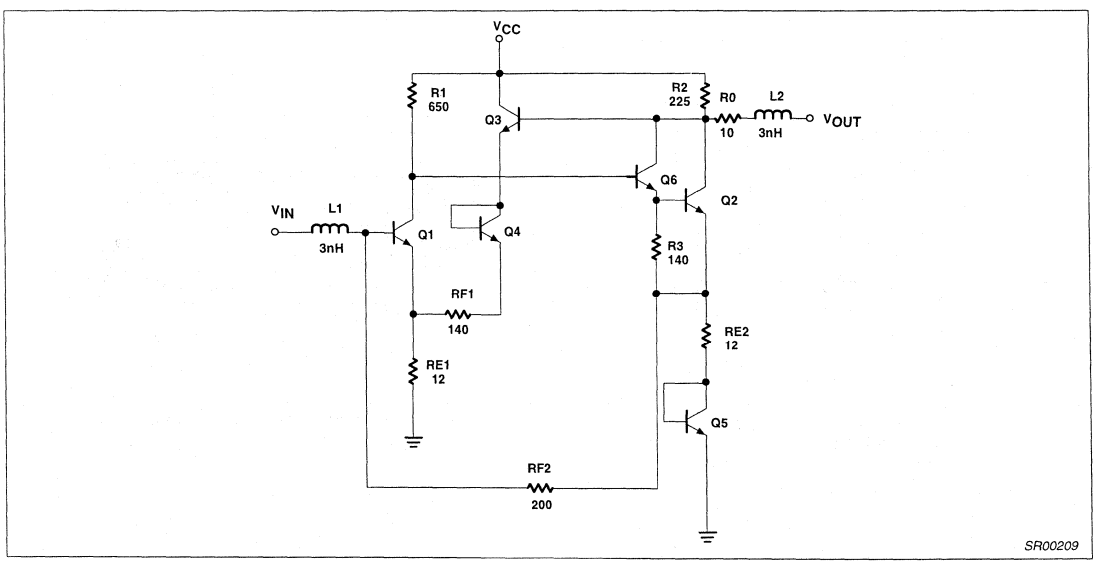


Figure 17. Schematic Diagram

PC BOARD MOUNTING

In order to realize satisfactory mounting of the SA5204A to a PC board, certain techniques need to be utilized. The board must be double-sided with copper and all pins must be soldered to their respective areas (i.e., all GND and V_{CC} pins on the package). The power supply should be decoupled with a capacitor as close to the V_{CC} pins as possible, and an RF choke should be inserted between the supply and the device. Caution should be exercised in the connection of input and output pins. Standard microstrip should be observed wherever possible. There should be no solder bumps or burrs or any obstructions in the signal path to cause launching problems. The path should be as straight as possible and lead lengths as short as possible from the part to the cable connection. Another important consideration is that the input and output should be AC-coupled. This is because at V_{CC}=6V, the input is approximately at 1V while the output is at 3.1V. The output must be decoupled into a low-impedance system, or the DC bias on the output of the amplifier will be loaded down, causing loss of output power. The easiest way to decouple the entire amplifier is by soldering a high-frequency chip capacitor directly to the input and output pins of the device. This circuit is shown in Figure 18. Follow these recommendations to get the best frequency response and noise immunity. The board design is as important as the integrated circuit design itself.

SCATTERING PARAMETERS

The primary specifications for the SA5204A are listed as S-parameters. S-parameters are measurements of incident and reflected currents and voltages between the source, amplifier, and load as well as transmission losses. The parameters for a two-port network are defined in Figure 19.

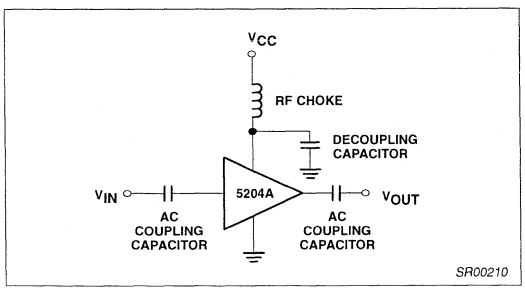
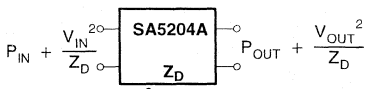


Figure 18. Circuit Schematic for Coupling and Power Supply Decoupling

Actual S-parameter measurements using an HP network analyzer (model 8505A) and an HP S-parameter tester (models 8503A/B) are shown in Figure 20.

Values for the figures below are measured and specified in the data sheet to ease adaptation and comparison of the SA5204A to other high-frequency amplifiers.
The most important parameter is S_{21}. It is defined as the square root of the power gain, and, in decibels, is equal to voltage gain as shown below:

$Z_D=Z_{IN}=Z_{OUT}$ for the SA5204A



$$\therefore \frac{P_{OUT}}{P_{IN}} = \frac{\frac{V_{OUT}^2}{Z_D}}{\frac{V_{IN}^2}{Z_D}} = \frac{V_{OUT}^2}{V_{IN}^2} = P_I$$

$P_I=V_I{}^2$

P_I=Insertion Power Gain

V_I=Insertion Voltage Gain

Measured value for the SA5204A = $|S_{21}|^2 = 100$

$$\therefore P_I = \frac{P_{OUT}}{P_{IN}} = |S_{21}|^2 = 100$$

$$\text{and } V_I = \frac{V_{OUT}}{V_{IN}} = \sqrt{P_I} = S_{21} = 10$$

In decibels:

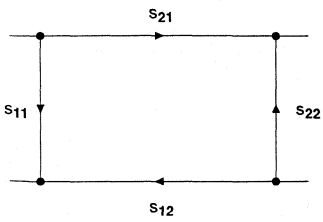
$P_{I(dB)} = 10 \text{ Log } |S_{21}|^2 = 20\text{dB}$

$V_{I(dB)} = 20 \text{ Log } S_{21} = 20\text{dB}$

$\therefore P_{I(dB)} = V_{I(dB)} = S_{21(dB)} = 20\text{dB}$

Also measured on the same system are the respective voltage standing wave ratios. These are shown in Figure 21. The VSWR can be seen to be below 1.5 across the entire operational frequency range.

Relationships exist between the input and output return losses and the voltage standing wave ratios. These relationships are as follows:



a. Two-Port Network Defined

S_{11} — INPUT RETURN LOSS

$$S_{11} = \sqrt{\frac{\text{POWER REFLECTED FROM INPUT PORT}}{\text{POWER AVAILABLE FROM GENERATOR AT INPUT PORT}}}$$

S_{12} — REVERSE TRANSMISSION LOSS OSOLATION

$$S_{12} = \sqrt{\text{REVERSE TRANSDUCER POWER GAIN}}$$

S_{21} — FORWARD TRANSMISSION LOSS OR INSERTION GAIN

$$S_{21} = \sqrt{\text{TRANSDUCER POWER GAIN}}$$

S_{22} — OUTPUT RETURN LOSS

$$S_{22} = \sqrt{\frac{\text{POWER REFLECTED FROM OUTPUT PORT}}{\text{POWER AVAILABLE FROM GENERATOR AT OUTPUT PORT}}}$$

b.

SR00211

Figure 19.

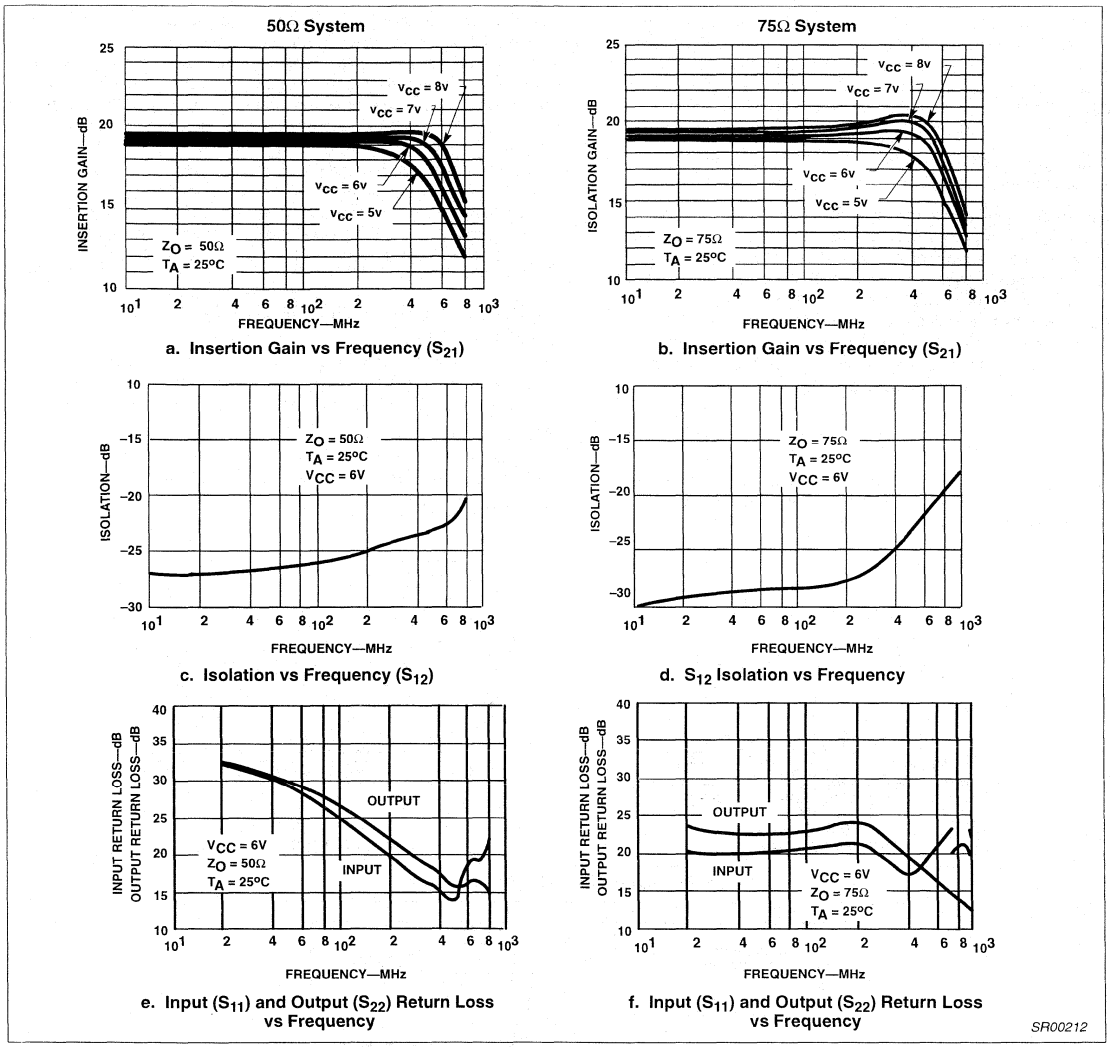


Figure 20.

INPUT RETURN LOSS=S_{11}dB
S_{11}dB=20 Log | S_{11} |

OUTPUT RETURN LOSS=S_{22}dB
S_{22}dB=20 Log | S_{22} |

INPUT VSWR=≤1.5

OUTPUT VSWR=≤1.5

1DB GAIN COMPRESSION AND SATURATED OUTPUT POWER

The 1dB gain compression is a measurement of the output power level where the small-signal insertion gain magnitude decreases 1dB from its low power value. The decrease is due to nonlinearities in the amplifier, an indication of the point of transition between small-signal operation and the large signal mode.

The saturated output power is a measure of the amplifier's ability to deliver power into an external load. It is the value of the amplifier's output power when the input is heavily overdriven. This includes the sum of the power in all harmonics.

INTERMODULATION INTERCEPT TESTS

The intermodulation intercept is an expression of the low level linearity of the amplifier. The intermodulation ratio is the difference in dB between the fundamental output signal level and the generated distortion product level. The relationship between intercept and

intermodulation ratio is illustrated in Figure 22, which shows product output levels plotted versus the level of the fundamental output for two equal strength output signals at different frequencies. The upper line shows the fundamental output plotted against itself with a 1dB to 1dB slope. The second and third order products lie below the fundamentals and exhibit a 2:1 and 3:1 slope, respectively.

The intercept point for either product is the intersection of the extensions of the product curve with the fundamental output.

The intercept point is determined by measuring the intermodulation ratio at a single output level and projecting along the appropriate product slope to the point of intersection with the fundamental. When the intercept point is known, the intermodulation ratio can be determined by the reverse process. The second order IMR is equal to the difference between the second order intercept and the fundamental output level. The third order IMR is equal to twice the difference between the third order intercept and the fundamental output level. These are expressed as:

$IP_2 = P_{OUT} + IMR_2$

$IP_3 = P_{OUT} + IMR_3/2$

where P_{OUT} is the power level in dBm of each of a pair of equal level fundamental output signals, IP_2 and IP_3 are the second and third order output intercepts in dBm, and IMR_2 and IMR_3 are the second and third order intermodulation ratios in dB. The intermodulation intercept is an indicator of intermodulation performance only in the small signal operating range of the amplifier. Above some output level which is below the 1dB compression point, the active device moves into large-signal operation. At this point the intermodulation products no longer follow the straight line output slopes, and the intercept description is no longer valid. It is therefore important to measure IP_2 and IP_3 at output levels well below 1dB compression. One must be careful, however, not to select too low levels because the test equipment may not be able to recover the signal from the noise. For the SA5204A we have chosen an output level of –10.5dBm with fundamental frequencies of 100.000 and 100.01MHz, respectively.

ADDITIONAL READING ON SCATTERING PARAMETERS

For more information regarding S-parameters, please refer to High-Frequency Amplifiers by Ralph S. Carson of the University of Missouri, Rolla, Copyright 1985; published by John Wiley & Sons, Inc.

"S-Parameter Techniques for Faster, More Accurate Network Design", HP App Note 95-1, Richard W. Anderson, 1967, HP Journal.

"S-Parameter Design", HP App Note 154, 1972.

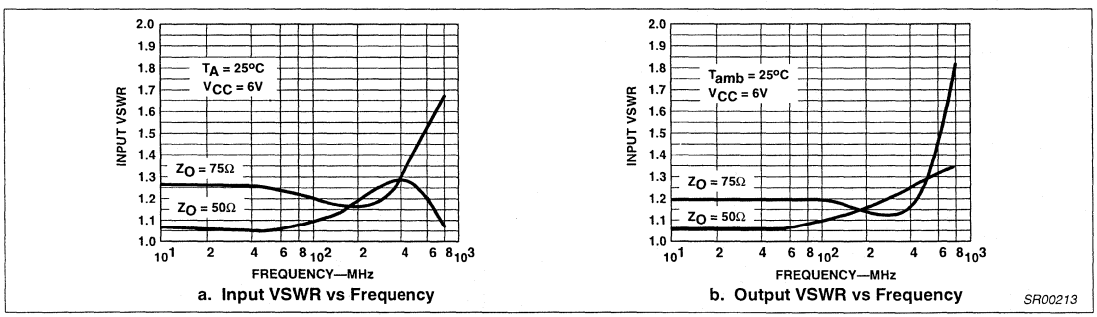


Figure 21. Input/Output VSWR vs Frequency

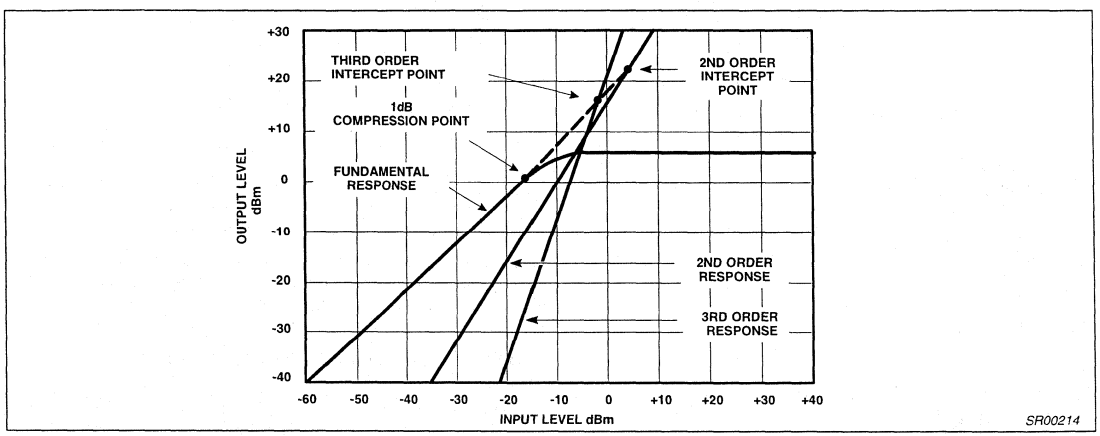


Figure 22.

Wide-band high-frequency amplifier SA5205A

DESCRIPTION

The SA5205A family of wideband amplifiers replace the SA5205 family. The 'A' parts are fabricated on a rugged 2µm bipolar process featuring excellent statistical process control. Electrical performance is nominally identical to the original parts.

The SA5205A is a high-frequency amplifier with a fixed insertion gain of 20dB. The SA5205A operates with a single supply of 6V, and only draws 24mA of supply current, which is much less than comparable hybrid parts. The noise figure is 4.8dB in a 75Ω system and 6dB in a 50Ω system.

Until now, most RF or high-frequency designers had to settle for discrete or hybrid solutions to their amplification problems. Most of these solutions required trade-offs that the designer had to accept in order to use high-frequency gain stages. These include high-power consumption, large component count, transformers, large packages with heat sinks, and high part cost. The SA5205A solves these problems by incorporating a wide-band amplifier on a single monolithic chip.

The part is well matched to 50 or 75Ω input and output impedances. The Standing Wave Ratios in 50 and 75Ω systems do not exceed 1.5 on either the input or output from DC to the -3dB bandwidth limit.

Since the part is a small monolithic IC die, problems such as stray capacitance are minimized. The die size is small enough to fit into a very cost-effective 8-pin small-outline (SO) package to further reduce parasitic effects.

No external components are needed other than AC coupling capacitors because the SA5205A is internally compensated and matched to 50 and 75Ω. The amplifier has very good distortion specifications, with second and third-order intermodulation intercepts of +24dBm and +17dBm respectively at 100MHz.

The device is ideally suited for 75Ω cable television applications such as decoder boxes, satellite receiver/decoders, and front-end amplifiers for TV receivers. It is also useful for amplified splitters and antenna amplifiers.

The part is matched well for 50Ω test equipment such as signal generators, oscilloscopes, frequency counters and all kinds of signal analyzers. Other applications at 50Ω include mobile radio, CB radio and data/video transmission in fiber optics, as well as broad-band LANs and telecom systems. A gain greater than 20dB can be achieved by cascading additional SA5205As in series as required, without any degradation in amplifier stability.

PIN CONFIGURATIONS

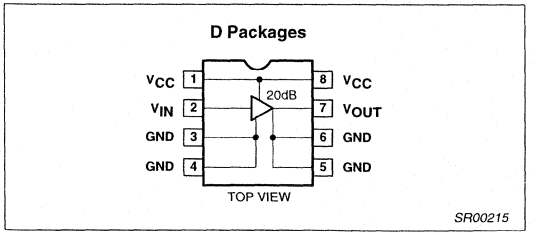


Figure 1. Pin Configuration

FEATURES

- 600MHz bandwidth
- 20dB insertion gain
- 4.8dB (6dB) noise figure ZO=75Ω (ZO=50Ω)
- No external components required
- Input and output impedances matched to 50/75Ω systems
- 2000V ESD protection

APPLICATIONS

- 75Ω cable TV decoder boxes
- Antenna amplifiers
- Amplified splitters
- Signal generators
- Frequency counters
- Oscilloscopes
- Signal analyzers
- Broad-band LANs
- Fiber-optics
- Modems
- Mobile radio
- Security systems
- Telecommunications

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Small Outline (SO) package	-40 to +85°C	SA5205AD	SOT96-1

EQUIVALENT SCHEMATIC

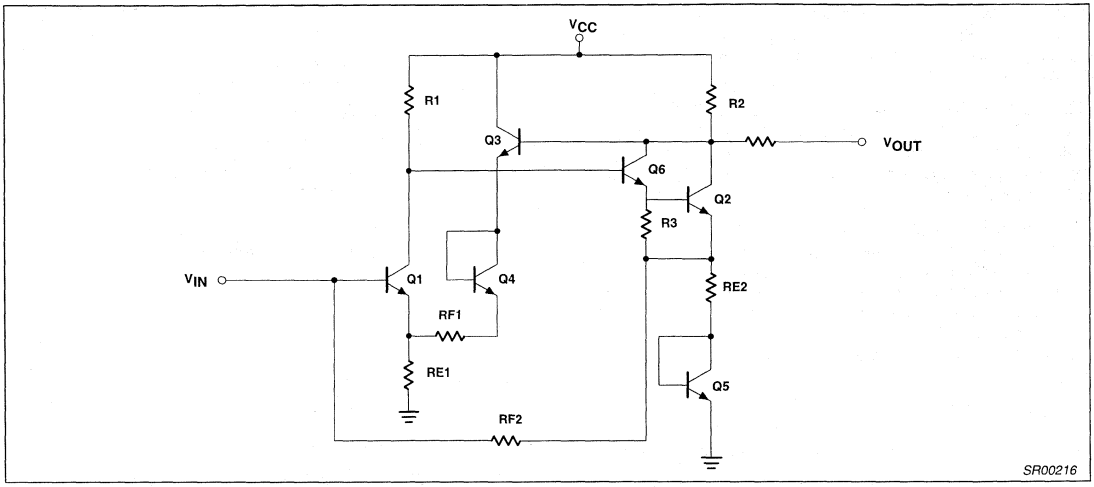


Figure 2. Equivalent Schematic

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	9	V
V_{AC}	AC input voltage	5	V_{P-P}
T_A	Operating ambient temperature range SA grade	-40 to +85	°C
P_{DMAX}	Maximum power dissipation, T_A=25°C (still-air)[1, 2] D package	780	mW

NOTES:
1. Derate above 25°C, at the following rates:
   D package at 6.2mW/°C
2. See "Power Dissipation Considerations" section.

DC ELECTRICAL CHARACTERISTICS

V_{CC}=6V, Z_S=Z_L=Z_O=50Ω and T_A=25°C in all packages, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SA5205A			UNIT
			Min	Typ	Max	
V_{CC}	Operating supply voltage range		5		8	V
		Over temperature	5		8	V
I_{CC}	Supply current		20	25	32	mA
		Over temperature	19	25	33	mA
S21	Insertion gain	f=100MHz	17	19	21	dB
		Over temperature	16.5		21.5	
S11	Input return loss	f=100MHz		25		dB
		DC - f_{MAX}	12			
S22	Output return loss	f=100MHz		27		dB
		DC - f_{MAX}	12			
S12	Isolation	f=100MHz		-25		dB
		DC - f_{MAX}	-18			
t_R	Rise time			500		ps
t_P	Propagation delay			500		ps
BW	Bandwidth	±0.5dB		450		MHz
f_{MAX}	Bandwidth	-3dB	550			MHz
	Noise figure (75Ω)	f=100MHz		4.8		dB
	Noise figure (50Ω)	f=100MHz		6.0		dB
	Saturated output power	f=100MHz		+7.0		dBm
	1dB gain compression	f=100MHz		+4.0		dBm
	Third-order intermodulation intercept (output)	f=100MHz		+17		dBm
	Second-order intermodulation intercept (output)	f=100MHz		+24		dBm

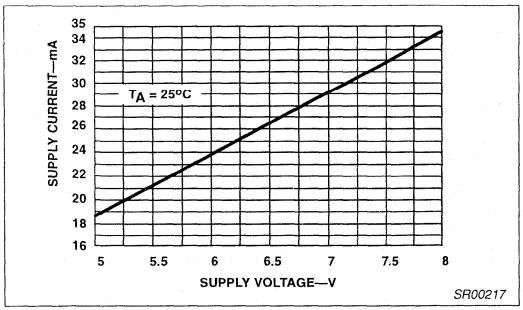


Figure 3. Supply Current vs Supply Voltage

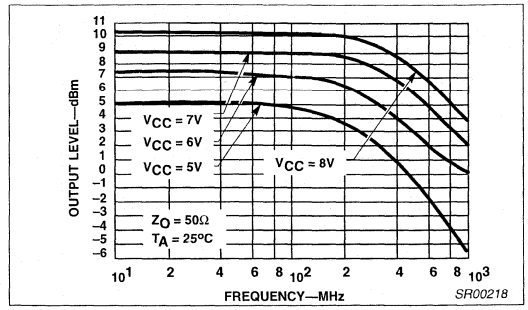


Figure 7. Saturated Output Power vs Frequency

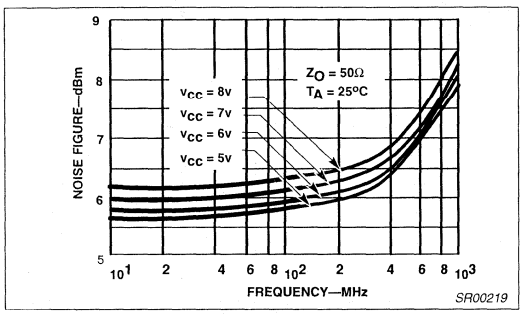


Figure 4. Noise Figure vs Frequency

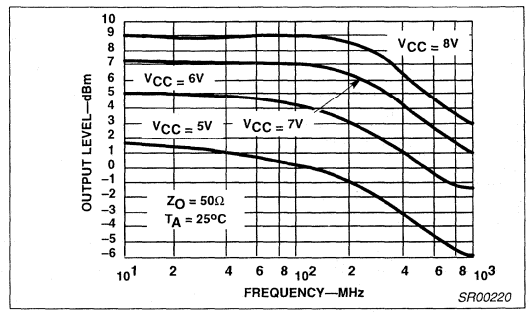


Figure 8. 1dB Gain Compression vs Frequency

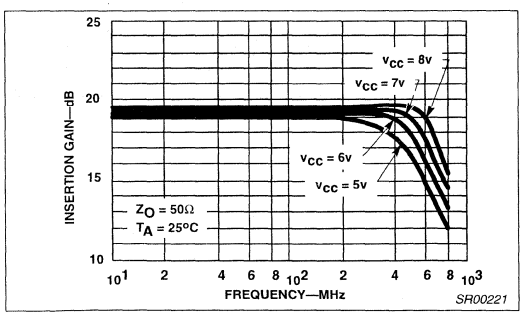


Figure 5. Insertion Gain vs Frequency (S_{21})

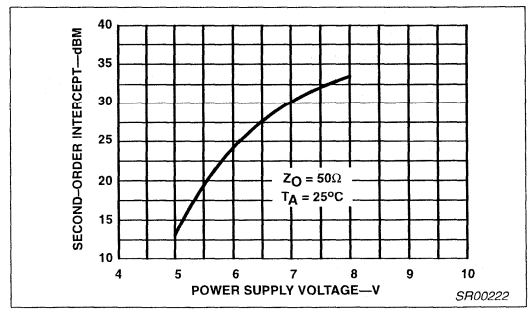


Figure 9. Second-Order Output Intercept vs Supply Voltage

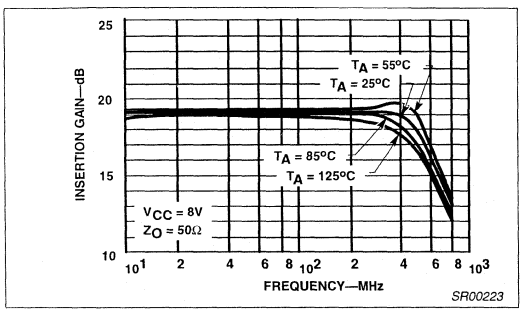


Figure 6. Insertion Gain vs Frequency (S_{21})

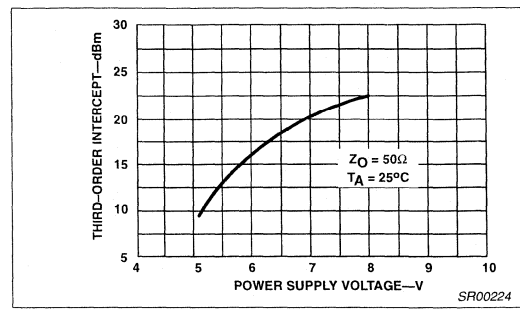


Figure 10. Third-Order Intercept vs Supply Voltage

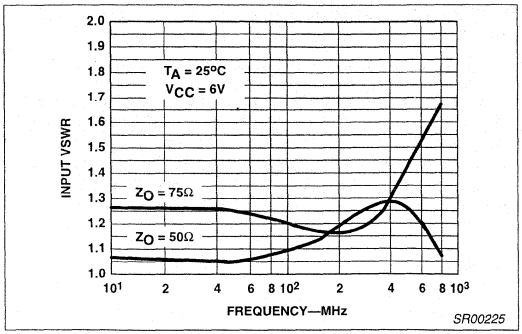


Figure 11. Input VSWR vs Frequency

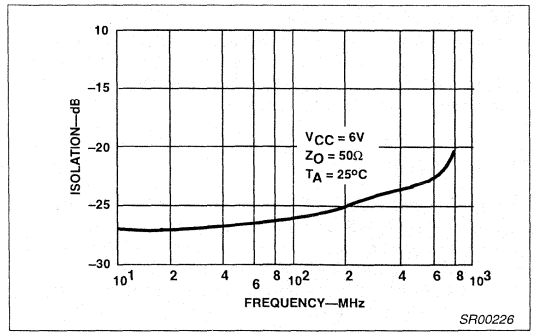


Figure 14. Isolation vs Frequency (S_{12})

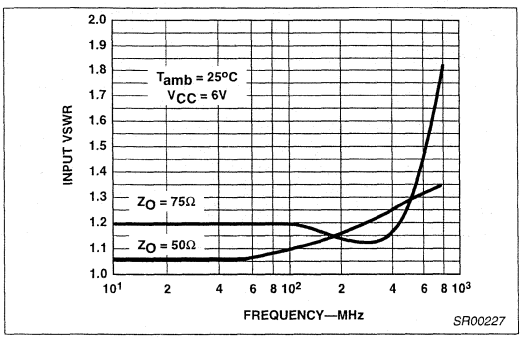


Figure 12. Output VSWR vs Frequency

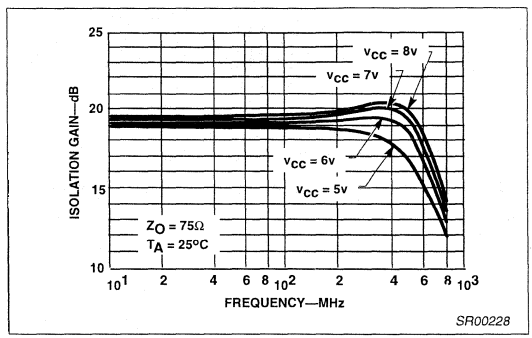


Figure 15. Insertion Gain vs Frequency (S_{21})

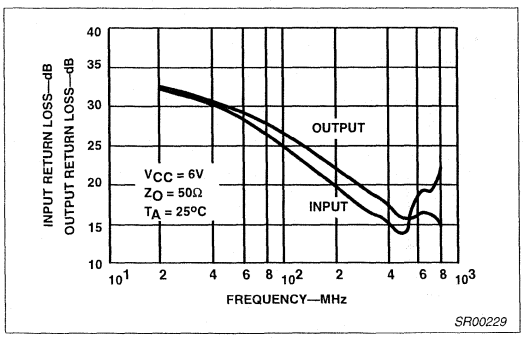


Figure 13. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

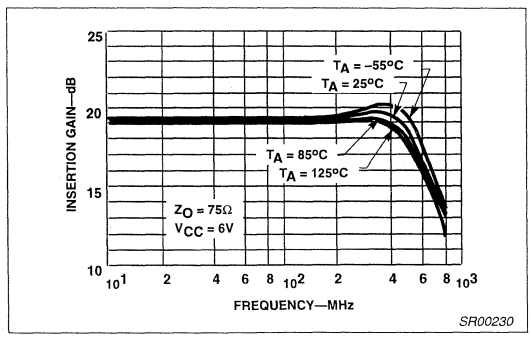


Figure 16. Insertion Gain vs Frequency (S_{21})

THEORY OF OPERATION

The design is based on the use of multiple feedback loops to provide wide-band gain together with good noise figure and terminal impedance matches. Referring to the circuit schematic in Figure 17, the gain is set primarily by the equation:

$$\frac{V_{OUT}}{V_{IN}} = \frac{(R_{F1} + R_{E1})}{R_{E1}} \quad (1)$$

which is series-shunt feedback. There is also shunt-series feedback due to R_{F2} and R_{E2} which aids in producing wideband terminal impedances without the need for low value input shunting resistors that would degrade the noise figure. For optimum noise performance, R_{E1} and the base resistance of Q_1 are kept as low as possible while R_{F2} is maximized.

The noise figure is given by the following equation:

NF =

$$10 \log \left[1 + \left[\frac{r_b + R_{E1} + \frac{KT}{2qI_{C1}}}{R_O} \right] \right] dB \quad (2)$$

where I_{C1}=5.5mA, R_{E1}=12Ω, r_b=130Ω, KT/q=26mV at 25°C and R_O=50 for a 50Ω system and 75 for a 75Ω system.

The DC input voltage level V_{IN} can be determined by the equation:

$$V_{IN}=V_{BE1}+(I_{C1}+I_{C3})\ R_{E1}$$

where R_{E1}=12Ω, V_{BE}=0.8V, I_{C1}=5mA and I_{C3}=7mA (currents rated at V_{CC}=6V).

Under the above conditions, V_{IN} is approximately equal to 1V.

Level shifting is achieved by emitter-follower Q_3 and diode Q_4 which provide shunt feedback to the emitter of Q_1 via R_{F1}. The use of an emitter-follower buffer in this feedback loop essentially eliminates problems of shunt feedback loading on the output. The value of R_{F1}=140Ω is chosen to give the desired nominal gain. The DC output voltage V_{OUT} can be determined by:

$$V_{OUT}=V_{CC}-(I_{C2}+I_{C6})R2, \quad (4)$$

where V_{CC}=6V, R_2=225Ω, I_{C2}=8mA and I_{C6}=5mA.

From here it can be seen that the output voltage is approximately 3.1V to give relatively equal positive and negative output swings. Diode Q_5 is included for bias purposes to allow direct coupling of R_{F2} to the base of Q_1. The dual feedback loops stabilize the DC operating point of the amplifier.

The output stage is a Darlington pair (Q_6 and Q_2) which increases the DC bias voltage on the input stage (Q_1) to a more desirable value, and also increases the feedback loop gain. Resistor R_0 optimizes the output VSWR (Voltage Standing Wave Ratio). Inductors L_1 and L_2 are bondwire and lead inductances which are roughly 3nH. These improve the high-frequency impedance matches at input and output by partially resonating with 0.5pF of pad and package capacitance.

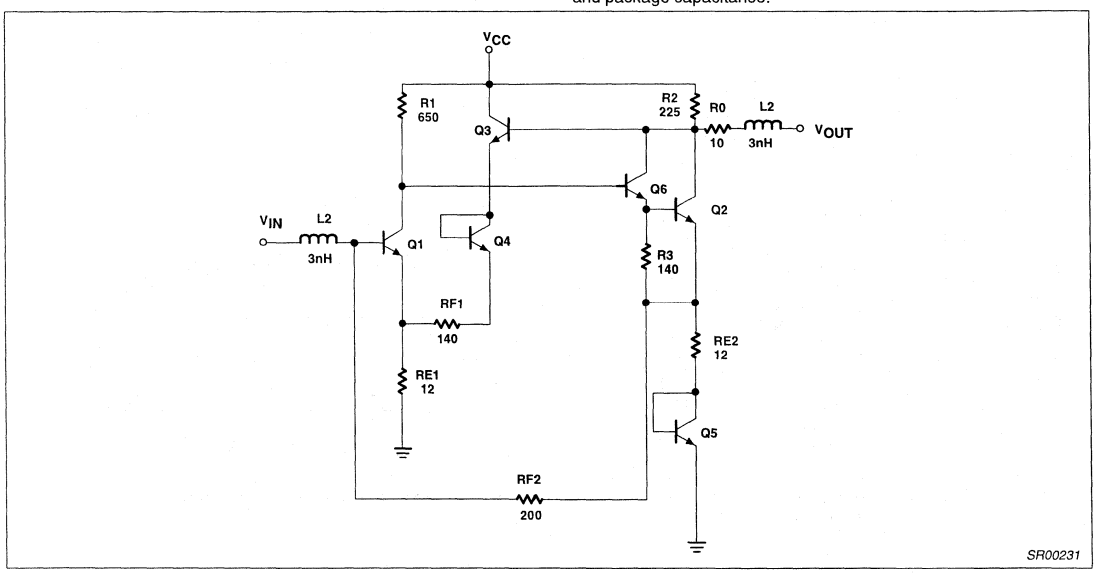


Figure 17. Schematic Diagram

POWER DISSIPATION CONSIDERATIONS

When using the part at elevated temperature, the engineer should consider the power dissipation capabilities.

At the nominal supply voltage of 6V, the typical supply current is 25mA (32mA Max). For operation at supply voltages other than 6V, see Figure 3 for I_{CC} versus V_{CC} curves. The supply current is inversely proportional to temperature and varies no more than 1mA between 25°C and either temperature extreme. The change is 0.1% per over the range.

The recommended operating temperature ranges are air-mount specifications. Better heat sinking benefits can be realized by mounting the D package body against the PC board plane.

PC BOARD MOUNTING

In order to realize satisfactory mounting of the SA5205A to a PC board, certain techniques need to be utilized. The board must be double-sided with copper and all pins must be soldered to their respective areas (i.e., all GND and V_{CC} pins on the SO package). The power supply should be decoupled with a capacitor as close to the V_{CC} pins as possible and an RF choke should be inserted between the supply and the device. Caution should be exercised in the connection of input and output pins. Standard microstrip should be observed wherever possible. There should be no solder bumps or burrs or any obstructions in the signal path to cause launching problems. The path should be as straight as possible and lead lengths as short as possible from the part to the cable connection. Another important consideration is that the input and output should be AC coupled. This is because at V_{CC}=6V, the input is approximately at 1V while the output is at 3.1V. The output must be decoupled into a low impedance system or the DC bias on the output of the amplifier will be loaded down causing loss of output power. The easiest way to decouple the entire amplifier is by soldering a high frequency chip capacitor directly to the input and output pins of the device. This circuit is shown in Figure 18. Follow these recommendations to get the best frequency response and noise immunity. The board design is as important as the integrated circuit design itself.

SCATTERING PARAMETERS

The primary specifications for the SA5205A are listed as S-parameters. S-parameters are measurements of incident and reflected currents and voltages between the source, amplifier and load as well as transmission losses. The parameters for a two-port network are defined in Figure 19.

Actual S-parameter measurements using an HP network analyzer (model 8505A) and an HP S-parameter tester (models 8503A/B) are shown in Figure 20.

Values for the figures below are measured and specified in the data sheet to ease adaptation and comparison of the SA5205A to other high-frequency amplifiers.

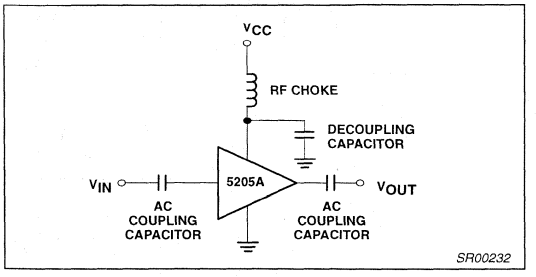


Figure 18. Circuit Schematic for Coupling and Power Supply Decoupling

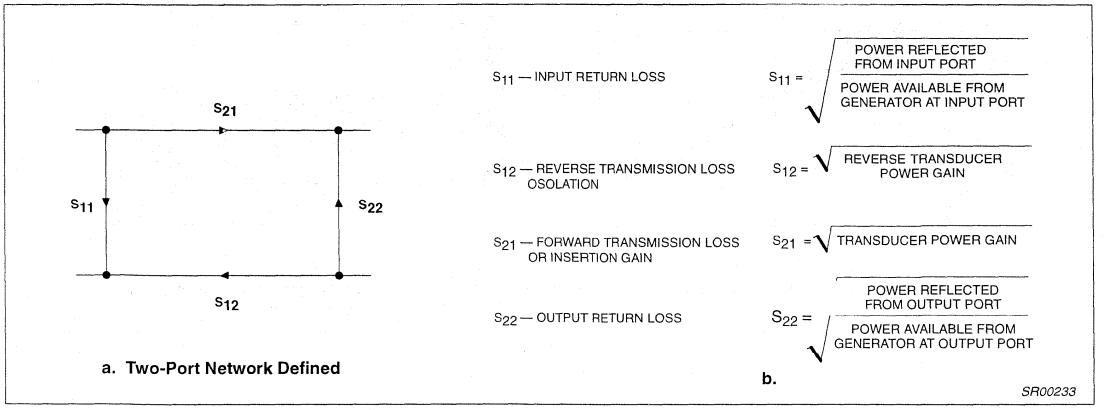
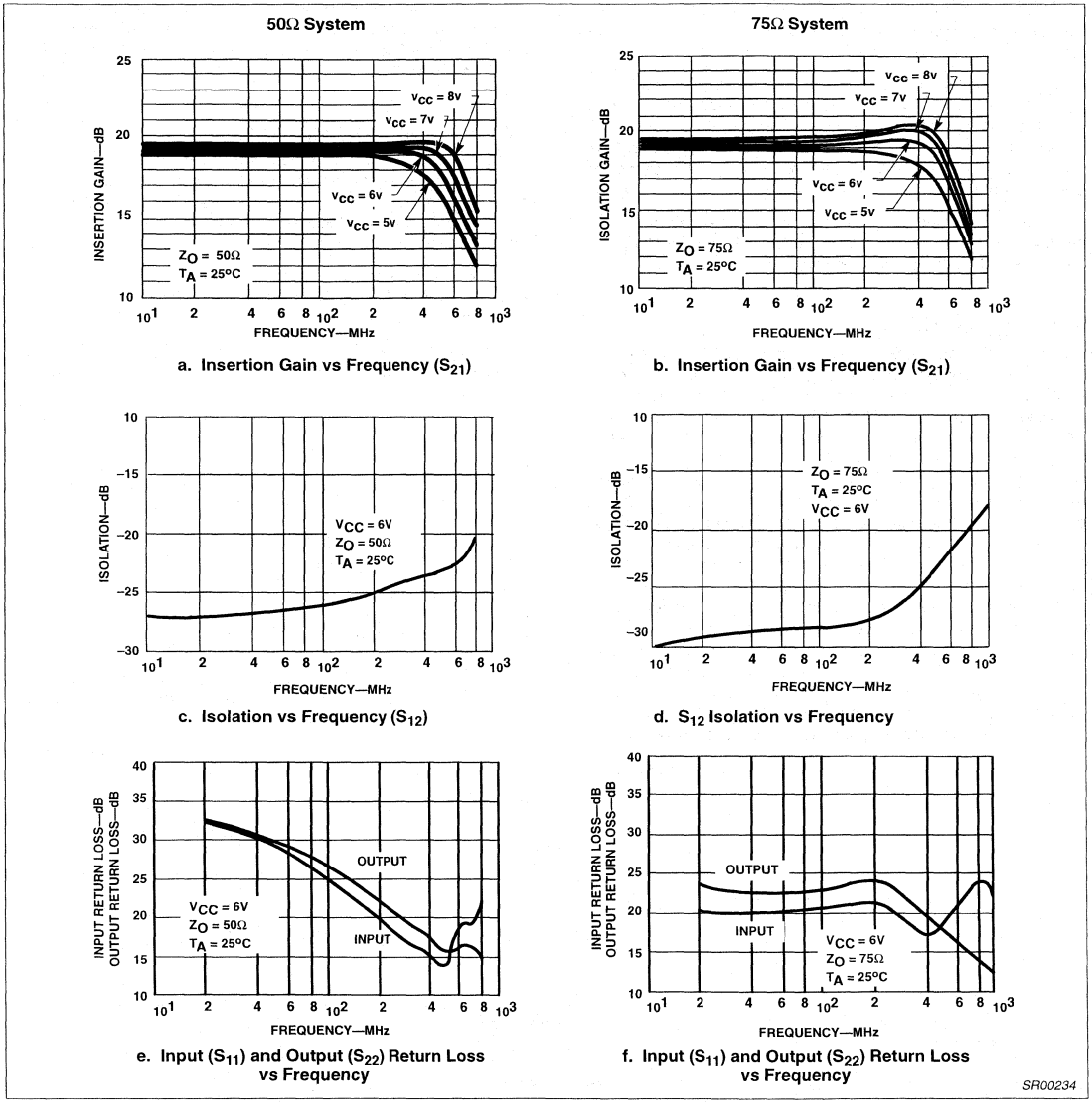


Figure 19.



a. Insertion Gain vs Frequency (S_{21})

b. Insertion Gain vs Frequency (S_{21})

c. Isolation vs Frequency (S_{12})

d. S_{12} Isolation vs Frequency

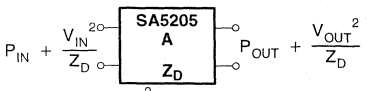
e. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

f. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

Figure 20.

The most important parameter is S_{21}. It is defined as the square root of the power gain, and, in decibels, is equal to voltage gain as shown below:

$Z_D=Z_{IN}=Z_{OUT}$ for the SA5205A



$$\therefore \frac{P_{OUT}}{P_{IN}} = \frac{\frac{V_{OUT}^2}{Z_D}}{\frac{V_{IN}^2}{Z_D}} = \frac{V_{OUT}^2}{V_{IN}^2} = P_I$$

$P_I=V_I{}^2$

P_I=Insertion Power Gain

V_I=Insertion Voltage Gain

Measured value for the SA5205A = $|S_{21}|^2 = 100$

$$\therefore P_I = \frac{P_{OUT}}{P_{IN}} = |S_{21}|^2 = 100$$

$$\text{and } V_I = \frac{V_{OUT}}{V_{IN}} = \sqrt{P_I} = S_{21} = 10$$

In decibels:

$P_{I(dB)} = 10 \text{ Log } |S_{21}|^2 = 20\text{dB}$

$V_{I(dB)} = 20 \text{ Log } S_{21} = 20\text{dB}$

$\therefore P_{I(dB)} = V_{I(dB)} = S_{21(dB)} = 20\text{dB}$

Also measured on the same system are the respective voltage standing wave ratios. These are shown in Figure 21. The VSWR can be seen to be below 1.5 across the entire operational frequency range.

Relationships exist between the input and output return losses and the voltage standing wave ratios. These relationships are as follows:

INPUT RETURN LOSS=S_{11}dB

S_{11}dB=20 Log $|S_{11}|$

OUTPUT RETURN LOSS=S_{22}dB

S_{22}dB=20 Log $|S_{22}|$

INPUT VSWR=≤1.5

OUTPUT VSWR=≤1.5

1dB GAIN COMPRESSION AND SATURATED OUTPUT POWER

The 1dB gain compression is a measurement of the output power level where the small-signal insertion gain magnitude decreases 1dB from its low power value. The decrease is due to nonlinearities in the amplifier, an indication of the point of transition between small-signal operation and the large signal mode.

The saturated output power is a measure of the amplifier's ability to deliver power into an external load. It is the value of the amplifier's output power when the input is heavily overdriven. This includes the sum of the power in all harmonics.

INTERMODULATION INTERCEPT TESTS

The intermodulation intercept is an expression of the low level linearity of the amplifier. The intermodulation ratio is the difference in dB between the fundamental output signal level and the generated distortion product level. The relationship between intercept and intermodulation ratio is illustrated in Figure 22, which shows product output levels plotted versus the level of the fundamental output for two equal strength output signals at different frequencies. The upper line shows the fundamental output plotted against itself with a 1dB to 1dB slope. The second and third order products lie below the fundamentals and exhibit a 2:1 and 3:1 slope, respectively.

The intercept point for either product is the intersection of the extensions of the product curve with the fundamental output.

The intercept point is determined by measuring the intermodulation ratio at a single output level and projecting along the appropriate product slope to the point of intersection with the fundamental. When the intercept point is known, the intermodulation ratio can be determined by the reverse process. The second order IMR is equal to the difference between the second order intercept and the fundamental output level. The third order IMR is equal to twice the difference between the third order intercept and the fundamental output level. These are expressed as:

$IP_2=P_{OUT}+IMR_2$

$IP_3=P_{OUT}+IMR_3/2$

where P_{OUT} is the power level in dBm of each of a pair of equal level fundamental output signals, IP_2 and IP_3 are the second and third order output intercepts in dBm, and IMR_2 and IMR_3 are the second and third order intermodulation ratios in dB. The intermodulation intercept is an indicator of intermodulation performance only in the small signal operating range of the amplifier. Above some output level which is below the 1dB compression point, the active device moves into large-signal operation. At this point the intermodulation products no longer follow the straight line output slopes, and the intercept description is no longer valid. It is therefore important to measure IP_2 and IP_3 at output levels well below 1dB compression. One must be careful, however, not to select too low levels because the test equipment may not be able to recover the signal from the noise. For the SA5205A we have chosen an output level of -10.5dBm with fundamental frequencies of 100.000 and 100.01MHz, respectively.

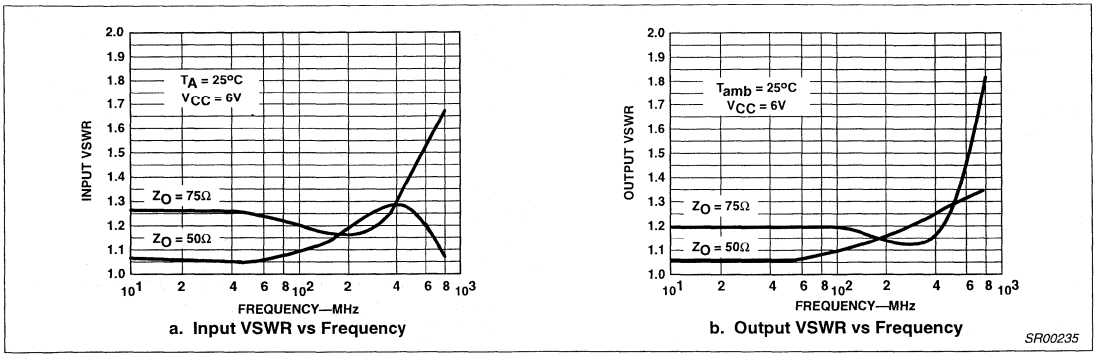


Figure 21. Input/Output VSWR vs Frequency

ADDITIONAL READING ON SCATTERING PARAMETERS

For more information regarding S-parameters, please refer to High-Frequency Amplifiers by Ralph S. Carson of the University of Missouri, Rolla, Copyright 1985; published by John Wiley & Sons, Inc.

"S-Parameter Techniques for Faster, More Accurate Network Design", HP App Note 95-1, Richard W. Anderson, 1967, HP Journal.

"S-Parameter Design", HP App Note 154, 1972.

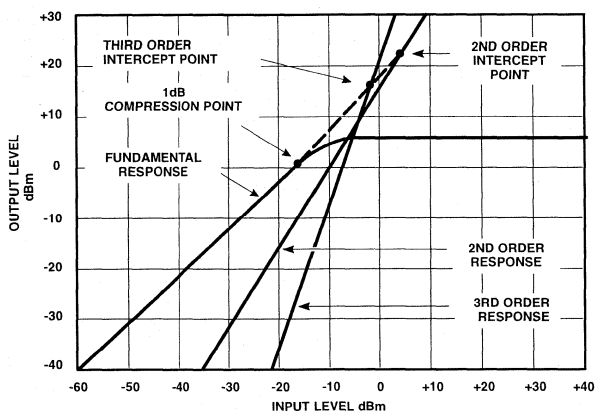


Figure 22.

Wideband variable gain amplifier SA5209

DESCRIPTION

The SA5209 represents a breakthrough in monolithic amplifier design featuring several innovations. This unique design has combined the advantages of a high speed bipolar process with the proven Gilbert architecture.

The SA5209 is a linear broadband RF amplifier whose gain is controlled by a single DC voltage. The amplifier runs off a single 5 volt supply and consumes only 40mA. The amplifier has high impedance (1kΩ) differential inputs. The output is 50Ω differential. Therefore, the 5209 can simultaneously perform AGC, impedance transformation, and the balun functions.

The dynamic range is excellent over a wide range of gain setting. Furthermore, the noise performance degrades at a comparatively slow rate as the gain is reduced. This is an important feature when building linear AGC systems.

PIN CONFIGURATION

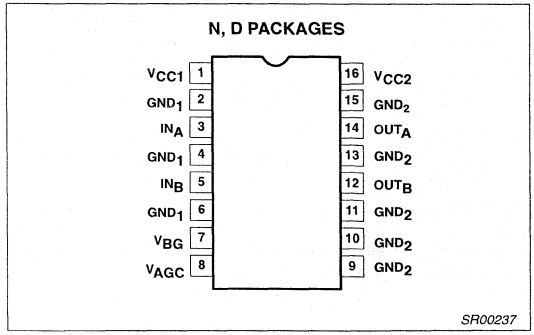


Figure 1. Pin Configuration

FEATURES

- Gain to 1.5GHz
- 850MHz bandwidth
- High impedance differential input
- 50Ω differential output
- Single 5V power supply
- 0 - 1V gain control pin
- >60dB gain control range at 200MHz
- 26dB maximum gain differential
- Exceptional $V_{CONTROL}$ / V_{GAIN} linearity
- 7dB noise figure minimum
- Full ESD protection
- Easily cascadable

APPLICATIONS

- Linear AGC systems
- Very linear AM modulator
- RF balun
- Cable TV multi-purpose amplifier
- Fiber optic AGC
- RADAR
- User programmable fixed gain block
- Video
- Satellite receivers
- Cellular communications

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Small Outline (SO) package	-40 to +85°C	SA5209D	SOT109-1
16-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA5209N	SOT38-4

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	-0.5 to +8.0	V
P_D	Power dissipation, T_A = 25°C (still air)[1] 16-Pin Plastic DIP 16-Pin Plastic SO	 1450 1100	 mW mW
T_{JMAX}	Maximum operating junction temperature	150	°C
T_{STG}	Storage temperature range	-65 to +150	°C

NOTES:
1. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance, θ_{JA}:
   16-Pin DIP: θ_{JA} = 85°C/W
   16-Pin SO: θ_{JA} = 110°C/W

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	V_{CC1} = V_{CC2} = 4.5 to 7.0V	V
T_A	Operating ambient temperature range SA Grade	-40 to +85	°C
T_J	Operating junction temperature range SA Grade	-40 to +105	°C

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC1} = V_{CC2} = +5V, V_{AGC} = 1.0V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
I_{CC}	Supply current	DC tested	38	43	48	mA
		Over temperature[1]	30		55	
A_V	Voltage gain (single-ended in/single-ended out)	DC tested, R_L = 10kΩ	17	19	21	dB
		Over temperature[1]	16		22	
A_V	Voltage gain (single-ended in/differential out)	DC tested, R_L = 10kΩ	23	25	27	dB
		Over temperature[1]	22		28	
R_{IN}	Input resistance (single-ended)	DC tested at ±50µA	0.9	1.2	1.5	kΩ
		Over temperature[1]	0.8		1.7	
R_{OUT}	Output resistance (single-ended)	DC tested at ±1mA	40	60	75	Ω
		Over temperature[1]	35		90	
V_{OS}	Output offset voltage (output referred)			±20	±100	mV
		Over temperature[1]			±250	
V_{IN}	DC level on inputs		1.6	2.0	2.4	V
		Over temperature[1]	1.4		2.6	
V_{OUT}	DC level on outputs		1.9	2.4	2.9	V
		Over temperature[1]	1.7		3.1	
PSRR	Output offset supply rejection ratio (output referred)		20	45		dB
		Over temperature[1]	15			
V_{BG}	Bandgap reference voltage	4.5V<V_{CC}<7V R_{BG} = 10kΩ	1.2	1.32	1.45	V
		Over temperature[1]	1.1		1.55	

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC1} = V_{CC2} = +5.0V, V_{AGC} = 1.0V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
R_{BG}	Bandgap loading	Over temperature[1]	2	10		kΩ
V_{AGC}	AGC DC control voltage range	Over temperature[1]		0-1.3		V
I_{BAGC}	AGC pin DC bias current	0V<V_{AGC}<1.3V		-0.7	-6	μA
		Over temperature[1]			-10	

NOTES:

1. "Over Temperature Range" testing is as follows:
   SA is -40 to +85°C
   At the time of this data sheet release, the D package over-temperature data sheet limits are guaranteed via guardbanded room temperature testing only.

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC1} = V_{CC2} = +5.0V, V_{AGC} = 1.0V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
BW	-3dB bandwidth		600	850		MHz
		Over temperature[1]	500			
GF	Gain flatness	DC - 500MHz		±0.4		dB
		Over temperature[1]		±0.6		
V_{IMAX}	Maximum input voltage swing (single-ended) for linear operation[2]			200		mV_{P-P}
V_{OMAX}	Maximum output voltage swing (single-ended) for linear operation[2]	R_L = 50Ω		400		mV_{P-P}
		R_L = 1kΩ		1.9		V_{P-P}
NF	Noise figure (unmatched configuration)	R_S = 50Ω, f = 50MHz		9.3		dB
V_{IN-EQ}	Equivalent input noise voltage spectral density	f = 100MHz		2.5		nV/√Hz
S12	Reverse isolation	f = 100MHz		-60		dB
$\Delta G/\Delta V_{CC}$	Gain supply sensitivity (single-ended)			0.3		dB/V
$\Delta G/\Delta T$	Gain temperature sensitivity	R_L = 50Ω		0.013		dB/°C
C_{IN}	Input capacitance (single-ended)			2		pF
BW_{AGC}	-3dB bandwidth of gain control function			20		MHz
P_{O-1dB}	1dB gain compression point at output	f = 100MHz		-3		dBm
P_{I-1dB}	1dB gain compression point at input	f = 100MHz, V_{AGC} =0.1V		-10		dBm
$IP3_{OUT}$	Third-order intercept point at output	f = 100MHz, V_{AGC} >0.5V		+13		dBm
$IP3_{IN}$	Third-order intercept point at input	f = 100MHz, V_{AGC} <0.5V		+5		dBm
ΔG_{AB}	Gain match output A to output B	f = 100MHz, V_{AGC} = 1V		0.1		dB

NOTE:

1. "Over Temperature Range" testing is as follows:
   SA is -40 to +85°C
   At the time of this data sheet release, the D package over-temperature data sheet limits are guaranteed via guardbanded room temperature testing only.
2. With R_L > 1kΩ, overload occurs at input for single-ended gain < 13dB and at output for single-ended gain > 13dB. With R_L = 50Ω, overload occurs at input for single-ended gain < 6dB and at output for single-ended gain > 6dB.

SA5209 APPLICATIONS

The SA5209 is a wideband variable gain amplifier (VGA) circuit which finds many applications in the RF, IF and video signal processing areas. This application note describes the operation of the circuit and several applications of the VGA. The simplified equivalent schematic of the VGA is shown in Figure 2. Transistors Q1-Q6 form the wideband Gilbert multiplier input stage which is biased by current source I1. The top differential pairs are biased from a buffered and level-shifted signal derived from the V_{AGC} input and the RF input appears at the lower differential pair. The circuit topology and layout offer low input noise and wide bandwidth. The second stage is a differential transimpedance stage with current feedback which maintains the wide bandwidth of the input stage. The output stage is a pair of emitter followers with 50Ω output impedance. There is also an on-chip bandgap reference with buffered output at 1.3V, which can be used to derive the gain control voltage.

Both the inputs and outputs should be capacitor coupled or DC isolated from the signal sources and loads. Furthermore, the two inputs should be DC isolated from each other and the two outputs should likewise be DC isolated from each other. The SA5209 was designed to provide optimum performance from a 5V power source. However, there is some range around this value (4.5 - 7V) that can be used.

The input impedance is about 1kΩ. The main advantage to a differential input configuration is to provide the balun function. Otherwise, there is an advantage to common mode rejection, a specification that is not normally important to RF designs. The source impedance can be chosen for two different performance characteristics: Gain, or noise performance. Gain optimization will be realized if the input impedance is matched to about 1kΩ. A 4:1 balun will provide such a broadband match from a 50Ω source. Noise performance will be optimized if the input impedance is matched to about 200Ω. A 2:1 balun will provide such a broadband match from a 50Ω source. The minimum noise figure can then be expected to be about 7dB. Maximum gain will be about 23dB for a single-ended output. If the differential output is used and properly matched, nearly 30dB can be realized. With gain optimization, the noise figure will degrade to about 8dB. With no matching unit at the input, a 9dB noise figure can be expected from a 50Ω source. If the source is terminated, the noise figure will increase to about 15dB. All these noise figures will occur at maximum gain.

The SA5209 has an excellent noise figure vs gain relationship. With any VGA circuit, the noise performance will degrade with decreasing gain. The 5209 has about a 1.2dB noise figure degradation for each 2dB gain reduction. With the input matched for optimum gain, the 8dB noise figure at 23dB gain will degrade to about a 20dB noise figure at 0dB gain.

The SA5209 also displays excellent linearity between voltage gain and control voltage. Indeed, the relationship is of sufficient linearity that high fidelity AM modulation is possible using the SA5209. A maximum control voltage frequency of about 20MHz permits video baseband sources for AM.

A stabilized bandgap reference voltage is made available on the SA5209 (Pin 7). For fixed gain applications this voltage can be resistor divided, and then fed to the gain control terminal (Pin 8). Using the bandgap voltage reference for gain control produces very stable gain characteristics over wide temperature ranges. The gain setting resistors are not part of the RF signal path, and thus stray capacitance here is not important.

The wide bandwidth and excellent gain control linearity make the SA5209 VGA ideally suited for the automatic gain control (AGC) function in RF and IF processing in cellular radio base stations, Direct Broadcast Satellite (DBS) decoders, cable TV systems, fiber optic receivers for wideband data and video, and other radio communication applications. A typical AGC configuration using the SA5209 is shown in Figure 3. Three SA5209s are cascaded with appropriate AC coupling capacitors. The output of the final stage drives the full-wave rectifier composed of two UHF Schottky diodes BAT17 as shown. The diodes are biased by R1 and R2 to V_{CC} such that a quiescent current of about 2mA in each leg is achieved. An SA5230 low voltage op amp is used as an integrator which drives the V_{AGC} pin on all three SA5209s. R3 and C3 filter the high frequency ripple from the full-wave rectified signal. A voltage divider is used to generate the reference for the non-inverting input of the op amp at about 1.7V. Keeping D3 the same type as D1 and D2 will provide a first order compensation for the change in Schottky voltage over the operating temperature range and improve the AGC performance. R6 is a variable resistor for adjustments to the op amp reference voltage. In low cost and large volume applications this could be replaced with a fixed resistor, which would result in a slight loss of the AGC dynamic range. Cascading three SA5209s will give a dynamic range in excess of 60dB.

The SA5209 is a very user-friendly part and will not oscillate in most applications. However, in an application such as with gains in excess of 60dB and bandwidth beyond 100MHz, good PC board layout with proper supply decoupling is strongly recommended.

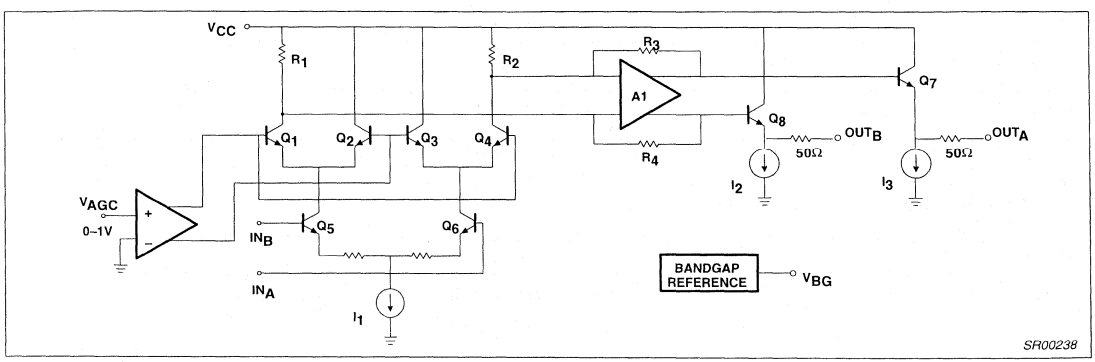


Figure 2. Equivalent Schematic of the VGA

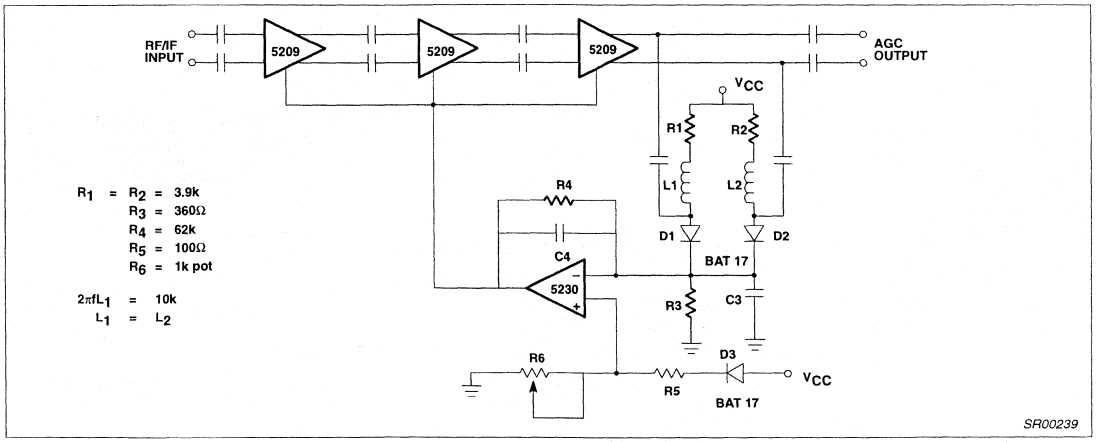


Figure 3. AGC Configuration Using Cascaded SA5209s

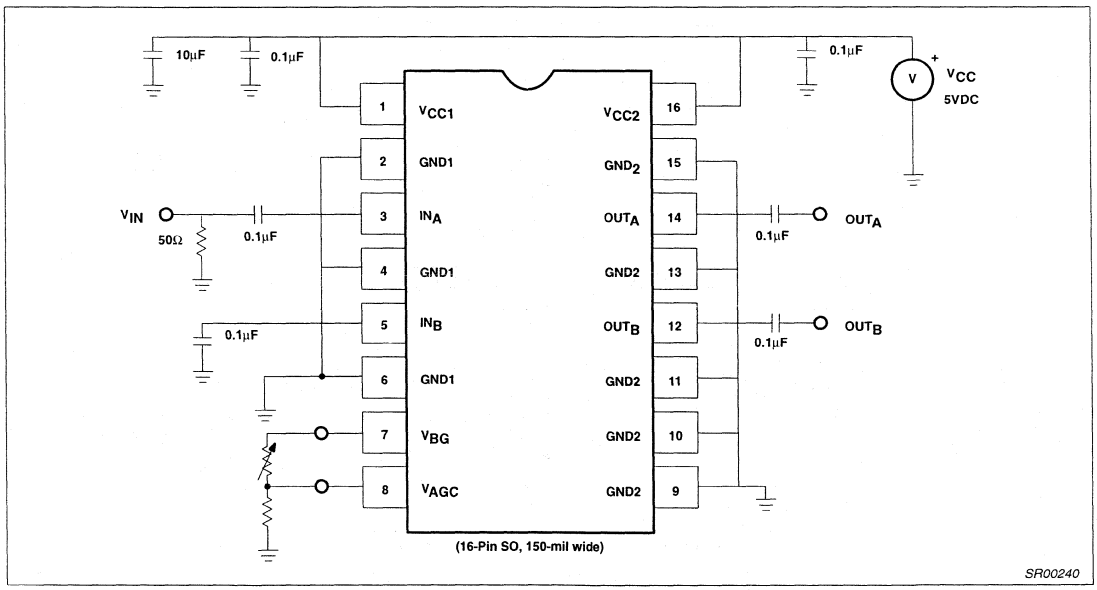


Figure 4. VGA AC Evaluation Board

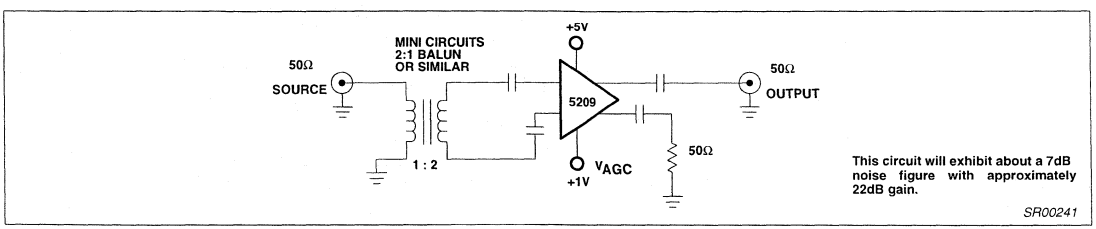


Figure 5. Broadband Noise Optimization

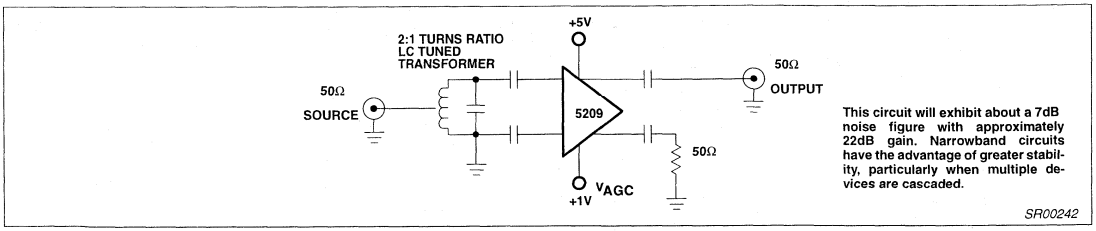


Figure 6. Narrowband Noise Optimization

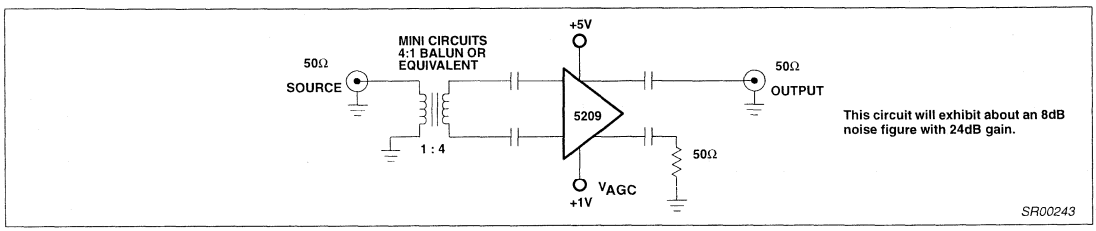


Figure 7. Broadband Gain Optimization

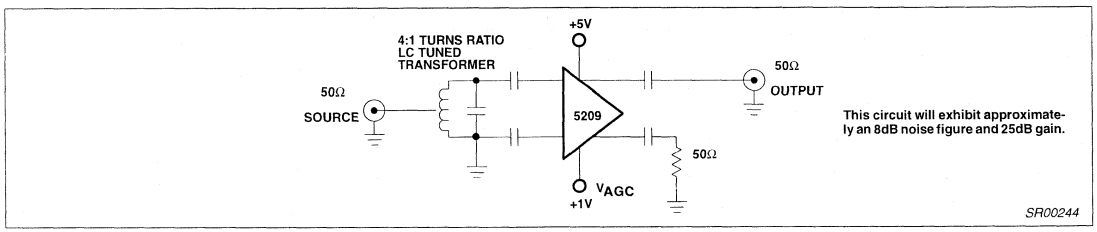


Figure 8. Narrowband Gain Optimization

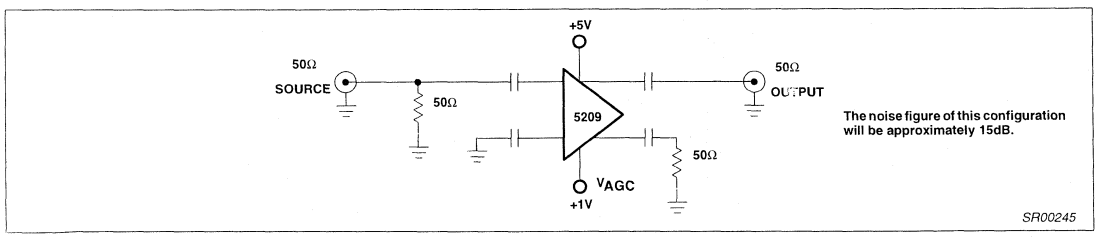


Figure 9. Simple Amplifier Configuration

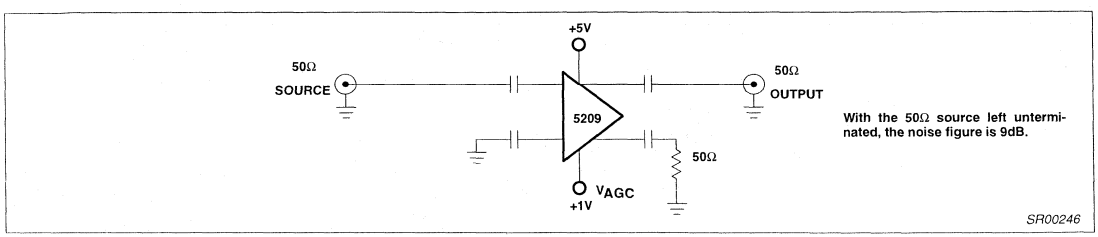


Figure 10. Unterminated Configuration

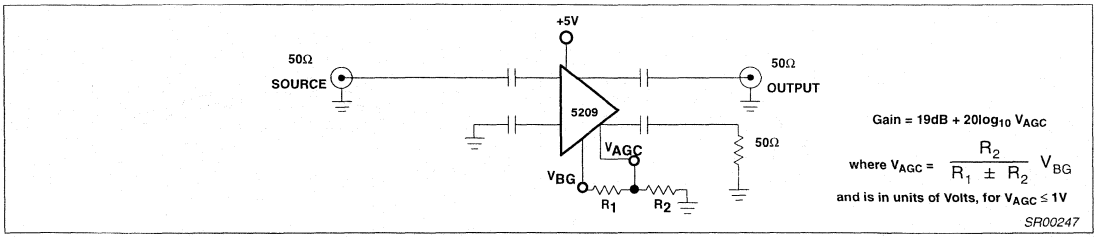


Figure 11. User-Programmable Fixed Gain Block

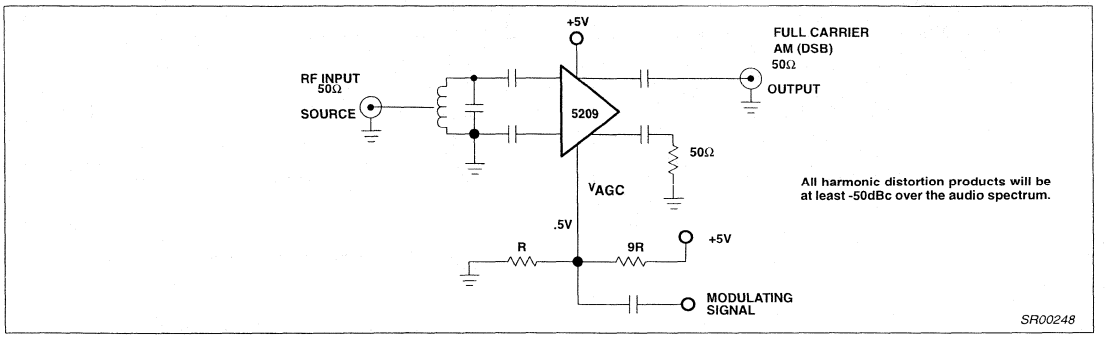


Figure 12. AM Modulator

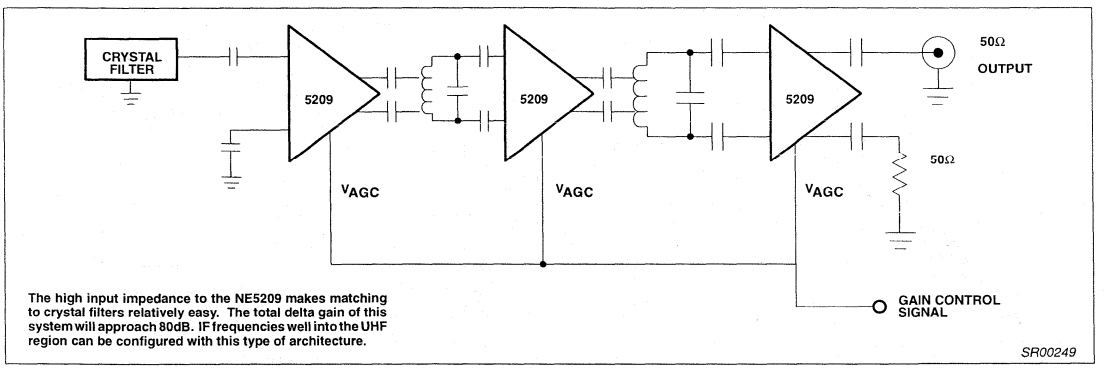


Figure 13. Receiver AGC IF Gain

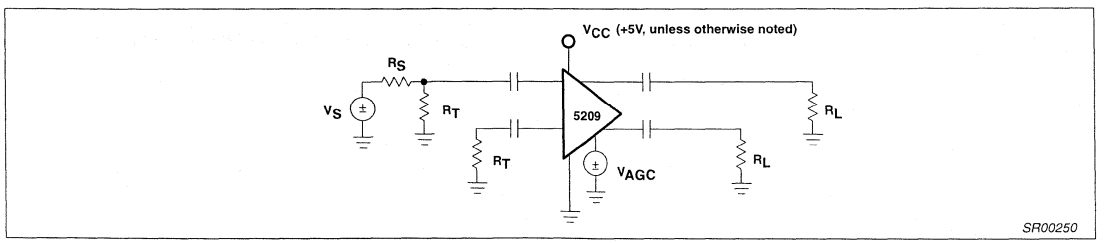


Figure 14. Test Set-up 1 (Used for all Graphs)

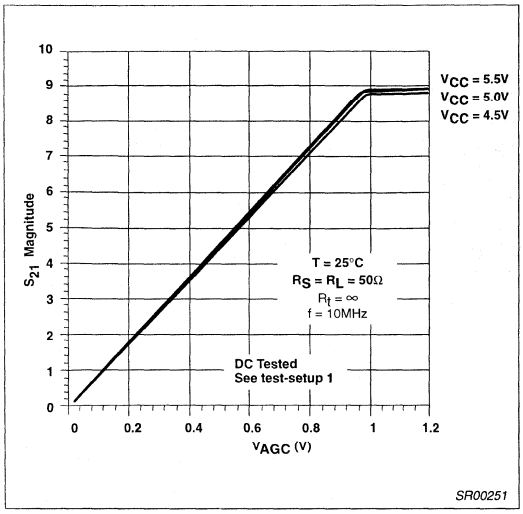


Figure 15. Gain vs V_{AGC} and V_{CC}

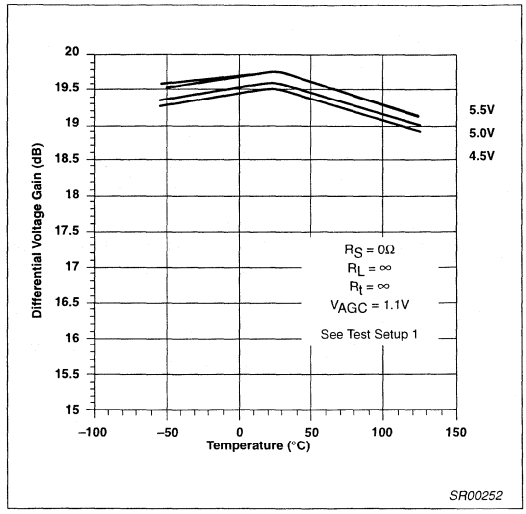


Figure 17. Voltage Gain vs Temperature and V_{CC}

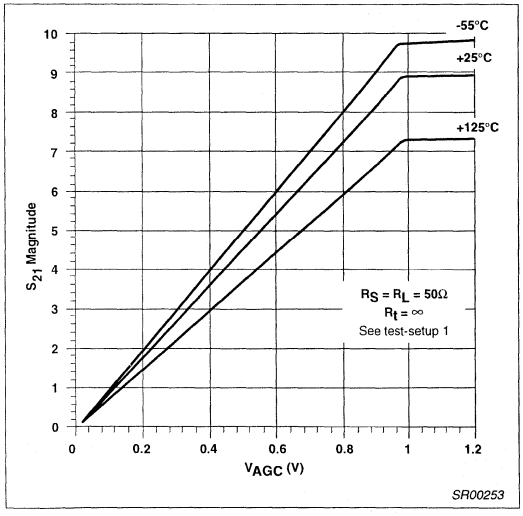


Figure 16. Insertion Gain vs V_{AGC} and Temperature

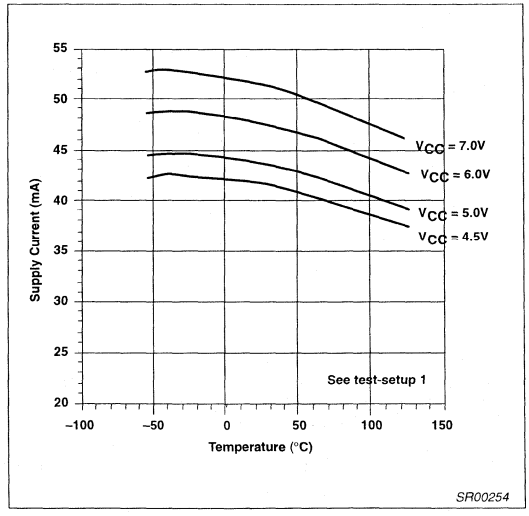


Figure 18. Supply Current vs Temperature and V_{CC}

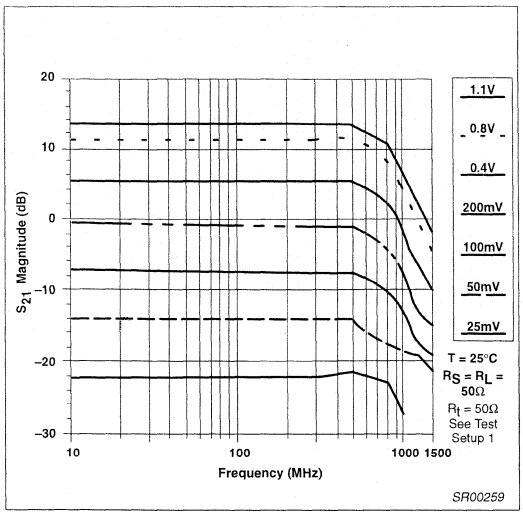


Figure 23. Insertion Gain vs Frequency and V_{AGC}

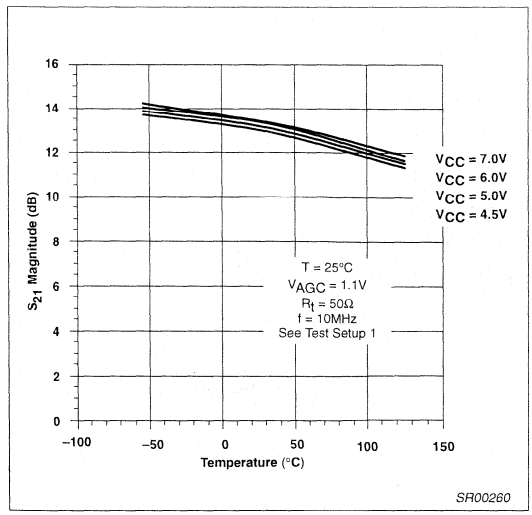


Figure 25. Insertion Gain vs Temperature and V_{CC}

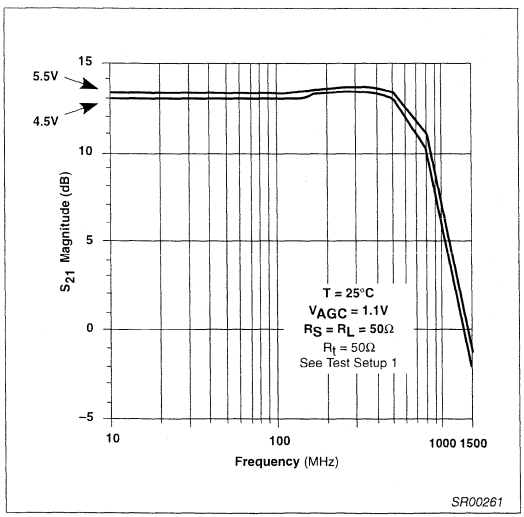


Figure 24. Insertion Gain vs Frequency and V_{CC}

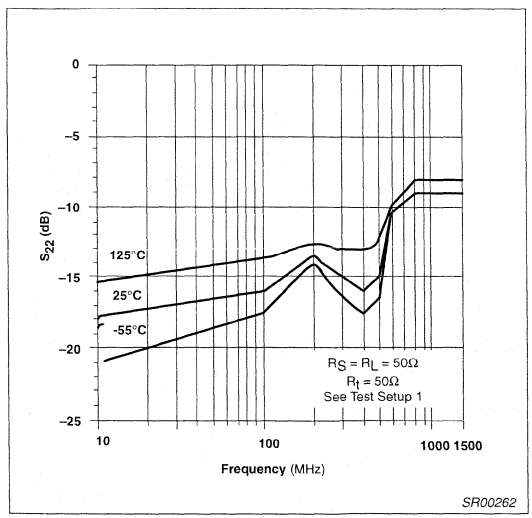


Figure 26. Output Return Loss vs Frequency

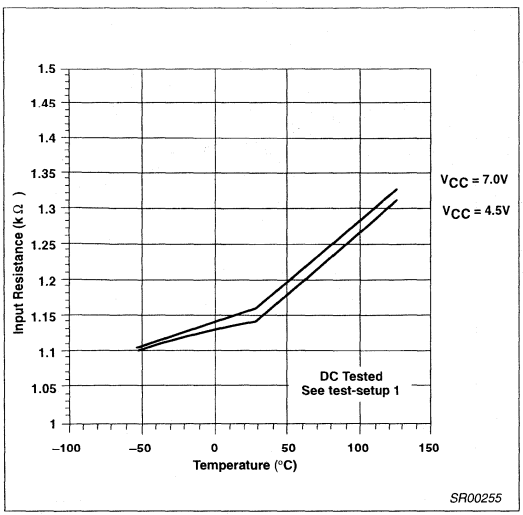


Figure 19. Input Resistance vs Temperature

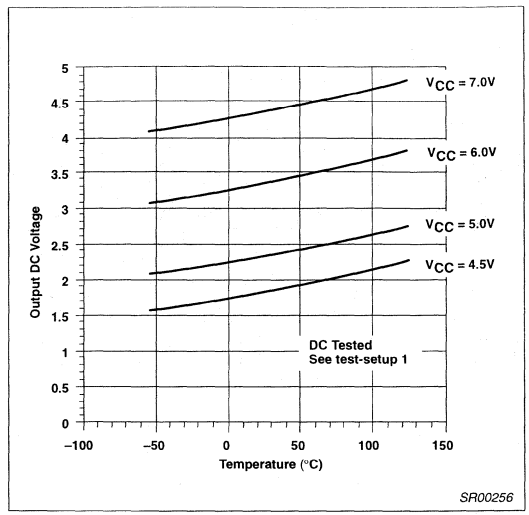


Figure 21. Output Bias Voltage vs Temperature and V_{CC}

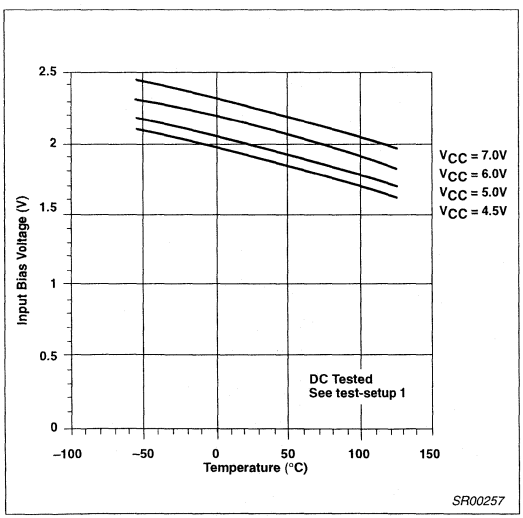


Figure 20. Input Bias Voltage vs Temperature

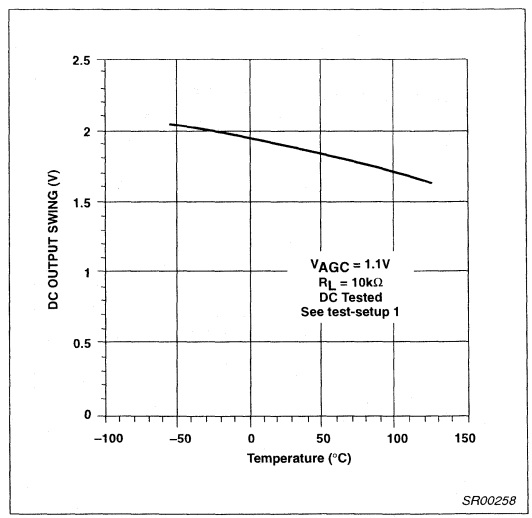


Figure 22. DC Output Swing vs Temperature

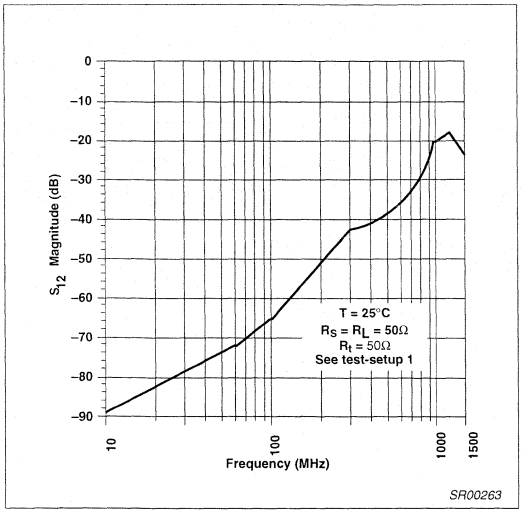


Figure 27. Reverse Isolation vs Frequency

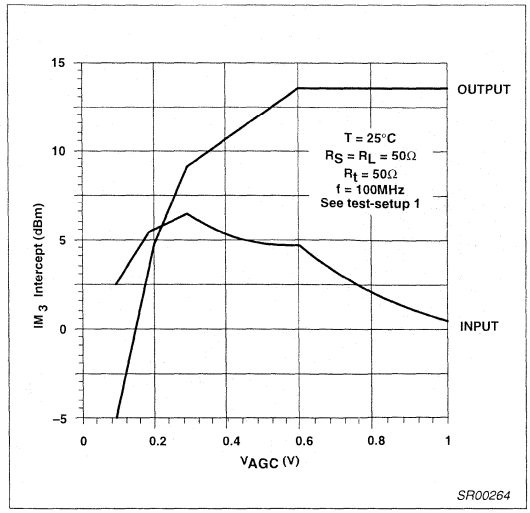


Figure 29. Third-Order Intermodulation Intercept vs V_{AGC}

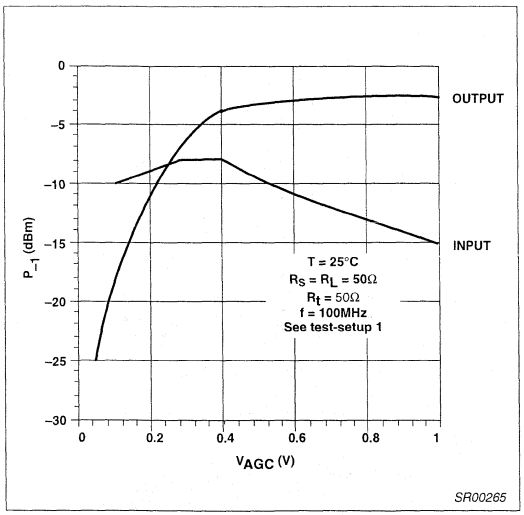


Figure 28. 1dB Gain Compression vs V_{AGC}

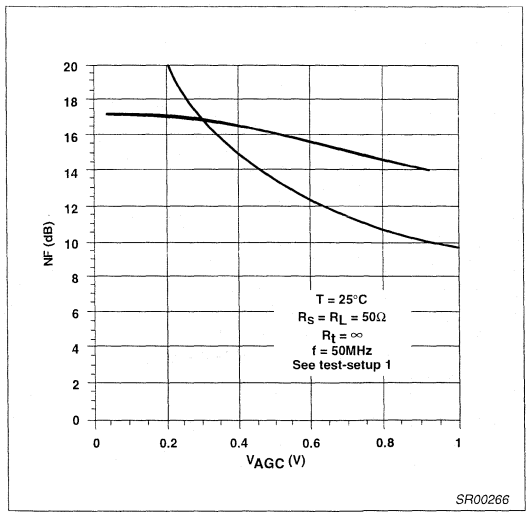


Figure 30. Noise Figure vs V_{AGC}

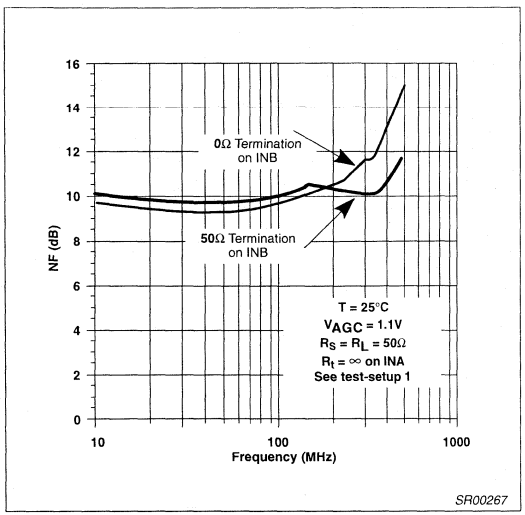


Figure 31. Noise Figure vs Frequency

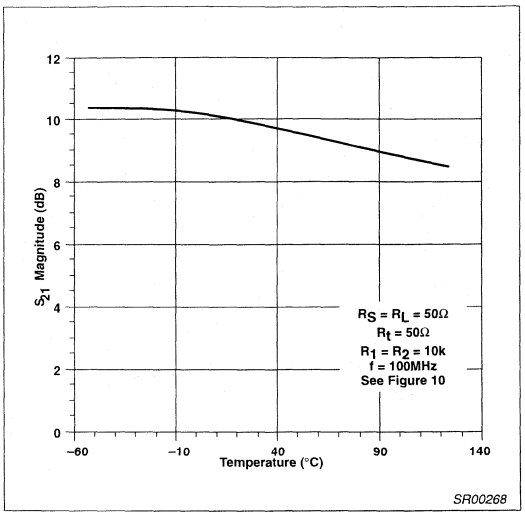


Figure 33. Fixed Gain vs Temperature

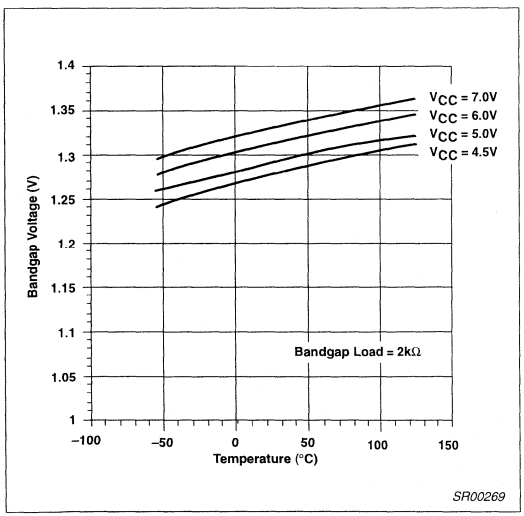


Figure 32. Bandgap Voltage vs Temperature and V_{CC}

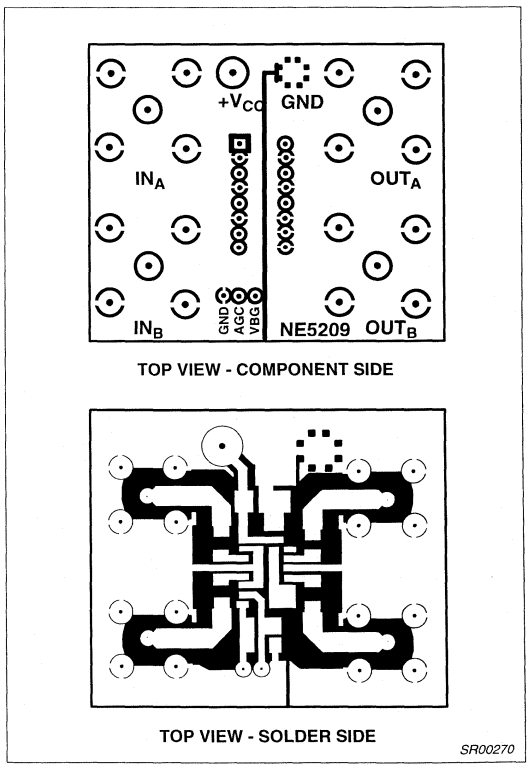
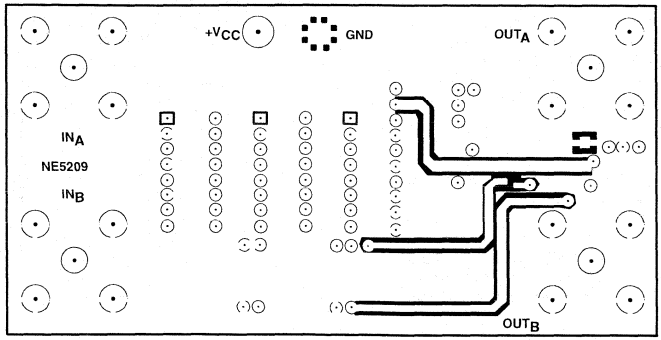
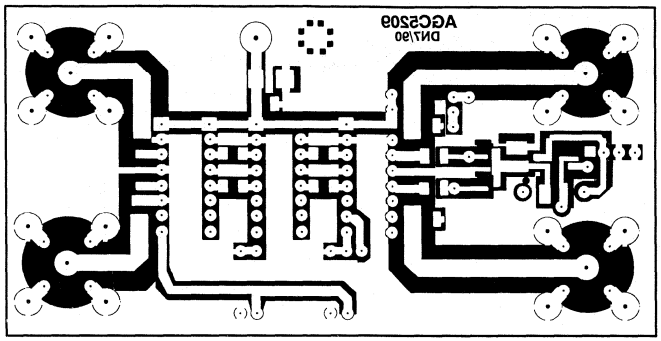


Figure 34. VGA AC Evaluation Board Layout



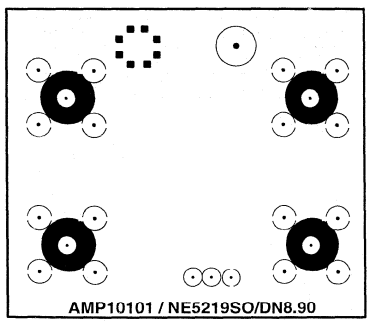
TOP VIEW - COMPONENT SIDE



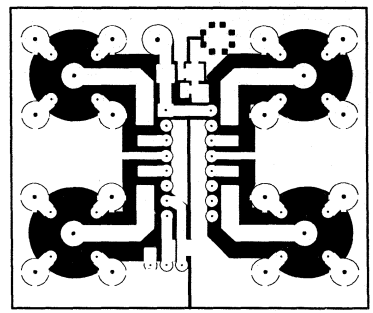
TOP VIEW - SOLDER SIDE

SR00271

Figure 35. AGC Configuration Using Cascaded SA5209s - Layout



TOP VIEW - COMPONENT SIDE



TOP VIEW - SOLDER SIDE

SR00272

Figure 36. VGA AC Evaluation Board Layout (DIP Package)

Wideband variable gain amplifier SA5219

DESCRIPTION

The SA5219 represents a breakthrough in monolithic amplifier design featuring several innovations. This unique design has combined the advantages of a high speed bipolar process with the proven Gilbert architecture.

The SA5219 is a linear broadband RF amplifier whose gain is controlled by a single DC voltage. The amplifier runs off a single 5 volt supply and consumes only 40mA. The amplifier has high impedance (1kΩ) differential inputs. The output is 50Ω differential. Therefore, the 5219 can simultaneously perform AGC, impedance transformation, and the balun functions.

The dynamic range is excellent over a wide range of gain setting. Furthermore, the noise performance degrades at a comparatively slow rate as the gain is reduced. This is an important feature when building linear AGC systems.

PIN CONFIGURATION

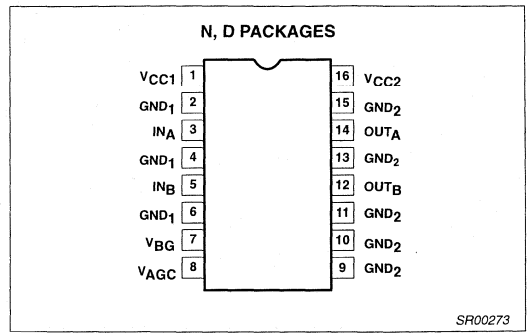


Figure 1. Pin Configuration

FEATURES

- 700MHz bandwidth
- High impedance differential input
- 50Ω differential output
- Single 5V power supply
- 0 - 1V gain control pin
- >60dB gain control range at 200MHz
- 26dB maximum gain differential
- Exceptional $V_{CONTROL}$ / V_{GAIN} linearity
- 7dB noise figure minimum
- Full ESD protection
- Easily cascadable

APPLICATIONS

- Linear AGC systems
- Very linear AM modulator
- RF balun
- Cable TV multi-purpose amplifier
- Fiber optic AGC
- RADAR
- User programmable fixed gain block
- Video
- Satellite receivers
- Cellular communications

ORDERING INFORMATION

Description	Temperature Range	Order Code	DWG #
16-Pin Plastic Small Outline (SO) package	-40 to +85°C	SA5219D	SOT109-1
16-Pin Plastic Dual In-Line package (DIP)	-40 to +85°C	SA5219N	SOT28-4

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	-0.5 to +8.0	V
P_D	Power dissipation, T_A = 25°C (still air)[1] 16-Pin Plastic DIP 16-Pin Plastic SO	 1450 1100	 mW mW
T_{JMAX}	Maximum operating junction temperature	150	°C
T_{STG}	Storage temperature range	-65 to +150	°C

NOTES:
1. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance, θ_{JA}:
   16-Pin DIP: θ_{JA} = 85°C/W
   16-Pin SO: θ_{JA} = 110°C/W

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	V_{CC1} = V_{CC2} = 4.5 to 7.0V	V
T_A	Operating ambient temperature range SA Grade	-40 to +85	°C
T_J	Operating junction temperature range SA Grade	-40 to +105	°C

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC1} = V_{CC2} = +5V, V_{AGC} = 1.0V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
I_{CC}	Supply current	DC tested	36	43	50	mA
A_V	Voltage gain (single-ended in/single-ended out)	DC tested, R_L = 10kΩ	16	19	22	dB
A_V	Voltage gain (single-ended in/differential out)	DC tested, R_L = 10kΩ	22	25	28	dB
R_{IN}	Input resistance (single-ended)	DC tested at ±50μA	0.8	1.2	1.6	kΩ
R_{OUT}	Output resistance (single-ended)	DC tested at ±1mA	35	60	80	Ω
V_{OS}	Output offset voltage (output referred)			±20	±150	mV
V_{IN}	DC level on inputs		1.6	2.0	2.4	V
V_{OUT}	DC level on outputs		1.9	2.4	2.9	V
PSRR	Output offset supply rejection ratio		18	45		dB
V_{BG}	Bandgap reference voltage	4.5V<V_{CC}<7V R_{BG} = 10kΩ	1.2	1.32	1.45	V
R_{BG}	Bandgap loading		2	10		kΩ
V_{AGC}	AGC DC control voltage range			0-1.3		V
I_{BAGC}	AGC pin DC bias current	0V<V_{AGC}<1.3V		-0.7	-6	μA

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC1} = V_{CC2} = +5.0V, V_{AGC} = 1.0V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
BW	-3dB bandwidth			700		MHz
GF	Gain flatness	DC - 500MHz		±0.4		dB
V_{IMAX}	Maximum input voltage swing (single-ended) for linear operation[1]			200		mV_{P-P}
V_{OMAX}	Maximum output voltage swing (single-ended) for linear operation[1]	R_L = 50Ω		400		mV_{P-P}
		R_L = 1kΩ		1.9		V_{P-P}
NF	Noise figure (unmatched configuration)	R_S = 50Ω, f = 50MHz		9.3		dB
V_{IN-EQ}	Equivalent input noise voltage spectral density	f = 100MHz		2.5		$nV/\sqrt{Hz}$
S12	Reverse isolation	f = 100MHz		-60		dB
$\Delta G/\Delta V_{CC}$	Gain supply sensitivity (single-ended)			0.3		dB/V
$\Delta G/\Delta T$	Gain temperature sensitivity	R_L = 50Ω		0.013		dB/°C
C_{IN}	Input capacitance (single-ended)			2		pF
BW_{AGC}	-3dB bandwidth of gain control function			20		MHz
P_{O-1dB}	1dB gain compression point at output	f = 100MHz		-3		dBm
P_{I-1dB}	1dB gain compression point at input	f = 100MHz, V_{AGC} =0.1V		-10		dBm
$IP3_{OUT}$	Third-order intercept point at output	f = 100MHz, V_{AGC} >0.5V		+13		dBm
$IP3_{IN}$	Third-order intercept point at input	f = 100MHz, V_{AGC} <0.5V		+5		dBm
ΔG_{AB}	Gain match output A to output B	f = 100MHz, V_{AGC} = 1V		0.1		dB

NOTE:

1. With R_L > 1kΩ, overload occurs at input for single-ended gain < 13dB and at output for single-ended gain > 13dB. With R_L = 50Ω, overload occurs at input for single-ended gain < 6dB and at output for single-ended gain > 6dB.

SA5219 APPLICATIONS

The SA5219 is a wideband variable gain amplifier (VGA) circuit which finds many applications in the RF, IF and video signal processing areas. This application note describes the operation of the circuit and several applications of the VGA. The simplified equivalent schematic of the VGA is shown in Figure 2. Transistors Q1-Q6 form the wideband Gilbert multiplier input stage which is biased by current source I1. The top differential pairs are biased from a buffered and level-shifted signal derived from the V_{AGC} input and the RF input appears at the lower differential pair. The circuit topology and layout offer low input noise and wide bandwidth. The second stage is a differential transimpedance stage with current feedback which maintains the wide bandwidth of the input stage. The output stage is a pair of emitter followers with 50Ω output impedance. There is also an on-chip bandgap reference with buffered output at 1.3V, which can be used to derive the gain control voltage.

Both the inputs and outputs should be capacitor coupled or DC isolated from the signal sources and loads. Furthermore, the two inputs should be DC isolated from each other and the two outputs should likewise be DC isolated from each other. The SA5219 was designed to provide optimum performance from a 5V power source. However, there is some range around this value (4.5 - 7V) that can be used.

The input impedance is about 1kΩ. The main advantage to a differential input configuration is to provide the balun function. Otherwise, there is an advantage to common mode rejection, a specification that is not normally important to RF designs. The source impedance can be chosen for two different performance characteristics: Gain, or noise performance. Gain optimization will be realized if the input impedance is matched to about 1kΩ. A 4:1 balun will provide such a broadband match from a 50Ω source. Noise performance will be optimized if the input impedance is matched to about 200Ω. A 2:1 balun will provide such a broadband match from a 50Ω source. The minimum noise figure can then be expected to be about 7dB. Maximum gain will be about 23dB for a single-ended output. If the differential output is used and properly matched, nearly 30dB can be realized. With gain optimization, the noise figure will degrade to about 8dB. With no matching unit at the input, a 9dB noise figure can be expected from a 50Ω source. If the source is terminated, the noise figure will increase to about 15dB. All these noise figures will occur at maximum gain.

The SA5219 has an excellent noise figure vs gain relationship. With any VGA circuit, the noise performance will degrade with decreasing gain. The 5219 has about a 1.2dB noise figure degradation for each 2dB gain reduction. With the input matched for optimum gain, the 8dB noise figure at 23dB gain will degrade to about a 20dB noise figure at 0dB gain.

The SA5219 also displays excellent linearity between voltage gain and control voltage. Indeed, the relationship is of sufficient linearity that high fidelity AM modulation is possible using the SA5219. A

maximum control voltage frequency of about 20MHz permits video baseband sources for AM.

A stabilized bandgap reference voltage is made available on the SA5219 (Pin 7). For fixed gain applications this voltage can be resistor divided, and then fed to the gain control terminal (Pin 8). Using the bandgap voltage reference for gain control produces very stable gain characteristics over wide temperature ranges. The gain setting resistors are not part of the RF signal path, and thus stray capacitance here is not important.

The wide bandwidth and excellent gain control linearity make the SA5219 VGA ideally suited for the automatic gain control (AGC) function in RF and IF processing in cellular radio base stations, Direct Broadcast Satellite (DBS) decoders, cable TV systems, fiber optic receivers for wideband data and video, and other radio communication applications. A typical AGC configuration using the SA5219 is shown in Figure 3. Three SA5219s are cascaded with appropriate AC coupling capacitors. The output of the final stage drives the full-wave rectifier composed of two UHF Schottky diodes BAT17 as shown. The diodes are biased by R1 and R2 to V_{CC} such that a quiescent current of about 2mA in each leg is achieved. An SA5230 low voltage op amp is used as an integrator which drives the V_{AGC} pin on all three SA5219s. R3 and C3 filter the high frequency ripple from the full-wave rectified signal. A voltage divider is used to generate the reference for the non-inverting input of the op amp at about 1.7V. Keeping D3 the same type as D1 and D2 will provide a first order compensation for the change in Schottky voltage over the operating temperature range and improve the AGC performance. R6 is a variable resistor for adjustments to the op amp reference voltage. In low cost and large volume applications this could be replaced with a fixed resistor, which would result in a slight loss of the AGC dynamic range. Cascading three SA5219s will give a dynamic range in excess of 60dB.

The SA5219 is a very user-friendly part and will not oscillate in most applications. However, in an application such as with gains in excess of 60dB and bandwidth beyond 100MHz, good PC board layout with proper supply decoupling is strongly recommended.

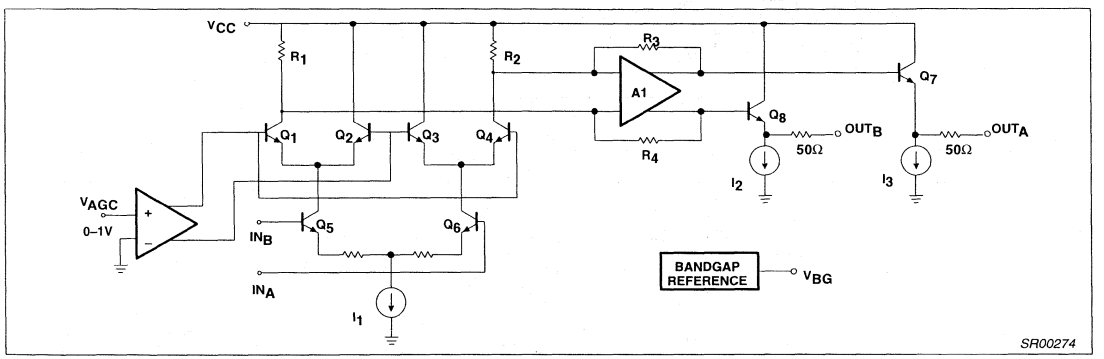


Figure 2. Equivalent Schematic of VGA

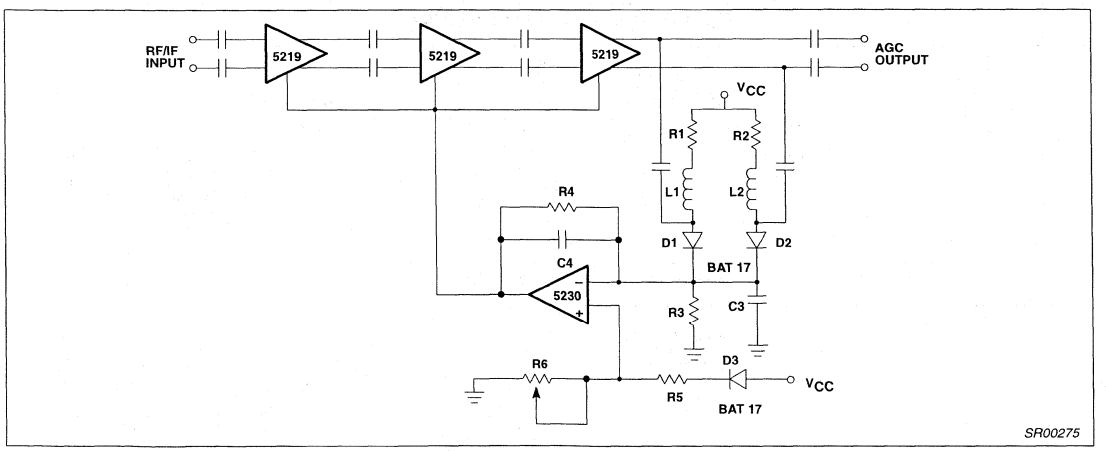


Figure 3. AGC Configuration Using Cascaded SA5219s

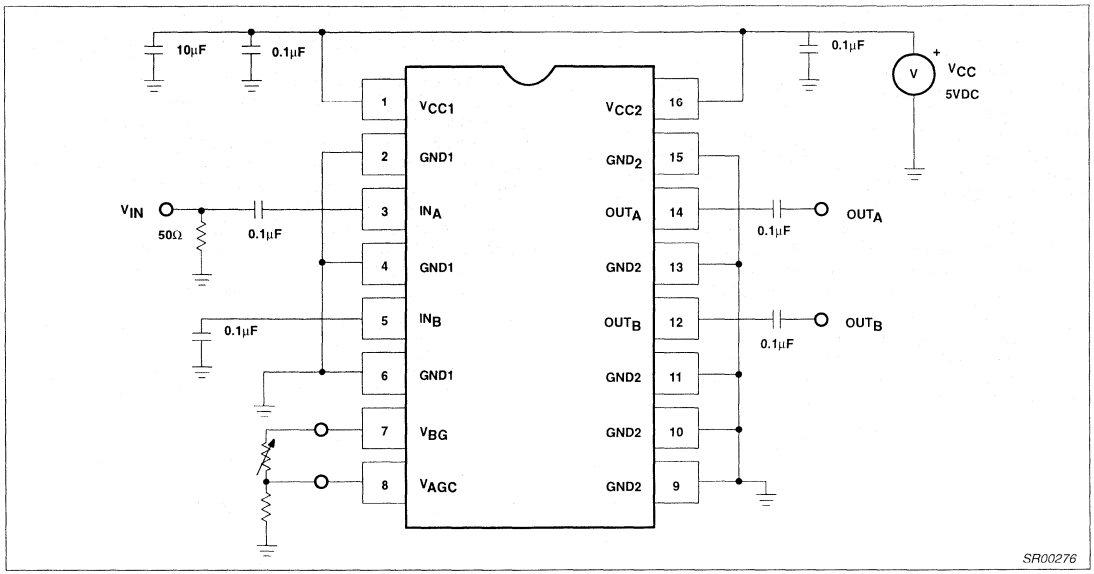


Figure 4. VGA AC Evaluation Board

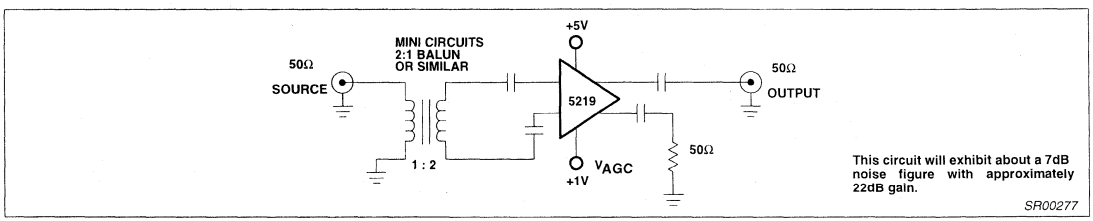


Figure 5. Broadband Noise Optimization

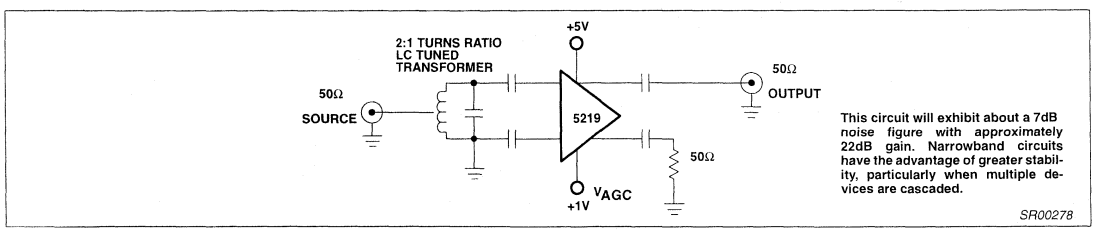


Figure 6. Narrowband Noise Optimization

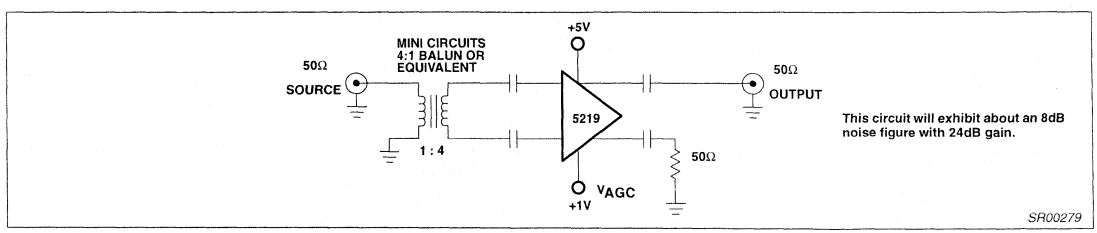


Figure 7. Broadband Gain Optimization

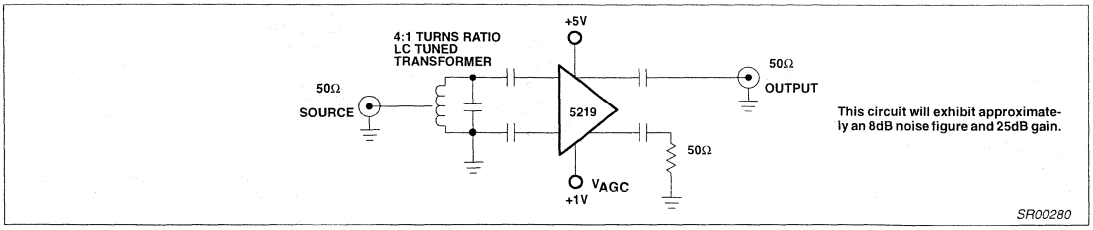


Figure 8. Narrowband Gain Optimization

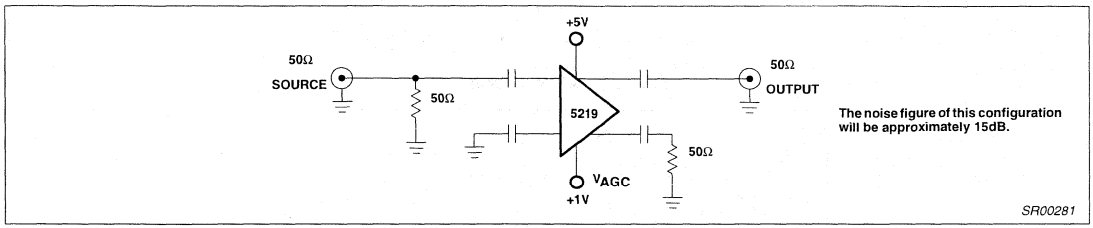


Figure 9. Simple Amplifier Configuration

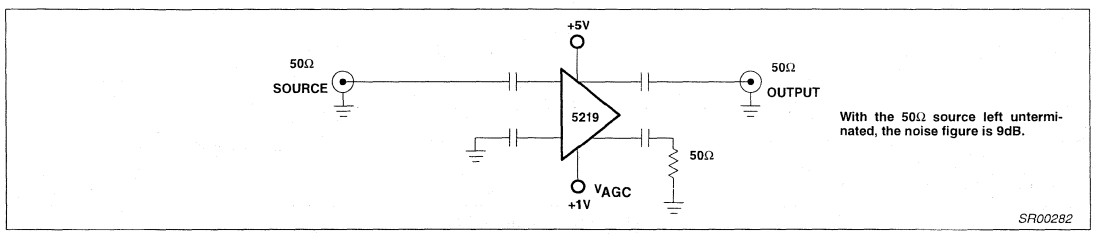


Figure 10. Unterminated Configuration

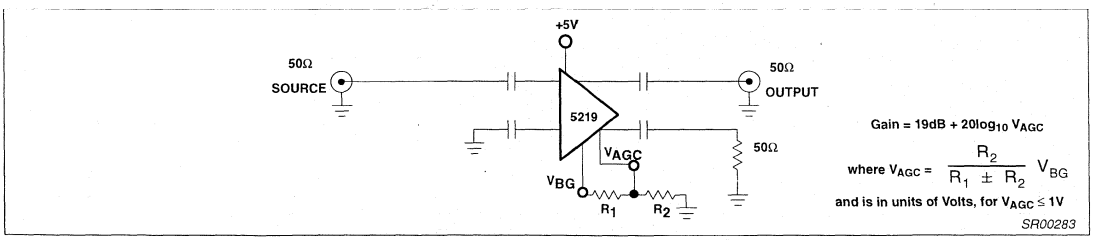


Figure 11. User-Programmable Fixed Gain Block

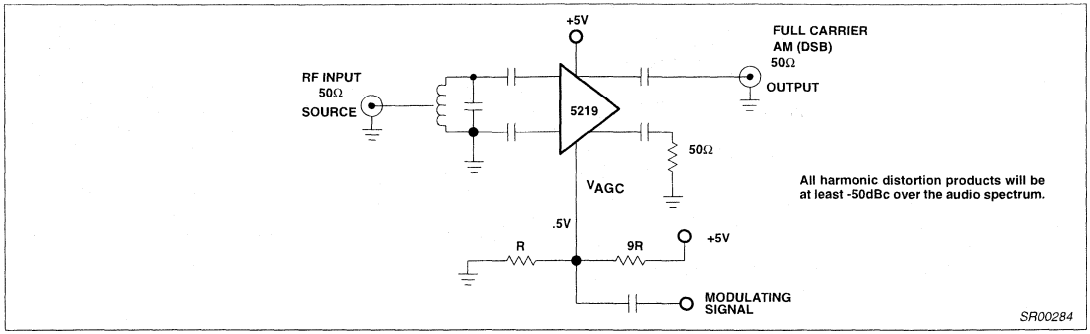


Figure 12. AM Modulator

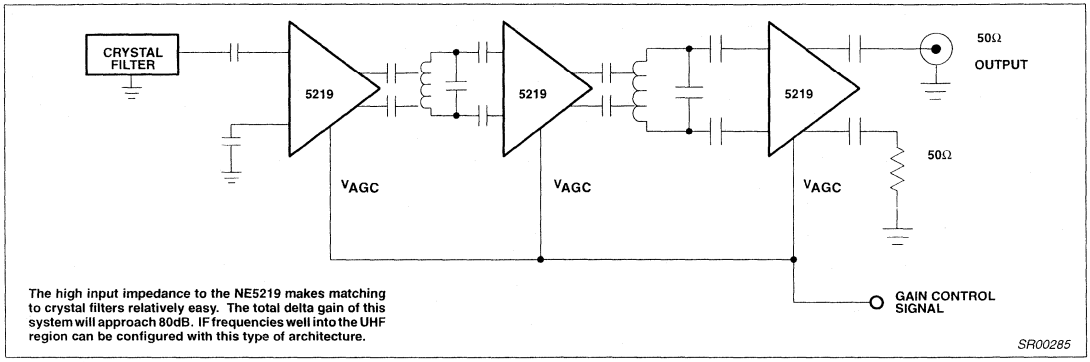


Figure 13. Receiver AGC IF Gain

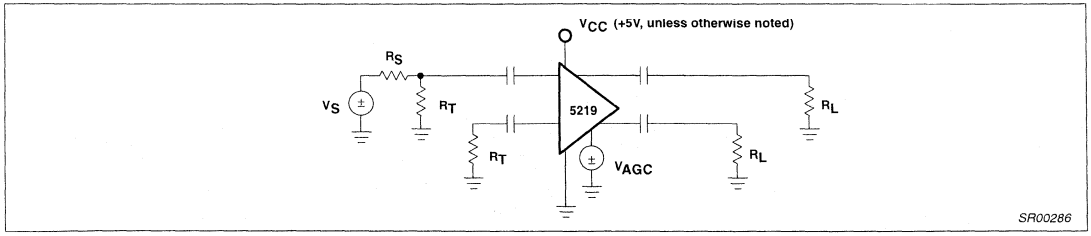


Figure 14. Test Set-up 1 (Used for all Graphs)

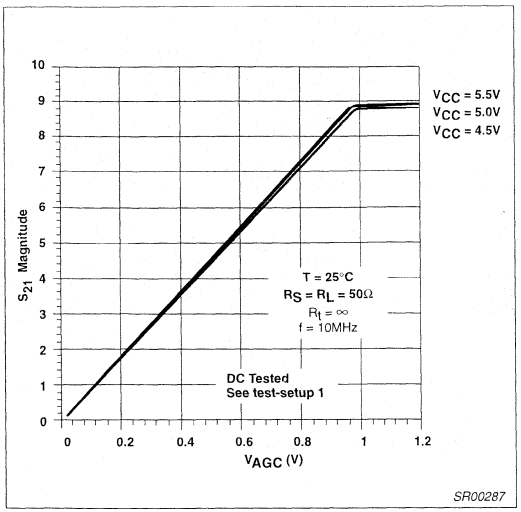


Figure 15. Gain vs V_{AGC} and V_{CC}

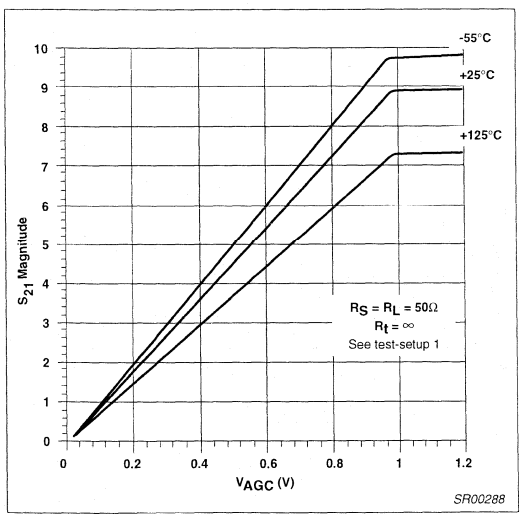


Figure 16. Insertion Gain vs V_{AGC} and Temperature

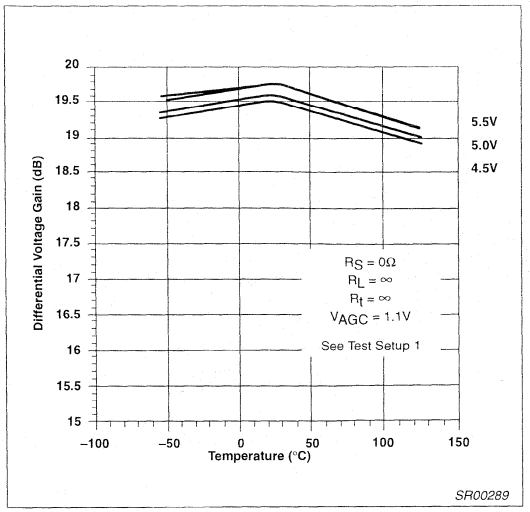


Figure 17. Voltage Gain vs Temperature and V_{CC}

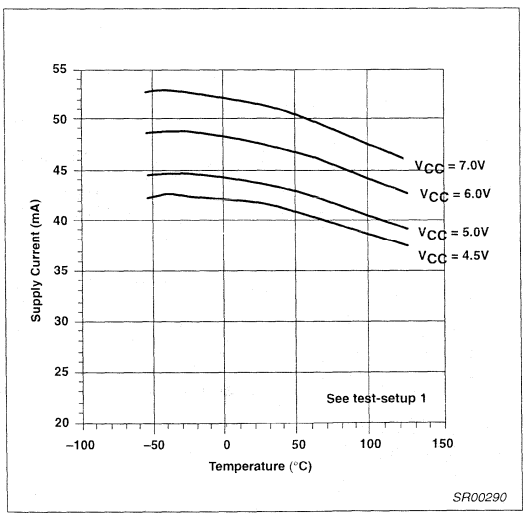


Figure 18. Supply Current vs Temperature and V_{CC}

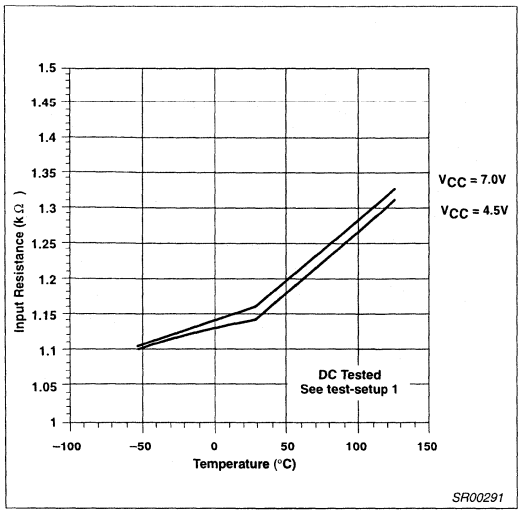


Figure 19. Input Resistance vs Temperature

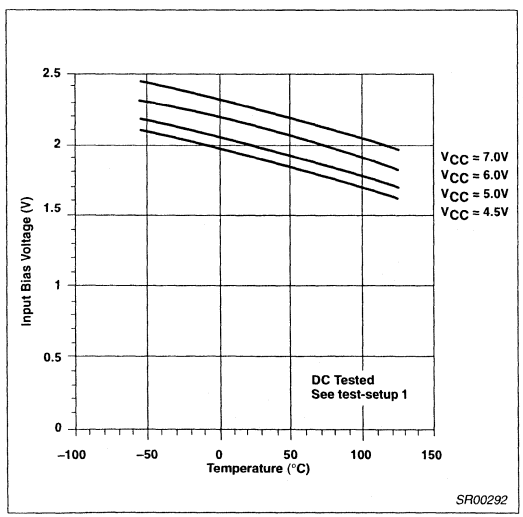


Figure 20. Input Bias Voltage vs Temperature

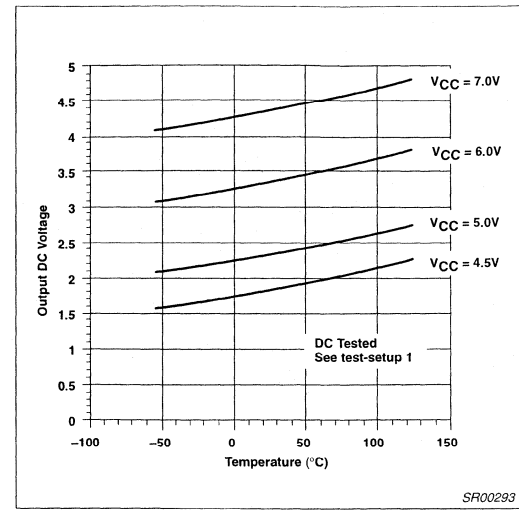


Figure 21. Output Bias Voltage vs Temperature and V_{CC}

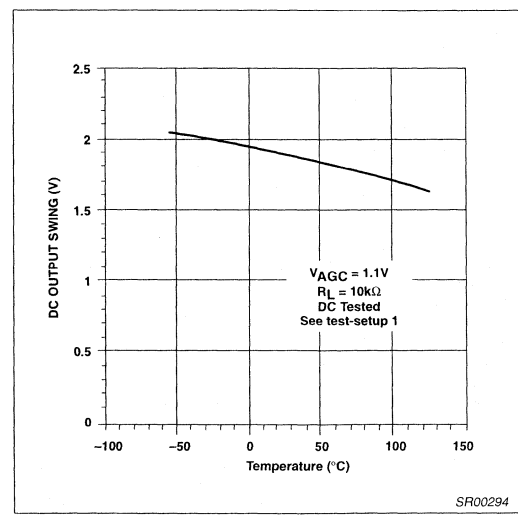


Figure 22. DC Output Swing vs Temperature

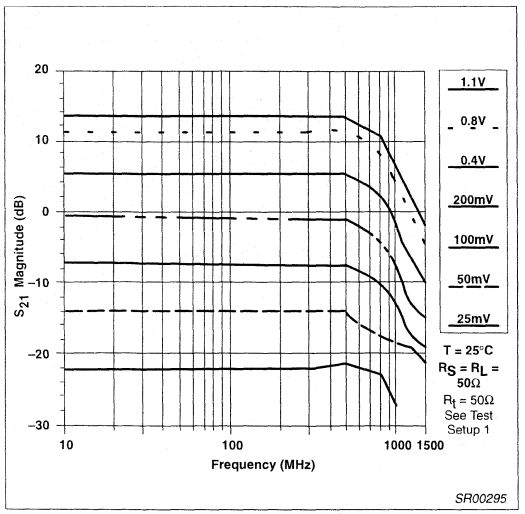


Figure 23. Insertion Gain vs Frequency and V_{AGC}

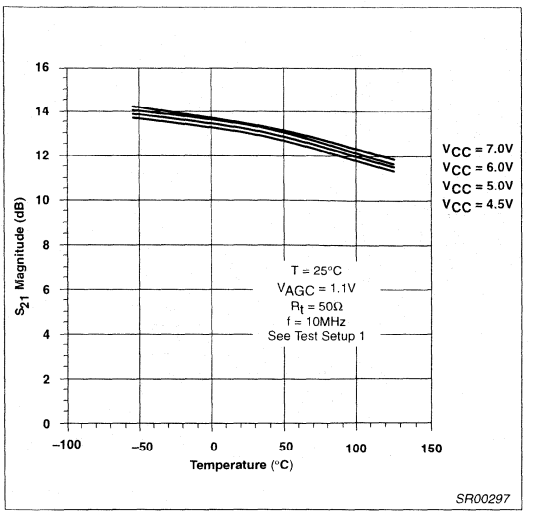


Figure 25. Insertion Gain vs Temperature and V_{CC}

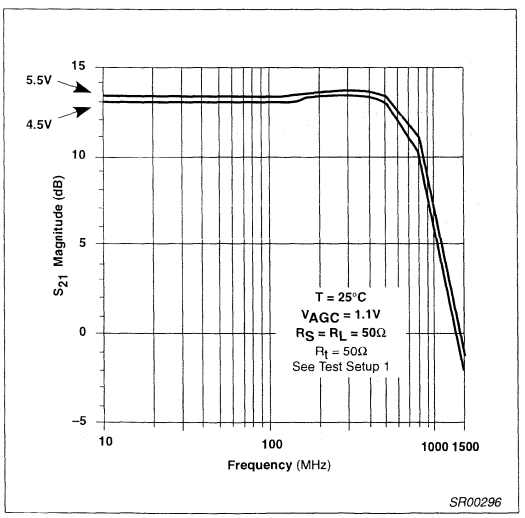


Figure 24. Insertion Gain vs Frequency and V_{CC}

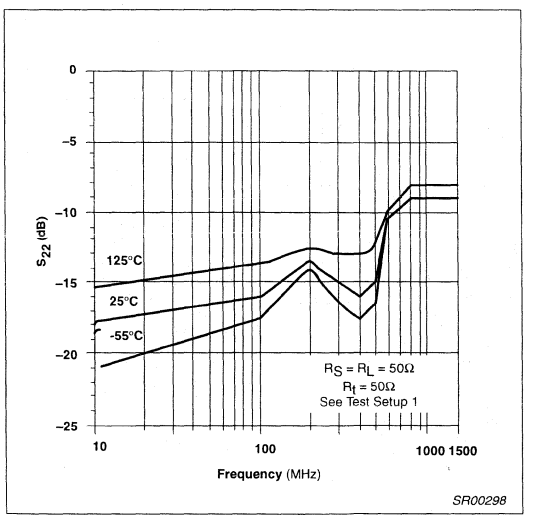


Figure 26. Output Return Loss vs Frequency

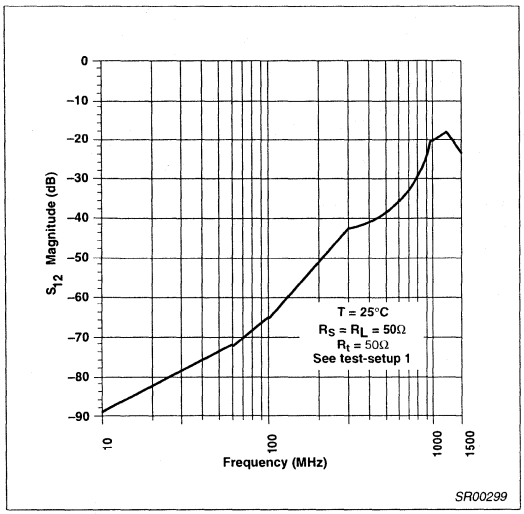


Figure 27. Reverse Isolation vs Frequency

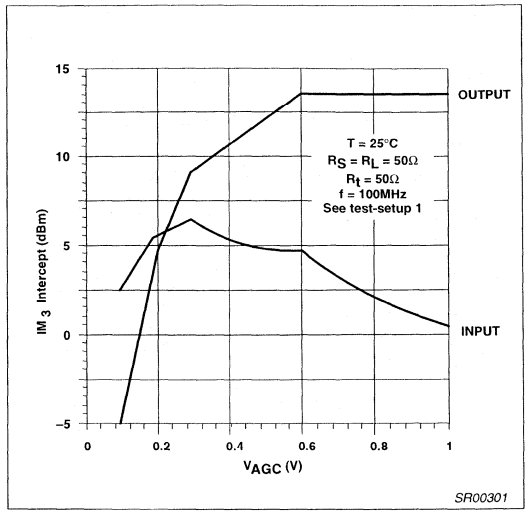


Figure 29. Third-Order Intermodulation Intercept vs V_{AGC}

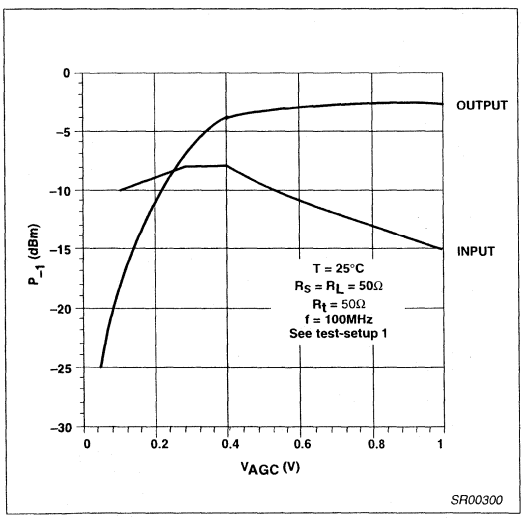


Figure 28. 1dB Gain Compression vs V_{AGC}

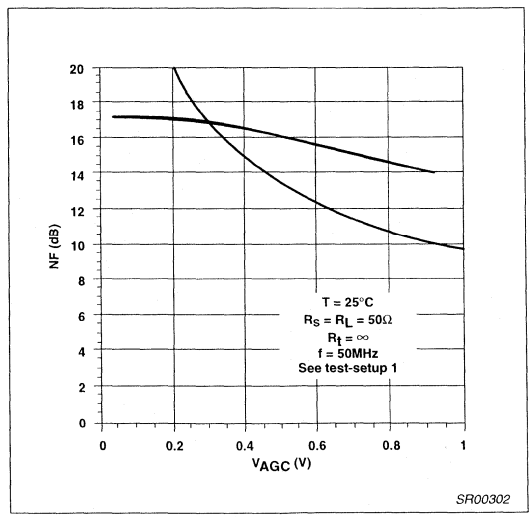


Figure 30. Noise Figure vs V_{AGC}

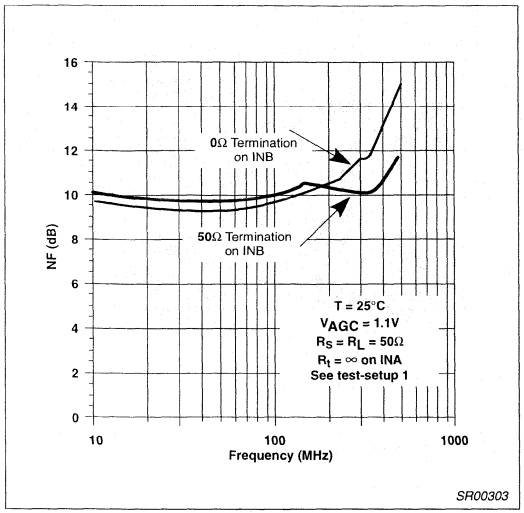


Figure 31. Noise Figure vs Frequency

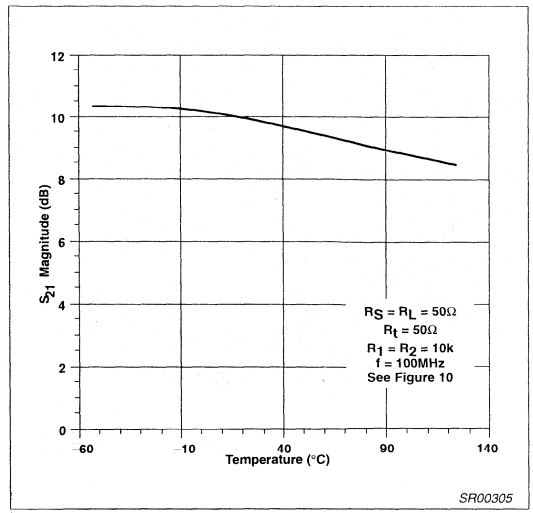


Figure 33. Fixed Gain vs Temperature

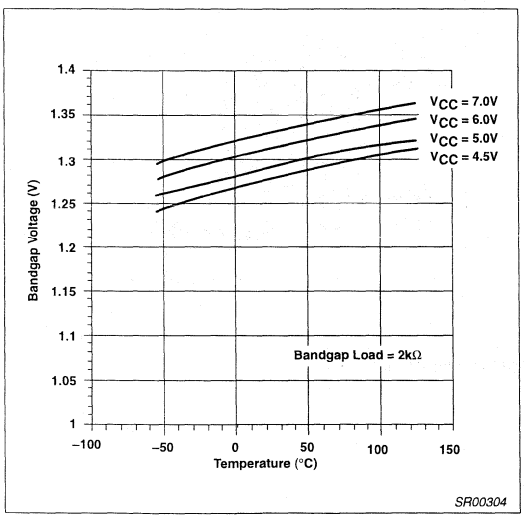
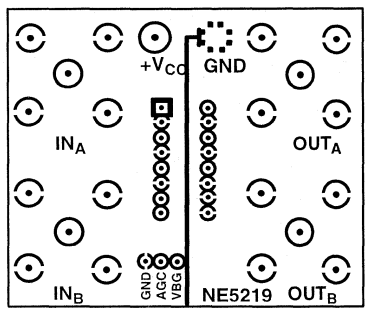
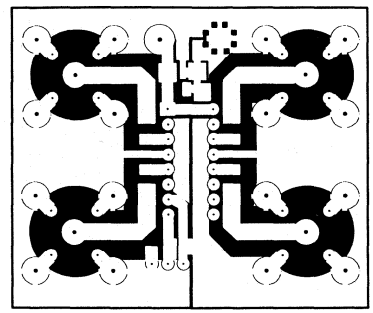


Figure 32. Bandgap Voltage vs Temperature and V_{CC}



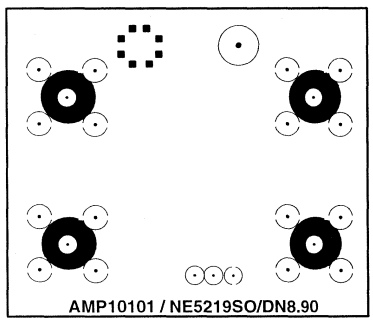
TOP VIEW - COMPONENT SIDE



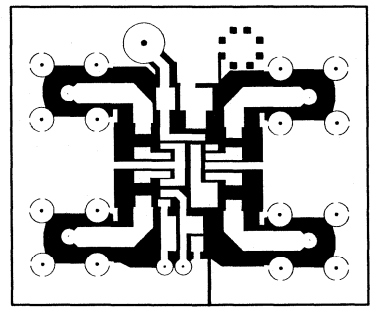
TOP VIEW - SOLDER SIDE

SR00306

Figure 34. VGA AC Evaluation Board Layout (DIP Package)



BOTTOM VIEW - D Package



TOP VIEW - D Package

SR00307

Figure 35. VGA AC Evaluation Board Layout (SO Package)

Audio processor – companding, VOX and amplifier section SA5752

DESCRIPTION

The SA5752 is a high performance low power audio signal processing system especially designed to meet the requirements for small size and low voltage operation of hand-held equipment. The SA5752 subsystem includes a low noise microphone preamplifier with adustable gain, a noise cancellation switching amplifier with adjustable threshold, a voice operated transmitter (VOX) switch, VOX control, an audio compressor with buffered input, audio expandor, and an internal bandgap voltage regulator with power down capability. When used with Philips Semiconductors' SA5753, the complete audio processing function of an AMPS or TACS cellular telephone is easily implemented. The system also meets the requirements of the proposed NAMPS or NTACS specifications. The SA5752 can also be used without the SA5753 in a wide variety of radio communications applications.

FEATURES

- Operating voltage range: 2V to 5.5V
- Miniature SSOP
- High performance
- Adjustable VOX and noise cancellation threshold
- Adjustable gain preamplifier
- Audio companding
- ESD protected
- Open collector VOX output
- Logic inputs CMOS compatible
- Power down mode
- Few external components
- Meets AMPS/TACS/NAMPS/NTACS requirements

PIN CONFIGURATION

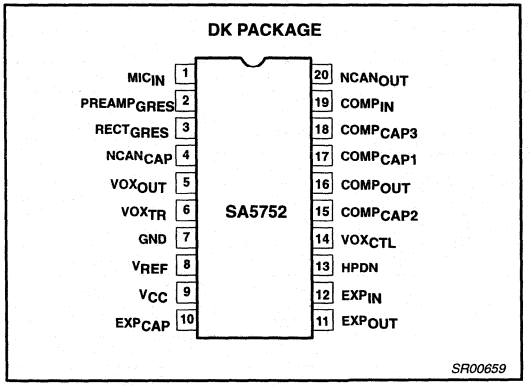


Figure 1. Pin Configuration

BENEFITS

- Very compact applications
- Long battery life in portable equipment
- Complete cellular audio function with the SA5753

APPLICATIONS

- Cellular radio
- Mobile communications
- High performance cordless telephones
- 2-way radio

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Shrink Small Outline Package (SSOP)	-40 to +85°C	SA5752DK	SOT266-1

PIN DESCRIPTIONS

PIN NO.	SYMBOL	DESCRIPTION
1	MIC_{IN}	Microphone input
2	$PREAMP_{GRES}$	Preamplifier gain resistor
3	$RECT_{GRES}$	Rectifier gain resistor
4	$NCAN_{CAP}$	Noise cancellation timing capacitor
5	VOX_{OUT}	Voice operated transmission output
6	VOX_{TR}	Voice operated transmission threshold resistor
7	GND	Ground
8	V_{REF}	Reference voltage
9	V_{CC}	Positive supply
10	EXP_{CAP}	Expandor timing capacitor
11	EXP_{OUT}	Expandor output
12	EXP_{IN}	Expandor input
13	HPDN	Hardware power-down
14	VOX_{CTL}	Voice operated transmission control
15	$COMP_{CAP2}$	Compressor capacitor 2 DC block
16	$COMP_{OUT}$	Compressor output
17	$COMP_{CAP1}$	Compressor timing capacitor 1
18	$COMP_{CAP3}$	Compressor capacitor 3 DC block
19	$COMP_{IN}$	Compressor input
20	$NCAN_{OUT}$	Noise cancellation output

BLOCK DIAGRAM

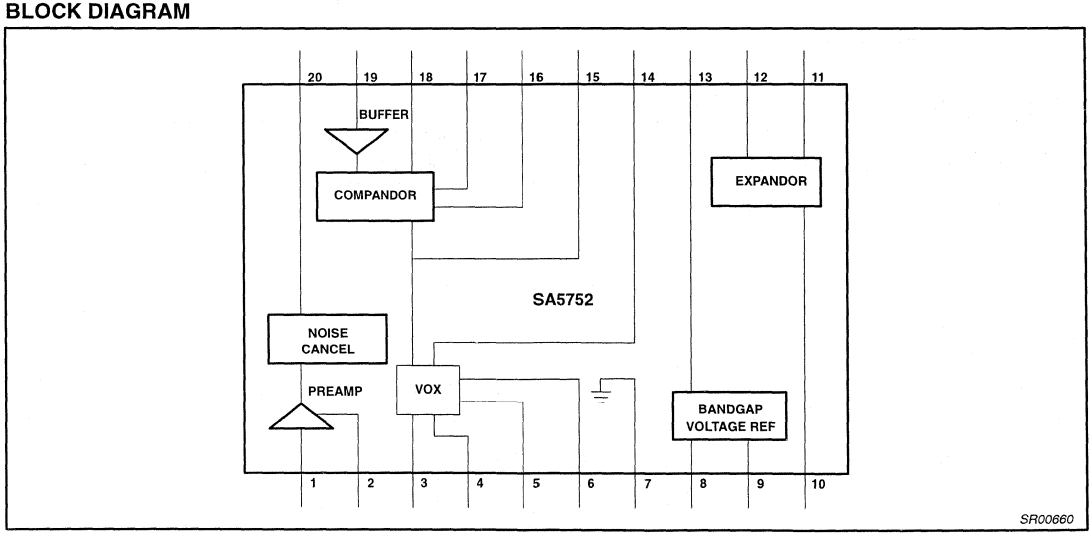


Figure 2. Block Diagram

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Power supply voltage range	-0.3 to 6	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{CC}+0.3)	V
T_{STG}	Storage temperature	-65 to +150	°C
T_A	Ambient operating temperature	-40 to +85	°C

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = +3.0V, 0dB = 77.5mV_{RMS}. See test circuit, Figure 6.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
V_{CC}	Supply voltage		2.7[4]	3.0	5.5	V
I_{CC}	Supply current	No signal Power down mode		3.1 125	4.0	mA µA
Z_L	Load impedance pins $NCAN_{OUT}$, EXP_{OUT}		50			kΩ
	$COMP_{OUT}$[1]		10			kΩ
Z_{IN}	Input impedance $COMP_{IN}$, MIC_{IN}		40	50	60	kΩ
	EXP_{IN}[2]		2.0			kΩ
	Noise cancellation current	Pin 6		25		µA
V_{OS}	DC offset $NCAN_{OUT}$[3]		-50	–3.0	50	mV

NOTES:
1. Compressor is tested in production with 50kΩ load.
2. Not tested in production.
3. Offset values are identical for both gain states of noise reduction circuit.
4. Operational down to V_{CC} = 2V.

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = +3.0V, 0dB level = 77.5mV_{RMS}. See test circuit, Figure 6.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
	Preamplifier gain range Preamplifier voltage gain 0dB Preamplifier voltage gain 40dB	 Pin 2 open Pin 2 AC ground	0 -1.0 39.0	 0 40	40 1.0 41.0	dB dB dB
	Preamplifier noise density	Pin 2 AC grounded RS = 50kΩ unweighted 20Hz-20kHz		7		nV/√Hz
		weighted CCIR DIN45405 20-20kHz		8		nV/√Hz
	Switch amplifier gain		9	10	11	dB
Compandor 1kHz, all tests[1]						
$COMP_{OUT}$	Compressor error at -21dB output level	Input level = -42dB	–1.0	–0.16	1.0	dB
$COMP_{OUT}$	Compressor error at -10dB output level	Input level = -20dB	-1.0	–0.11	1.0	dB
$COMP_{OUT}$	Compressor error at 0dB output level	Input level = 0dB	-1.5	+0.1	1.5	dB
$COMP_{OUT}$	Compressor error at +5dB output level	Input level = +10dB	-1.0	+0.04	1.0	dB
$COMP_{OUT}$	Compressor error at +10dB output level	Input level = +20dB	-1.0	+0.02	1.0	dB
EXP_{OUT}	Expandor error at -42dB output level	Input level = -21dB	–1.0	–0.12	1.0	dB
EXP_{OUT}	Expandor error at -21dB output level	Input level = -10.5dB	-1.0	+0.1	1.0	dB
EXP_{OUT}	Expandor error at -10dB output level	Input level = -5dB	-1.0	+0.03	1.0	dB

AC ELECTRICAL CHARACTERISTICS (Contineud)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
EXP_{OUT}	Expandor error at 0dB output level	Input level = 0dB	-1.5	–0.2	1.5	dB
EXP_{OUT}	Expandor error at +10dB output level	Input level = +5dB	-1.0	+0.03	1.0	dB
EXP_{OUT}	Expandor error at +20dB output level[2]	Input level = +10dB	-1.0	–0.1	1.0	dB
EXP_{OUT}	Expandor V_{OS}	No signal	-50.0	+3.0	50.0	mV
EXP_{OUT}	Expandor output DC shift	No signal to 0dB	-100	+2.0	100	mV
	Timing capacitors compandor			2200		nF
THD	Total harmonic distortion					
	Compressor	1kHz, 0dB BW=300-3kHz		0.2	1	%
	Expandor	1kHz, 0dB BW=300-3kHz		0.1	1	%
	$NCAN_{OUT}$	1kHz. Pin 2 open output level = 0dB		0.02	1	%
		1kHz, Pin 2 open output level = +20dB		0.06	1	%
VOX_{OUT}	Sink current				0.5	mA
	Low level High level	Open collector I_L = 0.5mA		 V_{CC}	0.4	V V
VOX_{CTL}	Input current Low		-50	–6.6	0	µA
	High		-10	–0.02	+10	µA
	Input level Low High		0 $0.7V_{CC}$		$0.3V_{CC}$ V_{CC}	V V
H_{PDN}	Input current Low		-10	–4.1	+10	µA
	High		-10	–0.2	+10	µA
	Input level Low High		0 $0.7V_{CC}$		$0.3V_{CC}$ V_{CC}	V V
	Reference filter capacitor			10		µF

NOTE:
1. Measurements are relative to 0dB output.
2. Measurement is indicative of the output dynamic range capability.

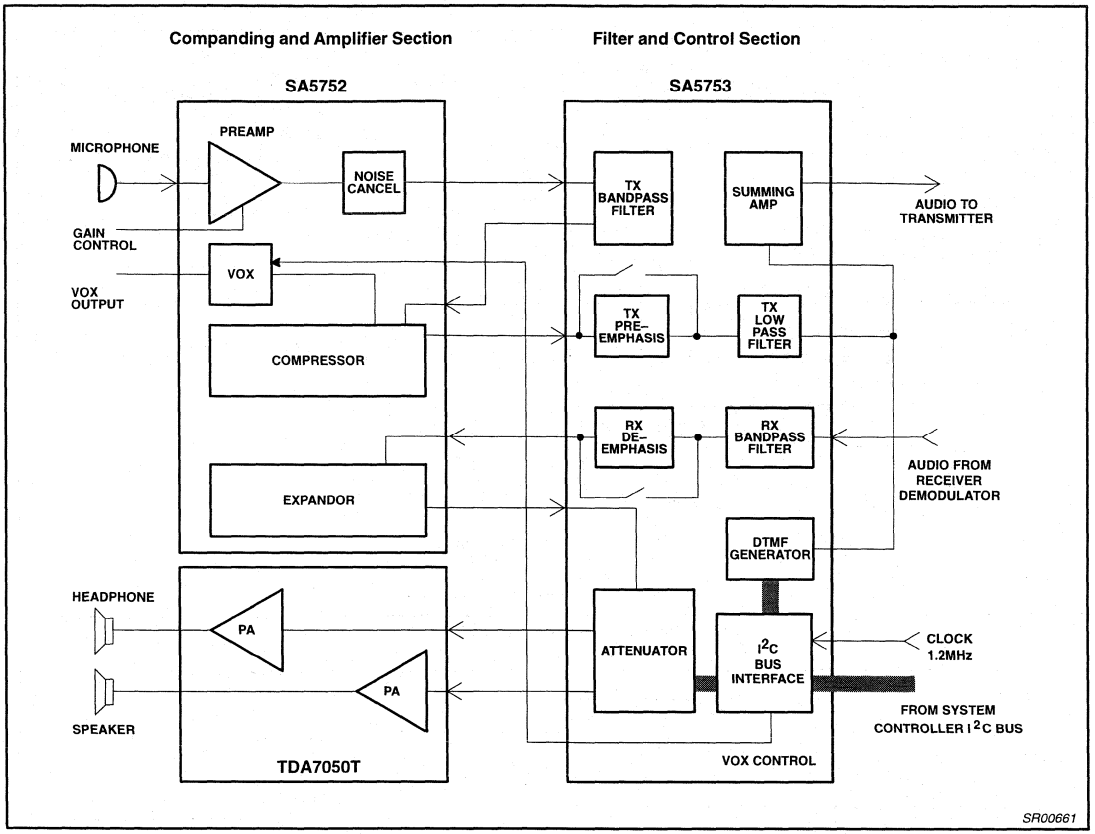


Figure 3. Typical Configuration of Audio Processor (APROC) System Chip Set

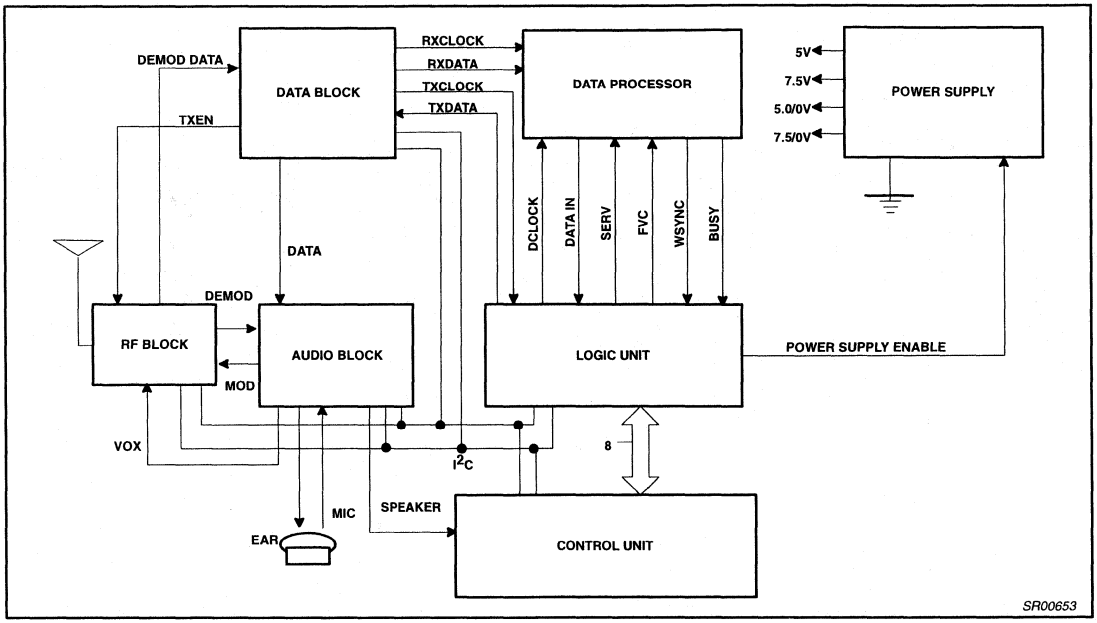


Figure 4. Cellular Radio System

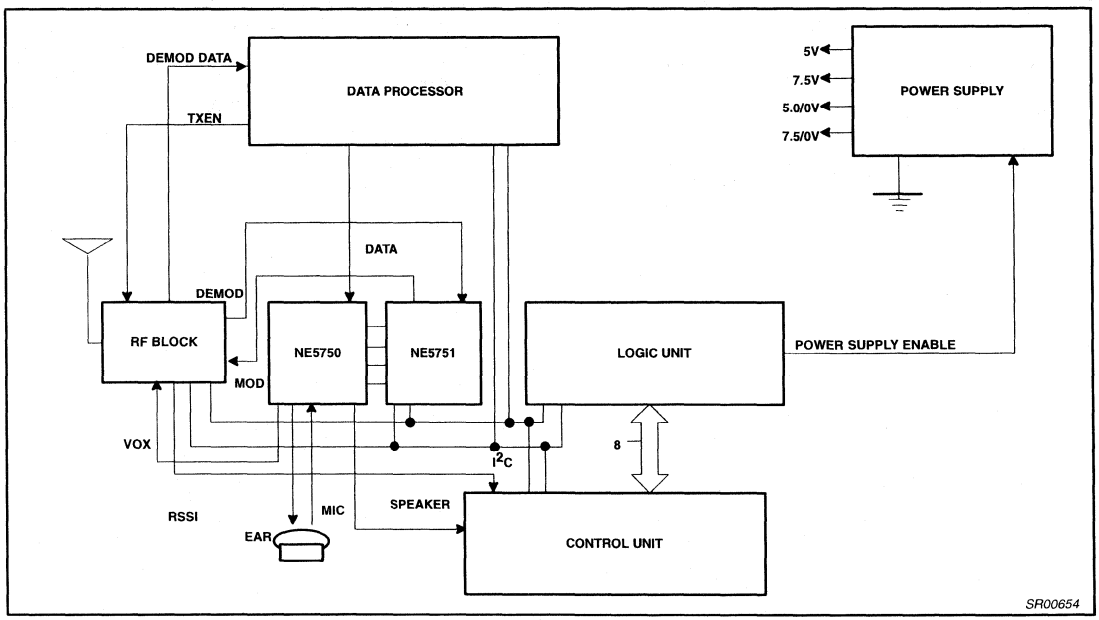


Figure 5. APROC Application Diagram

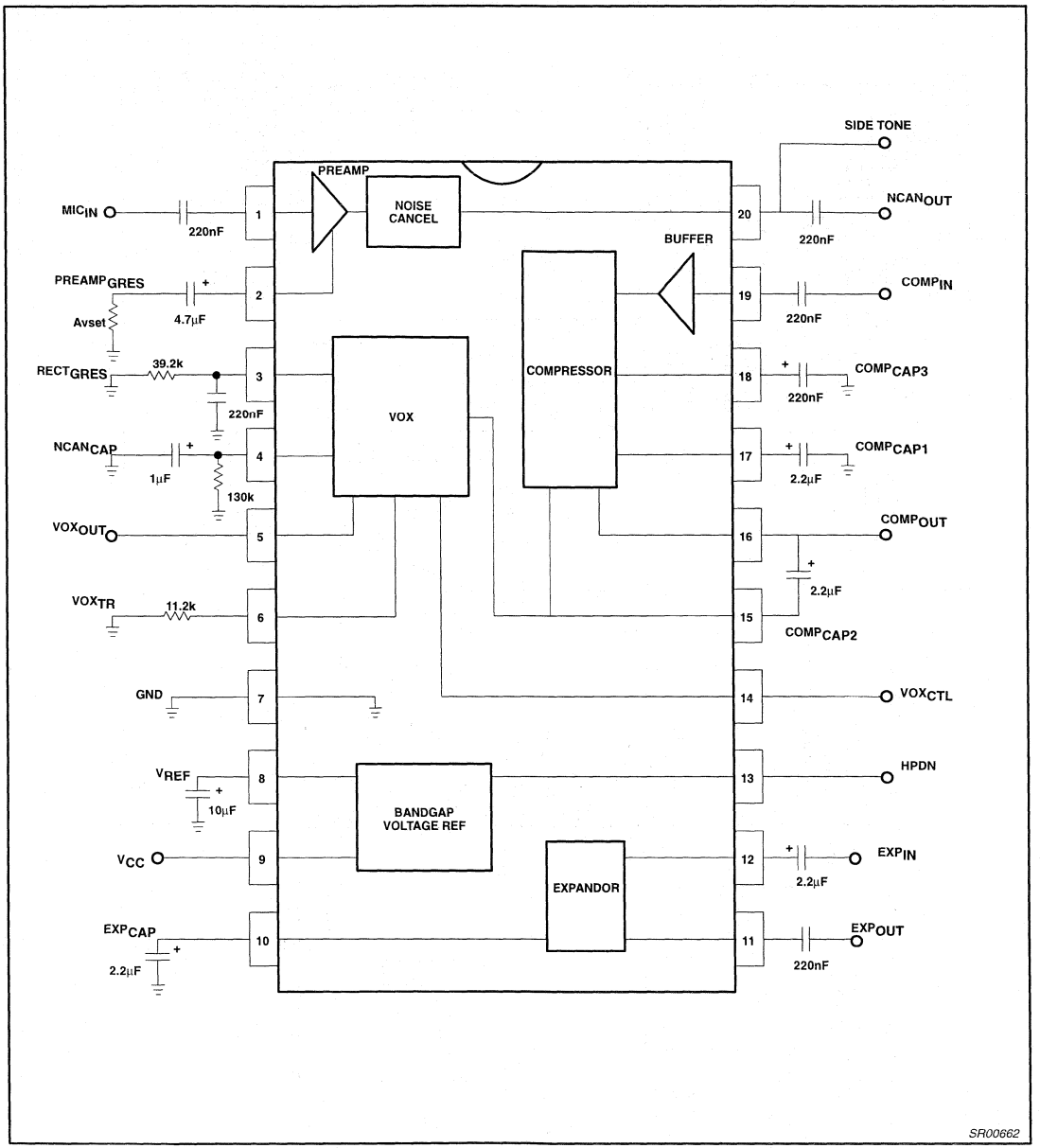


Figure 6. SA5752 Test and Application Circuit

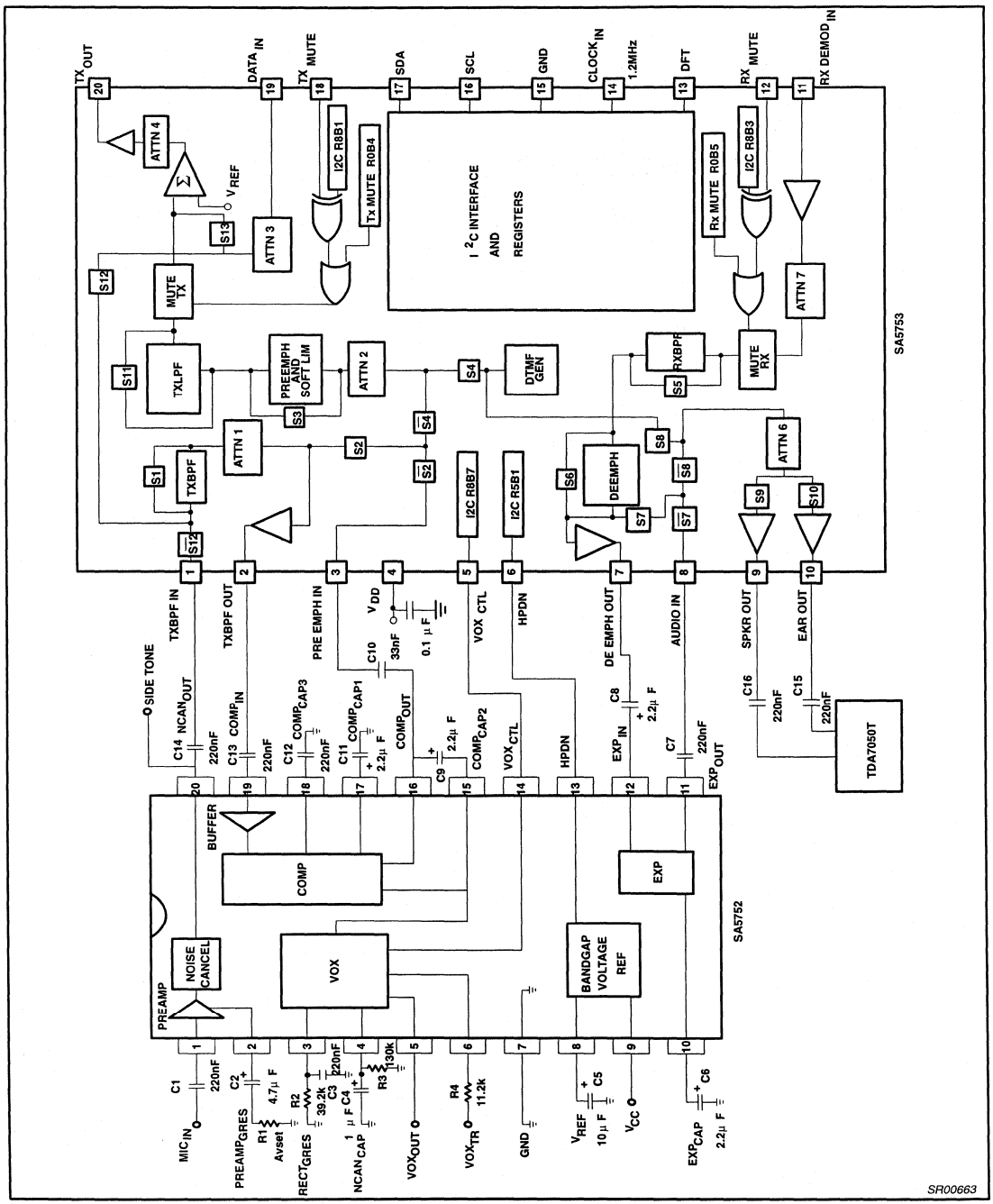


Figure 7. Application Diagram for the Audio Processor

TYPICAL PERFORMANCE CHARACTERISTICS

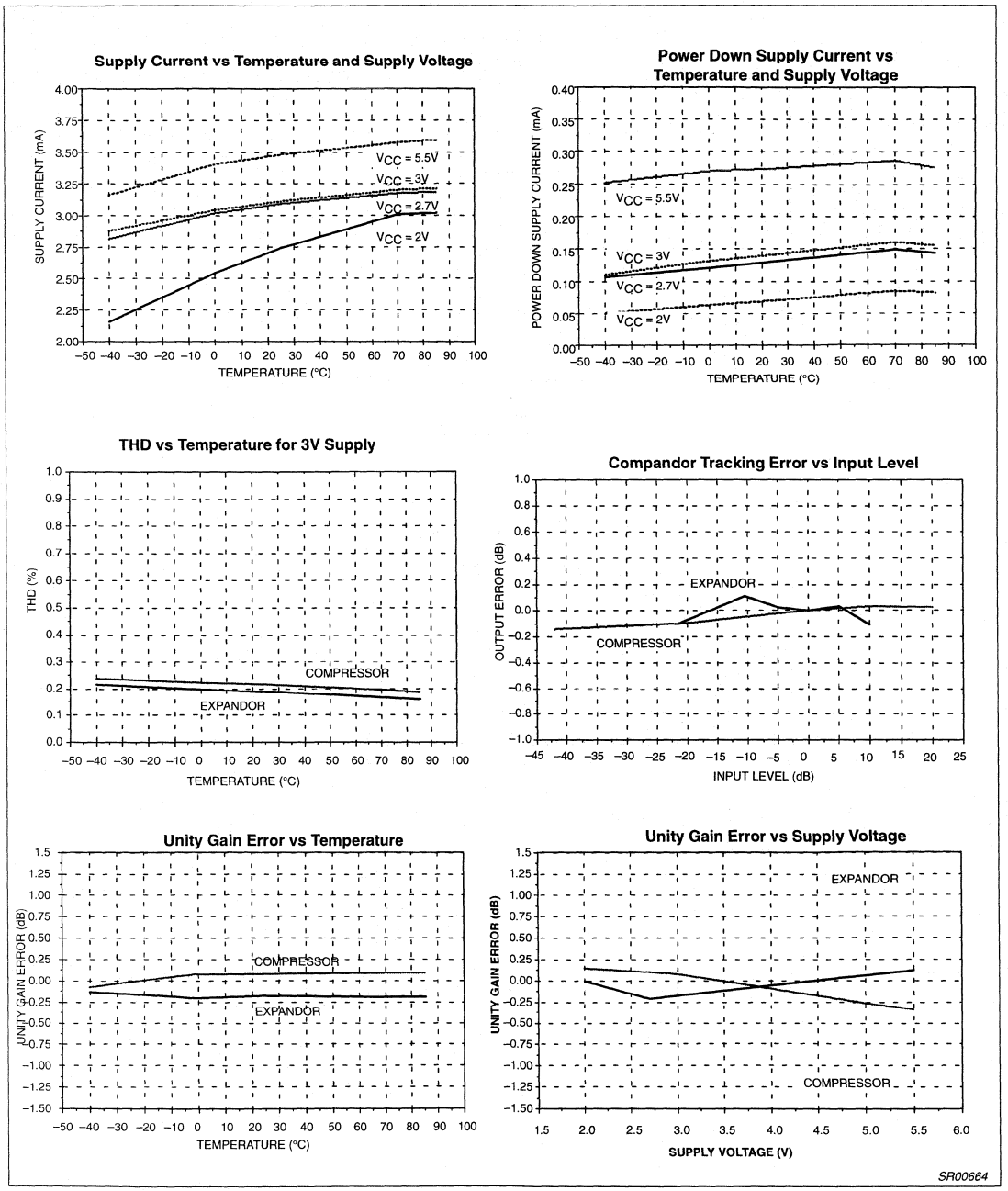
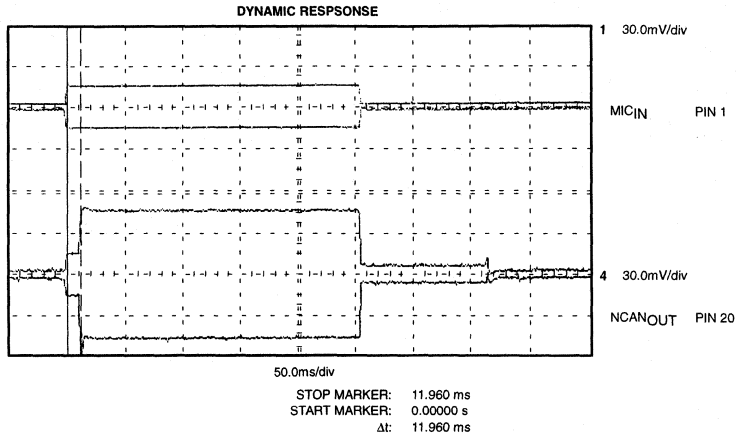


Figure 8. Typical Performance Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Noise Cancellation Switching Amplifier



Voice Activated Transmitter (VOX)

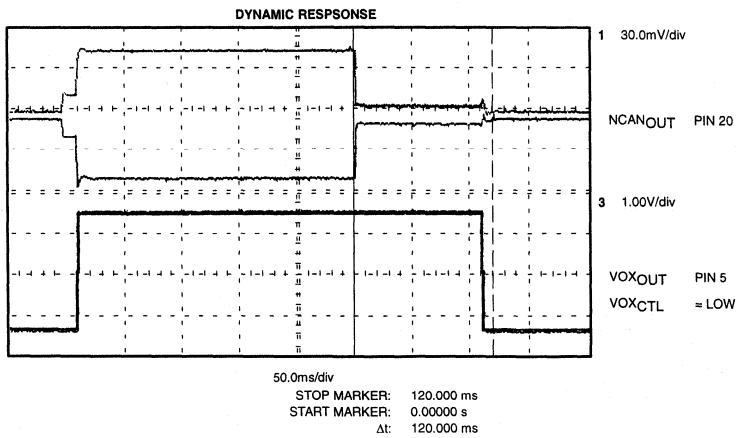


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Figure 9. Typical Performance Characteristics (cont.)

Audio processor – filter and control section SA5753

DESCRIPTION

The SA5753 is a high performance low power CMOS audio signal processing system especially designed to meet the requirements for small size and low voltage operation of hand-held equipment. The SA5753 subsystem includes complementary transmit/receive voice band (300-3000Hz), switched capacitor bandpass filters with pre-emphasis and de-emphasis respectively, a transmit low pass filter, peak deviation limiter for transmit, digitally controlled attenuators for signal level and volume control, audio path mute switches, a programmable DTMF generator, power-down circuitry for low current standby, power-on reset capability, and an I^2C interface. When the SA5753 is used with an SA5752 (companding function), the complete audio processing system of an AMPS, TACS, NAMPS or NTACS cellular telephone is easily implemented.

The system also meets the requirements of the proposed NAMPS or NTACS specification, and can be used in cordless telephone applications.

The SA5753 can be operated without the I^2C bus interface by pulling DFT (Pin 13) HIGH.

BENEFITS

- Very compact application
- Long battery life in portable equipment
- Complete cellular audio function with the SA5752

APPLICATIONS

- Cellular radio
- Mobile communications
- High performance cordless telephones
- 2-way radio

PIN CONFIGURATION

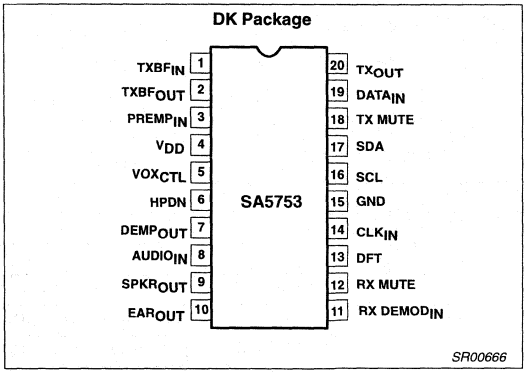


Figure 1. Pin Configuration

FEATURES

- Low 3V supply
- Miniature SSOP package
- Low power
- High performance
- Built-in programmable DTMF generator
- Built-in digitally controlled attenuators for modulation and volume control
- Built-in peak-deviation limiter
- I^2C Bus controlled
- Power-on reset
- Power down capability
- Programmable mute control
- Meets AMPS/TACS/NAMPS/NTACS requirements

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Shrink Small Outline Package (SSOP)	-40 to +85°C	SA5753DK	SOT266-1

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Power supply voltage range	-0.3 to 6	V
V_{IN}	Voltage applied to any other pin	-0.3 to V_{DD}+0.3	V
	Storage temperature	-65 to +150	°C
T_A	Ambient operating temperature	-40 to +85	°C

PIN DESCRIPTIONS

PIN NO.	SYMBOL	DESCRIPTION
1	$TXBF_{IN}$	Transmit bandpass filter input
2	$TXBF_{OUT}$	Transmit bandpass filter output
3	$PREMP_{IN}$	Pre-emphasis input
4	V_{DD}	Positive supply
5	VOX_{CTL}	Vox control output
6	HPDN	Power-down I/O
7	$DEMP_{OUT}$	De-emphasis output
8	$AUDIO_{IN}$	Audio input
9	$SPKR_{OUT}$	Audio output to speaker
10	EAR_{OUT}	Audio output to earpiece
11	RX $DEMOD_{IN}$	Rx demodulated audio signal input
12	RX MUTE	RX audio signal mute input
13	DFT	Default input, non-I^2C or stand-alone operation
14	CLK_{IN}	Clock input (1.2MHz)
15	GND	Ground
16	SCL	I^2C serial clock line
17	SDA	I^2C serial data line
18	TX MUTE	Tx audio signal mute input
19	$DATA_{IN}$	Data input
20	TX_{OUT}	Transmit output

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{DD} = +3.3V, unless otherwise specified. See test circuit, Figure 2.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
V_{DD}	Power supply voltage		3.0	3.3	5.5	V
I_{DD}	Supply current	Operating IDLE Power Down (PWDN)		1.7 600 200		mA µA µA
I_{IH}	Input current high TX MUTE, RX MUTE, HPDN DFT	$V_{IN} = V_{DD}$	 –10 0	 0 +10	 +10 +30	 µA µA
I_{IL}	Input current low TX MUTE, RX MUTE, HPDN, DFT	V_{IN} = GND	 –30 –10	 –10 0	 0 +10	 µA µA
V_{IH}	Input voltage high		0.7V_{DD}		V_{DD}	V
V_{IL}	Input voltage low		0		0.3V_{DD}	V

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{DD} = +3.3V. See test circuit, Figure 2. Clock frequency = 1.2MHz; test level = 0dBV = 77.5mV_{RMS} = -20dBm, unless otherwise specified. All gain control blocks (Attenuators) = 0dB gain, NAMPS and VCO bits set to 0.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
	RX BPF anti alias rejection			40		dB
	RX BPF input impedance	f= 1kHz		100		kΩ
	RX BPF gain with de-emphasis	f = 1kHz	-1.0	0	1.0	dB
	RX BPF gain with de-emphasis	f = 100Hz		-30		dBm0
	RX BPF gain with de-emphasis	f = 300Hz	8.5	9.6	11.5	dBm0
	RX BPF gain with de-emphasis	f = 3kHz	-11.5	-10.0	-8.5	dBm0
	RX BPF gain with de-emphasis	f = 5.9kHz		-58		dBm0
	RX BPF noise with de-emphasis	300Hz-3kHz		200		µV_{RMS}
	RX dynamic range	with deemphasis		80		dB
	$DEMP_{OUT}$ output impedance	f = 1kHz			40	Ω
	$DEMP_{OUT}$ output swing (1%)	2kΩ to $V_{DD/2}$; f = 1kHz		2.4		V_{P-P}
	$SPKR_{OUT}$ ouput swing (1%)	50kΩ to$V_{DD/2}$; f = 1kHz	V_{DD} -1	2.4		V_{P-P}
	EAR_{OUT} output swing (1%)	50kΩ to $V_{DD/2}$; f = 1kHz	V_{DD} -1	2.4		V_{P-P}
	$SPKR_{OUT}$ noise / EAR_{OUT} noise			200		µV_{RMS}
	CLK_{IN} high		2.1		3.0	V
	CLK_{IN} low		0		1.0	V
	TX BPF anti alias rejection	f > 50kHz		40		dB
	TX BPF input impedance	f = 3kHz		100		KΩ
	TX BPF noise	300 - 3000kHz		200		µV_{RMS}
	TX LPF gain	f = 5.9kHz		-39	-36	dBm0
	TX LPF gain with pre-emphasis	f = 1kHz, 0dBV		2.43		dB
	TX LPF gain with pre-emphasis	f = 100Hz		-19		dBm0
	TX LPF gain with pre-emphasis	f = 300Hz		-10.45		dBm0
	TX LPF gain with pre-emphasis	f = 3kHz		9.14		dBm0
	TX LPF gain with pre-emphasis	f = 5900Hz		-28		dBm0
	TX LPF gain with pre-emphasis	f = 9kHz		-48		dBm0
	TX overall gain	1kHz		2.43		dB
	TX overall gain	100Hz		-58	-44	dBm0
	TX overall gain	300Hz	-11.5	-10.4	-8.5	dBm0

AC ELECTRICAL CHARACTERISTICS (continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
	TX overall gain	3kHz	8	9	9.6	dBm0
	TX overall gain	5.9kHz		-52	-45	dBm0
	TX BPF dynamic range			TBD		dB
	$PREMP_{IN}$ input impedance	f = 3kHz		100		kΩ
	TX_{OUT} Slew rate	C_L = 15pF		0.75		V/µs
	Output impedance	f = 3kHz			40	Ω
	Output swing (limiting)			1.2		V_{P-P}
	Output swing (1% THD)	5kΩ load (25°C)		1.0		V_{P-P}
	Tx DTMF signal with TXLPF and pre-emphasis			0.45		V/kHz
	Rx DTMF sidetone		–0.8		5.2	dBm0
	Time delay to mute from RX MUTE or TX MUTE transition	$V_{IN} = V_{IL}$ to V_{IH} $V_{IN} = V_{IH}$ to V_{IL}		0.5 0.5		µs µs

Table 1. Gain Control Blocks (Bit 0 is Least Significant Bit)

SYMBOL	Bits	TYPICAL STEP (dB)	TYPICAL GAIN (dB)	
			MIN	MAX
A1	4	–0.8	–12.0	0
A2a	5	±0.25	–3.75	+3.75
A2b	2	–6, (–12 on first)	–24.0	0
A3	4	–1.0	–17.0	–2.0
A4	4	±0.5	–3.5	+3.5
A6	4	–2.0	–30.0	0
A7	4	±0.5	–3.5	+3.5
NAMPS	1		+1.9 in A2b –7.6 in A4	
VCO	1		+6.0 in A4	
For A2a, A4 and A7:		MSB sets the sign of the gain MSB = 0 for gain MSB = 1 for attenuation		
For all Gain Blocks:		All bits set to 0 = 0dB gain All bits set to 1 = maximum gain or attenuation		

FUNCTIONAL DESCRIPTION

The SA5753 is an audio signal processor designed to meet the requirements of compact low voltage radio telephone equipment. It includes transmit and receive bandpass filters for voiceband (300-3000Hz) with pre-emphasis and de-emphasis respectively, a transmit peak deviation limiter, voice channel mute switches and a data path which can be summed into the transmit channel. An I^2C interface is provided for software programmability of a DTMF generator, mute polarity, selection of different power down and operating modes and control of the gain in both the transmit and receive channels.

Software programmable gain control allows the device to be automatically optimized during equipment production and offers flexibility during normal operation.

Gain Blocks

The programmable gain blocks are shown in Table 1 and Figure 2. The purpose for each block is as follows:

a. A1 compensates for microphone gain variations in the transmit path.

b. A2a compensates for transmitter dynamic range variations due to manufacturing tolerances of the SA5753 and SA5752 compandor companion device. To meet AMPS requirements, the dynamic range between the zero crossing signal level of the compandor and the peak signal allowed by the deviation limiter is adjusted to 12.34dB.

c. A2b allows coarse attenuation to be inserted in the transmit path to eliminate positive feedback effects in hands-free speaker applications. First step is 12dB followed by two steps of 6dB.

d. A3 sets the gain between the $DATA_{IN}$ pin (Pin 19) and the TX_{OUT} pin (Pin 20) and should be adjusted after A2a and A4 have been previously optimized. The SA5753 will interface directly with the UMA1000T data processor (which produces a 2Vpk data signal). For NAMPS applications an additional 10 to 14dB resistive divider must be added at the $DATA_{IN}$ pin (Pin 19) for a 2V data signal.

e. A4 compensates for transmit gain variations due to manufacturing tolerances of the SA5753, SA5752 and VCO connected to TX_{OUT} (Pin 20). After A2a has been adjusted to set dynamic range then A4 is used to set the peak output voltage at TX_{OUT} (Pin 20) such that a nominal 10kHz/V VCO produces a peak deviation of 12kHz to meet AMPS specifications.

f. A6 is the volume control for both the $SPKR_{OUT}$ and EAR_{OUT}.

g. A7 compensates for manufacturing tolerances in the SA5753 and preceeding demodulator. For AMPS requirements, a 1kHz tone with 2.9kHz deviation should produce an output signal at $DEMP_{OUT}$ (Pin 7) corresponding to the zero crossing signal level of the expandor.

NAMPS and VCO Offsets

For NAMPS applications, a '1' programmed into R5B3 (register 5, bit 3) will offset the transmit gain for NAMPS applications. It is recommended that A2a and A4 be programmed after the NAMPS option is set to compensate for manufacturing tolerances in the NAMPS offset, itself.

When the VCO bit of R5B2 is a '1', an extra gain of 6dB is provided at TX_{OUT} for direct interface to VCOs with a nominal gain of 5kHz/V.

Operation Using the I²C Communications Bus

The SA5753 includes on-chip gain blocks and options which can be programmed through an I²C interface bus. To use this capability, the DFT pin (Pin 13) must be pulled LOW. In this mode, all signal level adjustments can be made through software with no external potentiometers required.

With DFT pulled LOW, the HPDN pin (Pin 6) is an OUTPUT having the same value as the program bit in register 5 bit 1 (R5B1) of the control register bit map. The value at the VOX_{CTL} output (Pin 5) is the same as the program bit in R8B7. The HPDN and VOX_{CTL} outputs can be used to control the state of the SA5752 companion device.

Power On Reset and Power Down Modes

In order to avoid undefined states of the SA5753 when power is initially applied, a power-on-reset circuit is incorporated which defaults RxP and TxP such that the receive and transmit paths are muted if a 'high' voltage is applied to RX MUTE and TX MUTE (Pins 12 and 18). RX MUTE and TX MUTE include on-chip pull up resistors so, during power up, the user may apply a logic '1' to these pins or leave them floating. After power up, the registers can be programmed and the mutes removed by a quick access write to R0.

Three software controlled low power modes are provided on the SA5753. These are POWER DOWN (PWDN), IDLE and DENA and can be selected by programming a '1' into R6B2, R6B1 or R6B0 as follows. In PWDN mode (R6B2=1) both the voice and data channels are powered down with the respective I/O pins at a high impedance. In DENA mode (R6B1=1) the voice channels are powered down, but the data channel (from $DATA_{IN}$ and TX_{OUT}) is fully active. In IDLE mode (R6B1=1, R6B0=1) both voice and data channels are powered down. (See Table on page 8.)

The difference between selecting IDLE and PWDN is that the former maintains the normal operational bias voltages at all voice and data I/O pins and provides a glitch-free transfer from power down to a fully active mode and vice-versa.

Although the POWER DOWN mode exhibits lower power consumption, glitches may occur when transferring to an active mode because of the previous high impedance of the I/O pins.

The VOX_{CTL} and HPDN pins (Pins 5 and 6) still have the same value as R8B7 and R5B1 in all low power modes.

Operation Without Using the I²C Bus

The SA5753 can be operated in a default mode with the I²C bus bypassed. To use this mode, the DFT pin (Pin 13) is pulled HIGH, then the I²C bus is bypassed and the SA5753 operates as if all register bits in the I²C address map table are set to '0' except R1B2 (S13), R0B0 (S10) and R0B1 (S9), which are set to '1' to enable the receiver output. R6B2 (PWDN), which is controlled by the state of the HPDN pin (Pin 6), which is an input in DEFAULT mode.

When HPDN is pulled HIGH, the R6B2 bit is set to '0' and the SA5753 is placed in it's normal operating mode with all Gain Control Blocks set to 0dB except A3, which is set to –2dB.

When HPDN is pulled LOW, the R6B2 bit is set to '1' and the SA5753 enters POWER DOWN.

There is no on-chip pull-up or pull-down structure on the HPDN pin and so it must not be allowed to float in DEFAULT mode since the operating mode of the SA5753 will then be undetermined.

The Tx MUTE and Rx MUTE pins must be pulled LOW to enable the transmit and receive paths, respectively.

The VOXCTL pin (Pin 5) will follow the value of the control bit stored in R8B7 prior to pulling DFT HIGH.

The DTMF is disabled in the DEFAULT mode.

Programming Without the I²C Protocol

In the default mode, with DFT (Pin 13) and HPDN (Pin 6) pulled HIGH, the registers in the control register bit map are chained together so that bit 0 of a register is connected to bit 7 of the preceeding register with R0B6, R0B7, R1B6 and R1B7 bypassed, i.e., R0B5 is connected to R1B0, R1B5 is connected to R2B0, R2B7 is connected to R3B0, etc. Bits can then be loaded as a serial stream through the SDA pin of the I²C bus by the negative edge of a shifting clock applied at the SCL pin of the I²C bus. When a bit is loaded at SDA it will load first into R0B0 and then will be shifted to R8B7 after 68 clock edges.

A total of 68 clock pulses (applied at SCL) are therefore required to completely load the registers.

In this mode of operation the contents of the register map are also shifted out from the VOX_{CTL} pin since it takes the same value as R8B7. After power up there is no reset within the registers so the first 68 bits clock out at the VOX_{CTL} pin will have an indeterminate value.

Summary: To use this capability, the DFT pin and the HPDN pin must be pulled HIGH, the serial bit stream loaded through SCL synchronous with the negative clock edge applied at SCL for 68 clock pulses, and then the DFT pin pulled LOW.

NOTE: Default Mode is not tested in production.

Cordless Telephone Applications

For cordless telephone applications, a switch S12 is provided (R5B0) to route data through the complete transmit path while inhibiting the voice channel. In the receive path, a quick access mode is provided through the I²C to disable both EAR_{OUT} and $SPKR_{OUT}$, by setting R0B0 and R0B1, when data is detected at the $DEMP_{OUT}$ pin (Pin 7).

I²C CHARACTERISTICS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both SDA and SCL are bidirectional lines connected to a positive supply voltage via a pull-up resistor. When the bus is free, both lines are HIGH. Data transfer may be initiated only when the bus is not busy (both lines HIGH).

The output devices, or stages, connected to the bus must have an open drain or open collector output in order to perform the wired-AND function.

Data at the I²C bus can be transferred at a rate up to 100kbits/s. The number of devices connected to the bus is solely dependent on the maximum allowed bus capacitance of 400pF.

For devices operating over a wide range of supply voltages, such as the SA5753, the following levels have been defined for a logical LOW and HIGH;

$V_{ILMAX} = 0.3V_{DD}$ (max. input LOW voltage)
$V_{IHMIN} = 0.7V_{DD}$ (min. input HIGH voltage)

Data Transfer

Data is transferred from a transmitting device to a receiving device with one data bit transferred during each clock pulse on the SCL line. The transmitter also generates the clock once arbitration has given it control of the SCL line. The data on the SDA line must remain stable during the HIGH period of the clock cycle, otherwise it may be interpreted as a control signal.

Start and Stop Conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH to LOW transition of the data line while the clock line is HIGH is defined as a start condition. A LOW to HIGH transition of the data line while the clock is HIGH is defined as a stop condition.

Acknowledgement

Following each byte of data transfered, the receiver must acknowledge successful reception. To do this the transmitter releases the SDA line (allowing it to go HIGH) at the end of each transmitted byte, and it is pulled LOW by the receiver. If this condition is maintained during the next HIGH period of the clock pulse (called the acknowledge clock pulse) then data transfer is resumed. If the receiver does not pull the SDA line LOW, the transmitter will abort the transfer.

I²C Bus Data Configurations

The SA5753 is always a slave receiver in the I²C bus configuration). The slave address consists of eight bits in the serial mode and is internally fixed.

Control Registers

The control register bit map is shown below. Either a quick access or normal address mode can be used, determined by the two MSB bits in the first word following the SA5753 address word. If the quick access mode is used, the registers R0 or R1 can be updated by sending only two bytes of information (address plus update). If R0 or R1 are updated using the address mode, then B7 and B6 of the data word are ignored. In all access modes, incremental register addressing is supported with following words updating the next register until a 'stop' bit is sent.

High Tone DTMF Register

MSB							LSB
HD7	HD6	HD5	HD4	HD3	HD2	HD1	HD0

The eight bits determine the output frequency by the following formula.:

High Frequency = 1200kHz/6/HD
where HD is the value of the register.

Low Tone DTMF Register

MSB							LSB
LD7	LD6	LD5	LD4	LD3	LD2	LD1	LD0

The eight bits determine the output frequency by the following formula.:

Low Frequency = 1200kHz/14/LD
where LD is the value of the register.

The operation of the 96ms DTMF timer is initiated by the loading of the low tone DTMF register. This timer terminates transmission of the tones as the generated tones cross the reference level after 96ms. The on time of the tones can thus vary by up to one cycle of the tones.

Continuous tones can be obtained by again loading DTC = 1 in R1, bit 5.

Single tones can be obtained by loading 2 into the unused tone register to silence it.

Loading a value of 1 or 0 into the registers will default the register value to 257 or 256 for high tone or low tone, respectively.

Phase continuous frequency modulation can be produced by loading a new value into a DTMF register during continuous operation (DTC=1).

I²C Address and Access

S	A7 A6 A5 A4 A3 A2 A1 A0	ACK	F7 F6 F5 F4 F3 F2 F1 F0	ACK	...	P

S = start, A0 = 0, ACK = acknowledge, P = stop, A7–0 = SA5753 address fixed internally at 1000000.
Access mode is determined by F7, F6.

All access modes support incremental addressing.

Mode	F7	F6	Action
quick access	0	0	Load F5–F0 to R0B5 – R0B0
quick access	0	1	Load F5-F0 to R1B5 – R1B0
test mode	1	0	For test only. DO NOT USE.
address mode	1	1	F3–F0 point to register

Address Map

REG	Address				Register Bits							
	F3	F2	F1	F0	B7	B6	B5	B4	B3	B2	B1	B0
R0	0	0	0	0	Y	Y	RxM	TxM	A2bb1	A2bb0	S9	S10
R1	0	0	0	1	Y	Y	DTC	S4	S8	S13	S7	S2
R2	0	0	1	0	HD7	HD6	HD5	HD4	HD3	HD2	HD1	HD0
R3	0	0	1	1	LD7	LD6	LD5	LD4	LD3	LD2	LD1	LD0
R4	0	1	0	0	A1b3	A1b2	A1b1	A1b0	A4b3	A4b2	A4b1	A4b0
R5	0	1	0	1	A6b3	A6b2	A6b1	A6b0	NAMPS	VCO	HPDN	S12
R6	0	1	1	0	A2ab4	A2ab3	A2ab2	A2ab1	A2ab0	PWDN	IDLE 1	IDLE 0
R7	0	1	1	1	A3b3	A3b2	A3b1	A3b0	A7b3	A7b2	A7b1	A7b0
R8	1	0	0	0	VOX_{CTL}	S3	S5	S6	S11	RxP	TxP	S1

Y = ignored in address mode.
For all bits TRUE = '1'

A1b3–0 = program bits for gain block A1
A2ab4–0 = program bits for gain block A2a
A2bb1–0 = program bits for gain block A2b
A3b3–0 = program bits for gain block A3
A4b4–0 = program bits for gain block A4
A5b2–0 = program bits for gain block A5
A6b3–0 = program bits for gain block A6
A7b3–0 = program bits for gain block A7
HD7–0 = high tone DTMF
LD7–0 = low tone DTMF
NAMPS = program bit for NAMPS offset
VCO = 6dB higher TX_{OUT}
RxM = receive mute
TxM = transmit mute
RxP = receive mute polarity
VOX_{CTL} = enable VOX of compandor/expander circuit. This bit appears at the VOX_{CTL} pin (Pin 5) of the SA5753.
HPDN = enable power down of compandor circuit. This bit appears at the HPDN pin (Pin 6) of the SA5753
PWDN, IDLE1, IDLE0 see Table below

TxP = transmit mute polarity
DTC = DTMF continuous
S1 = bypass TXBPF
S2 = bypass compressor in TX path, inhibit pre-emph input
S3 = bypass pre-emp and limiter in Tx path
S4 = enable DTMF to TX path and inhibit $PREMP_{IN}$ and S2.
S5 = bypass RXBPF
S6 = bypass de-emph in RX path
S7 = bypass expandor in RX path, inhibit audio input
S8 = enable DTMF to RX path and inhibit $AUDIO_{IN}$ and S7.
S9 = enable $SPKR_{OUT}$
S10 = enable EAR_{OUT}
S11 = bypass TXLPF
S12 = cordless data option established
S13 = enable data path

Low Power Modes (R6B0 – R6B2)

PWDN	IDLE1	IDLE0	
1	X	X	(PWDN) Complete power down except I²C, I/Os high impedance.
0	1	0	(DENA) Low power, I/Os at $V_{DD}/2$, $DATA_{IN}$ to TX_{OUT} enabled.
0	1	1	(IDLE) Low power, I/Os at $V_{DD}/2$, $DATA_{IN}$ to TX_{OUT} disabled.
0	0	0	Normal operation.
0	0	1	$DATA_{IN}$ to TX_{OUT} disabled.

X = don't care.

SR00667

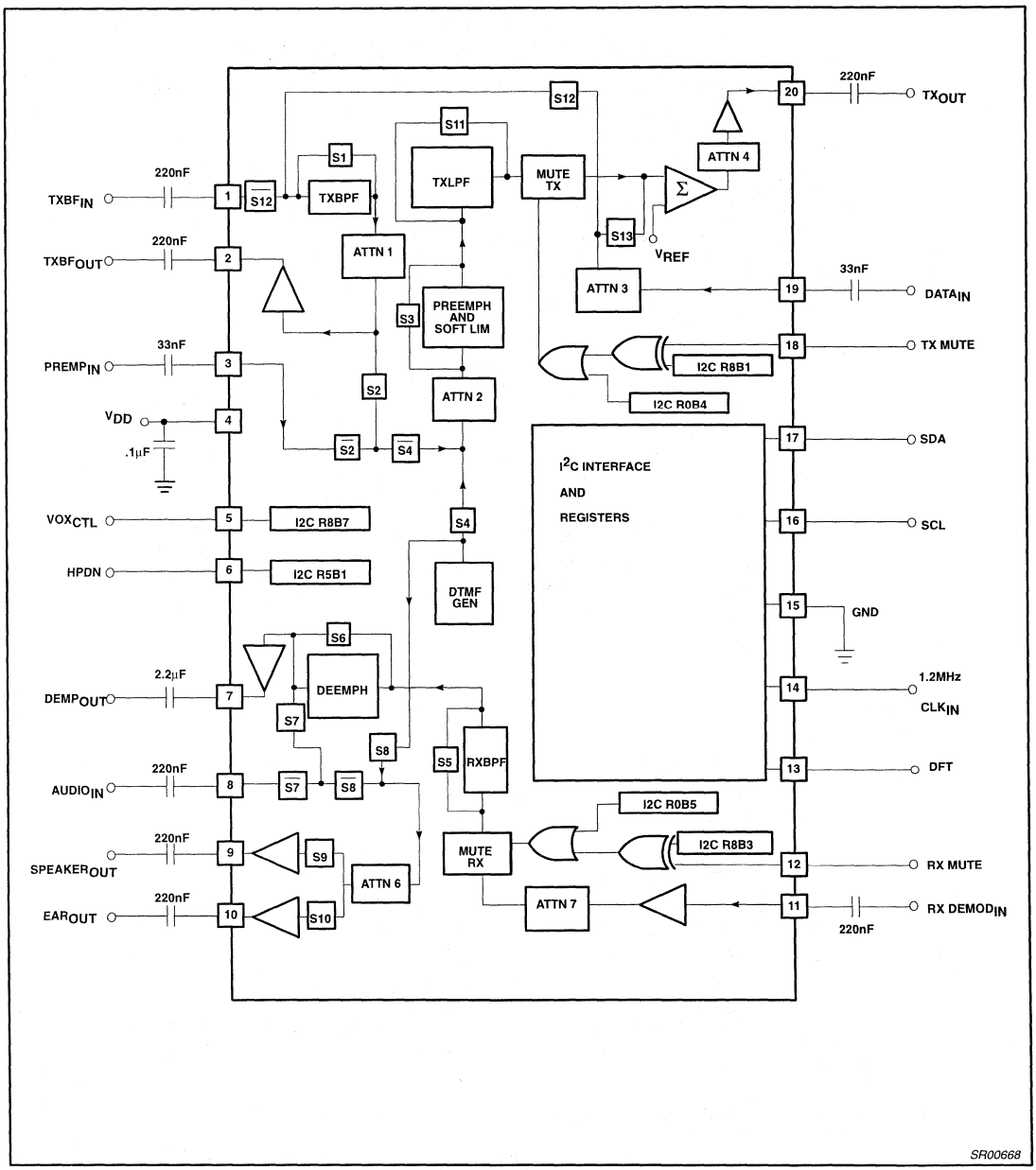


Figure 2. SA5753 Test and Application Circuit

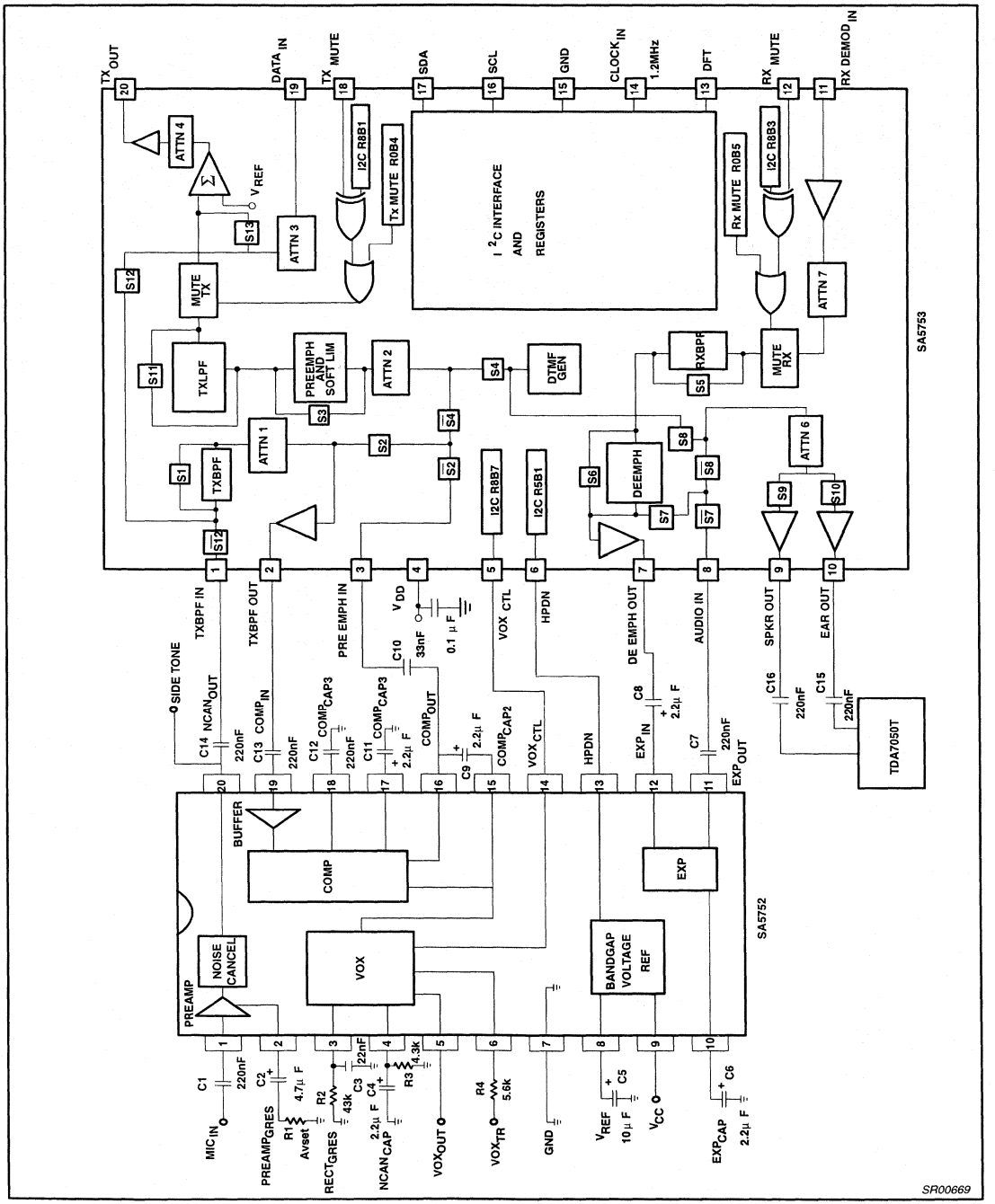


Figure 3. Application Diagram for the Audio Processor

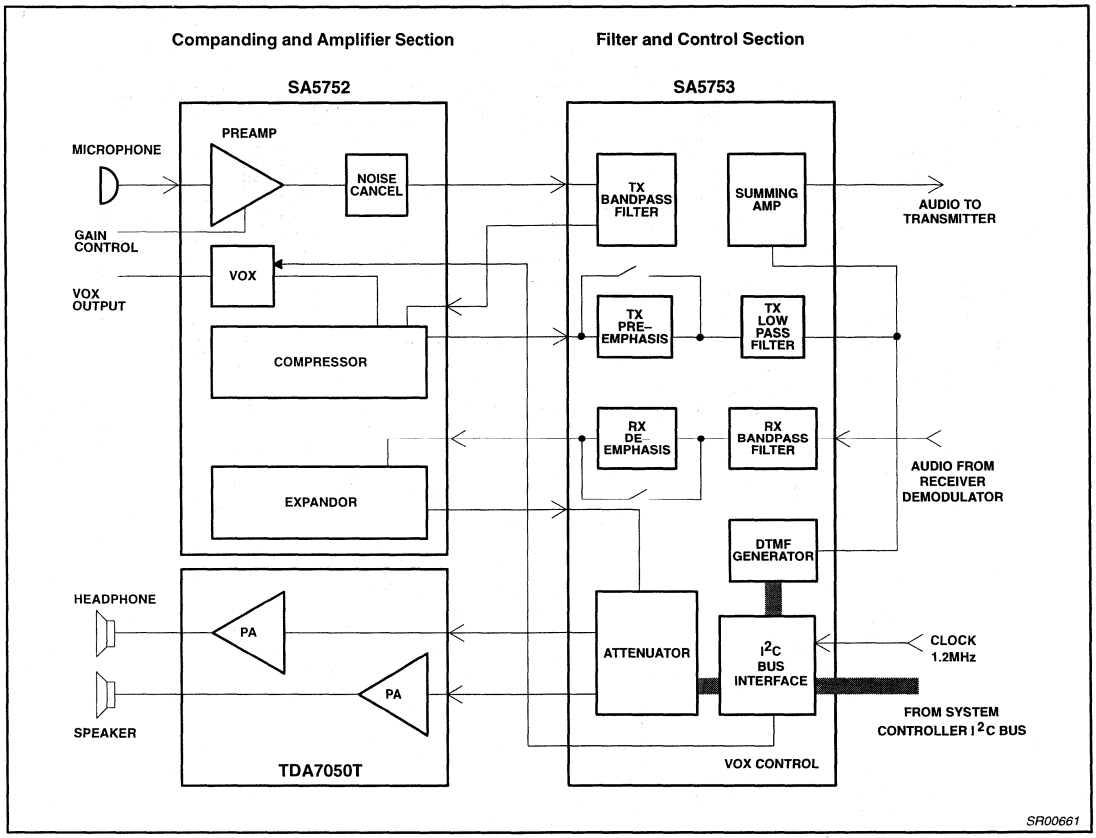


Figure 4. Typical Configuration of Audio Processor (APROC) System Chip Set

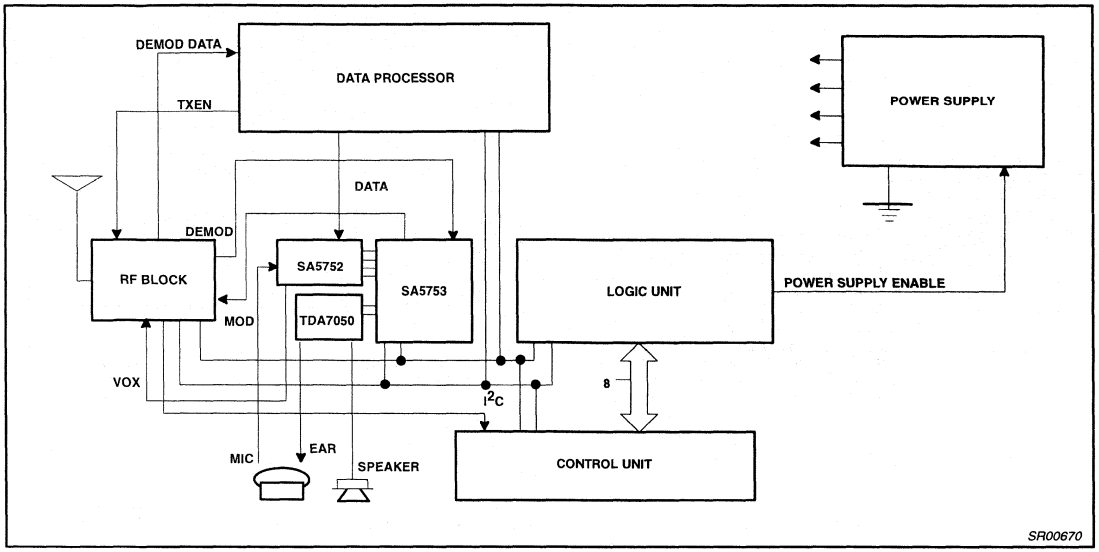


Figure 5. APROC Application Diagram

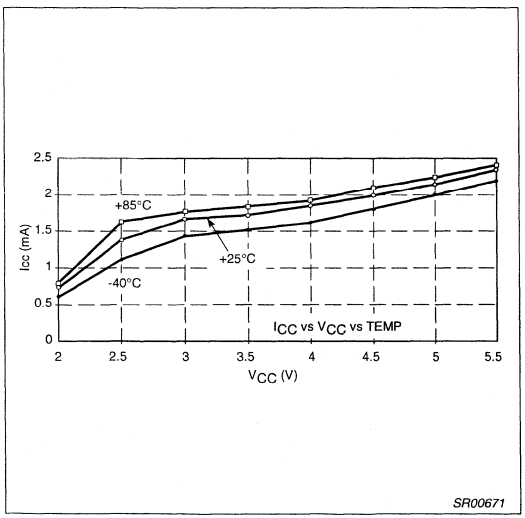


Figure 6. SA5753 Normal Operation

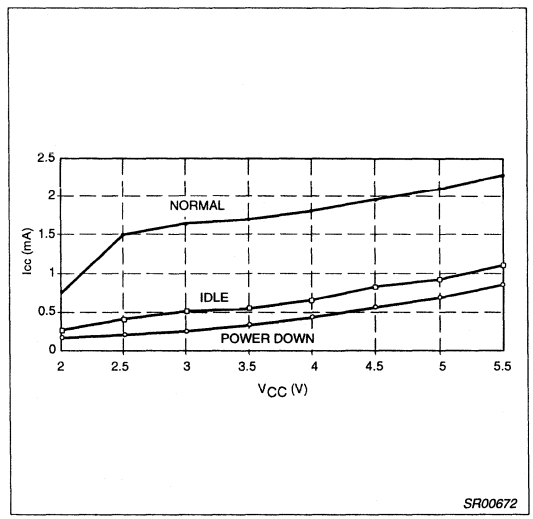


Figure 7. SA5753 Power Mode Comparison (I_{CC})

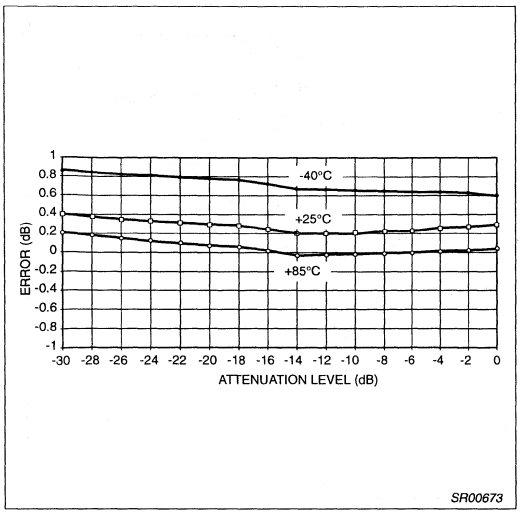


Figure 8. Gain Control, A6 Linearity

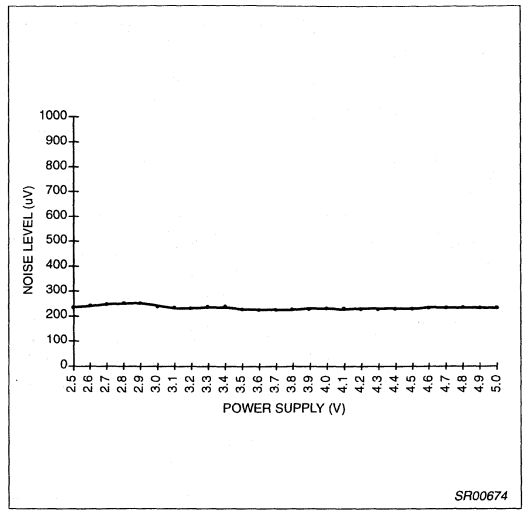


Figure 9. Power Supply vs Noise at TXBPF (25°C)

1.3GHz low voltage fractional–N synthesizer SA7016

FEATURES

- Low phase noise
- Fully programmable main divider
- Internal fractional spurious compensation
- Hardware and software power down

APPLICATIONS

- PCS
- Cellular phones
- Portable battery–powered radio equipment.

General description

The SA7016 BICMOS device integrates programmable dividers, charge pumps and a phase comparator to implement a phase–locked loop. The device is designed to operate from 3 NiCd cells, in pocket phones, with low current and nominal 3 V supplies.

The synthesizer operates at VCO input frequencies up to 1.3 GHz. The synthesizer has fully programmable main and reference dividers. All divider ratios are supplied via a 3–wire serial programming bus.

Separate power and ground pins are provided to the analog and digital circuits. The ground leads should be externally short–circuited to prevent large currents flowing across the die and thus causing damage. V_{DDCP} should be equal to V_{DD}.

The charge pump current (gain) is fixed by an external resistance at pin RSET (pin). Only passive loop filters are used; the charge–pump operates within a wide voltage compliance range to provide a wider tuning range.

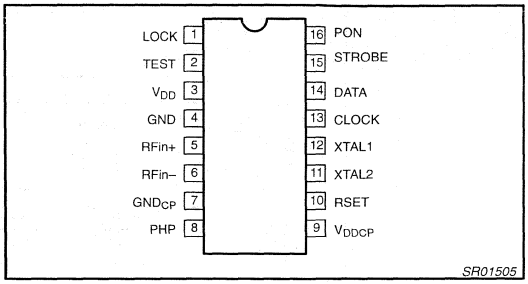


Figure 1. Pin Configuration

Quick reference data

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply voltage	V_{DD}	2.7	–	5.5	V
V_{DDCP}	Analog supply voltage	$V_{DDCP} = V_{DD}$	2.7	–	5.5	V
$I_{DDCP}+I_{DD}$	Supply current		–	5.0	6.0	mA
$I_{DDCP}+I_{DD}$	Total supply current in power–down mode		–	25	–	µA
f_{VCO}	Input frequency		500	–	1300	MHz
f_{XTAL}	Crystal reference input frequency		10	–	40	MHz
f_{PC}	Maximum phase comparator frequency		–		4	MHz
T_{amb}	Operating ambient temperature		–40	–	+85	°C

Ordering information

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SA7016	TSSOP16	Plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403–1

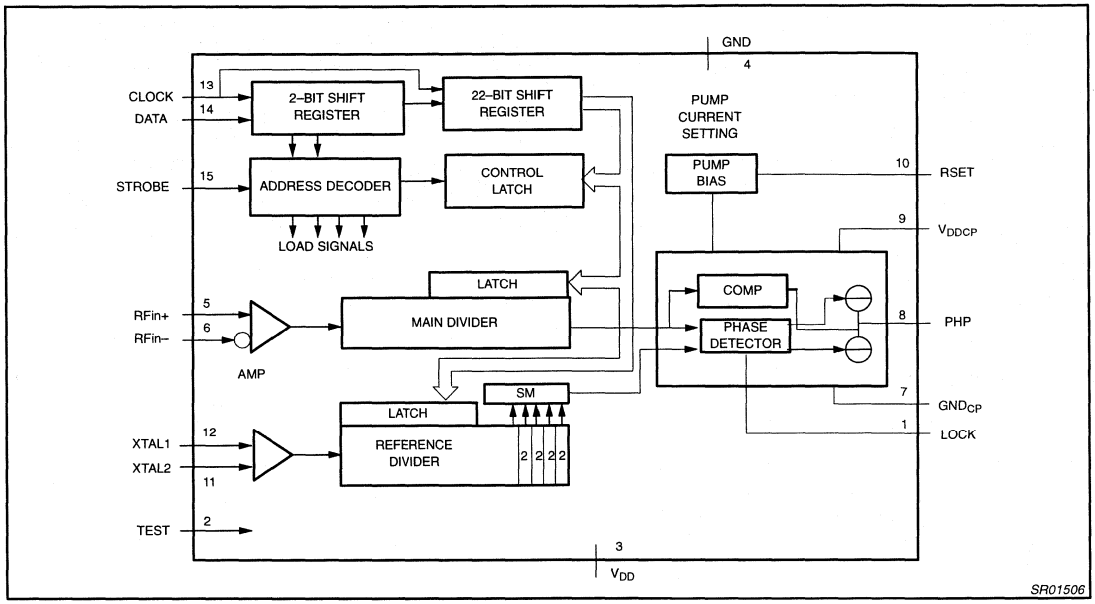


Figure 2. Block Diagram

PINNING

SYMBOL	PIN	DESCRIPTION
LOCK	1	Lock detect output
TEST	2	Test
V_{DD}	3	Digital supply
GND	4	Digital ground
RFin+	5	RF positive input to main divider
RFin–	6	RF negative input to main divider
GND_{CP}	7	Charge pump ground
PHP	8	Main NORMAL chargepump
V_{DDCP}	9	Charge pump supply voltage
RSET	10	External resistor from this pin to ground sets the chargepump current
XTAL2	11	Reference input
XTAL1	12	Reference input
CLOCK	13	Programming bus clock input
DATA	14	Programming bus data input
STROBE	15	Programming bus enable input
PON	16	Power down control

FUNCTIONAL DESCRIPTION

Main Fractional–N divider

The RFin input (pins 5 and 6) drive a pre–amplifier to provide the clock to the first divider stage. For single ended operation, the signal should be fed to one of the inputs while the other one is AC grounded. The pre–amplifier has a high input impedance, dominated by pin and pad capacitance. The circuit operates with signal levels from –15dBm to +0dBm, and at frequencies as high as 1.3 GHz. The divider consists of a fully programmable bipolar prescaler followed by a CMOS counter. Divide ratios (512 to 65536) allow a minimum phase comparison frequency of 25kHz at 1.3 GHz RF.

At the completion of a main divider cycle, a main divider output pulse is generated which will drive the main phase comparator. Also, the fractional accumulator is incremented by the value of NF. The accumulator works with modulo Q set by FMOD. When the accumulator overflows the overall division ratio N will be increased by 1 to N + 1, the average division ratio over Q main divider cycles (either 5 or 8) will be

$$Nfrac = N + \frac{NF}{Q} \quad (1)$$

The output of the main divider will be modulated with a fractional phase ripple. The phase ripple is proportional to the contents of the fractional accumulator and is nulled by the fractional compensation charge pump.

The reloading of a new programming word is synchronized to the state of the main divider to avoid introducing a phase disturbance.

Phase detector

The reference and main (aux) divider outputs are connected to a phase/frequency detector that controls the charge pump. The pump current is set by a an external resistor. The dead zone (caused by finite time taken to switch the current sources on or off) is cancelled by forcing the pumps ON for a minimum time at every cycle (backlash time) providing improved linearity.

Lock Detect

The output LOCK maintains a logic '1' when the phase detector indicates a lock condition. The lock condition is defined as a phase difference of less than ± 1 period of the frequency at the inputs XTAL1,2. Out of lock (logic '0') is indicated when the counter is powered down.

Power–down mode

The power–down signal can be either hardware (PON) or software (PD). The PON signal exclusively ORed with the PD signal. If PON=0, then the part is powered up when PD=1. PON can be used to invert the polarity of the software bit PD. When the synthesizer is reactivated after the power–down the main and reference dividers are synchronized to avoid possibility of random phase errors on power–up.

Reference divider

The reference divider consists of a divider with programmable values between 4 and 1023.

Serial programming bus

The serial input is a 3–wire input (CLOCK, STROBE, DATA) to program all counter divide ratios, fractional compensation DAC, selection and enable bits. Figure 5 shows the timing diagram of the serial input. When the STROBE goes active HIGH, the clock is disabled and the data in the shift register remains unchanged. Depending on the 2 address bits the data is latched into different working registers or temporary registers. In order to fully program the synthesizer, 2 words must be sent: B, and A. Table 1 shows the format and the contents of each word. The D word is for testing purposes only. The data for the fractional compensation DAC, FC is stored by the B word in temporary registers. When the A word is loaded, the data of these temporary registers is loaded together with the main divider ratio.

Limiting values

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	Digital supply voltage	–0.3	+5.5	V
V_{DDCP}	Analog supply voltage	–0.3	+5.5	V
$\Delta V_{DDCP}–V_{DD}$	Difference in voltage between V_{DDCP} and V_{DD}		±0.3	V
V_n	Voltage at pins 1, 2, 5, 6, 11 to 16	–0.3	V_{DD} + 0.3	V
V_1	Voltage at pin 8, 9	–0.3	V_{DDCP}+ 0.3	V
ΔV_{GND}	Difference in voltage between GND_{CP} and GND (these pins should be connected together)	–0.3	+0.3	V
P_{tot}	Total power dissipation		TBD	mW
T_{stg}	Storage temperature	–55	+125	°C
T_{amb}	Operating ambient temperature	–30	+85	°C
T_j	Maximum junction temperature		TBD	°C

Handling

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

Thermal characteristics

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	Thermal resistance from junction to ambient in free air	120	K/W

Characteristics

V_{DDCP}=V_{DD}=3.0V, T_A=25°C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply; pins 3, 9						
V_{DD}	Digital supply voltage		2.7	–	5.5	V
V_{DDCP}	Analog supply voltage	V_{DDCP} = V_{DD}	2.7	–	5.5	V
$I_{DDTotal}$	Synthesizer operational digital supply current	V_{DD} = 3.0V	–	5.0	6.0	mA
$I_{standby}$	Total supply current in power–down mode	logic levels 0 or V_{DD}	–	25	TBD	µA
RFin main divider input; pins 5, 6						
f_{VCO}	VCO input frequency		500	–	1300	MHz
$V_{RFin(rms)}$	AC–coupled input signal level	R_s = 50 Ω; MAX. limit is indicative	–20	–	0	dBm
Z_{IRFin}	Input impedance (real part)	f_{VCO} = 1.0 GHz	–	TBD	–	kΩ
C_{IRFin}	Typical pin input capacitance	indicative, not tested	–	TBD	–	pF
N_m	Main divider ratio		512	–	65535	
f_{PCmax}	Maximum loop comparison frequency	indicative, not tested	–	–	4	MHz
Reference divider input; pins 11, 12						
f_{REFin}	Input frequency range from crystal		10	–	40	MHz
VRFin	AC–coupled input signal level	R_S=50Ω; MAX. limit is indicative	–5	–	+5	dBm
Z_{REFin}	Input impedance (real part)		–	TBD	–	kΩ
C_{REFin}	Typical pin input capacitance	indicative, not tested	–	TBD	–	pF
R_{REF}	Reference division ratio		4	–	1023	
Charge pump current setting resistor input; pin 10						
R_{SET}	External resistor from pin 3 to ground		6	7.5	24	kΩ
V_{SET}	Regulated voltage at pin 3	R_{SET}=7.5 kΩ	–	1.23	–	V
Charge pump outputs (including fractional compensation pump); pins 8; R_{SET} =7.5 KΩ, FC=80						
Icp	Charge pump current ratio to Iset	Current gain I_{PH}/I_{SET}	–15		+15	%
I_{MATCH}	Sink–to–source current matching	V_{ph}=1/2 V_{DDCP}.	–5		+5	%
I_{ZOUT}	Output current variation versus Vph[2]	V_{ph} in compliance range	–10		+10	%
I_{LPH}	Charge pump off leakage current	V_{cp}=1/2 V_{CC}	–10	±1	+10	nA
V_{ph}	Charge pump voltage compliance		0.7	–	V_{DDCP}–0.8	V
Phase noise						
C/N	Synthesizer's contribution to close–in–phase noise of 900 MHz RF signal at 1 kHz offset.	fref=19.44MHz; fcomp=240kHz indicative, not tested	–	–83	–	dBc Hz
Interface logic input signal levels; pins 3, 11, 12, 14, 15, 16						
V_{IH}	HIGH level input voltage		0.7*V_{DD}	–	V_{DD}+0.3	V
V_{IL}	LOW level input voltage		–0.3	–	0.3*V_{DD}	V
I_{bias}	Input bias current	logic 1 or logic 0	–5	–	+5	µA

Lock detect output signal (in push/pull mode); pin 1						
V_{OL}	LOW level output voltage	I_{sink}=2mA	–	–	0.4	V
V_{OH}	HIGH level output voltage	I_{source}=–2mA	V_{DD}–0.4	–	–	V

NOTES:

1. $I_{SET} = \frac{V_{SET}}{R_{SET}}$ bias current for charge pumps.

2. The relative output current variation is defined thus:

$$\frac{\Delta I_{OUT}}{I_{OUT}} = 2 \cdot \frac{(I_2 - I_1)}{|(I_2 + I_1)|}; \text{ with } V_1 = 0.7V,\ V_2 = V_{DDCP} - 0.8V \text{ (See Figure 3.)}$$

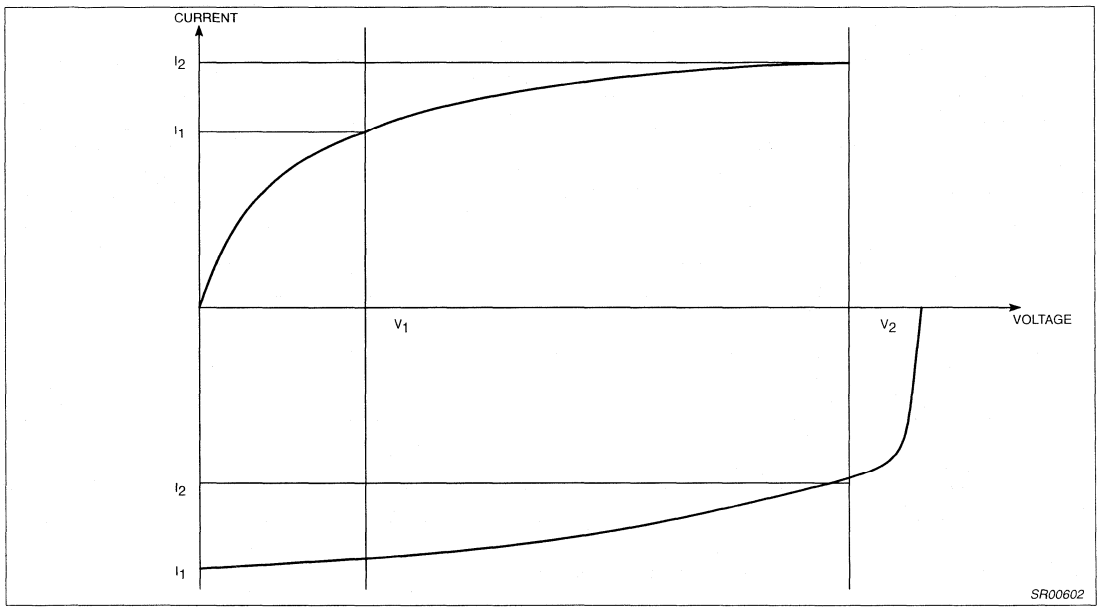


Figure 3. Relative Output Current Variation

Serial bus timing characteristics. See Figure 4.

V_{DD}= V_{DDCP} =3.0V; T_{amb} = 25°C unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Serial programming clock; CLK					
t_r	Input rise time	–	10	40	ns
t_f	Input fall time	–	10	40	ns
T_{cy}	Clock period	100	–	–	ns
Enable programming; STROBE					
t_{START}	Delay to rising clock edge	40	–	–	ns
t_W	Minimum inactive pulse width	1/fcomp	–	–	ns
$T_{SU;\overline{E}}$	Enable set–up time to next clock edge	20	–	–	ns
Register serial input data; DATA					
$t_{SU;DAT}$	Input data to clock set–up time	20	–	–	ns
$t_{HD;DAT}$	Input data to clock hold time	20	–	–	ns

Application information

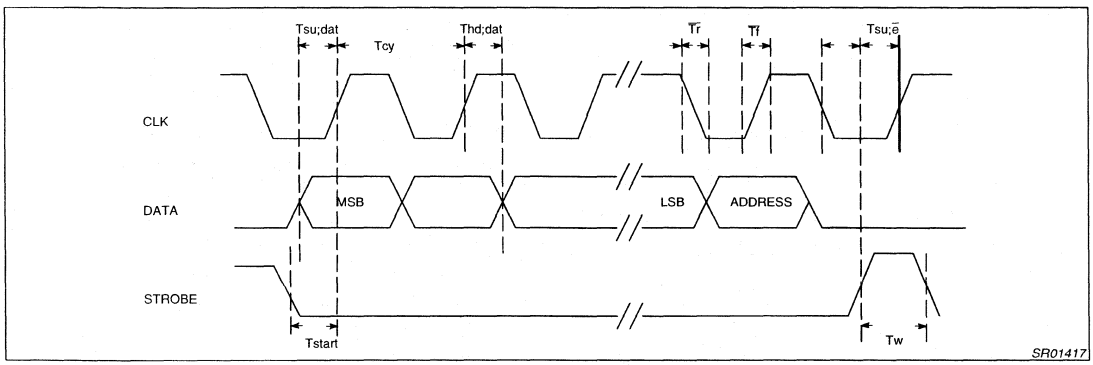


Figure 4. Serial Bus Timing Diagram

Main Output Charge Pump and Fractional Compensation Current.

The main charge pump on pin PHP is driven by the main phase detector; and the charge pump current values are determined by the current at pin RSET. The fractional compensation is derived from the current at RSET, the contents of the fractional accumulator FRD and by the program value of the FC DAC. The timing for the fractional compensation is derived form the main divider. See table of charge pump ratios.

Data format

Table 1 Format of programmed data

LAST IN		MSB	SERIAL PROGRAMMING FORMAT				FIRST IN LSB
p23	p22	p21	p20	../..	../..	p1	p0

Table 2 A word, length 24 bits

LAST IN					MSB														LSB	FIRST IN	
Address		fmod	Fractional–N			Main Divider ratio														Spare	
0	0	FM	NF2	NF1	NF0	N15	N14	N13	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	N0	SP1	SP2
Default:		0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	1	0	0	0	0	0	0

A word select	Fixed to 00.
Fractional Modulus select	FM 0=modulo 8, 1=modulo 5.
Fractional–N Increment	NF2..0 Fractional N Increment values 000 to 111.
N–Divider	N0..N15, Main divider values 512 to 65535 allowed for divider ratio.

B word, length 24 bits

ADDRESS		REFERENCE DIVIDER										LOCK	PD	CP	FRACTIONAL COMPENSATION DAC								SPARE
0	1	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	LO	MAIN	CP0	FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0	SP3
Default:		0	0	0	1	0	1	0	0	0	1	0	0	0	0	1	0	1	0	0	0	0	0

B word select	Fixed to 01
R–Divider	R0..R9, Reference divider values 4 to 1023 allowed for divider ration.
Charge pump current Ratio	CP0: Charge pump current ratio, see table of charge pump currents.
Lock detect output	L0 0 Main lock detect signal present at the LOCK pin (push/pull). 1 Main lock detect signal present at the LOCK pin (open drain). When main loop is in power down mode, the lock indicator is low.
Power down	Main=1: power to N–divider, reference divider, main charge pumps, Main=0 to power down.
Fractional Compensation	FC7..0 Fractional Compensation charge pump current DAC, values 0 to 255. Recommended values: FC=80 for MOD 8; FC=128 for MOD 5.

Table 4 D word, length 24 bits

ADDRESS			SYNTHESIZER TEST BITS																			
1	1	0																				

Charge pump currents

CP0	I_{PHP}	I_{PHP-SU}
0	3xIset	15xIset
1	1xIset	5xIset

NOTES

1. $I_{SET}=^{Vset}/_{Rset}$: bias current for charge pumps.
2. I_{PHP_SU} is the total current at pin PHP during speed up condition.

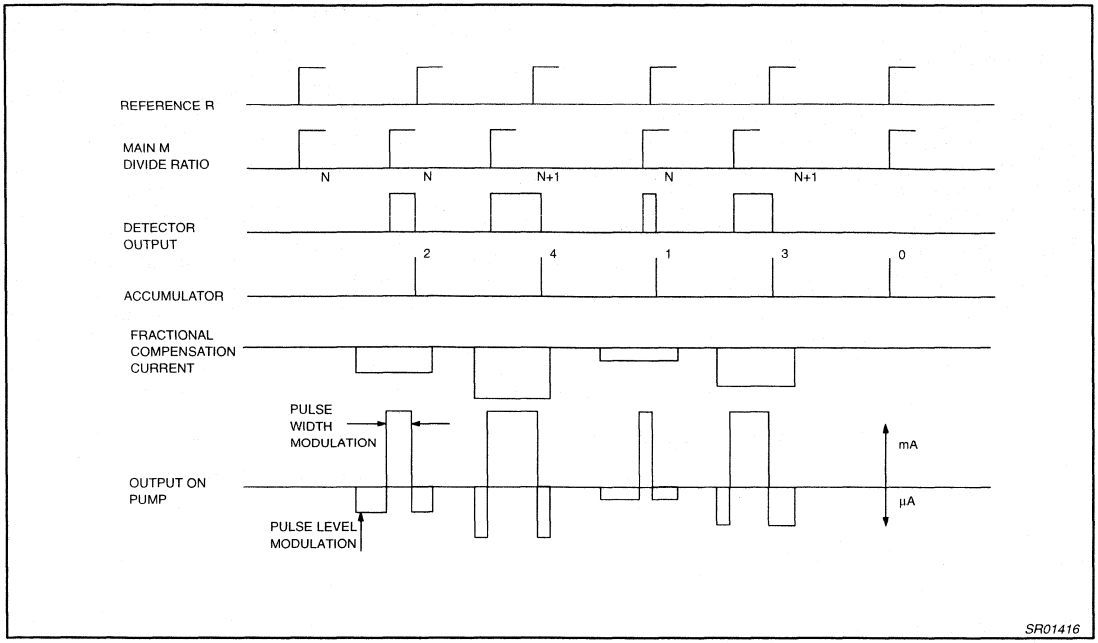


Figure 5. Waveforms for NF=2, Fraction=0.4

Fig 5. shows that for a proper fractional compensation, the area of the fractional compensation current pulse must be equal to the area of the charge pump ripple output.

1GHz low-voltage Fractional-N synthesizer SA7025

DESCRIPTION

The SA7025 is a monolithic low power, high performance dual frequency synthesizer fabricated in QUBiC BiCMOS technology. Featuring Fractional-N division with selectable modulo 5 or 8 implemented in the Main synthesizer to allow the phase detector comparison frequency to be five or eight times the channel spacing. This feature reduces the overall division ratio yielding a lower noise floor and faster channel switching. The phase detectors and charge pumps are designed to achieve phase detector comparison frequencies up to 5MHz. A triple modulus prescaler (divide by 64/65/72) is integrated on chip with a maximum input frequency of 1.04GHz. Programming and channel selection are realized by a high speed 3-wire serial interface.

FEATURES

- Operation up to 1.04GHz
- Fast locking by "Fractional-N" divider
- Auxiliary synthesizer
- Digital phase comparator with proportional and integral charge pump output
- High speed serial input
- Low power consumption
- Programmable charge pump currents
- Supply voltage range 2.7 to 5.5V
- Excellent input sensitivity: V_{RF_IN} = –20dBm

APPLICATIONS

- NADC (North American Digital Cellular)
- PDC (Personal Digital Cellular)
- Cellular radio
- Spread-spectrum receivers

PIN CONFIGURATION

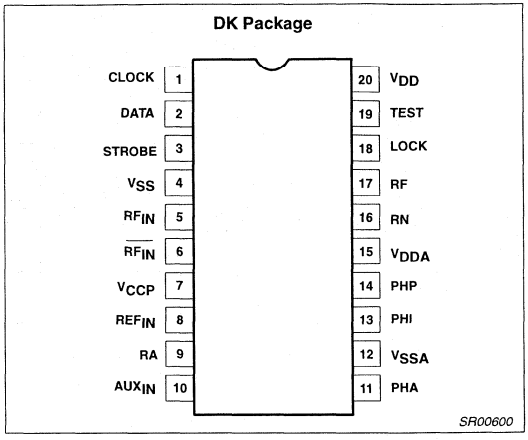


Figure 1. Pin Configuration

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Shrink Small Outline Package (SSOP)	–40 to +85°C	SA7025DK	SOT266-1

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V	Supply voltage, V_{DD}, V_{DDA}, V_{CCP}	-0.3 to +6.0	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{DD} + 0.3)	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range	-40 to +85	°C

NOTE: Thermal impedance (θ_{JA}) = 117°C/W. This device is ESD sensitive.

PIN DESCRIPTIONS

Symbol	Pin	Description
CLOCK	1	Serial clock input
DATA	2	Serial data input
STROBE	3	Serial strobe input
V_{SS}	4	Digital ground
RF_{IN}	5	Prescaler positive input
$\overline{RF_{IN}}$	6	Prescaler negative input
V_{CCP}	7	Prescaler positive supply voltage. This pin supplies power to the prescaler and RF input buffer
REF_{IN}	8	Reference divider input
RA	9	Auxiliary current setting; resistor to V_{SSA}
AUX_{IN}	10	Auxiliary divider input
PHA	11	Auxiliary phase detector output
V_{SSA}	12	Analog ground
PHI	13	Integral phase detector output
PHP	14	Proportional phase detector output
V_{DDA}	15	Analog supply voltage. This pin supplies power to the charge pumps, Auxiliary prescaler, Auxiliary and Reference buffers.
RN	16	Main current setting; resistor to V_{SSA}
RF	17	Fractional compensation current setting; resistor to V_{SSA}
LOCK	18	Lock detector output
TEST	19	Test pin; connect to V_{DD}
V_{DD}	20	Digital supply voltage. This pin supplies power to the CMOS digital part of the device

BLOCK DIAGRAM

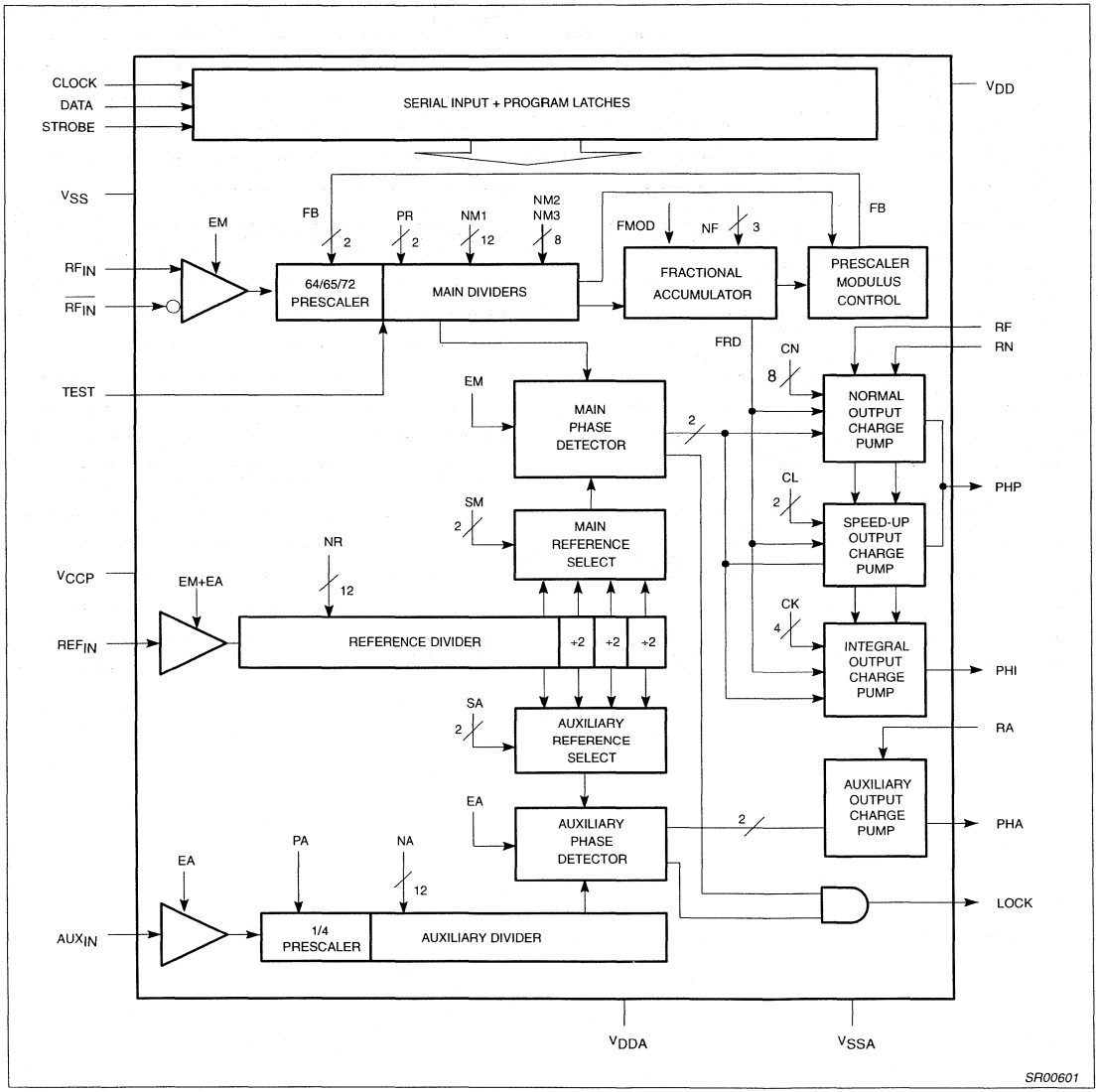


Figure 2. Block Diagram

DC ELECTRICAL CHARACTERISTICS

$V_{DD} = V_{DDA} = V_{CCP} = 3V$; $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{SUPPLY}	Recommended operating conditions	$V_{CCP} = V_{DD}$, $V_{DDA} \geq V_{DD}$	2.7		5.5	V
$I_{STANDBY}$	Total standby supply currents	EM = EA = 0, $I_{RN} = I_{RF} = I_{RA} = 0$		50	500	µA
Operational supply currents: $I = I_{DD} + I_{CCP} + I_{DDA}$; $I_{RN} = 25µA$, $I_{RA} = 25µA$, (see Note 5)						
I_{AUX}	Operational supply currents	EM = 0, EA = 1		3.5		mA
I_{MAIN}	Operational supply currents	EM = 1, EA = 0		5.5		mA
I_{TOTAL}	Operational supply currents	EM = EA = 1		7.5		mA
Digital inputs CLK, DATA, STROBE						
V_{IH}	High level input voltage range		$0.7xV_{DD}$		V_{DD}	V
V_{IL}	Low level input voltage range		0		$0.3xV_{DD}$	V
Digital outputs LOCK						
V_{OL}	Output voltage LOW	$I_O = 2mA$			0.4	V
V_{OH}	Output voltage HIGH	$I_O = -2mA$	$V_{DD}-0.4$			V
Charge pumps: $V_{DDA} = 3V$ / $I_{RX} = 25µA$ or $V_{DDA} = 5V$ / $I_{RX} = 62.5µA$, V_{PHX} in range, unless otherwise specified. (See Note 16)						
$\|I_{RX}\|$	Setting current range for any setting resistor	$2.7V < V_{DDA} < 5.5V$		25		µA
		$4.5V < V_{DDA} < 5.5V$		62.5		
V_{PHOUT}	Output voltage range		0.7		$V_{DDA}-0.8$	V
Charge pump PHA						
$\|I_{PHA}\|$	Output current PHA	$I_{RA} = -62.5µA$; $V_{PHA} = V_{DDA}/2$ [13]	400	500	600	µA
		$I_{RA} = -25µA$; $V_{PHA} = V_{DDA}/2$	160	200	240	
$\frac{\Delta I_{PHP\_A}}{\|I_{PHP\_A}\|}$	Relative output current variation PHA	$I_{RA} = -62.5µA$ [2, 13]		2	6	%
ΔI_{PHA_M}	Output current matching PHA pump	$V_{DDA} = 3V$, $I_{RA} = 25µA$			±50	µA
		$V_{DDA} = 5V$, $I_{RA} = 62.5µA$			±65	
Charge pump PHP, normal mode [1, 4, 6] $V_{RF} = V_{DDA}$						
$\|I_{PHP\_N}\|$	Output current PHP	$I_{RN} = -62.5µA$; $V_{PHP} = V_{DDA}/2$ [13]	440	550	660	µA
		$I_{RN} = -25µA$; $V_{PHP} = V_{DDA}/2$	175	220	265	
$\frac{\Delta I_{PHP\_N}}{I_{PHP\_N}}$	Relative output current variation PHP	$I_{RN} = -62.5µA$ [2, 13]		2	6	%
$\Delta I_{PHP\_N\_M}$	Output current matching PHP normal mode	$V_{DDA} = 3V$, $I_{RA} = 25µA$			±50	µA
		$V_{DDA} = 5V$, $I_{RA} = 62.5µA$			±65	
Charge pump PHP, speed-up mode [1, 4, 7] $V_{RF} = V_{DDA}$						
$\|I_{PHP\_S}\|$	Output current PHP	$I_{RN} = -62.5µA$; $V_{PHP} = V_{DDA}/2$ [13]	2.20	2.75	3.30	mA
		$I_{RN} = -25µA$; $V_{PHP} = V_{DDA}/2$	0.85	1.1	1.35	
$\frac{\Delta I_{PHP\_S}}{I_{PHP\_S}}$	Relative output current variation PHP	$I_{RN} = -62.5µA$ [2, 13]		2	6	%
$\Delta I_{PHP\_S\_M}$	Output current matching PHP speed-up mode	$V_{DDA} = 3V$, $I_{RA} = 25µA$			±250	µA
		$V_{DDA} = 5V$, $I_{RA} = 62.5µA$			±300	
Charge pump PHI, speed-up mode [1, 4, 8] $V_{RF} = V_{DDA}$						
$\|I_{PHI}\|$	Output current PHI	$I_{RN} = -62.5µA$; $V_{PHI} = V_{DDA}/2$ [13]	4.4	5.5	6.6	mA
		$I_{RN} = -25µA$; $V_{PHI} = V_{DDA}/2$	1.75	2.2	2.65	
$\frac{\Delta I_{PHI}}{I_{PHI}}$	Relative output current variation PHI	$I_{RN} = -62.5µA$ [2, 13]		2	8	%
ΔI_{PHI_M}	Output current matching PHI pump	$V_{DDA} = 3V$, $I_{RA} = 25µA$			±500	µA
		$V_{DDA} = 5V$, $I_{RA} = 62.5µA$			±600	
Fractional compensation PHP, normal mode [1, 9] $V_{RN} = V_{DDA}$, $V_{PHP} = V_{DDA}/2$						
$I_{PHP\_F\_N}$	Fractional compensation output current PHP vs F_{RD} [3]	$I_{RF} = -62.5µA$; $F_{RD} = 1$ to 7 [13]	–625	–400	–250	nA
		$I_{RF} = -25µA$; $F_{RD} = 1$ to 7	–250	–180	–100	

DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Fractional compensation PHP, speed up mode [1, 10] $V_{PHP} = V_{DDA}$, $V_{RN} = V_{DDA}$						
$I_{PHP\_F\_S}$	Fractional compensation output current PHP vs F_{RD}[3]	$I_{RF} = -62.5\mu A; F_{RD} = 1$ to 7[13]	–3.35	–2.0	–1.1	µA
		$I_{RF} = -25\mu A; F_{RD} = 1$ to 7	–1.35	–1.0	–0.5	
	Pump leakage		–20		20	nA
Fractional compensation PHI, speed up mode [1, 11] $V_{PHP} = V_{DDA}/2$, $V_{RN} = V_{DDA}$						
I_{PHI_F}	Fractional compensation output current PHI vs F_{RD}[3]	$I_{RF} = -62.5\mu A; F_{RD} = 1$ to 7[13]	–5.4	–4.0	–2.6	µA
		$I_{RF} = -25\mu A; F_{RD} = 1$ to 7	–2.15	–1.6	–1.05	
Charge pump leakage currents, charge pump not active						
I_{PHP_L}	Output leakage current PHP; normal mode[1]	$V_{PHP} = 0.7$ to $V_{DDA} - 0.8$		0.1	10	nA
I_{PHI_L}	Output leakage current PHI; normal mode[1]	$V_{PHI} = 0.7$ to $V_{DDA} - 0.8$		0.1	10	nA
I_{PHA_L}	Output leakage current PHA	$V_{PHA} = 0.7$ to $V_{DDA} - 0.8$		0.1	10	nA

AC ELECTRICAL CHARACTERISTICS

$V_{DD} = V_{DDA} = V_{CCP} = 3V$; $T_A = 25°C$; $f_{RF\_IN} = 1GHz$, input level = –20dBm; unless otherwise specified. Test Circuit, Figure 4. The parameters listed below are tested using automatic test equipment to assure consistent electrical characteristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Main divider						
f_{RF_IN}	Input signal frequency	Direct coupled input[14]			1.04	GHz
		1000pF input coupling			1.04	
V_{RF_IN}	Input sensitivity	1040MHz	–20		0	dBm
Reference divider ($V_{DD} = V_{DDA} = 3V$ or $V_{DD} = 3V$ / $V_{DDA} = 5V$)						
f_{REF_IN}	Input signal frequency	$2.7 < V_{DD}$ and $V_{DDA} < 5.5V$			25	MHz
		$2.7 < V_{DD}$ and $V_{DDA} < 4.5V$			30	
V_{REF_IN}	Input signal range, AC coupled	$2.7 < V_{DD}$ and $V_{DDA} < 5.5V$	500			mV_{P-P}
		$2.7 < V_{DD}$ and $V_{DDA} < 4.5V$	300			
Z_{REF_IN}	Reference divider input impedance[15]			100		kΩ
				3		pF
Auxiliary divider						
f_{AUX_IN}	Input signal frequency		0		50	MHz
	PA = "0", prescaler enabled	$4.5V \le V_{DDA} \le 5.5V$	0		150	
	Input signal frequency		0		30	
	PA = "1", prescaler disabled	$4.5V \le V_{DDA} \le 5.5V$	0		40	
V_{AUX_IN}	Input signal range, AC coupled		200			mV_{P-P}
Z_{AUX_IN}	Auxiliary divider input impedance			100		kΩ
				3		pF
Serial interface[15]						
f_{CLOCK}	Clock frequency				10	MHz
t_{SU}	Set-up time: DATA to CLOCK, CLOCK to STROBE		30			ns
t_H	Hold time; CLOCK to DATA		30			ns
t_W	Pulse width; CLOCK		30			ns
	Pulse width; STROBE	B, C, D, E words	30			
In-Loop Performance[17] $V_{DDA} = 5V$, $V_{DD} = 2.7V$						
R_{MM}	Main loop residual FM	FVCO = 1030MHz		300	600	Hz

AC ELECTRICAL CHARACTERISTICS (continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
t_{SW}	Pulse width; STROBE	A word, PR = '01'	$\frac{1}{f_{VCO}} \cdot (NM2 \cdot 65) + t_W$			ns
		A word, PR = '10'	$\frac{1}{f_{VCO}} \cdot [(NM2 \cdot 65) + (NM3 + 1) \cdot 72] + t_W$			

NOTES:

1. When a serial input "A" word is programmed, the main charge pumps on PHP and PHI are in the "speed up mode" as long as STROBE = H. When this is not the case, the main charge pumps are in the "normal mode".
2. The relative output current variation is defined thus:
$$\frac{\Delta I_{OUT}}{I_{OUT}} = 2 \cdot \frac{(I_2 - I_1)}{|(I_2 + I_1)|}$$; with $V_1 = 0.7V$, $V_2 = V_{DDA} - 0.8V$ (see Figure 3).
3. F_{RD} is the value of the 3 bit fractional accumulator.
4. Monotonicity is guaranteed with $C_N = 0$ to 255.
5. Power supply current measured with $V_{DD} = V_{CCP} = 3V$, $V_{DDA} = 5V$, $f_{RF\ IN} = 915.99MHz$, XTAL at 21.36MHz, AUX at 85.92MHz (PA = '0'), Main comp frequency = 240kHz, Auxiliary comp frequency = 120kHz, CN = 160, CL = 0, CK = 0. Internal registers NM1 = 52, NM2 = 0, NM3 = 4, PR = '10', SM = '00', SA = '01', NA = 179, NF = 5, FMOD = 8, NR = 89, PA = 0, IRN = IRA = IRF = 25µA, lock condition, normal mode. Operational supply current = $I_{DDA} + I_{DD} + I_{CCP}$.
6. Specification condition: CN = 255
7. Specification conditions:
   1) CN = 255; CL = 1, or
   2) CN = 75; CL = 3
8. Typical output current $|I_{PHI}| = -I_{RN} \times CN \times 2^{(CL+1)} \times CK/32$:
   1) CN = 160; CL = 3; CK = 1, or
   2) CN = 160; CL = 2; CK = 2, or
   3) CN = 160; CL = 1; CK = 4, or
   4) CN = 160; CL = 0; CK = 8
9. Any RFD, CL = 1 for speed-up pump. The integral pump is intended for switching only and the fractional compensation is not guaranteed.
10. Specification conditions: F_{RD} = 1 to 7; CL = 1.
11. Specification conditions:
    1) F_{RD} = 1 to 7; CL = 1; CK = 2, or
    2) F_{RD} = 1 to 7; CL = 2; CK = 1.
12. The matching is defined by the sum of the P and the N pump for a given output voltage.
13. Limited analog supply voltage range 4.5 to 5.5V.
14. For f_{IN} < 50MHz, low frequency operation requires DC-coupling and a minimum input slew rate of 32V/µs.
15. Guaranteed by design.
16. Close in noise for the charge pumps is tested on a sample basis in a typical application in order to eliminate parts outside the normal distribution.
17. $F_{XTAL} = 14.4MHz$, $V_{XTAL} = 500mV_{P-P}$, comparison frequency = 200kHz, Loop bandwidth = 5kHz, Audio filter = 300Hz to 15kHz.

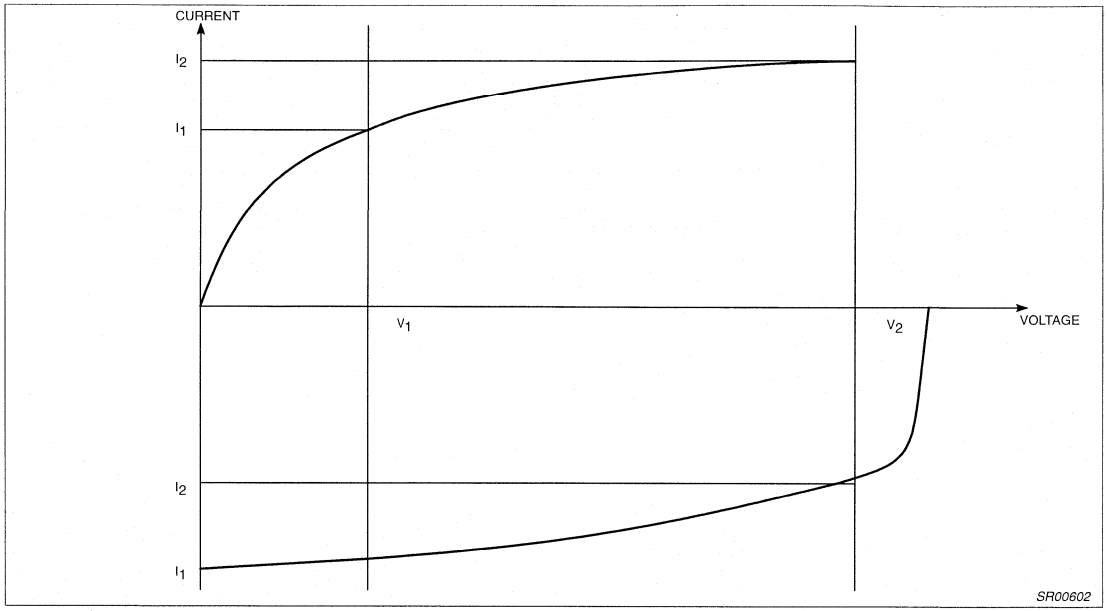


Figure 3. Relative Output Current Variation

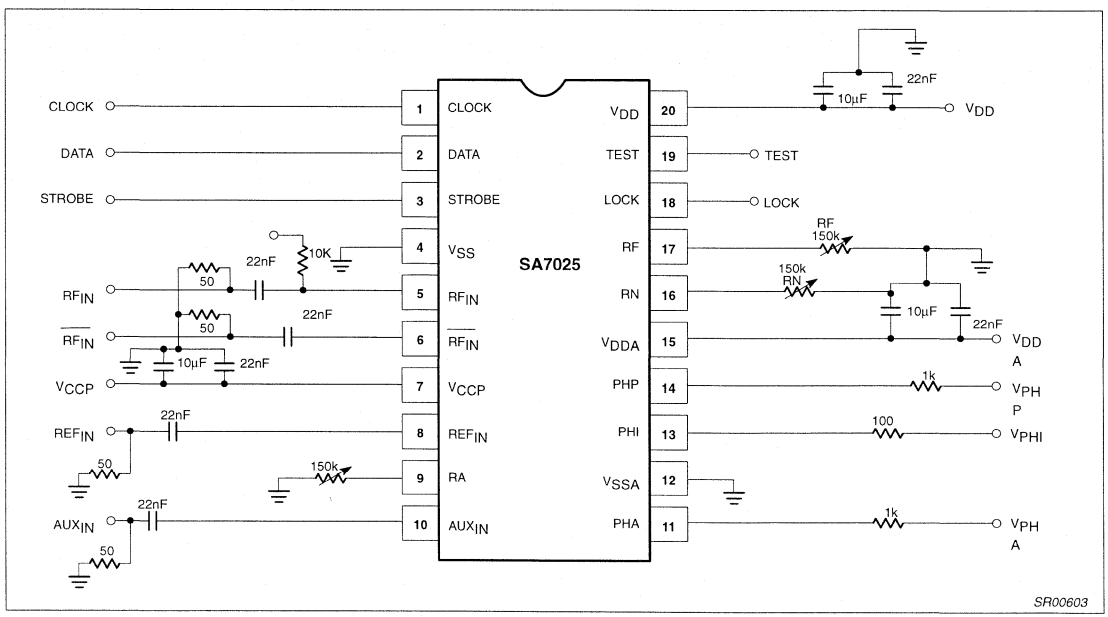


Figure 4. Test Circuit

AC TIMING CHARACTERISTICS

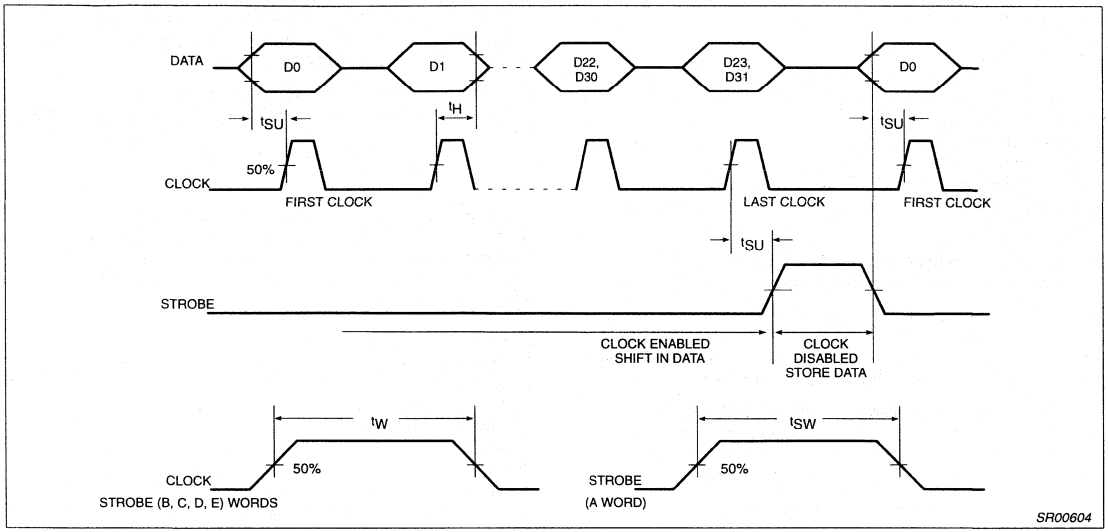


Figure 5. Serial Input Timing Sequence

FUNCTIONAL DESCRIPTION

Serial Input Programming

The serial input is a 3-wire input (CLOCK, STROBE, DATA) to program all counter ratios, DACs, selection and enable bits. The programming data is structured into 24 or 32 bit words; each word includes 1 or 4 address bits. Figure 5 shows the timing diagram of the serial input. When the STROBE = L, the clock driver is enabled and on the positive edges of the CLOCK the signal on DATA input is clocked into a shift register. When the STROBE = H, the clock is disabled and the data in the shift register remains stable. Depending on the 1 or 4 address bits the data is latched into different working registers or temporary registers. In order to fully program the synthesizer, 4 words must be sent: D, C, B and A. Figure 6 and Table 1 shows the format and the contents of each word. The E word is for testing purposes only. The E (test) word is reset when programming the D word. The data for CN and PR is stored by the B word in temporary registers. When the A word is loaded, the data of these temporary registers is loaded together with the A word into the work registers which avoids false temporary main divider input. CN is only loaded from the temporary registers when a short 24 bit A0 word is used. CN will be directly loaded by programming a long 32 bit A1 word. The flag LONG in the D word determines whether A0 (LONG = "0") or A1 (LONG = "1") format is applicable. The A word contains new data for the main divider.

Main Divider Synchronization

The A word is loaded only when a main divider synchronization signal is also active in order to avoid phase jumps when reprogramming the main divider. The synchronization signal is generated by the main divider. The signal is active while the NM1 divider is counting down from the programmed value. The new A word will be loaded after the NM1 divider has reached its terminal count; also, at this time a main divider output pulse will be sent to the main phase detector. The loading of the A word is disabled while the NM2 or NM3 dividers are counting up to their programmed values. Therefore, the new A word will be correctly loaded provided that the STROBE signal has been at an active high value for at least a minimum number of VCO input cycles at RF_{IN} or $\overline{RF_{IN}}$.

$$t\_strobe\_min = \frac{1}{f_{VCO}}(NM_2 \cdot 65) + t_W \text{ for PR = '01'}$$

$$t\_strobe\_min = \frac{1}{f_{VCO}}[NM_2 \cdot 65 + (NM_3 + 1) \cdot 72] + t_W \text{ for PR = '10'}$$

Programming the A word means also that the main charge pumps on output PHP and PHI are set into the speed-up mode as long as the STROBE is H.

Auxiliary Divider

The input signal on AUX_IN is amplified to logic level by a single-ended CMOS input buffer, which accepts low level AC coupled input signals. This input stage is enabled if the serial control bit EA = "1". Disabling means that all currents in the input stage are switched off. A fixed divide by 4 is enabled if PA = "0". This divider has been optimized to accept a high frequency input signal. If PA = "1", this divider is disabled and the input signal is fed directly to the second stage, which is a 12-bit programmable divider with standard input frequency (40MHz). The division ratio can be expressed as:

if PA = "0": N = 4 x NA

if PA = "1": N = NA; with NA = 4 to 4095

Reference Divider

The input signal on REF_IN is amplified to logic level by a single-ended CMOS input buffer, which accepts low level AC coupled input signals. This input stage is enabled by the OR function of the serial input bits EA and EM. Disabling means that all currents in the input stage are switched off. The reference divider consists of a programmable divider by NR (NR = 4 to 4095) followed by a three bit binary counter. The 2 bit SM register (see Figure 7) determines which of the 4 output pulses is selected as the main

phase detector input. The 2 bit SA register determines the selection of the auxiliary phase detector signal.

Main Divider

The differential inputs are amplified (to internal ECL logic levels) and provide excellent sensitivity (–20dBm at 1GHz) making the prescaler ideally suited to directly interface to a VCO as integrated on the SA620 RF gain stage, VCO and mixer device. The internal triple modulus prescaler feedback loop FB controls the selection of the divide by ratios 64/65/72, and reduces the minimum system division ratio below the typical value required by standard dual modulus (64/65) devices.

This input stage is enabled when serial control bit EM = "1". Disabling means that all currents in the prescaler are switched off.

The main divider is built up by a 12 bit counter plus a sign bit. Depending on the serial input values NM1, NM2, NM3, and the prescaler select PR, the counter will select a prescaler ratio during a number of input cycles according to Table 2 and Table 3.

The loading of the work registers NM1, NM2, NM3 and PR is synchronized with the state of the main counter, to avoid extra phase disturbance when switching over to another main divider ratio as explained in the Serial Input Programming section.

At the completion of a main divider cycle, a main divider output pulse is generated which will drive the main phase comparator. Also, the fractional accumulator is incremented with NF. The accumulator works modulo Q. Q is preset by the serial control bit FMOD to 8 when FMOD = "1". Each time the accumulator overflows, the feedback to the prescaler will select one cycle using prescaler ratio R2 instead of R1.

As shown above, this will increase the overall division ratio by 1 if R2 = R1 + 1. The mean division ratio over Q main divider will then be

$$NQ = N + \frac{NF}{Q}$$

Programming a fraction means the prescaler with main divider will divide by N or N + 1. The output of the main divider will be modulated with a fractional phase ripple. This phase ripple is proportional to the contents of the fractional accumulator FRD, which is used for fractional current compensation.

Phase Detectors

The auxiliary and main phase detectors are a two D-type flip-flop phase and frequency detector shown in Figure 8. The flip-flops are set by the negative edges of output signals of the dividers. The rising edge of the signal, L, will reset the flip-flops after both flip-flops have been set. Around zero phase error this has the effect of delaying the reset for 1 reference input cycle. This avoids non-linearity or deadband around zero phase error. The flip-flops drive on-chip charge pumps. A source current from the charge pump indicates the VCO frequency will be increased; a sink current indicates the VCO frequency will be decreased.

1.3GHz low voltage fractional–N dual synthesizer SA7026

FEATURES

- Low phase noise
- Fully programmable main and auxiliary dividers
- NORMAL & INTEGRAL charge pumps outputs
- Fast Locking Adaptive mode design
- Internal fractional spurious compensation
- Hardware and software power down

APPLICATIONS

- PCS
- Cellular phones
- Portable battery–powered radio equipment.

General description

The SA7026 BICMOS device integrates programmable dividers, charge pumps and a phase comparator to implement a phase–locked loop. The device is designed to operate from 3 NiCd cells, in pocket phones, with low current and nominal 3 V supplies.

The synthesizer operates at VCO input frequencies up to 1.3 GHz. The synthesizer has fully programmable main, auxiliary and reference dividers. All divider ratios are supplied via a 3–wire serial programming bus.

Separate power and ground pins are provided to the analog and digital circuits. The ground leads should be externally short–circuited to prevent large currents flowing across the die and thus causing damage. V_{DDA} should be equal to V_{DD}.

The charge pump current (gain) is fixed by an external resistance at pin RSET (pin). Only passive loop filters are used; the charge–pump operates within a wide voltage compliance range to provide a wider tuning range.

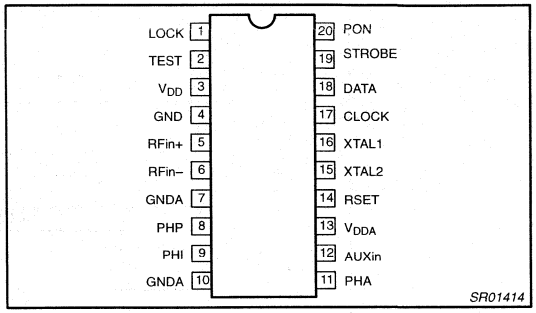


Figure 1. Pin Configuration

Quick reference data

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply voltage	V_{DD}	2.7	–	5.5	V
V_{DDA}	Analog supply voltage	$V_{DDA} = V_{DD}$	2.7	–	5.5	V
$I_{DDA}+I_{DD}$	Supply current	Main and aux. on	–	6.5	8.0	mA
$I_{DDA}+I_{DD}$	Total supply current in power–down mode		–	25	–	µA
f_{VCO}	Input frequency		500	–	1300	MHz
f_{AUX}	Input frequency		10	–	550	MHz
f_{XTAL}	Crystal reference input frequency		10	–	40	MHz
f_{PC}	Maximum phase comparator frequency		–		4	MHz
T_{amb}	Operating ambient temperature		–40	–	+85	°C

Ordering information

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SA7026DK	SSOP20	Plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266–1

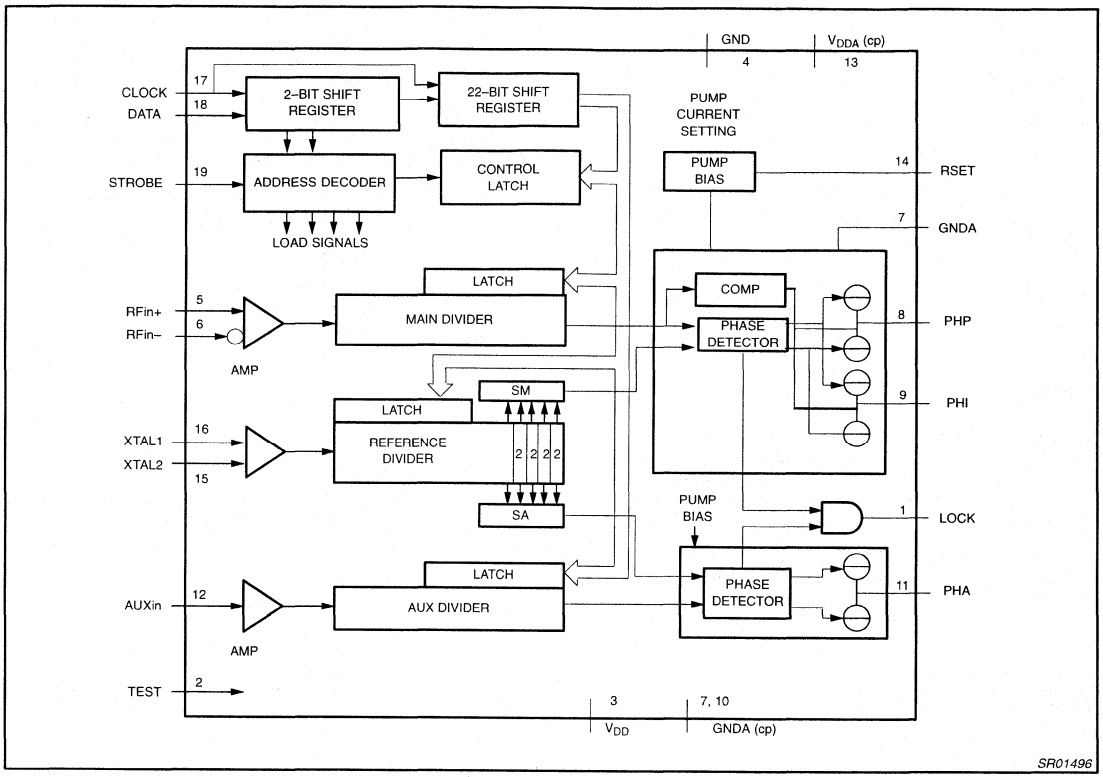


Figure 2. Block Diagram

PINNING

SYMBOL	PIN	DESCRIPTION
LOCK	1	Lock detect output
TEST	2	Test
V_{DD}	3	Digital supply
GND	4	Digital ground
RFin+	5	RF positive input to main divider
RFin–	6	RF negative input to main divider
GNDA	7	Charge pump ground
PHP	8	Main NORMAL chargepump
PHI	9	Main INTEGRAL chargepump
GNDA	10	Charge Pump Ground
PHA	11	Auxiliary chargepump output
AUXin	12	Input to auxiliary divider
V_{DDA}	13	Charge pump supply voltage
RSET	14	External resistor from this pin to ground sets the chargepump current
XTAL2	15	Reference input
XTAL1	16	Reference input
CLOCK	17	Programming bus clock input
DATA	18	Programming bus data input
STROBE	19	Programming bus enable input
PON	20	Power down control

FUNCTIONAL DESCRIPTION

Main Fractional–N divider

The RFin input (pins 5 and 6) drive a pre–amplifier to provide the clock to the first divider stage. For single ended operation, the signal should be fed to one of the inputs while the other one is AC grounded. The pre–amplifier has a high input impedance, dominated by pin and pad capacitance. The circuit operates with signal levels from –15dBm to +0dBm, and at frequencies as high as 1.3 GHz. The divider consists of a fully programmable bipolar prescaler followed by a CMOS counter. Divide ratios (512 to 65536) allow a minimum phase comparison frequency of 25kHz at 1.3 GHz RF.

At the completion of a main divider cycle, a main divider output pulse is generated which will drive the main phase comparator. Also, the fractional accumulator is incremented by the value of NF. The accumulator works with modulo Q set by FMOD. When the accumulator overflows the overall division ratio N will be increased by 1 to N + 1, the average division ratio over Q main divider cycles (either 5 or 8) will be

$$Nfrac \quad N \quad \frac{NF}{Q} \qquad (1)$$

The output of the main divider will be modulated with a fractional phase ripple. The phase ripple is proportional to the contents of the fractional accumulator and is nulled by the fractional compensation charge pump.

The reloading of a new programming word is synchronized to the state of the main divider to avoid introducing a phase disturbance.

Phase detector

The reference and main (aux) divider outputs are connected to a phase/frequency detector that controls the charge pump. The pump current is set by a an external resistor. The dead zone (caused by finite time taken to switch the current sources on or off) is cancelled by forcing the pumps ON for a minimum time at every cycle (backlash time) providing improved linearity.

Power–down mode

The power–down signal can be either hardware (PON) or software (PD). The PON signal exclusively ORed with the PD signal. If PON=0, then the part is powered up when PD=1. PON can be used to invert the polarity of the software bit PD. When the synthesizer is reactivated after the power–down the main and reference dividers are synchronized to avoid possibility of random phase errors on power–up.

Lock Detect

The output LOCK maintains a logic '1' when the auxiliary phase detector ANDed with the main phase detector indicates a lock condition. The lock condition for the main and auxiliary synthesizers is defined as a phase difference of less than ± 1 period of the frequency at the input XTAL1, 2. One counter can fulfill the lock condition when the other counter is powered down. Out of lock (logic '0' is indicated when both counters are powered down.

Reference divider

The reference divider consists of a divider with programmable values between 4 and 1023 followed by a three bit binary counter. The 3 bit SM (SA) register (see figure 5) determines which fo the 5 output pulses are selected as the main (auxiliary) phase detector input.

Auxiliary divider

The auxiliary divider consists of a divider with fully programmable values between 128 and 16384. The AUXin input, pin 13, drives a pre–amplifier to provide the clock to the first divider stage. The AUXin negative input is internally connected to ground. The pre–amplifier has a high input impedance, dominated by pin and pad capacitance. The circuit operates with signal levels from –15dBm to +0dBm, and at frequencies as high as 550 MHz. The divider consists of a fully programmable bipolar prescaler followed by a CMOS counter. The divide ratios allow a minimum phase comparison frequency of 25kHz at 550 MHz RF.

Serial programming bus

The serial input is a 3–wire input (CLOCK, STROBE, DATA) to program all counter divide ratios, fractional compensation DAC, selection and enable its. The programming data is structured into 24 bit words; each word includes 2 address bits. Figure 6 shows the timing diagram of the serial input. When the STROBE goes active HIGH, the clock is disabled and the data in the shift register remains unchanged. Depending on the 2 address bits the data is latched into different working registers or temporary registers. In order to fully program the synthesizer, 3 words must be sent: C, B, and A. Table 1

shows the format and the contents of each word. The D word is for testing purposes only. The data for the fractional compensation DAC, FC is stored by the B word in temporary registers. When the A word is loaded, the data of these temporary registers is loaded together with the main divider ratio.

Limiting values

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	Digital supply voltage	−0.3	+5.5	V
V_{DDA}	Analog supply voltage	−0.3	+5.5	V
$\Delta V_{DDA}–V_{DD}$	Difference in voltage between V_{DDA} and V_{DD}		±0.3	V
V_n	Voltage at pins 1, 2, 5, 6, 12, 15 to 20	−0.3	V_{DD} + 0.3	V
V_1	Voltage at pin 8, 9, 13	−0.3	V_{DDA} + 0.3	V
ΔV_{GND}	Difference in voltage between GNDA and GND (these pins should be connected together)	−0.3	+0.3	V
P_{tot}	Total power dissipation		TBD	mW
T_{stg}	Storage temperature	−55	+125	°C
T_{amb}	Operating ambient temperature	−30	+85	°C
T_j	Maximum junction temperature		TBD	°C

Handling

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

Thermal characteristics

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	Thermal resistance from junction to ambient in free air	120	K/W

Characteristics

$V_{DDA}=V_{DD}=3.0V$, $T_A=25^{\circ}C$; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply; pins 3, 13						
V_{DD}	Digital supply voltage		2.7	–	5.5	V
V_{DDA}	Analog supply voltage	$V_{DDA} = V_{DD}$	2.7	–	5.5	V
$I_{DDTotal}$	Synthesizer operational digital supply current	V_{DD} = 3.0 V	–	6.5	8.0	mA
$I_{standby}$	Total supply current in power–down mode	logic levels 0 or V_{DD}	–	25	TBD	µA
RFin main divider input; pins 5, 6						
f_{VCO}	VCO input frequency		500	–	1300	MHz
$V_{RFin(rms)}$	AC–coupled input signal level	R_s = 50 Ω; MAX. limit is indicative	–20	–	0	dBm
Z_{IRFin}	Input impedance (real part)	f_{VCO} = 2.0 GHz	–	TBD	–	kΩ
C_{IRFin}	Typical pin input capacitance	indicative, not tested	–	TBD	–	pF
N_m	Main divider ratio		512	–	65535	
f_{PCmax}	Maximum loop comparison frequency	indicative, not tested	–	–	4	MHz
AUX reference divider input; pins 12						
f_{AUXin}	Input frequency range		10	–	550	MHz
V_{AUXin}	AC–coupled input signal level	R_s=50Ω; MAX. limit is indicative	–15	–	0	dBm
Z_{AUXin}	Input impedance (real part)	f_{VCO}=500 MHZ	–	TBD	–	kΩ
C_{AUXin}	Typical pin input capacitance	indicative, not tested	–	TBD	–	pF
N_{AUX}	Auxiliary division ratio		128	–	16384	
Reference divider input; pins 15, 16						
f_{REFin}	Input frequency range from crystal		10	–	40	MHz
VRFin	AC–coupled input signal level	R_S=50Ω; MAX. limit is indicative	–5	–	+5	dBm
Z_{REFin}	Input impedance (real part)		–	TBD	–	kΩ
C_{REFin}	Typical pin input capacitance	indicative, not tested	–	TBD	–	pF
R_{REF}	Reference division ratio	SA=SM="000"	4	–	1023	
Charge pump current setting resistor input; pin 14						
R_{SET}	External resistor from pin 3 to ground		6	7.5	24	kΩ
V_{SET}	Regulated voltage at pin 3	R_{SET}=7.5 kΩ	–	1.23	–	V
Charge pump outputs (including fractional compensation pump); pins 8, 9, 11; R_{SET} =7.5 KΩ, FC=80						
Icp	Chargepump current ratio to Iset	CURRENT GAIN I_{PH}/I_{SET}	–15		+15	%
I_{MATCH}	Sink–to–source current matching	V_{ph}=1/2 V_{DDA}	–5		+5	%
I_{ZOUT}	Output current variation versus Vph^2	V_{ph} in compliance range	–10		+10	%
I_{LPH}	Charge pump off leakage current	V_{cp}=1/2 V_{CC}	–10	±1	+10	nA

V_{ph}	Charge pump voltage compliance		0.7	–	V_{DDA}–0.8	V
Phase noise						
C/N	Synthesizer's contribution to close–in–phase noise of 900 MHz RF signal at 1 kHz offset.	fref=19.44MHz; fcomp=80kHz indicative, not tested	–	–82	–	dBc/Hz
C/N	Synthesizer's contribution to close–in–phase noise of 1300 MHz RF signal at 1 kHz offset.	fref=19.44MHz; fcomp=240kHz indicative, not tested	–	–78	–	dBc/Hz
Interface logic input signal levels; pins 3, 15, 16, 18, 19, 20						
V_{IH}	HIGH level input voltage		0.7*V_{DD}	–	V_{DD}+0.3	V
V_{IL}	LOW level input voltage		–0.3	–	0.3*V_{DD}	V
I_{bias}	Input bias current	logic 1 or logic 0	–5	–	+5	µA
Lock detect output signal (in push/pull mode); pin 1						
V_{OL}	LOW level output voltage	I_{sink} = 2mA	–	–	0.4	V
V_{OH}	HIGH level output voltage	I_{source} = –2mA	V_{DD}–0.4	–	–	V

NOTES:

1. $I_{SET} = \frac{V_{SET}}{R_{SET}}$ bias current for charge pumps.

2. The relative output current variation is defined thus:

$\frac{\Delta I_{OUT}}{I_{OUT}}$ 2· $\frac{(I_2-I_1)}{|(I_2 \quad I_1)|}$; with V_1 0.7V, V_2 V_{DDA} –0.8V (See Figure 3.)

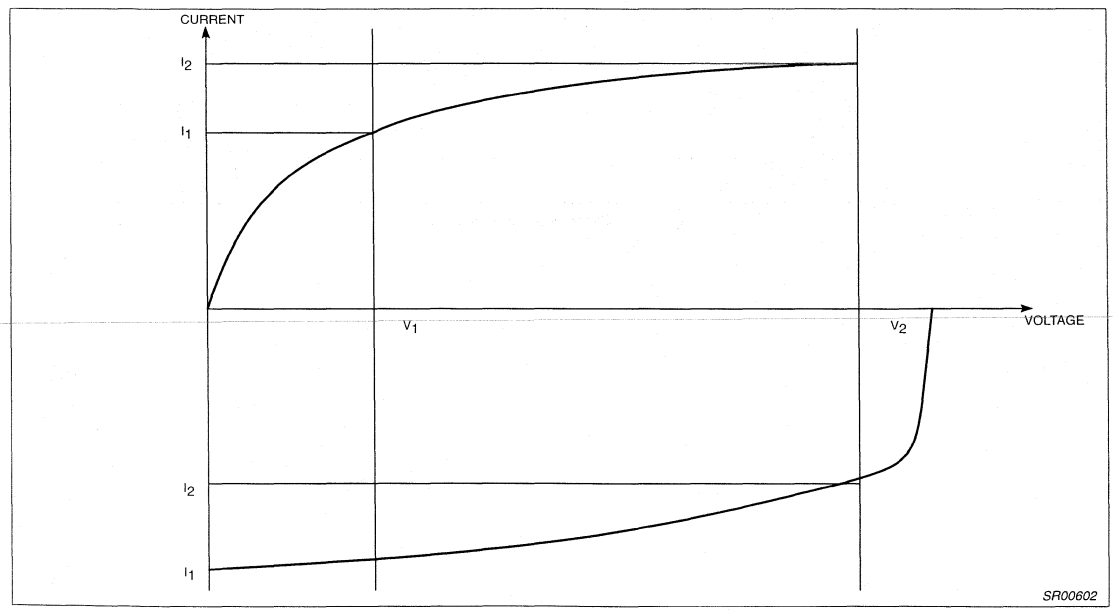


Figure 3. Relative Output Current Variation

Serial bus timing characteristics. See Figure 4.

V_{DD}= V_{DDA} =3.0V; T_{amb} = 25°C unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Serial programming clock; CLK					
t_r	Input rise time	–	10	40	ns
t_f	Input fall time	–	10	40	ns
T_{cy}	Clock period	100	–	–	ns
Enable programming; STROBE					
t_{START}	Delay to rising clock edge	40	–	–	ns
t_W	Minimum inactive pulse width	1/fcomp	–	–	ns
$T_{SU;\overline{E}}$	Enable set–up time to next clock edge	20	–	–	ns
Register serial input data; DATA					
$t_{SU;DAT}$	Input data to clock set–up time	20	–	–	ns
$t_{HD;DAT}$	Input data to clock hold time	20	–	–	ns

Application information

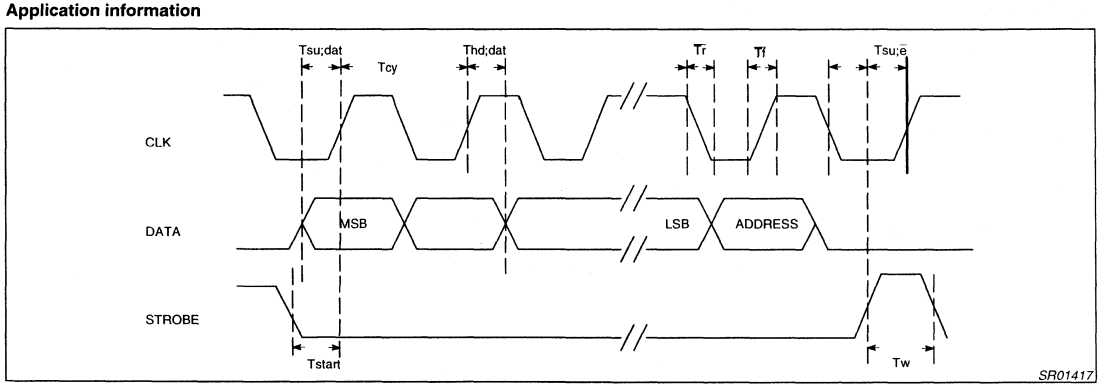


Figure 4. Serial Bus Timing Diagram

Main Output Charge Pumps and Fractional Compensation Currents.

The main charge pumps on pins PHP and PHI are driven by the main phase detector and the charge pump current values are determined by the current at pin RSET. The fractional compensation is derived from the current at RSET, the contents of the fractional accumulator FRD and by the program value of the FC DAC. The timing for the fractional compensation is derived form the main divider. See table of charge pump ratios.

Data format

Table 1 Format of programmed data

LAST IN		MSB	SERIAL PROGRAMMING FORMAT				FIRST IN LSB
p23	p22	p21	p20	../..	../..	p1	p0

Table 2 A word, length 24 bits

LAST IN					MSB														LSB	FIRST IN	
Address		fmod	Fractional–N			Main Divider ratio															Spare
0	0	FM	NF2	NF1	NF0	N15	N14	N13	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	N0	SK1	SK2
Default:		0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	1	0	0	0	0	0	0

A word select	Fixed to 00.
Fractional Modulus select	FM 0=modulo 8, 1=modulo 5.
Fractional–N Increment	NF2..0 Fractional N Increment values 000 to 111.
N–Divider	N0..N15, Main divider values 512 to 65535 allowed for divider ratio.

B word, length 24 bits

ADDRESS		REFERENCE DIVIDER										LOCK		PD		FRACTIONAL COMPENSATION DAC							
0	1	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	L1	L0	Main	Aux	FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0
Default:		0	0	0	1	0	1	0	0	0	1	0	0	1	1	0	1	0	1	0	0	0	0

B word select	Fixed to 01
R–Divider	R0..R9, Reference divider values 4 to 1023 allowed for divider ration.
Charge pump current Ratio	CP1, CP0: Charge pump current ratio, see table of charge pump currents.
Lock detect output	L1 L0 0 0 Combined main, aux. lock detect signal present at the LOCK pin (push/pull). 0 1 Combined main, aux, lock detect signal present at the LOCK pin (open drain). 1 0 Main lock detect signal present at the LOCK pin. 1 1 Auxiliary loop lock detect signal present at the LOCK pin. When auxiliary loop and main loop are in power down mode, the lock indicator is low.
Power down	Main=1: power to N–divider, reference divider, main charge pumps, Main=0 to power down. Aux=1: power to Aux divider, reference divider, aux charge pump, Aux=0 to power down.
Fractional Compensation	FC7..0 Fractional Compensation charge pump current DAC, values 0 to 255. Recommended values: FC=80 for MOD 8; FC=128 for MOD 5.

Table 3 C word, length 24 bits

Address		Auxiliary Divider														CP		SM			SA		
1	0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	CP1	CP0	SM2	SM1	SM0	SA2	SA1	SA0
Default		0	0	0	0	0	1	1	1	0	0	1	0	1	0	1	1	0	0	0	0	0	0

C word select	Fixed to 10
A–Divider	A0..A13, Auxiliary divider values 128 to 16384 allowed for divider ratio.
Charge pump current Ratio	CP1, CP0: Charge pump current ratio, see table fo charge pump currents.
Main comparison select	SM comparison divider select for main phase detector.
Aux comparison select	SA Comparison divider select for auxiliary phase detector.

Table 4 D word, length 24 bits

ADDRESS			SYNTHESIZER TEST BITS																		
1	1	0																			

Main and auxiliary chargepump currents

CP1	CP0	I_{PHA}	I_{PHP}	I_{PHP-SU}	I_{PHI}
0	0	1.5xIset	3xIset	15xIset	36xIset
0	1	0.5xIset	1xIset	5xIset	12xIset
1	0	1.5xIset	3xIset	15xIset	0
1	1	0.5xIset	1xIset	5xIset	0

NOTES
1. $I_{SET}={}^{Vset}/_{Rset}$: bias current for charge pumps.
2. CP1 is used to disable the PHI pump, I_{PHP_SU} is the total current at pin PHP during speed up condition.

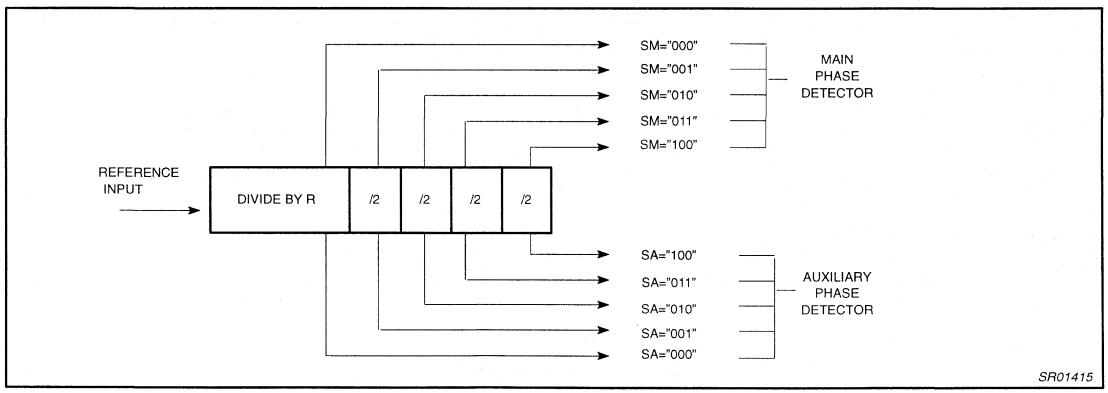


Figure 5. Reference Divider

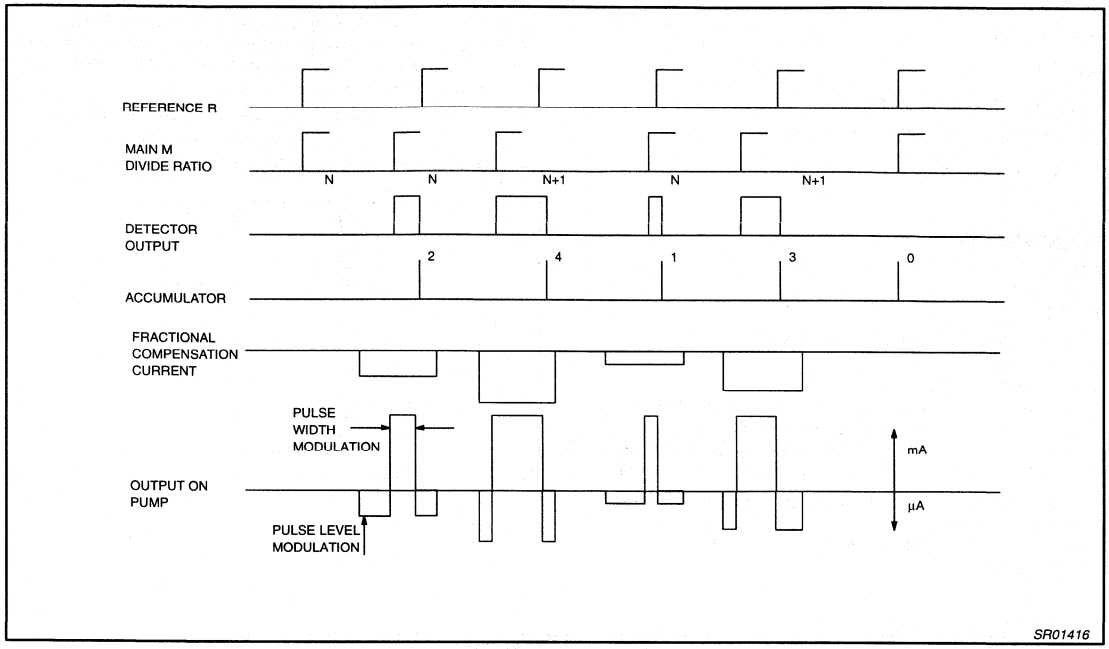


Figure 6. Waveforms for NF=2, Fraction=0.4

Fig 6. shows that for a proper fractional compensation, the area of the fractional compensation current pulse must be equal to the area of the charge pump ripple output.

2.5GHz low voltage fractional–N synthesizer SA8016

FEATURES

- Low phase noise
- Fully programmable main divider
- Internal fractional spurious compensation
- Hardware and software power down

APPLICATIONS

- PCS
- Cellular phones
- Portable battery–powered radio equipment.

General description

The SA8016 BICMOS device integrates programmable dividers, charge pumps and a phase comparator to implement a phase–locked loop. The device is designed to operate from 3 NiCd cells, in pocket phones, with low current and nominal 3 V supplies.

The synthesizer operates at VCO input frequencies up to 2.5 GHz. The synthesizer has fully programmable main and reference dividers. All divider ratios are supplied via a 3–wire serial programming bus.

Separate power and ground pins are provided to the analog and digital circuits. The ground leads should be externally short–circuited to prevent large currents flowing across the die and thus causing damage. V_{DDCP} should be equal to V_{DD} .

The charge pump current (gain) is fixed by an external resistance at pin RSET (pin). Only passive loop filters are used; the charge–pump operates within a wide voltage compliance range to provide a wider tuning range.

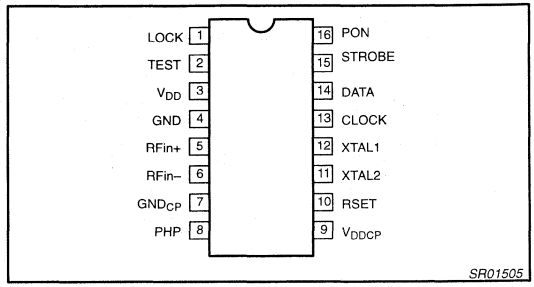


Figure 1. Pin Configuration

Quick reference data

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply voltage	V_{DD}	2.7	–	5.5	V
V_{DDCP}	Analog supply voltage	$V_{DDCP} = V_{DD}$	2.7	–	5.5	V
$I_{DDCP}+I_{DD}$	Supply current		–	6.5	8.0	mA
$I_{DDCP}+I_{DD}$	Total supply current in power–down mode		–	25	–	µA
f_{VCO}	Input frequency		800	–	2500	MHz
f_{XTAL}	Crystal reference input frequency		10	–	40	MHz
f_{PC}	Maximum phase comparator frequency		–		4	MHz
T_{amb}	Operating ambient temperature		–40	–	+85	°C

Ordering information

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SA8016	TSSOP16	Plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403–1

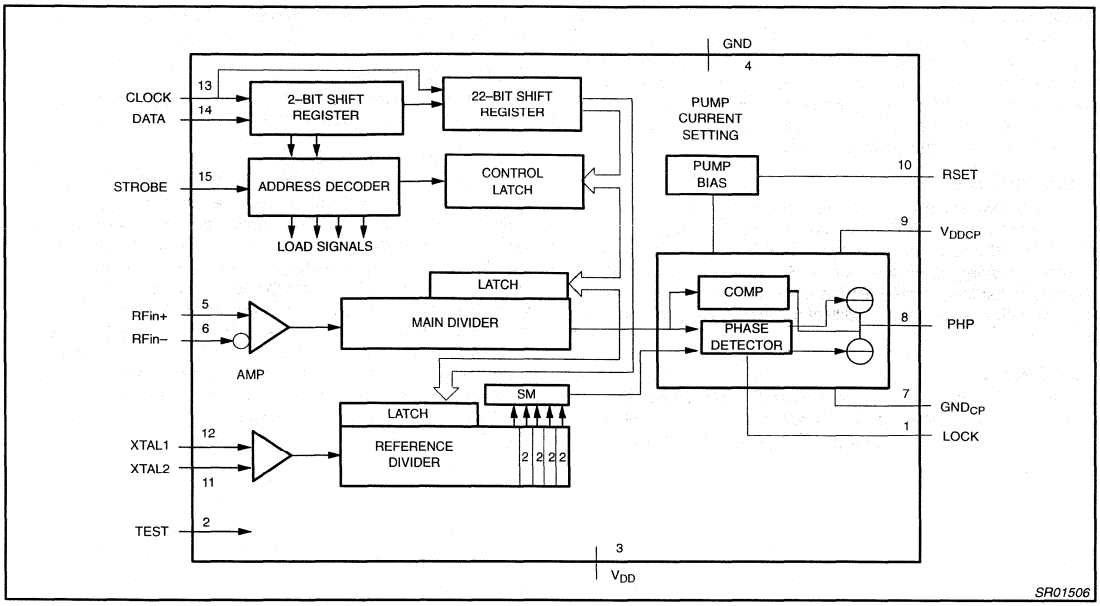


Figure 2. Block Diagram

PINNING

SYMBOL	PIN	DESCRIPTION
LOCK	1	Lock detect output
TEST	2	Test
V_{DD}	3	Digital supply
GND	4	Digital ground
RFin+	5	RF positive input to main divider
RFin–	6	RF negative input to main divider
GND_{CP}	7	Charge pump ground
PHP	8	Main NORMAL chargepump
V_{DDCP}	9	Charge pump supply voltage
RSET	10	External resistor from this pin to ground sets the chargepump current
XTAL2	11	Reference input
XTAL1	12	Reference input
CLOCK	13	Programming bus clock input
DATA	14	Programming bus data input
STROBE	15	Programming bus enable input
PON	16	Power down control

FUNCTIONAL DESCRIPTION

Main Fractional–N divider

The RFin input (pins 5 and 6) drive a pre–amplifier to provide the clock to the first divider stage. For single ended operation, the signal should be fed to one of the inputs while the other one is AC grounded. The pre–amplifier has a high input impedance, dominated by pin and pad capacitance. The circuit operates with signal levels from –15dBm to +0dBm, and at frequencies as high as 2.5 GHz. The divider consists of a fully programmable bipolar prescaler followed by a CMOS counter. Divide ratios (512 to 65536) allow a minimum phase comparison frequency of 25kHz at 2.5 GHz RF.

At the completion of a main divider cycle, a main divider output pulse is generated which will drive the main phase comparator. Also, the fractional accumulator is incremented by the value of NF. The accumulator works with modulo Q set by FMOD. When the accumulator overflows the overall division ratio N will be increased by 1 to N + 1, the average division ratio over Q main divider cycles (either 5 or 8) will be

$$Nfrac = N + \frac{NF}{Q} \quad (1)$$

The output of the main divider will be modulated with a fractional phase ripple. The phase ripple is proportional to the contents of the fractional accumulator and is nulled by the fractional compensation charge pump.

The reloading of a new programming word is synchronized to the state of the main divider to avoid introducing a phase disturbance.

Phase detector

The reference and main divider outputs are connected to a phase/frequency detector that controls the charge pump. The pump current is set by a an external resistor. The dead zone (caused by finite time taken to switch the current sources on or off) is cancelled by forcing the pumps ON for a minimum time at every cycle (backlash time) providing improved linearity.

Power–down mode

The power–down signal can be either hardware (PON) or software (PD). The PON signal exclusively ORed with the PD signal. If PON=0, then the part is powered up when PD=1. PON can be used to invert the polarity of the software bit PD. When the synthesizer is reactivated after the power–down the main and reference dividers are synchronized to avoid possibility of random phase errors on power–up.

Lock Detect

The output LOCK maintains a logic '1' when the phase detector indicates a lock condition. The lock condition is defined as a phase difference of less than ± 1 period of the frequency at the inputs XTAL1,2. Out of lock (logic '0') is indicated when the counter is powered down.

Reference divider

The reference divider consists of a divider with programmable values between 4 and 1023.

Serial programming bus

The serial input is a 3–wire input (CLOCK, STROBE, DATA) to program all counter divide ratios, fractional compensation DAC, selection and enable bits. Figure 5 shows the timing diagram of the serial input. When the STROBE goes active HIGH, the clock is disabled and the data in the shift register remains unchanged. Depending on the 2 address bits the data is latched into different working registers or temporary registers. In order to fully program the synthesizer, 2 words must be sent: B, and A. Table 1 shows the format and the contents of each word. The D word is for testing purposes only. The data for the fractional compensation DAC, FC is stored by the B word in temporary registers. When the A word is loaded, the data of these temporary registers is loaded together with the main divider ratio.

Limiting values

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	Digital supply voltage	–0.3	+5.5	V
V_{DDCP}	Analog supply voltage	–0.3	+5.5	V
$\Delta V_{DDCP}–V_{DD}$	Difference in voltage between V_{DDCP} and V_{DD}		±0.3	V
V_n	Voltage at pins 1, 2, 5, 6, 11 to 16	–0.3	V_{DD} + 0.3	V
V_1	Voltage at pin 8, 9	–0.3	V_{DDCP} + 0.3	V
ΔV_{GND}	Difference in voltage between GND_{CP} and GND (these pins should be connected together)	–0.3	+0.3	V
P_{tot}	Total power dissipation		TBD	mW
T_{stg}	Storage temperature	–55	+125	°C
T_{amb}	Operating ambient temperature	–30	+85	°C
T_j	Maximum junction temperature		TBD	°C

Handling

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

Thermal characteristics

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	Thermal resistance from junction to ambient in free air	120	K/W

Characteristics

V_{DDCP}=V_{DD}=3.0V, T_A=25°C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply; pins 3, 9						
V_{DD}	Digital supply voltage		2.7	–	5.5	V
V_{DDCP}	Analog supply voltage	V_{DDCP} = VDD	2.7	–	5.5	V
$I_{DDTotal}$	Synthesizer operational digital supply current	V_{DD} = 3.0 V	–	6.5	8	mA
$I_{standby}$	Total supply current in power–down mode	logic levels 0 or V_{DD}	–	25	TBD	µA
RFin main divider input; pins 5, 6						
f_{VCO}	VCO input frequency		800	–	2500	MHz
$V_{RFin(rms)}$	AC–coupled input signal level	R_s = 50 Ω; MAX. limit is indicative	–20	–	0	dBm
Z_{IRFin}	Input impedance (real part)	f_{VCO} = 2.0 GHz	–	TBD	–	kΩ
C_{IRFin}	Typical pin input capacitance	indicative, not tested	–	TBD	–	pF
N_m	Main divider ratio		512	–	65535	
f_{PCmax}	Maximum loop comparison frequency	indicative, not tested	–	–	4	MHz
Reference divider input; pins 11, 12						
f_{REFin}	Input frequency range from crystal		10	–	40	MHz
VRFin	AC–coupled input signal level	R_S=50Ω; MAX. limit is indicative	–5	–	+5	dBm
Z_{REFin}	Input impedance (real part)		–	TBD	–	kΩ
C_{REFin}	Typical pin input capacitance	indicative, not tested	–	TBD	–	pF
R_{REF}	Reference division ratio		4	–	1023	
Charge pump current setting resistor input; pin 10						
R_{SET}	External resistor from pin 3 to ground		6	7.5	24	kΩ
V_{SET}	Regulated voltage at pin 3	R_{SET}=7.5 kΩ	–	1.23	–	V
Charge pump outputs (including fractional compensation pump); pins 8; R_{SET} =7.5 KΩ, FC=80						
Icp	Charge pump current ratio to Iset	Current gain I_{PH}/I_{SET}	–15		+15	%
I_{MATCH}	Sink–to–source current matching	V_{ph}=1/2 VDD_{CP}	–5		+5	%
I_{ZOUT}	Output current variation versus Vph^2	V_{ph} in compliance range	–10		+10	%
I_{LPH}	Charge pump off leakage current	V_{cp}=1/2 V_{CC}	–10	±1	+10	nA
V_{ph}	Charge pump voltage compliance		0.7	–	V_{DDCP}–0.8	V
Phase noise						
C/N	Synthesizer's contribution to close–in–phase noise of 1800 MHz RF signal at 1 kHz offset.	fref=19.68MHz; fcomp=80kHz indicative, not tested	–	–78	–	dBc Hz
C/N	Synthesizer's contribution to close–in–phase noise of 2100 MHz RF signal at 1 kHz offset.	fref=19.44MHz; fcomp=240kHz indicative, not tested	–	–73	–	dBc Hz

Interface logic input signal levels; pins 3, 11, 12, 14, 15, 16						
V_{IH}	HIGH level input voltage		0.7*V_{DD}	–	V_{DD}+0.3	V
V_{IL}	LOW level input voltage		–0.3	–	0.3*V_{DD}	V
I_{bias}	Input bias current	logic 1 or logic 0	–5	–	+5	µA
Lock detect output signal (in push/pull mode); pin 1						
V_{OL}	LOW level output voltage	I_{sink} = 2mA	–	–	0.4	V
V_{OH}	HIGH level output voltage	I_{source} = –2mA	V_{DD}–0.4	–	–	V

NOTES:

1. $I_{SET} = \frac{V_{SET}}{R_{SET}}$ bias current for charge pumps.

2. The relative output current variation is defined thus:

$\frac{\Delta I_{OUT}}{I_{OUT}} = 2 \cdot \frac{(I_2 - I_1)}{|(I_2 + I_1)|}$; with V_1 = 0.7V, $V_2 = V_{DDCP}$ –0.8V (See Figure 3.)

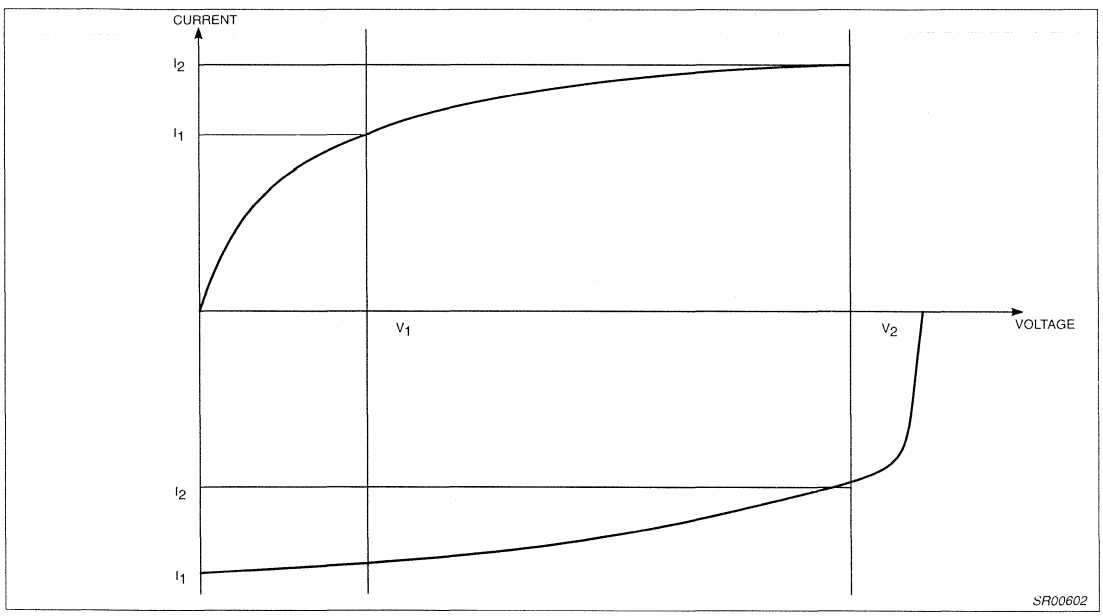


Figure 3. Relative Output Current Variation

Serial bus timing characteristics. See Figure 4.

V_{DD} = V_{DDCP} =3.0V; T_{amb} = 25°C unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Serial programming clock; CLK					
t_r	Input rise time	–	10	40	ns
t_f	Input fall time	–	10	40	ns
T_{cy}	Clock period	100	–	–	ns
Enable programming; STROBE					
t_{START}	Delay to rising clock edge	40	–	–	ns
t_W	Minimum inactive pulse width	1/fcomp	–	–	ns
$T_{SU;\overline{E}}$	Enable set–up time to next clock edge	20	–	–	ns
Register serial input data; DATA					
$t_{SU;DAT}$	Input data to clock set–up time	20	–	–	ns
$t_{HD;DAT}$	Input data to clock hold time	20	–	–	ns

Application information

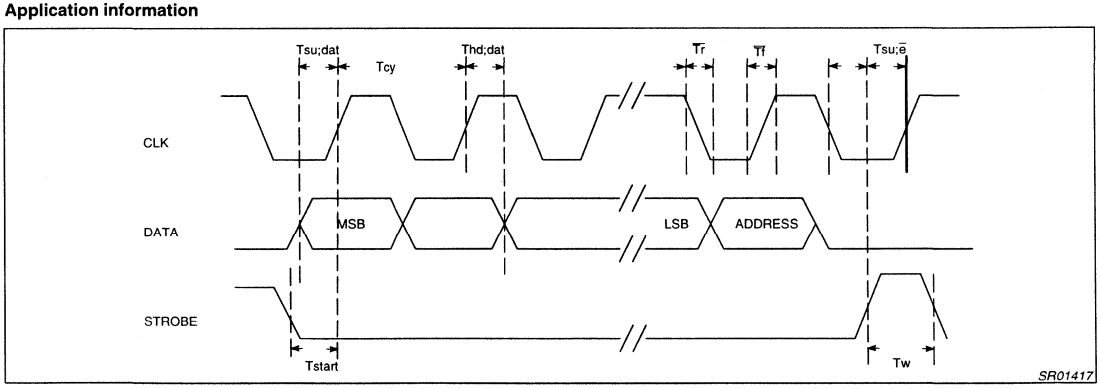


Figure 4. Serial Bus Timing Diagram

Main Output Charge Pump and Fractional Compensation Current.

The main charge pump on pin PHP is driven by the main phase detector; and the charge pump current values are determined by the current at pin RSET. The fractional compensation is derived from the current at RSET, the contents of the fractional accumulator FRD and by the program value of the FC DAC. The timing for the fractional compensation is derived form the main divider. See table of charge pump ratios.

Data format

Table 1 Format of programmed data

LAST IN		MSB	SERIAL PROGRAMMING FORMAT				FIRST IN LSB
p23	p22	p21	p20	../..	../..	p1	p0

Table 2 A word, length 24 bits

LAST IN					MSB														LSB	FIRST IN	
Address		fmod	Fractional–N		Main Divider ratio															Spare	
0	0	FM	NF2	NF1	NF0	N15	N14	N13	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	N0	SP1	SP2
Default:		0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	1	0	0	0	0	0	0

A word select	Fixed to 00.
Fractional Modulus select	FM 0=modulo 8, 1=modulo 5.
Fractional–N Increment	NF2..0 Fractional N Increment values 000 to 111.
N–Divider	N0..N15, Main divider values 512 to 65535 allowed for divider ratio.

B word, length 24 bits

ADDRESS		REFERENCE DIVIDER										LOCK	PD	CP	FRACTIONAL COMPENSATION DAC								SPARE
0	1	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	LO	MAIN	CP0	FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0	SP3
Default:		0	0	0	1	0	1	0	0	0	1	0	0	0	0	1	0	1	0	0	0	0	0

B word select	Fixed to 01
R–Divider	R0..R9, Reference divider values 4 to 1023 allowed for divider ration.
Charge pump current Ratio	CP0: Charge pump current ratio, see table of charge pump currents.
Lock detect output	L0 0 Main lock detect signal present at the LOCK pin (push/pull). 1 Main lock detect signal present at the LOCK pin (open drain). When main loop is in power down mode, the lock indicator is low.
Power down	Main=1: power to N–divider, reference divider, main charge pumps, Main=0 to power down.
Fractional Compensation	FC7..0 Fractional Compensation charge pump current DAC, values 0 to 255. Recommended values: FC=80 for MOD 8; FC=128 for MOD 5.

Table 4 D word, length 24 bits

ADDRESS			SYNTHESIZER TEST BITS																			
1	1	0																				

Charge pump currents

CP0	I_{PHP}	I_{PHP-SU}
0	3xIset	15xIset
1	1xIset	5xIset

NOTES

1. $I_{SET}=V_{set}/R_{set}$: bias current for charge pumps.
2. I_{PHP_SU} is the total current at pin PHP during speed up condition.

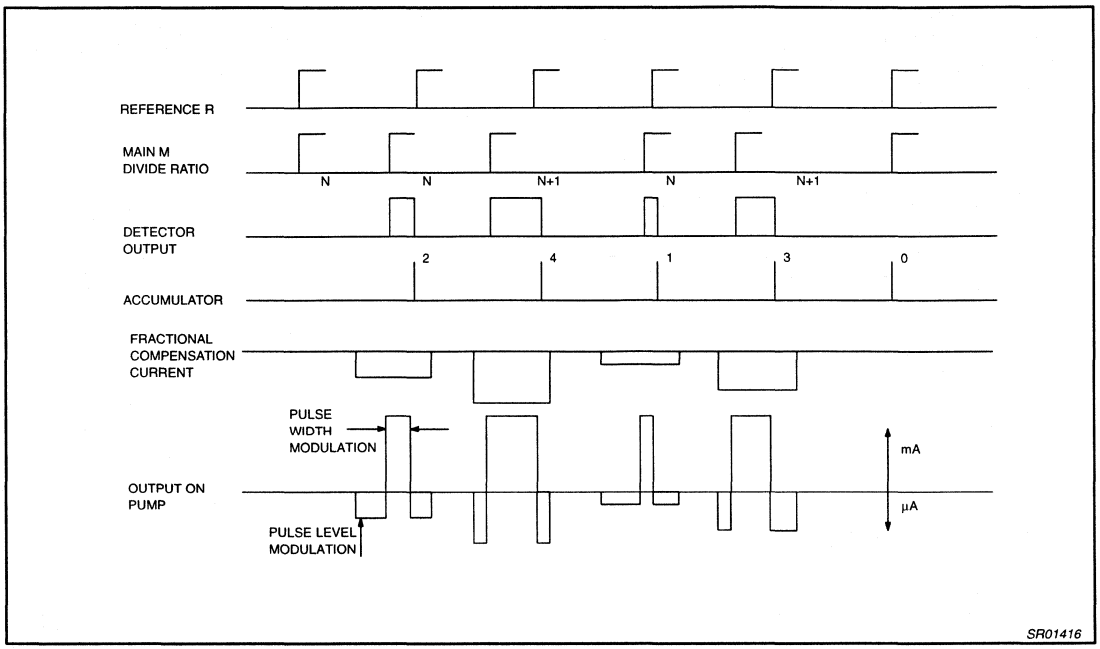


Figure 5. Waveforms for NF=2, Fraction=0.4

Fig 5. shows that for a proper fractional compensation, the area of the fractional compensation current pulse must be equal to the area of the charge pump ripple output.

1.8GHz low-voltage Fractional-N synthesizer SA8025A

DESCRIPTION

The SA8025A is a monolithic low power, high performance dual frequency synthesizer fabricated in QUBiC BiCMOS technology. The SA8025A is an improved version of the SA8025, suitable for narrow band systems like the Japan Personal Digital Cellular (PDC) system. The new design improves the performance of the fractional spur compensation circuitry. The new version is pin-for-pin compatible with the previous version. Featuring Fractional-N division with selectable modulo 5 or 8 implemented in the Main synthesizer to allow the phase detector comparison frequency to be five or eight times the channel spacing. This feature reduces the overall division ratio yielding a lower noise floor and faster channel switching. The phase detectors and charge pumps are designed to achieve phase detector comparison frequencies up to 5MHz. A four modulus prescaler (divide by 64/65/68/73) is integrated on chip with a maximum input frequency of 1.8GHz at 3V. Programming and channel selection are realized by a high speed 3-wire serial interface. A 1GHz version (SA7025DK) is also available with the same pinout.

FEATURES

- Operation up to 1.8GHz at 3V
- Fast locking by "Fractional-N" divider
- Auxiliary synthesizer
- Digital phase comparator with proportional and integral charge pump output
- High speed serial input
- Low power consumption
- Programmable charge pump currents

PIN CONFIGURATION

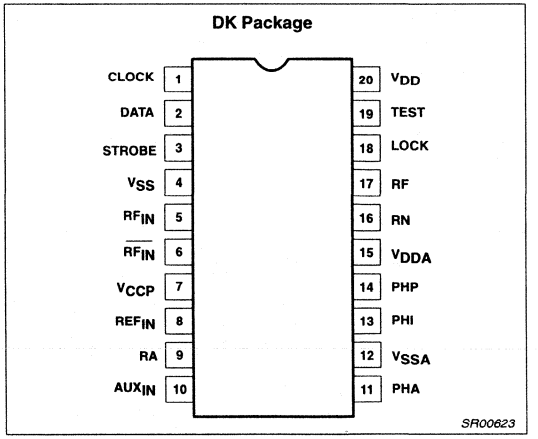


Figure 1. Pin Configuration

- Supply voltage range 2.7 to 5.5V
- Excellent input sensitivity: V_{RF_IN} = –20dBm

APPLICATIONS

- PHS (Personal Handy-phone System)
- PDC (Personal Digital Cellular)
- PCS (Personal Communication Service)
- Portable communication systems

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Shrink Small Outline Package (SSOP)	–40 to +85°C	SA8025ADK	SOT266-1

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V	Supply voltage, V_{DD}, V_{DDA}, V_{CCP}	-0.3 to +6.0	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{DD} + 0.3)	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range	-40 to +85	°C

NOTE: Thermal impedance (θ_{JA}) = 117°C/W. This device is ESD sensitive.

PIN DESCRIPTIONS

Symbol	Pin	Description
CLOCK	1	Serial clock input
DATA	2	Serial data input
STROBE	3	Serial strobe input
V_{SS}	4	Digital ground
RF_{IN}	5	Prescaler positive input
$\overline{RF_{IN}}$	6	Prescaler negative input
V_{CCP}	7	Prescaler positive supply voltage. This pin supplies power to the prescaler and RF input buffer
REF_{IN}	8	Reference divider input
RA	9	Auxiliary current setting; resistor to V_{SSA}
AUX_{IN}	10	Auxiliary divider input
PHA	11	Auxiliary phase detector output
V_{SSA}	12	Analog ground
PHI	13	Integral phase detector output
PHP	14	Proportional phase detector output
V_{DDA}	15	Analog supply voltage. This pin supplies power to the charge pumps, Auxiliary prescaler, Auxiliary and Reference buffers.
RN	16	Main current setting; resistor to V_{SSA}
RF	17	Fractional compensation current setting; resistor to V_{SSA}
LOCK	18	Lock detector output
TEST	19	Test pin; connect to V_{DD}
V_{DD}	20	Digital supply voltage. This pin supplies power to the CMOS digital part of the device

BLOCK DIAGRAM

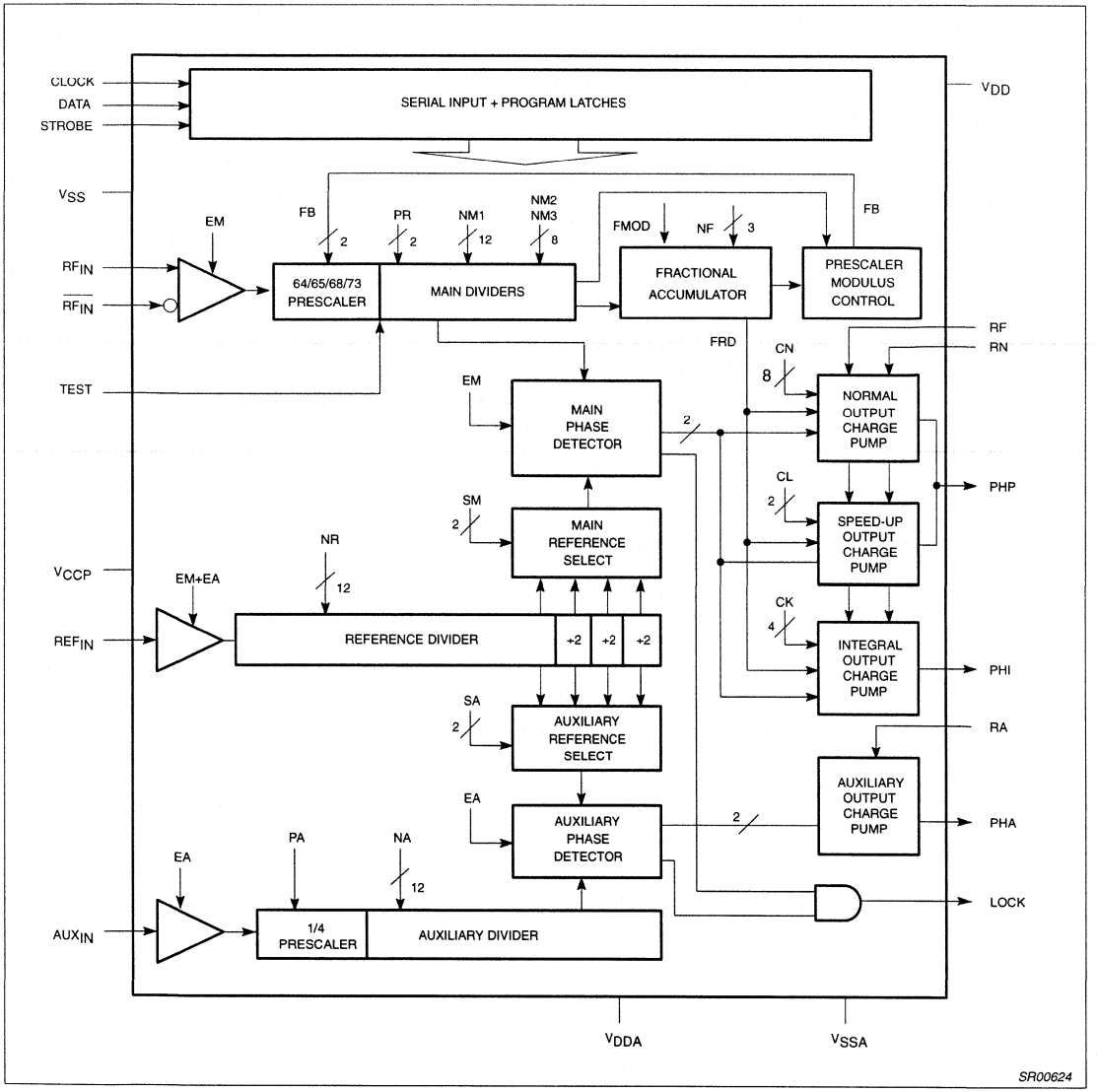


Figure 2. Block Diagram

DC ELECTRICAL CHARACTERISTICS

$V_{DD} = V_{DDA} = V_{CCP} = 3V$; $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{SUPPLY}	Recommended operating conditions	$V_{CCP} = V_{DD}$, $V_{DDA} \geq V_{DD}$	2.7		5.5	V
$I_{STANDBY}$	Total standby supply currents	EM = EA = 0, $I_{RN} = I_{RF} = I_{RA} = 0$		50	500	µA
Operational supply currents: $I = I_{DD} + I_{CCP} + I_{DDA}$; $I_{RN} = 25\mu A$, $I_{RA} = 25\mu A$, (see Note 5)						
I_{AUX}	Operational supply currents	EM = 0, EA = 1		3.5		mA
I_{MAIN}	Operational supply currents	EM = 1, EA = 0		11.0		mA
I_{TOTAL}	Operational supply currents	EM = EA = 1		13.5		mA
Digital inputs CLK, DATA, STROBE						
V_{IH}	High level input voltage range		$0.7xV_{DD}$		V_{DD}	V
V_{IL}	Low level input voltage range		0		$0.3xV_{DD}$	V
Digital outputs LOCK						
V_{OL}	Output voltage LOW	$I_O = 2mA$			0.4	V
V_{OH}	Output voltage HIGH	$I_O = -2mA$	$V_{DD}-0.4$			V
Charge pumps: $V_{DDA} = 3V$ / $I_{RX} = 25\mu A$ or $V_{DDA} = 5V$ / $I_{RX} = 62.5\mu A$, V_{PHX} in range, unless otherwise specified.						
$\lvert I_{RX} \rvert$	Setting current range for any setting resistor	$2.7V < V_{DDA} < 5.5V$		25		µA
		$4.5V < V_{DDA} < 5.5V$		62.5		
V_{PHOUT}	Output voltage range		0.7		$V_{DDA}-0.8$	V
Charge pump PHA						
$\lvert I_{PHA} \rvert$	Output current PHA	$I_{RN} = -62.5\mu A$; $V_{PHP} = V_{DDA}/2$ [13]	400	500	600	µA
		$I_{RN} = -25\mu A$; $V_{PHP} = V_{DDA}/2$	160	200	240	
$\frac{\Delta I_{PHP\_A}}{\lvert I_{PHP\_A} \rvert}$	Relative output current variation PHA	$I_{RA} = -62.5\mu A$ [2, 13]		2	6	%
ΔI_{PHA_M}	Output current matching PHA pump	$V_{DDA} = 3V$, $I_{RA} = 25\mu A$			±50	µA
		$V_{DDA} = 5V$, $I_{RA} = 62.5\mu A$			±65	
Charge pump PHP, normal mode [NO TAG, 4, 6] $V_{RF} = V_{DDA}$						
$\lvert I_{PHP\_N} \rvert$	Output current PHP	$I_{RN} = -62.5\mu A$; $V_{PHP} = V_{DDA}/2$ [13]	440	550	660	µA
		$I_{RN} = -25\mu A$; $V_{PHP} = V_{DDA}/2$	175	220	265	
$\frac{\Delta I_{PHP\_N}}{I_{PHP\_N}}$	Relative output current variation PHP	$I_{RN} = -62.5\mu A$ [2, 13]		2	6	%
$\Delta I_{PHP\_N\_M}$	Output current matching PHP normal mode	$V_{DDA} = 3V$, $I_{RA} = 25\mu A$			±50	µA
		$V_{DDA} = 5V$, $I_{RA} = 62.5\mu A$			±65	
Charge pump PHP, speed-up mode [NO TAG, 4, 7] $V_{RF} = V_{DDA}$						
$\lvert I_{PHP\_S} \rvert$	Output current PHP	$I_{RN} = -62.5\mu A$; $V_{PHP} = V_{DDA}/2$ [13]	2.20	2.75	3.30	mA
		$I_{RN} = -25\mu A$; $V_{PHP} = V_{DDA}/2$	0.85	1.1	1.35	
$\frac{\Delta I_{PHP\_S}}{I_{PHP\_S}}$	Relative output current variation PHP	$I_{RN} = -62.5\mu A$ [2, 13]		2	6	%
$\Delta I_{PHP\_S\_M}$	Output current matching PHP speed-up mode	$V_{DDA} = 3V$, $I_{RA} = 25\mu A$			±250	µA
		$V_{DDA} = 5V$, $I_{RA} = 62.5\mu A$			±300	
Charge pump PHI, speed-up mode [NO TAG, 4, 8] $V_{RF} = V_{DDA}$						
$\lvert I_{PHI} \rvert$	Output current PHI	$I_{RN} = -62.5\mu A$; $V_{PHI} = V_{DDA}/2$ [13]	4.4	5.5	6.6	mA
		$I_{RN} = -25\mu A$; $V_{PHI} = V_{DDA}/2$	1.75	2.2	2.65	
$\frac{\Delta I_{PHI}}{I_{PHI}}$	Relative output current variation PHI	$I_{RN} = -62.5\mu A$ [2, 13]		2	8	%
ΔI_{PHI_M}	Output current matching PHI pump	$V_{DDA} = 3V$, $I_{RA} = 25\mu A$			±500	µA
		$V_{DDA} = 5V$, $I_{RA} = 62.5\mu A$			±600	
Fractional compensation PHP, normal mode [NO TAG, 9] $V_{RN} = V_{DDA}$, $V_{PHP} = V_{DDA}/2$						
$I_{PHP\_F\_N}$	Fractional compensation output current PHP vs F_{RD} [3]	$I_{RF} = -62.5\mu A$; F_{RD} = 1 to 7 [13]	–625	–400	–250	nA
		$I_{RF} = -25\mu A$; F_{RD} = 1 to 7	–300	–180	–50	

DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Fractional compensation PHP, speed up mode [NO TAG, 10] **$V_{PHP} = V_{DDA}$, $V_{RN} = V_{DDA}$**						
$I_{PHP\_F\_S}$	Fractional compensation output current PHP vs F_{RD}[3]	I_{RF} = –62.5µA;F_{RD} = 1 to 7[13]	–3.35	–2	–1.1	µA
		I_{RF} = –25µA;F_{RD} = 1 to 7	–1.35	–1.0	–0.5	
	Pump leakage		–20		20	nA
Charge pump leakage currents, charge pump not active						
I_{PHP_L}	Output leakage current PHP; normal mode[NO TAG]	V_{PHP} = 0.7 to V_{DDA} – 0.8		0.1	20	nA
I_{PHI_L}	Output leakage current PHI; normal mode[NO TAG]	V_{PHI} = 0.7 to V_{DDA} – 0.8		0.1	20	nA
I_{PHA_L}	Output leakage current PHA	V_{PHA} = 0.7 to V_{DDA} – 0.8		0.1	20	nA

AC ELECTRICAL CHARACTERISTICS

$V_{DD} = V_{DDA} = V_{CCP}$ = 3V; T_A = 25°C; unless otherwise specified. Test Circuit, Figure 4. The parameters listed below are tested using automatic test equipment to assure consistent electrical characteristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Main divider guaranteed and tested on an automatic tester. Some performance parameters may be improved by using optimized layout.						
f_{RF_IN}	Input signal frequency	Pin = -20dBm, Direct coupled input[14]	0		1.8	GHz
		Pin = -20dBm, 1000pF input coupling			1.8	
V_{RF_IN}	Input sensitivity	f_{IN} = 1800MHz	–20		0	dBm
Reference divider ($V_{DD} = V_{DDA}$ = 3V or V_{DD} = 3V / V_{DDA} = 5V)						
f_{REF_IN}	Input signal frequency	2.7 < V_{DD} and V_{DDA} < 5.5V			25	MHz
		2.7 < V_{DD} and V_{DDA} < 4.5V			30	
V_{REF_IN}	Input signal range, AC coupled	2.7 < V_{DD} and V_{DDA} < 5.5V	500			mV_{P-P}
		2.7 < V_{DD} and V_{DDA} < 4.5V	300			
Z_{REF_IN}	Reference divider input impedance[15]			100		kΩ
				3		pF
Auxiliary divider						
f_{AUX_IN}	Input signal frequency		0		50	MHz
	PA = "0", prescaler enabled	4.5V ≤ V_{DDA} ≤ 5.5V	0		150	
	Input signal frequency		0		30	
	PA = "1", prescaler disabled	4.5V ≤ V_{DDA} ≤ 5.5V	0		40	
V_{AUX_IN}	Input signal range, AC coupled		200			mV_{P-P}
Z_{AUX_IN}	Auxiliary divider input impedance[15]			100		kΩ
				3		pF
Serial interface[15]						
f_{CLOCK}	Clock frequency				10	MHz
t_{SU}	Set-up time: DATA to CLOCK, CLOCK to STROBE		30			ns
t_H	Hold time; CLOCK to DATA		30			ns
t_W	Pulse width; CLOCK		30			ns
	Pulse width; STROBE	B, C, D, E words	30			
In-Loop Performance[16] **V_{DDA} = 5V, V_{DD} = 2.7V**						
RF_{MM}	Main loop residual FM	F_{VCO} = 1780MHz		600	900	Hz

AC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
t_{SW}	Pulse width; STROBE	A word, PR = '01'	$\frac{1}{f_{VCO}} \cdot (NM2 \cdot 65) + t_W$			ns
		A word, PR = '10'	$\frac{1}{f_{VCO}} \cdot [(NM2 \cdot 65) + (NM3 + 1) \cdot 68] + t_W$			
		A word, PR = '11'	$\frac{1}{f_{VCO}} \cdot [(NM2 \cdot 65 + (NM3 + 1) \cdot 68 + (NM4 + 1) \cdot 73)] + t_W$			
		A word, PR = '00'	$\frac{1}{f_{VCO}} \cdot [(NM2 \cdot 65) + (NM4 + 1) \cdot 73] + t_W$			

NOTES:

1. When a serial input "A" word is programmed, the main charge pumps on PHP and PHI are in the "speed up mode" as long as STROBE = H. When this is not the case, the main charge pumps are in the "normal mode".
2. The relative output current variation is defined thus:
$$\frac{\Delta I_{OUT}}{I_{OUT}} = 2 \cdot \frac{(I_2 - I_1)}{|(I_2 + I_1)|} \text{ with } V_1 = 0.7V,\ V_2 = V_{DDA} - 0.8V \text{ (see Figure 3).}$$
3. F_{RD} is the value of the 3 bit fractional accumulator.
4. Monotonicity is guaranteed with C_N = 0 to 255.
5. Power supply current measured with f_{RF_IN} = 1667.4MHz, NM1 = 0, NM2 = 1, NM3 = 1, NM4 = 4, FMOD = 8, N = 694 6/8, main phase detector frequency = 2.4MHz, $f_{REF\ IN}$ = 19.2MHz, NR = 8, SM = 1, f_{AUX_IN} = 150MHz, NA = 125, SA = 1, PA = 0, auxiliary phase detector frequency = 300kHz, IRN = IRA = IRF = 25µA, CN = 160, CL = 0, CK = 0, lock condition, normal mode, $V_{CCP} = V_{DD} = V_{DDA}$ = 3V. Operational supply current = $I_{DDA} + I_{DD} + I_{CCP}$.
6. Specification condition: CN = 255
7. Specification conditions:
   1) CN = 255; CL = 1, or
   2) CN = 75; CL = 3
8. Typical output current $|I_{PHI}| = -I_{RN} \times CN \times 2^{(CL+1)} \times CK/32$:
   1) CN = 160; CL = 3; CK = 1, or
   2) CN = 160; CL = 2; CK = 2, or
   3) CN = 160; CL = 1; CK = 4, or
   4) CN = 160; CL = 0; CK = 8
9. Any RFD, CL = 1 for speed-up pump. The integral pump is intended for switching only and the fractional compensation is not guaranteed.
10. Specification conditions: F_{RD} = 1 to 7; CL = 1.
11. Specification conditions:
    1) F_{RD} = 1 to 7; CL = 1; CK = 2, or
    2) F_{RD} = 1 to 7; CL = 2; CK = 1.
12. The matching is defined by the sum of the P and the N pump for a given output voltage.
13. Limited analog supply voltage range 4.5 to 5.5V.
14. For f_{IN} < 50MHz, low frequency operation requires DC-coupling and a minimum input slew rate of 32V/µs.
15. Guaranteed by design.
16. F_{XTAL} = 14.4MHz, V_{XTAL} = 500mV_{P-P}, comparison Freq. = 200kHz, Loop bandwidth = 5kHz, Audio filter = 300Hz to 15kHz.

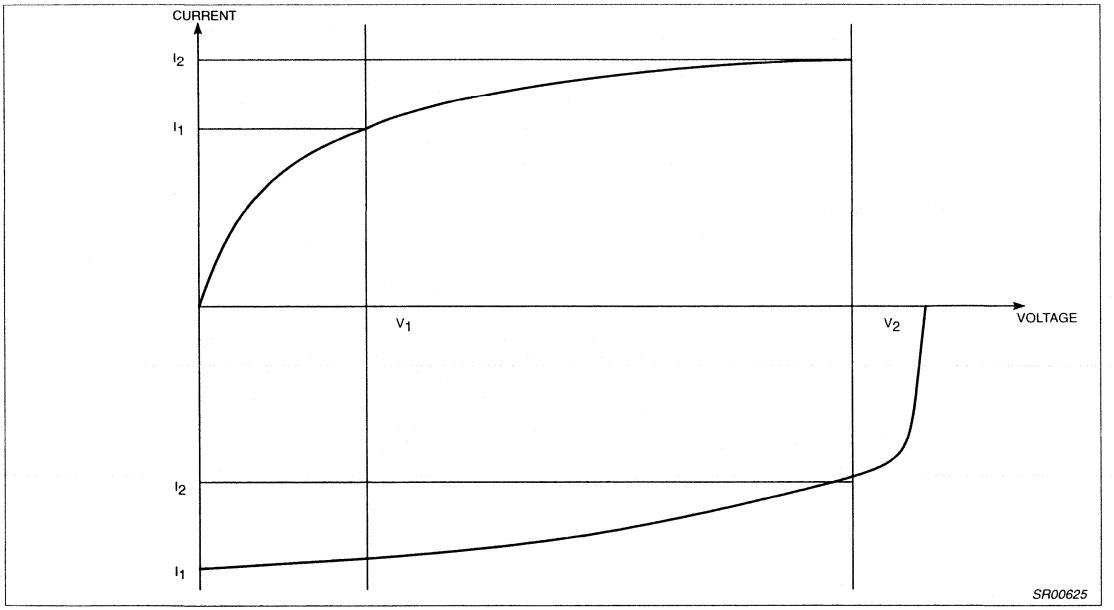


Figure 3. Relative Output Current Variation

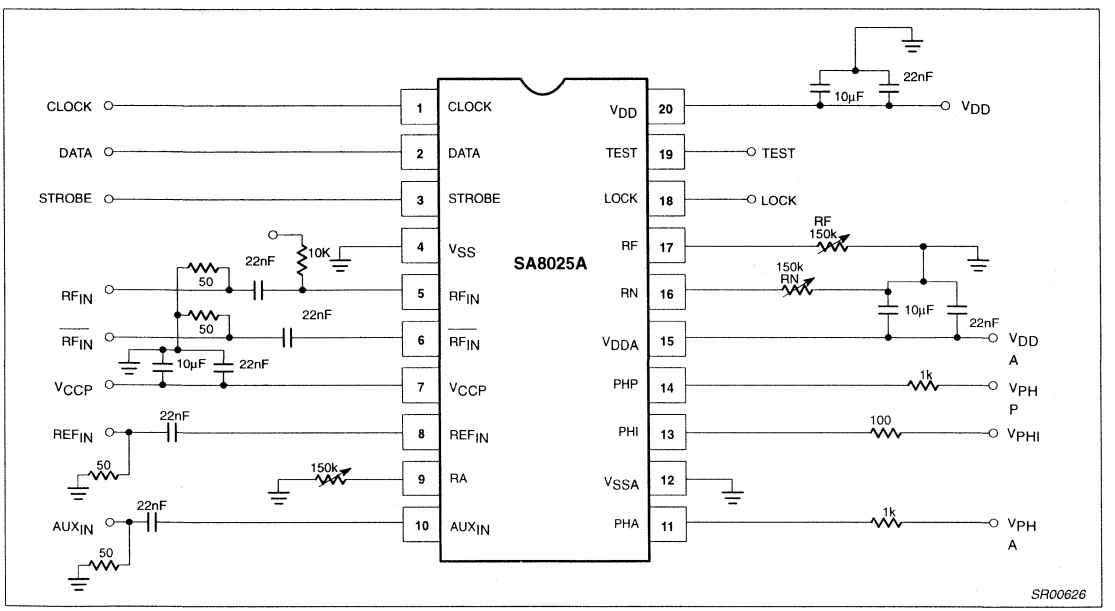


Figure 4. Test Circuit

AC TIMING CHARACTERISTICS

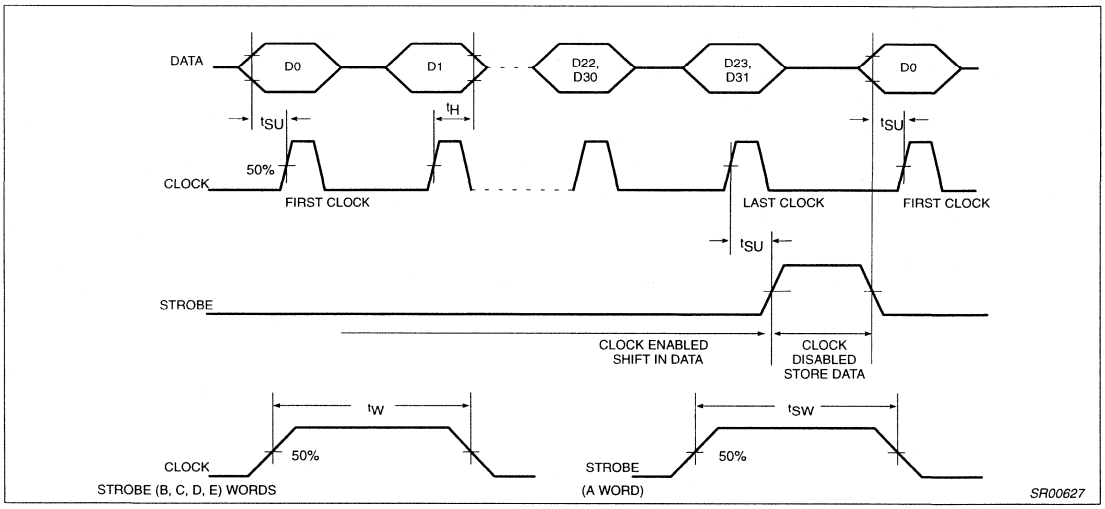


Figure 5. Serial Input Timing Sequence

FUNCTIONAL DESCRIPTION

Serial Input Programming

The serial input is a 3-wire input (CLOCK, STROBE, DATA) to program all counter ratios, DACs, selection and enable bits. The programming data is structured into 24 or 32 bit words; each word includes 1 or 4 address bits. Figure 5 shows the timing diagram of the serial input. When the STROBE = L, the clock driver is enabled and on the positive edges of the CLOCK the signal on DATA input is clocked into a shift register. When the STROBE = H, the clock is disabled and the data in the shift register remains stable. Depending on the 1 or 4 address bits the data is latched into different working registers or temporary registers. In order to fully program the synthesizer, 4 words must be sent: D, C, B and A. Figure 6 and Table 1 shows the format and the contents of each word. The E word is for testing purposes only. The E (test) word is reset when programming the D word. The data for CN and PR is stored by the B word in temporary registers. When the A word is loaded, the data of these temporary registers is loaded together with the A word into the work registers which avoids false temporary main divider input. CN is only loaded from the temporary registers when a short 24 bit A0 word is used. CN will be directly loaded by programming a long 32 bit A1 word. The flag LONG in the D word determines whether A0 (LONG = "0") or A1 (LONG = "1") format is applicable. The A word contains new data for the main divider.

Main Divider Synchronization

The A word is loaded only when a main divider synchronization signal is also active in order to avoid phase jumps when reprogramming the main divider. The synchronization signal is generated by the main divider. The signal is active while the NM1 divider is counting down from the programmed value. The new A word will be loaded after the NM1 divider has reached its terminal count; also, at this time a main divider output pulse will be sent to the main phase detector. The loading of the A word is disabled while the other dividers are counting up to their programmed values.

Therefore, the new A word will be correctly loaded provided that the STROBE signal has been at an active high value for at least a minimum number of VCO input cycles at RF_{IN} or $\overline{RF_{IN}}$.

For PR = '01'

$$t\_strobe\_min = \frac{1}{f_{VCO}}(NM2 \cdot 65) + t_W$$

For PR = '10'

$$t\_strobe\_min = \frac{1}{f_{VCO}}[NM2 \cdot 65 + (NM3 + 1) \cdot 68] + t_W$$

For PR = '11'

$$t\_strobe\_min = \frac{1}{f_{VCO}} \cdot [(NM2 \cdot 65 + (NM3 + 1) \; 68 + (NM4 + 1) \cdot 73)] + t_W$$

For PR = '00'

$$t\_strobe\_min = \frac{1}{f_{VCO}} \cdot [(NM2 \cdot 65) + (NM4 + 1) \cdot 73] + t_W$$

Programming the A word means also that the main charge pumps on output PHP and PHI are set into the speed-up mode as long as the STROBE is H.

Auxiliary Divider

The input signal on AUX_IN is amplified to logic level by a single-ended CMOS input buffer, which accepts low level AC coupled input signals. This input stage is enabled if the serial control bit EA = "1". Disabling means that all currents in the input stage are switched off. A fixed divide by 4 is enabled if PA = "0". This divider has been optimized to accept a high frequency input signal. If PA = "1", this divider is disabled and the input signal is fed directly to the second stage, which is a 12-bit programmable divider with standard input frequency (40MHz). The division ratio can be expressed as:

if PA = "0": N = 4 x NA

if PA = "1": N = NA; with NA = 4 to 4095

Reference Divider

The input signal on REF_IN is amplified to logic level by a single-ended CMOS input buffer, which accepts low level AC coupled input signals. This input stage is enabled by the OR function of the serial input bits EA and EM. Disabling means that all currents in the input stage are switched off. The reference divider consists of a programmable divider by NR (NR = 4 to 4095) followed by a three bit binary counter. The 2 bit SM register (see Figure 7) determines which of the 4 output pulses is selected as the main phase detector input. The 2 bit SA register determines the selection of the auxiliary phase detector signal.

Main Divider

The differential inputs are amplified (to internal ECL logic levels) and provide excellent sensitivity (–20dBm at 1.7GHz) making the prescaler ideally suited to directly interface to a VCO as integrated on the Philips front-end devices including RF gain stage, VCO and mixer. The internal four modulus prescaler feedback loop FB controls the selection of the divide by ratios 64/65/68/73, and reduces the minimum system division ratio below the typical value required by standard dual modulus (64/65) devices.

This input stage is enabled when serial control bit EM = "1". Disabling means that all currents in the prescaler are switched off.

The main divider is built up by a 12 bit counter plus a sign bit. Depending on the serial input values NM1, NM2, NM3, NM4 and the prescaler select PR, the counter will select a prescaler ratio during a number of input cycles according to Table 2 and Table 3.

The loading of the work registers NM1, NM2, NM3, NM4 and PR is synchronized with the state of the main counter, to avoid extra phase disturbance when switching over to another main divider ratio as explained in the Serial Input Programming section.

At the completion of a main divider cycle, a main divider output pulse is generated which will drive the main phase comparator. Also, the fractional accumulator is incremented with NF. The accumulator works modulo Q. Q is preset by the serial control bit FMOD to 8 when FMOD = "1". Each time the accumulator overflows, the feedback to the prescaler will select one cycle using prescaler ratio R2 instead of R1.

As shown above, this will increase the overall division ratio by 1 if R2 = R1 + 1. The mean division ratio over Q main divider will then be

$$NQ = N + \frac{NF}{Q}$$

Programming a fraction means the prescaler with main divider will divide by N or N + 1. The output of the main divider will be modulated with a fractional phase ripple. This phase ripple is proportional to the contents of the fractional accumulator FRD, which is used for fractional current compensation.

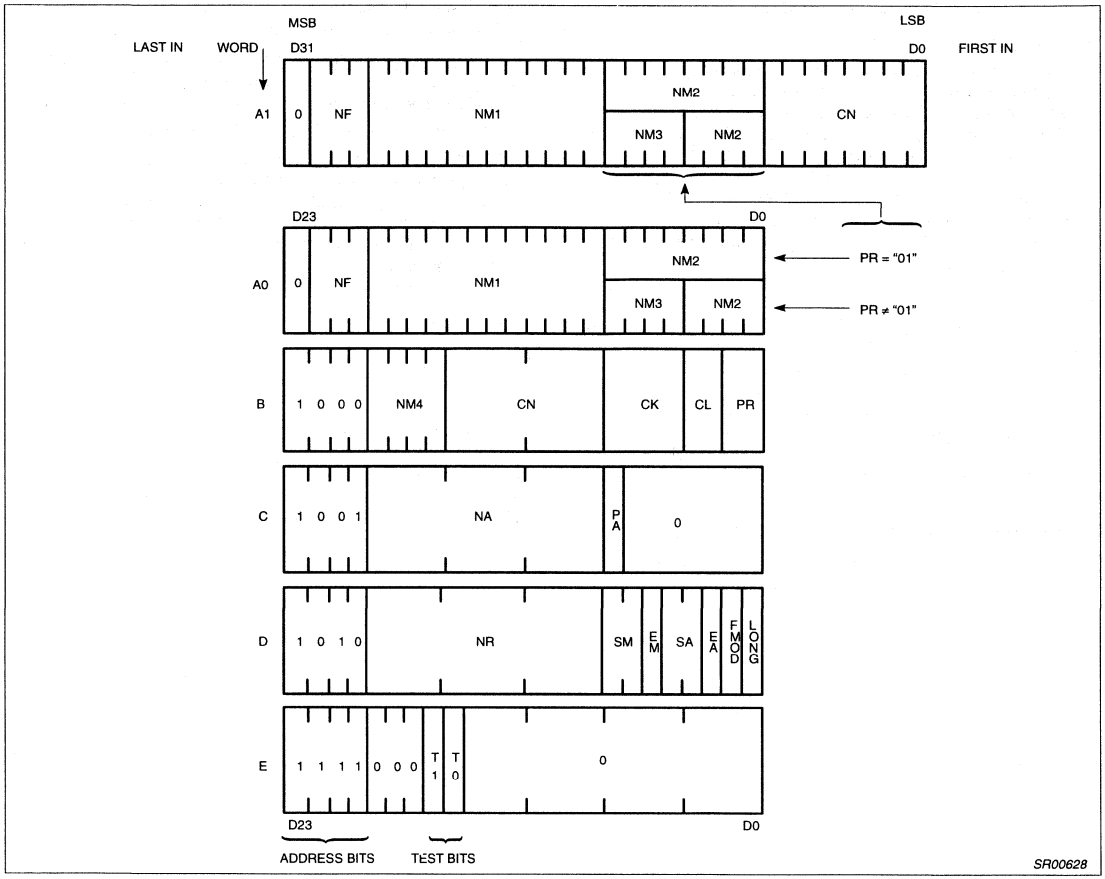


Figure 6. Serial Input Word Format

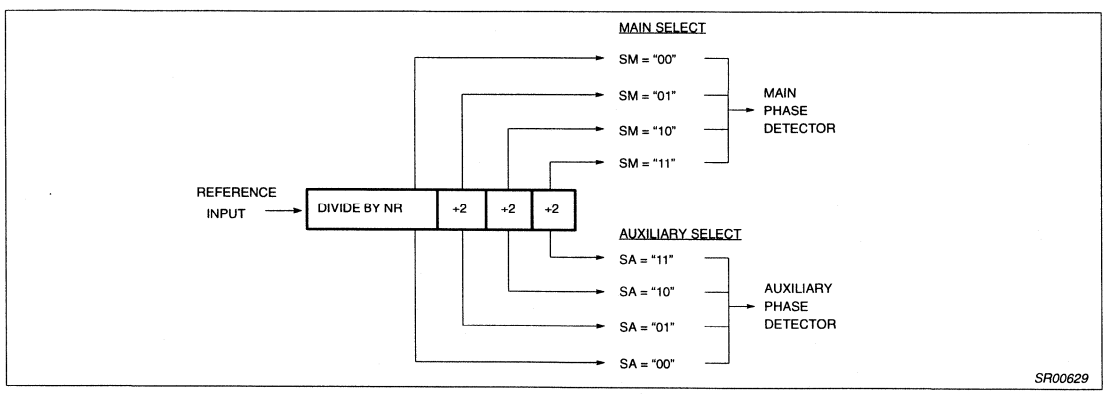


Figure 7. Reference Divider

Table 1. Function Table

Symbol	Bits	Function
NM1	12	Number of main divider cycles when prescaler modulus = 64*
NM2	8 if PR = "01" 4 if PR = "10"	Number of main divider cycles when prescaler modulus = 65*
NM3	4 if PR = "10"	Number of main divider cycles when prescaler modulus = 68*
NM4	4 if PR = "11" or "00"	Number of main divider cycles when prescaler modulus = 73*
PR	2	Prescaler type in use PR = "01": modulus 2 prescaler (64/65) PR = "10": modulus 3 prescaler (64/65/68) PR = "11": modulus 4 prescaler (64/65/68/73) PR = "00": modulus 3 prescaler (64/65/73)
NF	3	Fractional-N increment
FMOD	1	Fractional-N modulus selection flag "1": modulo 8 "0": modulo 5
LONG	1	A word format selection flag "0": 24 bit A0 format "1": 32 bit A1 format
CN	8	Binary current setting factor for main charge pumps
CL	2	Binary acceleration factor for proportional charge pump current
CK	4	Binary acceleration factor for integral charge pump current
EM	1	Main divider enable flag
EA	1	Auxiliary divider enable flag
SM	2	Reference select for main phase detector
SA	2	Reference select for auxiliary phase detector
NR	12	Reference divider ratio
NA	12	Auxiliary divider ratio
PA	1	Auxiliary prescaler mode: PA = "0": divide by 4 PA = "1": divide by 1
*Not including reset cycles and Fractional-N effects.		

Table 2. Prescaler Ratio

The total division ratio from prescaler to the phase detector may be expressed as:	
if PR = "01"	N = (NM1 + 2) x 64 + NM2 x 65 N' = (NM1 + 1) x 64 + (NM2 + 1) x 65 (*)
if PR = "10"	N = (NM1 + 2) x 64 + NM2 x 65 + (NM3 + 1) x 68 N' = (NM1 + 1) x 64 + (NM2 + 1) x 65 + (NM3 + 1) x 68 (*)
if PR = "11"	N = (NM1 + 2) x 64 + NM2 x 65 + (NM3 + 1) x 68 + (NM4 + 1) x 73 N' = (NM1 + 1) x 64 + (NM2 + 1) x 65 + (NM3 + 1) x 68 + (NM4 + 1) x 73 (*)
if PR = "00"	N = (NM1 + 2) x 64 + NM2 x 65 + (NM4 + 1) x 73 N' = (NM1 + 1) x 64 + (NM2 + 1) x 65 + (NM4 + 1) x 73 (*)
(*) When the fractional accumulator overflows the prescaler ratio = 65 (64 + 1) and the total division ratio N' = N + 1	

Table 3. PR Modulus

PR	Modulus Prescaler	Bit Capacity			
		NM1	NM2	NM3	NM4
01	2	12	8	–	–
10	3	12	4	4	–
11	4	12	4	4	4
00	3	12	8	–	4

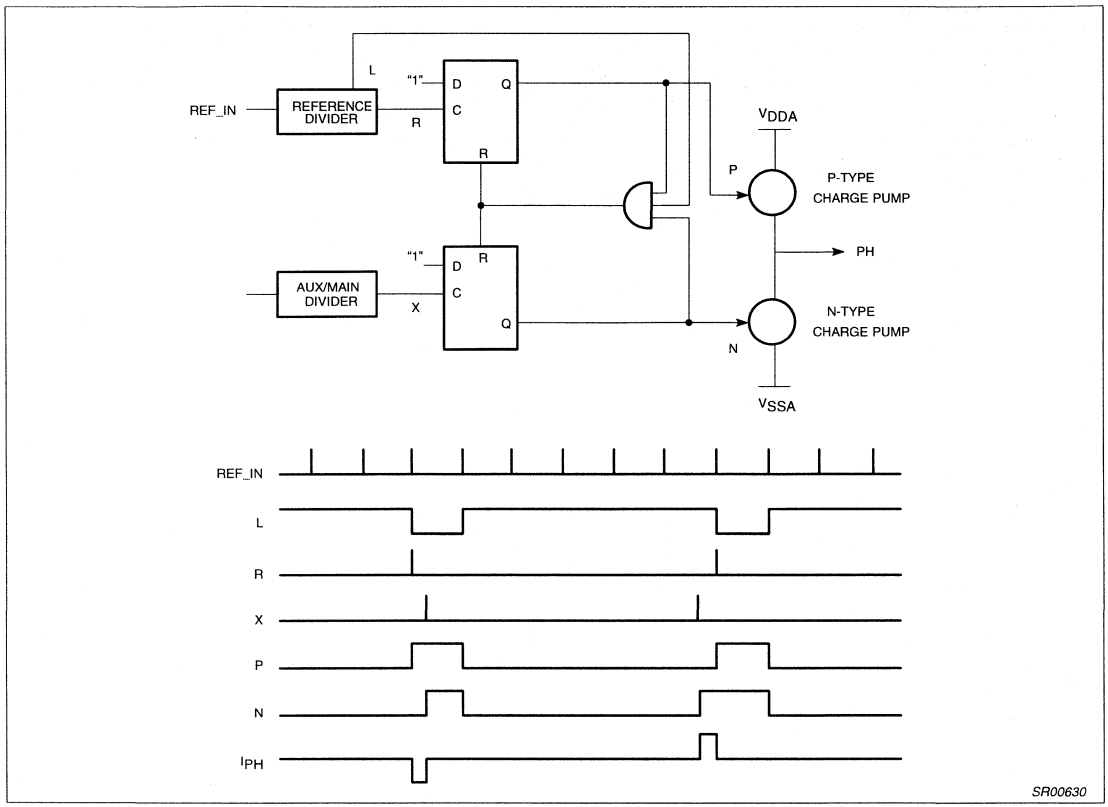


Figure 8. Phase Detector Structure with Timing

Phase Detectors

The auxiliary and main phase detectors are a two D-type flip-flop phase and frequency detector shown in Figure 8. The flip-flops are set by the negative edges of output signals of the dividers. The rising edge of the signal, L, will reset the flip-flops after both flip-flops have been set. Around zero phase error this has the effect of delaying the reset for 1 reference input cycle. This avoids non-linearity or deadband around zero phase error. The flip-flops drive on-chip charge pumps. A source current from the charge pump indicates the VCO frequency will be increased; a sink current indicates the VCO frequency will be decreased.

Current Settings

The SA8025A has 3 current setting pins: RA, RN and RF. The active charge pump currents and the fractional compensation currents are linearly dependent on the current connected between the current setting pin and V_{SS}. The typical value R (current setting resistor) can be calculated with the formula:

$$R = \frac{V_{DDA} - 0.9 - 150\sqrt{I_R}}{I_R}$$

The current can be set to zero by connecting the corresponding pin to V_{DDA}.

Auxiliary Output Charge Pumps

The auxiliary charge pumps on pin PHA are driven by the auxiliary phase detector and the current value is determined by the external resistor RA at pin RA. The active charge pump current is typically:

$$|I_{PHA}| = 8 \cdot I_{RA}$$

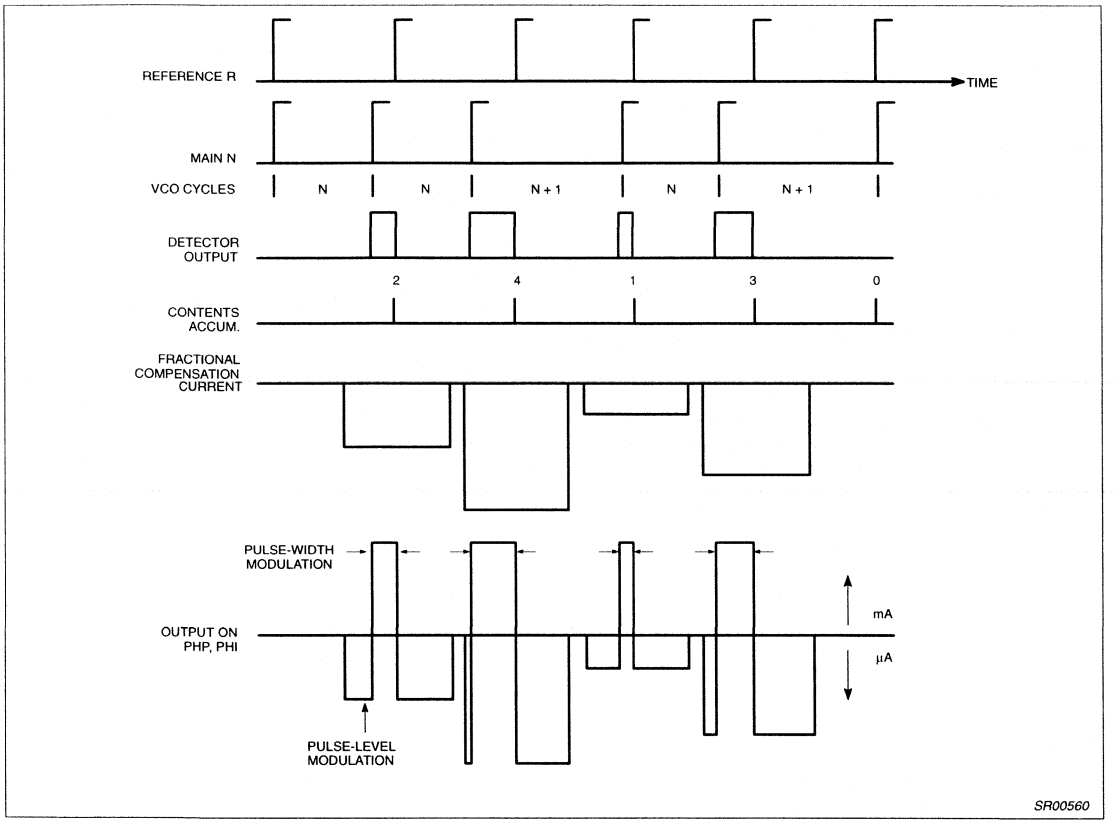


Figure 9. Waveforms for NF = 2, Fraction = 0.4

Main Output Charge Pumps and Fractional Compensation Currents

The main charge pumps on pin PHP and PHI are driven by the main phase detector and the current value is determined by the current at pin RN and via a number of DACs which are driven by registers of the serial input. The fractional compensation current is determined by the current at pin RF, the contents of the fractional accumulator FRD and a number of DACs driven by registers from the serial input. The timing for the fractional compensation is derived from the reference divider. The current is on during 1 input reference cycle before and 1 cycle after the output signal to the phase comparator. Figure 9 shows the waveforms for a typical case.

When the serial input A word is loaded, the output circuits are in the "speed-up mode" as long as the STROBE is H, else the "normal mode" is active. In the "normal mode" the current output PHP is:

$$I_{PHP\_N} = I_{PHP} + I_{PHP\_comp}$$

where:

$$|I_{PHP}| = \frac{CN \cdot I_{RN}}{32} \quad \text{:charge pump current}$$

$$|I_{PHP\_comp}| = FRD \cdot \frac{I_{RF}}{128} \quad \text{:fractional comp. current}$$

The current in PHI is zero in "normal mode".

In "speed-up mode" the current in output PHP is:

$$I_{PHP\_S} = I_{PHP} + I_{PHP\_comp}$$

$$|I_{PHP}| = \left(\frac{CN \cdot I_{RN}}{32}\right)(2^{CL+1} + 1)$$

$$|I_{PHP\_comp}| = \left(\frac{FRD \cdot I_{RF}}{128}\right)(2^{CL+1} + 1)$$

In "speed-up mode" the current in output PHI is:

$$I_{PHI\_S} = I_{PHI} + I_{PHI\_comp}$$

where:

$$|I_{PHI}| = \left(\frac{CN \cdot I_{RN}}{32}\right)(2^{CL+1})\ CK$$

$$|I_{PHI\_comp}| = \left(\frac{FRD \cdot I_{RN}}{128}\right)(2^{CL+1})\ CK$$

Figure 9 shows that for proper fractional compensation, the area of the fractional compensation current pulse must be equal to the area of the charge pump ripple output. This means that the current setting on the input RN, RF is approximately:

$$\frac{I_{RN}}{I_{RF}} \approx \frac{(Q \cdot f_{VCO})}{(3 \cdot CN \cdot F_{INR})}$$

where:

Q	=	fractional-N modulus
$f_{VCO} = f_{INM} \times N$,		input frequency of the prescaler
F_{INR} =		input frequency of the reference divider

PHI pump is meant for switching only. Current and compensation are not as accurate as PHP.

Lock Detect

The output LOCK is H when the auxiliary phase detector AND the main phase detector indicates a lock condition. The lock condition is defined as a phase difference of less than +1 cycle on the reference input REF_IN. The lock condition is also fulfilled when the relative counter is disabled (EM = "0" or respectively EA = "0") for the main, respectively auxiliary counter.

Test Modes

The lock output is selectable as f_{REF}, f_{AUX}, f_{MAIN} and lock. Bits T1 and T0 of the E word control the selection (see Figures 6 and 10).

If T1 = T0 = Low, or if the E-word is not sent, the lock output is configured as the normal lock output described in the Lock Detect section.

If T1 = Low and T0 = High, the lock output is configured as f_{REF}. The signal is the buffered output of the reference divider NR and the 3-bit binary counter SM. The f_{REF} signal appears as normally low and pulses high whenever the divider reaches terminal count from the value programmed into the NR and SM registers. The f_{REF} signal can be used to verify the divide ratio of the Reference divider.

If T1 = High and T0 = Low, the lock output is configured as f_{AUX}. The signal is normally high and pulses low whenever the divider reaches terminal count from the value programmed into the NA and PA registers. The f_{AUX} signal can be used to verify the divide ratio of the Auxiliary divider.

If T1 = High and T0 = High, the lock output is configured as f_{MAIN}. The signal is the buffered output of the MAIN divider. The f_{MAIN} signal appears as normally high and pulses low whenever the divider reaches terminal count from the value programmed into the NM1, NM2, NM3 or NM4 registers. The f_{MAIN} signal can be used to verify the divide ratio of the MAIN divider and the prescaler.

Test Pin

The Test pin, Pin 19, is a buffered logic input which is exclusively ORed with the output of the prescaler. The output of the XOR gate is the input to the MAIN divider. The Test pin must be connected to V_{DD} during normal operation as a synthesizer. This pin can be used as an input for verifying the divide ratio of the MAIN divider; while in this condition the input to the prescaler, RF_{IN}, may be connected to V_{CCP} through a 10kΩ resistor in order to place prescaler output into a known state.

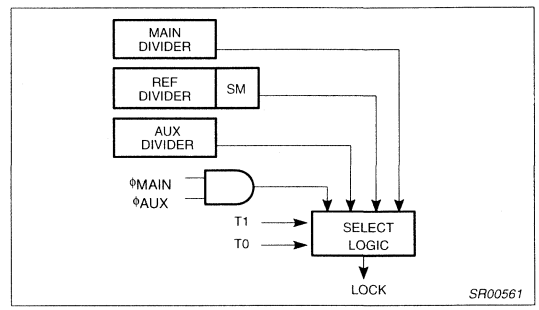


Figure 10. Test Mode Diagram

PIN FUNCTIONS

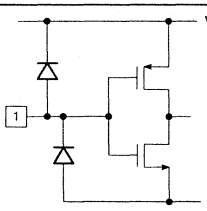
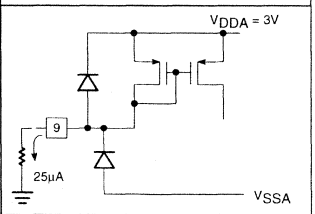
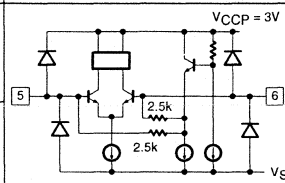
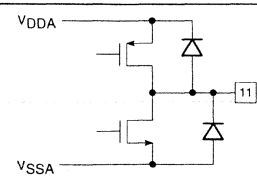
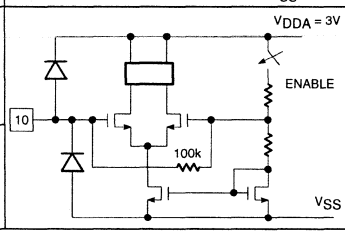
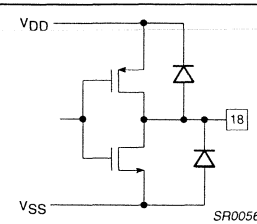
PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT	PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
1	CLOCK	—		9	RA	1.35	
2	DATA	—		16	RN	1.35	
3	STROBE	—					
19	TEST	—		17	RF	1.35	
5	RF_{IN}	2.1		11	PHA	—	
6	$\overline{RF_{IN}}$	2.1		13	PHI	—	
				14	PHP	—	
8	REF_{IN}	1.8		18	LOCK	—	
10	AUX_{IN}	1.8					

Figure 11. Pin Functions

TYPICAL PERFORMANCE CHARACTERISTICS

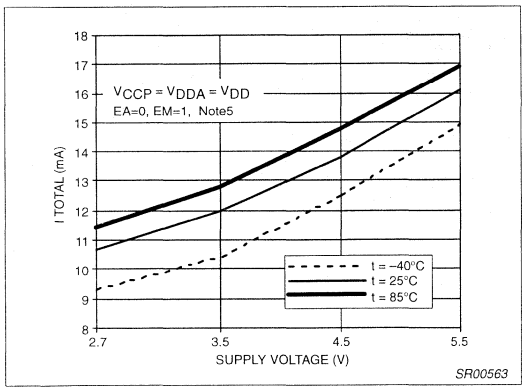


Figure 12. Operational Supply Current vs Supply Voltage and Temperature

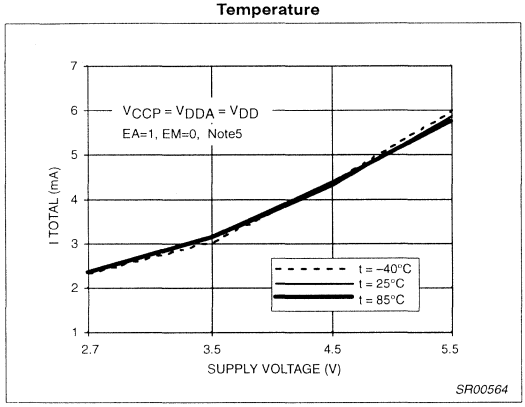


Figure 13. Auxiliary Operational Supply Current vs Supply Voltage and Temperature

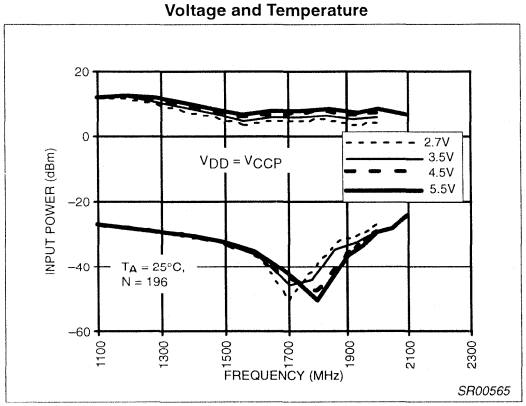


Figure 14. Main Divider Input Power vs Frequency and Supply

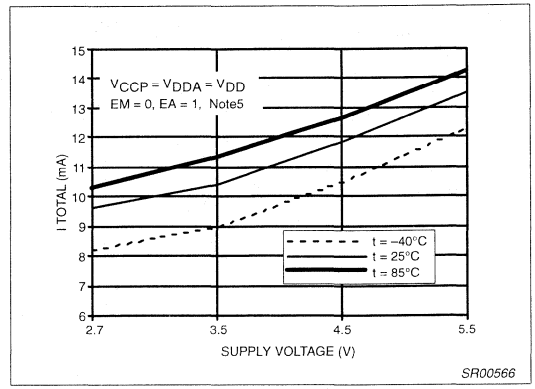


Figure 15. Main Operational Supply Current vs Supply Voltage and Temperature

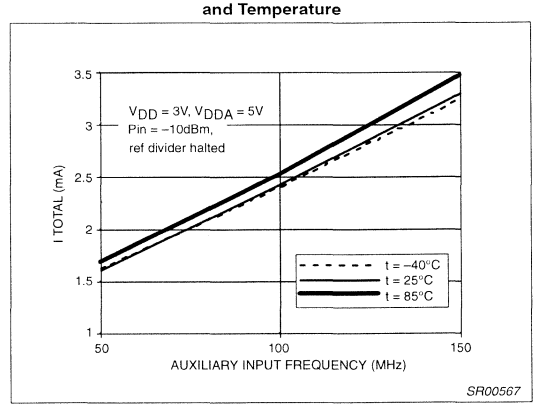


Figure 16. Auxiliary Operational Supply Current vs Frequency and Temperature

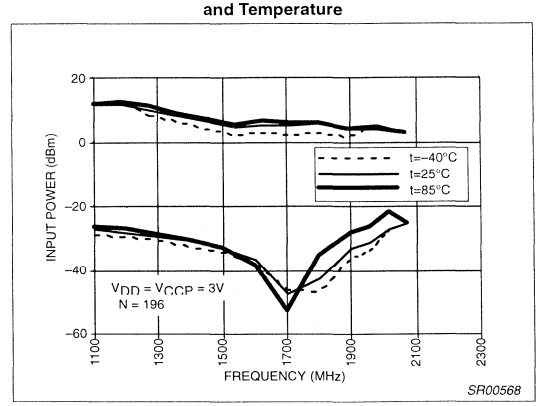


Figure 17. Main Divider Input Power vs Frequency and Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

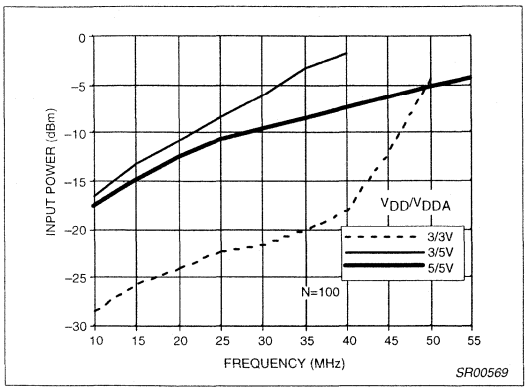


Figure 18. Reference Divider Minimum Input Power vs Frequency and Supply

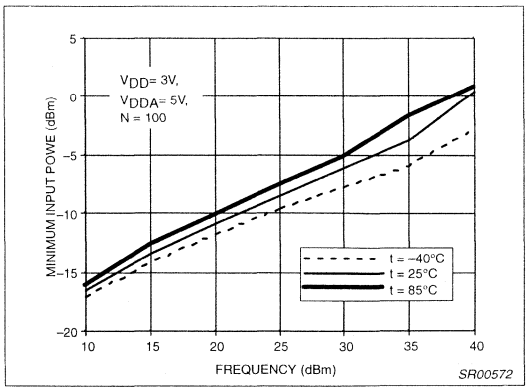


Figure 21. Reference Divider Minimum Input Power vs Frequency and Temperature

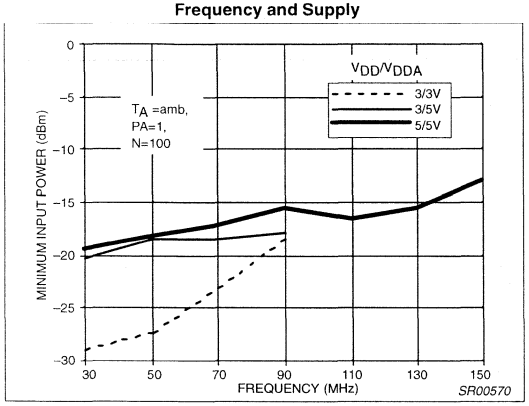


Figure 19. Auxiliary Divider Minimum Input Power vs Frequency and Supply

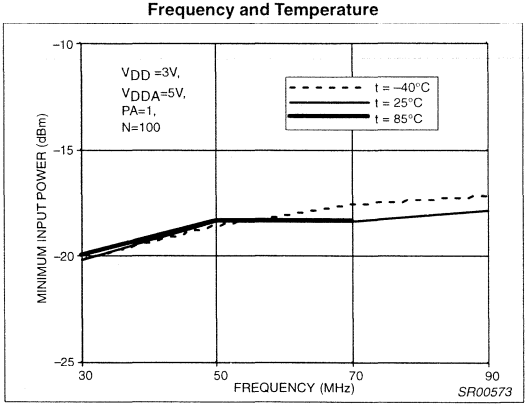


Figure 22. Auxiliary Divider Minimum Input Power vs Frequency and Temperature

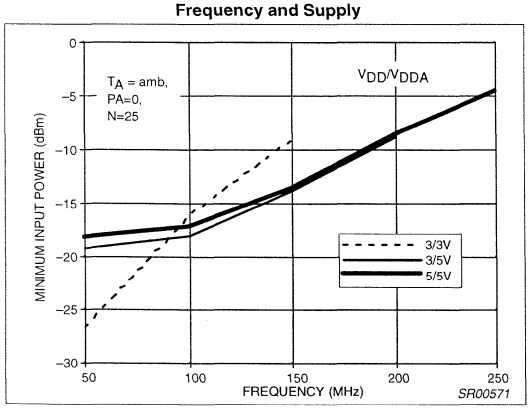


Figure 20. Auxiliary Divider Minimum Input Power vs Frequency and Supply

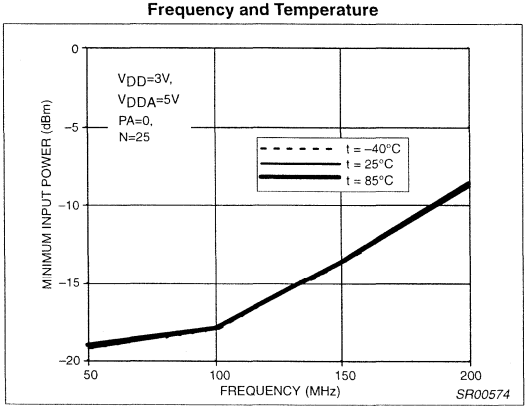


Figure 23. Auxiliary Divider Minumum Input Power vs Frequency and Temperature

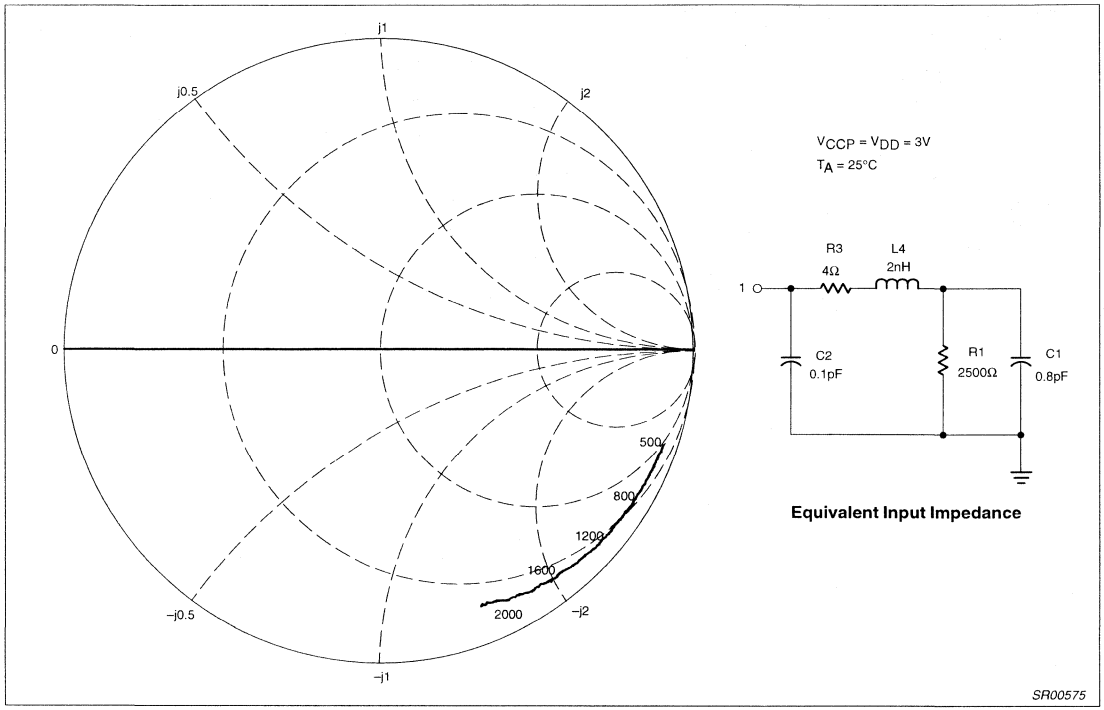
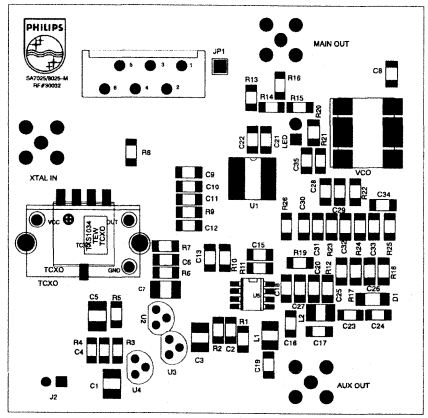
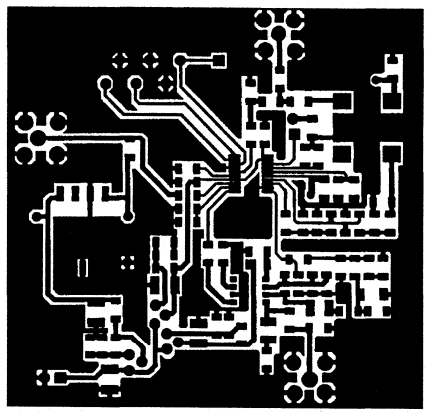


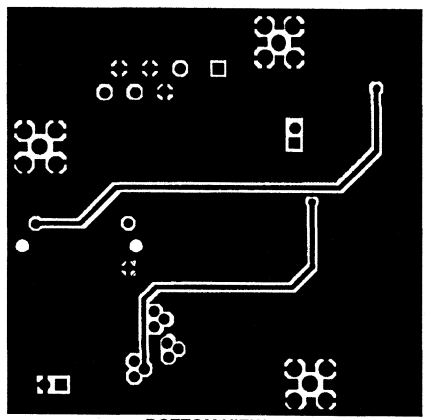
Figure 24. Typical RF_{IN} Input Impedance



TOP SILK SCREEN



TOP VIEW



BOTTOM VIEW

SR00576

Figure 25. SA8025ADK Demoboard Layout (NOT ACTUAL SIZE)

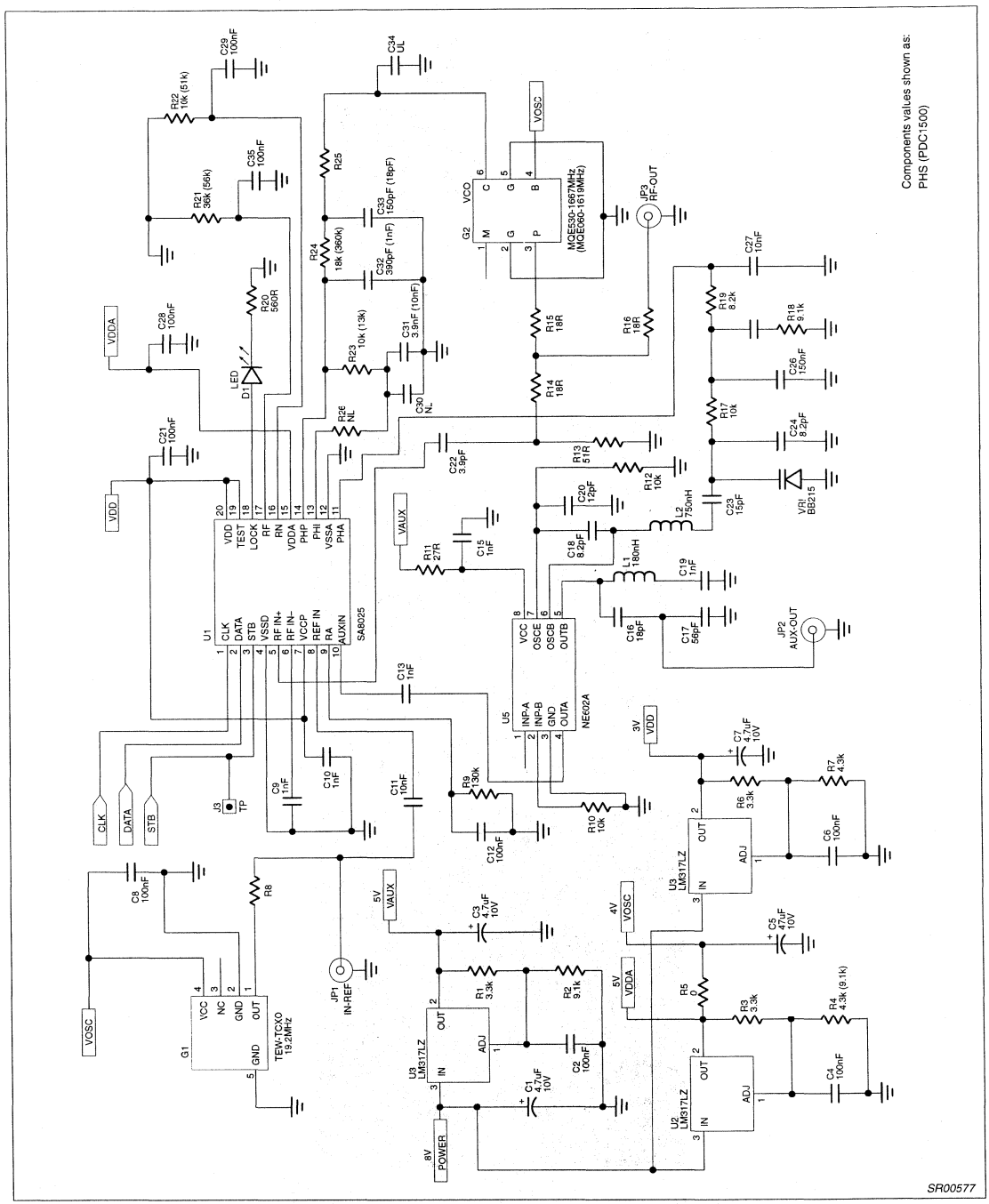


Figure 26. SA8025ADK Application Circuit

2.5GHz low voltage fractional–N dual synthesizer SA8026

FEATURES

- Low phase noise
- Fully programmable main and auxiliary dividers
- NORMAL & INTEGRAL charge pumps outputs
- Fast Locking Adaptive mode design
- Internal fractional spurious compensation
- Hardware and software power down

APPLICATIONS

- PCS
- Cellular phones
- Portable battery–powered radio equipment.

General description

The SA8026 BICMOS device integrates programmable dividers, charge pumps and a phase comparator to implement a phase–locked loop. The device is designed to operate from 3 NiCd cells, in pocket phones, with low current and nominal 3 V supplies.

The synthesizer operates at VCO input frequencies up to 2.5 GHz. The synthesizer has fully programmable main, auxiliary and reference dividers. All divider ratios are supplied via a 3–wire serial programming bus.

Separate power and ground pins are provided to the analog and digital circuits. The ground leads should be externally short–circuited to prevent large currents flowing across the die and thus causing damage. V_{DDA} should be equal to V_{DD}.

The charge pump current (gain) is fixed by an external resistance at pin RSET (pin). Only passive loop filters are used; the charge–pump operates within a wide voltage compliance range to provide a wider tuning range.

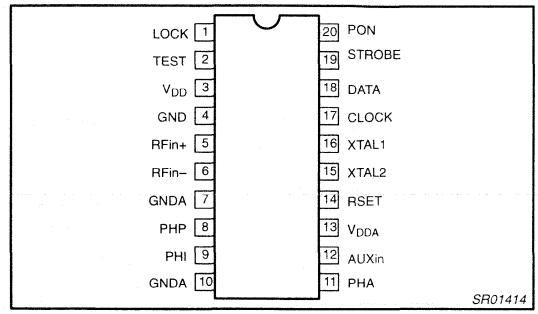


Figure 1. Pin Configuration

Quick reference data

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply voltage	V_{DD}	2.7	–	5.5	V
V_{DDA}	Analog supply voltage	$V_{DDA} = V_{DD}$	2.7	–	5.5	V
$I_{DDA}+I_{DD}$	Supply current	Main and aux. on	–	8.5	10	mA
$I_{DDA}+I_{DD}$	Total supply current in power–down mode		–	25	–	µA
f_{VCO}	Input frequency		800	–	2500	MHz
f_{AUX}	Input frequency		10	–	550	MHz
f_{XTAL}	Crystal reference input frequency		10	–	40	MHz
f_{PC}	Maximum phase comparator frequency		–		4	MHz
T_{amb}	Operating ambient temperature		–40	–	+85	°C

Ordering information

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SA8026DK	SSOP20	Plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266–1

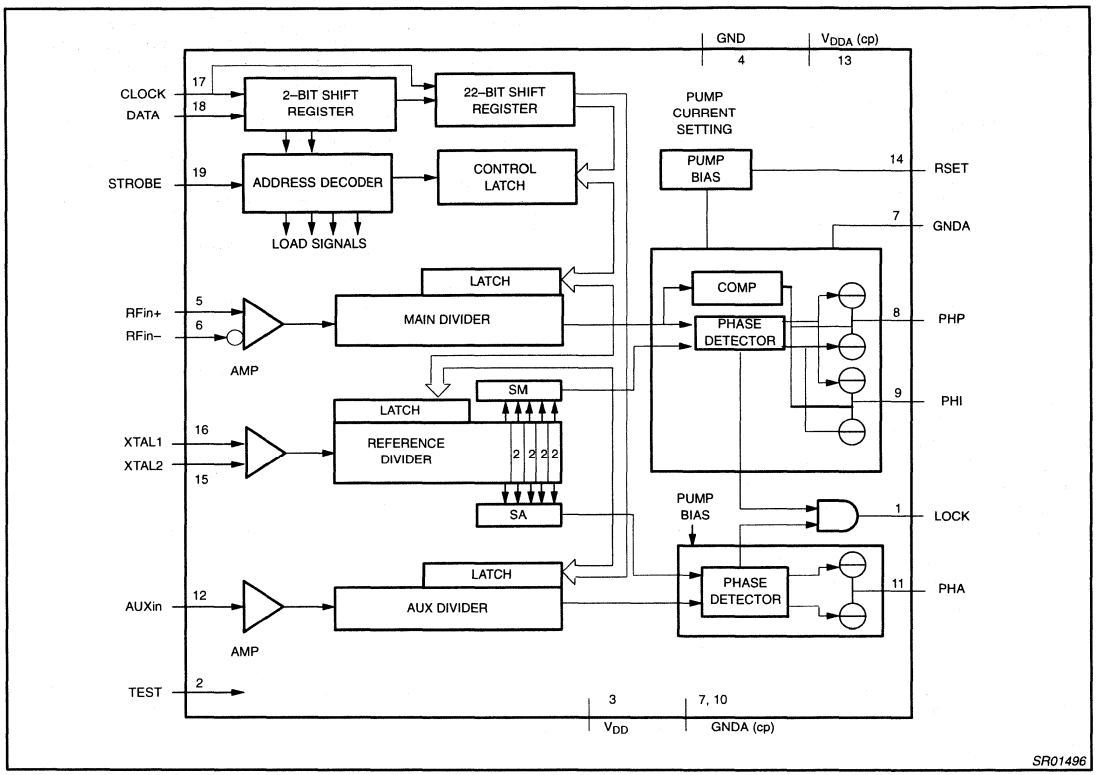


Figure 2. Block Diagram

PINNING

SYMBOL	PIN	DESCRIPTION
LOCK	1	Lock detect output
TEST	2	Test
V_{DD}	3	Digital supply
GND	4	Digital ground
RFin+	5	RF positive input to main divider
RFin–	6	RF negative input to main divider
GNDA	7	Charge pump ground
PHP	8	Main NORMAL chargepump
PHI	9	Main INTEGRAL chargepump
GNDA	10	Charge Pump Ground
PHA	11	Auxiliary chargepump output
AUXin	12	Input to auxiliary divider
V_{DDA}	13	Charge pump supply voltage
RSET	14	External resistor from this pin to ground sets the chargepump current
XTAL2	15	Reference input
XTAL1	16	Reference input
CLOCK	17	Programming bus clock input
DATA	18	Programming bus data input
STROBE	19	Programming bus enable input
PON	20	Power down control

FUNCTIONAL DESCRIPTION

Main Fractional–N divider

The RFin input (pins 5 and 6) drive a pre–amplifier to provide the clock to the first divider stage. For single ended operation, the signal should be fed to one of the inputs while the other one is AC grounded. The pre–amplifier has a high input impedance, dominated by pin and pad capacitance. The circuit operates with signal levels from –15dBm to +0dBm, and at frequencies as high as 2.5 GHz. The divider consists of a fully programmable bipolar prescaler followed by a CMOS counter. Divide ratios (512 to 65536) allow a minimum phase comparison frequency of 25kHz at 2.5 GHz RF.

At the completion of a main divider cycle, a main divider output pulse is generated which will drive the main phase comparator. Also, the fractional accumulator is incremented by the value of NF. The accumulator works with modulo Q set by FMOD. When the accumulator overflows the overall division ratio N will be increased by 1 to N + 1, the average division ratio over Q main divider cycles (either 5 or 8) will be

$$Nfrac \quad N \quad \frac{NF}{Q} \qquad (1)$$

The output of the main divider will be modulated with a fractional phase ripple. The phase ripple is proportional to the contents of the fractional accumulator and is nulled by the fractional compensation charge pump.

The reloading of a new programming word is synchronized to the state of the main divider to avoid introducing a phase disturbance.

Phase detector

The reference and main (aux) divider outputs are connected to a phase/frequency detector that controls the charge pump. The pump current is set by a an external resistor. The dead zone (caused by finite time taken to switch the current sources on or off) is cancelled by forcing the pumps ON for a minimum time at every cycle (backlash time) providing improved linearity.

Power–down mode

The power–down signal can be either hardware (PON) or software (PD). The PON signal exclusively ORed with the PD signal. If PON=0, then the part is powered up when PD=1. PON can be used to invert the polarity of the software bit PD. When the synthesizer is reactivated after the power–down the main and reference dividers are synchronized to avoid possibility of random phase errors on power–up.

Lock Detect

The output LOCK maintains a logic '1' when the auxiliary phase detector ANDed with the main phase detector indicates a lock condition. The lock condition for the main and auxiliary synthesizers is defined as a phase difference of less than ± 1 period of the frequency at the input XTAL1, 2. One counter can fulfill the lock condition when the other counter is powered down. Out of lock (logic '0' is indicated when both counters are powered down.

Reference divider

The reference divider consists of a divider with programmable values between 4 and 1023 followed by a three bit binary counter. The 3 bit SM (SA) register (see figure 5) determines which fo the 5 output pulses are selected as the main (auxiliary) phase detector input.

Auxiliary divider

The auxiliary divider consists of a divider with fully programmable values between 128 and 16384. The AUXin input, pin 13, drives a pre–amplifier to provide the clock to the first divider stage. The AUXin negative input is internally connected to ground. The pre–amplifier has a high input impedance, dominated by pin and pad capacitance. The circuit operates with signal levels from –15dBm to +0dBm, and at frequencies as high as 550 MHz. The divider consists of a fully programmable bipolar prescaler followed by a CMOS counter. The divide ratios allow a minimum phase comparison frequency of 25kHz at 550 MHz RF.

Serial programming bus

The serial input is a 3–wire input (CLOCK, STROBE, DATA) to program all counter divide ratios, fractional compensation DAC, selection and enable its. The programming data is structured into 24 bit words; each word includes 2 address bits. Figure 6 shows the timing diagram of the serial input. When the STROBE goes active HIGH, the clock is disabled and the data in the shift register remains unchanged. Depending on the 2 address bits the data is latched into different working registers or temporary registers. In order to fully program the synthesizer, 3 words must be sent: C, B, and A. Table 1 shows the format and the contents of each word. The D word is for testing purposes only. The data for the fractional compensation

DAC, FC is stored by the B word in temporary registers. When the A word is loaded, the data of these temporary registers is loaded together with the main divider ratio.

Limiting values

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	Digital supply voltage	–0.3	+5.5	V
V_{DDA}	Analog supply voltage	–0.3	+5.5	V
$\Delta V_{DDA}–V_{DD}$	Difference in voltage between V_{DDA} and V_{DD}		±0.3	V
V_n	Voltage at pins 1, 2, 5, 6, 12, 15 to 20	–0.3	V_{DD} + 0.3	V
V_1	Voltage at pin 8, 9, 13	–0.3	V_{DDA} + 0.3	V
ΔV_{GND}	Difference in voltage between GNDA and GND (these pins should be connected together)	–0.3	+0.3	V
P_{tot}	Total power dissipation		TBD	mW
T_{stg}	Storage temperature	–55	+125	°C
T_{amb}	Operating ambient temperature	–30	+85	°C
T_j	Maximum junction temperature		TBD	°C

Handling

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

Thermal characteristics

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j–a}$	Thermal resistance from junction to ambient in free air	120	K/W

Characteristics

$V_{DDA}=V_{DD}=3.0V$, $T_A=25°C$; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply; pins 3, 13						
V_{DD}	Digital supply voltage		2.7	–	5.5	V
V_{DDA}	Analog supply voltage	$V_{DDA} = V_{DD}$	2.7	–	5.5	V
$I_{DDTotal}$	Synthesizer operational digital supply current	V_{DD} = 3.0V	–	8.5	10	mA
$I_{standby}$	Total supply current in power–down mode	logic levels 0 or V_{DD}	–	25	TBD	µA
RFin main divider input; pins 5, 6						
f_{VCO}	VCO input frequency		800	–	2500	MHz
$V_{RFin(rms)}$	AC–coupled input signal level	R_s = 50 Ω; MAX. limit is indicative	–20	–	0	dBm
Z_{IRFin}	Input impedance (real part)	f_{VCO} = 2.0 GHz	–	TBD	–	kΩ
C_{IRFin}	Typical pin input capacitance	indicative, not tested	–	TBD	–	pF
N_m	Main divider ratio		512	–	65535	
f_{PCmax}	Maximum loop comparison frequency	indicative, not tested	–	–	4	MHz
AUX reference divider input; pins 12						
f_{AUXin}	Input frequency range		10	–	550	MHz
V_{AUXin}	AC–coupled input signal level	R_s=50Ω; MAX. limit is indicative	–15	–	0	dBm
Z_{AUXin}	Input impedance (real part)	f_{VCO}=500 MHZ	–	TBD	–	kΩ
C_{AUXin}	Typical pin input capacitance	indicative, not tested	–	TBD	–	pF
N_{AUX}	Auxiliary division ratio		128	–	16384	
Reference divider input; pins 15, 16						
f_{REFin}	Input frequency range from crystal		10	–	40	MHz
VRFin	AC–coupled input signal level	R_S=50Ω; MAX. limit is indicative	–5	–	+5	dBm
Z_{REFin}	Input impedance (real part)		–	TBD	–	kΩ
C_{REFin}	Typical pin input capacitance	indicative, not tested	–	TBD	–	pF
R_{REF}	Reference division ratio	SA=SM="000"	4	–	1023	
Charge pump current setting resistor input; pin 14						
R_{SET}	External resistor from pin 3 to ground		6	7.5	24	kΩ
V_{SET}	Regulated voltage at pin 3	R_{SET}=7.5 kΩ	–	1.23	–	V
Charge pump outputs (including fractional compensation pump); pins 8, 9, 11; R_{SET} =7.5 KΩ, FC=80						
Icp	Chargepump current ratio to Iset	CURRENT GAIN I_{PH}/I_{SET}	–15		+15	%
I_{MATCH}	Sink–to–source current matching	V_{ph}=1/2 V_{DDA}	–5		+5	%
I_{ZOUT}	Output current variation versus Vph^2	V_{ph} in compliance range	–10		+10	%
I_{LPH}	Charge pump off leakage current	V_{cp}=1/2 V_{CC}	–10	±1	+10	nA

V_{ph}	Charge pump voltage compliance		0.7	–	V_{DDA}–0.8	V
Phase noise						
C/N	Synthesizer's contribution to close–in–phase noise of 1800 MHz RF signal at 1 kHz offset.	fref=19.68MHz; fcomp=80kHz indicative, not tested	–	–78	–	dBc/Hz
C/N	Synthesizer's contribution to close–in–phase noise of 2100 MHz RF signal at 1 kHz offset.	fref=19.44MHz; fcomp=240kHz indicative, not tested	–	–73	–	dBc/Hz
Interface logic input signal levels; pins 3, 15, 16, 18, 19, 20						
V_{IH}	HIGH level input voltage		0.7*V_{DD}	–	V_{DD}+0.3	V
V_{IL}	LOW level input voltage		–0.3	–	0.3*V_{DD}	V
I_{bias}	Input bias current	logic 1 or logic 0	–5	–	+5	µA
Lock detect output signal (in push/pull mode); pin 1						
V_{OL}	LOW level output voltage	I_{sink} = 2mA	–	–	0.4	V
V_{OH}	HIGH level output voltage	I_{source} = –2mA	V_{DD}–0.4	–	–	V

NOTES:

1. $I_{SET} = \frac{V_{SET}}{R_{SET}}$ bias current for charge pumps.

2. The relative output current variation is defined thus:

$\frac{\Delta I_{OUT}}{I_{OUT}} \quad 2 \cdot \frac{(I_2 - I_1)}{|(I_2 \quad I_1)|}$; with V_1 0.7V, V_2 V_{DDA} –0.8V (See Figure 3.)

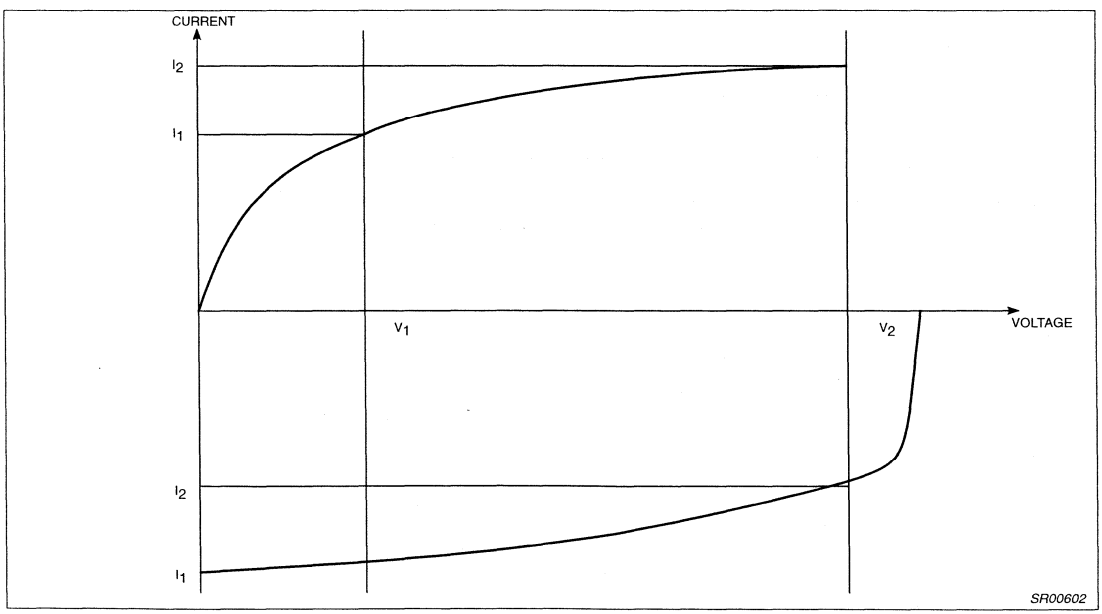


Figure 3. Relative Output Current Variation

Serial bus timing characteristics. See Figure 4.

V_{DD}= V_{DDA} =3.0V; T_{amb} = 25°C unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Serial programming clock; CLK					
t_r	Input rise time	–	10	40	ns
t_f	Input fall time	–	10	40	ns
T_{cy}	Clock period	100	–	–	ns
Enable programming; STROBE					
t_{START}	Delay to rising clock edge	40	–	–	ns
t_W	Minimum inactive pulse width	1/fcomp	–	–	ns
$T_{SU;\overline{E}}$	Enable set–up time to next clock edge	20	–	–	ns
Register serial input data; DATA					
$t_{SU;DAT}$	Input data to clock set–up time	20	–	–	ns
$t_{HD;DAT}$	Input data to clock hold time	20	–	–	ns

Application information

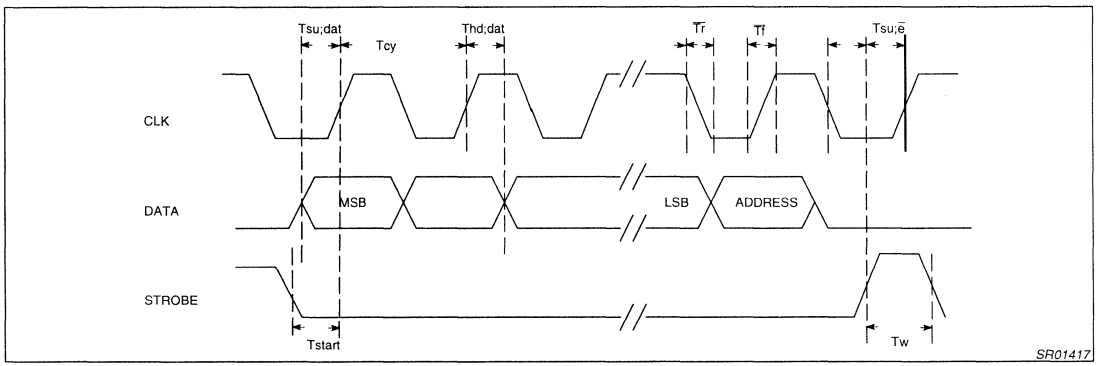


Figure 4. Serial Bus Timing Diagram

Main Output Charge Pumps and Fractional Compensation Currents.

The main charge pumps on pins PHP and PHI are driven by the main phase detector and the charge pump current values are determined by the current at pin RSET. The fractional compensation is derived from the current at RSET, the contents of the fractional accumulator FRD and by the program value of the FC DAC. The timing for the fractional compensation is derived form the main divider. See table of charge pump ratios.

Data format

Table 1 Format of programmed data

LAST IN		MSB	SERIAL PROGRAMMING FORMAT				FIRST IN LSB
p23	p22	p21	p20	../..	../..	p1	p0

Table 2 A word, length 24 bits

LAST IN					MSB														LSB	FIRST IN	
Address		fmod	Fractional–N		Main Divider ratio															Spare	
0	0	FM	NF2	NF1	NF0	N15	N14	N13	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	N0	SK1	SK2
Default:		0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	1	0	0	0	0	0	0

A word select	Fixed to 00.
Fractional Modulus select	FM 0=modulo 8, 1=modulo 5.
Fractional–N Increment	NF2..0 Fractional N Increment values 000 to 111.
N–Divider	N0..N15, Main divider values 512 to 65535 allowed for divider ratio.

B word, length 24 bits

ADDRESS		REFERENCE DIVIDER										LOCK		PD		FRACTIONAL COMPENSATION DAC							
0	1	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	L1	L0	Main	Aux	FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0
Default:		0	0	0	1	0	1	0	0	0	1	0	0	1	1	0	1	0	1	0	0	0	0

B word select	Fixed to 01
R–Divider	R0..R9, Reference divider values 4 to 1023 allowed for divider ration.
Charge pump current Ratio	CP1, CP0: Charge pump current ratio, see table of charge pump currents.
Lock detect output	L1 L0 0 0 Combined main, aux. lock detect signal present at the LOCK pin (push/pull). 0 1 Combined main, aux, lock detect signal present at the LOCK pin (open drain). 1 0 Main lock detect signal present at the LOCK pin. 1 1 Auxiliary loop lock detect signal present at the LOCK pin. When auxiliary loop and main loop are in power down mode, the lock indicator is low.
Power down	Main=1: power to N–divider, reference divider, main charge pumps, Main=0 to power down. Aux=1: power to Aux divider, reference divider, aux charge pump, Aux=0 to power down.
Fractional Compensation	FC7..0 Fractional Compensation charge pump current DAC, values 0 to 255. Recommended values: FC=80 for MOD 8; FC=128 for MOD 5.

Table 3 C word, length 24 bits

Address		Auxiliary Divider														CP		SM			SA		
1	0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	CP1	CP0	SM2	SM1	SM0	SA2	SA1	SA0
Default		0	0	0	0	0	1	1	1	0	0	1	0	1	0	1	1	0	0	0	0	0	0

C word select	Fixed to 10
A–Divider	A0..A13, Auxiliary divider values 128 to 16384 allowed for divider ratio.
Charge pump current Ratio	CP1, CP0: Charge pump current ratio, see table fo charge pump currents.
Main comparison select	SM comparison divider select for main phase detector.
Aux comparison select	SA Comparison divider select for auxiliary phase detector.

Table 4 D word, length 24 bits

ADDRESS			SYNTHESIZER TEST BITS																		
1	1	0																			

Main and auxiliary chargepump currents

CP1	CP0	I_{PHA}	I_{PHP}	I_{PHP-SU}	I_{PHI}
0	0	1.5xIset	3xIset	15xIset	36xIset
0	1	0.5xIset	1xIset	5xIset	12xIset
1	0	1.5xIset	3xIset	15xIset	0
1	1	0.5xIset	1xIset	5xIset	0

NOTES
1. $I_{SET}=^{Vset}/_{Rset}$: bias current for charge pumps.
2. CP1 is used to disable the PHI pump, I_{PHP_SU} is the total current at pin PHP during speed up condition.

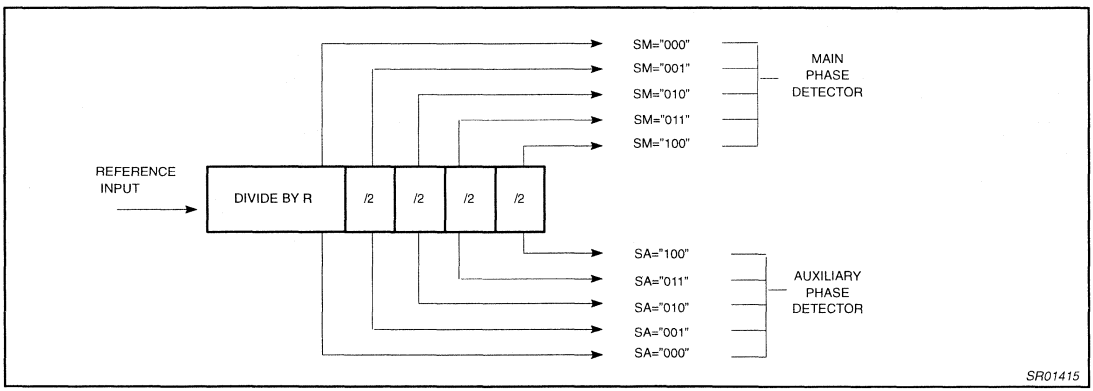


Figure 5. Reference Divider

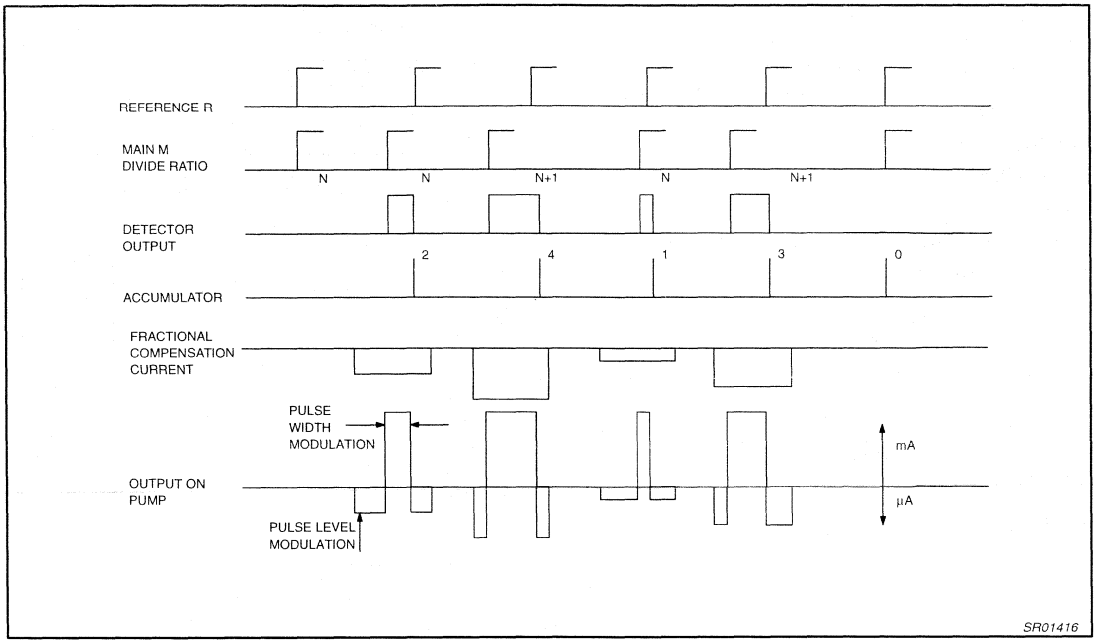


Figure 6. Waveforms for NF=2, Fraction=0.4

Fig 6. shows that for a proper fractional compensation, the area of the fractional compensation current pulse must be equal to the area of the charge pump ripple output.

900 MHz transmit modulator and 1.3 GHz fractional–N synthesizer

SA9024

DESCRIPTION

This specification defines the requirements for a transmitter modulator and fractional–N synthesizer IC to be used in cellular telephones which employ the North American Dual Mode Cellular System (IS–136).

FEATURES

- Low current from 3.75V supply
- Low phase noise
- Main loop with internal charge pump and fractional compensation
- 3–line serial interface bus
- Power down for the synthesizers
- Speedup mode for faster switching

APPLICATIONS

- Cellular phones
- Portable battery–powered radio equipment.

GENERAL DESCRIPTION

The SA9024 BICMOS device integrates:

- Main channel synthesizer
- Auxiliary synthesizer
- Transmit offset synthesizer and oscillator
- I/Q modulator
- Power control
- Reference and clock buffers
- Control logic for programming and power down modes

PIN CONFIGURATION

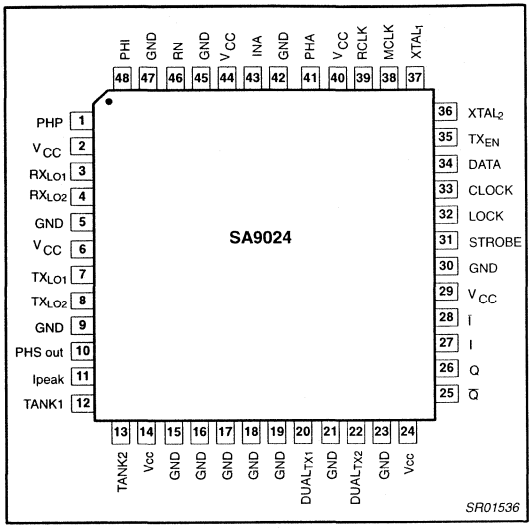


Figure 1. Pin Configuration

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply voltage	V_{CC}	3.6	3.75	3.9	V
I_{CC}	Supply current		–	TBD	–	mA
I_{CC_save}	Total supply current in power–down mode		–	TBD	–	mA
f_{VCO}	Input frequency		800	–	1300	MHz
f_{AUX}	Input frequency		10	–	500	MHz
f_{XTAL}	Crystal reference input frequency		10	–	40	MHz
f_{PC}	Maximum phase comparator frequency	Main and Aux loops	–	–	5	MHz
T_{amb}	Operating ambient temperature		–40	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SA9024	LQFP48	Plastic low profile quad flat package; 48 leads; body 7x7x1.4 mm	SOT313-2

CONNECTIONS

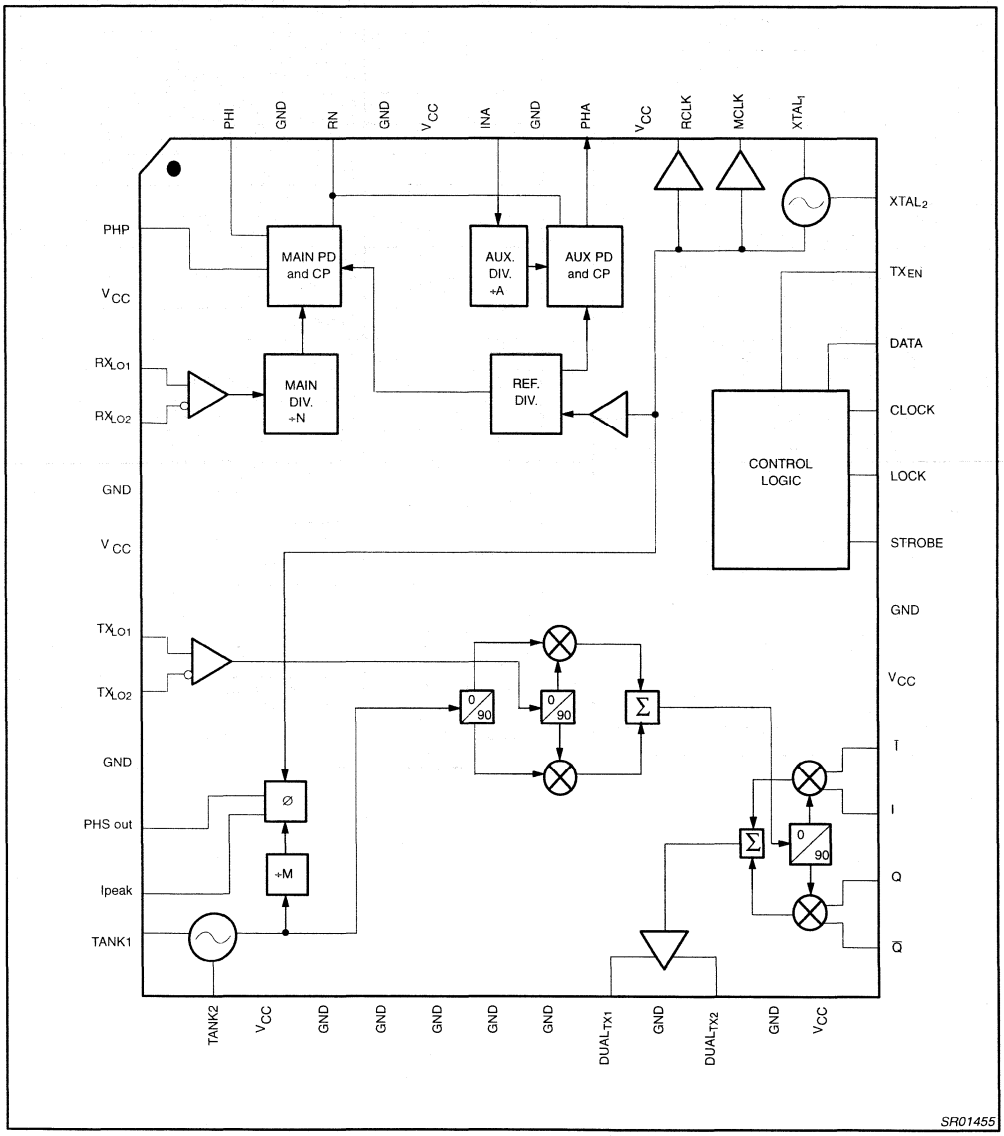


Figure 2. SA9024 Block Diagram

PIN DESCRIPTIONS

PIN NO.	PIN	DESCRIPTION
1	PHP	Proportional charge pump output
2	V_{CC}	Digital supply voltage
3	RX_{LO1}	Differential LO input
4	RX_{LO2}	Differential LO input
5	GND	Digital Ground
6	V_{CC}	Tank supply voltage
7	TX_{LO1}	Differential Transmit LO Input
8	TX_{LO2}	Differential Transmit LO Input
9	GND	Tank Ground
10	PHS OUT	Charge pump output (transmit offset)
11	I_{PEAK}	PHS out current set resistor
12	TANK1	VCO differential tank
13	TANK2	VCO differential tank
14	V_{CC}	Tx supply voltage
15	GND	Tx Ground
16	GND	Tx Ground
17	GND	Tx Ground
18	GND	Tx Ground
19	GND	Tx Ground
20	DUALTX1	Dual mode RF output
21	GND	Tx Ground
22	DUALTX2	Dual mode RF output
23	GND	Tx Ground
24	V_{CC}	Tx supply voltage
25	$\overline{Q}$	Inverting quadrature input
26	Q	Non–Inverting quadrature input
27	$\overline{I}$	Non–inverting in phase modulation input
28	I	Inverting in phase modulation input
29	V_{CC}	Tx supply voltage
30	GND	Tx Ground
31	STROBE	Data input latch enable
32	LOCK	Lock detect
33	CLOCK	Serial clock input
34	DATA	Serial data input
35	TX_{EN}	Transmit enable
36	$XTAL_2$	Crystal Oscillator emitter input
37	$XTAL_1$	Crystal Oscillator base Input
38	MCLK	Buffered oscillator output
39	RCLK	Buffered oscillator output
40	V_{CC}	REF supply voltage
41	PHA	Auxiliary charge pump output
42	GND	REF Ground
43	INA	RX_{IF} input
44	V_{CC}	CP supply voltage
45	GND	CP Ground
46	RN	CP current set resistor
47	GND	CP Ground
48	PHI	Integral charge pump output

OPERATING MODES & POWER DOWN CONTROL

There are two power saving modes of operation which the SA9024 can be put into, dependent on the status of the system. The intention of these different modes is to disable circuity that is not in use at the time in order to reduce power consumption. During sleep mode, only circuitry which is required to provide a master clock to the digital portion of the system is enabled. During receive mode, circuitry which is used to perform the receive function and provide a master clock is enabled. In transmit mode all the functions of the chip are enabled which are required to perform transmit, receive and provide master clock.

SA9024 POWER MODE TRUTH TABLE

	Sleep Mode		Receive Mode		Transmit Mode	
Enabled	yes	no	yes	no	yes	no
Crystal Oscillator	✓		✓		✓	
Phase detector and charge pump (transmit offset)		✓		✓	✓	
VCO		✓		✓	✓	
SSB Up-converter		✓		✓	✓	
MCLK Buffer	✓		✓		✓	
RCLK Buffer		✓	✓		✓	
÷M offset loop divider		✓		✓	✓	
TX_{LO} Buffer		✓		✓	✓	
RX_{LO} Buffer		✓	✓		✓	
I/Q Modulator		✓		✓	✓	
Variable Gain Amp.		✓		✓	✓	
Control Logic	✓		✓		✓	
Main Divider		✓	✓		✓	
Reference Divider		✓	✓		✓	
Auxiliary Divider		✓	✓		✓	
Main Phase Detector and charge pump		✓	✓		✓	
Auxiliary Phase Detector and charge pump		✓	✓		✓	
Lock Detect		✓	✓		✓	

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	VALUE		UNIT
		MIN.	MAX.	
V_{CC}	Supply voltage	-0.3	+4.5	V
V_{IN}	Voltage applied to any other pin	-0.3	V_{CC}+0.3	V
P_N	Power dissipation, T_A = 25°C (still air)		980	mW
T_{JMAX}	Operation junction temperature		TBD	°C
P_{MAX}	Power input/output		+10/+14	dBm
I_{MAX}	DC current into any I/O pin	-10	+10	mA
T_{STG}	Storage temperature	–65	+150	°C
T_o	Operating temperature	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3.75 V; T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{CC}	Power supply range		3.6	3.75	3.9	V
I_{CC}	Supply current	Sleep mode		2		mA
		Standby mode		17		
		Operating: full power analog		95		
		Operating: full power digital DUAL[1]		52		
I / $\overline{I}$	In-phase differential input	quiescent		V_{CC} /2		V
Q / $\overline{Q}$	Quadrature phase differential input	quiescent		V_{CC} /2		V
V_{IL}	Clock, Data, Strobe, TX_{EN}	Input logic low	–0.3		0.3 × V_{CC}	V
V_{IH}	Clock, data, strobe, TX_{EN}	Input logic high	0.7 × V_{CC}		V_{CC}+0.3	V
T_A	Ambient temperature range		-40	+25	+85	°C
Digital Outputs Lock						
V_{OL}	Output voltage LOW	I_O = 2mA			0.4	V
V_{OH}	Output voltage HIGH	I_O = -2mA	V_{CC} – 0.4			V
Charge Pump Current Setting Resistor Input; RN, R_{Ipeak}						
RN	External resistor to ground		6	7.5	24	kΩ
R_{Ipeak}	External resistor to ground			4.7		kΩ
V_{RN}	Regulated voltage	RN = 7.5 kΩ		1.23		V
V_{Ipeak}	Regulated voltage	R_{ipeak} = 4.7 kΩ		1.3		V
I_{peak}	PHSOUT programming	R_{ipeak} = 4.7 kΩ		0.26		mA
PHS_{gain}	PHSOUT gain	R_{ipeak} = 4.7 kΩ		24xI_{peak}		mA
Kϕ	PD phase gain	Transmit offset PLL in phase lock		4.33		mA/rad
Charge Pump Outputs (including fractional compensation pump, not PHS) RN = 7.5 kΩ						
I_{OPH}	Charge pump output current error versus expected current.		–15		15	%
I_{MATCH}	Sink to source current matching	V_{PHX} = V_{CC}/2	–5		5	%
	Current output variation versus V_{PHX}	V_{PHX} in compliance range	–10		10	%
	Charge pump off, leakage current	V_{PHX} = V_{CC}/2	–10	±1	10	nA
V_{PH}	Charge pump voltage compliance[3]		0.7		V_{CC} – 0.8	V
Charge Pump Outputs (only PHS) R_{Ipeak} = 4.7 kΩ						
I_{OPH}	Charge pump output current error versus expected current.		–15		15	%
I_{MATCH}	Sink to source current matching	V_{PHS} = V_{CC}/2	–10		10	%

	Current output variation versus V_{PH}	V_{PHS} in compliance range	–25		25	%
V_{PH}	Charge pump voltage compliance		0.5		V_{CC}–0.5	V

AC ELECTRICAL CHARACTERISTICS

V_{CC} = +3.75 V; T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Modulator						
$TX_{LO\ 1/2}$	Transmit LO input (AC-coupled; 50Ω single-ended, 100Ω differential)	Input power Frequency range	-13 900		-10 1100	dBm MHz
VSWR				2:1		
TANK1/2	VCO tank differential inputs	Frequency range	90		180	MHz
÷M	PLL offset divider	Maximum input frequency	180			MHz
$XTAL_1$	Osc. transistor base	Osc. frequency	10		40	MHz
$XTAL_2$	Osc. transistor emitter	Osc. frequency	10		40	MHz
XO	Negative resistance			–100		Ω
RCLK, MCLK	Reference buffer output Frequency range Output levels Harmonic content	Z_{LOAD} = 5kΩ| 7 pF	 10 0.7	 1.0	 40 1.4 –10	 MHz V_{P-P} dBc
TX_{EN}	Transmit enable	Transmit enable Transmit disable		TX_{EN} = 1 TX_{EN} = 0		Logic
Q / $\overline{Q}$ I / $\overline{I}$	Baseband in-phase differential inputs	Maximum frequency Diff. mod. level Diff. input impedance DC bias point	1.8 0.8 10.0 1.8	 0.9 V_{CC}/2	 1.0 2.55	MHz V_{P-P} kΩ V
TX_{RF}	TX_{RF} operating range		820		920	MHz
$DUAL_{TX}$	DUAL output SE=1, TX_{EN}=1 (with external matching) (50Ω)	AMPS/DAMPS	820		853	MHz
$DUAL_{TX}$	Differential output, ($DUAL_{TX}$) open-collector, matched to 200Ω differential impedance	Output level (avg. min., I and Q quad., 0dB VGA) Gain flatness	+6.0	+10 1	+13.5	dBm dB
$DUAL_{TX}$	Linearity worst case intermod. products (0dB VGA OR +6 dBm, whichever is less, I & Q in-phase)	3rd-order 5th-order 7th-order		-42 -55 -65	-30 -45 -53	dBc
$DUAL_{TX}$	Carrier suppression (I & Q in quadrature)	VGA = 0dB VGA = -38dB		-45 -33	-30	dBc
$DUAL_{TX}$	Sideband suppression (I & Q in quadrature)			-45	-32	dBc
$DUAL_{TX}$	Spurious output	2 to 284 MHz			-45	dBc
		824 to 849 MHz			-47	
		849 to 869 MHz			-45	
		869 to 894 MHz			-104	dBm
		894 to 8490 MHz			-45	dBc
$DUAL_{TX}$	TX_{LO} up-conversion products	TX_{LO}			-21	dBc
		Upper Side Band			–21	
		TX_{LO} ±3 × TX_{OFFSET}			-36	
		Harmonics ≤ 10th			-21	
$DUAL_{TX}$	Broad-band noise (0dB VGA or +6 dBm, whichever is less)	869 to 894 MHz			-123	dBm/Hz
$DUAL_{TX}$	Adjacent channel noise power	@ 30 kHz			-95	dBc/Hz
$DUAL_{TX}$	Alternate channel noise power	@ 60 kHz			–101	dBc/Hz

Synthesizer						
		Main Divider				
f_{MMAX}	Input frequency range		800		1300	MHz
	Input harmonics	No multi–clocking	–10			dBc
$RX_{LO\ 1/2}$	Synthesizer LO input (AC-coupled; external shunt 50Ω single-ended, 100Ω differential)	Input power	–20		0	dBm
		Reference Divider				
f_{RMAX}	Input frequency RANGE		10		40	MHz
	Input harmonics	No multi–clocking	–10			dBc
		Auxiliary Divider				
f_{AMAX}	Input frequency RANGE		10		500	MHz
	Input harmonics	No multi–clocking	–10			dBc
V_{INA}	Input signal amplitude		0.200			V_{P-P}
		Serial Interface				
f_{CLOCK}	Clock frequency				10	MHz
t_{SU}	Set-up time: DATA to CLOCK, CLOCK to STROBE		30			ns
t_H	Hold time: CLOCK to DATA		30			ns
t_{SW}	Pulse width	CLOCK	30			ns
		STROBE (B - D words)	30			
		A word	$\frac{1}{f_{REF} \cdot NREF} + t_W$			

1. Transmit mode @ 33% duty cycle.
2. The relative output current variation is defined thus:
   $\Delta I_{out}/I_{out} = 2x(I_2 - I_1)/|(I_2 + I_1)|$; with V_1=0.7V, $V_2 = V_{CC}$–0.8V (see figure 3)
3. Power supply current measured with $f_{RX\ =\ 2100.54\ MHZ}$, f_{REF} = 19.44 MHz, f_{INA}= 109.92 MHz, main phase detector bias resistor = 7.5 kΩ. Main phase detector reference frequency = 240 kHz, auxiliary phase detector frequency = 240 kHz.
4. Maximum and minimum levels guaranteed by design and random testing for temperature range of –40 to +85°C.
5. Power is rated at I/Q input level of $0.9V_{PP}$.

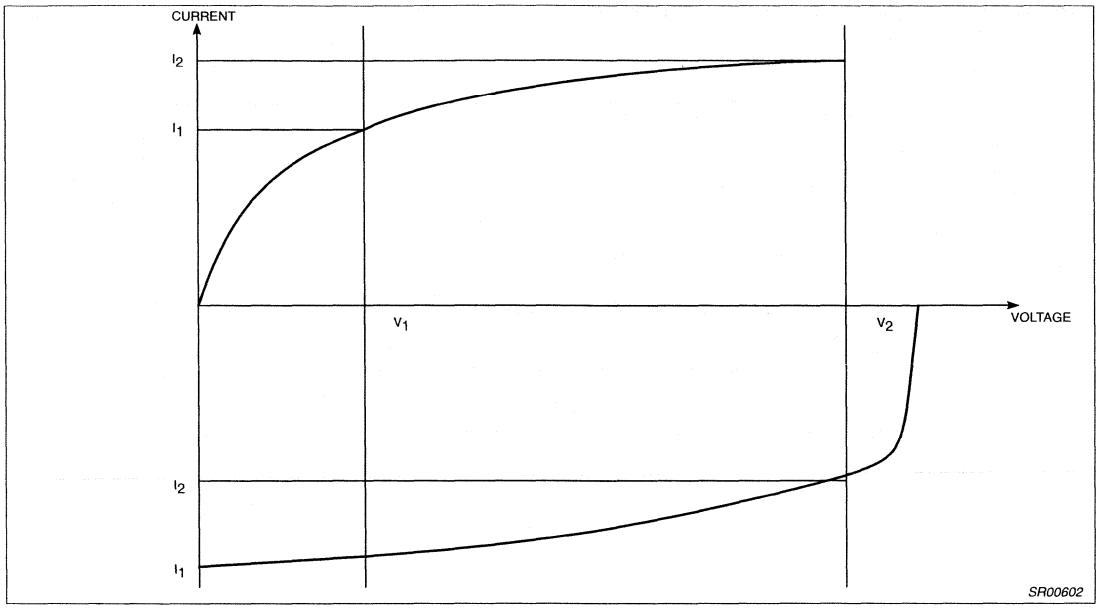


Figure 3. Output Current Definition

Functional Description Main Channel Synthesizer & Auxiliary Synthesizer

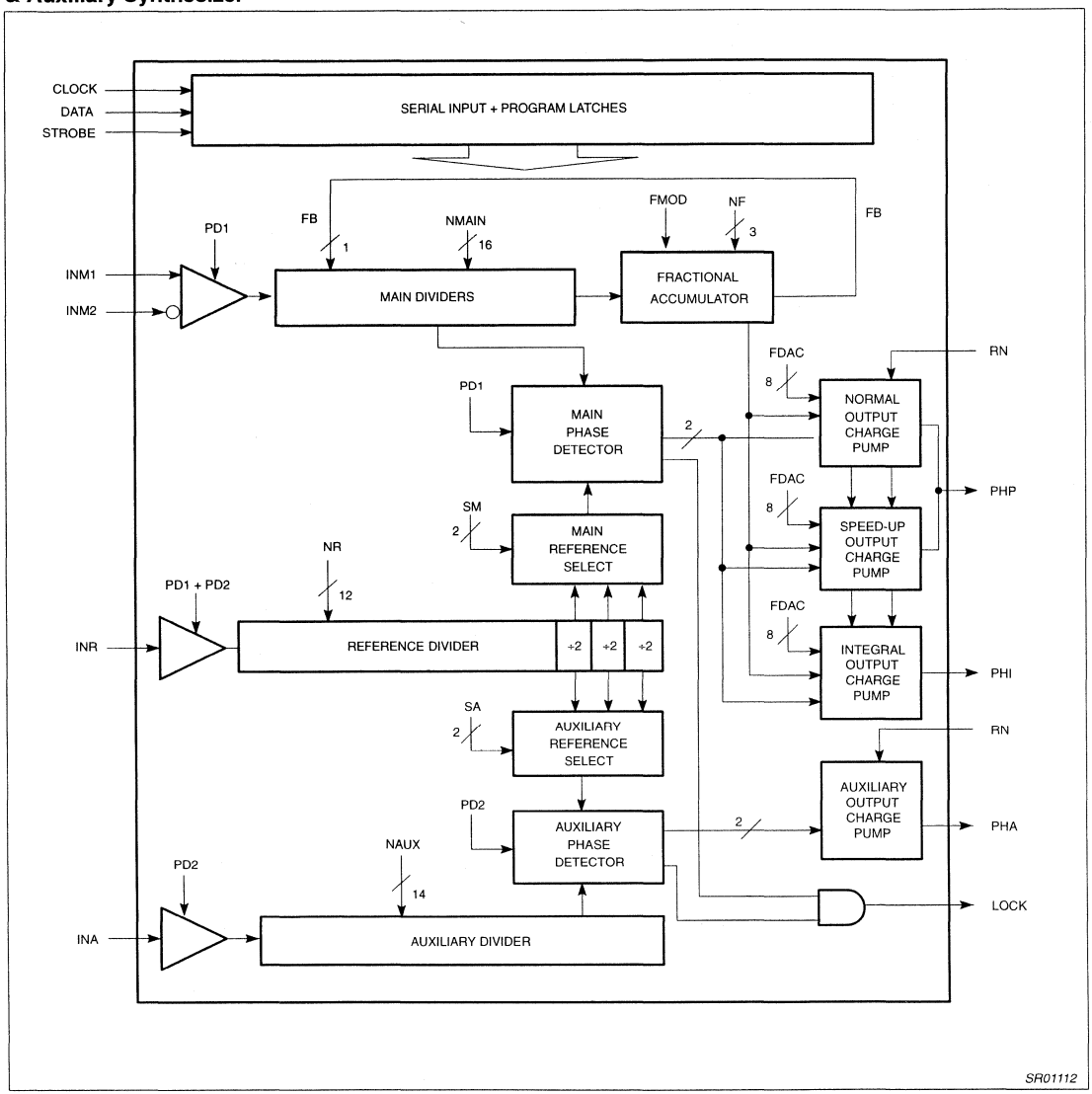


Figure 4. Synthesizer Block Diagram

Serial Programming Input

The serial input is a 3-wire input (CLOCK, DATA, STROBE) used to program all counter ratios, DACs, selection and enable bits. The programming data is structured into 24-bit words; each word includes 2 or 3 address bits. Figure [5] shows the timing diagram of the serial input. When STROBE = L, the clock driver is enabled and on positive edges of the CLOCK, the signal on DATA input is clocked into a shift register. When STROBE = H, the clock is disabled and the data in the shift register remains stable.

Depending on the 2 or 3 address bits, data is latched into different working or temporary registers. In order to fully program the synthesizer, 3 words must be sent: A, B and C. The D word programs all other functions within the SA9024. Those functions are

power control, ÷M (offset loop), SE (Tx offset loop synthesizer enable), DUAL mode, Sleep Mode 1 and Sleep Mode 2.

The data for FDAC is stored by the B word into a temporary register. When the A word is loaded, the data in this temporary register is loaded together with the A word into the work registers to avoid false temporary main synthesizer output caused by changes in fractional compensation.

The A word contains new data for the main divider. The A word is loaded into the working registers only when a main divider synchronization signal is active to avoid phase jumps when reprogramming the main divider. The synchronization pulse is generated by the main divider when it has reached its terminal count, at which time a main divider output pulse is also sent to the main phase detector. This disables the loading of the A word each main divider cycle during maximum of (NREF / f_{REF}) seconds. Therefore, to be sure that the A word will be correctly loaded, the STROBE signal must be high for at least (NREF / f_{REF}) seconds. When programming the A word, the main charge pumps on output PHP and PHI are set into the speed–up mode as soon as the A word is latched into the working registers and remain so as long as STROBE is held high.

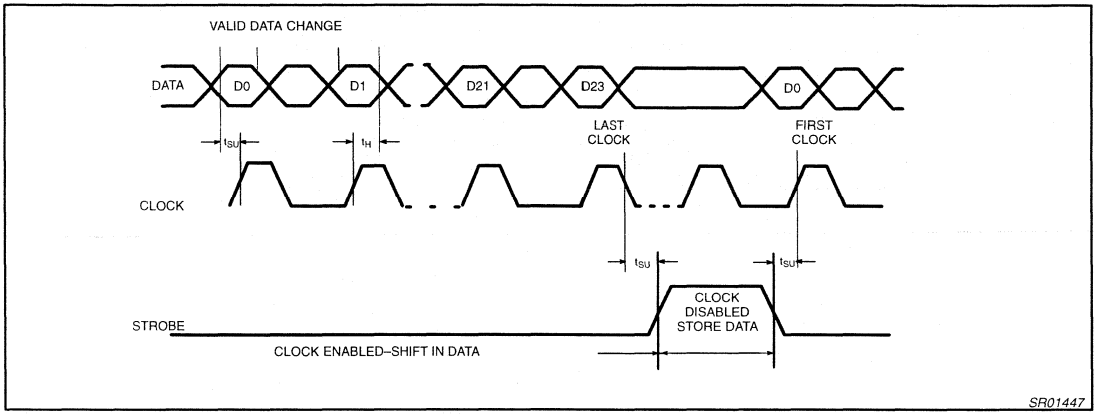


Figure 5. Serial Input Timing Sequence

Table 1. Function Table

Symbol	Bits	Function
FMOD	1	Fractional-N modulus selection flag: '0' = modulo 8 '1' = modulo 5
NF	3	Fractional-N increment
NMAIN	16	Main divider ratio; 512 to 65,535 allowed
NREF	10	Reference divider ratio; 4 to 1,023 allowed, RSM, RSA = "0 0"
RSM	2	Reference select for main phase detector
RSA	2	Reference select for auxiliary phase detector
FDAC	8	Fractional compensation charge pump current DAC
NAUX	14	Auxiliary divider ratio; 128 to 16,384 allowed
CP	2	Charge pump current ratio select (see table 1)
LD	2	Lock detect output select (see table 2)
PD1	1	PD1 = 0 for power down; shuts off power to main divider and main chargepumps, anded with PD2 to turn off ref. divider.
PD2	1	PD2 = 0 for power down; shuts off power to auxiliary divider, and auxiliary charge pumps; anded with PD1 to turn off ref. divider.
PC	8	Power control (see note 3)
M	2	÷M, M = 6, 7, 8, 9 (see note 4)
SE	1	Transmit offset synthesizer on/off
TM	1	Transmit mode: '0' = DUAL
AD	1	Mode control, 1 = digital; 0 = analog
SM1	1	Sleep mode 1
SM2	1	Sleep mode 2

1. Data bits are shifted in on the the leading clock edge, with the least significant bit (LSB) first and the most significant bit (MSB) last.
2. On the rising edge of the strobe and with the address decoder output = 1, the contents of the input shift register are transferred to the working registers. The strobe rising edge comes one half clock period after the clock edge on which the MSB of a word is shifted in.
3. The PC bits are used for the power control function. Eight (8) bits of data allows for appropriate resolution of the power control. 00000000 = 0 dB: 11111111 = –45.9 dB (= 255 ∠ 0.18).
4. The M bits are used to program the ÷M counter for integer values between 6 and 9. 00 = 6, 01 = 7, 10 = 8, 11 = 9.
5. The TM bit is used to put the SA9024 into DUAL mode operation. In DUAL mode (TM = 0).
6. The AD bit allows a reduction in the linearity of the DUAL output driver while in AMPS mode.
7. The SM1 bit is used to shut down the TX_{LO} buffers. SM1 = 1, buffers on; SM1 = 0, buffers off.
8. The SM2 bit is used to shut down the RCLK buffer. SM2 = 1, buffer on; SM2 = 0, buffer off.
9. The SE bit turns on and off the offset loop synthesizer circuits. SE = 1, synthesizer on; SE = 0, synthesizer off.
10. The LOCK bits determine what signal is present on the LOCK pin as follows:

Table 2.

Lock Detect Output Select*	
LOCK	**LOCK Pin Function**
00	Main, auxiliary and offset lock condition
01	Main and auxiliary lock condition
10	Main lock detect condition
11	Auxiliary lock condition

*When a section is in power down mode, the lock indicator for that section is high.

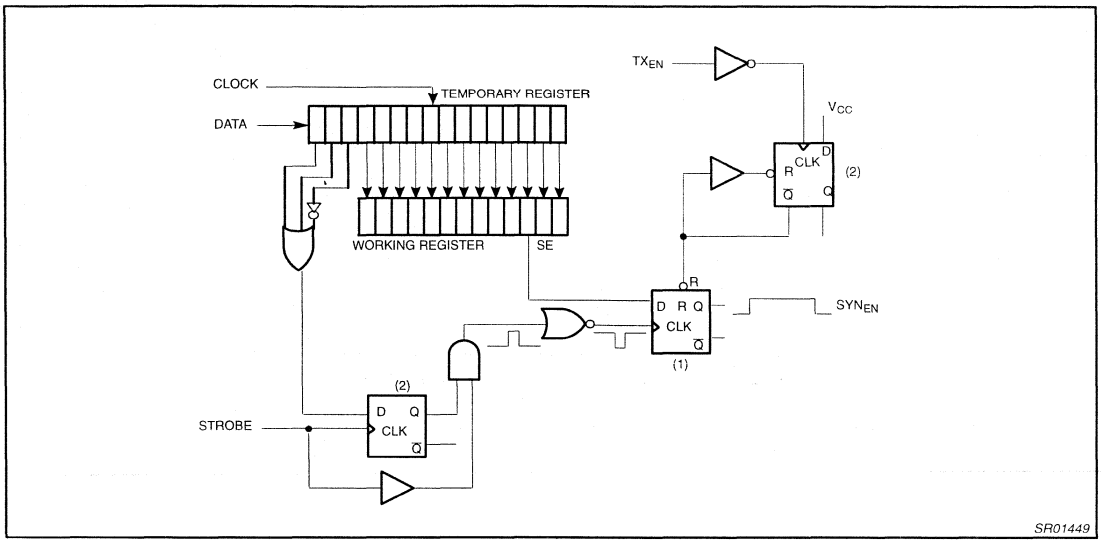


Figure 6. Transmit Offset Synthesizer Reset Circuit

In Figure 6, the falling edge of the strobe and address, inverted, toggles the Q output of flip-flop (1) to a '1' state, enabling the phase detector, VCO, divide by M, TX_{IF} buffer and SSB up-converter. Approximately 80µs after the synthesizer is locked, the TX_{EN} signal (enabled = 1) turns on the modulator and variable gain amplifier. The rising edge of TX_{EN} has no effect on SYN_{EN}, however, the falling (rising inverted) edge toggles the $\overline{Q}$ output of D flip-flop (2) to a '0' state. This disables the synthesizer, modulator and variable gain amplifier. To insure that slow edges on TX_{EN} do not cause improper operation, the TX_{EN} is a Schmitt trigger design.

The address decoder for program word 'D' ANDed together with the strobe is used to load the contents of the temporary register into the working registers. D flip-flop (3) is used to prevent multiple strobe and address pulses in the event the address decoder output toggles on garbage bits during the time the strobe remains in a '1' state.

The temporary register is common to the transmit offset synthesizer, main channel synthesizer and auxiliary synthesizer.

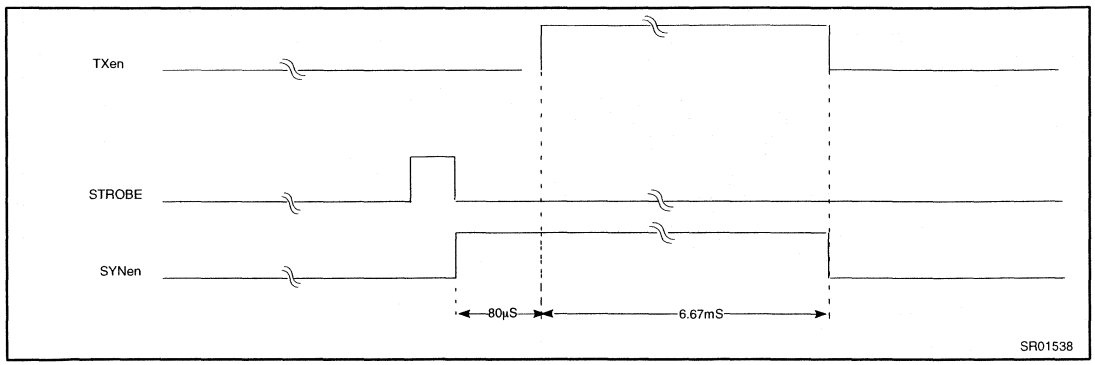


Figure 7. Transmit Offset Synthesizer Timing Diagram

Data format

Format of programmed data

LAST IN		MSB	SERIAL PROGRAMMING FORMAT				FIRST IN LSB
p23	p22	p21	p20	../..	../..	p1	p0

A word, length 24 bits

Last in					MSB														LSB	First IN	
Address		fmod	Fractional–N		Main Divider ratio– Nmain															Spare	
0	0	Fmod	NF2	NF1	NF0	N15	N14	N13	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	N0	sk1	sk2
Default:		0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	1	0	0	0	0	0	0

A word select	Fixed to 00.
Fractional Modulus select	FM 0=modulo 8, 1=modulo 5.
Fractional–N Increment	NF2..0 Fractional N Increment values 000 to 111.
N–Divider	N0..N15, Main divider values 512 to 65535 allowed for divider ratio.

B word, length 24 bits

ADDRESS		REFERENCE DIVIDER NREF										RSM		RSA		FRACTIONAL COMPENSATION DAC							
0	1	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	RSM 1	RSM 0	RSA 1	RSA 0	Fdac 7	Fdac 6	Fdac 5	Fdac 4	Fdac 3	Fdac 2	Fdac 1	Fdac 0
Default:		0	0	0	1	0	1	0	0	0	1	0	0	0	0	x	x	x	x	x	x	x	x

B word select	Fixed to 01
R–Divider	R0..R9, Reference divider values 4 to 1023 allowed for divider ration.
Charge pump current Ratio	CP1, CP0: Charge pump current ratio, see table of charge pump currents.
Main comparison select	RSM Comparison divider select for main phase detector.
Aux comparison select	RSA Comparison divider select for auxiliary phase detector.
Fractional Compensation	Fdac7..0, Fractional compensation charge pump current DAC, values 0 to 255. FDAC = 77 for best op MOD8.

C word, length 24 bits

ADDRESS		AUXILIARY DIVIDER NAUX													CP		LOCK		PD		SPARE	
1	0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	CP1	CP0	LD1	LD0	PD1	PD2	PD3	LOD
Default		0	0	0	0	0	1	1	1	0	0	1	0	1	0	1	1	0	0	TX_{EN}	TX_{EN}	0	0

C word select	Fixed to 10
A–Divider	A0..A13, Auxiliary divider values 128 to 16384 allowed for divider ratio.
Charge pump current Ratio	CP1, CP0: Charge pump current ratio, see table fo charge pump currents.
Lock detect output	LD1 LD0 0 0 Combined main, aux. & offset loop lock detect signal present at the LOCK pin. 0 1 Combined main and aux. lock detect signal present at the LOCK pin. 1 0 Main lock detect signal present at the LOCK pin. 1 1 Auxiliary loop lock detect signal present at the LOCK pin. When a section is in power down mode, the lock indicator for that section is high.
Power down	PD1=1: power to N–divider, reference divider, main charge pumps, PD1=0 to power down. PD2=1: power to Aux divider, reference divider, Aux charge pump, PD2=0 to power down.

Table 3.
Main and auxiliary chargepump currents

CP1	CP0	I_{PHA}	I_{PHP}	I_{PHP-SU}	I_{PHI_SU}
0	0	1.5xIset	3xIset	15xIset	36xIset
0	1	0.5xIset	1xIset	5xIset	12xIset
1	0	1.5xIset	3xIset	15xIset	0
1	1	0.5xIset	1xIset	5xIset	0

NOTES
1. I_{SET} = Vset/RN; bias current for charge pumps.
2. CP1 is used to disable the PHI pump.
3. Iphp_su is the total current out of PHP in speedup mode.

D word, length 24 bits

Address			Power Control								M divider		SE	TM	AD	Sleep Mode		Test pa_current					
1	1	0	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	M1	M0	SE	TM	AD	SM1	SM2	pai5	pai4	pai3	pai2	pai1	pai0
Default:			x	x	x	x	x	x	x	x	0	0	0	0	0	0	0	0	0	0	0	0	0
D0 word select			Fixed to 110.																				
Output Power Control			PC7(msb)...PC0(lsb) Provides output power attenuation for DUAL mode amplifier outputs in 0.18 dB steps, Fx = 45.9 dB.																				
M Divider			00 = 6, 01 = 7, 10 = 8, 11 = 9																				
Offset loop power down			SE Offset loop synthesizer power down, SE = 1 power on, SE = 0 power down (sleep mode).																				
DUAL mode select			TM = 0 DUALmode																				
AMPS/DAMPS mode select			AD = 1 DAMPS mode. AD = 0 AMPs mode																				
TX buffers power down			SM1 TX Local oscillator buffers power down. SM1 = 1 power on, SM1 = 0 to power down. SM2 RCLK buffer power down. SM2 = 1 power on, SM2 = 0 to power down.																				
Test: pa_current:pai			TX test bits for controlling the current in the power amp. Should be 0 during normal operation.																				

MODES OF OPERATION

There are two power saving modes of operation which the circuit can be put into, dependent on the status of the system. The intention of these different modes is to disable circuitry that is not in use at the time in order to reduce power consumption. During sleep mode, only circuitry which is required to provide a master clock to the digital portion of the system is enabled. During receive mode, circuitry which is used to perform the receive function and provide a master clock is enabled. In transmit mode all the functions of the circuit are enabled which are required to perform transmit, receive and provide master clock. When the circuit is powered for the first time, it is in DUAL MODE SLEEP.

Mode Programming

Mode	Dual Mode AMPS			
Mode Setting and BlockStatus (X = ON)	**Sleep**	**RX**	**TX**	**Logic**
TX_{EN}	0	0	1	
PD1	0	1	1	
PD2	0	1	1	
SE–>SYNen	0	0	1	
TM	0	0	0	
SM1	0	0	1	
SM2	0	1	1	
Main loop, Ndivider, RXLO buffer		X	X	PD1
Aux loop, Adivider		X	X	PD2
Rdivider		X	X	PD1 .OR. PD2
Offset VCO, Mdivider			X	SE (+delay) See $SE–>SYN_{EN}$ diagram
RCL buffer		X	X	SM2
MCL buffer, reference input	X	X	X	1 (always ON)
$DUAL_{TX}$ PA			X	(.not. TM) .and. TX_{EN} .and. SM1
TXLO buffer, SSB up–converter			X	SM1
I/Q MODULATOR, VGA			X	TXEN .AND. SM1
Control Logic	X	X	X	1 (always ON)

Main Divider

The input signal on RX_{LO} is amplified to a logic level by a balanced input comparator giving a common mode rejection. This input stage is enabled by serial control bit PD1 = 1. Disabling means that all currents in the comparator are switched off. The main divider is built up to be a 16-bit counter.

The loading of the work registers FMOD, NF and NMAIN is synchronized with the state of the main counter to avoid extra phase disturbance when switching over to another main divider ratio as is explained in the Serial Programming Input chapter.

At the completion of a main divider cycle, a main divider output pulse is generated which will drive the main phase comparator. Also, the fractional accumulator is incremented with NF. The accumulator works modulo Q. Q is preset by the serial control bit FMOD to 8 when FMOD = '0'. Each time the accumulator overflows, the total divide ratio will be NMAIN + 1 for the next cycle. The mean division ratio over Q main divider cycles will then be:

$$NQ = NMAIN + \frac{NF}{Q}$$

Synchronization is provided to avoid a random phase on the phase detector upon the loading of a new ratio and when powering up the loop.

Auxiliary Divider

The input signal on INA is amplified to logic level by a single-ended input buffer, which accepts low level AC-coupled input signals. This input stage is enabled if the serial control bit PD2 = '1'. Disabling means that all currents in the buffer and prescaler are switched off. The auxiliary divider is programmed with 14 bits and has continuous integer division ratios over the range of 128 to 16,384.

Reference Divider (Figure 8)

The input can be driven by a differential crystal input or an external TCXO. This input stage is enabled by the OR function of the serial input bits PD1 and PD2. Disabling means that all currents are switched off. The reference divider consists of a programmable divide by N_{REF} (N_{REF} = 4 to 1,023) followed by a 3-bit binary counter. The 2 bit SM determines which of the four output pulses is selected as the main phase detector signal. To obtain the best time spacing for the main and auxiliary reference signals, a different output will be used for the auxiliary phase detector, reducing the possibility of unwanted interactions.

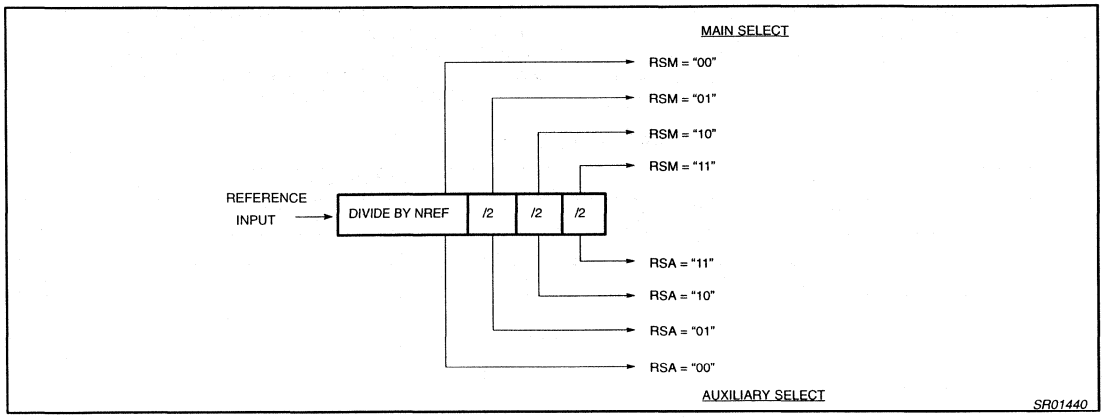


Figure 8. Reference Variable Divider

Phase Detectors (Figure 9)

The auxiliary and main phase detectors each consist of a 2 D-type flip-flop phase and frequency detector. Each flip-flop is set by the negative edge of the divider terminal count output pulse. The reset inputs are activated after a delay when both flip-flops have been set. This avoids non-linearity or dead-band around zero phase error. The flip-flops drive on-chip charge pumps. A pull-up current from the charge pump indicates the VCO frequency shall be increased while a pull-down pulse indicates the VCO frequency shall be decreased.

Current Settings

The IC has two current setting pins, RN and I_{PEAK}. The active charge pump currents and the fractional compensation currents are linearly dependent on the current in the current setting pins. This current, I_{SET}, is set by an external resistor connected between the current setting pin and V_{SS}.

Auxiliary Output Charge Pumps

The auxiliary charge pumps on pin PHA are driven by the auxiliary phase detector and the current value is determined by the external resistor attached to pin RN.

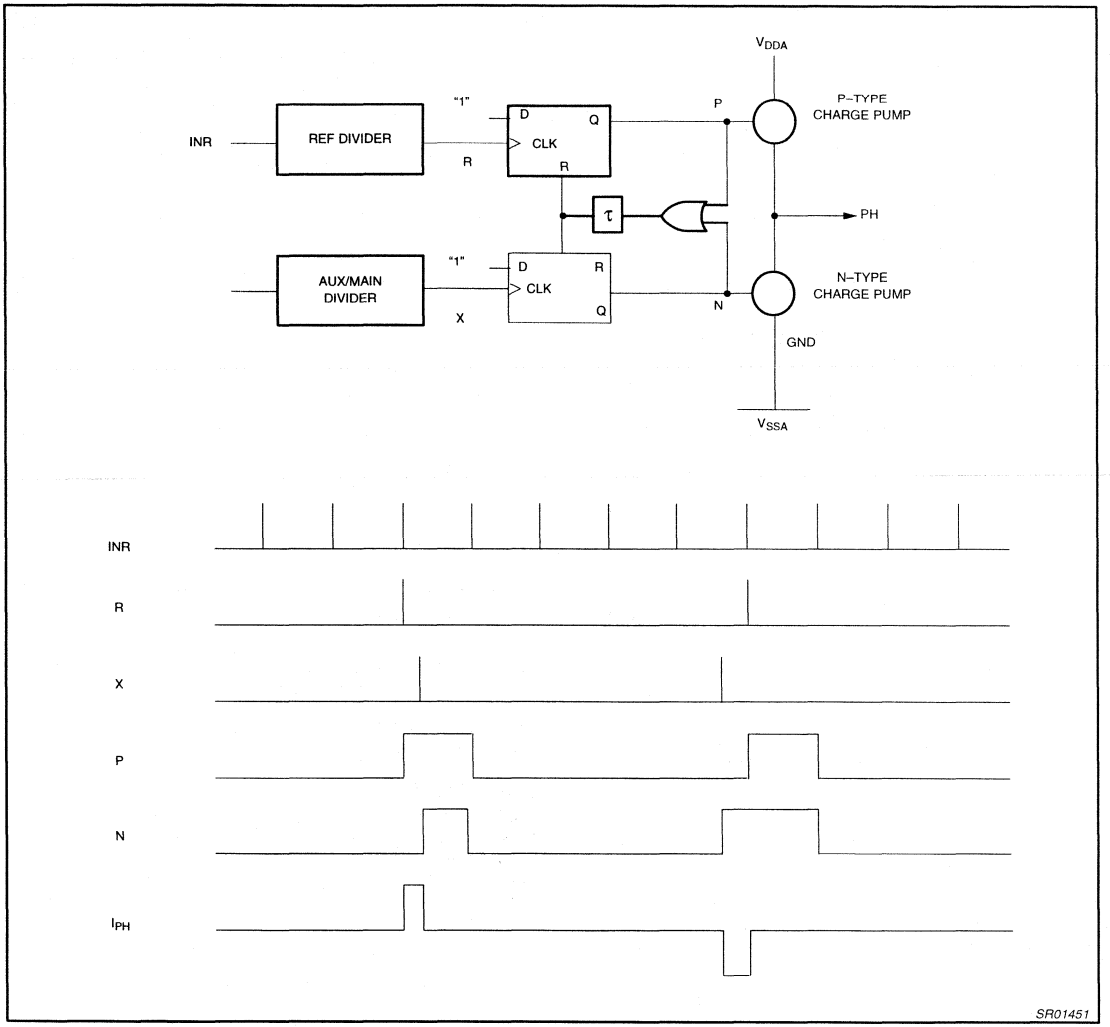


Figure 9. Phase Detector Structure With Timing

Main Output Charge Pumps and Fractional Compensation Currents

The main charge pumps on pin PHP and PHI are driven by the main phase detector. The current value is determined by the current at pin RN. The fractional compensation current is linearly dependent on the main charge pump current and its level relative to the main charge pumps is set by an 8-bit programmable DAC. The timing for the fractional compensation is derived from the main divider. The current level based on the value of FRD, FDAC and I_{SET}. Figure 10 shows the waveforms (not to scale) for a typical base.

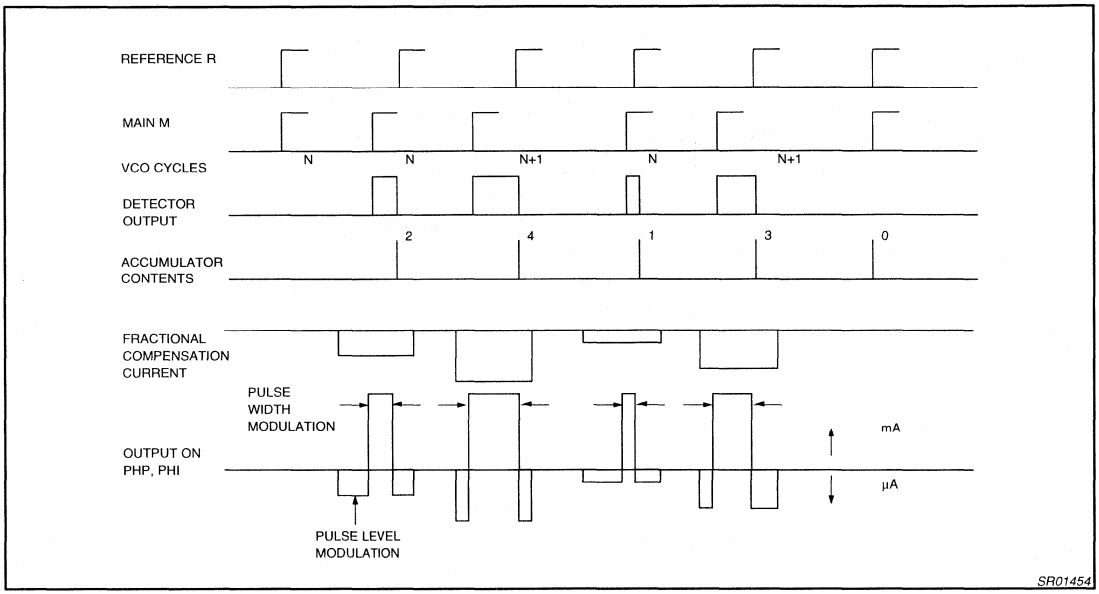


Figure 10. Waveforms for NF = 2; Fraction = 0.4

Figure 10 shows that for a proper fractional compensation, the area of the fractional compensation current pulse must be equal to the area of the charge pump ripple output.

The fractional compensation current is derived from the main charge pump in that it will follow all the current scaling through external resistor setting, programming or speedup operation.

For a given pump,

$$Icomp = \frac{Ipump}{128} \times \frac{Fdac}{5 \times 128} \times FRD$$

Where:
Icomp is the compensation current, Ipump is the pump current, Fdac is the fractional DAC value and FRD is the fractional accumulator value.

The theoretical value for Fdac would then be: 128 for Fmod = 1 (modulo 5) and 80 for Fmod = 0 (modulo 8).

When the serial input A word is loaded, the output circuits are in the "speedup mode" as long as the STROBE is H, otherwise the "normal mode" is active.

Lock Detect

The output LOCK maintains a logic '1' when the auxiliary phase detector ANDed with the main phase detector ANDed with Offset Phase Detector indicates a lock condition. During the Standby mode of operation when the offset loop is unlocked, (SYN_{EN} = low – see figure 6), the offset phase detector lock output is forced to an on (locked) state so that the lock detect will give an indication of receiver lock. The lock condition for the main and auxiliary synthesizers is defined as a phase difference of less than ±1 cycle on the reference input INR. The LOCK condition is also fulfilled when the relative counter is disabled (PD1 = '0' or PD2 = '0') for the main or auxiliary counter, respectively.

Functional Description of Offset Loop, Modulator and Power Control

Transmit Offset Synthesizer

The transmit offset phase locked loop portion of the SA9024 design consists of the following functional blocks: reference oscillator, limiters, phase detector, ÷M, IF VCO and passive loop filter. Harmonic contents of this signal are attenuated by an LP filter. The output of the IF VCO is also divided by N and compared with the reference oscillator in the phase detector.

Reference Oscillator

This Oscillator is used to generate the reference frequency together with an external crystal and varicap. The output is internally routed to three buffers and a phase comparator. It is possible to run the oscillator as an amplifier from an external reference signal (TCXO).

Phase Detector and Charge Pump

The phase comparator is used to compare the output of the divider with the reference. It provides an output proportional to the phase difference between the divided down VCO and the reference. This output is then filtered and used as the control voltage input to the VCO. The phase detector is a Gilbert multiplier cell type, having a linear output from 0 to π ($\pi/2 \pm \pi/2$), followed by a charge pump. The charge pump peak output current is programmable to 6.4mA via the use of an external resistor.

A preliminary design analysis has been performed with the following loop parameters:

A lock detect signal is provided and ANDed together with lock detect signals from both the main channel synthesizer and auxiliary synthesizer. While in standby mode, the lock detect signal will be forced to a valid lock state so that the lock detect signal will indicate when the main and auxiliary phase detectors have achieved phase lock.

Divide by M

The ÷M is a 2-bit programmable divider which can be configured for ney integer divide from 6 to 9. The divider is used to convert the VCO output down to the reference frequency before feeding it into the phase comparator.

VCO

This oscillator is used to generate the transmit IF frequency between 90MHz and 180MHz. The VCO tank is configured using a parallel inductor tuning varactor diode. DC blocking capacitors are used to isolate the varactor control voltage from the VCO tank DC bias voltages.

SSB Up-converter and TX_{IF} Buffer

The TX_{IF} buffer provides isolation between the SSB Up-converter and the VCO output. The Single Sideband Up-converter (SSB) is an active Gilbert cell multiplier (matched pair), combined with two quadrature phase shift networks and a low pass filter. The SSB up-converter is used to reject the unwanted upper sideband that would normally occur during the up-conversion process.

I/Q Modulator

The quadrature modulator is an active Gilbert cell multiplier (matched pair) with cross coupled outputs. These outputs are then provided to the variable gain amplifier. When the in-phase input I = cos (ωt) and the quadrature-phase input Q = sin (ωt) (i.e., Q lags I by 90°), the resulting output should be upper single sideband.

Variable Gain Amplifiers

The variable gain amplifiers are used to control the output level of the device, with a power control range of 45.9dB. The output stages are differential, matched from 200Ω to 50Ω.

Power Control

The power control range should be greater than or equal to 45.9dB, having a monotonically decreasing slope, with 0dB = +11.5 dBm nominal. Eight bits are available for power control programming. The top 6 bits (PC7 to PC2) provide coarse attenuation with .6dB step size accuracy. The bottom 2 bits provide fine attenuation with .18 dB step size accuracy.

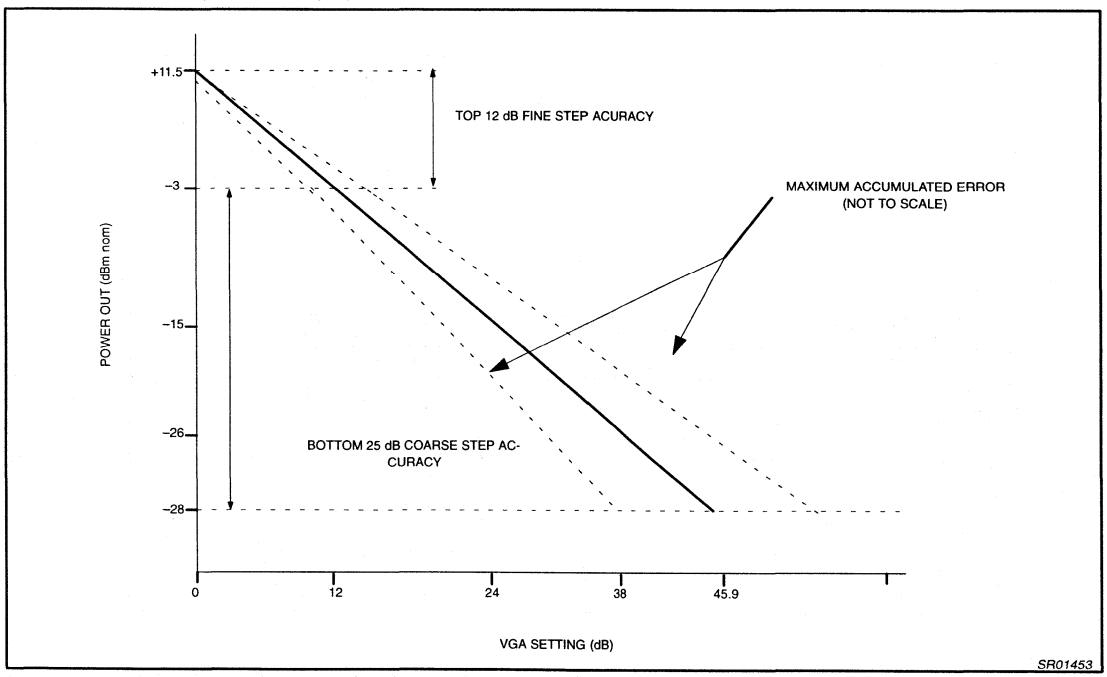


Figure 11. Power Control

Oscillator Buffers

There are three buffers for the reference signal, two of which are used to provide external reference signals. The internal reference signal is used for the main and auxiliary synthesizer reference. The second buffer (MCLK) is used as a master clock for external digital circuitry which is always on, while the third buffer (RCLK) is used as a clock for external digital circuitry which is not used in sleep mode.

LO Buffers

The LO buffers are used to provide isolation for the VCO and between the transmitter up-converter and channel synthesizer.

900 MHz transmit modulator and 2.2 GHz fractional–N synthesizer

SA9025

DESCRIPTION

This specification defines the requirements for a transmitter modulator and fractional–N synthesizer IC to be used in cellular telephones which employ the North American Dual Mode Cellular System (IS–136).

FEATURES

- Low current from 3.75V supply
- Low phase noise
- Main loop with internal charge pump and fractional compensation
- 3–line serial interface bus
- Power down for the synthesizers
- Speedup mode for faster switching

APPLICATIONS

- Cellular phones
- Portable battery–powered radio equipment.

GENERAL DESCRIPTION

The SA9025 BICMOS device integrates:

- Main channel synthesizer
- Auxiliary synthesizer
- Transmit offset synthesizer and oscillator
- I/Q modulator
- Power control
- Reference and clock buffers
- Control logic for programming and power down modes

PIN CONFIGURATION

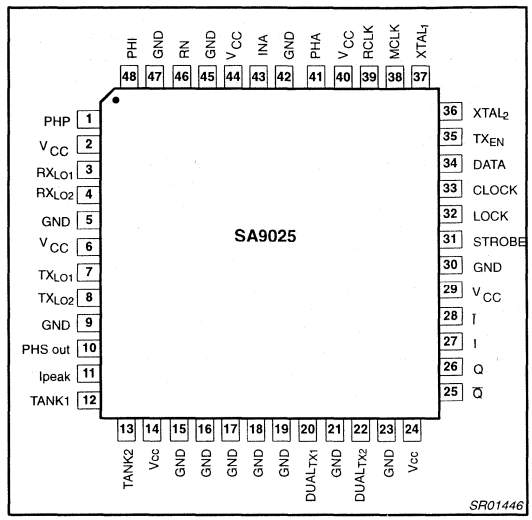


Figure 1. Pin Configuration

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply voltage	V_{CC}	3.6	3.75	3.9	V
I_{CC}	Supply current		–	TBD	–	mA
I_{CC_save}	Total supply current in power–down mode		–	TBD	–	mA
f_{VCO}	Input frequency		800	–	2200	MHz
f_{AUX}	Input frequency		10	–	500	MHz
f_{XTAL}	Crystal reference input frequency		10	–	40	MHz
f_{PC}	Maximum phase comparator frequency	Main and Aux loops	–	–	5	MHz
T_{amb}	Operating ambient temperature		–40	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SA9025	LQFP48	Plastic low profile quad flat package; 48 leads; body 7x7x1.4 mm	SOT313-2

CONNECTIONS

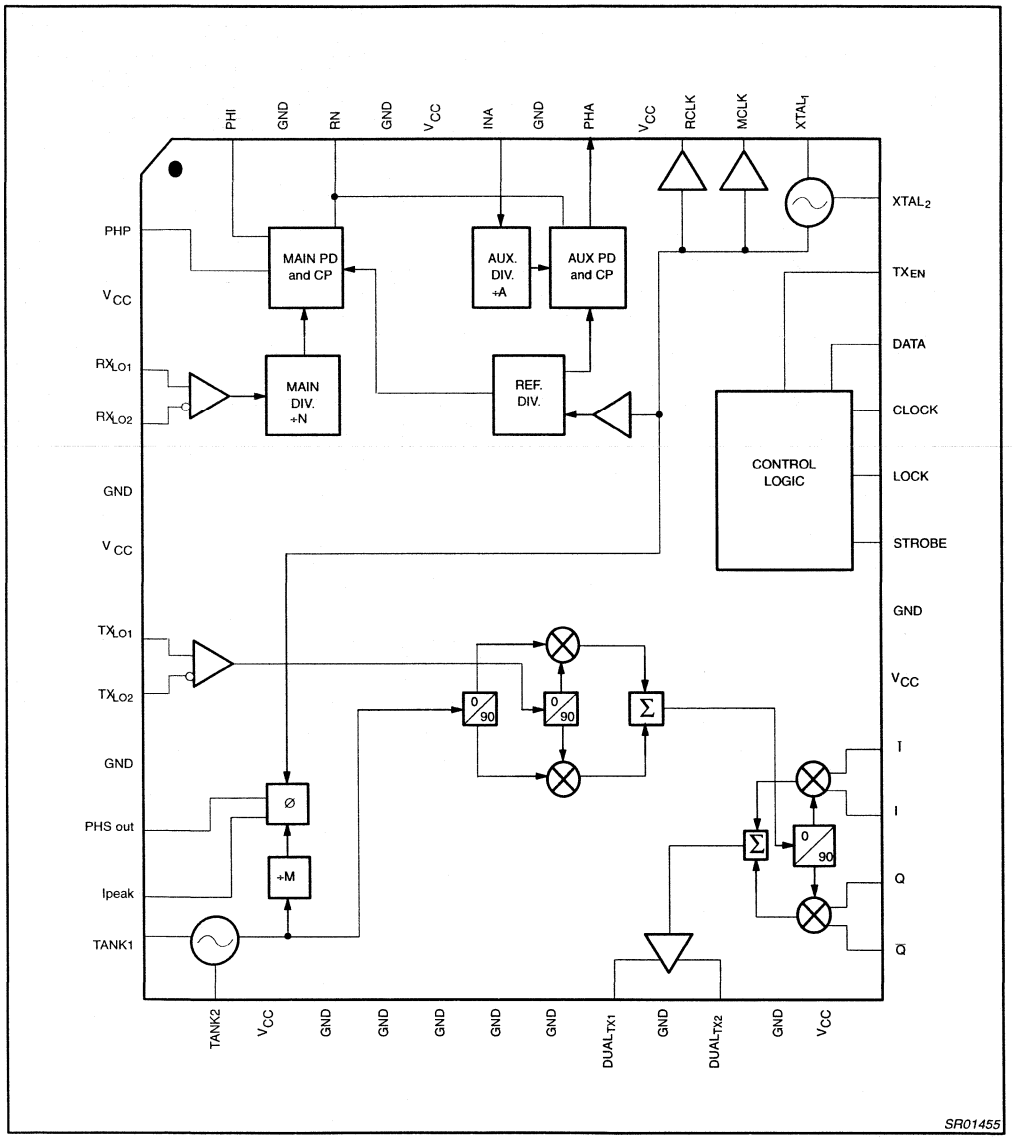


Figure 2. SA9025 Block Diagram

PIN DESCRIPTIONS

PIN NO.	PIN	DESCRIPTION
1	PHP	Proportional charge pump output
2	V_{CC}	Digital supply voltage
3	RX_{LO1}	Differential LO input
4	RX_{LO2}	Differential LO input
5	GND	Digital Ground
6	V_{CC}	Tank supply voltage
7	TX_{LO1}	Differential Transmit LO Input
8	TX_{LO2}	Differential Transmit LO Input
9	GND	Tank Ground
10	PHS OUT	Charge pump output (transmit offset)
11	I_{PEAK}	PHS out current set resistor
12	TANK1	VCO differential tank
13	TANK2	VCO differential tank
14	V_{CC}	Tx supply voltage
15	GND	Tx Ground
16	GND	Tx Ground
17	GND	Tx Ground
18	GND	Tx Ground
19	GND	Tx Ground
20	DUALTX1	Dual mode RF output
21	GND	Tx Ground
22	DUALTX2	Dual mode RF output
23	GND	Tx Ground
24	V_{CC}	Tx supply voltage
25	$\overline{Q}$	Inverting quadrature input
26	Q	Non–Inverting quadrature input
27	$\overline{I}$	Non–inverting in phase modulation input
28	I	Inverting in phase modulation input
29	V_{CC}	Tx supply voltage
30	GND	Tx Ground
31	STROBE	Data input latch enable
32	LOCK	Lock detect
33	CLOCK	Serial clock input
34	DATA	Serial data input
35	TX_{EN}	Transmit enable
36	$XTAL_2$	Crystal Oscillator emitter input
37	$XTAL_1$	Crystal Oscillator base Input
38	MCLK	Buffered oscillator output
39	RCLK	Buffered oscillator output
40	V_{CC}	REF supply voltage
41	PHA	Auxiliary charge pump output
42	GND	REF Ground
43	INA	RX_{IF} input
44	V_{CC}	CP supply voltage
45	GND	CP Ground
46	RN	CP current set resistor
47	GND	CP Ground
48	PHI	Integral charge pump output

OPERATING MODES & POWER DOWN CONTROL

There are two power saving modes of operation which the SA9025 can be put into, dependent on the status of the system. The intention of these different modes is to disable circuity that is not in use at the time in order to reduce power consumption. During sleep mode, only circuitry which is required to provide a master clock to the digital portion of the system is enabled. During receive mode, circuitry which is used to perform the receive function and provide a master clock is enabled. In transmit mode all the functions of the chip are enabled which are required to perform transmit, receive and provide master clock.

SA9025 POWER MODE TRUTH TABLE

	Sleep Mode		Receive Mode		Transmit Mode	
Enabled	yes	no	yes	no	yes	no
Crystal Oscillator	✓		✓		✓	
Phase detector and charge pump (transmit offset)		✓		✓	✓	
VCO		✓		✓	✓	
SSB Up-converter		✓		✓	✓	
MCLK Buffer	✓		✓		✓	
RCLK Buffer		✓	✓		✓	
÷M offset loop divider		✓		✓	✓	
TX_{LO} Buffer		✓		✓	✓	
RX_{LO} Buffer		✓	✓		✓	
I/Q Modulator		✓		✓	✓	
Variable Gain Amp.		✓		✓	✓	
Control Logic	✓		✓		✓	
Main Divider		✓	✓		✓	
Reference Divider		✓	✓		✓	
Auxiliary Divider		✓	✓		✓	
Main Phase Detector and charge pump		✓	✓		✓	
Auxiliary Phase Detector and charge pump		✓	✓		✓	
Lock Detect		✓	✓		✓	

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	VALUE		UNIT
		MIN.	MAX.	
V_{CC}	Supply voltage	-0.3	+4.5	V
V_{IN}	Voltage applied to any other pin	-0.3	V_{CC}+0.3	V
P_N	Power dissipation, T_A = 25°C (still air)		980	mW
T_{JMAX}	Operation junction temperature		TBD	°C
P_{MAX}	Power input/output		+10/+14	dBm
I_{MAX}	DC current into any I/O pin	-10	+10	mA
T_{STG}	Storage temperature	–65	+150	°C
T_o	Operating temperature	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3.75 V; T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{CC}	Power supply range		3.6	3.75	3.9	V
I_{CC}	Supply current	Sleep mode		2		mA
		Standby mode		17		
		Operating: full power analog		95		
		Operating: full power digital DUAL[1]		52		
I / $\overline{I}$	In-phase differential input	quiescent		V_{CC} /2		V
Q / $\overline{Q}$	Quadrature phase differential input	quiescent		V_{CC} /2		V
V_{IL}	Clock, Data, Strobe, TX_{EN}	Input logic low	–0.3		0.3 × V_{CC}	V
V_{IH}	Clock, data, strobe, TX_{EN}	Input logic high	0.7 × V_{CC}		V_{CC}+0.3	V
T_A	Ambient temperature range		-40	+25	+85	°C
Digital Outputs Lock						
V_{OL}	Output voltage LOW	I_O = 2mA			0.4	V
V_{OH}	Output voltage HIGH	I_O = -2mA	V_{CC} – 0.4			V
Charge Pump Current Setting Resistor Input; RN, R_{Ipeak}						
RN	External resistor to ground		6	7.5	24	kΩ
R_{Ipeak}	External resistor to ground			4.7		kΩ
V_{RN}	Regulated voltage	RN = 7.5 kΩ		1.23		V
V_{Ipeak}	Regulated voltage	R_{ipeak} = 4.7 kΩ		1.3		V
I_{peak}	PHSOUT programming	R_{ipeak} = 4.7 kΩ		0.26		mA
PHS_{gain}	PHSOUT gain	R_{ipeak} = 4.7 kΩ		24xI_{peak}		mA
Kϕ	PD phase gain	Transmit offset PLL in phase lock		4.33		mA/rad
Charge Pump Outputs (including fractional compensation pump, not PHS) RN = 7.5 kΩ						
I_{OPH}	Charge pump output current error versus expected current.		–15		15	%
I_{MATCH}	Sink to source current matching	V_{PHX} = V_{CC}/2	–5		5	%
	Current output variation versus V_{PHX}	V_{PHX} in compliance range	–10		10	%
	Charge pump off, leakage current	V_{PHX} = V_{CC}/2	–10	±1	10	nA
V_{PH}	Charge pump voltage compliance[3]		0.7		V_{CC} – 0.8	V
Charge Pump Outputs (only PHS) R_{ipeak} = 4.7 kΩ						
I_{OPH}	Charge pump output current error versus expected current.		–15		15	%
I_{MATCH}	Sink to source current matching	V_{PHS} = V_{CC}/2	–10		10	%

	Current output variation versus V_{PH}	V_{PHS} in compliance range	–25		25	%
V_{PH}	Charge pump voltage compliance		0.5		V_{CC}–0.5	V

AC ELECTRICAL CHARACTERISTICS

V_{CC} = +3.75 V; T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Modulator						
$TX_{LO\ 1/2}$	Transmit LO input (AC-coupled; 50Ω single-ended, 100Ω differential)	Input power Frequency range	-13 900		-10 1100	dBm MHz
VSWR				2:1		
TANK1/2	VCO tank differential inputs	Frequency range	90		180	MHz
÷M	PLL offset divider	Maximum input frequency	180			MHz
$XTAL_1$	Osc. transistor base	Osc. frequency	10		40	MHz
$XTAL_2$	Osc. transistor emitter	Osc. frequency	10		40	MHz
XO	Negative resistance			–100		Ω
RCLK, MCLK	Reference buffer output Frequency range Output levels Harmonic content	Z_{LOAD} = 5kΩ| | 7 pF	 10 0.7	 1.0	 40 1.4 –10	 MHz V_{P-P} dBc
TX_{EN}	Transmit enable	Transmit enable Transmit disable		TX_{EN} = 1 TX_{EN} = 0		Logic
Q / $\overline{Q}$ I / $\overline{I}$	Baseband in-phase differential inputs	Maximum frequency Diff. mod. level Diff. input impedance DC bias point	1.8 0.8 10.0 1.8	 0.9 V_{CC}/2	 1.0 2.55	MHz V_{P-P} kΩ V
TX_{RF}	TX_{RF} operating range		820		920	MHz
$DUAL_{TX}$	DUAL output SE=1, TX_{EN}=1 (with external matching) (50Ω)	AMPS/DAMPS	820		853	MHz
$DUAL_{TX}$	Differential output, ($DUAL_{TX}$) open-collector, matched to 200Ω differential impedance	Output level (avg. min., I and Q quad., 0dB VGA) Gain flatness	+9.0	+11.0 1	+13.0	dBm dB
$DUAL_{TX}$	Linearity worst case intermod. products (0dB VGA OR +9 dBm, whichever is less, I & Q in-phase)	3rd-order 5th-order 7th-order		-42 -55 -65	-34 -45 -53	dBc
$DUAL_{TX}$	Carrier suppression (I & Q in quadrature)	VGA = 0dB VGA = -38dB		-45 -33	-35	dBc
$DUAL_{TX}$	Sideband suppression (I & Q in quadrature)			-45	-35	dBc
$DUAL_{TX}$	Spurious output	2 to 284 MHz			-45	dBc
		824 to 849 MHz			-47	
		849 to 869 MHz			-45	
		869 to 894 MHz			-104	dBm
		894 to 8490 MHz			-45	dBc
$DUAL_{TX}$	TX_{LO} up-conversion products	TX_{LO}			-21	dBc
		Upper Side Band			-21	
		TX_{LO} ±3 × TX_{OFFSET}			-36	
		Harmonics ≤ 10th			-21	
$DUAL_{TX}$	Broad-band noise (0dB VGA or +9 dBm, whichever is less)	869 to 894 MHz			-123	dBm/Hz
$DUAL_{TX}$	Adjacent channel noise power	@ 30 kHz			-95	dBc/Hz
$DUAL_{TX}$	Alternate channel noise power	@ 60 kHz			–101	dBc/Hz

Synthesizer						
Main Divider						
f_{MMAX}	Input frequency range		800		2200	MHz
	Input harmonics	No multi–clocking	–10			dBc
$RX_{LO\ 1/2}$	Synthesizer LO input (AC-coupled; external shunt 50Ω single-ended, 100Ω differential)	Input power	–20		0	dBm
Reference Divider						
f_{RMAX}	Input frequency RANGE		10		40	MHz
	Input harmonics	No multi–clocking	–10			dBc
Auxiliary Divider						
f_{AMAX}	Input frequency RANGE		10		500	MHz
	Input harmonics	No multi–clocking	–10			dBc
V_{INA}	Input signal amplitude		0.200			V_{P-P}
Serial Interface						
f_{CLOCK}	Clock frequency				10	MHz
t_{SU}	Set-up time: DATA to CLOCK, CLOCK to STROBE		30			ns
t_H	Hold time: CLOCK to DATA		30			ns
t_{SW}	Pulse width	CLOCK	30			ns
		STROBE (B - D words)	30			
		A word	$\frac{1}{f_{REF} \cdot NREF} + t_W$			

1. Transmit mode @ 33% duty cycle.
2. The relative output current variation is defined thus:
   $\Delta I_{out}/I_{out} = 2x(I_2 - I_1)/I(I_2 + I_1)I$; with V_1=0.7V, $V_2 = V_{CC}$–0.8V (see figure 3)
3. Power supply current measured with $f_{RX\ =\ 2100.54\ MHZ}$, f_{REF} = 19.44 MHz, f_{INA}= 109.92 MHz, main phase detector bias resistor = 7.5 kΩ. Main phase detector reference frequency = 240 kHz, auxiliary phase detector frequency = 240 kHz.
4. Maximum and minimum levels guaranteed by design and random testing for temperature range of –40 to +85°C.
5. Power is rated at I/Q input level of $0.9V_{PP}$.

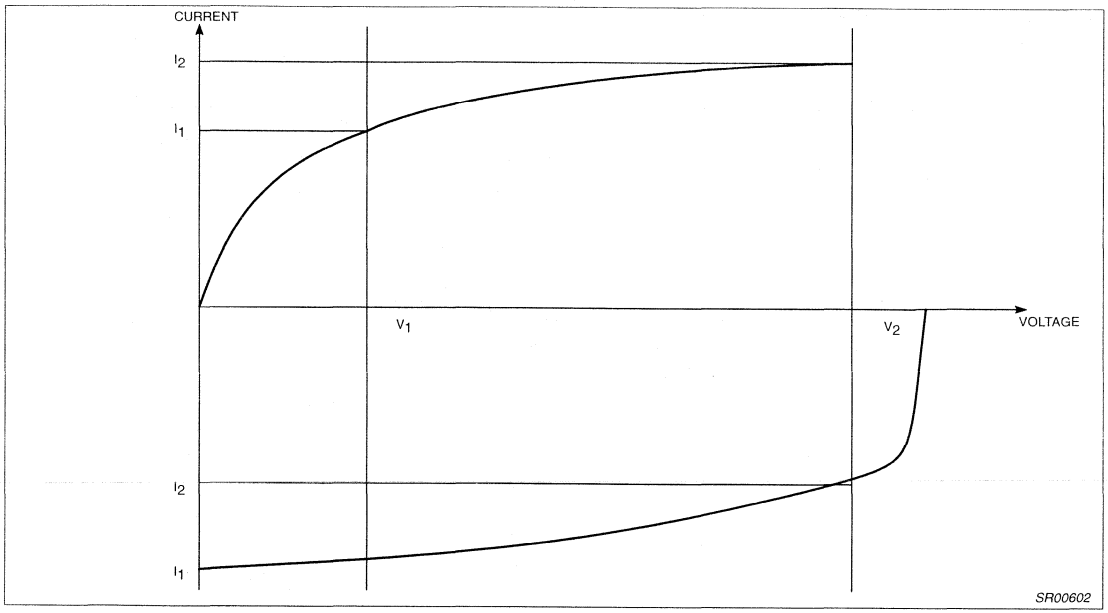


Figure 3. Output Current Definition

Functional Description Main Channel Synthesizer & Auxiliary Synthesizer

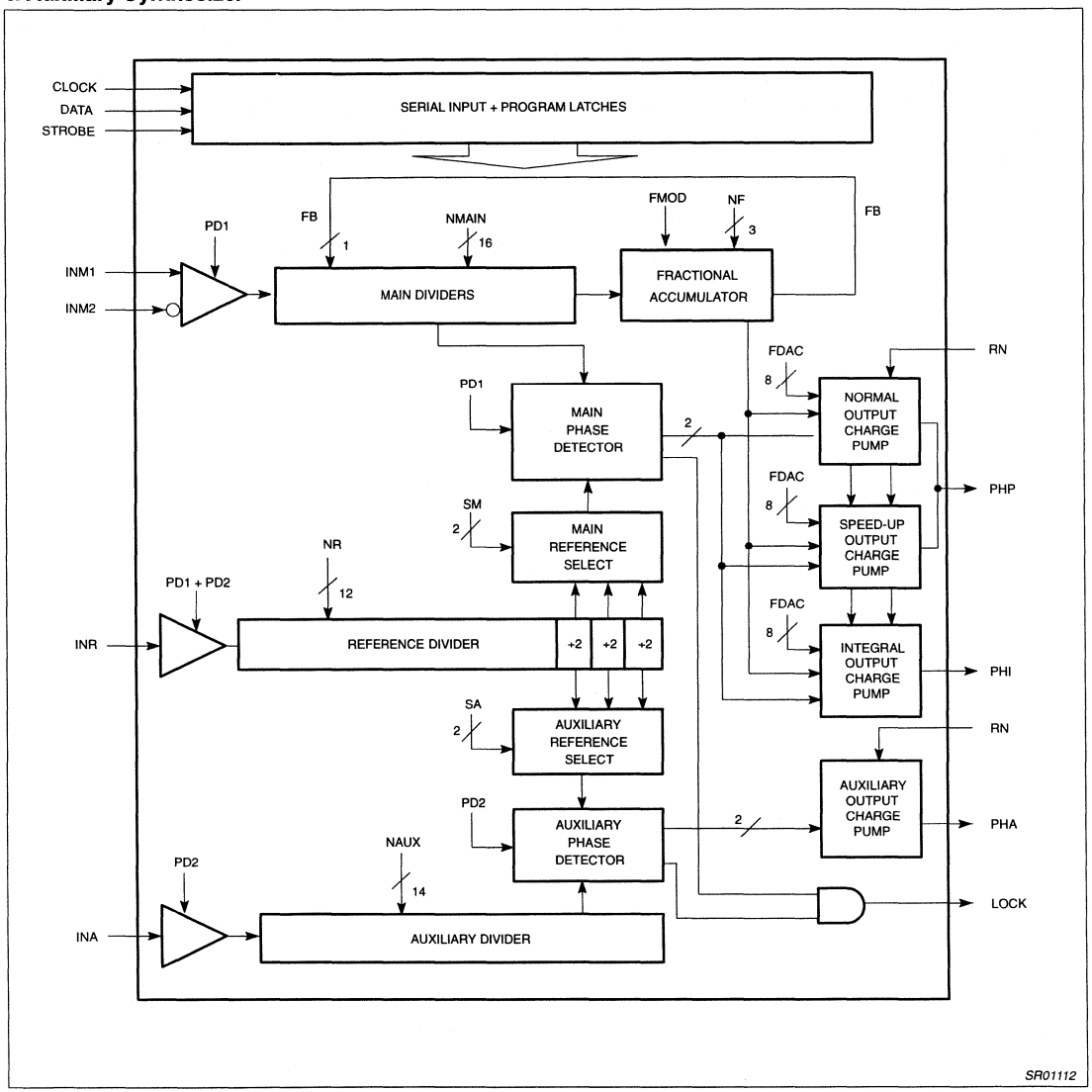


Figure 4. Synthesizer Block Diagram

Serial Programming Input

The serial input is a 3-wire input (CLOCK, DATA, STROBE) used to program all counter ratios, DACs, selection and enable bits. The programming data is structured into 24-bit words; each word includes 2 or 3 address bits. Figure [5] shows the timing diagram of the serial input. When STROBE = L, the clock driver is enabled and on positive edges of the CLOCK, the signal on DATA input is clocked into a shift register. When STROBE = H, the clock is disabled and the data in the shift register remains stable.

Depending on the 2 or 3 address bits, data is latched into different working or temporary registers. In order to fully program the synthesizer, 3 words must be sent: A, B and C. The D word programs all other functions within the SA9025. Those functions are

power control, ÷M (offset loop), SE (Tx offset loop synthesizer enable), DUAL mode, Sleep Mode 1 and Sleep Mode 2.

The data for FDAC is stored by the B word into a temporary register. When the A word is loaded, the data in this temporary register is loaded together with the A word into the work registers to avoid false temporary main synthesizer output caused by changes in fractional compensation.

The A word contains new data for the main divider. The A word is loaded into the working registers only when a main divider synchronization signal is active to avoid phase jumps when reprogramming the main divider. The synchronization pulse is generated by the main divider when it has reached its terminal count, at which time a main divider output pulse is also sent to the main phase detector. This disables the loading of the A word each main divider cycle during maximum of (NREF / f_{REF}) seconds. Therefore, to be sure that the A word will be correctly loaded, the STROBE signal must be high for at least (NREF / f_{REF}) seconds. When programming the A word, the main charge pumps on output PHP and PHI are set into the speed–up mode as soon as the A word is latched into the working registers and remain so as long as STROBE is held high.

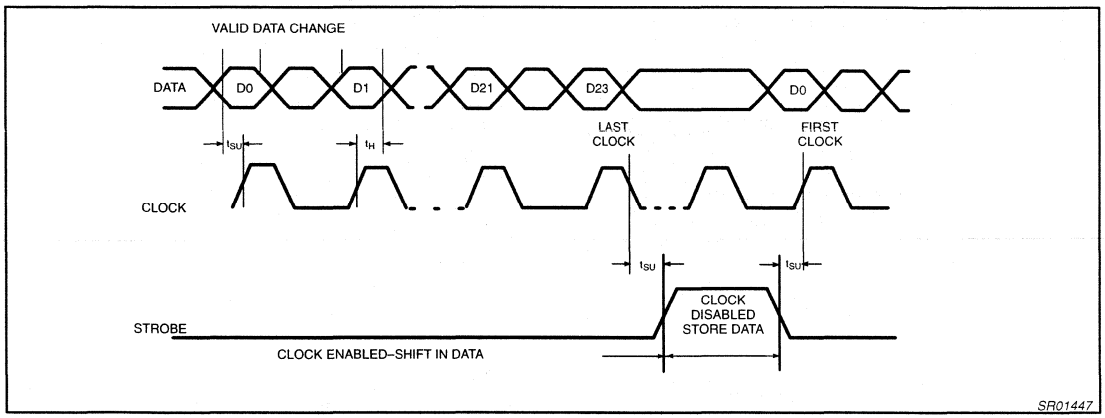


Figure 5. Serial Input Timing Sequence

Table 1. Function Table

Symbol	Bits	Function
FMOD	1	Fractional-N modulus selection flag: '0' = modulo 8 '1' = modulo 5
NF	3	Fractional-N increment
NMAIN	16	Main divider ratio; 512 to 65,535 allowed
NREF	10	Reference divider ratio; 4 to 1,023 allowed, RSM, RSA = "0 0"
RSM	2	Reference select for main phase detector
RSA	2	Reference select for auxiliary phase detector
FDAC	8	Fractional compensation charge pump current DAC
NAUX	14	Auxiliary divider ratio; 128 to 16,384 allowed
CP	2	Charge pump current ratio select (see table 1)
LD	2	Lock detect output select (see table 2)
PD1	1	PD1 = 0 for power down; shuts off power to main divider and main chargepumps, anded with PD2 to turn off ref. divider.
PD2	1	PD2 = 0 for power down; shuts off power to auxiliary divider, and auxiliary charge pumps; anded with PD1 to turn off ref. divider.
PC	8	Power control (see note 3)
M	2	÷M, M = 6, 7, 8, 9 (see note 4)
SE	1	Transmit offset synthesizer on/off
TM	1	Transmit mode: '0' = DUAL
AD	1	Mode control, 1 = digital; 0 = analog
SM1	1	Sleep mode 1
SM2	1	Sleep mode 2

1. Data bits are shifted in on the the leading clock edge, with the least significant bit (LSB) first and the most significant bit (MSB) last.
2. On the rising edge of the strobe and with the address decoder output = 1, the contents of the input shift register are transferred to the working registers. The strobe rising edge comes one half clock period after the clock edge on which the MSB of a word is shifted in.
3. The PC bits are used for the power control function. Eight (8) bits of data allows for appropriate resolution of the power control. 00000000 = 0 dB: 11111111 = –45.9 dB (= 255 ∠ 0.18).
4. The M bits are used to program the ÷M counter for integer values between 6 and 9. 00 = 6, 01 = 7, 10 = 8, 11 = 9.
5. The TM bit is used to put the SA9025 into DUAL mode operation. In DUAL mode (TM = 0).
6. The AD bit allows a reduction in the linearity of the DUAL output driver while in AMPS mode.
7. The SM1 bit is used to shut down the TX_{LO} buffers. SM1 = 1, buffers on; SM1 = 0, buffers off.
8. The SM2 bit is used to shut down the RCLK buffer. SM2 = 1, buffer on; SM2 = 0, buffer off.
9. The SE bit turns on and off the offset loop synthesizer circuits. SE = 1, synthesizer on; SE = 0, synthesizer off.
10. The LOCK bits determine what signal is present on the LOCK pin as follows:

Table 2.

Lock Detect Output Select*	
LOCK	**LOCK Pin Function**
00	Main, auxiliary and offset lock condition
01	Main and auxiliary lock condition
10	Main lock detect condition
11	Auxiliary lock condition

*When a section is in power down mode, the lock indicator for that section is high.

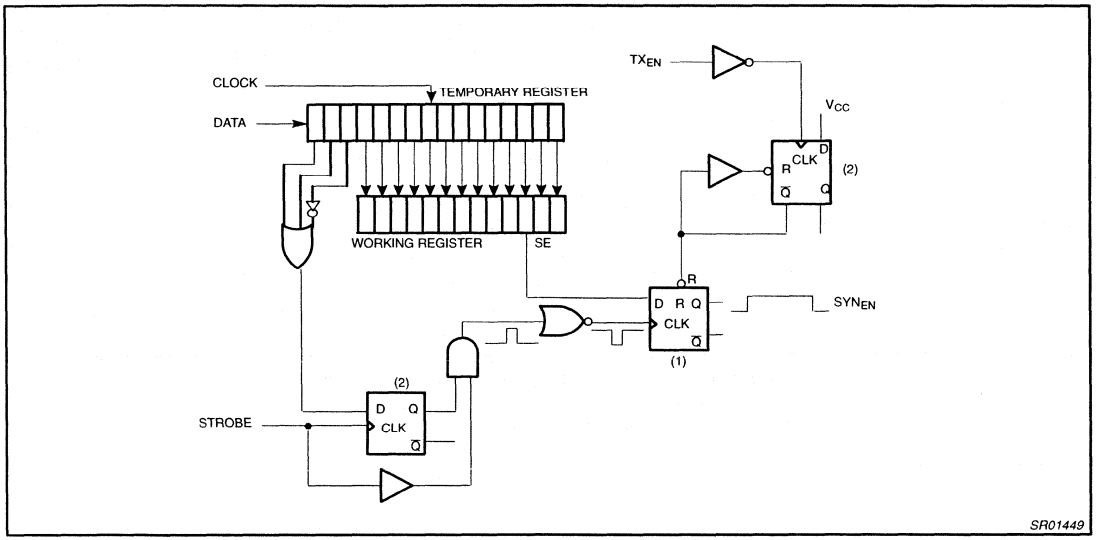


Figure 6. Transmit Offset Synthesizer Reset Circuit

In Figure 6, the falling edge of the strobe and address, inverted, toggles the Q output of flip-flop (1) to a '1' state, enabling the phase detector, VCO, divide by M, TX_{IF} buffer and SSB up-converter. Approximately 80µs after the synthesizer is locked, the TX_{EN} signal (enabled = 1) turns on the modulator and variable gain amplifier. The rising edge of TX_{EN} has no effect on SYN_{EN}, however, the falling (rising inverted) edge toggles the $\overline{Q}$ output of D flip-flop (2) to a '0' state. This disables the synthesizer, modulator and variable gain amplifier. To insure that slow edges on TX_{EN} do not cause improper operation, the TX_{EN} is a Schmitt trigger design.

The address decoder for program word 'D' ANDed together with the strobe is used to load the contents of the temporary register into the working registers. D flip-flop (3) is used to prevent multiple strobe and address pulses in the event the address decoder output toggles on garbage bits during the time the strobe remains in a '1' state.

The temporary register is common to the transmit offset synthesizer, main channel synthesizer and auxiliary synthesizer.

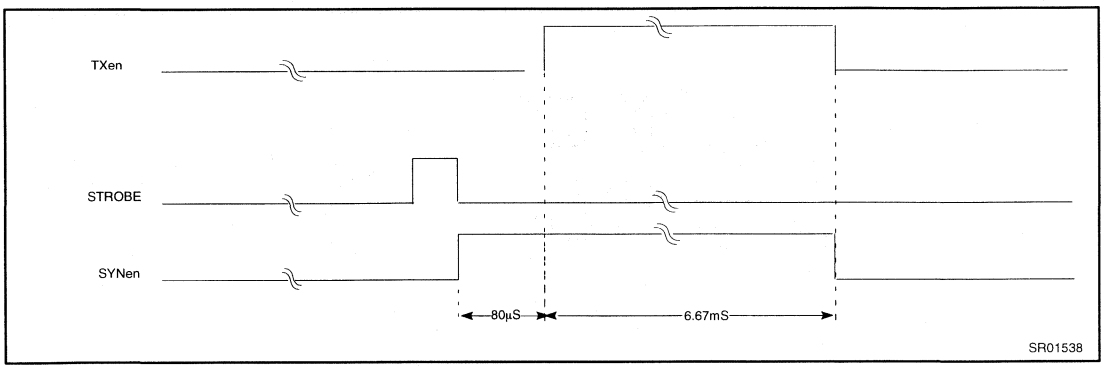


Figure 7. Transmit Offset Synthesizer Timing Diagram

Data format

Format of programmed data

LAST IN		MSB	SERIAL PROGRAMMING FORMAT				FIRST IN LSB
p23	p22	p21	p20	../..	../..	p1	p0

A word, length 24 bits

Last in					MSB														LSB	First IN	
Address		fmod	Fractional–N																	Spare	
0	0	Fmod	NF2	NF1	NF0	N15	N14	N13	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	N0	sk1	sk2
Default:		0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	1	0	0	0	0	0	0

A word select	Fixed to 00.
Fractional Modulus select	FM 0=modulo 8, 1=modulo 5.
Fractional–N Increment	NF2..0 Fractional N Increment values 000 to 111.
N–Divider	N0..N15, Main divider values 512 to 65535 allowed for divider ratio.

B word, length 24 bits

ADDRESS		REFERENCE DIVIDER NREF										RSM		RSA		FRACTIONAL COMPENSATION DAC							
0	1	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	RSM 1	RSM 0	RSA 1	RSA 0	Fdac 7	Fdac 6	Fdac 5	Fdac 4	Fdac 3	Fdac 2	Fdac 1	Fdac 0
Default:		0	0	0	1	0	1	0	0	0	1	0	0	0	0	x	x	x	x	x	x	x	x

B word select	Fixed to 01
R–Divider	R0..R9, Reference divider values 4 to 1023 allowed for divider ration.
Charge pump current Ratio	CP1, CP0: Charge pump current ratio, see table of charge pump currents.
Main comparison select	RSM Comparison divider select for main phase detector.
Aux comparison select	RSA Comparison divider select for auxiliary phase detector.
Fractional Compensation	Fdac7..0, Fractional compensation charge pump current DAC, values 0 to 255. FDAC = 77 for best op MOD8.

C word, length 24 bits

ADDRESS		AUXILIARY DIVIDER NAUX													CP		LOCK		PD		SPARE	
1	0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	CP1	CP0	LD1	LD0	PD1	PD2	PD3	LOD
Default		0	0	0	0	0	1	1	1	0	0	1	0	1	0	1	1	0	0	TX_{EN}	TX_{EN}	0	0

C word select	Fixed to 10
A–Divider	A0..A13, Auxiliary divider values 128 to 16384 allowed for divider ratio.
Charge pump current Ratio	CP1, CP0: Charge pump current ratio, see table fo charge pump currents.
Lock detect output	LD1 LD0 0 0 Combined main, aux. & offset loop lock detect signal present at the LOCK pin. 0 1 Combined main and aux. lock detect signal present at the LOCK pin. 1 0 Main lock detect signal present at the LOCK pin. 1 1 Auxiliary loop lock detect signal present at the LOCK pin. When a section is in power down mode, the lock indicator for that section is high.
Power down	PD1=1: power to N–divider, reference divider, main charge pumps, PD1=0 to power down. PD2=1: power to Aux divider, reference divider, Aux charge pump, PD2=0 to power down.

Table 3.
Main and auxiliary chargepump currents

CP1	CP0	I_{PHA}	I_{PHP}	I_{PHP-SU}	I_{PHI_SU}
0	0	1.5xIset	3xIset	15xIset	36xIset
0	1	0.5xIset	1xIset	5xIset	12xIset
1	0	1.5xIset	3xIset	15xIset	0
1	1	0.5xIset	1xIset	5xIset	0

NOTES
1. I_{SET} = Vset/RN; bias current for charge pumps.
2. CP1 is used to disable the PHI pump.
3. Iphp_su is the total current out of PHP in speedup mode.

D word, length 24 bits

Address			Power Control								M divider		SE	TM	AD	Sleep Mode		Test pa_current					
1	1	0	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	M1	M0	SE	TM	AD	SM1	SM2	pai5	pai4	pai3	pai2	pai1	pai0
Default:			x	x	x	x	x	x	x	x	0	0	0	0	0	0	0	0	0	0	0	0	0

D0 word select	Fixed to 110.
Output Power Control	PC7(msb)...PC0(lsb) Provides output power attenuation for DUAL mode amplifier outputs in 0.18 dB steps, Fx = 45.9 dB.
M Divider	00 = 6, 01 = 7, 10 = 8, 11 = 9
Offset loop power down	SE Offset loop synthesizer power down, SE = 1 power on, SE = 0 power down (sleep mode).
DUAL mode select	TM = 0 DUALmode
AMPS/DAMPS mode select	AD = 1 DAMPS mode. AD = 0 AMPs mode
TX buffers power down	SM1 TX Local oscillator buffers power down. SM1 = 1 power on, SM1 = 0 to power down. SM2 RCLK buffer power down. SM2 = 1 power on, SM2 = 0 to power down.
Test: pa_current:pai	TX test bits for controlling the current in the power amp. Should be 0 during normal operation.

MODES OF OPERATION

There are two power saving modes of operation which the circuit can be put into, dependent on the status of the system. The intention of these different modes is to disable circuitry that is not in use at the time in order to reduce power consumption. During sleep mode, only circuitry which is required to provide a master clock to the digital portion of the system is enabled. During receive mode, circuitry which is used to perform the receive function and provide a master clock is enabled. In transmit mode all the functions of the circuit are enabled which are required to perform transmit, receive and provide master clock. When the circuit is powered for the first time, it is in DUAL MODE SLEEP.

Mode Programming

Mode	Dual Mode AMPS			
Mode Setting and BlockStatus (X = ON)	Sleep	RX	TX	Logic
TX_{EN}	0	0	1	
PD1	0	1	1	
PD2	0	1	1	
SE–>SYNen	0	0	1	
TM	0	0	0	
SM1	0	0	1	
SM2	0	1	1	
Main loop, Ndivider, RXLO buffer		X	X	PD1
Aux loop, Adivider		X	X	PD2
Rdivider		X	X	PD1 .OR. PD2
Offset VCO, Mdivider			X	SE (+delay) See $SE–>SYN_{EN}$ diagram
RCL buffer		X	X	SM2
MCL buffer, reference input	X	X	X	1 (always ON)
$DUAL_{TX}$ PA			X	(.not. TM) .and. TX_{EN} .and. SM1
TXLO buffer, SSB up–converter			X	SM1
I/Q MODULATOR, VGA			X	TXEN .AND. SM1
Control Logic	X	X	X	1 (always ON)

Main Divider

The input signal on RX_{LO} is amplified to a logic level by a balanced input comparator giving a common mode rejection. This input stage is enabled by serial control bit PD1 = 1. Disabling means that all currents in the comparator are switched off. The main divider is built up to be a 16-bit counter.

The loading of the work registers FMOD, NF and NMAIN is synchronized with the state of the main counter to avoid extra phase disturbance when switching over to another main divider ratio as is explained in the Serial Programming Input chapter.

At the completion of a main divider cycle, a main divider output pulse is generated which will drive the main phase comparator. Also, the fractional accumulator is incremented with NF. The accumulator works modulo Q. Q is preset by the serial control bit FMOD to 8 when FMOD = '0'. Each time the accumulator overflows, the total divide ratio will be NMAIN + 1 for the next cycle. The mean division ratio over Q main divider cycles will then be:

$$NQ = NMAIN + \frac{NF}{Q}$$

Synchronization is provided to avoid a random phase on the phase detector upon the loading of a new ratio and when powering up the loop.

Auxiliary Divider

The input signal on INA is amplified to logic level by a single-ended input buffer, which accepts low level AC-coupled input signals. This input stage is enabled if the serial control bit PD2 = '1'. Disabling means that all currents in the buffer and prescaler are switched off. The auxiliary divider is programmed with 14 bits and has continuous integer division ratios over the range of 128 to 16,384.

Reference Divider (Figure 8)

The input can be driven by a differential crystal input or an external TCXO. This input stage is enabled by the OR function of the serial input bits PD1 and PD2. Disabling means that all currents are switched off. The reference divider consists of a programmable divide by N_{REF} (N_{REF} = 4 to 1,023) followed by a 3-bit binary counter. The 2 bit SM determines which of the four output pulses is selected as the main phase detector signal. To obtain the best time spacing for the main and auxiliary reference signals, a different output will be used for the auxiliary phase detector, reducing the possibility of unwanted interactions.

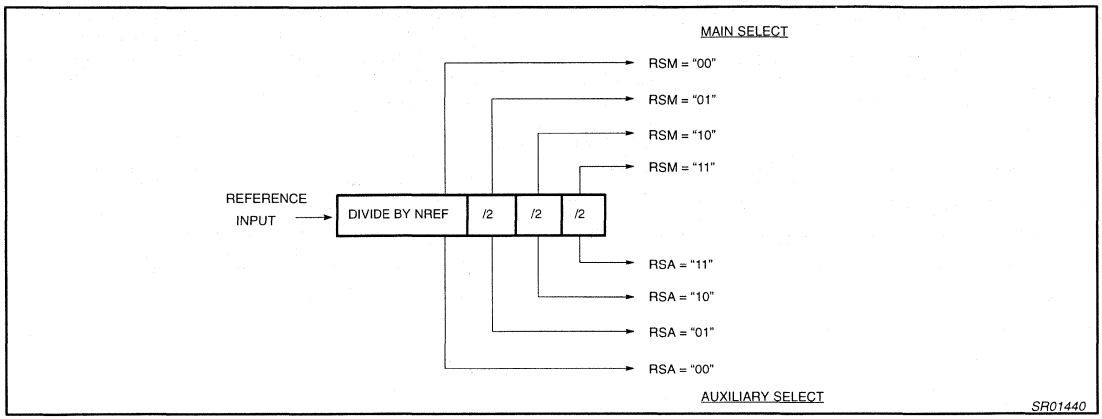


Figure 8. Reference Variable Divider

Phase Detectors (Figure 9)

The auxiliary and main phase detectors each consist of a 2 D-type flip-flop phase and frequency detector. Each flip-flop is set by the negative edge of the divider terminal count output pulse. The reset inputs are activated after a delay when both flip-flops have been set. This avoids non-linearity or dead-band around zero phase error. The flip-flops drive on-chip charge pumps. A pull-up current from the charge pump indicates the VCO frequency shall be increased while a pull-down pulse indicates the VCO frequency shall be decreased.

Current Settings

The IC has two current setting pins, RN and I_{PEAK}. The active charge pump currents and the fractional compensation currents are linearly dependent on the current in the current setting pins. This current, I_{SET}, is set by an external resistor connected between the current setting pin and V_{SS}.

Auxiliary Output Charge Pumps

The auxiliary charge pumps on pin PHA are driven by the auxiliary phase detector and the current value is determined by the external resistor attached to pin RN.

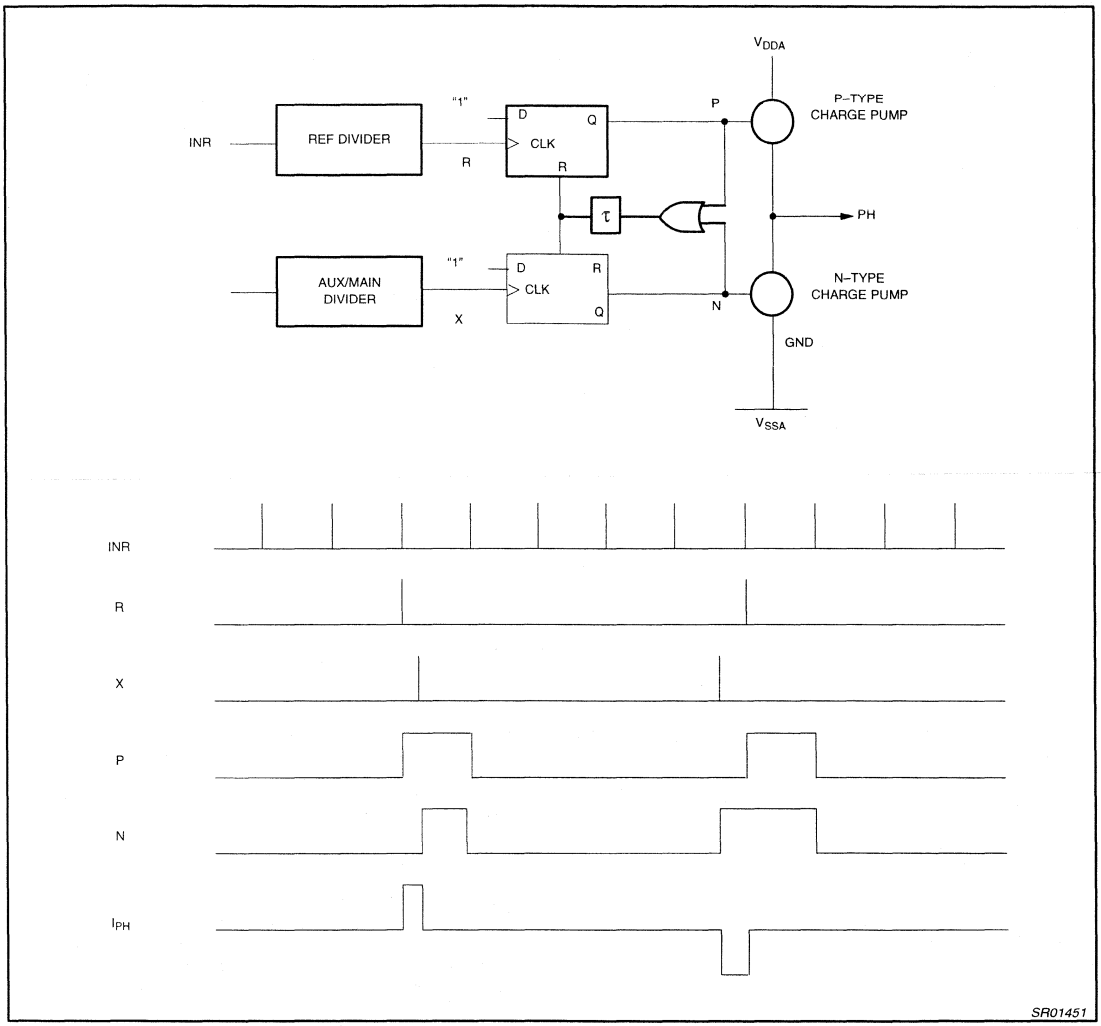


Figure 9. Phase Detector Structure With Timing

Main Output Charge Pumps and Fractional Compensation Currents

The main charge pumps on pin PHP and PHI are driven by the main phase detector. The current value is determined by the current at pin RN. The fractional compensation current is linearly dependent on the main charge pump current and its level relative to the main charge pumps is set by an 8-bit programmable DAC. The timing for the fractional compensation is derived from the main divider. The current level based on the value of FRD, FDAC and I_{SET}. Figure 10 shows the waveforms (not to scale) for a typical base.

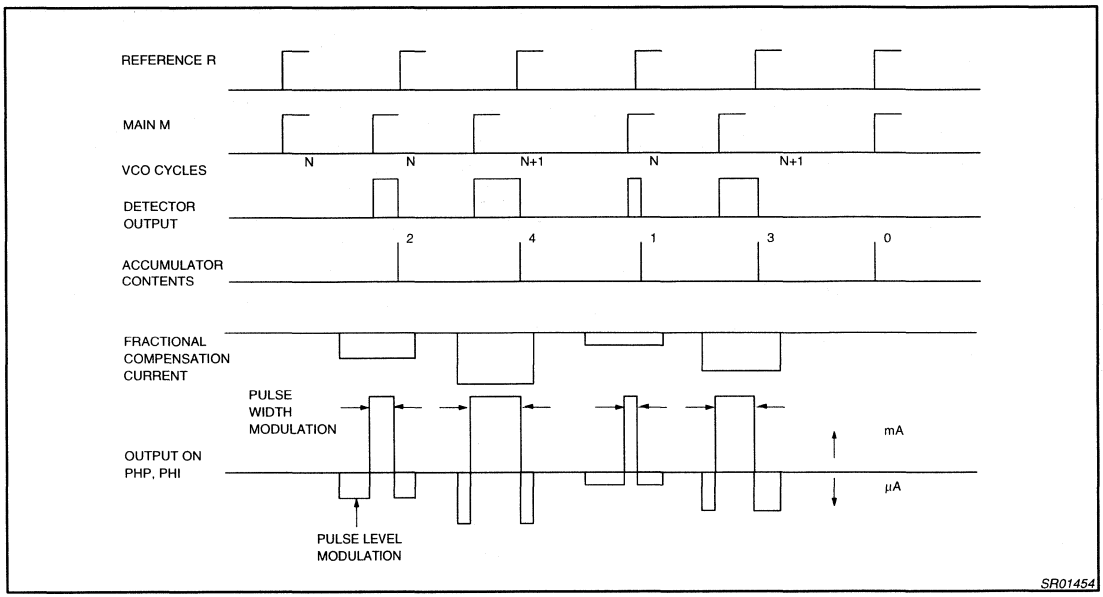


Figure 10. Waveforms for NF = 2; Fraction = 0.4

Figure 10 shows that for a proper fractional compensation, the area of the fractional compensation current pulse must be equal to the area of the charge pump ripple output.

The fractional compensation current is derived from the main charge pump in that it will follow all the current scaling through external resistor setting, programming or speedup operation.

For a given pump,

$$Icomp = \frac{Ipump}{128} \times \frac{Fdac}{5 \times 128} \times FRD$$

Where:
Icomp is the compensation current, Ipump is the pump current, Fdac is the fractional DAC value and FRD is the fractional accumulator value.

The theoretical value for Fdac would then be: 128 for Fmod = 1 (modulo 5) and 80 for Fmod = 0 (modulo 8).

When the serial input A word is loaded, the output circuits are in the "speedup mode" as long as the STROBE is H, otherwise the "normal mode" is active.

Lock Detect

The output LOCK maintains a logic '1' when the auxiliary phase detector ANDed with the main phase detector indicates a lock condition. The lock condition for the main and auxiliary synthesizers is defined as a phase difference of less than ± 1 cycle on the reference inputs XTAL1,2. The LOCK condition is also fulfilled when the relative counter is disabled (PD_{main} = '0' or PD_{aux} = '0') for the main or auxiliary counter, respectively. Lock indication when PD_{main} = PD_{aux} = '0'.

Functional Description of Offset Loop, Modulator and Power Control

Transmit Offset Synthesizer

The transmit offset phase locked loop portion of the SA9025 design consists of the following functional blocks: reference oscillator, limiters, phase detector, ÷M, IF VCO and passive loop filter. Harmonic contents of this signal are attenuated by an LP filter. The output of the IF VCO is also divided by N and compared with the reference oscillator in the phase detector.

Reference Oscillator

This Oscillator is used to generate the reference frequency together with an external crystal and varicap. The output is internally routed to three buffers and a phase comparator. It is possible to run the oscillator as an amplifier from an external reference signal (TCXO).

Phase Detector and Charge Pump

The phase comparator is used to compare the output of the divider with the reference. It provides an output proportional to the phase difference between the divided down VCO and the reference. This output is then filtered and used as the control voltage input to the VCO. The phase detector is a Gilbert multiplier cell type, having a linear output from 0 to π ($\pi/2 \pm \pi/2$), followed by a charge pump. The charge pump peak output current is programmable to 6.4mA via the use of an external resistor.

A preliminary design analysis has been performed with the following loop parameters:

A lock detect signal is provided and ANDed together with lock detect signals from both the main channel synthesizer and auxiliary

Battery charge level indicator SAA1501T

FEATURES

- High level of integration to allow assembly in intelligent battery packs
- Accurate charge and discharge account
- Large dynamic range of charge and discharge currents
- Independent settings of charge and discharge efficiency
- 2 V minimum supply voltage (2 cell operation)
- Temperature protection of batteries during charging
- Temperature controlled self-discharge
- Accurate charge current regulation
- Two charge amount display modes, LCD and LED.

GENERAL DESCRIPTION

The SAA1501T is intended to be used as a battery monitor and charge current control circuit in rechargeable battery systems.

The SAA1501T is processed in BiCMOS technology where the benefits of mixed bipolar and CMOS technology is fully utilized to achieve high accuracy measurements and digital signal processing in the same device. The general function of the integrated circuit is a Coulomb counter. During battery charging, the charge current and charge time are registered in a Coulomb counter. During discharge, the discharge current and time are recorded. The momentary charge amount of the batteries can be displayed either on an LCD screen or on an LED bargraph. Using the SAA1501T, intelligent batteries or intelligent battery powered systems can be easily designed with only a few external components.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		2.0	3.0	4.3	V
I_{CC}	supply current	V_{CC} = 3 V; $I_c = I_d$ = 60 µA	–	1.2	1.7	mA
I_{CCstb}	supply current in standby mode	V_{CC} = 3 V; $V_{CSI} = V_{DSI}$ = 0 V	–	–	100	µA
f_{osc}	fixed oscillator frequency	C_{osc} = 820 pF; R_{ref} = 51.5 kΩ	–	4.2	–	kHz
$V_{i(s)}$	input sense voltage (pins 9 and 10)		0	–	V_{CC} – 1.6	V
T_{amb}	operating ambient temperature		0	–	+70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA1501T	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1

BLOCK DIAGRAM

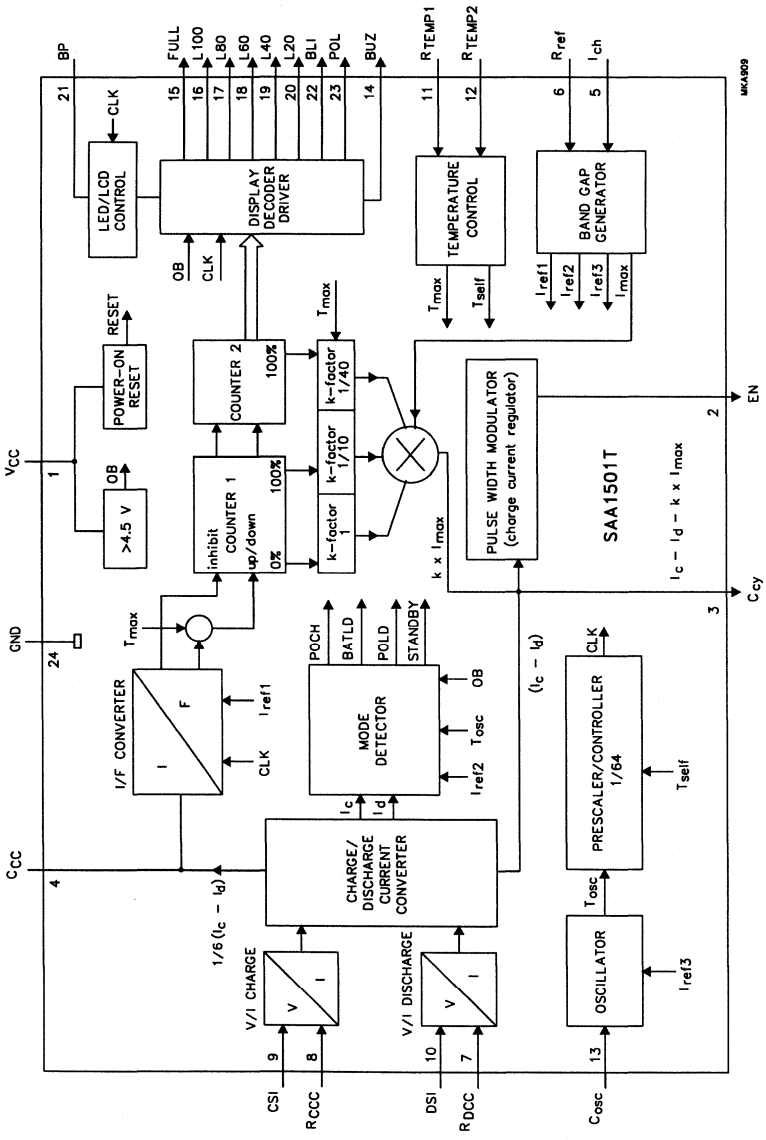


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{CC}	1	supply voltage
EN	2	enable output
C_{cy}	3	duty cycle capacitor output
C_{CC}	4	charge counter capacitor output
I_{ch}	5	maximum average charge current setting input
R_{ref}	6	current reference resistor input
R_{DCC}	7	discharge current conversion resistor input
R_{CCC}	8	charge current conversion resistor input
CSI	9	charge sense input
DSI	10	discharge sense input
R_{TEMP1}	11	temperature sensing resistor 1 input
R_{TEMP2}	12	temperature sensing resistor 2 input
C_{osc}	13	oscillator capacitor input
BUZ	14	buzzer output
FULL	15	battery full indication output
L100	16	100% segment indication output
L80	17	80% segment indication output
L60	18	60% segment indication output
L40	19	40% segment indication output
L20	20	20% segment indication output
BP	21	LCD back plane drive
BLI	22	battery low indicator LED output
POL	23	power-on LED output
GND	24	power ground

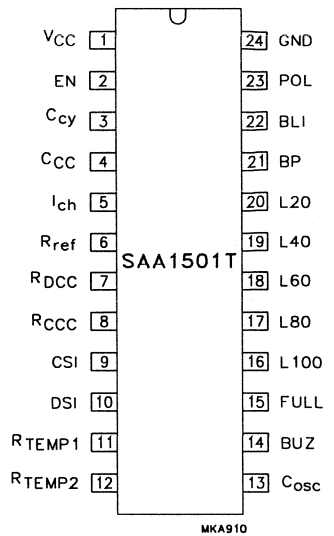


Fig.2 Pin configuration.

Low voltage mono/stereo power amplifier TDA7050T

GENERAL DESCRIPTION

The TDA7050T is a low voltage audio amplifier for small radios with headphones (such as watch, pen and pocket radios) in mono (bridge-tied load) or stereo applications.

Features

- Limited to battery supply application only (typ. 3 and 4 V)
- Operates with supply voltage down to 1,6 V
- No external components required
- Very low quiescent current
- Fixed integrated gain of 26 dB, floating differential input
- Flexibility in use – mono BTL as well as stereo
- Small dimension of encapsulation (see package design example).

QUICK REFERENCE DATA

Supply voltage range	V_P		1,6 to 6,0	V
Total quiescent current (at V_P = 3 V)	I_{tot}	typ.	3,2	mA
Bridge tied load application (BTL)				
Output power at R_L = 32 Ω				
V_P = 3 V; d_{tot} = 10%	P_o	typ.	140	mW
D.C. output offset voltage between the outputs	$\lvert\Delta V\rvert$	max.	70	mV
Noise output voltage (r.m.s. value)				
at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ.	140	μV
Stereo application				
Output power at R_L = 32 Ω				
d_{tot} = 10%; V_P = 3 V	P_o	typ.	35	mW
d_{tot} = 10%; V_P = 4,5 V	P_o	typ.	75	mW
Channel separation at R_S = 0 Ω; f = 1 kHz	α	typ.	40	dB
Noise output voltage (r.m.s. value)				
at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ.	100	μV

PACKAGE OUTLINE

8-lead mini-pack; plastic (SO8; SOT96A); SOT96-1; 1996 July 24.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	6 V
Peak output current	I_{OM}	max.	150 mA
Total power dissipation	see derating curve Fig.1		
Storage temperature range	T_{stg}	−55 to + 150	°C
Crystal temperature	T_c	max.	100 °C
A.C. and d.c. short-circuit duration			
at V_P = 3,0 V (during mishandling)	t_{sc}	max.	5 s

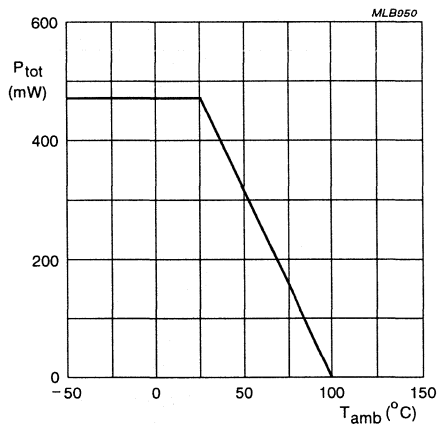


Fig.1 Power derating curve.

SO PACKAGE DESIGN EXAMPLE

To achieve the small dimension of the encapsulation the SO package is preferred with only 8 pins. Because a heatsink is not applicable, the dissipation is limited by the thermal resistance of the 8-pin SO encapsulation until:

$$\frac{T_{j\,max} - T_{amb}}{R_{th\,j\text{-}a}} = \frac{100 - 60}{160} = 0.25\ W$$

CHARACTERISTICS

V_P = 3 V; f = 1 kHz; R_L = 32 Ω; T_{amb} = 25 °C; unless otherwise specified

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply					
Supply voltage	V_P	1,6	–	6,0	V
Total quiescent current	I_{tot}	–	3,2	4	mA
Bridge-tied load application (BTL); see Fig.4					
Output power*					
V_P = 3,0 V; d_{tot} = 10%	P_o	–	140	–	mW
V_P = 4,5 V; d_{tot} = 10% (R_L = 64 Ω)	P_o	–	150	–	mW
Voltage gain	G_v	–	32	–	dB
Noise output voltage (r.m.s. value)					
R_S = 5 kΩ; f = 1 kHz	$V_{no(rms)}$	–	140	–	μV
R_S = 0 Ω; f = 500 kHz; B = 5 kHz	$V_{no(rms)}$	–	tbf	–	μV
D.C. output offset voltage (at R_S = 5 kΩ)	$\lvert\Delta V\rvert$	–	–	70	mV
Input impedance (at R_S = ∞)	$\lvert Z_i\rvert$	1	–	–	MΩ
Input bias current	I_i	–	40	–	nA
Stereo application; see Fig.5					
Output power*					
V_P = 3,0 V; d_{tot} = 10%	P_o	–	35	–	mW
V_P = 4,5 V; d_{tot} = 10%	P_o	–	75	–	mW
Voltage gain	G_v	24.5	26	27.5	dB
Noise output voltage (r.m.s. value)					
R_S = 5 kΩ; f = 1 kHz	$V_{no(rms)}$	–	100	–	μV
R_S = 0 Ω; f = 500 kHz; B = 5 kHz	$V_{no(rms)}$	–	tbf	–	μV
Channel separation					
R_S = 0 Ω; f = 1 kHz	α	30	40	–	dB
Input impedance (at R_S = ∞)	$\lvert Z_i\rvert$	2	–	–	MΩ
Input bias current	I_i	–	20	–	nA

* Output power is measured directly at the output pins of the IC. It is shown as a function of the supply voltage in Fig.2 (BTL application) and Fig.3 (stereo application).

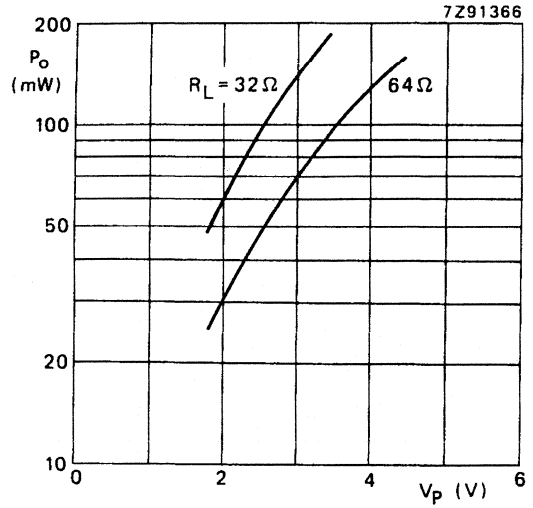


Fig.2 Output power across the load impedance (R_L) as a function of supply voltage (V_P) in BTL application. Measurements were made at f = 1 kHz; d_{tot} = 10%; T_{amb} = 25 °C.

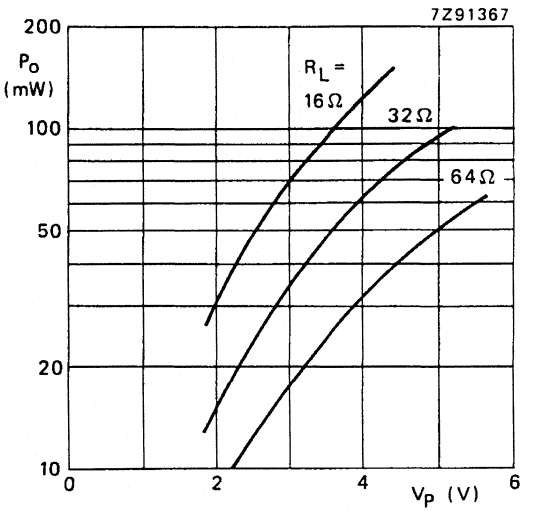


Fig.3 Output power across the load impedance (R_L) as a function of supply voltage (V_P) in stereo application. Measurements were made at f = 1 kHz; d_{tot} = 10%; T_{amb} = 25 °C.

APPLICATION INFORMATION

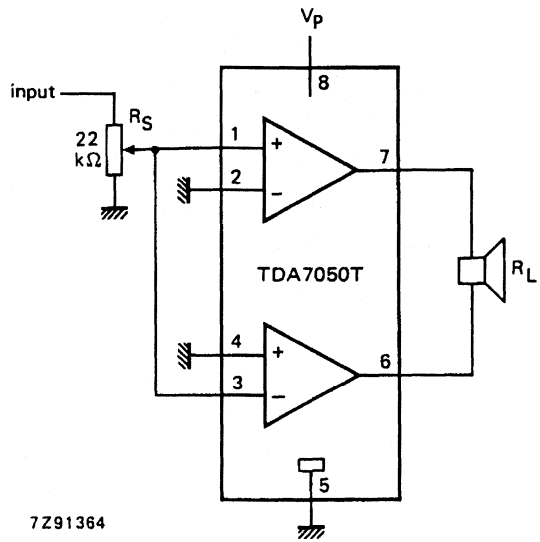


Fig.4 Application diagram (BTL); also used as test circuit.

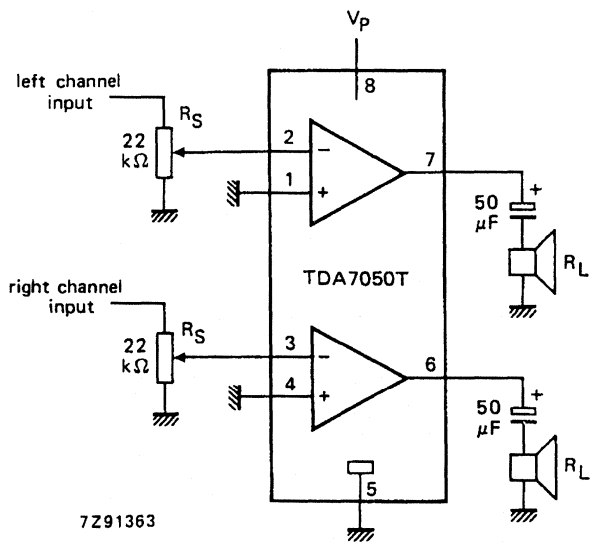


Fig.5 Application diagram (stereo); also used as test circuit.

1 W BTL mono audio amplifier with DC volume control

TDA7052A/AT

FEATURES

- DC volume control
- Few external components
- Mute mode
- Thermal protection
- Short-circuit proof
- No switch-on and off clicks
- Good overall stability
- Low power consumption
- Low HF radiation
- ESD protected on all pins

GENERAL DESCRIPTION

The TDA7052A/AT are mono BTL output amplifiers with DC volume control. They are designed for use in TV and monitors, but also suitable for battery-fed portable recorders and radios.

Missing Current Limiter (MCL)

A MCL protection circuit is built-in. The MCL circuit is activated when the difference in current between the output terminal of each amplifier exceeds 100 mA (typical 300 mA). This level of 100 mA allows for headphone applications (single-ended).

QUICK REFERENCE DATA

SYMBOL	PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage range		4.5	–	18	V
P_O	output power					
	TDA7052A	R_L = 8 Ω; V_P = 6 V	1.0	1.1	–	W
	TDA7052AT	R_L = 16 Ω; V_P = 6 V	0.5	0.55	–	W
G_v	maximum total voltage gain		34.5	35.5	36.5	dB
ϕ	gain control range		75	80	–	dB
I_P	total quiescent current	V_P = 6 V; R_L = ∞	–	7	12	mA
THD	total harmonic distortion					
	TDA7052A	P_O = 0.5 W	–	0.3	1	%
	TDA7052AT	P_O = 0.25 W	–	0.3	1	%

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA7052A	8	DIL	plastic	SOT97[1]
TDA7052AT	8	mini-pack	plastic	SOT96A[2]

Notes

1. SOT97-1; 1996 September 10.
2. SOT96-1; 1996 September 10.

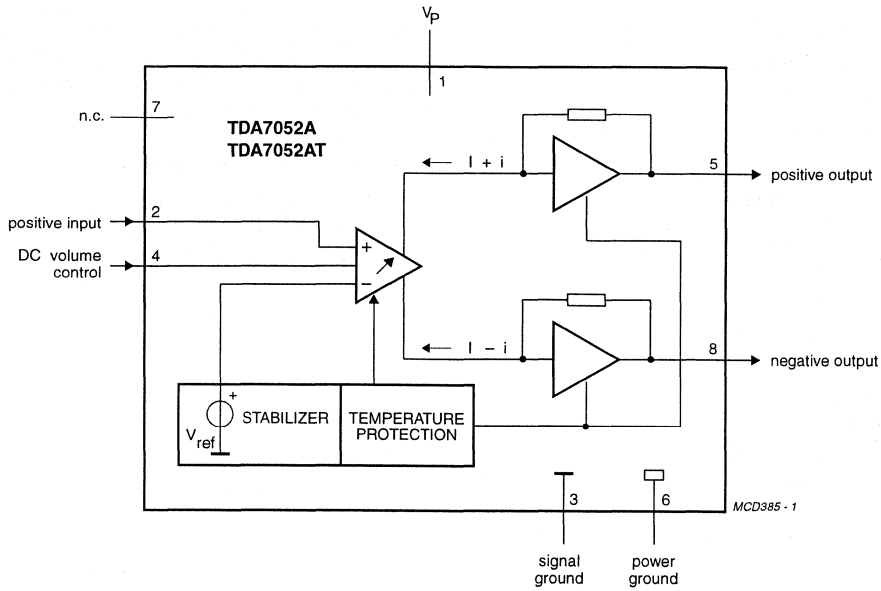


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_P	1	positive supply voltage
IN+	2	positive input
GND1	3	signal ground
VC	4	DC volume control
OUT+	5	positive output
GND2	6	power ground
n.c	7	not connected
OUT–	8	negative output

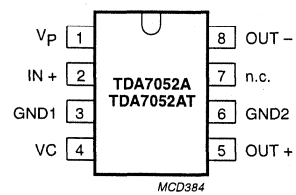


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA7052A/AT are mono BTL output amplifiers with DC volume control, designed for use in TV and monitors but also suitable for battery fed portable recorders and radios.

In conventional DC volume circuits the control or input stage is AC coupled to the output stage via external capacitors to keep the offset voltage low.

In the TDA7052A/AT the DC volume control stage is integrated into the input stage so that no coupling capacitors are required and yet a low offset voltage is maintained. At the same time the minimum supply remains low.

The BTL principle offers the following advantages:

- Lower peak value of the supply current
- The frequency of the ripple on the supply voltage is twice the signal frequency.

Thus a reduced power supply with smaller capacitors can be used which results in cost savings.

For portable applications there is a trend to decrease the supply voltage, resulting in a reduction of output power at conventional output stages. Using the BTL principle increases the output power.

The maximum gain of the amplifier is fixed at 35.5 dB. The DC volume control stage has a logarithmic control characteristic.

The total gain can be controlled from 35.5 dB to −44 dB. If the DC volume control voltage is below 0.3 V, the device switches to the mute mode.

The amplifier is short-circuit proof to ground, V_P and across the load. Also a thermal protection circuit is implemented. If the crystal temperature rises above +150 °C the gain will be reduced, so the output power is reduced.

Special attention is given to switch on and off clicks, low HF radiation and a good overall stability.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage range		–	18	V
I_{ORM}	repetitive peak output current		–	1.25	A
I_{OSM}	non-repetitive peak output current		–	1.5	A
P_{tot}	total power dissipation	$T_{amb} \leq 25\%$			
	TDA7052A		–	1.25	W
	TDA7052AT		–	0.8	W
T_{amb}	operating ambient temperature range		−40	+85	°C
T_{stg}	storage temperature range		−55	+150	°C
T_{vj}	virtual junction temperature		–	+150	°C
T_{sc}	short-circuit time		–	1	hr
V_2	input voltage pin 2		–	8	V
V_4	input voltage pin 4		–	8	V

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	
	TDA7052A	100 K/W
	TDA7052AT	155 K/W

Notes to the thermal resistance

TDA7052A: $V_P = 6$ V; $R_L = 8\ \Omega$. The maximum sine-wave dissipation is 0.9 W.
Therefore $T_{amb(max)} = 150 - 100 \times 0.9 = 60$ °C.

TDA7052AT: $V_P = 6$ V; $R_L = 16\ \Omega$. The maximum sine-wave dissipation is 0.46 W.
Therefore $T_{amb(max)} = 150 - 155 \times 0.46 = 78$ °C.

CHARACTERISTICS

V_P = 6 V; T_{amb} = 25 °C; f = 1 kHz; TDA7052A: R_L = 8 Ω; TDA7052AT: R_L = 16 Ω; unless otherwise specified (see Fig.6).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage range		4.5	–	18	V
I_P	total quiescent current	V_P = 6 V; R_L = ∞ note 1	–	7	12	mA
Maximum gain; V_4 = 1.4 V						
P_O	output power TDA7052A TDA7052AT	THD = 10%	 1.0 0.5	 1.1 0.55	 – –	 W W
THD	total harmonic distortion TDA7052A TDA7052AT	 P_O = 0.5 W P_O = 0.25 W	 – –	 0.3 0.3	 1 1	 % %
G_v	voltage gain		34.5	35.5	36.5	dB
V_I	input signal handling	V_4 = 0.8 V; THD < 1%	0.5	0.65	–	V
$V_{no(rms)}$	noise output voltage (RMS value)	f = 500 kHz; note 2	–	210	–	μV
B	bandwidth	–1 dB	–	20 Hz to 300 kHz	–	
SVRR	supply voltage ripple rejection	note 3	38	46	–	dB
$\|V_{off}\|$	DC output offset voltage		–	0	150	mV
Z_I	input impedance (pin 2)		15	20	25	kΩ
Minimum gain; V_4 = 0.5 V						
G_v	voltage gain		–	–44	–	dB
$V_{no(rms)}$	noise output voltage (RMS value)	note 4	–	20	30	μV
Mute position						
V_O	output voltage in mute position	$V_4 \leq$ 0.3 V; V_I = 600 mV	–	–	30	μV
DC volume control						
ϕ	gain control range		75	80	–	dB
I_4	control current	V_4 = 0.4 V	60	70	80	μA

Notes to the characteristics

1. With a load connected to the outputs the quiescent current will increase, the maximum value of this increase being equal to the DC output offset voltage dividend by R_L.
2. The noise output voltage (RMS value) at f = 500 kHz is measured with R_S = 0 Ω and bandwidth = 5 kHz.
3. The ripple rejection is measured with R_S = 0 Ω and f = 100 Hz to 10 kHz. The ripple voltage of 200 mV, (RMS value) is applied to the positive supply rail.
4. The noise output voltage (RMS value) is measured with R_S = 5 kΩ unweighted.

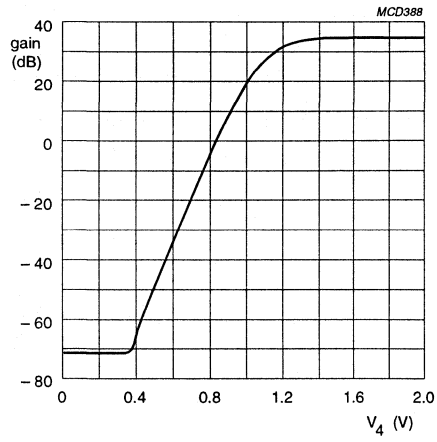


Fig.3 Gain control as a function of DC volume control.

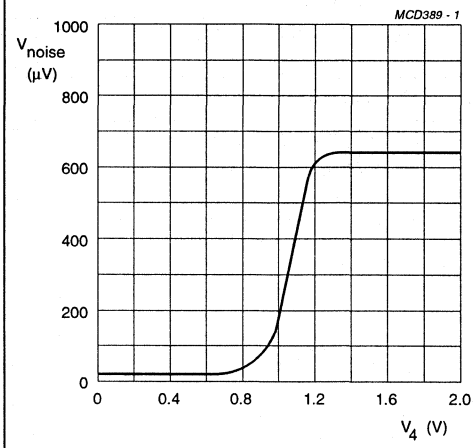


Fig.4 Noise output voltage as a function of DC volume control.

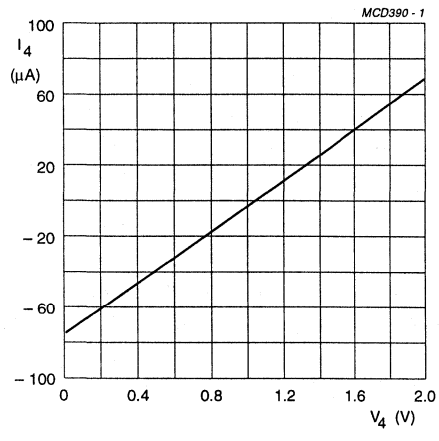
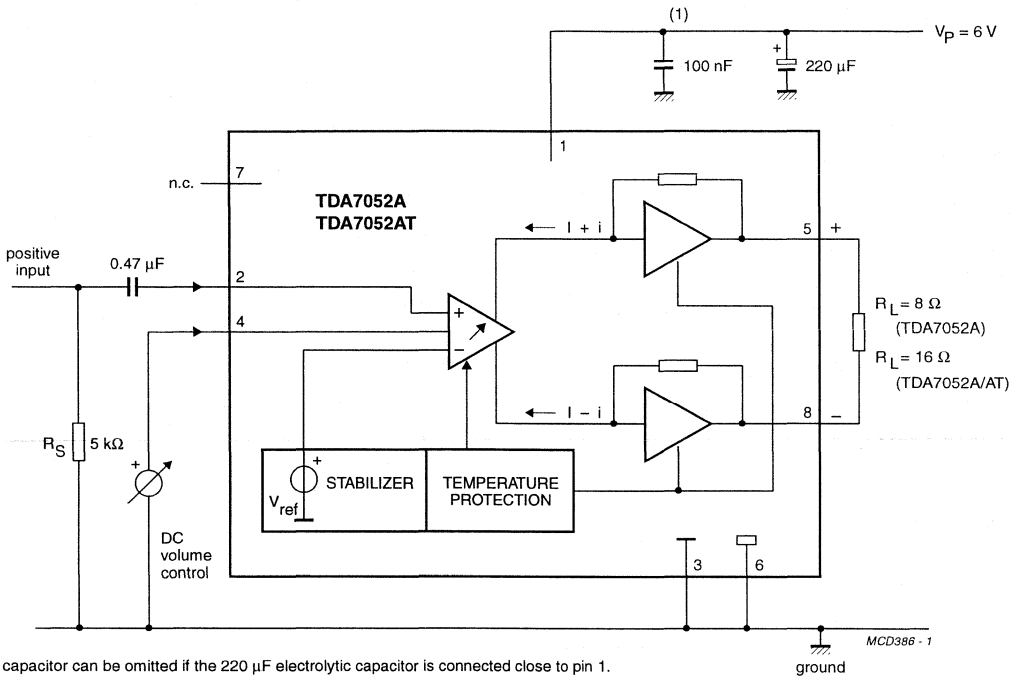


Fig.5 Control current as a function of DC volume control.

APPLICATION INFORMATION



This capacitor can be omitted if the 220 µF electrolytic capacitor is connected close to pin 1.

Fig.6 Test and application diagram.

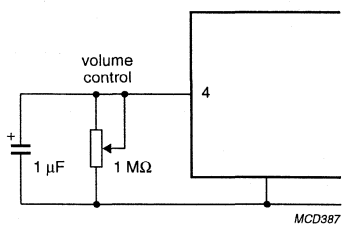


Fig.7 Application with potentiometer as volume control; maximum gain = 30 dB.

IC card interface TDA8002

FEATURES

- Single supply voltage interface (3.3 or 5 V environment)
- Low-power sleep mode
- Three specific protected half-duplex bidirectional buffered I/O lines
- V_{CC} regulation (5 V ±5%, I_{CC} <65 mA at V_{DD} = 5 V, with controlled rise and fall times
- Thermal and short-circuit protections with current limitations
- Automatic ISO 7816 activation and deactivation sequences
- Enhanced ESD protections on card side (>6 kV)
- Clock generation for the card up to 12 MHz with synchronous frequency changes
- Clock generation up to 20 MHz (auxiliary clock)
- Synchronous and asynchronous cards (memory and smart cards)
- ISO 7816, GSM11.11 compatibility and EMV (Europay, Mastercard, Visa) compliant
- Step-up converter for V_{CC} generation
- Supply supervisor for spikes elimination and emergency deactivation.

APPLICATIONS

- IC card readers for:
  - GSM applications
  - banking
  - electronic payment
  - identification
  - Pay TV
  - road tolling.

GENERAL DESCRIPTION

The TDA8002 is a complete low-power, analog interface for asynchronous and synchronous cards. It can be placed between the card and the microcontroller. It performs all supply, protection and control functions. It is directly compatible with ISO 7816, GSM11.11 and EMV specifications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DDA}	analog supply voltage		3.0	5	6.5	V
I_{DD}	supply current	sleep mode	–	–	150	µA
		idle mode; f_{CLK} = 2.5 MHz; f_{CLKOUT} = 10 MHz; V_{DD} = 5 V	–	–	6	mA
		active mode; f_{CLK} = 2.5 MHz; f_{CLKOUT} = 10 MHz; V_{DD} = 5 V	–	–	9	mA
		active mode; f_{CLK} = 2.5 MHz; f_{CLKOUT} = 10 MHz; V_{DD} = 3 V	–	–	12	mA
Card supply						
$V_{CC(O)}$	output voltage	DC load <65 mA	4.75	–	5.25	V
$I_{CC(O)}$	output current	V_{CC} short-circuited to GND	–	–	100	mA
General						
f_{CLK}	card clock frequency		0	–	12	MHz
T_{de}	deactivation cycle time		60	80	100	µs
P_{tot}	continuous total power dissipation					
	TDA8002AT; TDA8002BT	T_{amb} = −25 to +85 °C	–	–	0.56	W
	TDA8002G	T_{amb} = −25 to +85 °C	–	–	0.46	W
T_{amb}	operating ambient temperature		−25	–	+85	°C

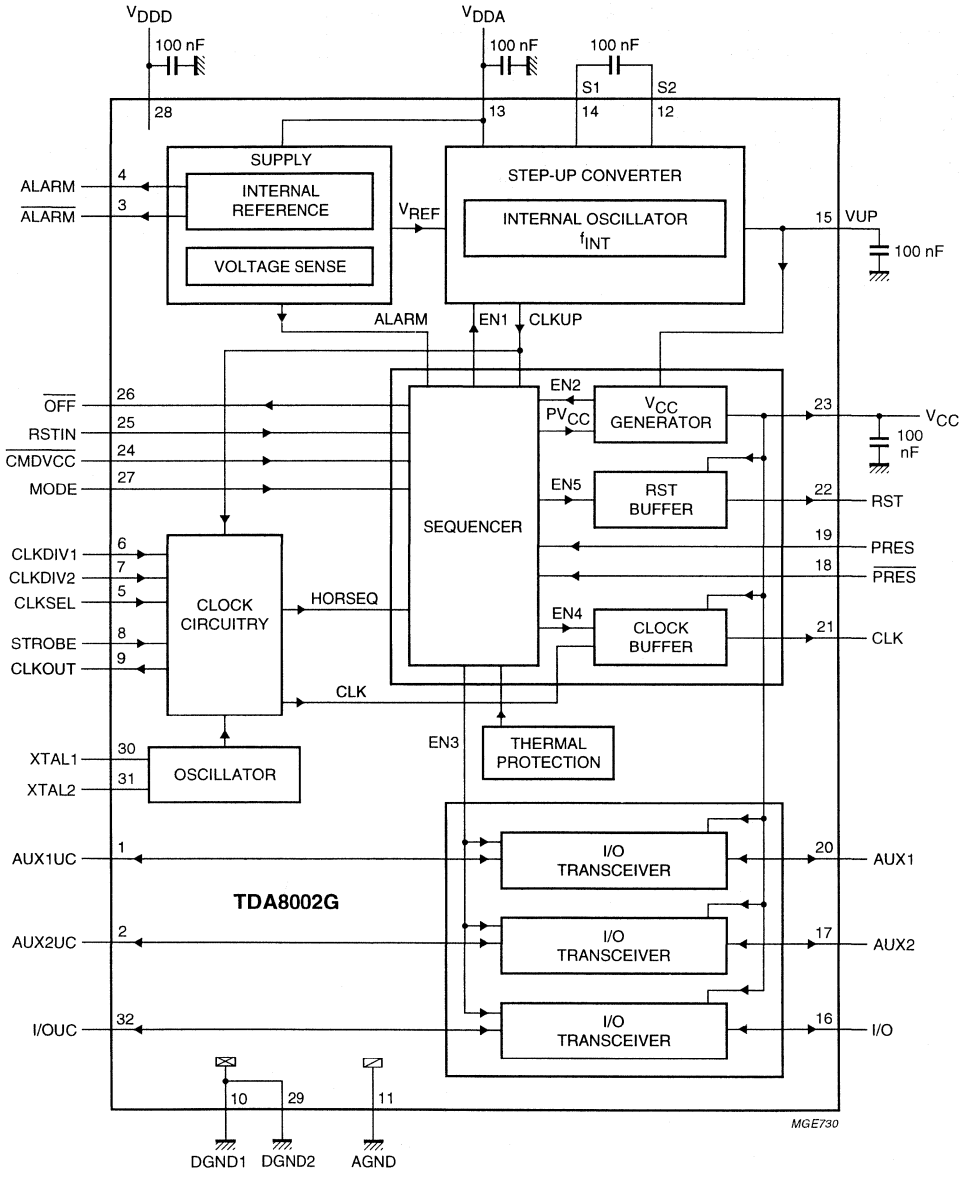
ORDERING INFORMATION

TYPE NUMBER[1]	PACKAGE			
	MARKING	NAME	DESCRIPTION	VERSION
TDA8002AT/3/C2[2]	TDA8002AT/3	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
TDA8002AT/5/C2[3]	TDA8002AT/5			
TDA8002BT/3/C2[2]	TDA8002BT/3			
TDA8002BT/5/C2[3]	TDA8002BT/5			
TDA8002G/3/C2[2]	80023	LQFP32	plastic low profile quad flat package; 32 leads; body 5 × 5 × 1.4 mm	SOT401-1
TDA8002G/5/C2[3]	80025			

Notes

1. The /3 or /5 suffix indicates the voltage supervisor option.
2. The /3 version can be used with a 3 or 5 V power supply environment (see Chapter "Functional description").
3. The /5 version can be used with a 5 V power supply environment.

BLOCK DIAGRAM



All capacitors are mandatory.

Fig.1 Block diagram (TDA8002G).

PINNING

SYMBOL	PIN			I/O	DESCRIPTION
	TYPE A	TYPE B	TYPE G		
XTAL1	1	1	30	I/O	crystal connection or input for external clock
XTAL2	2	2	31	I/O	crystal connection
I/OUC	3	3	32	I/O	data I/O line to and from microcontroller
AUX1UC	4	4	1	I/O	auxiliary line to and from microcontroller for synchronous applications
AUX2UC	5	–	2	I/O	auxiliary line to and from microcontroller for synchronous applications
$\overline{\text{ALARM}}$	–	5	3	O	open drain NMOS reset output for microcontroller (active LOW)
ALARM	6	6	4	O	open drain PMOS reset output for microcontroller (active HIGH)
CLKSEL	7	7	5	I	control input signal for CLK (LOW = XTAL oscillator; HIGH = STROBE input)
CLKDIV1	8	8	6	I	control input with CLKDIV2 for choosing CLK frequency
CLKDIV2	9	9	7	I	control input with CLKDIV1 for choosing CLK frequency
STROBE	10	10	8	I	external clock input for synchronous applications
CLKOUT	11	11	9	O	clock output (see Table 1)
DGND1	12	12	10	supply	digital ground 1
AGND	13	13	11	supply	analog ground
S2	14	14	12	I/O	capacitance connection for voltage doubler
V_{DDA}	15	15	13	supply	analog supply voltage
S1	16	16	14	I/O	capacitance connection for voltage doubler
VUP	17	17	15	I/O	output of voltage doubler (connect to 100 nF)
I/O	18	18	16	I/O	data I/O line to and from card
AUX2	19	–	17	I/O	auxiliary I/O line to and from card
$\overline{\text{PRES}}$	20	19	18	I	active LOW card input presence contact
PRES	–	20	19	I	active HIGH card input presence contact
AUX1	21	21	20	I/O	auxiliary I/O line to and from card
CLK	22	22	21	O	clock to card output (C3) (see Table 1)
RST	23	23	22	O	card reset output (C2)
V_{CC}	24	24	23	O	supply for card (C1) (decouple with 100 nF)
$\overline{\text{CMDVCC}}$	25	25	24	I	active LOW start activation sequence input from microcontroller
RSTIN	26	26	25	I	card reset input from microcontroller
$\overline{\text{OFF}}$	27	27	26	O	open drain NMOS interrupt output to microcontroller (active LOW)
MODE	28	28	27	I	operating mode selection input (HIGH = normal; LOW = sleep)
V_{DDD}	–	–	28	supply	digital supply voltage
DGND2	–	–	29	supply	digital ground 2

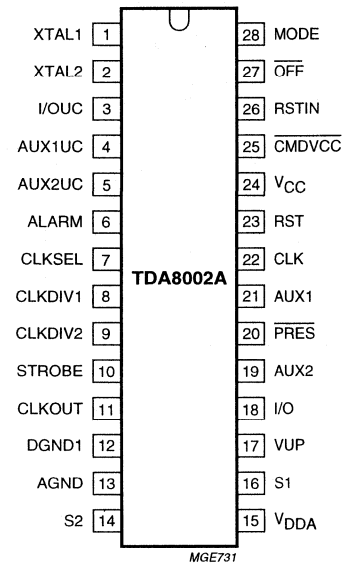


Fig.2 Pin configuration (TDA8002A).

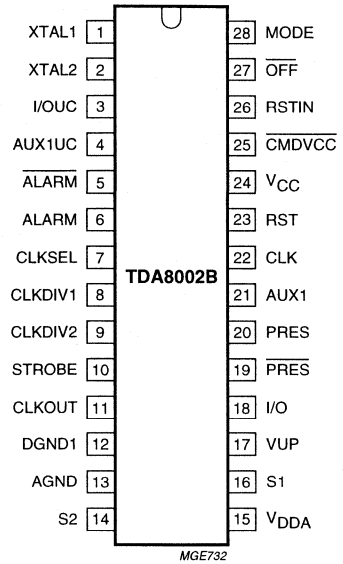


Fig.3 Pin configuration (TDA8002B).

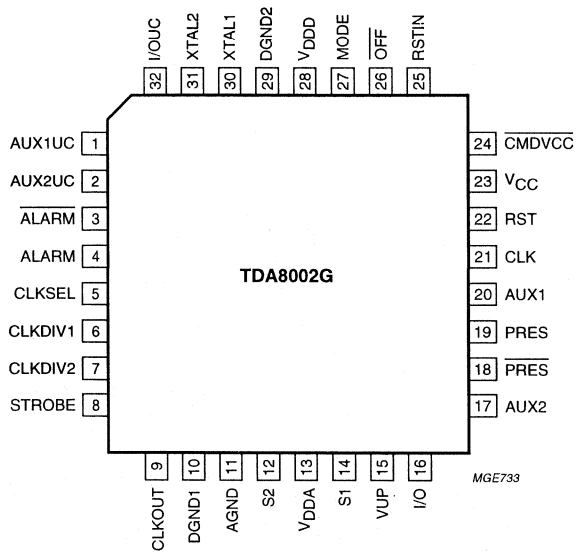


Fig.4 Pin configuration (TDA8002G).

FUNCTIONAL DESCRIPTION

Power supply

The supply pins for the chip are V_{DDA}, V_{DDD}, AGND, DGND1 and DGND2. V_{DDA} and V_{DDD} (i.e. V_{DD}) should be in the range of 3.0 to 6.5 V. All card contacts remain inactive during power-up or power-down.

On power-up, the logic is reset by an internal signal. The sequencer is not activated until V_{DD} reaches $V_{th2} + V_{hys2}$ (see Fig.5). When V_{DD} falls below V_{th2}, an automatic deactivation sequence of the contacts is performed.

Supply voltage supervisor (V_{DD})

This block surveys the V_{DD} supply. A defined reset pulse of 10 ms minimum (t_W) can be retriggered and is delivered on the ALARM outputs during power-up or power-down of V_{DD} (see Fig.5). This signal is also used for eliminating the spikes on card contacts during power-up or power-down.

When V_{DD} reaches $V_{th2} + V_{hys2}$, an internal delay is started. The ALARM outputs are active until this delay has expired. When V_{DD} falls below V_{th2}, ALARM is activated and a deactivation sequence of the contacts is performed.

For 3 V supply, the supervisor option must be chosen at 3 V. For 5 V supply, both options (3 or 5 V) may be chosen depending on the application.

Clock circuitry

The TDA8002 supports both synchronous and asynchronous cards (I^2C-bus memories requiring an acknowledge signal from the master are not supported). There are three methods to clock the circuitry:

- Apply a clock signal to pin STROBE
- Use of an internal RC oscillator
- Use of a quartz oscillator which should be connected between pins XTAL1 and XTAL2.

When CLKSEL is HIGH, the clock should be applied on the STROBE pin, and when CLKSEL is LOW, one of the internal oscillators is used.

When an internal clock is used, the clock output is available on pin CLKOUT. The RC oscillator is selected by making CLKDIV1 HIGH and CLKDIV2 LOW. The clock output to the card is available on pin CLK. The frequency of the card clock can be the input frequency divided by 2 or 4, STOP LOW or 1.25 MHz, depending on the states of CLKDIV1 or CLKDIV2 (see Table 1).

Do not change CLKSEL during activation. When in low-power (sleep) mode, the internal oscillator frequency which is available on pin CLKOUT is lowered to approximately 16 kHz for power-economy purposes.

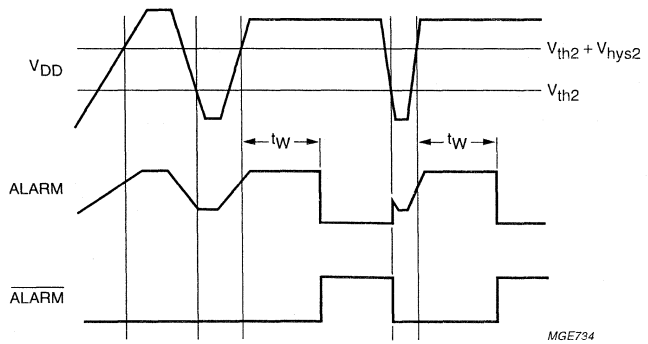


Fig.5 Alarm as a function of V_{DD} (pulse width 10 ms).

Table 1 Clock circuitry definition

MODE	CLKSEL	CLKDIV1	CLKDIV2	FREQUENCY OF CLK	FREQUENCY OF CLKOUT
HIGH	LOW	HIGH	LOW	$\frac{1}{2}f_{int}$	$\frac{1}{2}f_{int}$
HIGH	LOW	LOW	LOW	$\frac{1}{4}f_{xtal}$	f_{xtal}
HIGH	LOW	LOW	HIGH	$\frac{1}{2}f_{xtal}$	f_{xtal}
HIGH	LOW	HIGH	HIGH	STOP LOW	f_{xtal}
HIGH	HIGH	X(1)	X(1)	STROBE	f_{xtal}
LOW(2)	X(1)	X(1)	X(1)	STOP LOW	$\frac{1}{2}f_{int}$(3)

Notes

1. X = don't care.
2. In low-power mode.
3. f_{int} = 32 kHz in low-power mode.

I/O circuitry

The three I/O transceivers are identical. The state is HIGH for all I/O pins (i.e. I/O, I/OUC, AUX1, AUX1UC, AUX2 and AUX2UC). Pin I/O is referenced to V_{CC} and pin I/OUC to V_{DD}, thus ensuring proper operation in case $V_{CC} \neq V_{DD}$.

The first side on which a falling edge is detected becomes a master (input). An anti-latch circuitry first disables the detection of the falling edge on the other side, which becomes slave (output).

After a delay time t_d (about 50 ns), the logic 0 present on the master side is transferred on the slave side.

When the input is back to HIGH level, a current booster is turned on during the delay t_d on the output side and then both sides are back to their idle state, ready to detect the next logic 0 on any side.

In case of a conflict, both lines may remain LOW until the software enables the lines to be HIGH. The anti-latch circuitry ensures that the lines do not remain LOW if both sides return HIGH, regardless of the prior conditions. The maximum frequency on the lines is approximately 1 MHz.

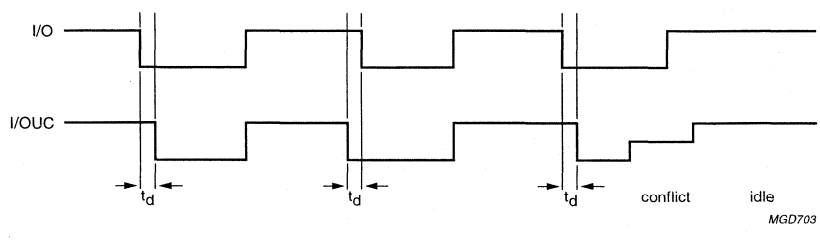


Fig.6 Master and slave signals.

Logic circuitry

After power-up, the circuit has six possible states of operation. Table 1 shows the sequence of these states.

IDLE MODE

After reset, the circuit enters the idle mode.
A minimum number of functions in the circuit are active while waiting for the microcontroller to start a session:

- All card contacts are inactive
- I/OUC, AUX1UC and AUX2UC are high-impedance
- Oscillator XTAL runs, delivering CLKOUT
- Voltage supervisor is active.

LOW-POWER (SLEEP) MODE

When pin MODE goes LOW, the circuit enters the low-power (sleep) mode. As long as pin MODE is LOW, no activation is possible.

If pin MODE goes LOW in the active mode, a normal deactivation sequence is performed before entering low-power mode. When pin MODE goes HIGH, the circuit enters normal operation after a delay of at least 6 ms (96 cycles of CLKOUT). During this time the CLKOUT remains at 16 kHz.

- All card contacts are inactive
- Oscillator XTAL does not run
- The V_{DD} supervisor, ALARM output, card presence detection and $\overline{OFF}$ output remain functional
- Internal oscillator is slowed to 32 kHz, CLKOUT providing 16 kHz.

ACTIVE MODE

When the activation sequence is completed, the TDA8002 will be in the active mode. Data is exchanged between the card and the microcontroller via the I/O lines.

State diagram

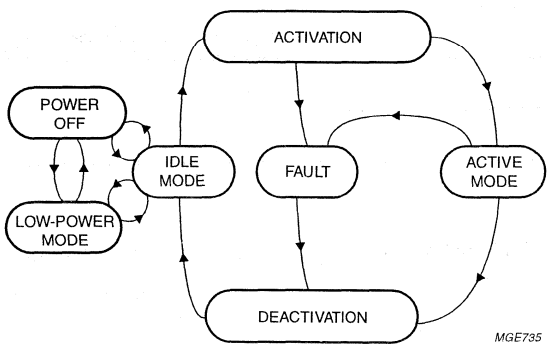


Fig.7 State diagram.

ACTIVATION SEQUENCE

From idle mode, the circuit enters the activation mode when the microcontroller sets the $\overline{\text{CMDVCC}}$ line LOW or sets the MODE line HIGH when the $\overline{\text{CMDVCC}}$ line is already LOW. The internal circuitry is then activated, the internal clock is activated and an activation sequence is executed. When RST is enabled, it becomes the inverse of RSTIN.

Figures 8 to 10 illustrate the activation sequence as described below:

1. Step-up converter is started ($t_1 \approx t_0$)
2. V_{CC} rises from 0 to 5 V ($t_2 = t_1 + 1\frac{1}{2}T$)
3. I/O, AUX1, AUX2 are enabled and CLK is enabled ($t_3 = t_1 + 4T$); a special circuitry ensures that I/O remains below V_{CC} during falling slope of V_{CC}
4. CLK is set by setting RSTIN to HIGH (t_4)
5. RST is enabled ($t_5 = t_1 + 7T$); after t_5, RSTIN has no further action on CLK, but is only controlling RST.

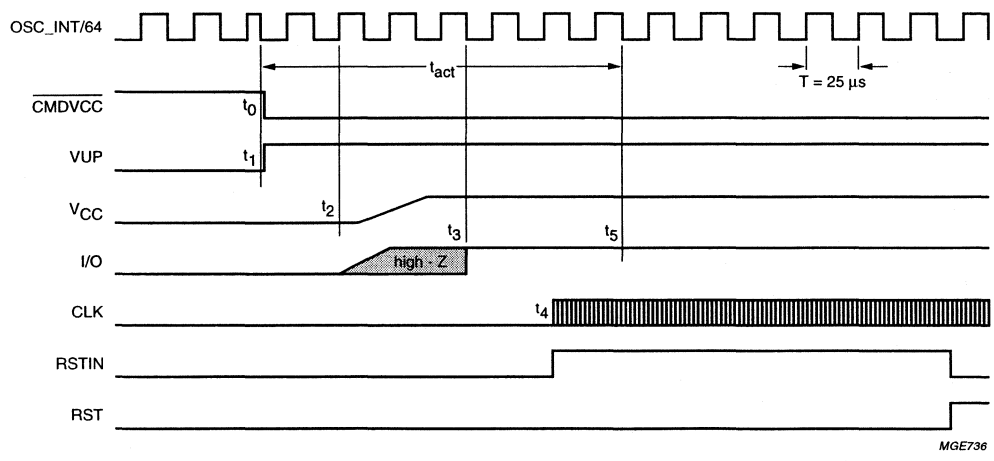


Fig.8 Activation sequence using RSTIN and $\overline{\text{CMDVCC}}$.

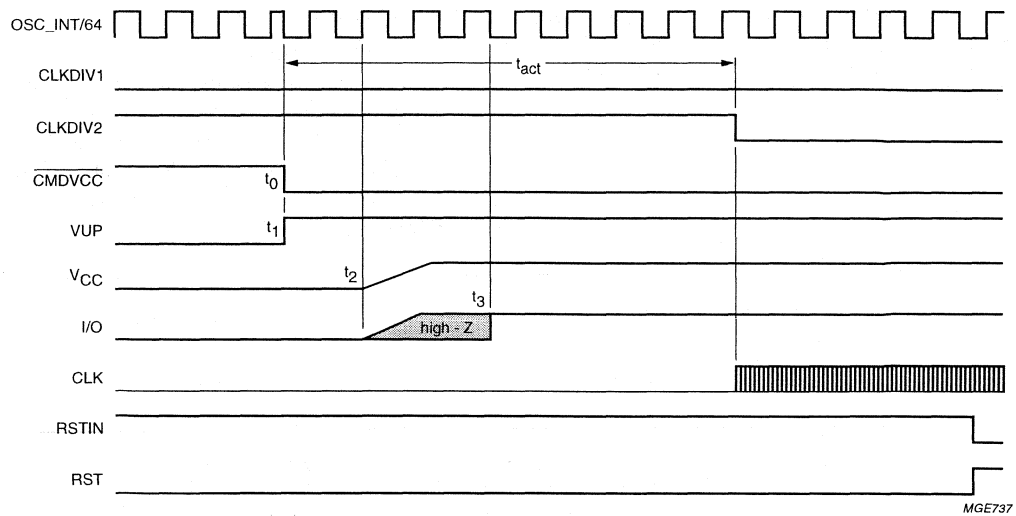


Fig.9 Activation sequence using $\overline{\text{CMDVCC}}$, CLKDIV1 and CLKDIV2 signals to enable CLK.

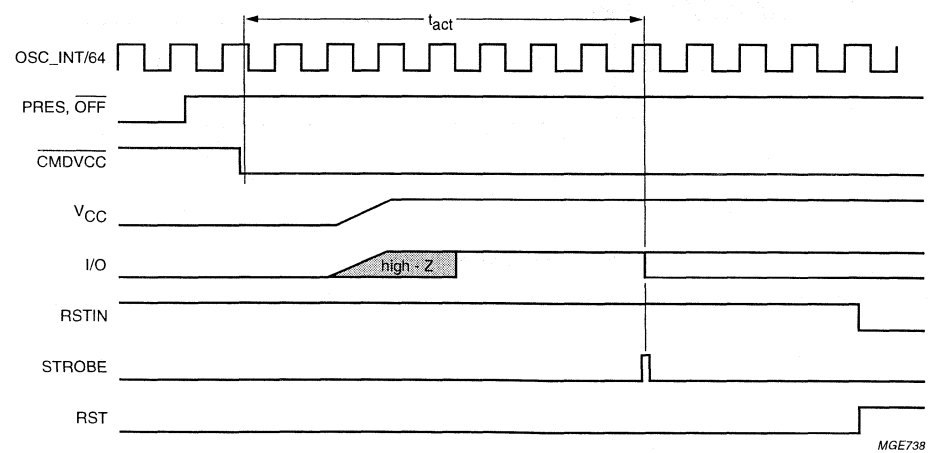


Fig.10 Activation sequence for synchronous application.

DEACTIVATION SEQUENCE

When a session is completed, the microcontroller sets the $\overline{\text{CMDVCC}}$ line to HIGH state or MODE line to LOW state. The circuit then executes an automatic deactivation sequence by counting the sequencer down and ends in idle mode.

Figures 11 and 12 illustrate the deactivation sequence as described below:

1. RST goes LOW ($t_{11} \approx t_{10}$)
2. CLK is stopped ($t_{12} = t_{11} + \frac{1}{2}T$)
3. I/O, AUX1, AUX2 are outputs into high-impedance state ($t_{13} = t_{11} + T$)
4. V_{CC} falls to zero ($t_{14} = t_{11} + 1\frac{1}{2}T$); a special circuitry ensures that I/O remains below V_{CC} during falling slope of V_{CC}
5. VUP falls ($t_{15} = t_{11} + 5T$).

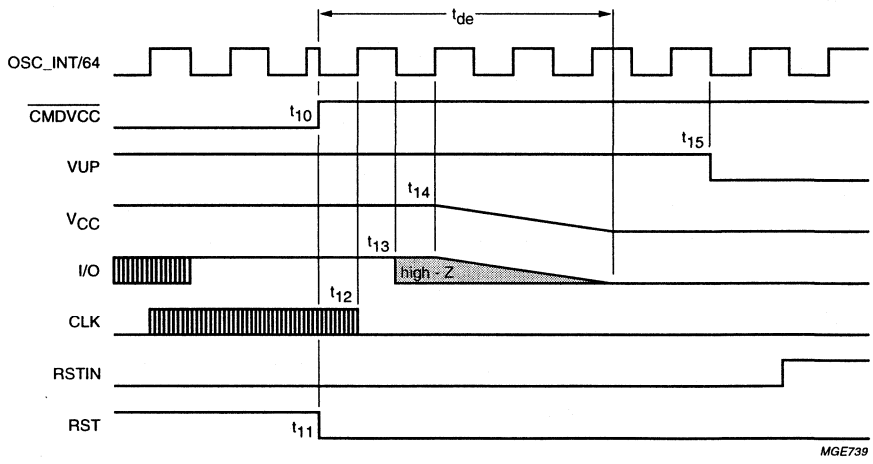


Fig.11 Deactivation sequence.

Fault detection

The following fault conditions are monitored by the circuit:

- Short-circuit or high current on V_{CC}
- Removing card during transaction
- V_{DD} dropping
- Overheating.

When one or more of these faults are detected, the circuit pulls the interrupt line $\overline{OFF}$ to its active LOW state and a deactivation sequence is initiated. In case the card is present the interrupt line $\overline{OFF}$ is set to HIGH when the microcontroller has reset the $\overline{CMDVCC}$ line HIGH (after completion of the deactivation sequence). In case the card is not present $\overline{OFF}$ remains LOW.

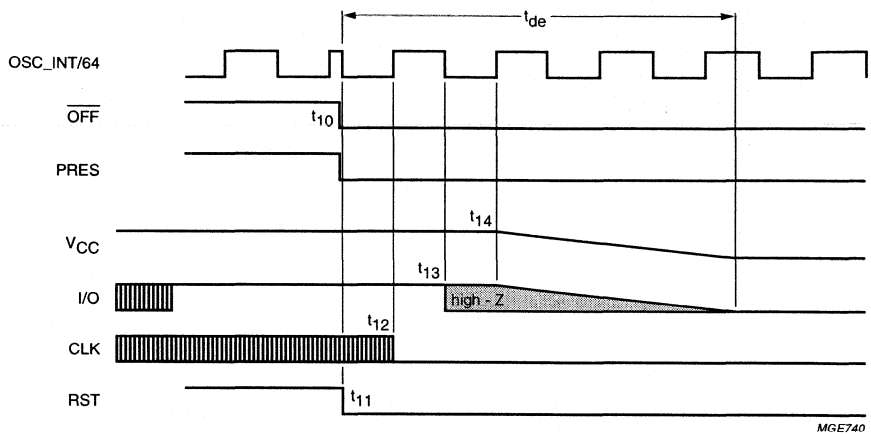


Fig.12 Emergency deactivation sequence.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); note 1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		−0.3	+6.5	V
$V_{i(CMOS)}$	voltage on CMOS pins XTAL1, XTAL2, ALARM, $\overline{\text{ALARM}}$, MODE, RSTIN, CLKSEL, AUX2UC, AUX1UC, CLKDIV1, CLKDIV2, CLKOUT, STROBE, $\overline{\text{CMDVCC}}$ and $\overline{\text{OFF}}$		−0.3	+6.5	V
$V_{i(card)}$	voltage on card contact pins I/O, AUX2, $\overline{\text{PRES}}$, PRES, AUX1, CLK, RST and V_{CC}		−0.3	+6.5	V
V_{es}	electrostatic handling on pins I/O, RST, V_{CC}, CLK, AUX1, AUX2, PRES and $\overline{\text{PRES}}$		−6	+6	kV
	on all other pins		−2	+2	kV
T_{stg}	storage temperature		−55	+125	°C
P_{tot}	continuous total power dissipation				
	TDA8002T	T_{amb} = −25 to +85 °C	−	0.56	W
	TDA8002G	T_{amb} = −25 to +85 °C	−	0.46	W
T_{amb}	operating ambient temperature		−25	+85	°C
T_j	junction temperature		−	150	°C

Note

1. Stress beyond these levels may cause permanent damage to the device. This is a stress rating only and functional operation of the device under this condition is not implied.

HANDLING

Every pin withstands the ESD test according to MIL-STD-883C class 3 for card contacts, class 2 for the remaining. Method 3015 (HBM 1500 Ω, 100 pF) 3 positive pulses and 3 negative pulses on each pin referenced to ground.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient in free air		
	SOT136-1	70	K/W
	SOT401-1	91	K/W

CHARACTERISTICS

V_{DD} = 5 V; T_{amb} = 25 °C; f_{xtal} = 10 MHz; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	positive supply voltage	option 5 V power supply (TDA8002xx/5)	4.5	5	6.5	V
		option 3.3 V or 5 V power supply (TDA8002xx/3)	3	5	6.5	V
$I_{DD(sl)}$	supply current	sleep mode; V_{DD} = 5 V	–	–	200	µA
$I_{DD(idle)}$	supply current	idle mode; V_{DD} = 5 V; f_{CLK} = 2.5 MHz; f_{CLKOUT} = 10 MHz	–	–	6	mA
$I_{DD(active)}$	supply current	active mode				
		V_{DD} = 5 V; f_{CLK} = 2.5 MHz; f_{CLKOUT} = 10 MHz	–	–	9	mA
		V_{DD} = 3.3 V; f_{CLK} = 2.5 MHz; f_{CLKOUT} = 10 MHz	–	–	12	mA
V_{th2}	threshold voltage on V_{DD} for voltage supervisor	falling				
		option 5 V power supply (TDA8002xx/5)	3.9	4.05	4.2	V
		option 3.3 V or 5 V power supply (TDA8002xx/3)	2.6	2.7	2.8	V
		rising				
		option 5 V power supply (TDA8002xx/5)	4	4.2	4.4	V
		option 3.3 or 5 V power supply (TDA8002xx/3)	2.7	2.85	2.99	V
V_{hys2}	hysteresis on V_{th2}		100	150	200	mV
CARD SUPPLY						
$V_{CC(O)(idle)}$	output voltage	idle mode	–	–	0.4	V
$V_{CC(O)(active)}$	output voltage	active mode				
		I_{CC} < 20 mA: DC load with 3 V < V_{DD} < 3.3 V	4.75	–	5.25	V
		I_{CC} < 65 mA: DC load with 3.3 V < V_{DD} < 6.5 V	4.75	–	5.25	V
		I_{CC} = 40 mA: AC load	4.6	–	5.4	V
$I_{CC(O)}$	output current	$V_{CC(O)}$ = from 0 to 5 V	–	–	65	mA
		V_{CC} short-circuited to ground	–	–	100	mA
SR	slew rate	rising or falling slope	0.12	0.17	0.22	V/µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Crystal connections (XTAL1 and XTAL2)						
C_{ext}	external capacitors	note 1	–	15	–	pF
f_{xtal}	resonance frequency	note 2	2	–	24	MHz
Data lines						
GENERAL						
t_{edge}	delay between falling edge of I/O, AUX1, AUX2 and I/OUC, AUX1UC, AUX2UC		–	200	–	ns
	delay between falling edge of I/OUC, AUX1UC, AUX2UC and I/O, AUX1, AUX2		–	200	–	ns
t_r, t_f	rise and fall times	$C_i = C_o = 30$ pF	–	–	0.5	µs
DATA LINES I/O, AUX1 AND AUX2						
$V_{OH(I/O)}$	HIGH-level output voltage on data lines	$I_{OH} = -20$ µA	$V_{CC} - 0.5$	–	$V_{CC} + 0.1$	V
		$I_{OH} = -100$ µA	3.5	–	–	V
$V_{OL(I/O)}$	LOW-level output voltage on data lines	$I_{I/O} = 1$ mA	–	–	300	mV
$V_{IH(I/O)}$	HIGH-level input voltage on data lines		1.8	–	V_{CC}	V
$V_{IL(I/O)}$	LOW-level input voltage on data lines		0	–	0.8	V
$V_{I/O(idle)}$	voltage on data lines outside a session		–	–	0.4	V
R_{pu}	internal pull-up resistance between data lines and V_{CC}		8	10	12	kΩ
I_{edge}	current from data lines when active pull-up is active		–	1	–	mA
$I_{IL(I/O)}$	LOW-level input current on data lines	$V_{IL} = 0.4$ V	–	–	–600	µA
$I_{IH(I/O)}$	HIGH-level input current on data lines	$V_{IH} = V_{CC}$	–	–	10	µA
DATA LINES I/OUC, AUX1UC AND AUX2UC						
$V_{OH(I/OUC)}$	HIGH-level output voltage on data lines	$I_{OH} = -20$ µA	$V_{DD} - 1$	–	$V_{DD} + 0.2$	V
$V_{OL(I/OUC)}$	LOW-level output voltage on data lines	$I_{I/OUC} = 1$ mA	–	–	300	mV
$V_{IH(I/OUC)}$	HIGH-level input voltage on data lines		$0.7V_{DD}$	–	V_{DD}	V
$V_{IL(I/OUC)}$	LOW-level input voltage on data lines		0	–	$0.3V_{DD}$	V
$Z_{I/OUC(idle)}$	impedance on data lines outside a session		10	–	–	MΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ALARM, $\overline{\text{ALARM}}$ and $\overline{\text{OFF}}$ when connected (open-drain outputs)						
$I_{OH(\overline{ALARM})}$	HIGH-level output current on pin $\overline{\text{ALARM}}$	$V_{OH(\overline{ALARM})}$ = 5 V	–	–	5	µA
$V_{OL(\overline{ALARM})}$	LOW-level output voltage on pin $\overline{\text{ALARM}}$	$I_{OL(\overline{ALARM})}$ = 2 mA	–	–	0.4	V
$I_{OH(OFF)}$	HIGH-level output current on pin $\overline{\text{OFF}}$	$V_{OH(OFF)}$ = 5 V	–	–	5	µA
$V_{OL(OFF)}$	LOW-level output voltage on pin $\overline{\text{OFF}}$	$I_{OL(OFF)}$ = 2 mA	–	–	0.4	V
$I_{OL(ALARM)}$	LOW-level output current on pin ALARM	$V_{OL(ALARM)}$ = 0 V	–	–	–5	µA
$V_{OH(ALARM)}$	HIGH-level output voltage on pin ALARM	$I_{OH(ALARM)}$ = –2 mA	V_{DD} – 1	–	–	V
t_W	ALARM pulse width		6	–	20	ms
Clock output (CLKOUT; powered from V_{DD})						
f_{CLKOUT}	frequency on CLKOUT		0	–	20	MHz
		low power	–	16	–	kHz
V_{OL}	LOW-level output voltage	I_{OL} = 1 mA	0	–	0.5	V
V_{OH}	HIGH-level output voltage	I_{OH} = –1 mA	V_{DD} – 0.5	–	–	V
t_r, t_f	rise and fall times	C_L = 15 pF; notes 3 and 5	–	–	8	ns
δ	duty factor	C_L = 15 pF; notes 3 and 5	40	–	60	%
Internal oscillator						
f_{int}	frequency of internal oscillator	active mode	2.2	2.7	3.2	MHz
		sleep mode	–	32	–	kHz
Card reset output (RST)						
$V_{O(inact)}$	output voltage	inactive modes	0	–	0.3	V
$t_{d(RST)}$	delay between RSTIN and RST	RST enabled	–	–	100	ns
V_{OL}	LOW-level output voltage	I_{OL} = 200 µA	0	–	0.3	V
V_{OH}	HIGH-level output voltage	I_{OH} = –200 µA	4.3	–	V_{CC}	V
		I_{OH} = –50 µA	V_{CC} – 0.5	–	V_{CC}	V
Card clock output (CLK)						
$V_{O(inact)}$	output voltage	inactive modes	0	–	0.3	V
V_{OL}	LOW-level output voltage	I_{OL} = 200 µA	0	–	0.3	V
V_{OH}	HIGH-level output voltage	I_{OH} = –50 µA	V_{CC} – 0.5	–	V_{CC}	V
t_r	rise time	C_L = 30 pF; note 3	–	–	8	ns
t_f	fall time	C_L = 30 pF; note 3	–	–	8	ns
δ	duty factor	C_L = 30 pF; note 3	45	–	55	%
SR	slew rate (rise and fall)		0.2	–	–	V/ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Strobe input (STROBE)						
f_{STROBE}	frequency on STROBE		0	–	20	MHz
V_{IL}	LOW-level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	–	V_{DD}	V
Logic inputs (CLKSEL, CLKDIV1, CLKDIV2, MODE, $\overline{CMDVCC}$ and RSTIN); note 4						
V_{IL}	LOW-level input voltage		0	–	0.8	V
V_{IH}	HIGH-level input voltage		1.8	–	V_{DD}	V
Logic inputs (PRES, $\overline{PRES}$); note 4						
V_{IL}	LOW-level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	–	V_{DD}	V
$I_{IL(PRES)}$	LOW-level input current on pin PRES	V_{OL} = 0 V	–	–	–10	µA
$I_{IH(PRES)}$	HIGH-level input current on pin PRES		–	–	10	µA
Protections						
T_{sd}	shut-down local temperature		–	135	–	°C
$I_{CC(sd)}$	shut-down current at V_{CC}		–	–	90	mA
Timing						
t_{act}	activation sequence duration	see Fig.9; guaranteed by design	–	180	220	µs
t_{de}	deactivation sequence duration	see Fig.11; guaranteed by design	50	70	90	µs
t_3	start of the window for sending CLK to the card	see Figs 8 and 9	–	–	130	µs
t_5	end of the window for sending CLK to the card	see Fig.8	150	–	–	µs

Notes

1. It may be necessary to put capacitors from XTAL1 and XTAL2 to ground depending on the choice of crystal or resonator.
2. When the oscillator is stopped in mode 1, XTAL1 is set to HIGH.
3. The transition time and duty cycle definitions are shown in Fig.13; $\delta = \frac{t_1}{t_1 + t_2}$
4. $\overline{PRES}$ and $\overline{CMDVCC}$ are active LOW; RSTIN and PRES are active HIGH.
5. CLKOUT transition time and duty cycle do not need to be tested.

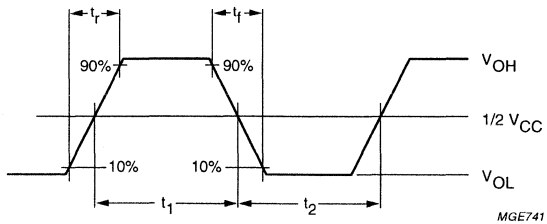


Fig.13 Definition of transition times.

APPLICATION INFORMATION

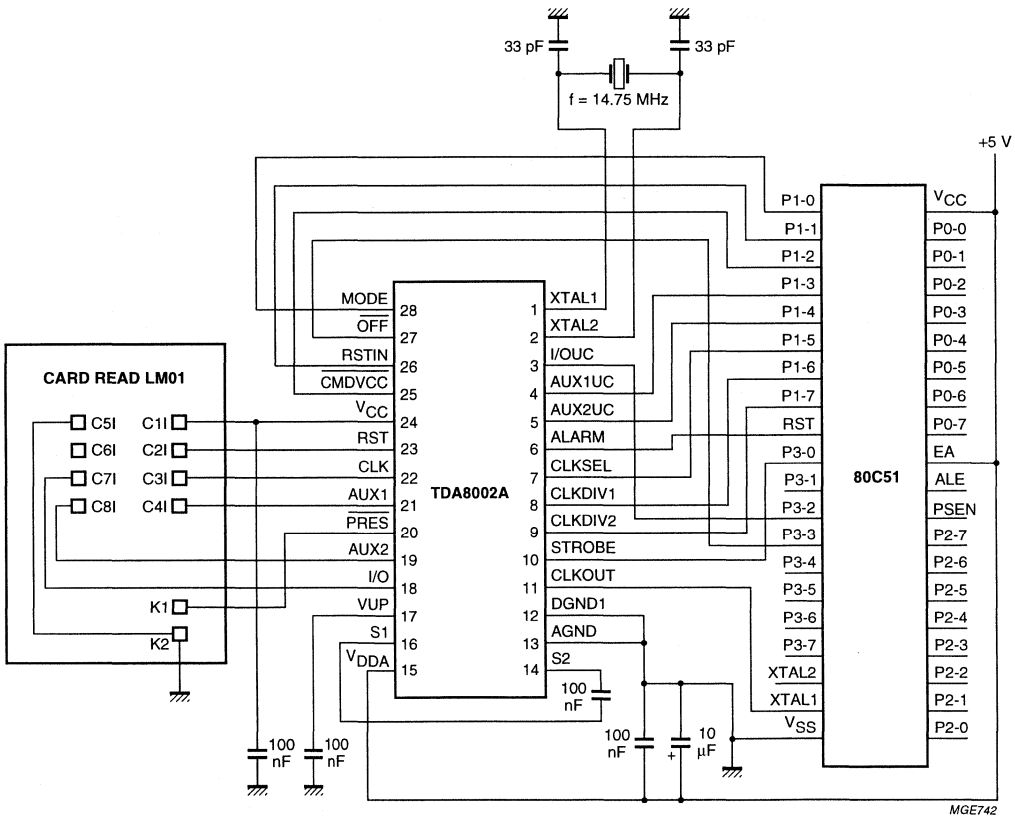


Fig.14 Application diagram (for more details, consult "*Application Note AN96096*").

Low-power smart card coupler TDA8005

FEATURES

- V_{CC} generation (5 V ±5%, 20 mA maximum with controlled rise and fall times)
- Clock generation (up to 8 MHz), with two times synchronous frequency doubling
- Clock STOP HIGH, clock STOP LOW or 1.25 MHz (from internal oscillator) for cards power-down mode
- Specific UART on I/O for automatic direct/inverse convention settings and error management at character level
- Automatic activation and deactivation sequences through an independent sequencer
- Supports the protocol T = 0 in accordance with ISO 7816, GSM11.11 requirements (Global System for Mobile communication); and EMV banking specification approved for Final GSM11.11 Test Approval (FTA)
- Several analog options are available for different applications (doubler or tripler DC/DC converter, card presence, active HIGH or LOW, threshold voltage supervisor, etc.
- Overloads and take-off protections
- Current limitations in the event of short-circuit
- Special circuitry for killing spikes during power-on or off
- Supply supervisor
- Step-up converter (supply voltage from 2.5 to 6 V)
- Power-down and sleep mode for low-power consumption
- Enhanced ESD protections on card side (6 kV minimum)
- Control and communication through a standard RS232 full duplex interface
- Optional additional I/O ports for:
  - keyboard
  - LEDs
  - display
  - etc.
- 80CL51 microcontroller core with 4 kbytes ROM and 256-byte RAM.

APPLICATIONS

- Portable smart card readers for protocol T = 0
- GSM mobile phones.

GENERAL DESCRIPTION

The TDA8005 is a low cost card interface for portable smart card readers. Controlled through a standard serial interface, it takes care of all ISO 7816 and GSM11-11 requirements. It gives the card and the set a very high level of security, due to its special hardware against ESD, short-circuiting, power failure, etc. Its integrated step-up converter allows operation within a supply voltage range of 2.5 to 6 V.

The very low-power consumption in Power-down and sleep modes saves battery power. A special version where the internal connections to the controller are fed outside through pins allows easy development and evaluation, together with a standard 80CL51 microcontroller.

Development tools, application report and support (hardware and software) are available.

The device can be supplied either as a masked chip with standard software handling all communication between smart card and a master controller in order to make the application easier, or as a maskable device.

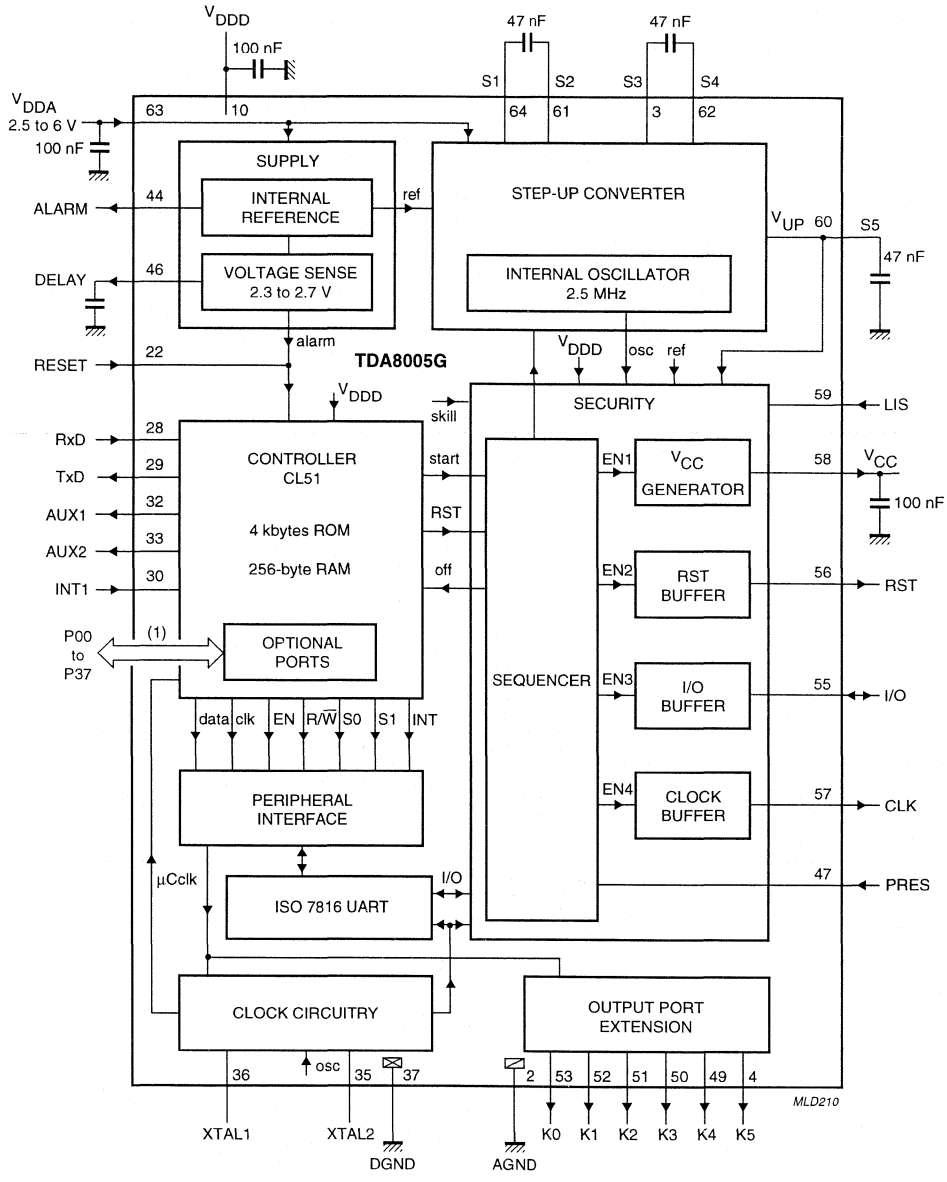
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	doubler and tripler option	2.5	–	6.0	V
$I_{DD(pd)}$	supply current in power-down mode	V_{DD} = 5 V; card inactive	–	–	100	µA
$I_{DD(sm)}$	supply current in sleep mode doubler	card powered but clock stopped	–	–	500	µA
$I_{DD(sm)}$	supply current in sleep mode tripler	card powered but clock stopped	–	–	500	µA
$I_{DD(om)}$	supply current in operating mode	unloaded; f_{xtal} = 13 MHz; $f_{\mu C}$ = 6.5 MHz; f_{card} = 3.25 MHz	–	–	5.5	mA
V_{CC}	card supply voltage	including static and dynamic loads on 100 nF capacitor	4.75	5.0	5.25	V
I_{CC}	card supply current	operating	–	–	20	mA
		limitation	–	–	30	mA
SR	slew rate on V_{CC} (rise and fall)	maximum load capacitor 150 nF (including typical 100 nF decoupling)	0.05	0.1	0.15	V/µs
t_{de}	deactivation cycle duration		–	–	100	µs
t_{act}	activation cycle duration		–	–	100	µs
f_{xtal}	crystal frequency		2	–	16	MHz
T_{amb}	operating ambient temperature		–25	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8005G	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
TDA8005H	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2

BLOCK DIAGRAM



(1) For details see Chapter "Pinning".

Fig.1 Block diagram (LQFP64; SOT314-2).

PINNING

SYMBOL	PIN		DESCRIPTION
	LQFP64 SOT314-2	QFP44 SOT307-2	
n.c.	1	–	not connected
AGND	2	1	analog ground
S3	3	2	contact 3 for the step-up converter
K5	4	–	output port from port extension
P03	5	3	general purpose I/O port (connected to P03)
P02	6	4	general purpose I/O port (connected to P02)
P01	7	5	general purpose I/O port (connected to P01)
n.c.	8	–	not connected
P00	9	6	general purpose I/O port (connected to P00)
V_{DDD}	10	7	digital supply voltage
n.c.	11	–	not connected
TEST1	12	8	test pin 1 (connected to P10; must be left open-circuit in the application)
P11	13	9	general purpose I/O port or interrupt (connected to P11)
P12	14	10	general purpose I/O port or interrupt (connected to P12)
P13	15	11	general purpose I/O port or interrupt (connected to P13)
P14	16	12	general purpose I/O port or interrupt (connected to P14)
n.c.	17	–	not connected
P15	18	13	general purpose I/O port or interrupt (connected to P15)
P16	19	14	general purpose I/O port or interrupt (connected to P16)
TEST2	20	15	test pin 2 (connected to PSEN; must be left open-circuit in the application)
P17	21	16	general purpose I/O port or interrupt (connected to P17)
RESET	22	17	input for resetting the microcontroller (active HIGH)
n.c.	23	–	not connected
n.c.	24	–	not connected
n.c.	25	–	not connected
n.c.	26	–	not connected
n.c.	27	–	not connected
RxD	28	18	serial interface receive line
TxD	29	19	serial interface transmit line
INT1	30	20	general purpose I/O port or interrupt (connected to P33)
T0	31	21	general purpose I/O port (connected to P34)
AUX1	32	22	push-pull auxiliary output (±5 mA; connected to timer T1 e.g. P35)
AUX2	33	23	push-pull auxiliary output (±5 mA; connected to timer P36)
P37	34	24	general purpose I/O port (connected to P37)
XTAL2	35	25	crystal connection
XTAL1	36	26	crystal connection or external clock input
DGND	37	27	digital ground
n.c.	38	–	not connected

SYMBOL	PIN		DESCRIPTION
	LQFP64 SOT314-2	QFP44 SOT307-2	
n.c.	39	–	not connected
P20	40	28	general purpose I/O port (connected to P20)
P21	41	–	general purpose I/O port (connected to P21)
P22	42	29	general purpose I/O port (connected to P22)
P23	43	30	general purpose I/O port (connected to P23)
ALARM	44	–	open-drain output for Power-On Reset (active HIGH or LOW by mask option)
n.c.	45	–	not connected
DELAY	46	31	external capacitor connection for delayed reset signal
PRES	47	32	card presence contact input (active HIGH or LOW by mask option)
TEST3	48	33	test pin 3 (must be left open-circuit in the application)
K4	49	–	output port from port extension
K3	50	–	output port from port extension
K2	51	–	output port from port extension
K1	52	–	output port from port extension
K0	53	–	output port from port extension
TEST4	54	34	test pin 4 (must be left open-circuit in the application)
I/O	55	35	data line to/from the card (ISO C7 contact)
RST	56	36	card reset output (ISO C2 contact)
CLK	57	37	clock output to the card (ISO C3 contact)
V_{CC}	58	38	card supply output voltage (ISO C1 contact)
LIS	59	39	supply for low-impedance on cards contacts
S5	60	40	contact 5 for the step-up converter
S2	61	41	contact 2 for the step-up converter
S4	62	42	contact 4 for the step-up converter
V_{DDA}	63	43	analog supply voltage
S1	64	44	contact 1 for the step-up converter

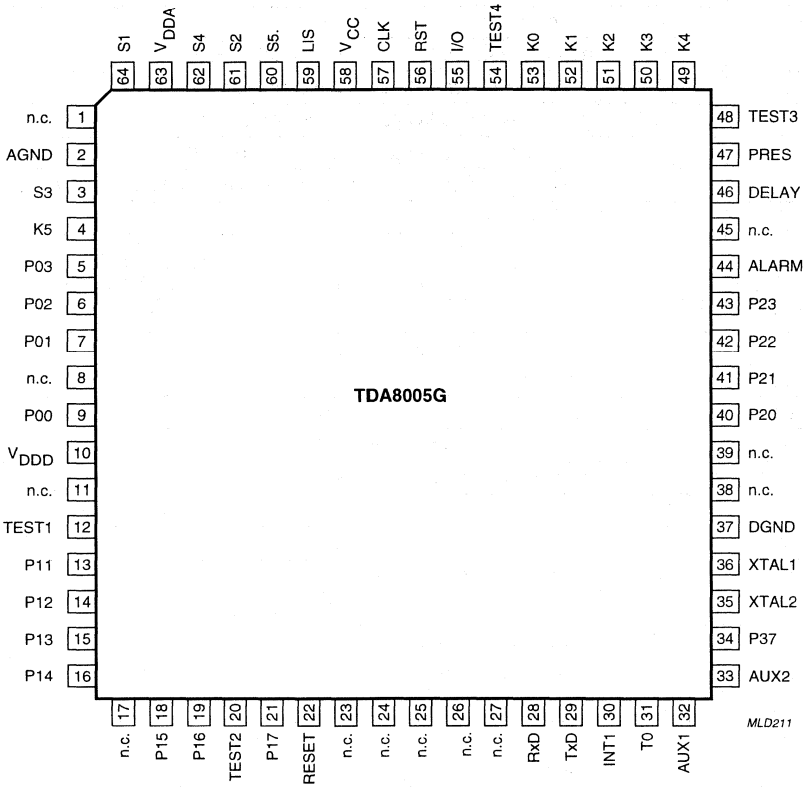


Fig.2 Pin configuration (LQFP64; SOT314-2).

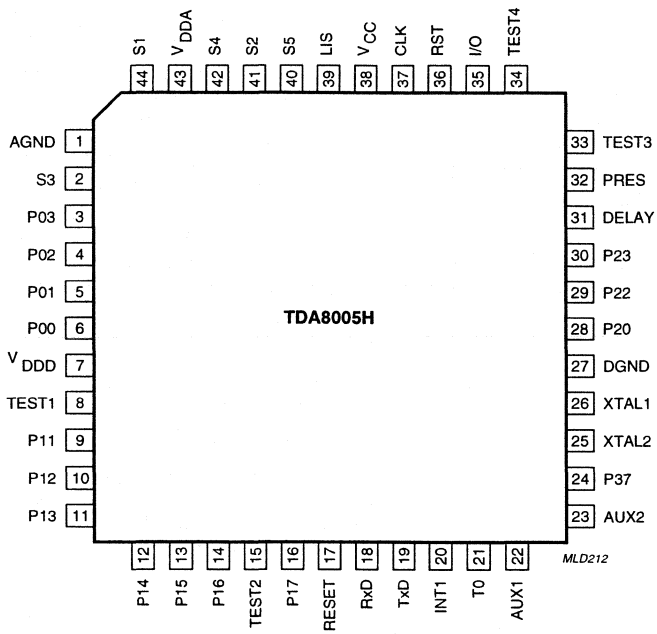


Fig.3 Pin configuration (QFP44; SOT307-2).

FUNCTIONAL DESCRIPTION

Microcontroller

The microcontroller is an 80CL51 with 256 bytes of RAM instead of 128. The baud rate of the UART has been multiplied by four in modes 1, 2 and 3 (which means that the division factor of 32 in the formula is replaced by 8 in both reception and transmission, and that in the reception modes, only four samples per bit are taken with decision on the majority of samples 2, 3 and 4) and the delay counter has been reduced from 1536 to 24.

Remark: this has an impact when getting out of PDOWN mode. It is recommended to switch to internal clock before entering PDOWN mode (see *"application report"*).

All the other functions remain unchanged. Please, refer to the published specification of the 80CL51 for any further information. Pins INT0, P10, P04 to P07 and P24 to P27 are used internally for controlling the smart card interface.

Mode 0 is unchanged. The baud rate for modes 1 and 3 is:

$$\frac{2^{SMOD}}{8} \times \frac{f_{clk}}{12 \times (256 - TH1)}$$

The baud rate for mode 2 is: $\frac{2^{SMOD}}{16} \times f_{clk}$

Table 1 Mode 3 timing

BAUD RATE	f_{clk} = 6.5 MHz; V_{DD} = 5 V		f_{clk} = 3.25 MHz; V_{DD} = 5 or 3 V	
	SMOD	TH1	SMOD	TH1
135416	1	255	–	–
67708	0	255	1	255
45139	1	253	–	–
33854	0	254	0	255
27083	1	251	–	–
22569	0	253	1	253
16927	–	–	0	254
13542	–	–	1	251
11285	0	250	0	253

Supply

The circuit operates within a supply voltage range of 2.5 to 6 V. The supply pins are V_{DDD}, DGND and AGND. Pins V_{DDA} and AGND supply the analog drivers to the card and have to be externally decoupled because of the large current spikes that the card and the step-up converter can create. An integrated spike killer ensures the contacts to the card remain inactive during power-up or power-down. An internal voltage reference is generated which is used within the step-up converter, the voltage supervisor, and the V_{CC} generator.

The voltage supervisor generates an alarm pulse, whose length is defined by an external capacitor tied to the DELAY pin, when V_{DDD} is too low to ensure proper operation (1 ms per 1 nF typical). This pulse is used as a RESET pulse by the controller, in parallel with an external RESET input, which can be tied to the system controller.

It is also used in order to either block any spurious card contacts during controllers reset, or to force an automatic deactivation of the contacts in the event of supply drop-out [see Sections "Activation sequence" and "Deactivation sequence (see Fig.10)"].

In the 64 pin version, this reset pulse is output to the open drain ALARM pin, which may be selected active HIGH or active LOW by mask option and may be used as a reset pulse for other devices within the application.

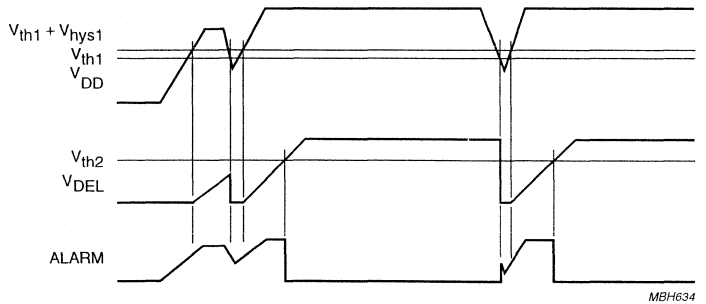


Fig.4 Supply supervisor.

Low impedance supply (pin LIS)

For some applications, it is mandatory that the contacts to the card (V_{CC}, RST, CLK and I/O) are low impedance while the card is inactive and also when the coupler is not powered. An auxiliary supply voltage on pin LIS ensures this condition where I_{LIS} = <5 µA for V_{LIS} = 5 V. This low impedance situation is disabled when V_{CC} starts rising during activation, and re-enabled when the step-up converter is stopped during deactivation. If this feature is not required, the LIS pin must be tied to V_{DD}.

Step-up converter

Except for the V_{CC} generator, and the other cards contacts buffers, the whole circuit is powered by V_{DDD} and V_{DDA}. If the supply voltage is 3 V or 5 V, then a higher voltage is needed for the ISO contacts supply. When a card session is requested by the controller, the sequencer first starts the step-up converter, which is a switched capacitors type, clocked by an internal oscillator at a frequency approximately 2.5 MHz. The output voltage, V_{UP}, is regulated at approximately 6,5 V and then fed to the V_{CC} generator. V_{CC} and GND are used as a reference for all other cards contacts. The step-up converter may be chosen as a doubler or a tripler by mask option, depending on the voltage and the current needed on the card.

ISO 7816 security

The correct sequence during activation and deactivation of the card is ensured through a specific sequencer, clocked by a division ratio of the internal oscillator.

Activation (START signal P05) is only possible if the card is present (PRES HIGH or LOW according to mask option), and if the supply voltage is correct (ALARM signal inactive), CLK and RST are controlled by RSTIN (P04), allowing the correct count of CLK pulses during Answer-to-Reset from the card.

The presence of the card is signalled to the controller by the OFF signal (P10).

During a session, the sequencer performs an automatic emergency deactivation in the event of card take-off, supply voltage drop, or hardware problems. The OFF signal falls thereby warning the controller.

Clock circuitry

The clock to the microcontroller and the clock to the card are derived from the main clock signal (XTAL from 2 to 16 MHz, or an external clock signal).

Microcontroller clock (f_{clk}) after reset, and during power reduction modes, the microcontroller is clocked with $f_{INT}/8$, which is always present because it is derived from the internal oscillator and gives the lowest power consumption. When required, (for card session, serial communication or anything else) the microcontroller may choose to clock itself with $\frac{1}{2}f_{xtal}$, $\frac{1}{4}f_{xtal}$ or $\frac{1}{2}f_{INT}$. All frequency changes are synchronous, thereby ensuring no hang-up due to short spikes etc.

Cards clock: the microcontroller may select to send the card $\frac{1}{2}f_{xtal}$, $\frac{1}{4}f_{xtal}$, $\frac{1}{8}f_{xtal}$ or $\frac{1}{2}f_{INT}$ (≈1.25 MHz), or to stop the clock HIGH or LOW. All transition are synchronous, ensuring correct pulse length during start or change in accordance with ISO 7816.

After power on, CLK is set at STOP LOW, and f_{clk} is set at $\frac{1}{8}f_{INT}$.

Power-down and sleep modes

The TDA8005 offers a large flexibility for defining power reduction modes by software. Some configurations are described below.

In the power-down mode, the microcontroller is in power-down and the supply and the internal oscillator are active. The card is not active; this is the smallest power consumption mode. Any change on P1 ports or on PRES will wake-up the circuit (for example, a key pressed on the keyboard, the card inserted or taken off).

In the sleep mode, the card is powered, but configured in the Idle or sleep mode. The step-up converter will only be active when it is necessary to reactivate V_{UP}. When the microcontroller is in Power-down mode any change on P1 ports or on PRES will wake up the circuit.

In both power reduction modes the sequencer is active, allowing automatic emergency deactivation in the event of card take-off, hardware problems, or supply drop-out.

The TDA8005 is set into Power-down or sleep mode by software. There are several ways to return to normal mode, Introduction or extraction of the card, detection of a change on P1 (which can be a key pressed) or a command from the system microcontroller. For example, if the system monitors the clock on XTAL1, it may stop this clock after setting the device into power-down mode and then wake it up when sending the clock again. In this situation, the internal clock should have been chosen before the f_{clk}.

Peripheral interface

This block allows synchronous serial communication with the three peripherals (ISO UART, CLOCK CIRCUITRY and OUTPUT PORTS EXTENSION).

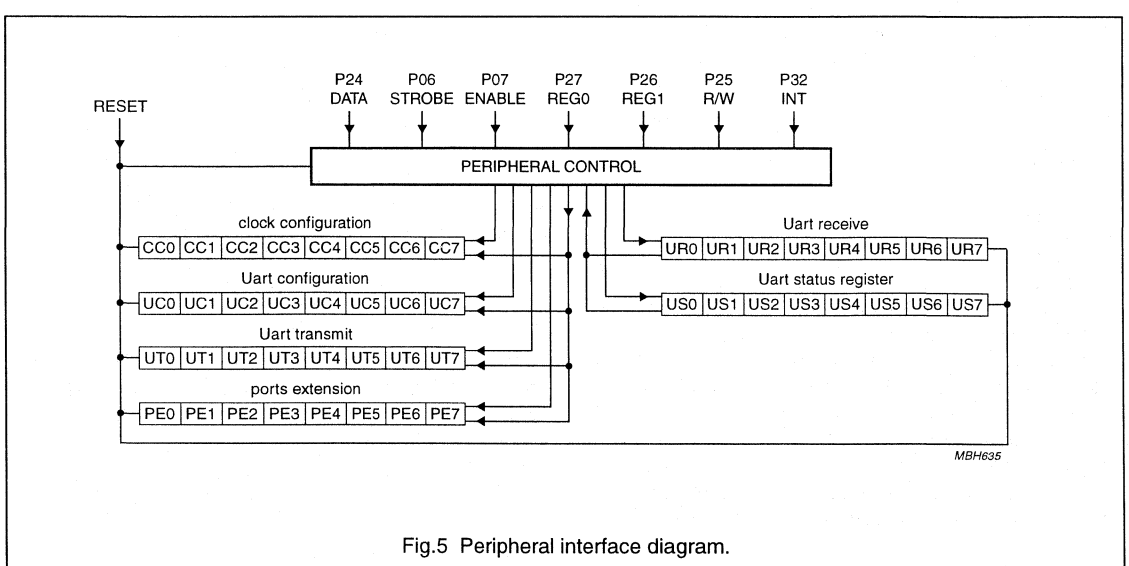


Fig.5 Peripheral interface diagram.

Table 2 Description of Fig.5

BIT NAME	DESCRIPTION
REG0 = 0, REG1 = 0, R/W = 0; CLOCK CONFIGURATION (Configuration after reset is cards clock STOP LOW, $f_{clk} = 1/8 f_{INT}$)	
CC0	cards clock = $1/2 f_{xtal}$
CC1	cards clock = $1/4 f_{xtal}$
CC2	cards clock = $1/8 f_{xtal}$
CC3	cards clock = $1/2 f_{INT}$
CC4	cards clock = STOP HIGH
CC5	$f_{clk} = 1/2 f_{xtal}$
CC6	$f_{clk} = 1/4 f_{xtal}$
CC7	$f_{clk} = 1/2 f_{INT}$
REG0 = 1, REG1 = 0, R/W = 0; UART CONFIGURATION (after reset all bits are cleared)	
UC0	ISO UART RESET
UC1	START SESSION
UC2	LCT (Last Character to Transmit)
UC3	TRANSMIT/RECEIVE
UC4 to UC7	not used
REG0 = 0, REG1 = 1, R/W = 0; UART TRANSMIT	
UT0 to UT7	LSB to MSB of the character to be transmitted to the card
REG0 = 1, REG1 = 1, R/W = 0; PORTS EXTENSION (after reset all bits are cleared)	
PE0 to PE5	PE0 to PE5 is the inverse of the value to be written on K0 to K5
PE6, PE7	not used
REG0 = 0, REG1 = 0, R/W = 1; UART RECEIVE	
UR0 to UR7	LSB to MSB of the character received from the card
REG0 = 1, REG1 = 0, R/W = 1; UART STATUS REGISTER (after reset all bits are cleared)	
US0	UART TRANSMIT buffer empty
US1	UART RECEIVE buffer full
US2	first start bit detected
US3	parity error detected during reception of a character (the UART has asked the card to repeat the character)
US4	parity error detected during transmission of a character. The controller must write the previous character in UART TRANSMIT, or abort the session.
US5 to US7	not used

USE OF PERIPHERAL INTERFACE

Write operation:

Select the correct register with R/W, REG0, REG1.

Write the word in the peripheral shift register (PSR) with DATA and STROBE. DATA is shifted on the rising edge of STROBE. 8 shifts are necessary.

Give a negative pulse on ENABLE. The data is parallel loaded in the register on the falling edge of ENABLE.

Read operation:

Select the correct register with R/W, REG0 and REG1.

Give a first negative pulse on ENABLE. The word is parallel loaded in the peripheral shift register on the rising edge of ENABLE.

Give a second negative pulse on ENABLE for configuring the PSR in shift right mode.

Read the word from PSR with DATA and STROBE. DATA is shifted on the rising edge of STROBE. 7 shifts are necessary.

Table 3 Example of peripheral interface

CHANGE OF CLOCK CONFIGURATION(1)		READ CHARACTER ARRIVED IN UART RECEIVE(2)	
	CLR REG0		CLR REG0
	CLR REG1		CLR REG1
	CLR R/W		SET R/W
	MOV R2, #8		CLR ENABLE
LOOP	RRC A		SET ENABLE
	MOV DATA C		CLR ENABLE
	CLR STROBE		SET ENABLE
	SET STROBE		MOV R2, #8
	DJNZ R2, LOOP	LOOP	MOV C, DATA
	CLR ENABLE		RRC A
	SET ENABLE		CLR STROBE
	SET DATA		SET STROBE
	RET		DJNZ R2, LOOP
			SET DATA
			RET

Notes

1. The new configuration is supposed to be in the accumulator.
2. The character will be in the accumulator.

ISO UART

The ISO UART handles all the specific requirements defined in ISO T = 0 protocol type. It is clocked with the cards clock, which gives the $f_{clk}/31$ sampling rate for start bit detection (the start bit is detected at the first LOW level on I/O) and the $f_{clk}/372$ frequency for ETU timing (in the reception mode the bit is sampled at ½ETU). It also allows the cards clock frequency changes without interfering with the baud rate.

This hardware UART allows operating of the microcontroller at low frequency, thus lowering EM radiations and power consumption. It also frees the microcontroller of fastidious conversions and real time jobs thereby allowing the control of higher level tasks.

The following occurs in the reception mode (see Fig.6):

- Detection of the inverse or direct convention at the begin of ATR.
- Automatic convention setting, so the microcontroller only receives characters in direct convention.
- Parity checking and automatic request for character repetition in case of error (reception is possible at 12 ETU).

In the transmission mode (see Fig.7):

- Transmission according to the convention detected during ATR, consequently the microcontroller only has to send characters in direct convention. Transmission of the next character may start at 12 ETU in the event of no error or 13 ETU in case of error.
- Parity calculation and detection of repetition request from the card in the event of error.
- The bit LCT (Last Character to Transmit) allows fast reconfiguration for receiving the answer 12 ETU after the start bit of the last transmitted character.

The ISO UART status register can inform which event has caused an interrupt. (Buffer full, buffer empty, parity error detected etc.) cf Peripheral Interface.

This register is reset when the microcontroller reads the status out of it.

The ISO UART configuration register enables the microcontroller to configure the ISO UART. cf Peripheral Interface.

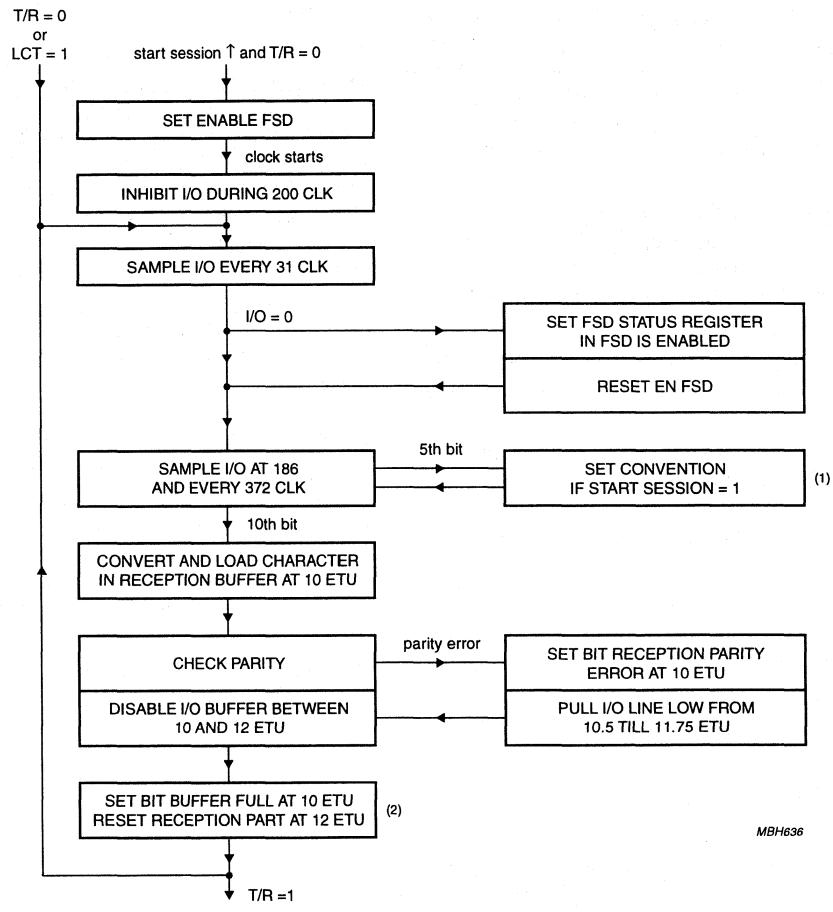
After power-on, all ISO UART registers are reset.

The ISO UART is configured in the reception mode. When the microcontroller wants to start a session, it sets the bits START SESSION and RESET ISO UART in UART CONFIGURATION and then sets START LOW. When the first start bit on I/O is detected (sampling rate $f_{clk}/31$), the UART sets the bit US2 (First Start Detect) in the status register which gives an interrupt on INT0 one CLK pulse later.

The convention is recognized on the first character of the ATR and the UART configures itself in order to exchange direct data without parity processing with the microcontroller whatever the convention of the card is. The bit START SESSION must be reset by software. At the end of every character, the UART tests the parity and resets what is necessary for receiving another character.

If no parity error is detected, the UART sets the bit US1 (BUFFER FULL) in the STATUS REGISTER which warns the microcontroller it has to read the character before the reception of the next one has been completed. The STATUS REGISTER is reset when read from the controller.

If a parity error has been detected, the UART pulls the I/O line LOW between 10.5 and 12 ETU. It also sets the bits BUFFER FULL and US3 (parity error during reception) in the STATUS REGISTER which warns the microcontroller that an error has occurred. The card is supposed to repeat the previous character.



(1) The start session is reset by software.

(2) The software may load the received character in the peripheral control at any time without any action on the ISO UART.

Fig.6 ISO UART reception flow chart.

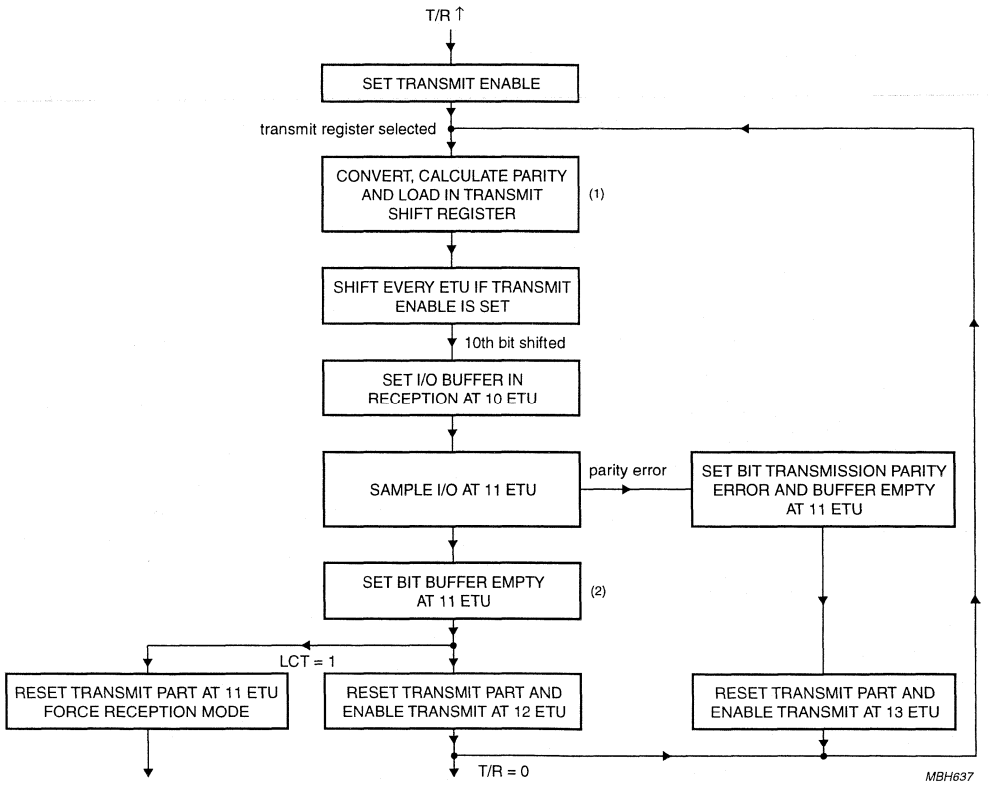
When the controller needs to transmit data to the card, it first sets the bit UC3 in the UART CONFIGURATION which configures the UART in the transmission mode. As soon as a character has been written in the UART TRANSMIT register, the UART makes the conversion, calculates the parity and starts the transmission on the rising edge of ENABLE. When the character has been transmitted, it surveys the I/O line at 11 ETU in order to know if an error has been detected by the card.

If no error has occurred, the UART sets the bit US0 (BUFFER EMPTY) in the STATUS REGISTER and waits for the next character. If the next character has been written before 12 ETU, the transmission will start at 12 ETU. If it was written after 12 ETU it will start on the rising edge of ENABLE.

If an error has occurred, it sets the bits BUFFER EMPTY and US4 (parity error during transmission) which warns the microcontroller to rewrite the previous character in the UART TRANSMIT register. If the character has been rewritten before 13 ETU, the transmission will start at 13 ETU. If it has been written after 13 ETU it will start on the rising edge of ENABLE.

When the transmission is completed, the microcontroller may set the bit LCT (Last Character to Transmit) so that the UART will force the reception mode into ready to get the reply from the card at 12 ETU. This bit must be reset before the end of the first reception. The bit T/R must be reset to enable the reception of the following characters.

When the session is completed, the microcontroller re-initializes the whole UART by resetting the bit RESET ISO UART.



(1) The transmit register may be loaded just after reading from the status register.
(2) The software must reset the last character but before completion of the first received character.

Fig.7 ISO UART transmission flow chart.

I/O buffer modes (see Fig.8)

The following are the I/O buffer modes:

1. I/O buffer disabled by ENIO.
2. I/O buffer in input, 20 kΩ pull-up resister connected between I/O and V_{CC}, I/O masked till 200 clock pulses.
3. I/O buffer in input, 20 kΩ pull-up resister connected between I/O and V_{CC}, I/O is sampled every 31 clock pulses.
4. I/O buffer in output, 20 kΩ pull-up resister connected between I/O and V_{CC}.
5. I/O buffer in output, I/O is pulled LOW by the N transistor of the buffer.
6. I/O buffer in output, I/O is strongly HIGH or LOW by the P or N transistor.

Output ports extension

In the LQFP64 version, 6 auxiliary output ports may be used for low frequency tasks (for example, keyboard scanning). These ports are push-pull output types (cf use in software document).

Activation sequence

When the card is inactive, V_{CC}, CLK, RST and I/O are LOW, with low impedance with respect to GND. The step-up converter is stopped. The I/O is configured in the reception mode with a high impedance path to the ISO UART, subsequently no spurious pulse from the card during power-up will be taken into account until I/O is enabled. When everything is satisfactory (voltage supply, card present, no hardware problems), the microcontroller may initiate an activation sequence by setting START LOW (t_0):

- The step-up converter is started (t_1)
- LIS signal is disabled by ENLI, and V_{CC} starts rising from 0 to 5 V with a controlled rise time of 0.1 V/µs typically (t_2)
- I/O buffer is enabled (t_3)
- Clock is sent to the card (t_4)
- RST buffer is enabled (t_5).

In order to allow a precise count of clock pulses during ATR, a defined time window (t_3; t_5) is opened where the clock may be sent to the card by means of RSTIN. Beyond this window, RSTIN has no more action on clock, and only monitors the cards RST contact (RST is the inverse of RSTIN).

The sequencer is clocked by $f_{INT}/64$ which leads to a time interval T of 25 µs typical. Thus $t_1 = 0$ to $\frac{1}{64}T$, $t_2 = t_1 + \frac{1}{2}3T$, $t_3 = t_1 + 4T$, $t_4 = t_3$ to t_5 and $t_5 = t_1 + 7T$ (see Fig.9).

Deactivation sequence (see Fig.10)

When the session is completed, the microcontroller sets START HIGH. The circuit then executes an automatic deactivation sequence:

- Card reset (RST falls LOW) at t_{10}
- Clock is stopped at t_{11}
- I/O becomes high impedance to the ISO UART (t_{12})
- V_{CC} falls to 0 V with typical 0.1 V/µs slew rate (t_{13})
- The step-up converter is stopped and CLK, RST, V_{CC} and I/O become low impedance to GND (t_{14}).
- $t_{10} < \frac{1}{64}T$; $t_{11} = t_{10} + \frac{1}{2}T$; $t_{12} = t_{10} + T$; $t_{13} = t_{10} + \frac{1}{2}3T$; $t_{14} = t_{10} + 5T$.

Protections

Main hardware fault conditions are monitored by the circuit

- Overcurrent on V_{CC}
- Short circuits between V_{CC} and other contacts
- Card take-off during transaction.

When one of these problems is detected, the security logic block pulls the interrupt line OFF LOW, in order to warn the microcontroller, and initiates an automatic deactivation of the contacts. When the deactivation has been completed, the OFF line returns HIGH, except if the problem was due to a card extraction in which case it remains LOW till a card is inserted.

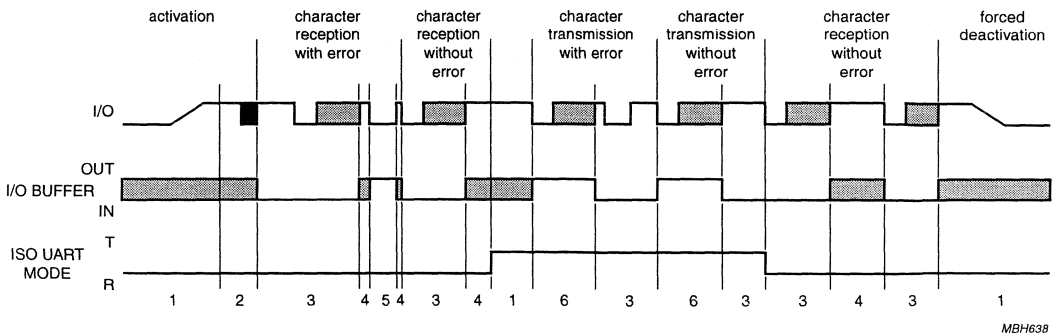


Fig.8 I/O buffer modes.

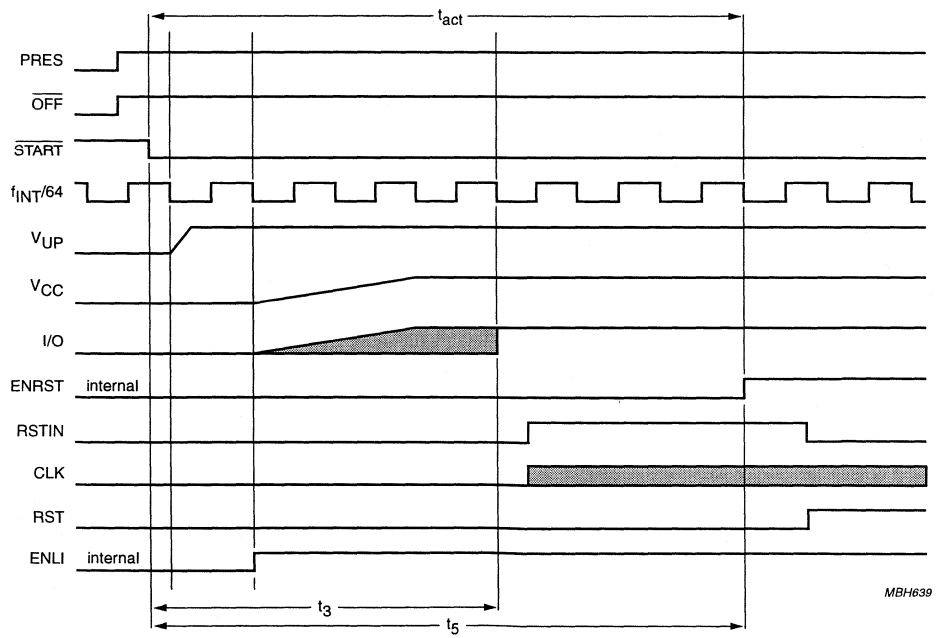


Fig.9 Activation sequence.

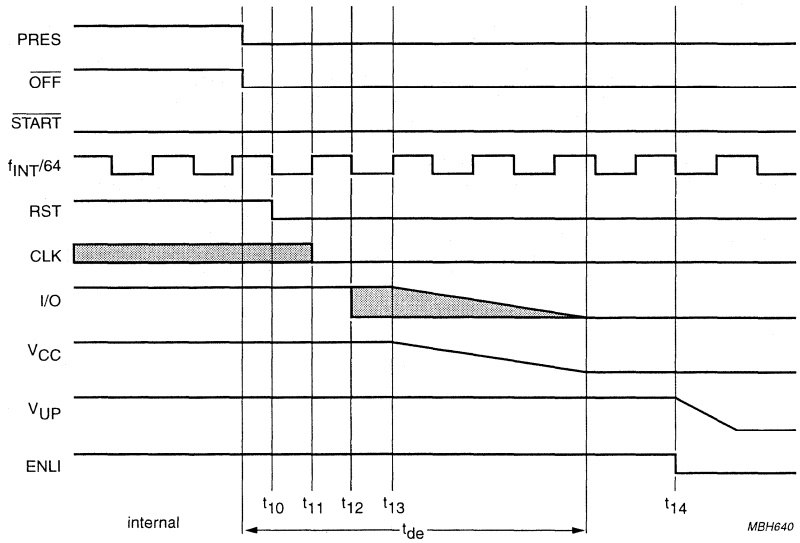


Fig.10 Emergency deactivation sequence after a card take-off.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage		–0	6.5	V
V_{DDD}	digital supply voltage		–0	6.5	V
V_n	all input voltages		–0	V_{DD} + 0.5	V
I_{n1}	DC current into XTAL1, XTAL2, RX, TX, RESET, INT1, P34, P37, P00 to P03, P11 to P17, P20 to P23 and TEST1 to TEST4		–	5	mA
I_{n2}	DC current from or to AUX1, AUX2		–10	+10	mA
I_{n3}	DC current from or to S1 to S5		–30	+30	mA
I_{n4}	DC current into DELAY		–5	+10	mA
I_{n5}	DC current from or to PRES		–5	+5	mA
I_{n6}	DC current from and to K0 to K5		–5	+5	mA
I_{n7}	DC current from or into ALARM (according to option choice)		–5	+5	mA
P_{tot}	continuous total power dissipation	T_{amb} = –20 to +85°C	–	500	mW
T_{stg}	IC storage temperature		–55	+150	°C
V_{es}	electrostatic discharge	on pins I/O, V_{CC}, RST, CLK and PRES	–6	+6	kV
		on other pins	–2	+2	kV
T_j	Operating Junction Temp.	–	–	125	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient in free air		
	LQFP64	70	K/W
	QFP44	60	K/W

CHARACTERISTICS

V_{DD} = 5 V; V_{SS} = 0 V; T_{amb} = 25 °C; for general purpose I/O ports see 80CL51 data sheet; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage	Option dependant	2.5	–	6.0	V
$I_{DD(pd)}$	supply current power-down mode	V_{DD} = 5 V; card inactive V_{DD} = 3V; " "	–	90	–	µA
$I_{DD(sm)}$	supply current sleep mode	card powered, but with clock stopped	–	500	–	µA
$I_{DD(om)}$	supply current operating mode	unloaded; f_{xtal} = 13 MHz; f_{clk} = 6.5 MHz; f_{card} = 3.25 MHz	–	5.5	–	mA
		V_{DD} = 3 V; f_{xtal} = 13 MHz; f_{clk} = 3.25 MHz; f_{card} = 3.25 MHz	–	3	–	mA
V_{th1}	threshold voltage on V_{DD} (falling)	supervisor option	2	–	2.3	V
			2.45	–	3	V
			3.8	–	4.5	V
V_{hys1}	hysteresis on V_{th1}		40	–	350	mV
V_{th2}	threshold voltage on DELAY		–	1.38	–	V
V_{DEL}	voltage on pin DELAY		4.6	–	V_{DD}	V
I_{DEL}	output current at DELAY	pin grounded (charge)	–1.5	–1	–0.4	µA
		V_{DEL} = V_{DD} (discharge)	4	6.8	10	mA
t_W	ALARM pulse width	C_{DEL} = 10 nF	–	10	–	ms
ALARM (open drain active HIGH or LOW output)						
I_{OH}	HIGH level output current	active LOW option; V_{OH} = 5 V	–	–	10	µA
V_{OL}	LOW level output voltage	active LOW option; I_{OL} = 2 mA	–	–	0.4	V
I_{OL}	LOW level output current	active HIGH option, V_{OL} = 0 V	–	–	–10	µA
V_{OH}	HIGH level output voltage	active HIGH option, I_{OH} = –2 mA	V_{DD} – 1	–	–	V
Crystal oscillator (note 1)						
f_{xtal}	crystal frequency		2	–	16	MHz
f_{EXT}	external frequency applied on XTAL1		0	–	16	MHz
Step-up converter						
f_{INT}	oscillation frequency		2	–	3	MHz
V_{UP}	voltage on S5		–	6.5	–	V
Low impedance supply (LIS)						
V_{LIS}	voltage on LIS		0	–	V_{DD}	V
I_{LIS}	current at LIS		–	–	7	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reset output to the card (RST)						
$V_{inactive}$	output voltage	when inactive	−0.3	–	0.4	V
		when LIS is used; $I_{inactive}$ = 1 mA	−0.3	–	0.4	V
$I_{inactive}$	current from RST when inactive and pin grounded		–	–	−1	mA
V_{OL}	LOW level output voltage	I_{OL} = 200 µA	−0.25	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} <−200 µA	4	–	V_{CC} + 0.3	V
t_r	rise time	C_L = 30 pF	–	–	1	µs
t_f	fall time	C_L = 30 pF	–	–	1	µs
Clock output to the card (CLK)						
$V_{inactive}$	output voltage	when inactive	−0.3	–	0.4	V
		when LIS is used; $I_{inactive}$ = 1 mA	−0.3	–	0.4	V
$I_{inactive}$	current from CLK when inactive and pin grounded		–	–	−1	mA
V_{OL}	LOW level output voltage	I_{OL} = 200 µA	−0.25	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} <−200 µA	V_{CC}−0.5	–	V_{CC}+0.25	V
t_r	rise time	C_L = 30 pF	–	–	15	ns
t_f	fall time	C_L = 30 pF	–	–	15	ns
f_{clk}	clock frequency	1 MHz Idle configuration	1	–	1.5	MHz
		low operating speed	–	–	2	MHz
		middle operating speed	–	–	4	MHz
		high operating speed	–	–	8	MHz
δ	duty cycle	C_L = 30 pF	45	–	55	%
Card supply voltage (V_{CC})						
$V_{inactive}$	output voltage	when inactive	−0.3	–	0.4	V
		when LIS is used; $I_{inactive}$ = 1 mA	−0.3	–	0.4	V
$I_{inactive}$	current from VCC when inactive and pin grounded		–	–	−1	mA
V_{cc}	output voltage in active mode with 100 nF capacitor; static load (up to 20 mA) dynamic current of 40 nA	I_{max} = 200 mA, f_{max} = 5 MHz, and duration <400 ns	– 4.75 4.5	–	– 5.25 5.5	V
I_{CC}	output current	V_{CC} = 5V	–	–	−20	mA
		V_{CC} shorted to GND	–	–	−40	mA
SR	slew rate	up or down (max capacitance is 150 nF)	0.04	0.1	0.16	V/µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data line (I/O)						
$V_{inactive}$	output voltage	when inactive	−0.3	–	0.4	V
		when LIS is used; $I_{inactive}$ = 1 mA	−0.3	–	0.4	V
$I_{inactive}$	current from I/O when inactive and pin grounded		–	–	−1	mA
V_{OL}	LOW level output voltage (I/O configured as an output)	I_{OL} = 1 mA	−0.25	–	0.3	V
V_{OH}	HIGH level output voltage (I/O configured as an output)	I_{OH} <−100 μA	V_{CC}+0.8	–	V_{CC}+0.25	V
V_{IL}	input voltage LOW (I/O configured as an input)	I_{IL} = 1 mA	0	–	0.5	V
V_{IH}	input voltage HIGH (I/O configured as an input)	I_{IL} = 100 μA	V_{CC}+0.6	–	V_{CC}	V
t_r	rise time	C_L = 30 pF	–	–	1	μs
t_f	fall time	C_L = 30 pF	–	–	1	μs
R_{pu}	pull-up resistor connected to V_{CC} when I/O is input	see Table 4 for options	–	–	–	
Protections						
$I_{CC(sd)}$	shutdown current at V_{CC}		–	−30	–	mA
Timing						
t_{act}	activation sequence duration		–	–	225	μs
t_{de}	deactivation sequence duration		–	–	150	μs
$t_{3(start)}$	start of the window for sending clock to the card		–	–	130	μs
$t_{5(end)}$	end of the window for sending clock to the card		140	–	–	μs
Auxiliary outputs (AUX1, AUX2)						
V_{OL}	LOW level output voltage	I_{OL} = 5 mA	–	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = −5 mA	V_{DD} − 1	–	–	V
Output ports from extension (K0 to Kn)						
V_{OL}	LOW level output voltage	I_{OL} = 2 mA	–	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = −2 mA	V_{DD} − 1	–	–	V
Card presence input (PRES)						
V_{IL}	LOW level input voltage	I_{IL} = −1 mA	–	–	0.6	V
V_{IH}	HIGH level input voltage	I_{IH} = 100 μA	0.7V_{DD}	–	–	V
I_{IH}	HIGH level input current	V_{IH}=+5V	0.2	–	3	μA

Note

1. The crystal oscillator is the same as OPTION 3 of the 80CL51.

APPLICATION INFORMATION

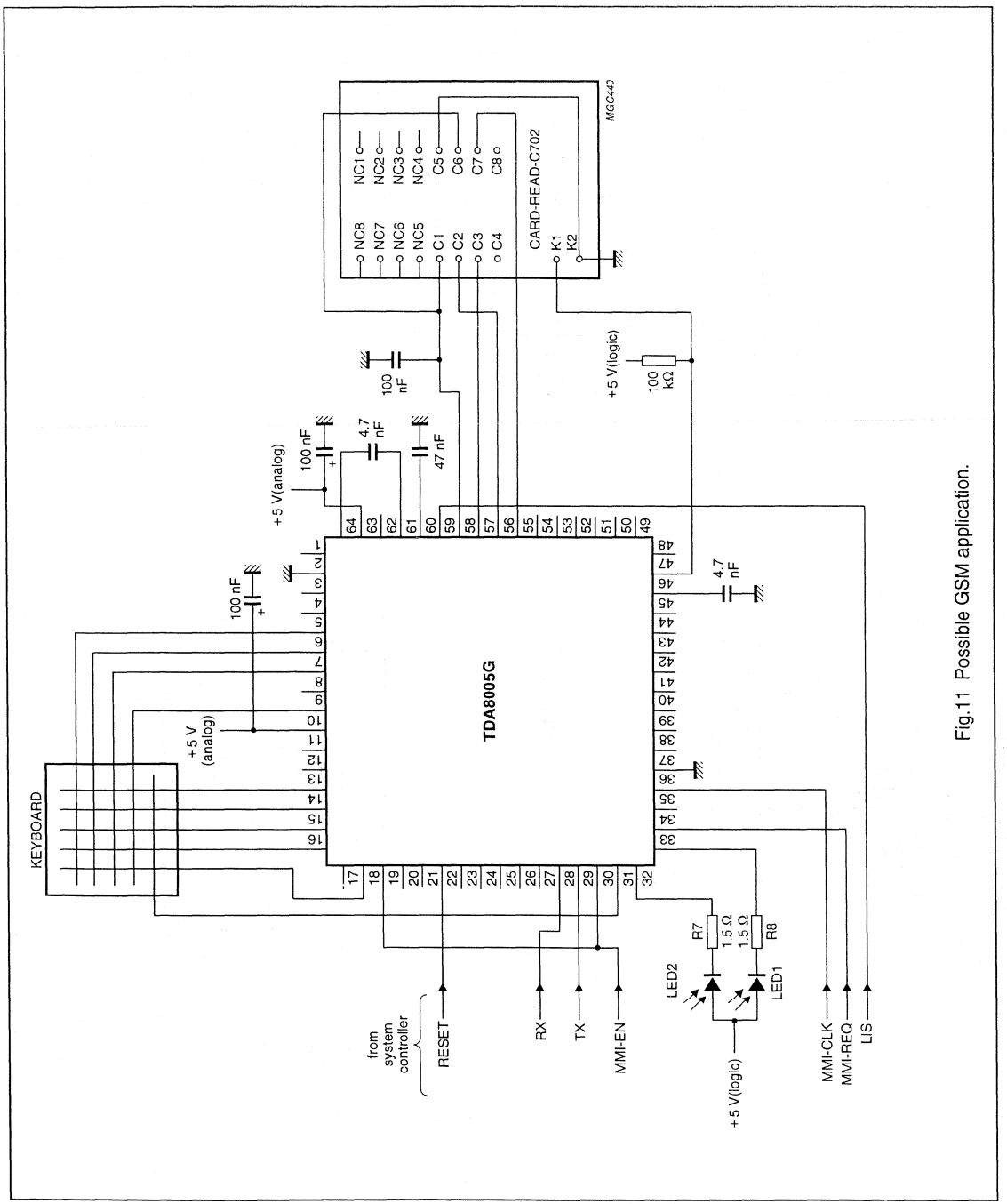


Fig.11 Possible GSM application.

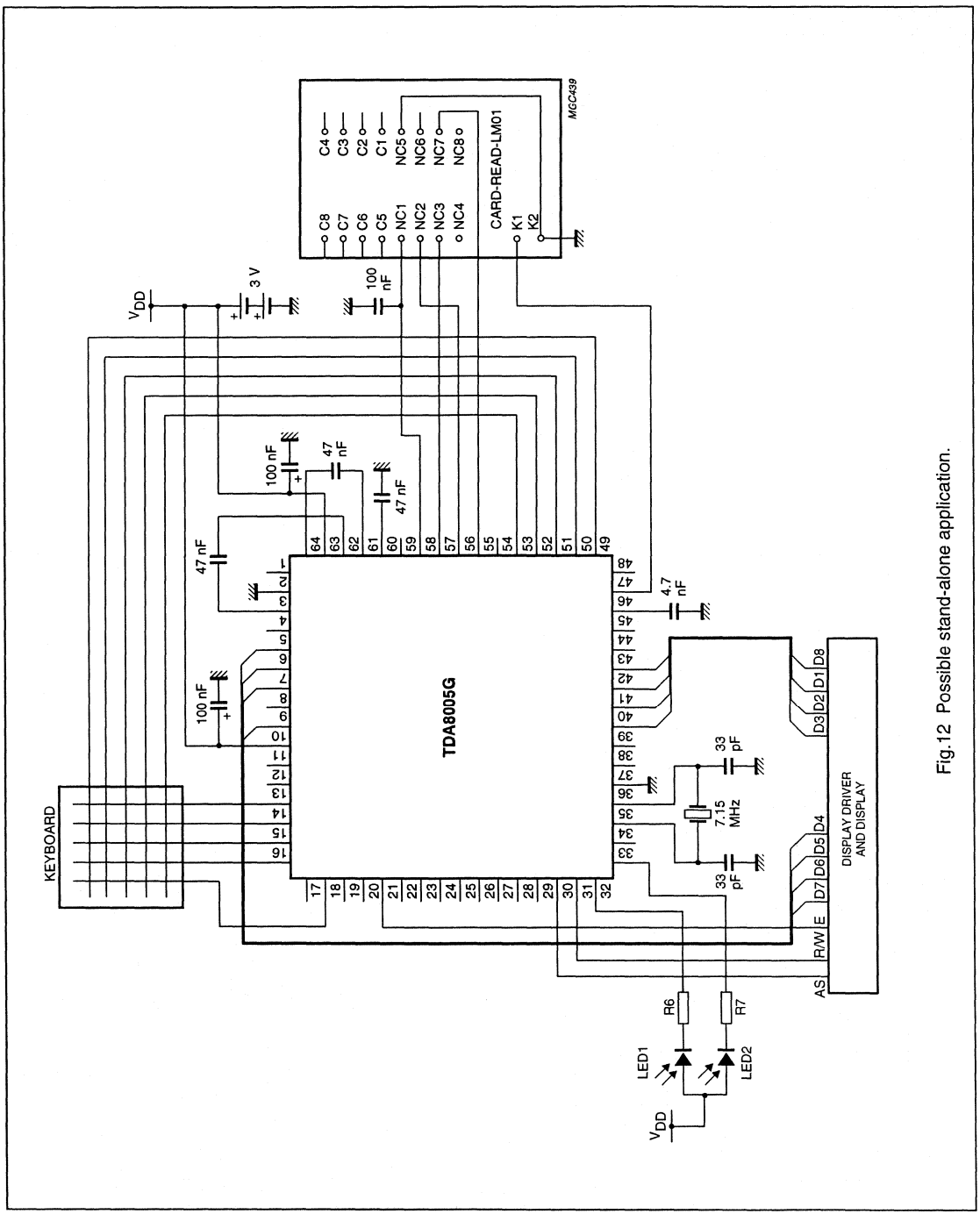


Fig.12 Possible stand-alone application.

Table 4 TDA8005 option choice form

FUNCTION	DESCRIPTION	OPTION
Ports		
P00		
P01		
P02		
P03		
P04	RSTIN (fixed)	3 S
P05	START (fixed)	3 S
P06	STR (fixed)	3 S
P07	EN (fixed)	3 S
P10	OFF (fixed)	2 S
P11		
P12		
P13		
P14		
P15		
P16		
P17		
P20		
P21		
P22		
P23		
P24	DATA (fixed)	1 S
P25	R/W (fixed)	3 S
P26	REG1 (fixed)	3 S
P27	REG0 (fixed)	3 S
P30		
P31		
P32	INT (fixed)	1 S
P33		
P34		
P35	AUXI (fixed)	3 S
P36	AUX2 (fixed)	3 S
P37		

FUNCTION	DESCRIPTION	OPTION
Analog options		
Step-up	doubler (updo) or tripler (uptri)	
Supervisor	2.3 (supervb, 3 (supervtr) or 4.5 (superVCI)	
I/O	low impedance (UARTI) or high impedance (UARTZ)	
I/O pull-up	10, 20 or 30 kΩ	
R_CLK	0, 50, 100, 150 or 200 Ω	
R_RST	0, 50, 80, 130 or 180 Ω	
ALARM	active HIGH (alarmbufp) or active LOW (alarmbufn)	
PRES	active HIGH (prestopp) or active LOW (prestopn)	

1 W BTL audio amplifier TDA8541

FEATURES

- Flexibility in use
- Few external components
- Low saturation voltage of output stage
- Gain can be fixed with external resistors
- Standby mode controlled by CMOS compatible levels
- Low standby current
- No switch-on/switch-off plops
- High supply voltage ripple rejection
- Protected against electrostatic discharge
- Outputs short-circuit safe to ground, V_{CC} and across the load
- Thermally protected.

GENERAL DESCRIPTION

The TDA8541(T) is a one channel audio power amplifier for an output power of 1 W with an 8 Ω load at a 5 V supply. The circuit contains a BTL amplifier with a complementary PNP-NPN output stage and standby/mute logic. The TDA8541T comes in an 8 pin SO package and the TDA8541 in an 8 pin DIP package.

APPLICATIONS

- Portable consumer products
- Personal computers
- Telephony.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		2.2	5	18	V
I_q	quiescent current	V_{CC} = 5 V	–	8	12	mA
I_{stb}	standby current		–	–	10	μA
P_o	output power	THD = 10%; R_L = 8 Ω; V_{CC} = 5 V	1	–	–	W
THD	total harmonic distortion	P_o = 0.5 W	–	0.15	–	%
SVRR	supply voltage ripple rejection		50	–	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8541T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
TDA8541	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1

BLOCK DIAGRAM

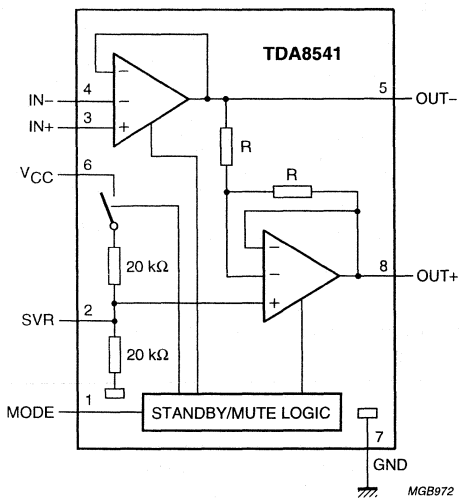


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
MODE	1	operating mode select (standby, mute, operating)
SVR	2	half supply voltage, decoupling ripple rejection
IN+	3	positive input
IN–	4	negative input
OUT–	5	negative loudspeaker terminal
V_{CC}	6	supply voltage
GND	7	ground
OUT+	8	positive loudspeaker terminal

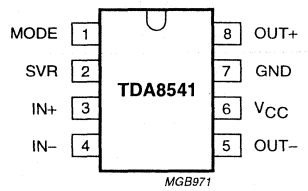


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA8541(T) is a 1 W BTL audio power amplifier capable of delivering 1 W output power to an 8 Ω load at THD = 10% using a 5 V power supply. Using the MODE pin the device can be switched to standby and mute condition. The device is protected by an internal thermal shutdown protection mechanism. The gain can be set within a range from 6 dB to 30 dB by external feedback resistors.

Power amplifier

The power amplifier is a Bridge Tied Load (BTL) amplifier with a complementary PNP-NPN output stage.
The voltage loss on the positive supply line is the saturation voltage of a PNP power transistor, on the negative side the saturation voltage of an NPN power transistor. The total voltage loss is <1 V and with a 5 V supply voltage and an 8 Ω loudspeaker an output power of 1 W can be delivered.

Mode select pin

The device is in standby mode (with a very low current consumption) if the voltage at the MODE pin is >(V_{CC} – 0.5 V), or if this pin is floating. At a MODE voltage level of less than 0.5 V the amplifier is fully operational. In the range between 1.5 V and V_{CC} – 1.5 V the amplifier is in mute condition. The mute condition is useful to suppress plop noise at the output, caused by charging of the input capacitor.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage	operating	−0.3	+18	V
V_I	input voltage		−0.3	V_{CC} + 0.3	V
I_{ORM}	repetitive peak output current		–	1	A
T_{stg}	storage temperature	non-operating	−55	+150	°C
T_{amb}	operating ambient temperature		−40	+85	°C
V_{psc}	AC and DC short-circuit safe voltage		–	10	V
P_{tot}	total power dissipation	SO8	–	0.8	W
		DIP8	–	1.2	W

QUALITY SPECIFICATION

In accordance with *"SNW-FQ-611-E"*. The number of the quality specification can be found in the *"Quality Reference Handbook"*. The handbook can be ordered using the code 9397 750 00192.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	in free air		
	TDA8541T (SO8)		160	K/W
	TDA8541 (DIP8)		100	K/W

DC CHARACTERISTICS

V_{CC} = 5 V; T_{amb} = 25 °C; R_L = 8 Ω; V_{MODE} = 0 V; measured in test circuit Fig.3; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	operating	2.2	5	18	V
I_q	quiescent current	$R_L = \infty$; note 1	–	8	12	mA
I_{stb}	standby current	$V_{MODE} = V_{CC}$	–	–	10	μA
V_O	DC output voltage	note 2	–	2.2	–	V
$\lvert V_{OUT+} - V_{OUT-} \rvert$	differential output voltage offset		–	–	50	mV
I_{IN+}, I_{IN-}	input bias current		–	–	500	nA
V_{MODE}	input voltage mode select	operating	0	–	0.5	V
		mute	1.5	–	V_{CC} − 1.5	V
		standby	V_{CC} − 0.5	–	V_{CC}	V
I_{MODE}	input current mode select	$0 < V_{MODE} < V_{CC}$	–	–	20	μA

Notes

1. With a load connected at the outputs the quiescent current will increase, the maximum of this increase being equal to the DC output offset voltage divided by R_L.
2. The DC output voltage with respect to ground is approximately $0.5 \times V_{CC}$.

AC CHARACTERISTICS

V_{CC} = 5 V; T_{amb} = 25 °C; R_L = 8 Ω; f = 1 kHz; V_{MODE} = 0 V; measured in test circuit Fig.3; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_o	output power	THD = 10%	1	1.2	–	W
		THD = 0.5%	0.6	0.9	–	W
THD	total harmonic distortion	P_o = 0.5 W	–	0.15	0.3	%
G_v	closed loop voltage gain	note 1	6	–	30	dB
Z_i	differential input impedance		–	100	–	kΩ
V_{no}	noise output voltage	note 2	–	–	100	μV
SVRR	supply voltage ripple rejection	note 3	50	–	–	dB
		note 4	40	–	–	dB
V_o	output voltage in mute condition	note 5	–	–	200	μV

Notes

1. Gain of the amplifier is 2 × R2/R1 in test circuit of Fig.3.
2. The noise output voltage is measured at the output in a frequency range from 20 Hz to 20 kHz (unweighted), with a source impedance of R_S = 0 Ω at the input.
3. Supply voltage ripple rejection is measured at the output, with a source impedance of R_S = 0 Ω at the input. The ripple voltage is a sine wave with a frequency of 1 kHz and an amplitude of 100 mV (RMS), which is applied to the positive supply rail.
4. Supply voltage ripple rejection is measured at the output, with a source impedance of R_S = 0 Ω at the input. The ripple voltage is a sine wave with a frequency between 100 Hz and 20 kHz and an amplitude of 100 mV (RMS), which is applied to the positive supply rail.
5. Output voltage in mute position is measured with an input voltage of 1 V (RMS) in a bandwidth of 20 kHz, so including noise.

TEST AND APPLICATION INFORMATION

Test conditions

Because the application can be either Bridge-Tied Load (BTL) or Single-Ended (SE), the curves of each application are shown separately.

The thermal resistance = 100 K/W for the DIP8 envelope; the maximum sine wave power dissipation for T_{amb} = 25 °C is:

$$\frac{150 - 25}{100} = 1.25 \text{ W}.$$

For T_{amb} = 60 °C the maximum total power dissipation is:

$$\frac{150 - 60}{100} = 0.9 \text{ W}.$$

BTL application

T_{amb} = 25 °C if not specially mentioned, V_{CC} = 5 V, f = 1 kHz, R_L = 8 Ω, G_v = 20 dB, audio band-pass 22 Hz to 22 kHz.

The BTL application diagram is shown in Fig.3.

The quiescent current has been measured without any load impedance. The total harmonic distortion as a function of frequency was measured with a low-pass filter of 80 kHz. The value of capacitor C2 influences the behaviour of the SVRR at low frequencies, increasing the value of C2 increases the performance of the SVRR. The figure of the mode select voltage (V_{ms}) as a function of the supply voltage shows three areas; operating, mute and standby. It shows, that the DC-switching levels of the mute and standby respectively depends on the supply voltage level.

SE application

T_{amb} = 25 °C if not specially mentioned, V_{CC} = 7.5 V, f = 1 kHz, R_L = 4 Ω, G_v = 20 dB, audio band-pass 22 Hz to 22 kHz.

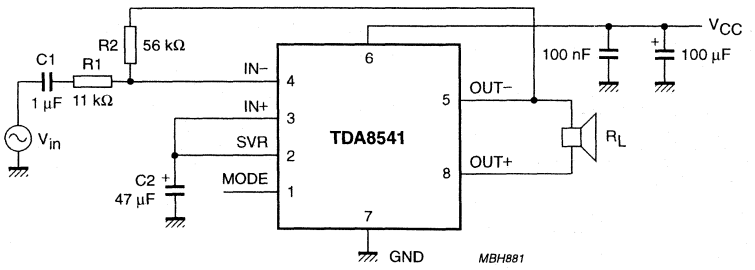
The SE application diagram is shown in Fig.13.

The capacitor value of C3 in combination with the load impedance determines the low frequency behaviour. The total harmonic distortion as a function of frequency was measured with low-pass filter of 80 kHz. The value of capacitor C2 influences the behaviour of the SVRR at low frequencies, increasing the value of C2 increases the performance of the SVRR.

General remark

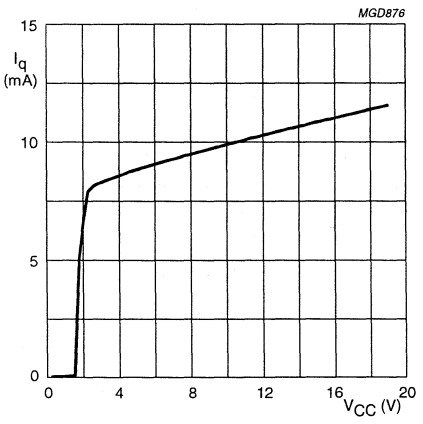
The frequency characteristic can be adapted by connecting a small capacitor across the feedback resistor. To improve the immunity of HF radiation in radio circuit applications, a small capacitor can be connected in parallel with the feedback resistor (56 kΩ); this creates a low-pass filter.

BTL APPLICATION



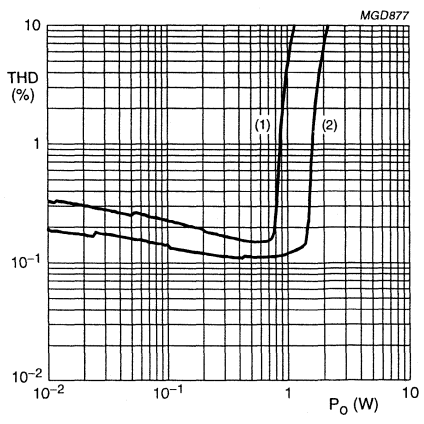
$$\text{Gain} = 2 \times \frac{R2}{R1}$$

Fig.3 BTL application.



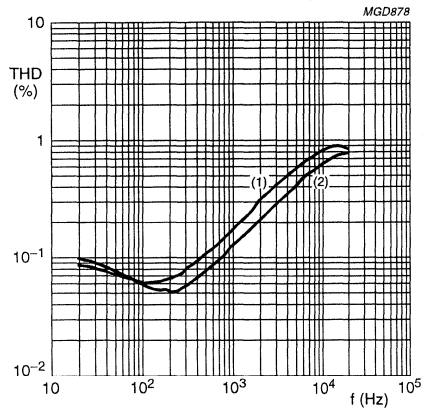
$R_L = \infty$.

Fig.4 I_q as a function of V_{CC}.



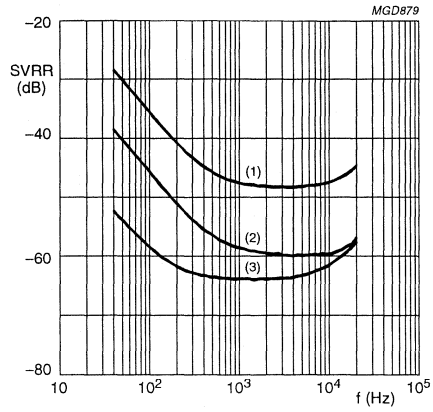
f = 1 kHz, G_v = 20 dB.
(1) V_{CC} = 5 V, R_L = 8 Ω.
(2) V_{CC} = 9 V, R_L = 16 Ω.

Fig.5 THD as a function of P_o.



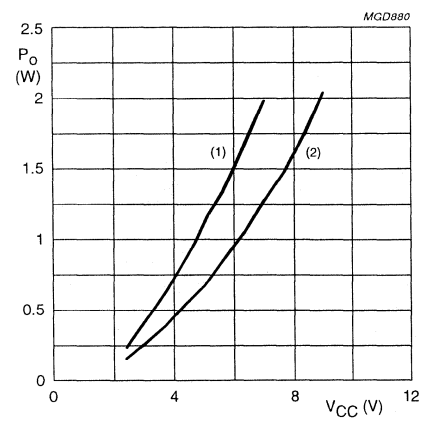
P_o = 0.5 W, G_v = 20 dB.
(1) V_{CC} = 5 V, R_L = 8 Ω.
(2) V_{CC} = 9 V, R_L = 16 Ω.

Fig.6 THD as a function of frequency.



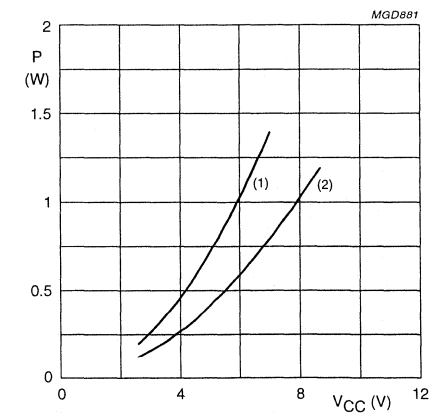
V_{CC} = 5 V, 8 Ω, R_s = 0 Ω, V_i = 100 mV.
(1) G_v = 30 dB.
(2) G_v = 20 dB.
(3) G_v = 6 dB.

Fig.7 SVRR as a function of frequency.



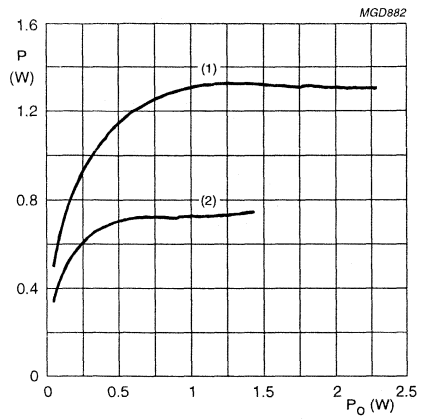
THD = 10%.
(1) R_L = 8 Ω.
(2) R_L = 16 Ω.

Fig.8 P_o as a function of V_{CC}.



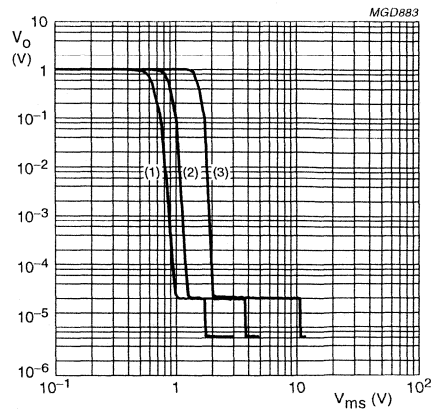
(1) R_L = 8 Ω.
(2) R_L = 16 Ω.

Fig.9 Worst case power dissipation as a function of V_{CC}.



Sine wave of 1 kHz.
(1) V_{CC} = 9 V, R_L = 16 Ω.
(2) V_{CC} = 5 V, R_L = 8 Ω.

Fig.10 P as a function of P_o.



Band-pass = 22 Hz to 22 kHz.
(1) V_{CC} = 3 V.
(2) V_{CC} = 5 V.
(3) V_{CC} = 12 V.

Fig.11 V_o as a function of V_{ms}.

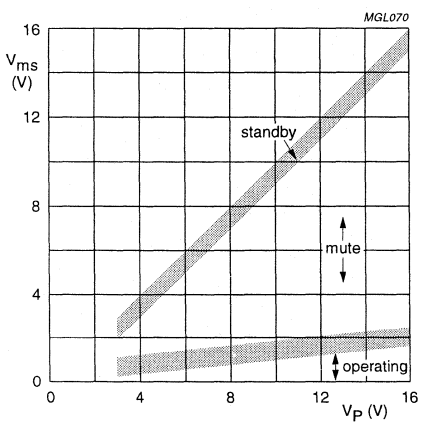
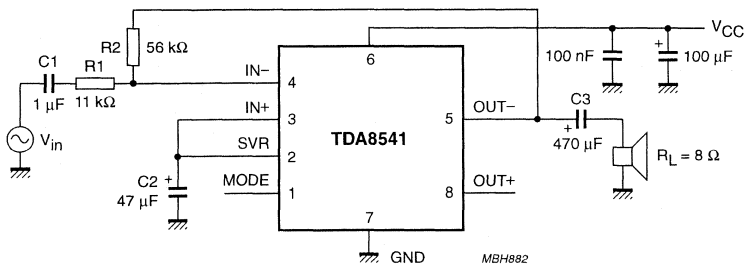


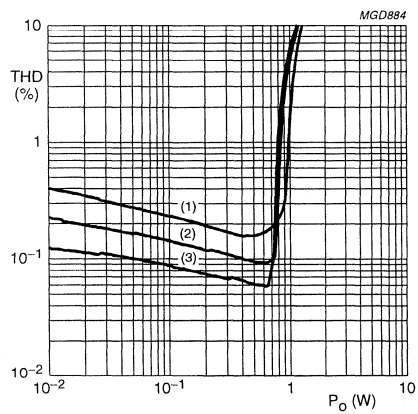
Fig.12 V_{ms} as a function of V_P.

SE APPLICATION



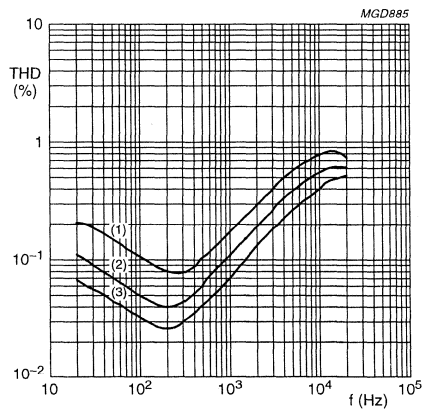
$$\text{Gain} = \frac{R2}{R1}$$

Fig.13 SE application.



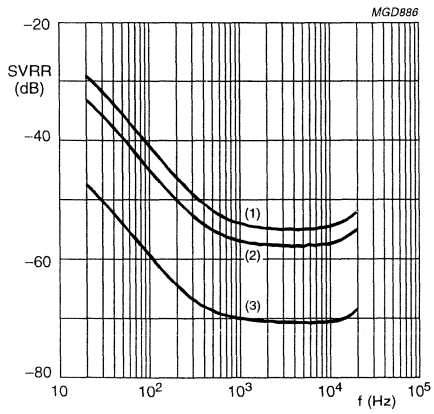
f = 1 kHz, G_v = 20 dB.
(1) V_{CC} = 7.5 V, R_L = 4 Ω.
(2) V_{CC} = 9 V, R_L = 8 Ω.
(3) V_{CC} = 12 V, R_L = 16 Ω.

Fig.14 THD as a function of P_o.



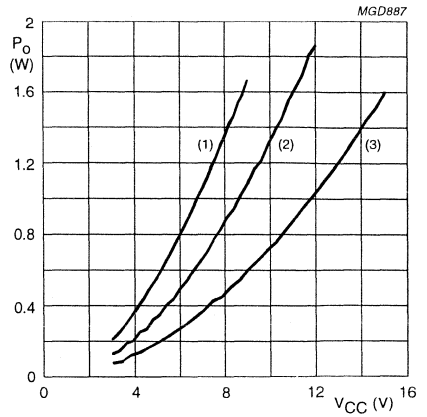
P_o = 0.5 W, G_v = 20 dB.
(1) V_{CC} = 7.5 V, R_L = 4 Ω.
(2) V_{CC} = 9 V, R_L = 8 Ω.
(3) V_{CC} = 12 V, R_L = 16 Ω.

Fig.15 THD as a function of frequency.



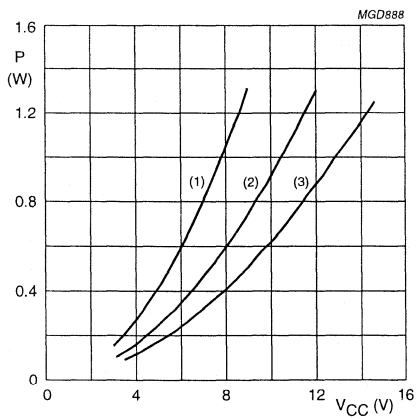
V_{CC} = 7.5 V, R_L = 4 Ω, R_s = 0 Ω, V_i = 100mV.
(1) G_v = 24 dB.
(2) G_v = 20 dB.
(3) G_v = 0 dB.

Fig.16 SVRR as a function of frequency.



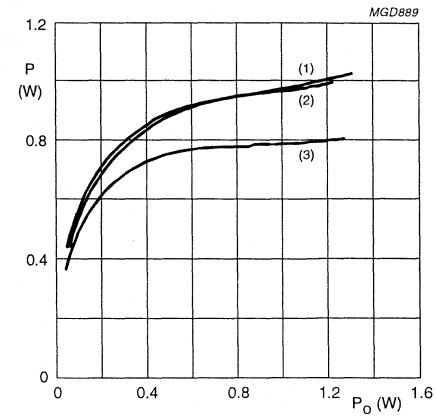
(1) THD = 10%, R_L = 4 Ω.
(2) THD = 10%, R_L = 8 Ω.
(3) THD = 10%, R_L = 16 Ω.

Fig.17 P_o as a function of V_{CC}.



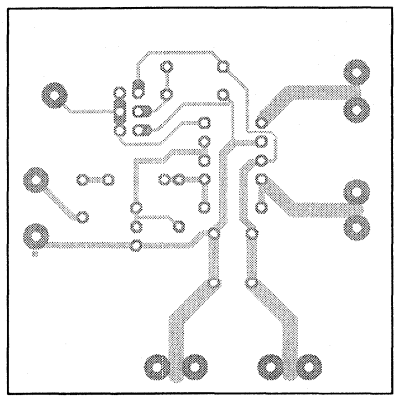
(1) R_L = 4 Ω.
(2) R_L = 8 Ω.
(3) R_L = 16 Ω.

Fig.18 Worst case power dissipation as a function of V_{CC}.

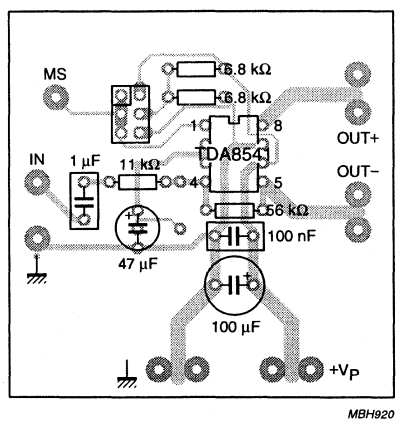


(1) V_{CC} = 7.5 V, R_L = 4 Ω.
(2) V_{CC} = 12 V, R_L = 16 Ω.
(3) V_{CC} = 9 V, R_L = 8 Ω.

Fig.19 P as a function of P_o.



a. Top view.



b. Component side.

Fig.20 Printed-circuit board layout (BTL and SE).

2 × 1 W BTL audio amplifier with output channel switching

TDA8547

FEATURES

- Selection between output channels
- Flexibility in use
- Few external components
- Low saturation voltage of output stage
- Gain can be fixed with external resistors
- Standby mode controlled by CMOS compatible levels
- Low standby current
- No switch-on/switch-off plops
- High supply voltage ripple rejection
- Protected against electrostatic discharge
- Outputs short-circuit safe to ground, V_{CC} and across the load
- Thermally protected.

APPLICATIONS

- Telecommunication equipment
- Portable consumer products
- Personal computers
- Motor-driver (servo).

GENERAL DESCRIPTION

The TDA8547(T) is a two channel audio power amplifier for an output power of 2 × 1 W with an 8 Ω load at a 5 V supply. The circuit contains two BTL amplifiers with a complementary PNP-NPN output stage and standby/mute logic. The operating condition of all channels of the device (standby, mute or on) is externally controlled by the MODE pin. With the SELECT pin one of the output channels can be switched in the standby condition. This feature can be used for loudspeaker selection and also reduces the quiescent current consumption.
The TDA8547T comes in a SO16 package and the TDA8547 in a DIP16 package.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		2.2	5	18	V
I_q	quiescent current	V_{CC} = 5 V; 2 channels	–	15	22	mA
		V_{CC} = 5 V; 1 channel	–	8	12	mA
I_{stb}	standby current		–	–	10	μA
P_o	output power	THD = 10%; R_L = 8 Ω; V_{CC} = 5 V	1	–	–	W
THD	total harmonic distortion	P_o = 0.5 W	–	0.15	–	%
SVRR	supply voltage ripple rejection		50	–	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8547T	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1
TDA8547	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1

BLOCK DIAGRAM

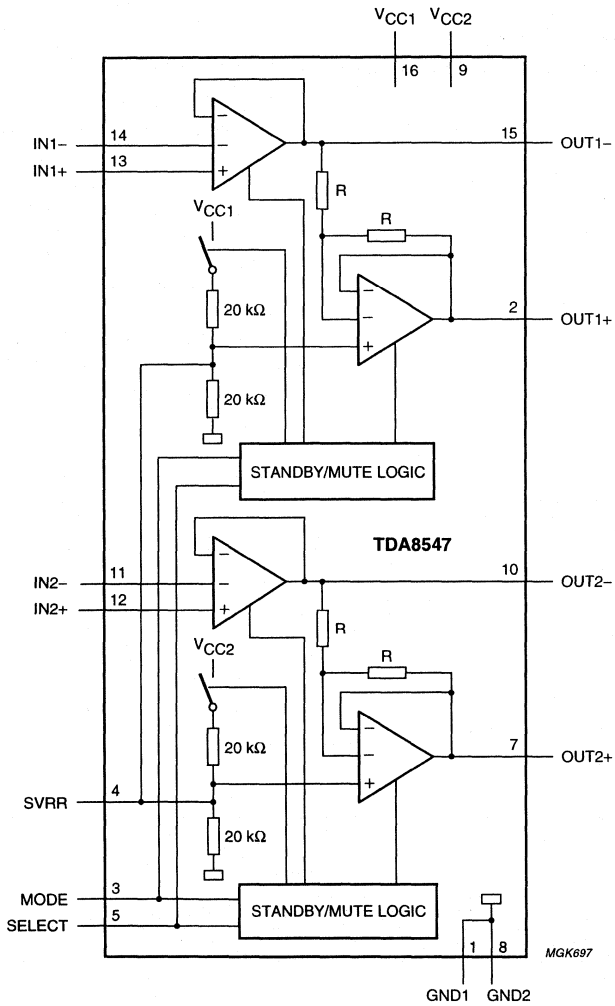


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
GND1	1	ground, channel 1
OUT1+	2	positive loudspeaker terminal, channel 1
MODE	3	operating mode select (standby, mute, operating)
SVRR	4	half supply voltage, decoupling ripple rejection
SELECT	5	input for selection of operating channel
n.c.	6	not connected
OUT2+	7	positive loudspeaker terminal, channel 2
GND2	8	ground, channel 2
V_{CC2}	9	supply voltage, channel 2
OUT2−	10	negative loudspeaker terminal, channel 2
IN2−	11	negative input, channel 2
IN2+	12	positive input, channel 2
IN1+	13	positive input, channel 1
IN1−	14	negative input, channel 1
OUT1−	15	negative loudspeaker terminal, channel 1
V_{CC1}	16	supply voltage, channel 1

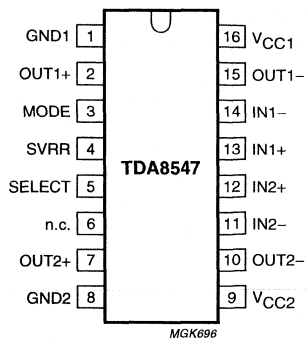


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA8547(T) is a 2 × 1 W BTL audio power amplifier capable of delivering 2 × 1 W output power to an 8 Ω load at THD = 10% using a 5 V power supply. Using the MODE pin the device can be switched to standby and mute condition. The device is protected by an internal thermal shutdown protection mechanism. The gain can be set within a range from 6 to 30 dB by external feedback resistors.

Power amplifier

The power amplifier is a Bridge-Tied Load (BTL) amplifier with a complementary PNP-NPN output stage.
The voltage loss on the positive supply line is the saturation voltage of a PNP power transistor, on the negative side the saturation voltage of a NPN power transistor. The total voltage loss is <1 V and with a 5 V supply voltage and an 8 Ω loudspeaker an output power of 1 W can be delivered.

MODE pin

The whole device (both channels) is in the standby mode (with a very low current consumption) if the voltage at the MODE pin is >(V_{CC} − 0.5 V), or if this pin is floating. At a MODE voltage level of less than 0.5 V the amplifier is fully operational. In the range between 1.5 V and V_{CC} − 1.5 V the amplifier is in mute condition. The mute condition is useful to suppress plop noise at the output caused by charging of the input capacitor.

SELECT pin

If the voltage at the SELECT pin is in the range between 1.5 V and V_{CC} − 1.5 V, or if it is kept floating, then both channels can be operational. If the SELECT pin is set to a LOW voltage or grounded, then only channel 2 can operate and the power amplifier of channel 1 will be in the standby mode. In this case only the loudspeaker at channel 2 can operate and the loudspeaker at channel 1 will be switched off. If the SELECT pin is set to a HIGH level or connected to V_{CC}, then only channel 1 can

operate and the power amplifier of channel 2 will be in the standby mode. In this case only the loudspeaker at channel 1 can operate and the loudspeaker at channel 2 will be switched off. Setting the SELECT pin to a LOW or a HIGH voltage results in a reduction of quiescent current consumption by a factor of approximately 2.

Switching with the SELECT pin during operating is not plop-free, because the input capacitor of the channel which is coming out of standby needs to be charged first.

For plop-free channel selecting the device has first to be set in mute condition with the MODE pin (between 1.5 V and V_{CC} – 1.5 V), then set the SELECT pin to the new level, after a delay set the MODE pin to a LOW level. The delay needed depends on the values of the input capacitor and the feedback resistors. Time needed is approx. 10 × C1 × (R1 + R2), so approximately 0.6 s. for the values in Fig.4.

Table 1 Control pins MODE and SELECT versus status of output channels

Voltage levels at control pins at V_P = 5 V; for other supply voltages see Figs. 14 and 15.

CONTROL PIN		STATUS OF OUTPUT CHANNEL		TYP. I_q (mA)
MODE	SELECT	CHANNEL 1	CHANNEL 2	
HIGH(1)/NC(2)	X(3)	standby	standby	0
HVP(4)	HVP(4)/NC(2)	mute	mute	15
LOW(5)	HVP(4)/NC(2)	on	on	15
HVP(4)/LOW(5)	HIGH(1)	mute/on	standby	8
HVP(4)/LOW(5)	HVP(4)/NC(2)	mute/on	mute/on	15
HVP(4)/LOW(5)	LOW(5)	standby	mute/on	8

Notes

1. HIGH = $V_{pin} > V_{CC} - 0.5$ V.
2. NC = not connected or floating.
3. X = don't care.
4. HVP = 1.5 V < $V_{pin} < V_{CC} - 1.5$ V.
5. LOW = $V_{pin} < 0.5$ V.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage	operating	−0.3	+18	V
V_I	input voltage		−0.3	V_{CC} + 0.3	V
I_{ORM}	repetitive peak output current		–	1	A
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	operating ambient temperature		−40	+85	°C
V_{Psc}	AC and DC short-circuit safe voltage		–	10	V
P_{tot}	total power dissipation	SO16	–	1.2	W
		DIP16	–	2.2	W

QUALITY SPECIFICATION

In accordance with *"SNW-FQ-611-E"*. The number of the quality specification can be found in the *"Quality Reference Handbook"*. The handbook can be ordered using the code 9397 750 00192.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air		
	TDA8547T (SO16)		100	K/W
	TDA8547 (DIP16)		55	K/W

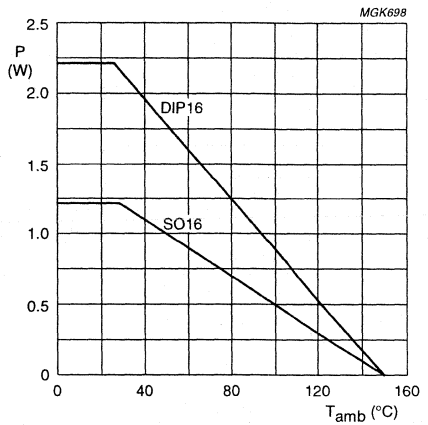


Fig.3 Power derating curve.

Table 2 Maximum ambient temperature at different conditions

V_{CC} (V)	R_L (Ω)	APPLICATION	OPERATION MODE	P_o (W)(1)	CONTINUOUS SINE WAVE DRIVEN		
					P_{max} (W)	$T_{amb(max)}$ (°C)	
						SO16	DIP16
5	8	2 channels	BTL	2 × 1.2	1.4	–	73
5	8	1 channel	BTL	1.2	0.7	80	112
7.5	8	2 channels	BTL	2 × 2.4	3.0	–	–
7.5	8	1 channel	BTL	2.4	1.5	–	68
7.5	16	2 channels	BTL	2 × 1.2	1.8	–	50
7.5	16	1 channel	BTL	1.2	0.9	60	100
7.5	28	2 channels	BTL	2 × 1	1.0	50	95
7.5	28	1 channel	BTL	1	0.5	100	122

Note

1. At THD = 10%.

DC CHARACTERISTICS

V_{CC} = 5 V; T_{amb} = 25 °C; R_L = 8 Ω; V_{MODE} = 0 V; gain = 20 dB; measured in BTL application circuit Fig.4; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	operating	2.2	5	18	V
I_q	quiescent current	BTL 2 channels; note 1	–	15	22	mA
		BTL 1 channel; note 1	–	8	12	mA
I_{stb}	standby current	$V_{MODE} = V_{CC}$	–	–	10	μA
V_O	DC output voltage	note 2	–	2.2	–	V
$\lvert V_{OUT+} - V_{OUT-} \rvert$	differential output voltage offset		–	–	50	mV
I_{IN+}, I_{IN-}	input bias current		–	–	500	nA
V_{MODE}	input voltage MODE pin	operating	0	–	0.5	V
		mute	1.5	–	V_{CC} – 1.5	V
		standby	V_{CC} – 0.5	–	V_{CC}	V
I_{MODE}	input current MODE pin	0 V < V_{MODE} < V_{CC}	–	–	20	μA
V_{SELECT}	input voltage SELECT pin	channel 1 = standby; channel 2 = on	0	–	1	V
		channel 1 = on; channel 2 = standby	V_{CC} – 1	–	V_{CC}	V
I_{SELECT}	input current SELECT pin	V_{SELECT} = 0 V	–	–	100	μA

Notes

1. Measured with $R_L = \infty$. With a load connected at the outputs the quiescent current will increase, the maximum of this increase being equal to the DC output offset voltage divided by R_L.
2. The DC output voltage with respect to ground is approximately $0.5V_{CC}$.

AC CHARACTERISTICS

V_{CC} = 5 V; T_{amb} = 25 °C; R_L = 8 Ω; f = 1 kHz; V_{MODE} = 0 V; gain = 20 dB; measured in BTL application circuit Fig.4; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_o	output power	THD = 10%	1	1.2	–	W
		THD = 0.5%	0.6	0.9	–	W
THD	total harmonic distortion	P_o = 0.5 W	–	0.15	0.3	%
G_v	closed loop voltage gain	note 1	6	–	30	dB
Z_i	differential input impedance		–	100	–	kΩ
V_{no}	noise output voltage	note 2	–	–	100	μV
SVRR	supply voltage ripple rejection	note 3	50	–	–	dB
		note 4	40	–	–	dB
V_o	output voltage	note 5	–	–	200	μV
α_{cs}	channel separation	$V_{SELECT} = 0.5V_{CC}$; note 6	40	–	–	dB

Notes

1. Gain of the amplifier is $2 \times \frac{R2}{R1}$ in BTL application circuit Fig.4.
2. The noise output voltage is measured at the output in a frequency range from 20 Hz to 20 kHz (unweighted), with a source impedance of R_S = 0 Ω at the input.
3. Supply voltage ripple rejection is measured at the output, with a source impedance of R_S = 0 Ω at the input. The ripple voltage is a sine wave with a frequency of 1 kHz and an amplitude of 100 mV (RMS), which is applied to the positive supply rail.
4. Supply voltage ripple rejection is measured at the output, with a source impedance of R_S = 0 Ω at the input. The ripple voltage is a sine wave with a frequency between 100 Hz and 20 kHz and an amplitude of 100 mV (RMS), which is applied to the positive supply rail.
5. Output voltage in mute position is measured with a 1 V (RMS) input voltage in a bandwidth of 20 Hz to 20 kHz, so including noise.
6. Channel separation is measured at the output with a source impedance of R_S = 0 Ω at the input and a frequency of 1 kHz. The output power in the operating channel is set to 0.5 W.

TEST AND APPLICATION INFORMATION

Test conditions

Because the application can be either Bridge-Tied Load (BTL) or Single-Ended (SE), the curves of each application are shown separately.

The thermal resistance = 55 K/W for the DIP16; the maximum sine wave power dissipation for T_{amb} = 25 °C is: $\frac{150 - 25}{55} = 2.3$ W

For T_{amb} = 60 °C the maximum total power dissipation is:

$\frac{150 - 60}{55} = 1.7$ W

BTL application

T_{amb} = 25 °C if not specially mentioned, V_{CC} = 5 V, f = 1 kHz, R_L = 8 Ω, G_v = 20 dB, audio band-pass 22 Hz to 22 kHz.

The BTL application circuit is illustrated in Fig.4.

The quiescent current has been measured without any load impedance and both channels driven. When one channel is active the quiescent current will be halved.
The total harmonic distortion as a function of frequency was measured using a low-pass filter of 80 kHz.
The value of capacitor C3 influences the behaviour of the SVRR at low frequencies: increasing the value of C3 increases the performance of the SVRR.
The figure of the MODE voltage (V_{MODE}) as a function of the supply voltage shows three areas; operating, mute and standby. It shows, that the DC-switching levels of the mute and standby respectively depend on the supply voltage level. The figure of the SELECT voltage (V_{SELECT}) as a function of the supply voltage shows the voltage levels for switching the channels in the active, mute or standby mode.

SE application

T_{amb} = 25 °C if not specially mentioned, V_{CC} = 7.5 V, f = 1 kHz, R_L = 4 Ω, G_v = 20 dB, audio band-pass 22 Hz to 22 kHz.

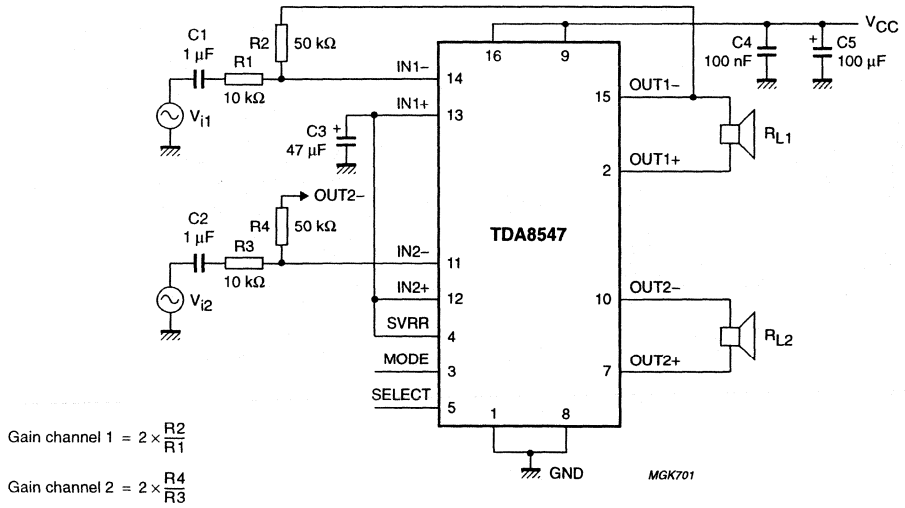
The SE application circuit is illustrated in Fig.16.

Increasing the value of electrolytic capacitor C3 will result in a better channel separation. Because the positive output is not designed for high output current (2 × I_o) at low load impedance (≤16 Ω), the SE application with output capacitors connected to ground is advised.
The capacitor value of C6/C7 in combination with the load impedance determines the low frequency behaviour.
The THD as a function of frequency was measured using a low-pass filter of 80 kHz. The value of capacitor C3 influences the behaviour of the SVRR at low frequencies: increasing the value of C3 increases the performance of the SVRR.

General remark

The frequency characteristic can be adapted by connecting a small capacitor across the feedback resistor. To improve the immunity to HF radiation in radio circuit applications, a small capacitor can be connected in parallel with the feedback resistor (56 kΩ); this creates a low-pass filter.

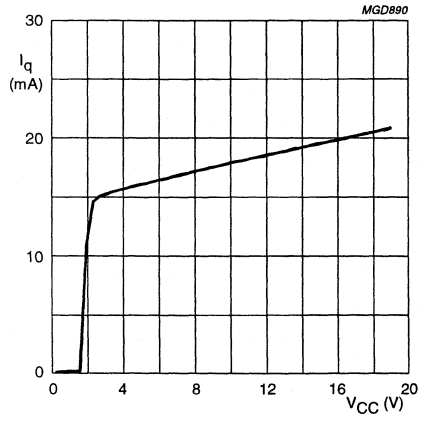
BTL APPLICATION



Gain channel 1 = $2 \times \frac{R2}{R1}$

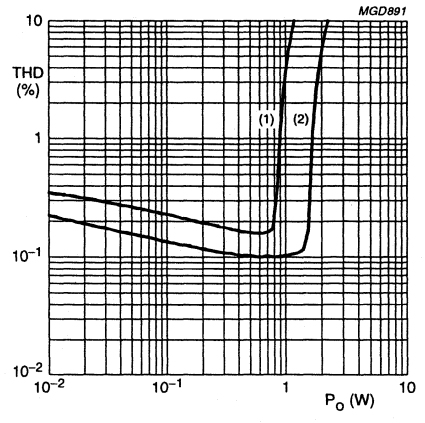
Gain channel 2 = $2 \times \frac{R4}{R3}$

Fig.4 BTL application.



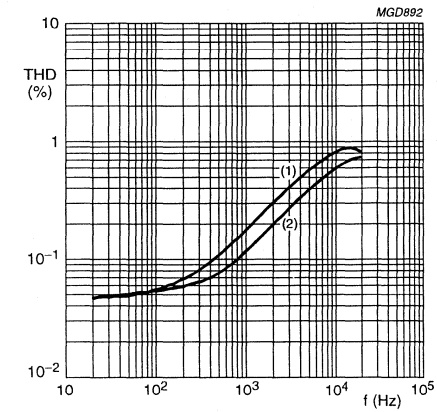
$R_L = \infty$.

Fig.5 I_q as a function of V_{CC}.



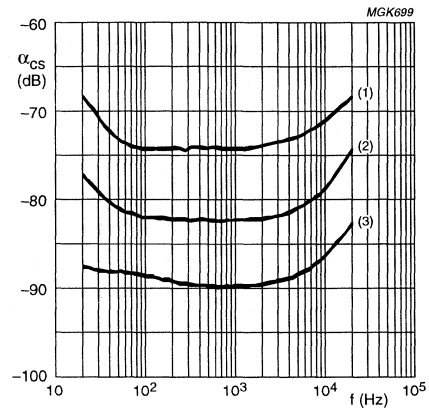
f = 1 kHz; G_v = 20 dB.
(1) V_{CC} = 5 V; R_L = 8 Ω.
(2) V_{CC} = 9 V; R_L = 16 Ω.

Fig.6 THD as a function of P_o.



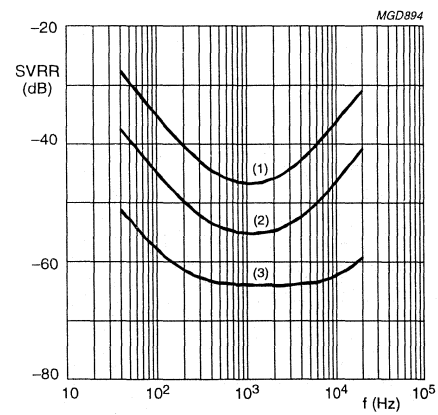
P_o = 0.5 W; G_v = 20 dB.
(1) V_{CC} = 5 V; R_L = 8 Ω.
(2) V_{CC} = 9 V; R_L = 16 Ω.

Fig.7 THD as a function of frequency.



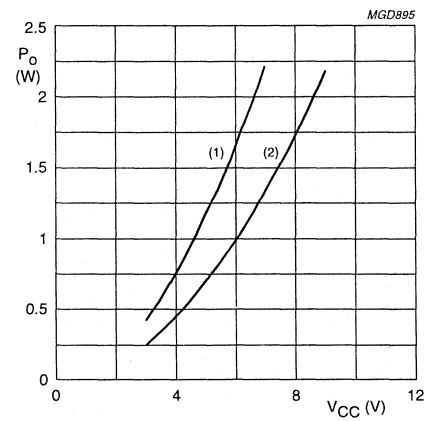
V_{CC} = 5 V; V_o = 2 V; R_L = 8 Ω.
(1) G_v = 30 dB.
(2) G_v = 20 dB.
(3) G_v = 6 dB.

Fig.8 Channel separation as a function of frequency.



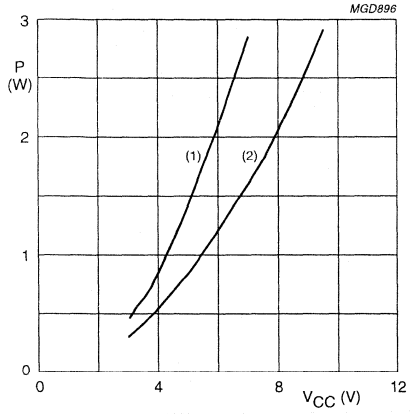
V_{CC} = 5 V; R_S = 0 Ω; V_r = 100 mV.
(1) G_v = 30 dB.
(2) G_v = 20 dB.
(3) G_v = 6 dB.

Fig.9 SVRR as a function of frequency.



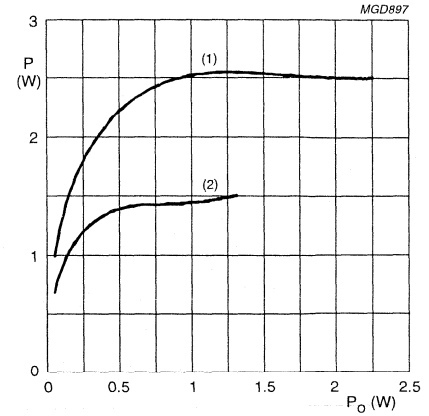
THD = 10%.
(1) R_L = 8 Ω.
(2) R_L = 16 Ω.

Fig.10 P_o as a function of V_{CC}.



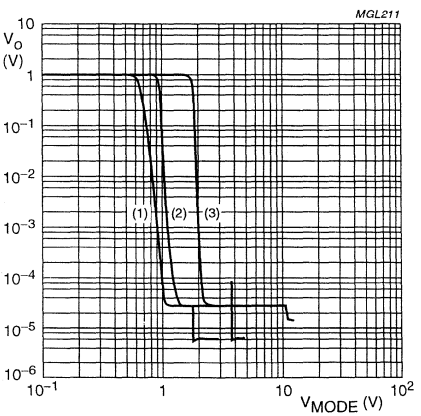
(1) R_L = 8 Ω.
(2) R_L = 16 Ω.

Fig.11 Worst case power dissipation as a function of V_{CC} (both channels on).



Sine wave of 1 kHz.
(1) V_{CC} = 9 V; R_L = 16 Ω.
(2) V_{CC} = 5 V; R_L = 8 Ω.

Fig.12 Power dissipation as a function of P_o (both channels on).



Band-pass = 22 Hz to 22 kHz.
(1) V_{CC} = 3 V.
(2) V_{CC} = 5 V.
(3) V_{CC} = 12 V.

Fig.13 V_o as a function of V_{MODE}.

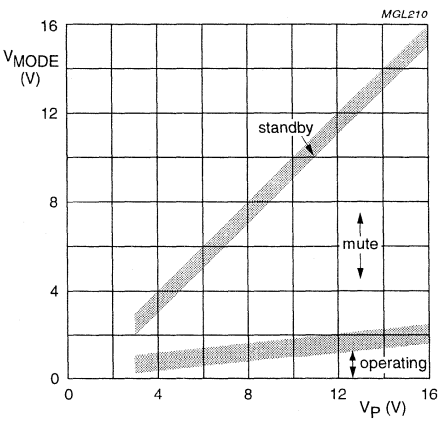


Fig.14 V_{MODE} as a function of V_P.

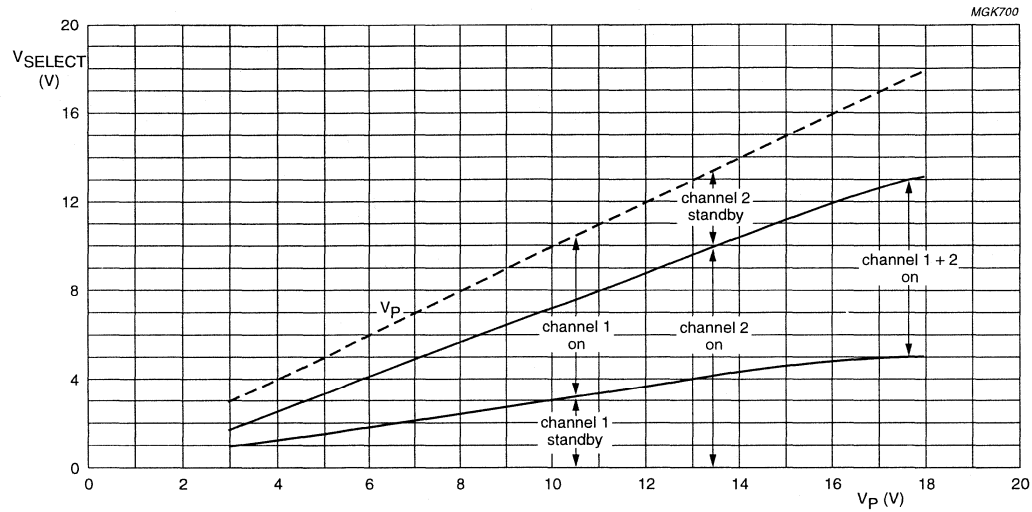


Fig.15 V_{SELECT} as a function of V_P.

SE APPLICATION

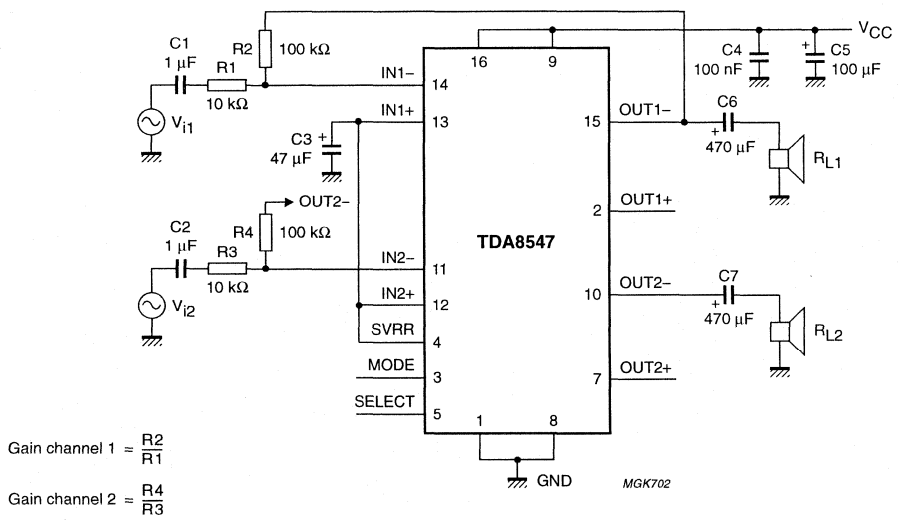
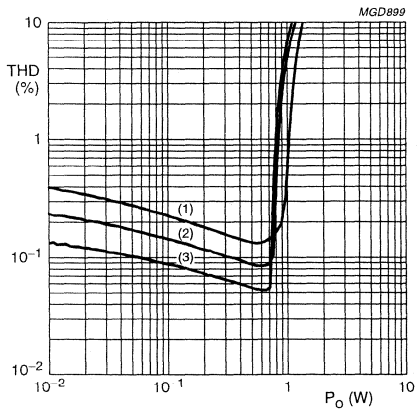
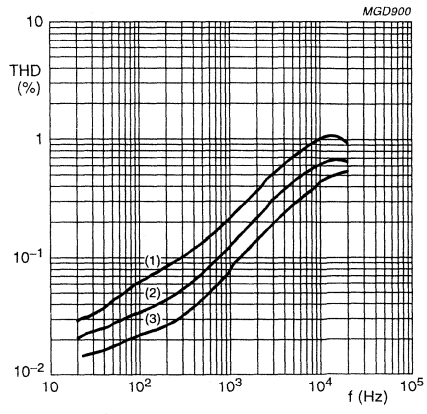


Fig.16 SE application.



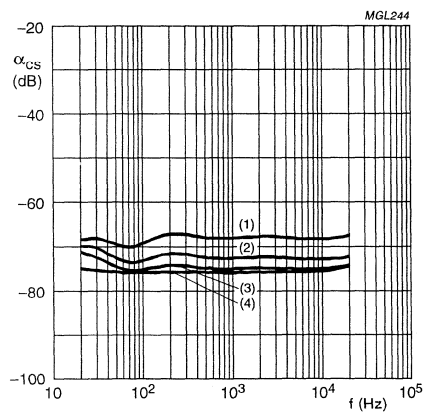
f = 1 kHz; G_v = 20 dB.
(1) V_{CC} = 7.5 V; R_L = 4 Ω.
(2) V_{CC} = 9 V; R_L = 8 Ω.
(3) V_{CC} = 12 V; R_L = 16 Ω.

Fig.17 THD as a function of P_o.



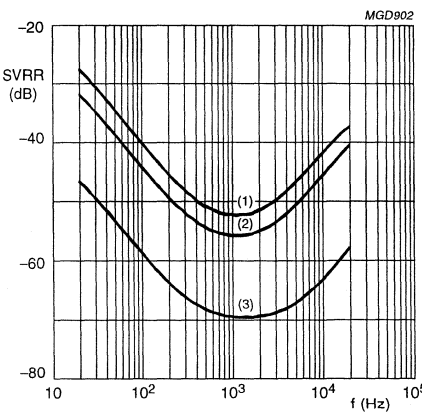
P_o = 0.5 W; G_v = 20 dB.
(1) V_{CC} = 7.5 V; R_L = 4 Ω.
(2) V_{CC} = 9 V; R_L = 8 Ω.
(3) V_{CC} = 12 V; R_L = 16 Ω.

Fig.18 THD as a function of frequency.



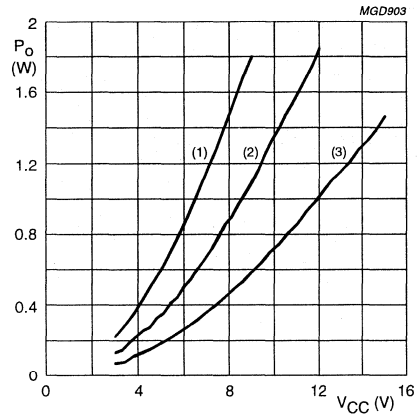
V_o = 1 V; G_v = 20 dB.
(1) V_{CC} = 7.5 V; R_L = 4 Ω.
(2) V_{CC} = 9 V; R_L = 8 Ω.
(3) V_{CC} = 12 V; R_L = 16 Ω.
(4) V_{CC} = 5 V; R_L = 32 Ω.

Fig.19 Channel separation as a function of frequency.



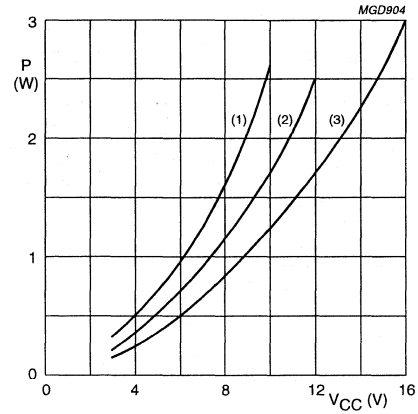
V_{CC} = 7.5 V; R_L = 4 Ω; R_S = 0 Ω; V_r = 100 mV.
(1) G_v = 24 dB.
(2) G_v = 20 dB.
(3) G_v = 0 dB.

Fig.20 SVRR as a function of frequency.



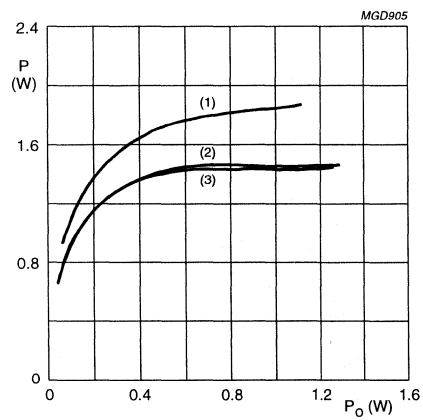
THD = 10%.
(1) R_L = 4 Ω.
(2) R_L = 8 Ω.
(3) R_L = 16 Ω.

Fig.21 P_o as a function of V_{CC}.



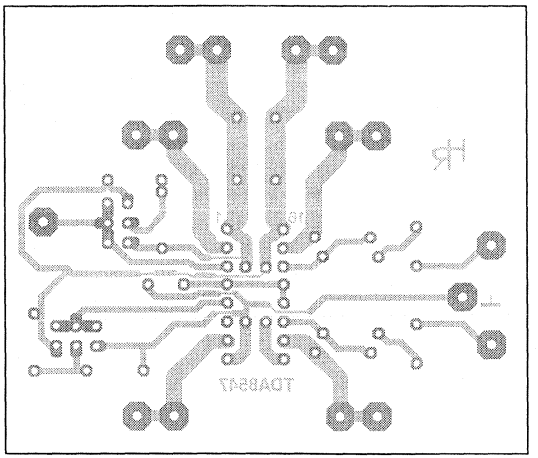
(1) R_L = 4 Ω.
(2) R_L = 8 Ω.
(3) R_L = 16 Ω.

Fig.22 Worst case power dissipation as a function of V_{CC} (both channels on).

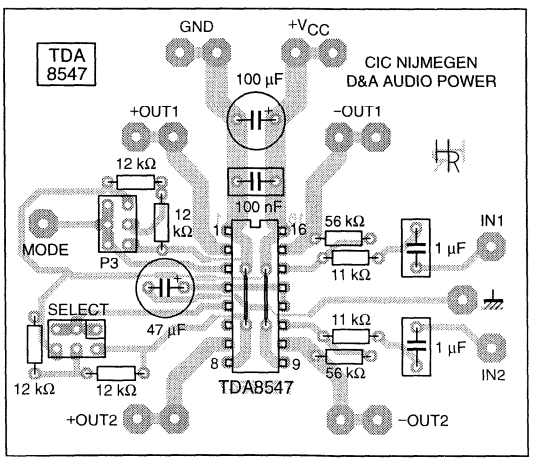


Sine wave of 1 kHz.
(1) V_{CC} = 12 V; R_L = 16 Ω.
(2) V_{CC} = 7.5 V; R_L = 4 Ω.
(3) V_{CC} = 9 V; R_L = 8 Ω.

Fig.23 Power dissipation as a function of P_o (both channels on).



a. Top view without components.



b. Top view with components.

Fig.24 Printed-circuit board layout (BTL and SE).

Hands free IC TEA1094; TEA1094A

FEATURES

- Low power consumption
- Power-down function (TEA1094A only)
- Microphone channel with:
  - externally adjustable gain
  - microphone mute function.
- Loudspeaker channel with:
  - externally adjustable gain
  - dynamic limiter to prevent distortion
  - rail-to-rail output stage for single-ended load drive
  - logarithmic volume control via linear potentiometer
  - loudspeaker mute function.
- Duplex controller consisting of:
  - signal envelope and noise envelope monitors for both channels with:
    externally adjustable sensitivity
    externally adjustable signal envelope time constant
    externally adjustable noise envelope time constant
  - decision logic with:
    externally adjustable switch-over timing
    externally adjustable idle mode timing
    externally adjustable dial tone detector in receive channel
  - voice switch control with:
    adjustable switching range
    constant sum of gain during switching
    constant sum of gain at different volume settings.

APPLICATIONS

- Mains, battery or line-powered telephone sets with hands-free/listening-in functions
- Cordless telephones
- Answering machines
- Fax machines.

GENERAL DESCRIPTION

The TEA1094 and TEA1094A are bipolar circuits intended for use in mains, battery or line-powered telephone sets, cordless telephones, answering machines and Fax machines. In conjunction with a member of the TEA106X, TEA111X families of transmission circuits, the devices offer a hands-free function. They incorporate a microphone amplifier, a loudspeaker amplifier and a duplex controller with signal and noise monitors on both channels.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA1094	DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1
TEA1094A	DIP24	plastic dual in-line package; 24 leads (600 mil)	SOT101-1
TEA1094T	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
TEA1094AT	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
TEA1094AM	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1

QUICK REFERENCE DATA

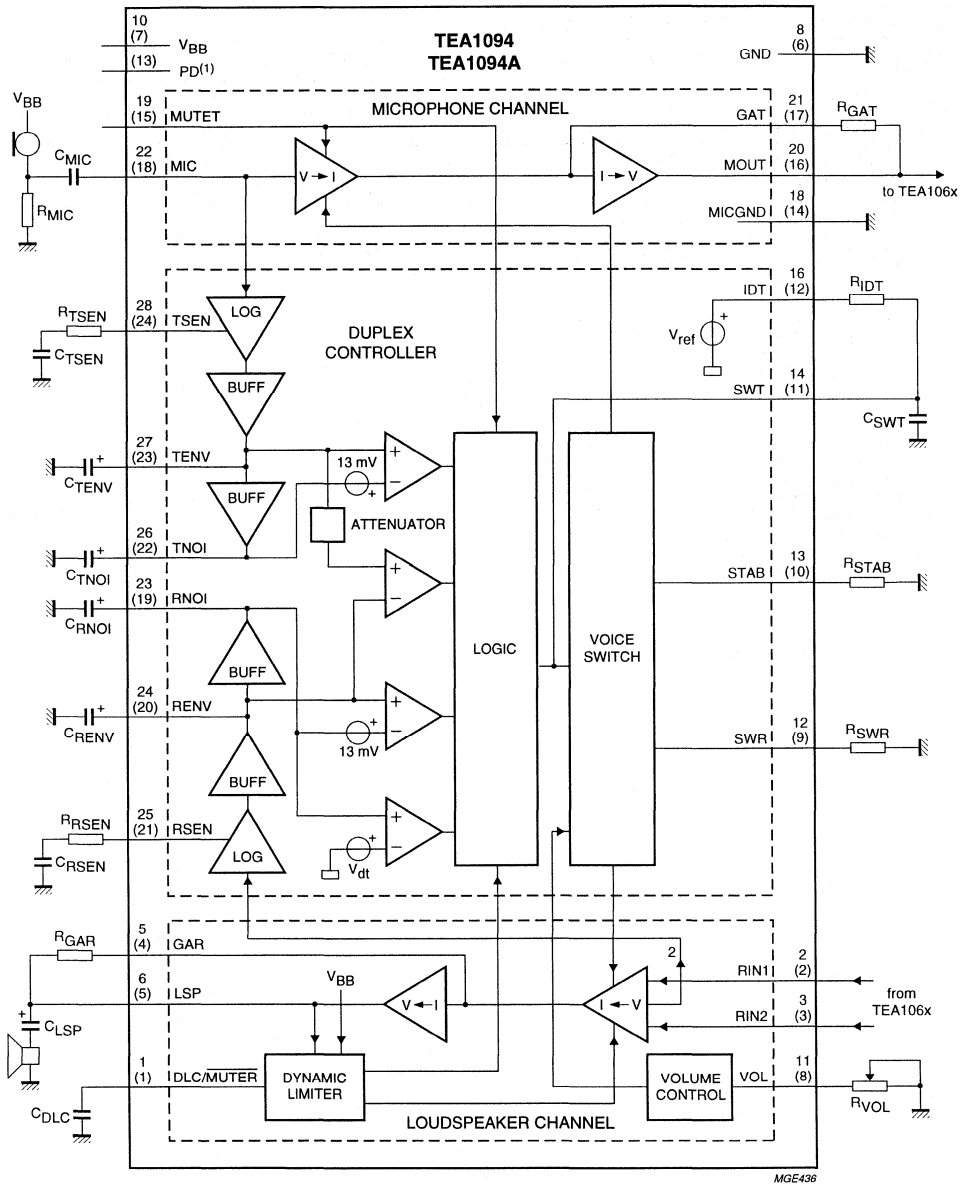
V_{BB} = 5 V; V_{GND} = 0 V; f = 1 kHz; T_{amb} = 25 °C; MUTET = LOW; PD = LOW (TEA1094A only); R_L = 50 Ω; R_{VOL} = 0 Ω; measured in test circuit of Fig.12; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{BB}	supply voltage		3.3	–	12.0	V
I_{BB}	current consumption from pin V_{BB}		–	3.1	4.4	mA
G_{vtx}	voltage gain from pin MIC to pin MOUT in transmit mode	V_{MIC} = 1 mV (RMS); R_{GAT} = 30.1 kΩ	13	15.5	18	dB
ΔG_{vtxr}	voltage gain adjustment with R_{GAT}		−15.5	–	+15.5	dB
G_{vrx}	voltage gain in receive mode; the difference between RIN1 and RIN2 to LSP	V_{RIN} = 20 mV (RMS); R_{GAR} = 66.5 kΩ; R_L = 50 Ω	16	18.5	21	dB
ΔG_{vrxr}	voltage gain adjustment with R_{GAR}		−18.5	–	+14.5	dB
$V_{O(p-p)}$	output voltage (peak-to-peak value)	V_{RIN} = 150 mV (RMS); R_{GAR} = 374 kΩ; R_L = 33 Ω; V_{BB} = 9.0 V; note 1	–	7.5	–	V
SWRA	switching range		–	40	–	dB
ΔSWRA	switching range adjustment with R_{SWR} referenced to R_{SWR} = 365 kΩ		−40	–	+12	dB
T_{amb}	operating ambient temperature		−25	–	+75	°C

Note

1. Corresponds to 200 mW output power.

BLOCK DIAGRAM



The pin numbers given in parenthesis are for the TEA1094A.

(1) TEA1094A only.

Fig.1 Block diagram.

PINNING

SYMBOL	PINS		DESCRIPTION
	TEA1094	TEA1094A	
DLC/$\overline{\text{MUTER}}$	1	1	dynamic limiter timing adjustment; receiver channel mute input
RIN1	2	2	receiver amplifier input 1
RIN2	3	3	receiver amplifier input 2
n.c.	4	–	not connected
GAR	5	4	receiver gain adjustment
LSP	6	5	loudspeaker amplifier output
n.c.	7	–	not connected
GND	8	6	ground reference
n.c.	9	–	not connected
V_{BB}	10	7	supply voltage
VOL	11	8	receiver volume adjustment
SWR	12	9	switching range adjustment
STAB	13	10	reference current adjustment
SWT	14	11	switch-over timing adjustment
n.c.	15	–	not connected
IDT	16	12	idle mode timing adjustment
PD	–	13	power-down input
n.c.	17	–	not connected
MICGND	18	14	ground reference for the microphone amplifier
MUTET	19	15	transmit channel mute input
MOUT	20	16	microphone amplifier output
GAT	21	17	microphone gain adjustment
MIC	22	18	microphone input
RNOI	23	19	receive noise envelope timing adjustment
RENV	24	20	receive signal envelope timing adjustment
RSEN	25	21	receive signal envelope sensitivity adjustment
TNOI	26	22	transmit noise envelope timing adjustment
TENV	27	23	transmit signal envelope timing adjustment
TSEN	28	24	transmit signal envelope sensitivity adjustment

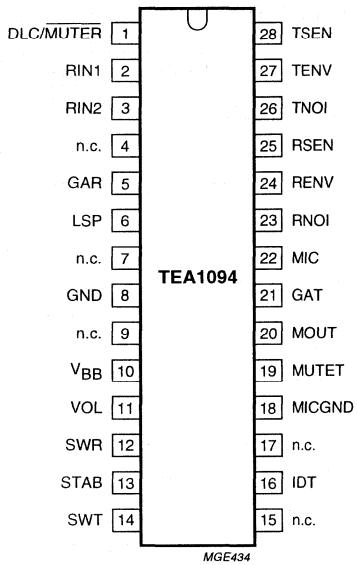


Fig.2 Pin configuration (TEA1094).

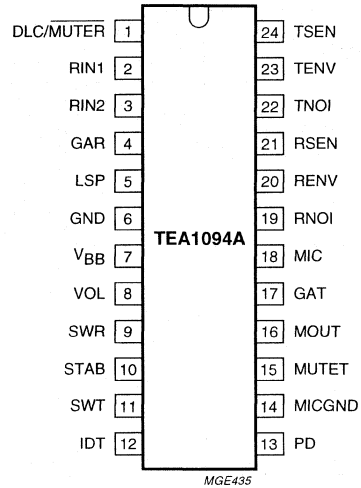


Fig.3 Pin configuration (TEA1094A).

FUNCTIONAL DESCRIPTION

General

The values given in the functional description are typical values unless otherwise specified.

A principle diagram of the TEA106X is shown on the left side of Fig.4. The TEA106X is a transmission circuit of the TEA1060 family intended for hand-set operation.
It incorporates a receiving amplifier for the earpiece, a transmit amplifier for the microphone and a hybrid.
For more details on the TEA1060 family, please refer to *"data Handbook IC03"*. The right side of Fig.4 shows a principle diagram of the TEA1094 and TEA1094A, hands-free add-on circuits with a microphone amplifier, a loudspeaker amplifier and a duplex controller.

As can be seen from Fig.4, a loop is formed via the sidetone network in the transmission circuit and the acoustic coupling between loudspeaker and microphone of the hands-free circuit. When this loop gain is greater than 1, howling is introduced. In a full duplex application, this would be the case.
The loop-gain has to be much lower than 1 and therefore has to be decreased to avoid howling. This is achieved by the duplex controller. The duplex controller of the TEA1094 and TEA1094A detects which channel has the 'largest' signal and then controls the gain of the microphone amplifier and the loudspeaker amplifier so that the sum of the gains remains constant.
As a result, the circuit can be in three stable modes:

1. Transmit mode (Tx mode).

   The gain of the microphone amplifier is at its maximum and the gain of the loudspeaker amplifier is at its minimum.

2. Receive mode (Rx mode).

   The gain of the loudspeaker amplifier is at its maximum and the gain of the microphone amplifier is at its minimum.

3. Idle mode.

   The gain of the amplifiers is halfway between their maximum and minimum value.

The difference between the maximum gain and minimum gain is called the switching range.

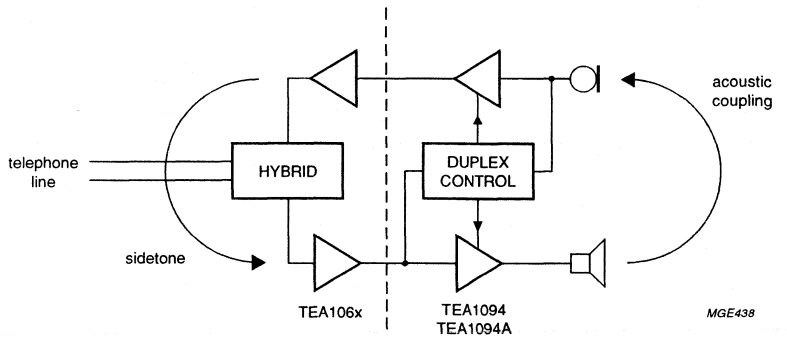


Fig.4 Hands-free telephone set principles.

Supply: pins V_{BB}, GND and PD

The TEA1094 and TEA1094A must be supplied with an external stabilized voltage source between pins V_{BB} and GND. In the idle mode, without any signal, the internal supply current is 3.1 mA at V_{BB} = 5 V.

To reduce the current consumption during pulse dialling or register recall (flash), the TEA1094A is provided with a power-down (PD) input. When the voltage on PD is HIGH the current consumption from V_{BB} is 180 μA.

Microphone channel: pins MIC, GAT, MOUT, MICGND and MUTET (see Fig.5)

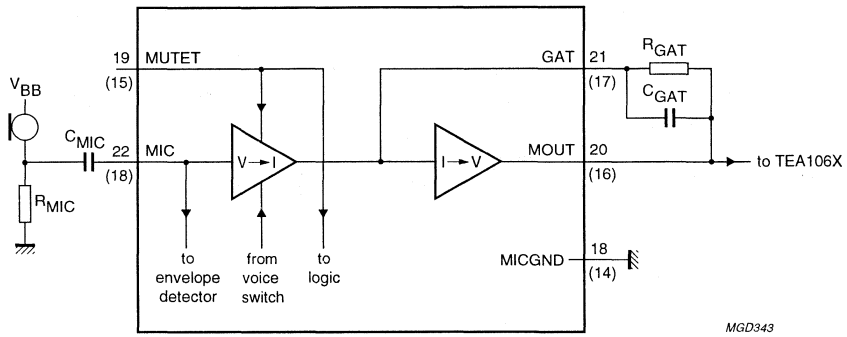
The TEA1094 and TEA1094A have an asymmetrical microphone input MIC with an input resistance of 20 kΩ. The gain of the input stage varies according to the mode of the TEA1094 and TEA1094A. In the transmit mode, the gain is at its maximum; in the receive mode, it is at its minimum and in the idle mode, it is halfway between maximum and minimum.

Switch-over from one mode to the other is smooth and click-free. The output capability at pin MOUT is 20 μA (RMS).

In the transmit mode, the overall gain of the microphone amplifier (from pins MIC to MOUT) can be adjusted from 0 dB up to 31 dB to suit specific application requirements. The gain is proportional to the value of R_{GAT} and equals 15.5 dB with R_{GAT} = 30.1 kΩ.

A capacitor must be connected in parallel with R_{GAT} to ensure stability of the microphone amplifier. Together with R_{GAT}, it also provides a first-order low-pass filter.

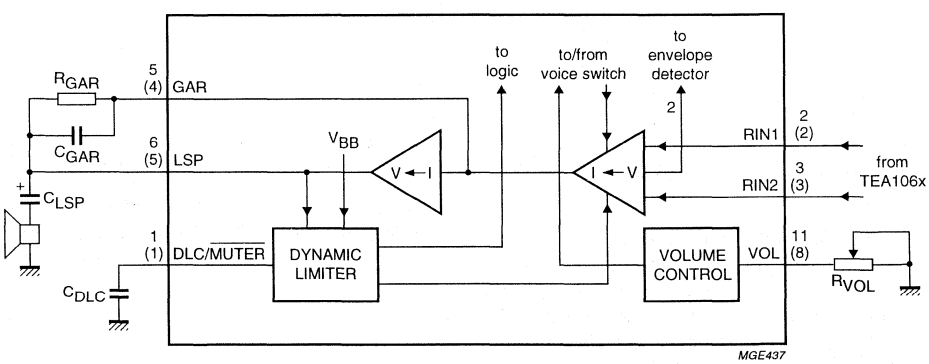
By applying a HIGH level on pin MUTET, the microphone amplifier is muted and the TEA1094 and TEA1094A are automatically forced into the receive mode.



The pin numbers given in parenthesis refer to the TEA1094A.

Fig.5 Microphone channel.

Loudspeaker channel



The pin numbers given in parenthesis refer to the TEA1094A.

Fig.6 Loudspeaker channel.

LOUDSPEAKER AMPLIFIER: PINS RIN1, RIN2, GAR AND LSP

The TEA1094 and TEA1094A have symmetrical inputs for the loudspeaker amplifier with an input resistance of 40 kΩ between RIN1 and RIN2 (2 × 20 kΩ). The input stage can accommodate signals up to 390 mV (RMS) at room temperature for 2% of total harmonic distortion (THD). The gain of the input stage varies according to the mode of the TEA1094 and TEA1094A. In the receive mode, the gain is at its maximum; in the transmit mode, it is at its minimum and in the idle mode, it is halfway between maximum and minimum. Switch-over from one mode to the other is smooth and click-free. The rail-to-rail output stage is designed to power a loudspeaker connected as a single-ended load (between LSP and GND).

In the receive mode, the overall gain of the loudspeaker amplifier can be adjusted from 0 dB up to 33 dB to suit specific application requirements. The gain from RIN1 and RIN2 to LSP is proportional to the value of R_{GAR} and equals 18.5 dB with R_{GAR} = 66.5 kΩ. A capacitor connected in parallel with R_{GAR} can be used to provide a first-order low-pass filter.

VOLUME CONTROL: PIN VOL

The loudspeaker amplifier gain can be adjusted with the potentiometer R_{VOL}. A linear potentiometer can be used to obtain logarithmic control of the gain at the loudspeaker amplifier. Each 950 Ω increase of R_{VOL} results in a gain loss of 3 dB. The maximum gain reduction with the volume control is internally limited to the switching range.

DYNAMIC LIMITER: PIN DLC/$\overline{\text{MUTER}}$

The dynamic limiter of the TEA1094 and TEA1094A prevents clipping of the loudspeaker output stage and protects the operation of the circuit when the supply voltage at V_{BB} falls below 2.9 V.

Hard clipping of the loudspeaker output stage is prevented by rapidly reducing the gain when the output stage starts to saturate. The time in which gain reduction is effected (clipping attack time) is approximately a few milliseconds. The circuit stays in the reduced gain mode until the peaks of the loudspeaker signals no longer cause saturation. The gain of the loudspeaker amplifier then returns to its normal value within the clipping release time (typically 250 ms). Both attack and release times are proportional to the value of the capacitor C_{DLC}. The total harmonic distortion of the loudspeaker output stage, in reduced gain mode, stays below 5% up to 10 dB (minimum) of input voltage overdrive [providing V_{RIN} is below 390 mV (RMS)].

When the supply voltage drops below an internal threshold voltage of 2.9 V, the gain of the loudspeaker amplifier is rapidly reduced (approximately 1 ms). When the supply voltage exceeds 2.9 V, the gain of the loudspeaker amplifier is increased again.

By forcing a level lower than 0.2 V on pin DLC/$\overline{\text{MUTER}}$, the loudspeaker amplifier is muted and the TEA1094 (TEA1094A) is automatically forced into the transmit mode.

Duplex controller

SIGNAL AND NOISE ENVELOPE DETECTORS: PINS TSEN, TENV, TNOI, RSEN, RENV AND RNOI

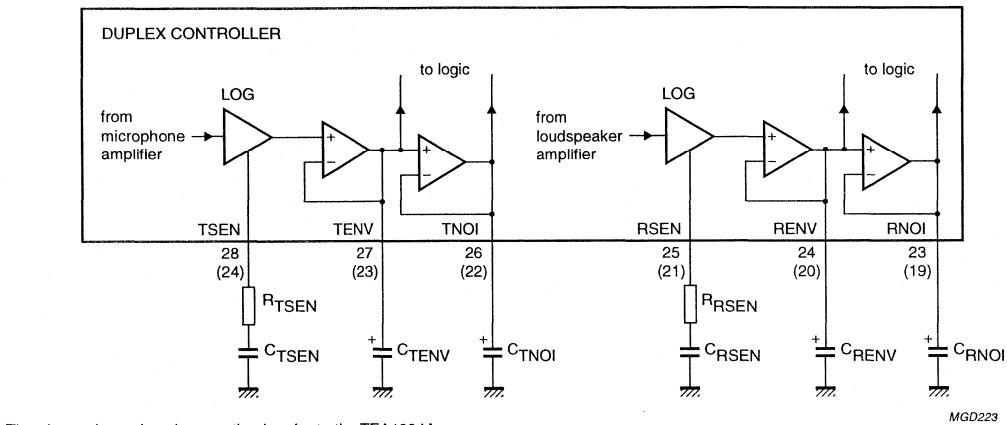
The signal envelopes are used to monitor the signal level strength in both channels. The noise envelopes are used to monitor background noise in both channels. The signal and noise envelopes provide inputs for the decision logic. The signal and noise envelope detectors are shown in Fig.7.

For the transmit channel, the input signal at MIC is 40 dB amplified to TSEN. For the receive channel, the differential signal between RIN1 and RIN2 is 0 dB amplified to RSEN. The signals from TSEN and RSEN are logarithmically compressed and buffered to TENV and RENV respectively. The sensitivity of the envelope detectors is set with R_{TSEN} and R_{RSEN}. The capacitors connected in series with the two resistors block any DC component and form a first-order high-pass filter. In the basic application, see Fig.13, it is assumed that V_{MIC} = 1 mV (RMS) and V_{RIN} = 100 mV (RMS) nominal and both R_{TSEN} and R_{RSEN} have a value of 10 kΩ. With the value of C_{TSEN} and C_{RSEN} at 100 nF, the cut-off frequency is at 160 Hz.

The buffer amplifiers leading the compressed signals to TENV and RENV have a maximum source current of 120 μA and a maximum sink current of 1 μA. Together with the capacitor C_{TENV} and C_{RENV}, the timing of the signal envelope monitors can be set. In the basic application, the value of both capacitors is 470 nF. Because of the logarithmic compression, each 6 dB signal increase means 18 mV increase of the voltage on the envelopes TENV or RENV at room temperature. Thus, timings can be expressed in dB/ms. At room temperature, the 120 μA sourced current corresponds to a maximum rise-slope of the signal envelope of 85 dB/ms. This is sufficient to track normal speech signals. The 1 μA current sunk by TENV or RENV corresponds to a maximum fall-slope of 0.7 dB/ms. This is sufficient for a smooth envelope and also eliminates the effect of echoes on switching behaviour.

To determine the noise level, the signals on TENV and RENV are buffered to TNOI and RNOI. These buffers have a maximum source current of 1 μA and a maximum sink current of 120 μA. Together with the capacitors C_{TNOI} and C_{RNOI}, the timing can be set. In the basic application of Fig.13 the value of both capacitors is 4.7 μF. At room temperature, the 1 μA sourced current corresponds to a maximum rise-slope of the noise envelope of approximately 0.07 dB/ms.

This is small enough to track background noise and not to be influenced by speech bursts. The 120 μA current that is sunk corresponds to a maximum fall-slope of approximately 8.5 dB/ms. However, during the decrease of the signal envelope, the noise envelope tracks the signal envelope so it will never fall faster than approximately 0.7 dB/ms. The behaviour of the signal envelope and noise envelope monitors is illustrated in Fig.8.



The pin numbers given in parenthesis refer to the TEA1094A.

Fig.7 Signal and noise envelope detectors.

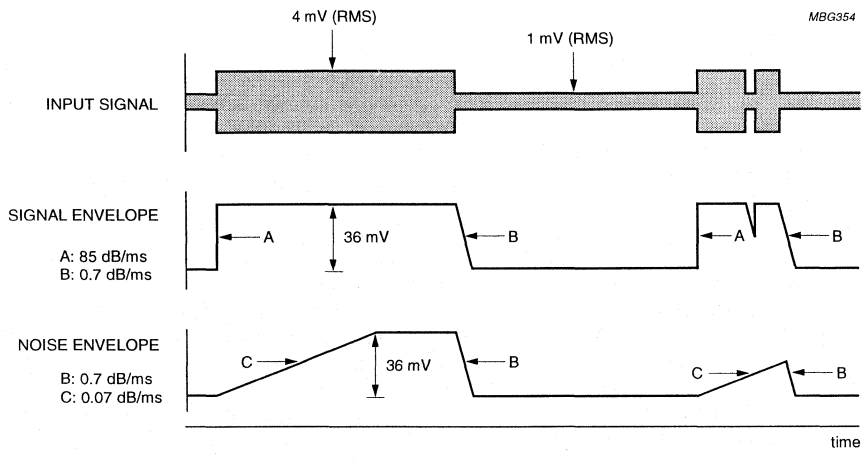
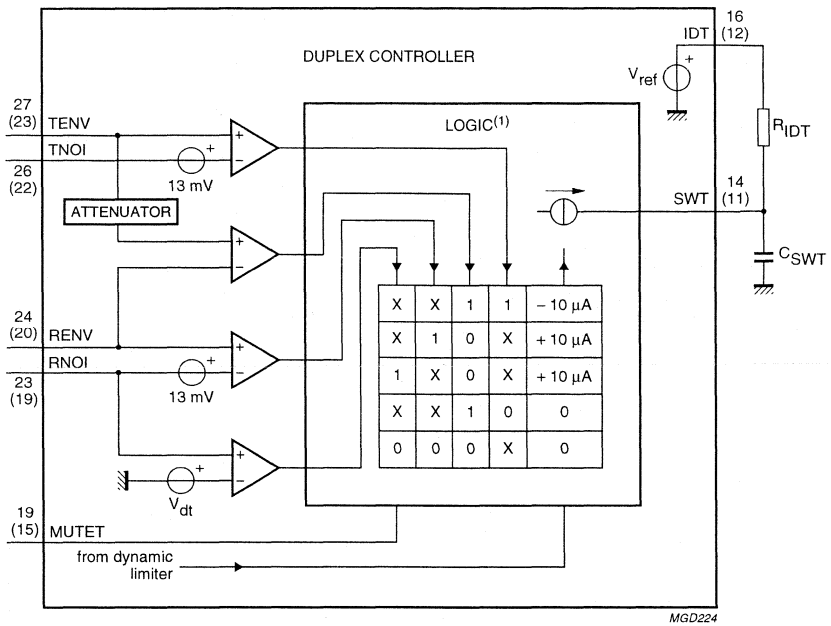


Fig.8 Signal and noise envelope waveforms.

DECISION LOGIC: PINS IDT AND SWT



The pin numbers given in parenthesis refer to the TEA1094A.

(1) When MUTET = HIGH, +10 µA is forced.
When DLC/$\overline{\text{MUTER}}$ < 0.2 V, −10 µA is forced.

Fig.9 Decision logic.

The TEA1094 and TEA1094A select their modes of operation (transmit, receive or idle mode) by comparing the signal and the noise envelopes of both channels. This is executed by the decision logic. The resulting voltage on pin SWT is the input for the voice-switch.

To facilitate the distinction between signal and noise, the signal is considered as speech when its envelope is more than 4.3 dB above the noise envelope. At room temperature, this is equal to a voltage difference $V_{ENV} - V_{NOI} = 13$ mV. This so called speech/noise threshold is implemented in both channels.

The signal on MIC contains both speech and the signal coming from the loudspeaker (acoustic coupling). When receiving, the contribution from the loudspeaker overrules the speech.

As a result, the signal envelope on TENV is formed mainly by the loudspeaker signal. To correct this, an attenuator is connected between TENV and the TENV/RENV comparator. Its attenuation equals that applied to the microphone amplifier.

When a dial tone is present on the line, without monitoring, the tone would be recognized as noise because it is a signal with a constant amplitude. This would cause the TEA1094 (TEA1094A) to go into the idle mode and the user of the set would hear the dial tone fade away. To prevent this, a dial tone detector is incorporated which, in standard applications, does not consider input signals between RIN1 and RIN2 as noise when they have a level greater than 127 mV (RMS). This level is proportional to R_{RSEN}.

As can be seen from Fig.9, the output of the decision logic is a current source. The logic table gives the relationship between the inputs and the value of the current source. It can charge or discharge the capacitor C_{SWT} with a current of 10 μA (switch-over). If the current is zero, the voltage on SWT becomes equal to the voltage on IDT via the high-ohmic resistor R_{IDT} (idling). The resulting voltage difference between SWT and IDT determines the mode of the TEA1094 (TEA1094A) and can vary between −400 and +400 mV (see Table 1).

Table 1 Modes of TEA1094; TEA1094A

$V_{SWT} - V_{IDT}$ (mV)	MODE
<−180	transmit mode
0	idle mode
>180	receive mode

The switch-over timing can be set with C_{SWT}, the idle mode timing with C_{SWT} and R_{IDT}. In the basic application given in Fig.13, C_{SWT} is 220 nF and R_{IDT} is 2.2 MΩ. This enables a switch-over time from transmit to receive mode or vice-versa of approximately 13 ms (580 mV swing on SWT). The switch-over time from idle mode to transmit mode or receive mode is approximately 4 ms (180 mV swing on SWT).

The switch-over time, from receive mode or transmit mode to idle mode, is equal to $4 \times R_{IDT}C_{SWT}$ and is approximately 2 seconds (idle mode time).

The inputs MUTET and DLC/$\overline{\text{MUTER}}$ overrule the decision logic. When MUTET goes HIGH, the capacitor C_{SWT} is charged with 10 μA thus resulting in the receive mode. When the voltage on pin DLC/$\overline{\text{MUTER}}$ goes lower than 0.2 V, the capacitor C_{SWT} is discharged with 10 μA thus resulting in the transmit mode.

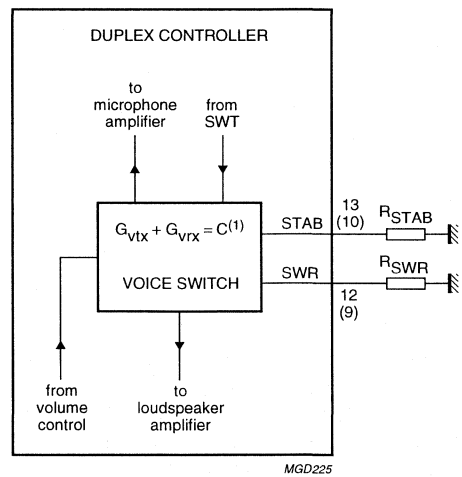
VOICE-SWITCH: PINS STAB AND SWR

A diagram of the voice-switch is illustrated in Fig.10. With the voltage on SWT, the TEA1094 (TEA1094A) voice-switch regulates the gains of the transmit and the receive channel so that the sum of both is kept constant.

In the transmit mode, the gain of the microphone amplifier is at its maximum and the gain of the loudspeaker amplifier is at its minimum. In the receive mode, the opposite applies. In the idle mode, both microphone and loudspeaker amplifier gains are halfway.

The difference between maximum and minimum is the so called switching range. This range is determined by the ratio of R_{SWR} and R_{STAB} and is adjustable between 0 and 52 dB. R_{STAB} should be 3.65 kΩ and sets an internally used reference current. In the basic application diagram given in Fig.13, R_{SWR} is 365 kΩ which results in a switching range of 40 dB. The switch-over behaviour is illustrated in Fig.11.

In the receive mode, the gain of the loudspeaker amplifier can be reduced using the volume control. Since the voice-switch keeps the sum of the gains constant, the gain of the microphone amplifier is increased at the same time (see dashed curves in Fig.11). In the transmit mode, however, the volume control has no influence on the gain of the microphone amplifier or the gain of the loudspeaker amplifier. Consequently, the switching range is reduced when the volume is reduced. At maximum reduction of volume, the switching range becomes 0 dB.



The pin numbers given in parenthesis refer to the TEA1094A.
(1) C = constant.

Fig.10 Voice switch.

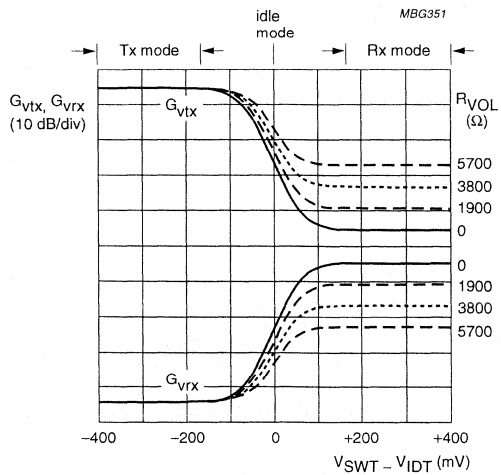


Fig.11 Switch-over behaviour.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{n(max)}$	maximum voltage on all pins; except pins V_{BB}, RIN1 and RIN2		$V_{GND} - 0.4$	$V_{BB} + 0.4$	V
$V_{RIN(max)}$	maximum voltage on pins RIN1 and RIN2		$V_{GND} - 1.2$	$V_{BB} + 0.4$	V
$V_{BB(max)}$	maximum voltage on pin V_{BB}		$V_{GND} - 0.4$	12.0	V
P_{tot}	total power dissipation	T_{amb} = 75 °C			
	TEA1094		–	1000	mW
	TEA1094A		–	910	mW
	TEA1094T		–	625	mW
	TEA1094AT		–	590	mW
	TEA1094AM		–	438	mW
T_{stg}	IC storage temperature		−40	+125	°C
T_{amb}	operating ambient temperature		−25	+75	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	TEA1094	45	K/W
	TEA1094A	50	K/W
	TEA1094T	70	K/W
	TEA1094AT	75	K/W
	TEA1094AM	104	K/W

CHARACTERISTICS

V_{BB} = 5 V; V_{GND} = 0 V; f = 1 kHz; T_{amb} = 25 °C; MUTET = LOW; PD = LOW (TEA1094A only); R_L = 50 Ω; R_{VOL} = 0 Ω; measured in test circuit of Fig.12; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (V_{BB}, GND and PD)						
V_{BB}	supply voltage		3.3	–	12.0	V
I_{BB}	current consumption from pin V_{BB}		–	3.1	4.4	mA
POWER-DOWN INPUT PD (TEA1094A ONLY)						
V_{IL}	LOW level input voltage		V_{GND} – 0.4	–	0.3	V
V_{IH}	HIGH level input voltage		1.5	–	V_{BB} + 0.4	V
I_{PD}	input current	PD = HIGH	–	2.5	5	µA
$I_{BB(PD)}$	current consumption from pin V_{BB} in power-down condition	PD = HIGH	–	180	240	µA
Microphone channel (MIC, GAT, MOUT, MUTET and MICGND)						
MICROPHONE AMPLIFIER						
$\|Z_i\|$	input impedance between pins MIC and MICGND		17	20	23	kΩ
G_{vtx}	voltage gain from pin MIC to MOUT in transmit mode	V_{MIC} = 1 mV (RMS)	13	15.5	18	dB
ΔG_{vtxr}	voltage gain adjustment with R_{GAT}		–15.5	–	+15.5	dB
ΔG_{vtxT}	voltage gain variation with temperature referenced to 25 °C	V_{MIC} = 1 mV (RMS); T_{amb} = –25 to +75 °C	–	±0.3	–	dB
ΔG_{vtxf}	voltage gain variation with frequency referenced to 1 kHz	V_{MIC} = 1 mV (RMS); f = 300 to 3400 Hz	–	±0.3	–	dB
V_{notx}	noise output voltage at pin MOUT	pin MIC connected to MICGND through 200 Ω in series with 10 µF; psophometrically weighted (P53 curve)	–	–100	–	dBmp

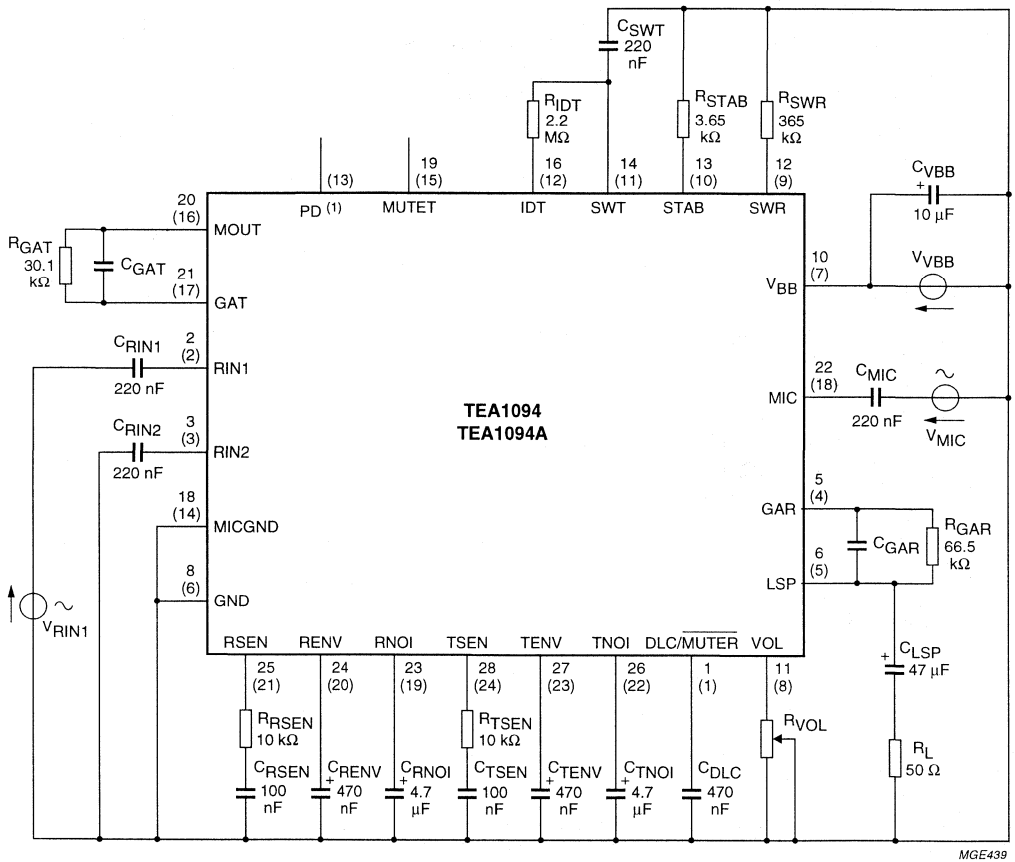
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
TRANSMIT MUTE INPUT MUTET						
V_{IL}	LOW level input voltage		V_{GND} – 0.4	–	0.3	V
V_{IH}	HIGH level input voltage		1.5	–	V_{BB} + 0.4	V
I_{MUTET}	input current	MUTET = HIGH	–	2.5	5	µA
ΔG_{vtxm}	voltage gain reduction with MUTET active	MUTET = HIGH	–	80	–	dB
Loudspeaker channel (RIN1, RIN2, GAR, LSP and DLC/$\overline{\text{MUTER}}$)						
LOUDSPEAKER AMPLIFIER						
$\|Z_i\|$	input impedance	between pins RIN1 or RIN2 and GND	17	20	23	kΩ
		between pins RIN1 and RIN2	34	40	46	kΩ
G_{vrx}	voltage gain in receive mode; between RIN1 and RIN2 to LSP	V_{RIN} = 20 mV (RMS)	16	18.5	21	dB
ΔG_{vrxr}	voltage gain adjustment with R_{GAR}		–18.5	–	+14.5	dB
ΔG_{vrxT}	voltage gain variation with temperature referenced to 25 °C	V_{RIN} = 20 mV (RMS); T_{amb} = –25 to +75 °C	–	±0.3	–	dB
ΔG_{vrxf}	voltage gain variation with frequency referenced to 1 kHz	V_{RIN} = 20 mV (RMS); f = 300 to 3400 Hz	–	±0.3	–	dB
$V_{RIN(rms)}$	maximum input voltage between RIN1 and RIN2 (RMS value)	R_{GAR} = 11.8 kΩ; for 2% THD in input stage	–	390	–	mV
$V_{norx(rms)}$	noise output voltage at pin LSP (RMS value)	inputs RIN1 and RIN2 short-circuited through 200 Ω in series with 10 µF; psophometrically weighted (P53 curve)	–	80	–	µV
CMRR	common mode rejection ratio		–	50	–	dB
ΔG_{vrxv}	voltage gain variation related to ΔR_{VOL} = 950 Ω	when total attenuation does not exceed the switching range	–	3	–	dB
OUTPUT CAPABILITY						
$V_{OSE(p-p)}$	output voltage (peak-to-peak value)	V_{RIN} = 300 mV (RMS); note 1	3.5	4.5	–	V
		V_{RIN} = 150 mV (RMS); R_{GAR} = 374 kΩ; R_L = 33 Ω; V_{BB} = 9.0 V; note 2	–	7.5	–	V
I_{OM}	maximum output current at LSP (peak value)		150	500	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DYNAMIC LIMITER						
t_{att}	attack time when V_{RIN} jumps from 20 mV to 20 mV + 10 dB	R_{GAR} = 374 kΩ	–	–	5	ms
t_{rel}	release time when V_{RIN} jumps from 20 mV + 10 dB to 20 mV	R_{GAR} = 374 kΩ	–	250	–	ms
THD	total harmonic distortion at V_{RIN} = 20 mV + 10 dB	R_{GAR} = 374 kΩ; $t > t_{att}$	–	0.9	5	%
$V_{BB(th)}$	V_{BB} limiter threshold		–	2.9	–	V
t_{att}	attack time when V_{BB} jumps below $V_{BB(th)}$		–	1	–	ms
MUTE RECEIVE						
$V_{DLC(th)}$	threshold voltage required on pin DLC/$\overline{\text{MUTER}}$ to obtain mute receive condition		V_{GND} – 0.4	–	0.2	V
$I_{DLC(th)}$	threshold current sourced by pin DLC/$\overline{\text{MUTER}}$ in mute receive condition	V_{DLC} = 0.2 V	–	100	–	µA
ΔG_{vrxm}	voltage gain reduction in mute receive condition	V_{DLC} < 0.2 V	–	80	–	dB
Envelope and noise detectors (TSEN, TENV, RSEN, RENV, RNOI and TNOI)						
PREAMPLIFIERS						
$G_{v(TSEN)}$	voltage gain from MIC to TSEN		37.5	40	42.5	dB
$G_{v(RSEN)}$	voltage gain between RIN1 and RIN2 to RSEN		–2.5	0	+2.5	dB
LOGARITHMIC COMPRESSOR AND SENSITIVITY ADJUSTMENT						
$\Delta V_{det(TSEN)}$	sensitivity detection on pin TSEN; voltage change on pin TENV when doubling the current from TSEN	I_{TSEN} = 0.8 to 160 µA	–	18	–	mV
$\Delta V_{det(RSEN)}$	sensitivity detection on pin RSEN; voltage change on pin RENV when doubling the current from RSEN	I_{RSEN} = 0.8 to 160 µA	–	18	–	mV
SIGNAL ENVELOPE DETECTORS						
$I_{source(ENV)}$	maximum current sourced from pin TENV or RENV		–	120	–	µA
$I_{sink(ENV)}$	maximum current sunk by pin TENV or RENV		0.75	1	1.25	µA
ΔV_{ENV}	voltage difference between pins RENV and TENV	when 10 µA is sourced from both RSEN and TSEN; envelope detectors tracking; note 3	–	±3	–	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
NOISE ENVELOPE DETECTORS						
$I_{source(NOI)}$	maximum current sourced from pins TNOI or RNOI		0.75	1	1.25	µA
$I_{sink(NOI)}$	maximum current sunk by pins TNOI or RNOI		–	120	–	µA
ΔV_{NOI}	voltage difference between pins RNOI and TNOI	when 5 µA is sourced from both RSEN and TSEN; noise detectors tracking; note 3	–	±3	–	mV
DIAL TONE DETECTOR						
$V_{RINDT(rms)}$	threshold level at pins RIN1 and RIN2 (RMS value)		–	127	–	mV
Decision logic (IDT and SWT)						
SIGNAL RECOGNITION						
$\Delta V_{Srx(th)}$	threshold voltage between pins RENV and RNOI to switch-over from receive to idle mode	$V_{RIN} < V_{RINDT}$; note 4	–	13	–	mV
$\Delta V_{Stx(th)}$	threshold voltage between pins TENV and TNOI to switch-over from transmit to idle mode	note 4	–	13	–	mV
SWITCH-OVER						
$I_{source(SWT)}$	current sourced from pin SWT when switching to receive mode		7.5	10	12.5	µA
$I_{sink(SWT)}$	current sunk by pin SWT when switching to transmit mode		7.5	10	12.5	µA
$I_{idle(SWT)}$	current sourced from pin SWT in idle mode		–	0	–	µA
Voice switch (STAB and SWR)						
SWRA	switching range		–	40	–	dB
ΔSWRA	switching range adjustment	with R_{SWR} referenced to 365 kΩ	–40	–	+12	dB
$\lvert\Delta G_v\rvert$	voltage gain variation from transmit mode to idle mode on both channels		–	20	–	dB
G_{tr}	gain tracking ($G_{vtx} + G_{vrx}$) during switching, referenced to idle mode		–	±0.5	–	dB

Notes

1. Corresponds to 50 mW output power.
2. Corresponds to 200 mW output power.
3. Corresponds to ±1 dB tracking.
4. Corresponds to 4.3 dB noise/speech recognition level.



The pin numbers given in parenthesis refer to the TEA1094A.

(1) TEA1094A only.

Fig.12 Test circuit.

APPLICATION INFORMATION

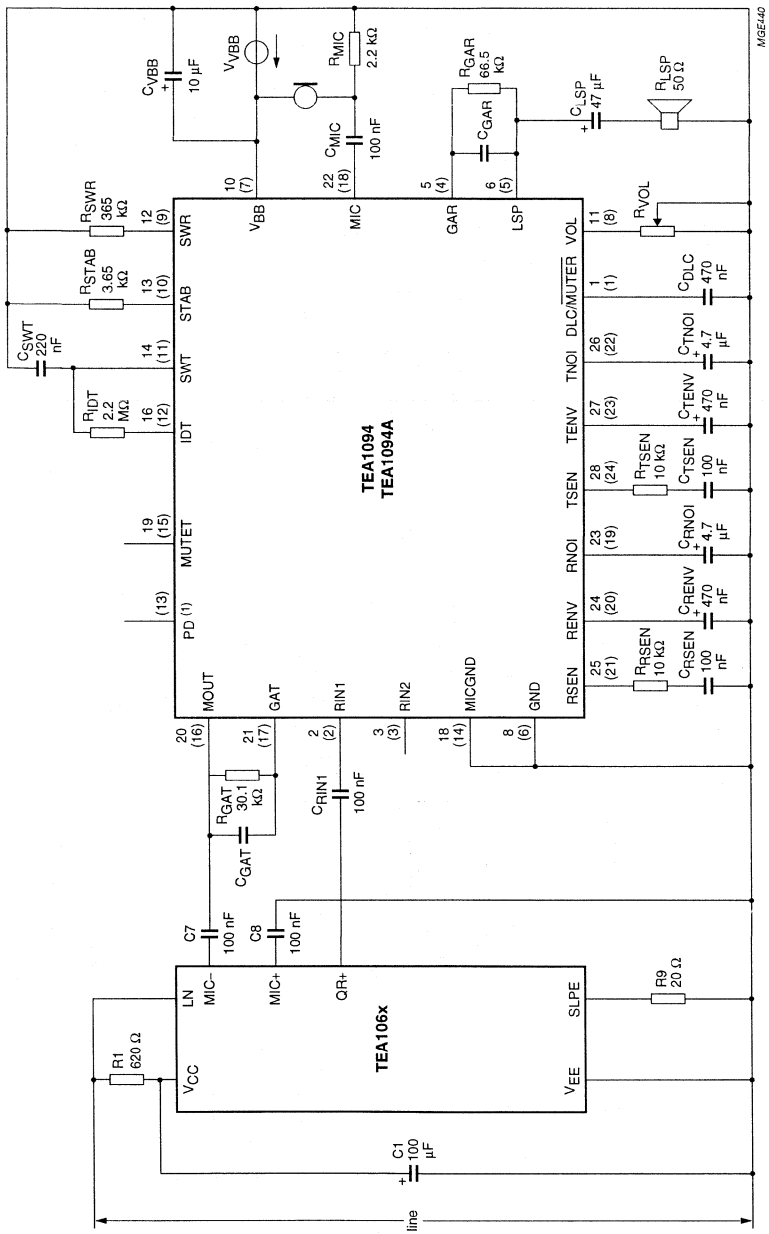


Fig.13 Basic application diagram.

The pin numbers given in parenthesis refer to the TEA1094A.

(1) TEA1094A only.

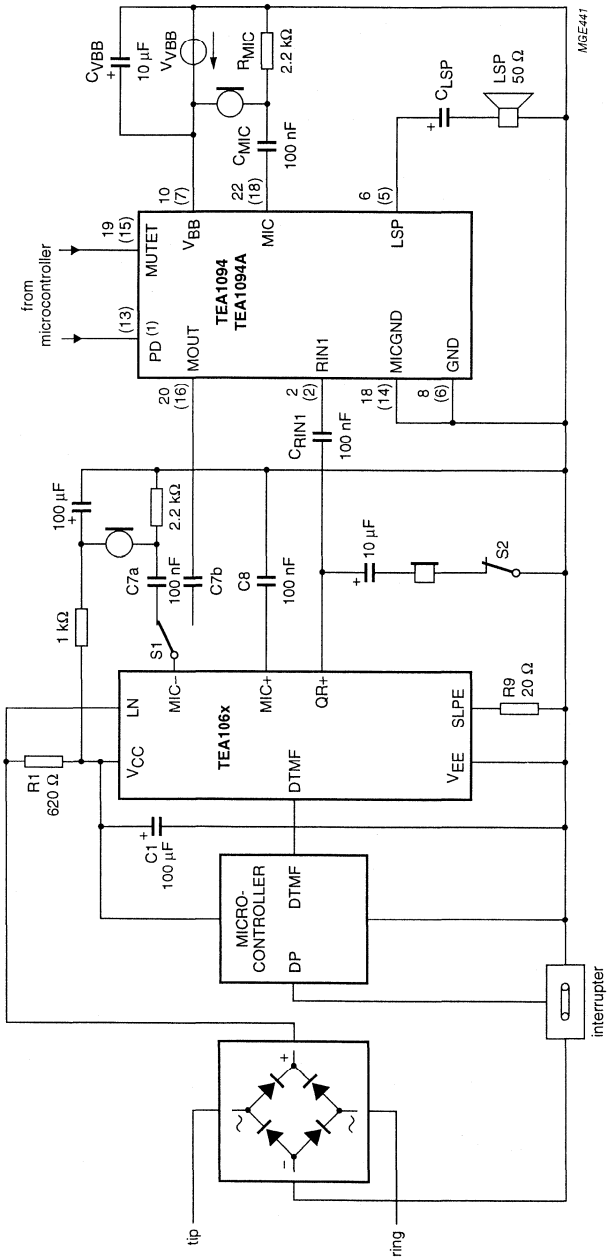


Fig.14 Application example.

The pin numbers given in parenthesis refer to the TEA1094A.

(1) TEA1094A only.

Voice switched speakerphone IC TEA1095

FEATURES

- External power supply with power-down function
- Transmit channel with:
  - externally adjustable gain
  - transmit mute function
- Receive channel with:
  - externally adjustable gain
  - logarithmic volume control via a linear potentiometer
  - receive mute function
- Duplex controller consisting of:
  - signal envelope and noise envelope monitors for both channels with:
    externally adjustable sensitivity
    externally adjustable signal envelope time constant
    externally adjustable noise envelope time constant
  - decision logic with:
    externally adjustable switch-over timing
    externally adjustable idle mode timing
    externally adjustable dial tone detector in receive channel
  - voice switch control with:
    adjustable switching range
    constant sum of gain during switching
    constant sum of gain at different volume settings.

APPLICATIONS

- Mains, battery or line-powered telephone sets
- Cordless telephones
- Answering machines
- Fax machines
- Hands-free car kits.

GENERAL DESCRIPTION

The TEA1095 is a bipolar circuit, that in conjunction with a member of the TEA106X, TEA111X families of transmission or TEA1096 transmission/iistening-in circuits offers a hands-free function. It incorporates a transmit amplifier, a receiver channel amplifier and a duplex controller with signal and noise monitors on both channels.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA1095	DIP24	plastic dual in-line package; 24 leads (600 mil)	SOT101-1
TEA1095T	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
TEA1095TS	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1

QUICK REFERENCE DATA

V_{BB} = 5 V; V_{GND} = 0 V; f = 1 kHz; T_{amb} = 25 °C; MUTETX = LOW; MUTERX = LOW; PD = LOW; R_{VOL} = 0 Ω; measured in test circuit of Fig.11; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{BB}	supply voltage		2.9	–	12.0	V
I_{BB}	current consumption from pin V_{BB}		–	2.7	3.8	mA
G_{vtx}	voltage gain from TXIN to TXOUT in transmit mode	V_{TXIN} = 1 mV (RMS); R_{GATX} = 30.1 kΩ	–	15.5	–	dB
ΔG_{vtxr}	voltage gain adjustment with R_{GATX}		−15.5	–	+24.5	dB
G_{vrx}	voltage gain from RXIN to RXOUT in receive mode	V_{RXIN} = 20 mV (RMS); R_{GARX} = 16.5 kΩ	–	6.5	–	dB
ΔG_{vrxr}	voltage gain adjustment with R_{GARX}		−20.5	–	+19.5	dB
SWRA	switching range		–	40	–	dB
ΔSWRA	switching range adjustment	with R_{SWR} referenced to R_{SWR} = 365 kΩ	−40	–	+12	dB
T_{amb}	operating ambient temperature		−25	–	+75	°C

BLOCK DIAGRAM

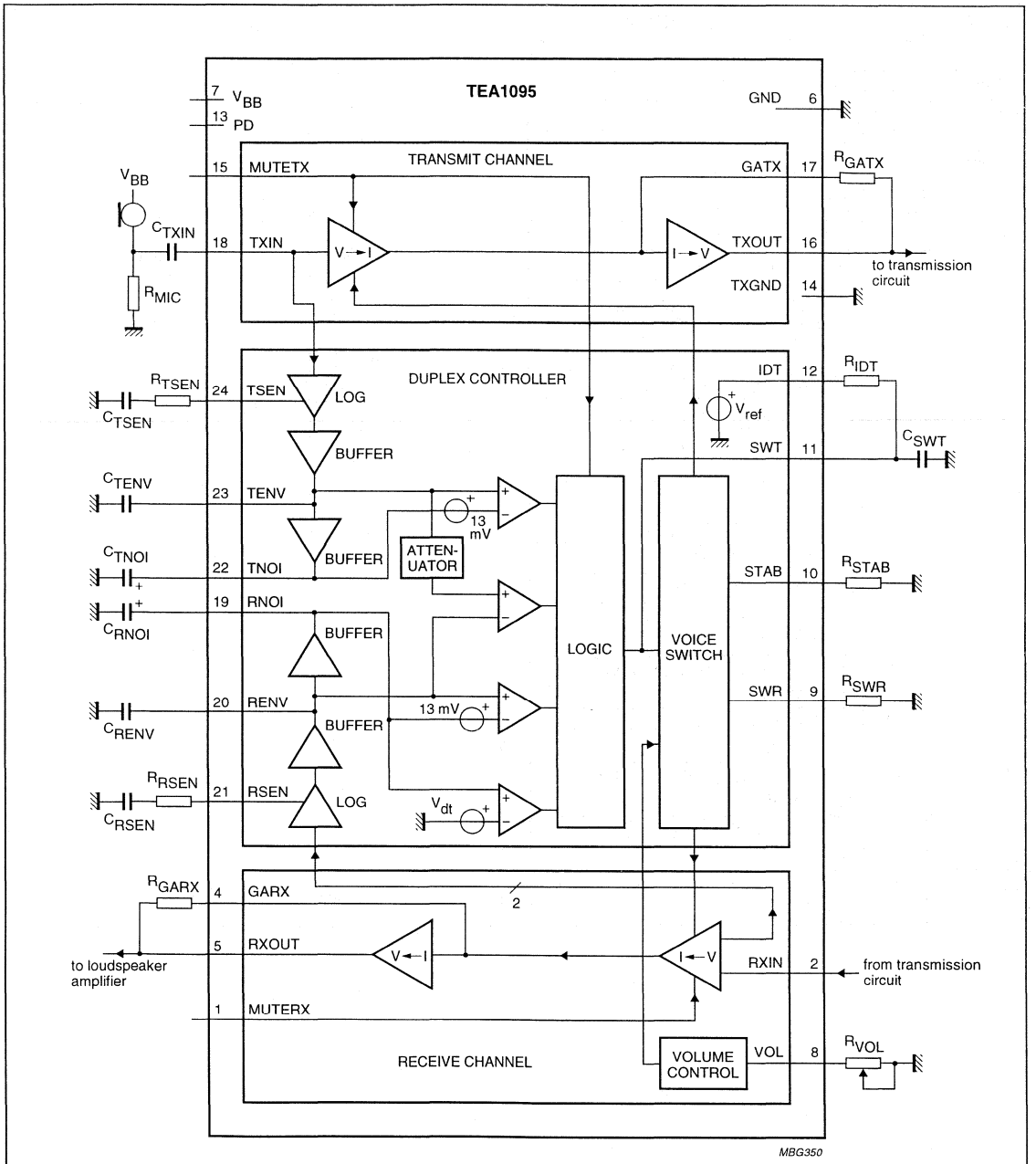


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
MUTERX	1	receiver channel mute input
RXIN	2	receiver amplifier input
n.c.	3	not connected
GARX	4	receiver gain adjustment
RXOUT	5	receiver amplifier output
GND	6	ground reference
V_{BB}	7	supply voltage input
VOL	8	receiver volume adjustment
SWR	9	switching range adjustment
STAB	10	reference current adjustment
SWT	11	switch-over timing adjustment
IDT	12	idle mode timing adjustment
PD	13	power-down input
TXGND	14	ground reference for the transmit channel
MUTETX	15	transmit channel mute input
TXOUT	16	transmit amplifier output
GATX	17	transmit gain adjustment
TXIN	18	transmit amplifier input
RNOI	19	receive noise envelope timing adjustment
RENV	20	receive signal envelope timing adjustment
RSEN	21	receive signal envelope sensitivity adjustment
TNOI	22	transmit noise envelope timing adjustment
TENV	23	transmit signal envelope timing adjustment
TSEN	24	transmit signal envelope sensitivity adjustment

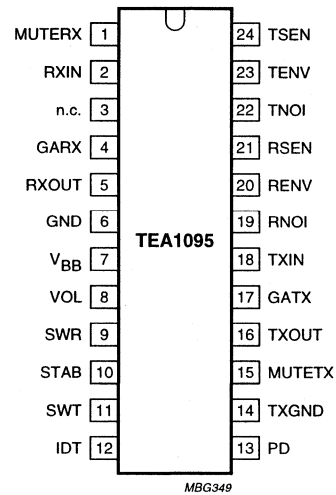


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The values given in the functional description are typical values except when otherwise specified.

A principle diagram of the TEA1096 is shown on the left side of Fig.3. The TEA1096 is a transmission and listening-in circuit. It incorporates a receiving amplifier for the earpiece, a transmit amplifier for the microphone, a loudspeaker amplifier and a hybrid. For more details on the TEA1096 circuit (please refer to *Data Handbook IC03*). The right side of Fig.3 shows a principle diagram of the TEA1095, a hands-free add-on circuit with a transmit amplifier, a receiver amplifier and a duplex controller.

As can be seen from Fig.3, a loop is formed via the sidetone network in the transmission circuit and the acoustic coupling between loudspeaker and microphone of the hands-free circuit. When this loop gain is greater than 1, howling is introduced. In a full duplex application, this would be the case. The loop-gain has to be much lower than 1 and therefore has to be decreased to avoid howling. This is achieved by the duplex controller. The duplex controller of the TEA1095 detects which channel has the 'largest' signal and then controls the gains of the transmit amplifier and the receiver amplifier such that the sum of the gains remains constant. As a result, the circuit can be in three stable modes:

1. Transmit mode (Tx mode): the gain of the transmit amplifier is at its maximum and the gain of the receiver amplifier is at its minimum.
2. Receive mode (Rx mode): the gain of the receiver amplifier is at its maximum and the gain of the transmit amplifier is at its minimum.
3. Idle mode: the gain of the amplifiers is halfway between their maximum and minimum value.

The difference between the maximum gain and minimum gain is called the switching range.

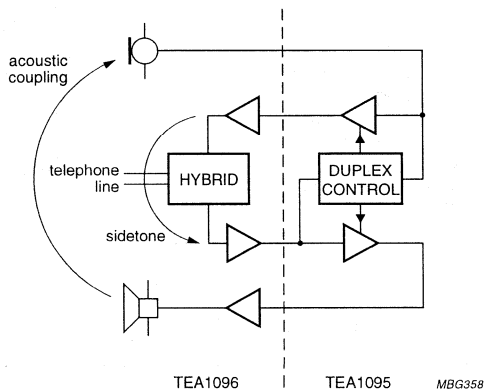


Fig.3 Hands-free telephone set principles.

Supply: pins V_{BB}, GND and PD

The TEA1095 must be supplied with an external stabilized voltage source between pins V_{BB} and GND. In idle mode, without any signal, the internal supply current is 2.7 mA at V_{BB} = 5 V.

To reduce current consumption during pulse dialling or register recall (flash), the TEA1095 is provided with a power-down (PD) input. When the voltage on PD is HIGH, the current consumption from V_{BB} is 140 μA.

Transmit channel: pins TXIN, GATX, TXOUT, TXGND and MUTETX

The TEA1095 has an asymmetrical transmit input (TXIN) with an input resistance of 20 kΩ. The gain of the input stage varies according to the mode of the TEA1095. In the transmit mode, the gain is at its maximum; in the receive mode, it is at its minimum and in the idle mode, it is halfway between maximum and minimum. Switch-over from one mode to the other is smooth and click-free. The output capability at pin TXOUT is 20 μA (RMS).

In the transmit mode, the overall gain of the transmit amplifier (from pin TXIN to TXOUT) can be adjusted from 0 dB to 40 dB to suit application specific requirements. The gain is proportional to the value of R_{GATX} and equals 15.5 dB with R_{GATX} = 30.1 kΩ.

A capacitor must be connected in parallel with R_{GATX} to ensure stability of the transmit amplifier. Together with R_{GATX}, it also provides a first-order low-pass filter.

By applying a HIGH level on pin MUTETX, the transmit amplifier is muted and the TEA1095 is automatically forced into the receive mode.

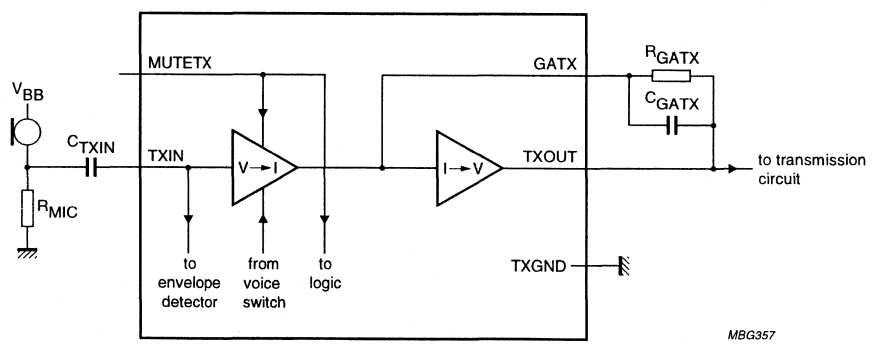


Fig.4 Transmit channel.

Receive channel

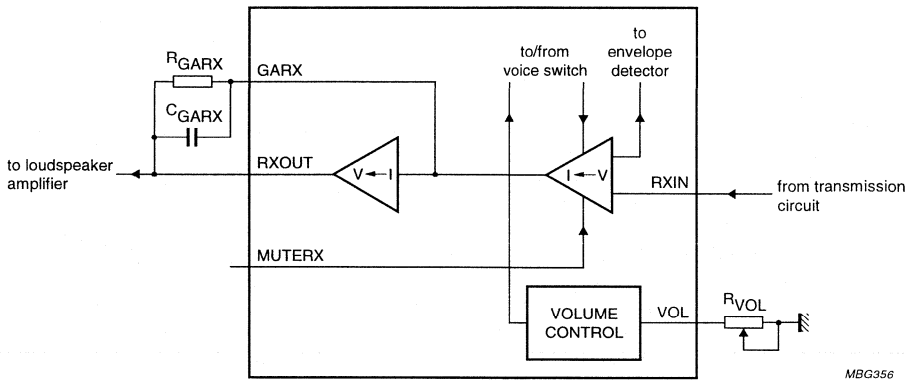


Fig.5 Receive channel.

RECEIVER AMPLIFIER: PINS RXIN, GARX, RXOUT AND MUTERX

The TEA1095 has an asymmetrical input (RXIN) for the receiver amplifier with an input resistance of 20 kΩ. The gain of the input stage varies according to the mode of the TEA1095. In the receive mode, the gain is at its maximum; in the transmit mode, it is at its minimum and in the idle mode, it is halfway between maximum and minimum. Switch-over from one mode to the other is smooth and click-free.

In the receive mode, the overall gain of the receive amplifier can be adjusted from −14 dB to +26 dB to suit application specific requirements. The gain from RXIN to RXOUT is proportional to the value of R_{GARX} and equals 6.5 dB with R_{GARX} = 16.5 kΩ. A capacitor connected in parallel with R_{GARX} can be used to provide a first-order low-pass filter.

By applying a HIGH level on pin MUTERX, the receiver amplifier is muted and the TEA1095 is automatically forced into the transmit mode.

VOLUME CONTROL: PIN VOL

The receiver amplifier gain can be adjusted with the potentiometer R_{VOL}. A linear potentiometer can be used to obtain logarithmic control of the gain of the receiver amplifier. Each 950 Ω increase of R_{VOL} results in a gain loss of 3 dB. The maximum gain reduction with the volume control is internally limited to the switching range.

Duplex controller

SIGNAL AND NOISE ENVELOPE DETECTORS: PINS TSEN, TENV, TNOI, RSEN, RENV AND RNOI

The signal envelopes are used to monitor the signal level strength in both channels. The noise envelopes are used to monitor background noise in both channels. The signal and noise envelopes provide inputs for the decision logic. The signal and noise envelopes detectors are shown in Fig.6.

For the transmit channel, the input signal at TXIN is 40 dB amplified to TSEN. For the receive channel, the input signal at RXIN is 0 dB amplified to RSEN. The signals from TSEN and RSEN are logarithmically compressed and buffered to TENV and RENV respectively. The sensitivity of the envelope detectors is set with R_{TSEN} and R_{RSEN}.

The capacitors connected in series with the two resistors block any DC component and form a first order high-pass filter. In the basic application (see Fig.12), it is assumed that V_{TXIN} = 1 mV (RMS) and V_{RXIN} = 100 mV (RMS) nominal and both R_{TSEN} and R_{RSEN} have a value of 10 kΩ. With the value of C_{TSEN} and C_{RSEN} at 100 nF, the cut-off frequency is at 160 Hz.

The buffer amplifiers leading the compressed signals to TENV and RENV have a maximum source current of 120 μA and a maximum sink current of 1 μA. Together with the capacitors C_{TENV} and C_{RENV}, the timing of the signal envelope monitors can be set. In the basic application, the value of both capacitors is 470 nF. Because of the logarithmic compression, each 6 dB signal increase means 18 mV increase of the voltage on the envelopes TENV or RENV at room temperature. Thus, timings can be expressed in dB/ms. At room temperature, the 120 μA sourced current corresponds to a maximum rise-slope of the signal envelope of 85 dB/ms. This is enough to track normal speech signals. The 1 μA current sunk by TENV or RENV corresponds to a maximum fall-slope of 0.7 dB/ms. This is enough for a smooth envelope and also eliminates the effect of echoes on switching behaviour.

To determine the noise level, the signal on TENV and RENV are buffered to TNOI and RNOI. These buffers have a maximum source current of 1 μA and a maximum sink current of 120 μA. Together with the capacitors C_{TNOI} and C_{RNOI}, the timing can be set. In the basic application of Fig.12, the value of both capacitors is 4.7 μF. At room temperature, the 1 μA sourced current corresponds to a maximum rise-slope of the noise envelope of approximately 0.07 dB/ms. This is small enough to track background noise and not to be influenced by speech bursts. The 120 μA current that is sunk corresponds to a maximum fall-slope of approximately 8.5 dB/ms. However, during the decrease of the signal envelope, the noise envelope tracks the signal envelope so it will never fall faster than approximately 0.7 dB/ms. The behaviour of the signal envelope and noise envelope monitors is illustrated in Fig.7.

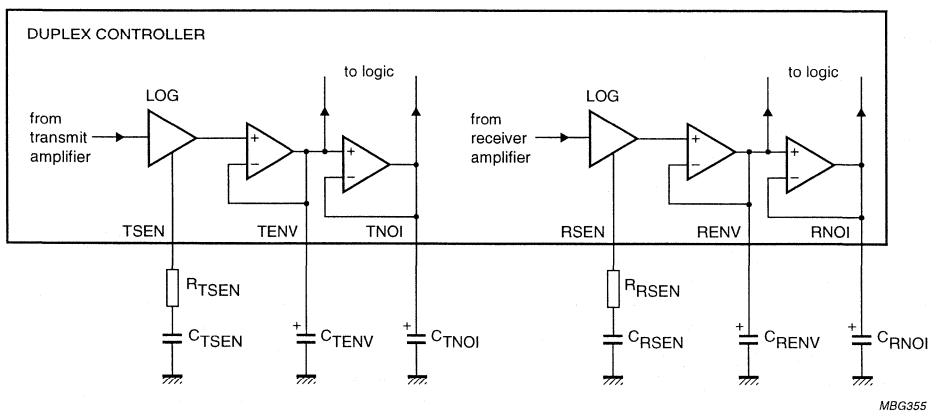


Fig.6 Signal and noise envelope detectors.

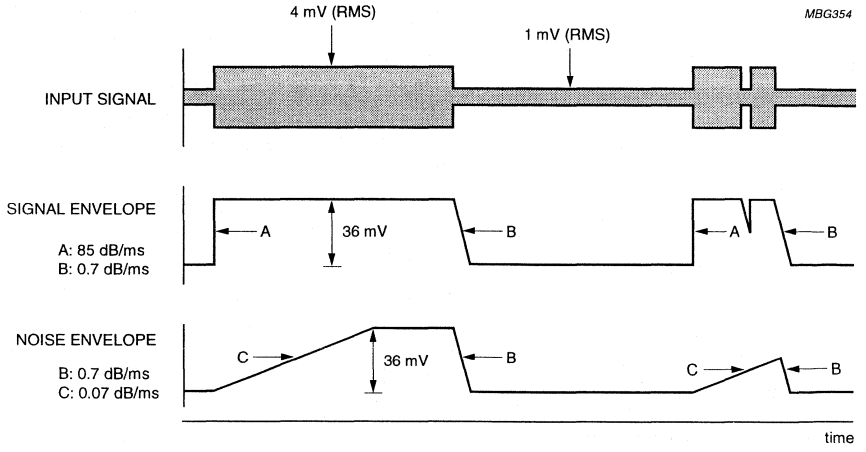
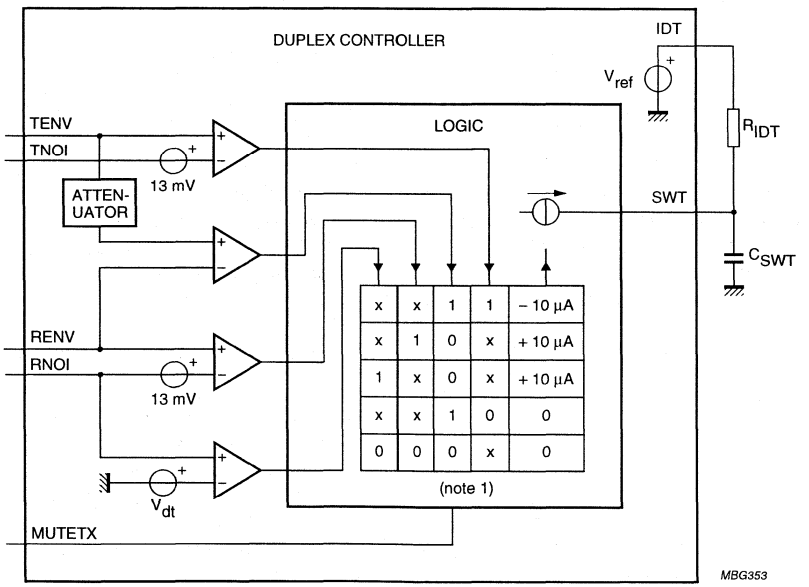


Fig.7 Signal and noise envelope waveforms.



(1) When MUTETX = HIGH +10 µA is forced. When MUTERX = HIGH −10 µA is forced.

Fig.8 Decision logic.

DECISION LOGIC: PINS IDT AND SWT

The TEA1095 selects its mode of operation (transmit, receive or idle mode) by comparing the signal and the noise envelopes of both channels. This is executed by the decision logic. The resulting voltage on pin SWT is the input for the voice-switch.

To facilitate the distinction between signal and noise, the signal is considered as speech when its envelope is more than 4.3 dB above the noise envelope. At room temperature, this is equal to a voltage difference $V_{ENV-NOI}$ = 13 mV. This so called speech/noise threshold is implemented in both channels.

The signal on TXIN contains both speech and the signal coming from the loudspeaker (acoustic coupling). When receiving, the contribution from the loudspeaker overrules the speech. As a result, the signal envelope on TENV is formed mainly by the loudspeaker signal. To correct this, an attenuator is connected between TENV and the TENV/RENV comparator. Its attenuation equals that applied to the transmit amplifier.

When a dial tone is present on the line, without monitoring, the tone would be recognized as noise because it is a signal with a constant amplitude. This would cause the TEA1095 to go into the idle mode and the user of the set would hear the dial tone fade away. To prevent this, a dial tone detector is incorporated which, in standard application, does not consider the input signals at RXIN as noise when they have a level greater than 42 mV (RMS). This level is proportional to R_{RSEN}.

As can be seen from Fig.8, the output of the decision logic is a current source. The logic table gives the relationship between the inputs and the value of the current source. It can charge or discharge the capacitor C_{SWT} with a current of 10 μA (switch-over). If the current is zero, the voltage on SWT becomes equal to the voltage on IDT via the high ohmic resistor R_{IDT} (idling). The resulting voltage difference between SWT and IDT determines the mode of the TEA1095 and can vary between −400 mV and +400 mV.

Table 1 Modes of TEA1095

$V_{SWT} - V_{IDT}$ (mV)	MODE
<−180	transmit mode
0	idle mode
>180	receive mode

The switch-over timing can be set with C_{SWT}, the idle mode timing with C_{SWT} and R_{IDT}. In the basic application given in Fig.12, C_{SWT} is chosen at 220 nF and R_{IDT} at 2.2 MΩ. This enables a switch-over time from transmit to receive mode or vice-versa of approximately 13 ms (580 mV swing on SWT). The switch-over time from idle mode to transmit mode or receive mode is approximately 4 ms (180 mV swing on SWT).

The switch-over time from receive mode or transmit mode to idle mode is equal to $4 \times R_{IDT}\ C_{SWT}$ and is approximately 2 s (idle mode time).

The inputs MUTETX and MUTERX overrule the decision logic. When MUTETX goes HIGH, the capacitor C_{SWT} is charged with 10 μA resulting in the receive mode. When the voltage on pin MUTERX goes HIGH, the capacitor C_{SWT} is discharged with 10 μA resulting in the transmit mode.

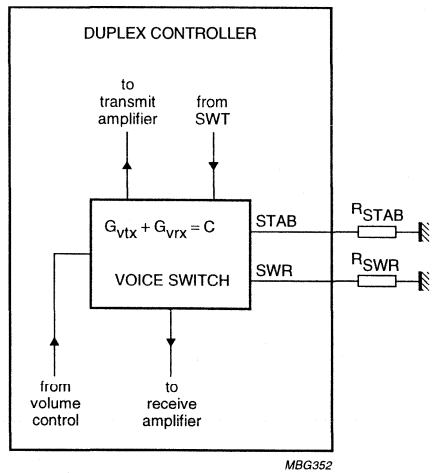
VOICE-SWITCH: PINS STAB AND SWR

A diagram of the voice-switch is illustrated in Fig.9. With the voltage on SWT, the TEA1095 voice-switch regulates the gains of the transmit and the receive channel such that the sum of both is kept constant.

In the transmit mode, the gain of the transmit amplifier is at its maximum and the gain of the receive amplifier is at its minimum. In the receive mode, the opposite applies. In the idle mode, both transmit and receive amplifier gains are halfway.

The difference between maximum and minimum is the so called switching range. This range is determined by the ratio of R_{SWR} and R_{STAB} and is adjustable between 0 and 52 dB. R_{STAB} should be equal to 3.65 kΩ and sets an internally used reference current. In the basic application diagram given in Fig.12, R_{SWR} is equal to 365 kΩ which results in a switching range of 40 dB. The switch-over behaviour is illustrated in Fig.10.

In the receive mode, the gain of the receive amplifier can be reduced using the volume control. Since the voice-switch keeps the sum of the gains constant, the gain of the transmit amplifier is increased at the same time (see dashed curves in Fig.10). In the transmit mode however, the volume control has no influence on the gain of the transmit amplifier or the gain of the receive amplifier. Consequently, the switching range is reduced when the volume is reduced. At maximum reduction of volume, the switching range becomes 0 dB.



Where C = constant.

Fig.9 Voice switch.

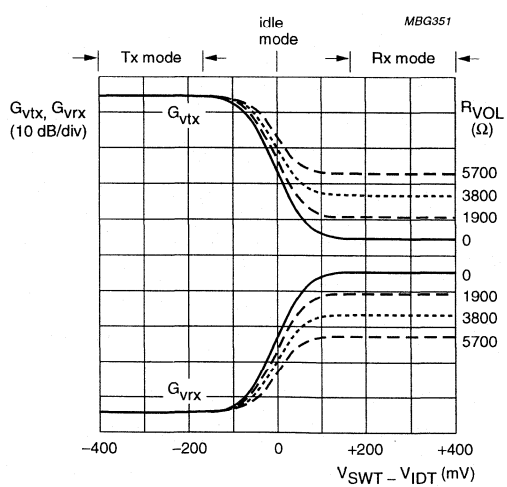


Fig.10 Switch-over behaviour.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{n(max)}$	maximum voltage on all pins; except pins V_{BB} and RXIN		V_{GND} – 0.4	V_{BB} + 0.4	V
$V_{RIN(max)}$	maximum voltage on pin RXIN		V_{GND} – 1.2	V_{BB} + 0.4	V
$V_{BB(max)}$	maximum voltage on pin V_{BB}		V_{GND} – 0.4	12.0	V
T_{stg}	IC storage temperature		–40	+125	°C
T_{amb}	operating ambient temperature		–25	+75	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	TEA1095	50	K/W
	TEA1095T	75	K/W
	TEA1095TS	104	K/W

CHARACTERISTICS

V_{BB} = 5 V; V_{GND} = 0 V; f = 1 kHz; T_{amb} = 25 °C; MUTETX = LOW; MUTERX = LOW; PD = LOW; R_{VOL} = 0 Ω; measured in test circuit of Fig.11; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (V_{BB}, PD and GND)						
V_{BB}	supply voltage		2.9	–	12.0	V
I_{BB}	current consumption from pin V_{BB}		–	2.7	3.8	mA
POWER-DOWN INPUT PD						
V_{IL}	LOW level input voltage		V_{GND} – 0.4	–	0.3	V
V_{IH}	HIGH level input voltage		1.5	–	V_{BB} + 0.4	V
I_{PD}	power-down input current	PD = HIGH	–	2.5	5	µA
$I_{BB(PD)}$	current consumption from pin V_{BB} in power-down mode	PD = HIGH	–	140	190	µA
Transmit channel (TXIN, GATX, TXOUT, MUTETX and TXGND)						
TRANSMIT AMPLIFIER						
$\lvert Z_i \rvert$	input impedance between pins TXIN and TXGND		17	20	23	kΩ
G_{vtx}	voltage gain from TXIN to TXOUT in transmit mode	V_{TXIN} = 1 mV (RMS); R_{GATX} = 30.1 kΩ	–	15.5	–	dB
ΔG_{vtxr}	voltage gain adjustment with R_{GATX}		–15.5	–	+24.5	dB
ΔG_{vtxT}	voltage gain variation with temperature referenced to 25 °C	V_{TXIN} = 1 mV (RMS); T_{amb} = –25 to +75 °C	–	±0.3	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ΔG_{vtxf}	voltage gain variation with frequency referenced to 1 kHz	V_{TXIN} = 1 mV (RMS); f = 300 to 3400 Hz	–	±0.3	–	dB
V_{notx}	noise output voltage at pin TXOUT	pin TXIN connected to TXGND through 200 Ω in series with 10 μF; psophometrically weighted (P53 curve)	–	−100	–	dBmp
TRANSMIT MUTE INPUT MUTETX						
V_{IL}	LOW level input voltage		V_{GND} − 0.4	–	0.3	V
V_{IH}	HIGH level input voltage		1.5	–	V_{BB} + 0.4	V
I_{MUTETX}	input current	MUTETX = HIGH	–	2.5	5	μA
ΔG_{vtxm}	voltage gain reduction with MUTETX active	MUTETX = HIGH	–	80	–	dB
Receive channel (RXIN, GARX, RXOUT and MUTERX)						
RECEIVE AMPLIFIER						
$\|Z_i\|$	input impedance between pins RXIN and GND		17	20	23	kΩ
G_{vrx}	voltage gain from RXIN to RXOUT in receive mode	V_{RXIN} = 20 mV (RMS); R_{GARX} = 16.5 kΩ	–	6.5	–	dB
ΔG_{vrxr}	voltage gain adjustment with R_{GARX}		−20.5	–	+19.5	dB
ΔG_{vrxT}	voltage gain variation with temperature referenced to 25 °C	V_{RXIN} = 20 mV (RMS); T_{amb} = −25 to +75 °C	–	±0.3	–	dB
ΔG_{vrxf}	voltage gain variation with frequency referenced to 1 kHz	V_{RXIN} = 20 mV (RMS); f_i = 300 to 3400 Hz	–	±0.3	–	dB
$V_{norx(rms)}$	noise output voltage at pin RXOUT (RMS value)	input RXIN short-circuited through 200 Ω in series with 10 μF; psophometrically weighted (P53 curve)	–	20	–	μV
ΔG_{vrxv}	voltage gain variation referenced to ΔR_{VOL} = 950 Ω	when total attenuation does not exceed the switching range	–	3	–	dB
RECEIVE MUTE INPUT MUTERX						
V_{IL}	LOW level input voltage		V_{GND} − 0.4	–	0.3	V
V_{IH}	HIGH level input voltage		1.5	–	V_{BB} + 0.4	V
I_{MUTERX}	input current	MUTERX = HIGH	–	2.5	5	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ΔG_{vrxm}	gain reduction with MUTERX active	MUTERX = HIGH	–	80	–	dB
Envelope and noise detectors (TSEN, TENV, TNOI, RSEN, RENV and RNOI)						
PREAMPLIFIERS						
$G_{v(TSEN)}$	voltage gain from TXIN to TSEN		–	40	–	dB
$G_{v(RSEN)}$	voltage gain between RXIN to RSEN		–	0	–	dB
LOGARITHMIC COMPRESSOR AND SENSITIVITY ADJUSTMENT						
$\varphi_{det(TSEN)}$	sensitivity detection on pin TSEN; voltage change on pin TENV when doubling the current from TSEN	I_{TSEN} = 0.8 to 160 μA	–	18	–	mV
$\varphi_{det(RSEN)}$	sensitivity detection on pin RSEN; voltage change on pin RENV when doubling the current from RSEN	I_{RSEN} = 0.8 to 160 μA	–	18	–	mV
SIGNAL ENVELOPE DETECTORS						
$I_{source(ENV)}$	maximum current sourced from pin TENV or RENV		–	120	–	μA
$I_{sink(ENV)}$	maximum current sunk by pin TENV or RENV		0.75	1	1.25	μA
ΔV_{ENV}	voltage difference between pins RENV and TENV	when 10 μA is sourced from both RSEN and TSEN; envelope detectors tracking; note 1	–	±3	–	mV
NOISE ENVELOPE DETECTORS						
$I_{source(NOI)}$	maximum current sourced from pins TNOI or RNOI		0.75	1	1.25	μA
$I_{sink(NOI)}$	maximum current sunk by pins TNOI or RNOI		–	120	–	μA
ΔV_{NOI}	voltage difference between pins RNOI and TNOI	when 2 μA is sourced from both RSEN and TSEN; noise detectors tracking; note 1	–	±3	–	mV
DIAL TONE DETECTOR						
$V_{RINDT(rms)}$	threshold level at pin RXIN (RMS value)		–	42	–	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Decision logic (IDT and SWT)						
SIGNAL RECOGNITION						
$\Delta V_{Srx(th)}$	threshold voltage between pins RENV and RNOI to switch-over from receive to idle mode	$V_{RXIN} < V_{RINDT}$; note 2	–	13	–	mV
$\Delta V_{Stx(th)}$	threshold voltage between pins TENV and TNOI to switch-over from transmit to idle mode	note 2	–	13	–	mV
SWITCH-OVER						
$I_{source(SWT)}$	current sourced from pin SWT when switching to receive mode		7.5	10	12.5	μA
$I_{sink(SWT)}$	current sunk by pin SWT when switching to transmit mode		7.5	10	12.5	μA
$I_{idle(SWT)}$	current sourced from pin SWT in idle mode		–	0	–	μA
Voice switch (STAB and SWR)						
SWRA	switching range		–	40	–	dB
ΔSWRA	switching range adjustment	with R_{SWR} referenced to R_{SWR} = 365 kΩ	–40	–	+12	dB
$\lvert\Delta G_v\rvert$	voltage gain variation from transmit mode to idle mode on both channels		–	20	–	dB
G_{tr}	gain tracking (G_{vtx} + G_{vrx}) during switching, referenced to idle mode		–	±0.5	–	dB

Notes

1. Corresponds to ±1 dB tracking.
2. Corresponds to 4.3 dB noise/speech recognition level.

TEST AND APPLICATION INFORMATION

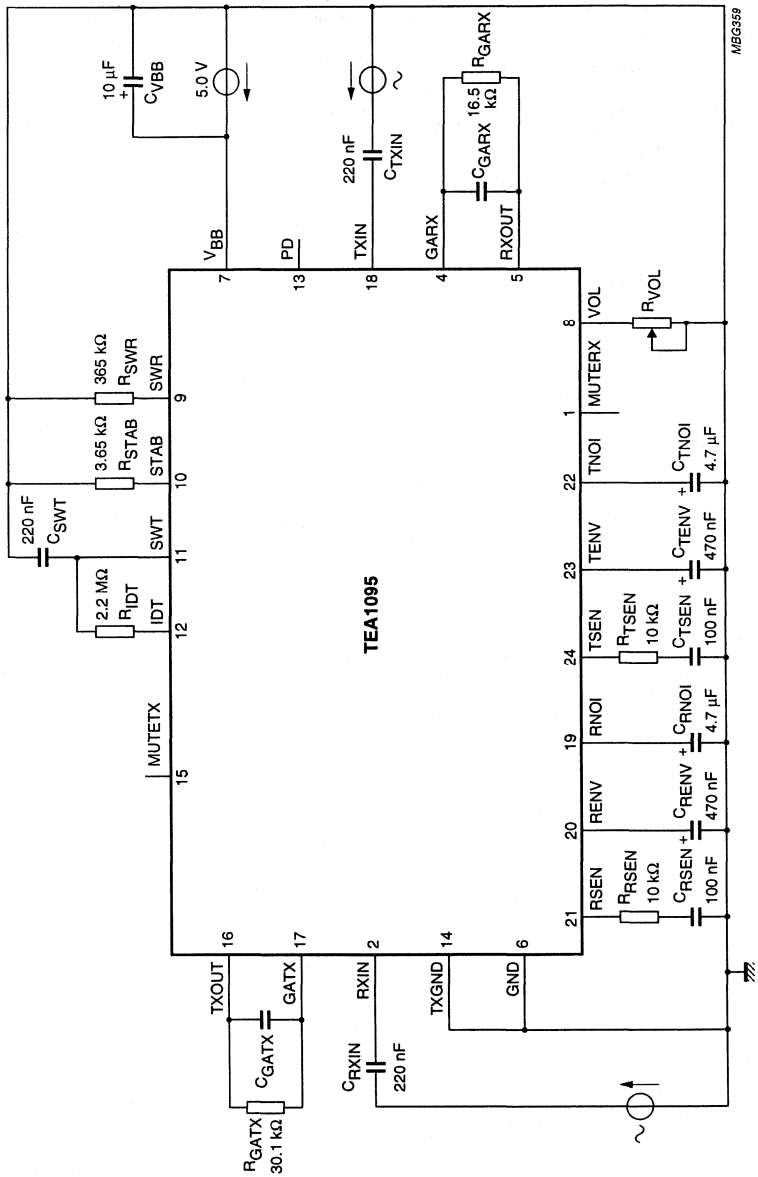


Fig.11 Test circuit.

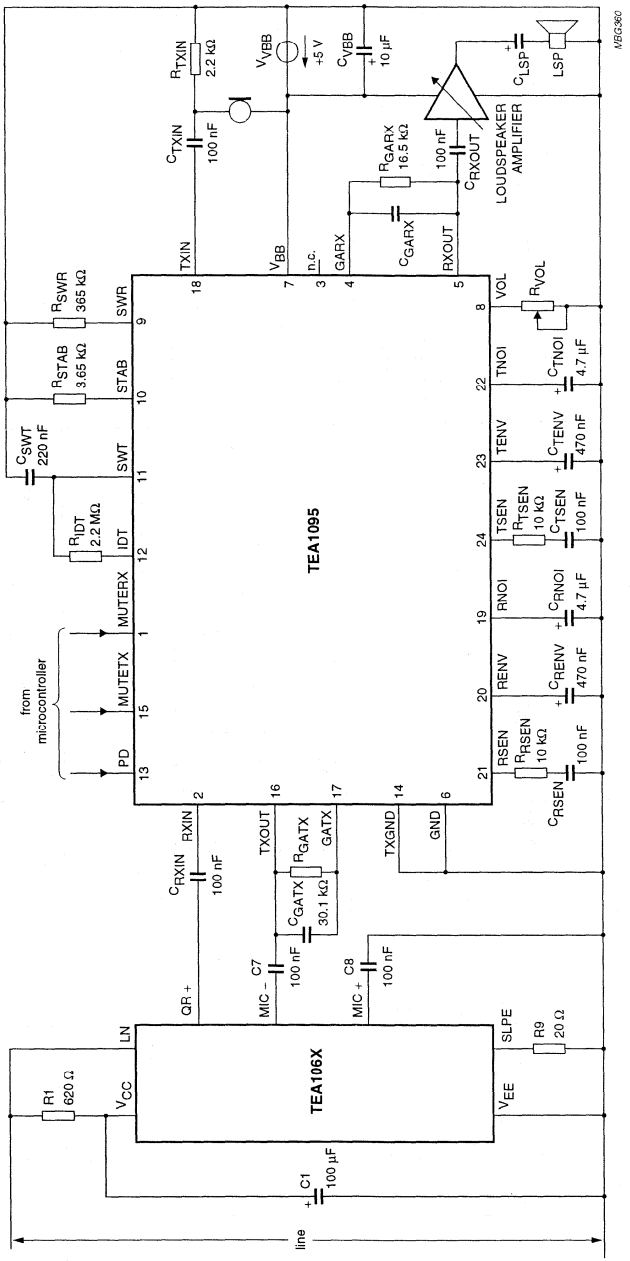
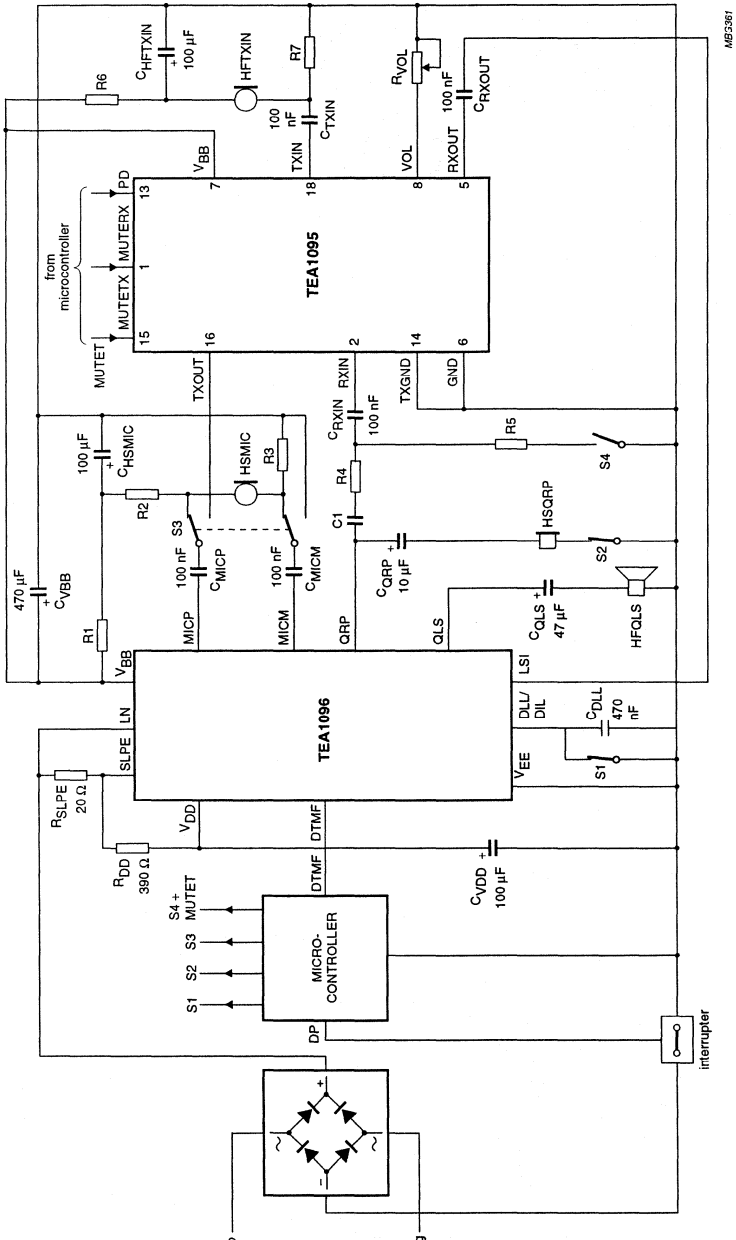


Fig.12 Basic application diagram.



MODE	SWITCH				MUTET
	S1	S2	S3	S4	
Hands-free	OPEN	OPEN	TXOUT	OPEN	LOW
Handset	CLOSED	CLOSED	HSMIC	OPEN	DON'T CARE
Handset plus listening-in	OPEN	CLOSED	HSMIC	CLOSED	HIGH

Fig.13 Application example.

Speech and Handsfree IC with auxiliary inputs/outputs and analog multiplexer

TEA1099H

FEATURES

Line interface

- Low DC line voltage
- Voltage regulator with adjustable DC voltage
- Symmetrical high impedance inputs (70 kΩ) for dynamic, magnetic or electret microphones
- DTMF input with confidence tone on earphone and/or loudspeaker
- Receive amplifier for dynamic, magnetic or piezo-electric earpieces (with externally adjustable gain)
- AGC: automatic gain control for true line loss compensation.

Supplies

- Provides a strong 3.3 V regulated supply for micro-controller or dialler
- Provides filtered power supply, optimized according to line current and compatible with external voltage or current sources
- Filtered 2 V power supply output for electret microphone
- Compatible with a ringer mode
- $\overline{PD}$ logic input for power down.

Handsfree

- Asymmetrical high input impedance for electret microphone
- Loudspeaker amplifier with single-ended rail-to-rail output and externally adjustable gain
- Dynamic limiter on loudspeaker amplifier to prevent distortion
- Logarithmic volume control on loudspeaker amplifier via linear potentiometer
- Duplex controller consisting of:
  - signal and noise envelope monitors for both channels (with adjustable sensitivities and timing)
  - decision logic (with adjustable switch-over and idle-mode timing)
  - voice switch control (with adjustable switching range and constant sum of gain during switching).

Auxiliary interfaces

- General auxiliary output for transmit and receive purposes
- Auxiliary transmit input with high signal level capability dedicated to line transmission
- Auxiliary receive input with high signal level capability
- Integrated multiplexer for channels selection.

APPLICATIONS

- Line powered telephone sets
- Cordless telephones
- Fax machines
- Answering machines.

GENERAL DESCRIPTION

The TEA1099H is an analog bipolar circuit dedicated for telephony applications. It includes a line interface, handset (HS) microphone and earpiece amplifiers, hands-free (HF) microphone and loudspeaker amplifiers, some specific auxiliary inputs/outputs (I/O's) and an analog multiplexer to enable the right transmit and/or receive channels. The multiplexer is controlled by a logic circuitry decoding four logic inputs provided by a micro-controller. Thirteen different application modes have been defined and can be accessed by selecting the right logic inputs. An application mode is a special combination of transmit and receive channels required by telephony applications.

This IC can be supplied by the line and/or by the mains if available (in a cordless telephone or an answering machine for example). It provides a 3.3 V supply for a micro-controller and a 2 V filtered voltage supply for an electret microphone. The IC is designed to facilitate the use of the loudspeaker amplifier during ringing phase.

QUICK REFERENCE DATA

I_{line} = 15 mA; R_{slpe} = 20 Ω; Z_{line} = 600 Ω; f = 1 kHz; T_{amb} = 25 °C; AGC pin connected to LN; $\overline{PD}$ = HIGH; HFC = LOW; AUXC = LOW; $\overline{MUTT}$ = HIGH; $\overline{MUTR}$ = HIGH; measured according to test circuits; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{line}	line current operating range	normal operation	11	–	140	mA
		with reduced performance	1	–	11	mA
V_{SLPE}	stabilized voltage between SLPE and GND	I_{line} = 15 mA	tbf	3.5	tbf	V
		I_{line} = 70 mA	tbf	5.9	tbf	V
V_{BB}	regulated supply voltage for internal circuitry	I_{line} = 15 mA	tbf	3.0	tbf	V
		I_{line} = 70mA	tbf	5.3	tbf	V
V_{DD}	regulated supply voltage on pin V_{DD}	V_{BB} > 3.3 V + 0.25 V (typ.)	–	3.3	3.6	V
		otherwise	–	V_{BB} – 0.25	–	V
V_{ESI}	external voltage supply allowed on pin ESI		–	–	5.5	V
I_{ESI}	external current supply allowed on pin ESI		–	–	140	mA
I_{BB}	current available on pin V_{BB}					
	in speech mode		–	11.5	–	mA
	in handsfree mode		–	9	–	mA
$I_{BB(PD)}$	current consumption on V_{BB} during power down phase	$\overline{PD}$ = LOW; AUXC = LOW	–	500	–	µA
$G_{v(MIC-LN)}$	voltage gain from pin MIC+/MIC– to LN	V_{MIC} = 4 mV (RMS)	tbf	44	tbf	dB
$G_{v(IR-RECO)}$	voltage gain from pin IR (referred to LN) to RECO	V_{IR} = 4 mV (RMS)	tbf	29	tbf	dB
$\Delta G_{v(QR)}$	gain voltage range between pins RECO and QR		–3	–	+15	dB
$G_{v(TXIN-TXOUT)}$	voltage gain from pin TXIN to TXOUT	V_{TXIN} = 4 mV (RMS); R_{GATX} = 30.1 kΩ	–	15	–	dB
$G_{v(HFTX-LN)}$	voltage gain from pin HFTX to LN	V_{HFTX} = 10 mV (RMS)	–	34	–	dB
$G_{v(HFRX-LSAO)}$	voltage gain from pin HFRX to LSAO	V_{HFRX} = 30 mV(RMS); R_{GALS} = 255 kΩ	–	28	–	dB
SWRA	switching range		–	40	–	dB
ΔSWRA	switching range adjustment	with R_{SWR} referred to 365 kΩ	–40	–	+12	dB
$\Delta G_{v(trx)}$	gain control range for transmit and receive amplifiers affected by the AGC; with respect to I_{line} = 15 mA	I_{line} = 70 mA	–	6.5	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA1099H	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body $10 \times 10 \times 1.75$ mm	SOT307-2

BLOCK DIAGRAM

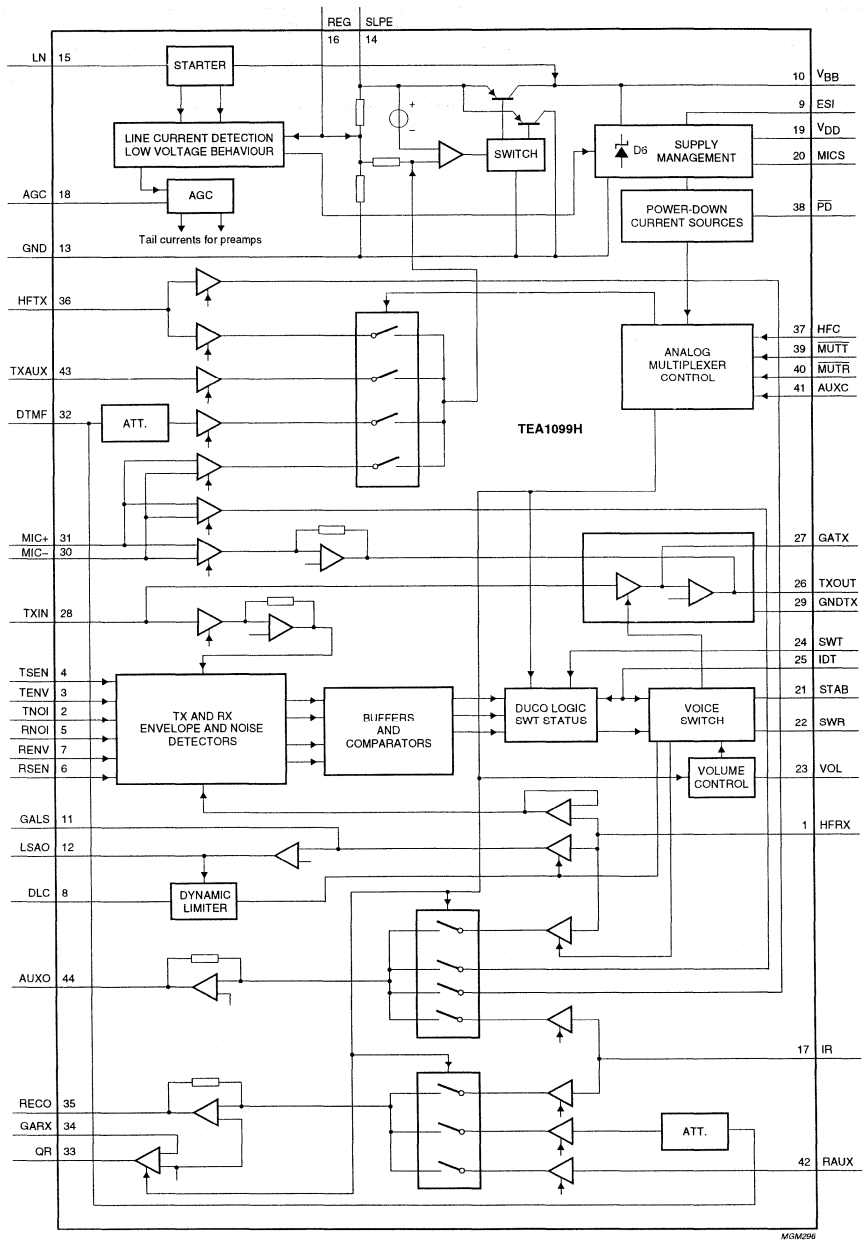


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
HFRX	1	receive input for loudspeaker amplifier or auxiliary receive amplifier
TNOI	2	transmit noise envelope timing adjustment
TENV	3	transmit signal envelope timing adjustment
TSEN	4	transmit signal envelope sensitivity adjustment
RNOI	5	receive noise envelope timing adjustment
RSEN	6	receive signal envelope sensitivity adjustment
RENV	7	receive signal envelope timing adjustment
DLC	8	dynamic limiter capacitor for the loudspeaker amplifier
ESI	9	external supply input
V_{BB}	10	stabilized supply for internal circuitry
GALS	11	loudspeaker amplifier gain adjustment
LSAO	12	loudspeaker amplifier output
GND	13	ground reference
SLPE	14	line current sense
LN	15	positive line terminal
REG	16	line voltage regulator decoupling
IR	17	receive amplifier input
AGC	18	automatic gain control / line loss compensation
V_{DD}	19	3.3 V regulated voltage supply for microcontrollers
MICS	20	microphone supply
STAB	21	reference current adjustment
SWR	22	switching range adjustment
VOL	23	loudspeaker volume adjustment
SWT	24	switch-over timing adjustment
IDT	25	idle mode timing adjustment
TXOUT	26	HF microphone amplifier output
GATX	27	HF microphone amplifier gain adjustment
TXIN	28	HF microphone amplifier input
GNDTX	29	ground reference for microphone amplifiers
MIC–	30	negative HS microphone amplifier input
MIC+	31	positive HS microphone amplifier input
DTMF	32	dual tone multi-frequency input
QR	33	earpiece amplifier output
GARX	34	earpiece amplifier gain adjustment
RECO	35	receive amplifier output
HFTX	36	transmit input for line amplifier or auxiliary receive amplifier
HFC	37	logic input
$\overline{PD}$	38	power-down input
$\overline{MUTT}$	39	logic input
$\overline{MUTR}$	40	logic input

SYMBOL	PIN	DESCRIPTION
AUXC	41	logic input
RAUX	42	auxiliary receive amplifier input
TXAUX	43	auxiliary transmit amplifier input
AUXO	44	auxiliary amplifier output

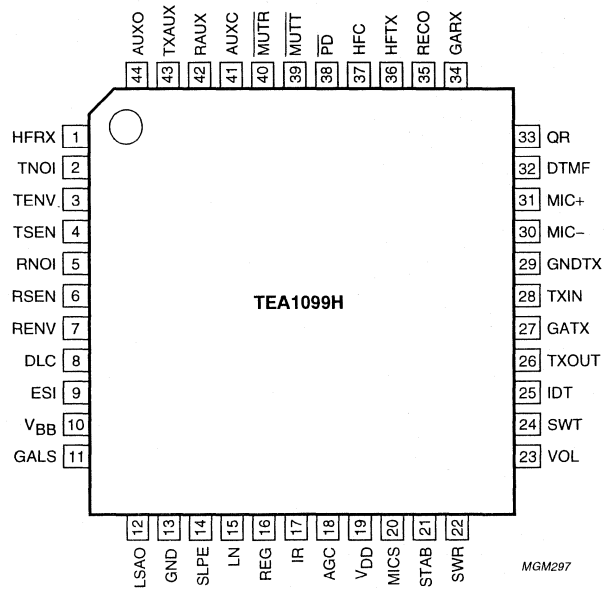


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

All data given in this chapter are typical values, except when otherwise specified.

Supplies

LINE INTERFACE AND INTERNAL SUPPLY (PINS LN, SLPE, REG AND V_{BB})

The supply for the TEA1099H and its peripherals is obtained from the line. The IC generates a stabilized reference voltage (V_{ref}) between pins SLPE and GND. This reference voltage is equal to 3.5 V for line currents lower than 18 mA. It than increases linearly with the line current and reaches the value of 5.9 V for line currents higher than 45 mA. For line currents below 9 mA, the internal reference voltage generating V_{ref} is automatically adjusted to a lower value. This is the

so-called low voltage area and the TEA1099H has limited performances in this area (see "Low voltage behaviour" section). This reference voltage is temperature compensated.

The voltage between pins SLPE and REG is used by the internal regulator to generate the stabilized reference voltage and is decoupled by means of a capacitor between pins LN and REG. This capacitor converted into an equivalent inductance realizes the set impedance conversion from its DC value (R_{SLPE}) to its AC value (done by an external impedance).

The IC regulates the line voltage at pin LN and it can be calculated as follows:

$$V_{LN} = V_{ref} + R_{SLPE} \times I_{SLPE}$$

$$I_{SLPE} = I_{line} - I^{x}$$

where:

I_{line} = line current

I^{x} = current consumed on pin LN (approximately a few µA)

I_{SLPE} = current flowing through the R_{SLPE} resistor

The preferred value for R_{SLPE} is 20 Ω. Changing this value will affect more than the DC characteristics; it also influences the transmit gains to the line, the gain control characteristic, the sidetone level and the maximum output swing on the line.

As can be seen from Fig.3, the internal circuitry is supplied by pin V_{BB}, which is a strong supply point combined with the line interface. The line current is flowing through the R_{SLPE} resistor and is sunk by the V_{BB} voltage stabilizer, becoming available for a loudspeaker amplifier or any peripheral IC. Its voltage is equal to 3.0 V for line currents lower than18 mA. It than increases linearly with the line current and reaches the value of 5.3 V for line currents greater than 45 mA. It is temperature compensated.

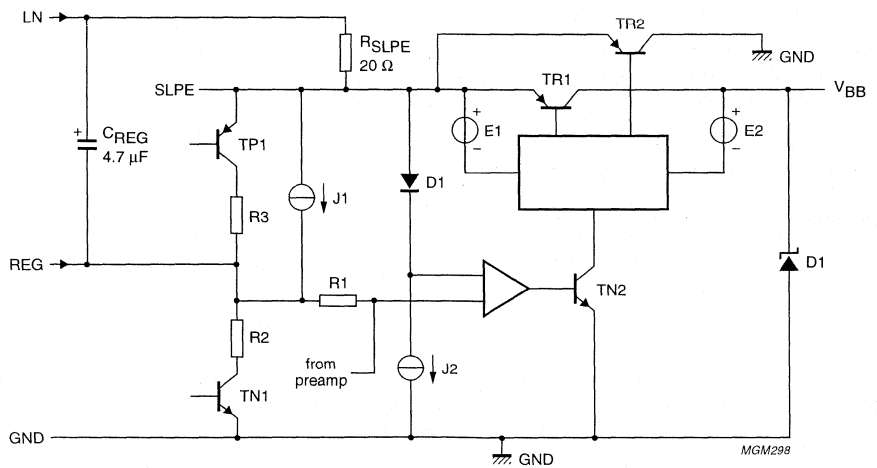


Fig.3 Line interface principle.

The aim of the current switch TR1-TR2 is to reduce distortion of large AC line signals. Current I_{SLPE} is supplied to V_{BB} via TR1 when the voltage on SLPE is greater than V_{BB} + 0.25 V. When the voltage on SLPE is lower than this value, the current I_{SLPE} is shunted to GND via TR2.

The reference voltage V_{ref} can be increased by connecting an external resistor between pins REG and SLPE. For large line currents, this increase can slightly affect some dynamic performances such as maximum signal level on the line for 2 % THD. The voltage on pin V_{BB} is not affected by this external resistor.

External supply (pins ESI and V_{BB})

The TEA1099H can be supplied by the line as well as by external power sources (voltage or current sources) that must be connected at pin ESI.

The IC will choose which supply to use according to the voltage it can provide. A voltage supply on ESI is efficient only if its value is greater than the working voltage of the internal V_{BB} voltage stabilizer. Otherwise the IC continues to be line powered. The current consumed on this source is at least equal to the internal consumption. It depends on the voltage difference between the value forced on ESI and the working voltage of the internal stabilizer. The current required increases with the voltage difference to manage. The excess current compared to the internal consumption becomes then available for other purposes such as supplying a loudspeaker amplifier. The voltage source should not exceed 5.5 V. If the value of the external voltage source can be lower than the working voltage of the internal stabilizer, an external diode is required to avoid reverse current flowing into the external power supply.

In case of current source, the voltage on V_{BB} and ESI depends on the current available. It is internally limited to 6 V. The current source should not exceed 140 mA.

Ringer mode (pins ESI, V_{BB}, AUXC and $\overline{PD}$)

The TEA1099H is designed to be activated during the ringing phase. The loudspeaker amplifier can be used for the ringing signal. The IC must be powered by an external supply on ESI, while applying a 'high' level on the logic input AUXC and a 'low' level on $\overline{PD}$ input. Only the HFRX input and the LSAO output are activated, in order to limit the current consumption. Some dynamic limitation is provided to prevent V_{BB} from being discharged below 2.7 V.

V_{DD} supply for micro-controller (pin V_{DD})

The voltage on V_{DD} supply point follows the voltage on V_{BB} with a difference typically equal to 200 mV and is internally limited to 3.3 V. This voltage is temperature compensated. This supply point can provide a current up to 2 mA typically. Its internal consumption stays low (a few 10 nA) as long as V_{DD} does not exceed 1.5 V.

An external voltage can be connected on V_{DD} with limited extra consumption on V_{DD} (typically 120 µA). This voltage source should not be lower than 3.5 V and higher than 5.5 V.

Supply for microphone (pins MICS and GNDTX)

The MICS output can be used as a supply for an electret microphone. Its voltage is equal to 2 V; it can source current up to 1 mA and has an output impedance equal to 200 Ω.

Low voltage behaviour

For line currents below 9 mA, the reference voltage is automatically adjusted to a lower value; the V_{BB} voltage follows the SLPE voltage with 250 mV difference. The excess current available for other purposes than DC biasing of the IC becomes small. In this low voltage area, the IC has limited performances.

When the V_{BB} voltage reaches 2.7 V, the V_{BB} detector of the receive dynamic limiter on LSAO acts continuously, discharging the DLC capacitor. In DC condition, the loudspeaker is then automatically disabled below this voltage.

When V_{BB} reaches 2.5 V, the TEA1099H is forced in a low voltage mode whatever the levels on the logic inputs are. It is a speech mode with reduced performances only enabling the microphone channel (between the MIC inputs and LN) and the earpiece amplifier. These two channels are able to deliver signals for line currents as small as 2 mA.

POWER-DOWN MODE (PINS $\overline{PD}$ AND AUXC)

To reduce consumption during dialling or register recall (flash), the TEA1099H is provided with a power-down input ($\overline{PD}$). When the voltage on both pins $\overline{PD}$ and AUXC is LOW, the current consumption from V_{BB} and V_{DD} is reduced to 500 µA. Therefore a capacitor of 470 µF on V_{BB} is sufficient to power the TEA1099H during pulse dialling or flash. The $\overline{PD}$ input has a pull-up structure, while AUXC has a pull-down structure. In this mode, the capacitor C_{REG} is internally disconnected.

Transmit channels (pins MIC+, MIC–, DTMF, TXAUX, HFTX and LN)

HANDSET MICROPHONE AMPLIFIER (PINS MIC+, MIC– AND LN)

The TEA1099H has symmetrical microphone inputs. The input impedance between MIC+ and MIC– is typically equal to 70 kΩ. The voltage gain between pins MIC+/MIC– and LN is set to 44 dB. Without limitation from the output, the microphone input stage can accommodate signals up to 18 mV (RMS) at room temperature for 2% of total harmonic distortion (THD). The microphone inputs are biased at one diode voltage.

Automatic gain control is provided for line loss compensation.

DTMF AMPLIFIER (PINS DTMF, LN AND RECO)

The TEA1099H has an asymmetrical DTMF input. The input impedance between DTMF and GND is typically equal to 20 kΩ. The voltage gain between pins DTMF and LN is set to 25.5 dB. Without limitation from the output, the input stage can accommodate signals up to 180 mV (RMS) at room temperature for 2% of total harmonic distortion (THD).

When the DTMF amplifier is enabled, dialling tones may be sent on the line. These tones can be heard in the earpiece or in the loudspeaker at a low level. This is called the confidence tone. The voltage attenuation between pins DTMF and RECO is typically equal to –17 dB.

The DC biasing of this input is 0 V.

The automatic gain control has no effect on these channels.

AUXILIARY TRANSMIT AMPLIFIER (PINS TXAUX AND LN)

The TEA1099H has an asymmetrical auxiliary input TXAUX. The input impedance between TXAUX and GND is typically equal to 20 kΩ. The voltage gain between pins TXAUX and LN is set to 12 dB. Without limitation from the output, the input stage can accommodate signals up to 0.9 V (RMS) at room temperature for 2% of total harmonic distortion (THD). The TXAUX input is biased at two diodes voltage.

Automatic gain control is provided for line loss compensation.

HANDS-FREE TRANSMIT OUTPUT STAGE (PINS HFTX AND LN)

The TEA1099H has an asymmetrical HFTX input, which is mainly intended for use in combination with the TXOUT output. The input impedance between HFTX and GND is typically equal to 20 kΩ. The voltage gain between pins HFTX and LN is set to 34 dB. Without limitation from the output, the input stage can accommodate signals up to 75 mV (RMS) at room temperature for 2% of total harmonic distortion (THD). The HFTX input is biased at two diodes voltage.

Automatic gain control is provided for line loss compensation.

MICROPHONE MONITORING ON TXOUT (PINS MIC+, MIC– AND TXOUT)

The voltage gain between the microphone inputs MIC+/MIC– and the output TXOUT is set to 49 dB. This channel gives an image of the signal sent on the line while speaking in the handset microphone. Using an external circuitry, this signal can be used for several purposes such as sending dynamic limitation or anti-howling in a listening-in application. The TXOUT output is biased at two diodes voltage.

The automatic gain control has no effect on these channels.

Receive channels (pins IR, RAUX, RECO, GARX and QR)

RX AMPLIFIER (PINS IR AND RECO)

The receive amplifier has one input IR which is referred to the line. The input impedance between pins IR and LN is typically equal to 20 kΩ and the DC biasing between these pins is equal to one diode voltage. The gain between pins IR (referred to LN) and RECO is typically equal to 29 dB. Without limitation from the output, the input stage can accommodate signals up to 45 mV (RMS) at room temperature for 2% of total harmonic distortion (THD).

This receive amplifier has a rail-to-rail output RECO, which is designed for use with high ohmic (real) loads (larger than 10 kΩ). This output is biased at two diodes voltage.

Automatic gain control is provided for line loss compensation.

EARPIECE AMPLIFIER (PINS GARX AND QR)

The earpiece amplifier is an operational amplifier having its output (QR) and its inverting input (GARX) available. Its input signal comes, via a decoupling capacitor, from the receive RECO output. It is used in combination with two resistors to get the required gain or attenuation compared to the receive gain. It can be chosen between –3 dB and 15 dB.

The earpiece amplifier has a rail-to-rail output QR, biased at two diodes voltage. It is designed for use with low ohmic (real) loads (150 Ω) or capacitive loads (100 nF in series with 100 Ω).

AUXILIARY RECEIVE AMPLIFIER (PINS RAUX AND RECO)

The auxiliary receive amplifier has an asymmetrical input RAUX; it uses the RECO output. Its input impedance between pins RAUX and GND is typically equal to 20 kΩ. The voltage gain between pins RAUX and RECO is equal to –3 dB. Without any limitation from the output, the input stage can accommodate signals up to 0.9 V (RMS) at room temperature for 2% of total harmonic distortion (THD).

This auxiliary amplifier has a rail-to-rail output RECO, which is designed for use with high ohmic (real) loads (larger than 10 kΩ). This output is biased at two diodes voltage.

The automatic gain control has no effect on this channel.

Auxiliary amplifiers using AUXO (pins MIC+, MIC–, HFTX, IR and AUXO)

The TEA1099H has an auxiliary output AUXO, biased at two diodes voltage. This output stage is a rail-to-rail one, designed for use with high ohmic (real) loads (larger than 10 kΩ). The AUXO output amplifier is used in three different channels, two transmit channels and one receive channel.

AUXILIARY AMPLIFIERS USING THE MICROPHONE INPUTS (PINS MIC+, MIC– AND AUXO)

The auxiliary transmit amplifier using the microphone MIC+/MIC– inputs has a gain of 25 dB referred to AUXO. Without limitation from the output, the input stage can accommodate signals up to 18 mV (RMS) at room temperature for 2% of total harmonic distortion (THD).

The automatic gain control has no effect on this channel.

AUXILIARY AMPLIFIERS USING HFTX (PINS HFTX AND AUXO)

The auxiliary transmit amplifier using the HFTX input has a gain of 15 dB referred to AUXO. Without limitation from the output, the input stage can accommodate signals up to 150 mV (RMS) at room temperature for 2% of total harmonic distortion (THD).

The automatic gain control has no effect on this channel.

RX AMPLIFIER USING IR (PINS IR AND AUXO)

The auxiliary receive amplifier uses pin IR as input. The input is referred to LN and the DC biasing between these two pins is one diode voltage. The voltage gain between the input IR (referred to LN) and the output AUXO is typically equal to 32 dB. Without limitation from the output, the input stage can accommodate signals up to 45 mV (RMS) at room temperature for 2% of total harmonic distortion (THD).

Automatic gain control is provided for line loss compensation.

AGC (pin AGC)

The TEA1099H performs automatic line loss compensation, which fits well with the true line attenuation. The automatic gain control varies the gain of some transmit and receive amplifiers in accordance with the DC line current. The control range is 6.5 dB, which corresponds approximately to a line length of 5.5 km for a 0.5 mm twisted-pair copper cable.

To enable this gain control, the pin AGC must be shorted to pin LN. The start current for compensation corresponds to a line current equal to typically 23 mA and the stop current to 57 mA. The start current can be increased by connecting an external resistor between pins AGC and LN. It can be increased up to 40 mA (using a resistor typically equal to 80 kΩ). The start and stop current will be maintained in a ratio equal to 2.5. By leaving the AGC pin opened, the gain control is disabled and no line loss compensation is performed.

Handsfree application

As can be seen from Fig.3, a loop is formed via the sidetone network in the line interface part and the acoustic coupling between loudspeaker and microphone of the hands-free part. When this loop gain is greater than 1, howling occurs. In a full duplex application, this would be the case. The loop-gain has to be much lower than 1 and therefore has to be decreased to avoid howling. This is achieved by the duplex controller. The duplex controller of the TEA1099H detects which channel has the 'largest' signal and then controls the gain of the microphone amplifier and the loudspeaker amplifier so that the sum of the gains remains constant.

As a result, the circuit in this hands-free application can be in three stable modes:

1. Transmit mode (Tx mode).

   The gain of the microphone amplifier is at its maximum and the gain of the loudspeaker amplifier is at its minimum.
2. Receive mode (RX mode).

   The gain of the loudspeaker amplifier is at its maximum and the gain of the microphone amplifier is at its minimum.
3. Idle mode.

   The gain of the amplifiers is halfway between their maximum and minimum value.

The difference between the maximum gain and minimum gain is called the switching range.

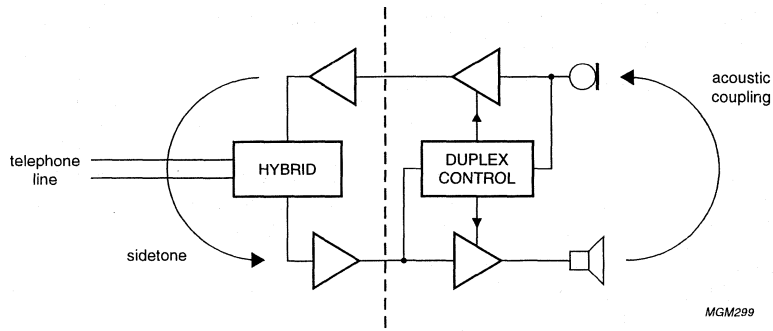


Fig.4 Hands-free telephone set principles.

HANDS-FREE MICROPHONE CHANNEL: PINS TXIN, GATX, TXOUT AND GNDTX (see Fig.5)

The TEA1099H has an asymmetrical hands-free microphone input TXIN with an input resistance of 20 kΩ. The DC biasing of the input is 0 V. The gain of the input stage varies according to the mode of the TEA1099H. In the transmit mode, the gain is at its maximum; in the receive mode, it is at its minimum and in the idle mode, it is halfway between maximum and minimum.

Switch-over from one mode to the other is smooth and click-free. The output TXOUT is biased at two diodes voltage and has a current capability equal to 20 μA (RMS). In the transmit mode, the overall gain of the microphone amplifier (from pins TXIN to TXOUT) can be adjusted from 0 dB up to 31 dB to suit specific application requirements. The gain is proportional to the value of R_{GATX} and equals 15 dB with R_{GATX} = 30.1 kΩ. Without limitation from the output, the microphone input stage can accommodate signals up to 18 mV (RMS) at room temperature for 2% of total harmonic distortion (THD).

A capacitor must be connected in parallel with R_{GATX} to ensure stability of the microphone amplifier. Together with R_{GATX}, it also provides a first-order low-pass filter.

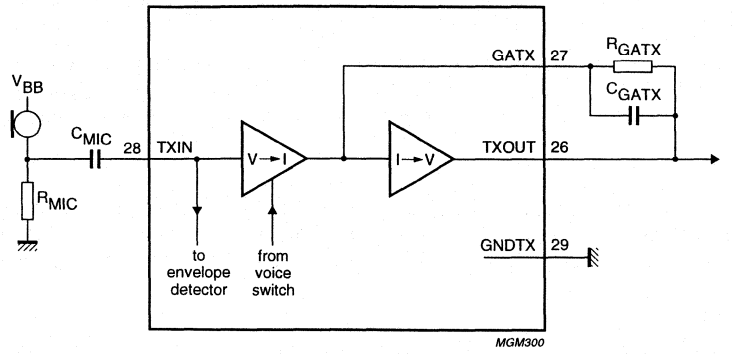


Fig.5 Hands-free microphone channel.

LOUDSPEAKER CHANNEL

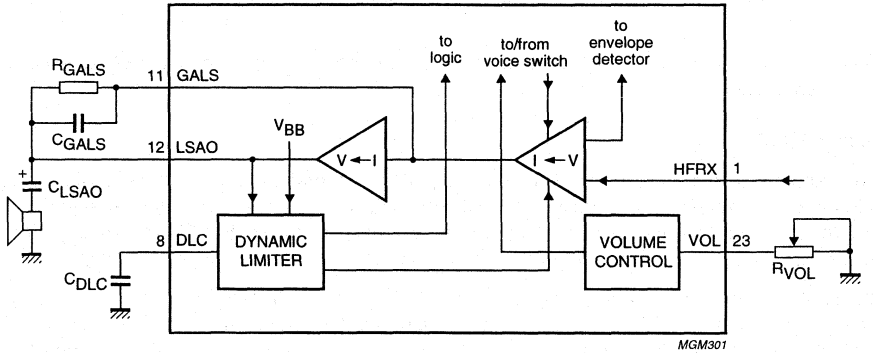


Fig.6 Loudspeaker channel.

Loudspeaker amplifier: pins HFRX, GALS and LSAO

The TEA1099H has an asymmetrical input for the loudspeaker amplifier with an input resistance of 20 kΩ between HFRX and GND. It is biased at two diodes voltage. The input stage can accommodate signals up to 450 mV (RMS) at room temperature for 2% of total harmonic distortion (THD).

The gain of the input stage varies according to the mode of the TEA1099H. In the receive mode, the gain is at its maximum; in the transmit mode, it is at its minimum and in the idle mode, it is halfway between maximum and minimum. Switch-over from one mode to the other is smooth and click-free. The rail-to-rail output stage is designed to power a loudspeaker connected as a single-ended load (between LSAO and GND).

In the receive mode, the overall gain of the loudspeaker amplifier can be adjusted from 0 dB up to 35 dB to suit specific application requirements. The gain from HFRX to LSAO is proportional to the value of R_{GALS} and equals 28 dB with R_{GALS} = 255 kΩ. A capacitor connected in parallel with R_{GALS} can be used to provide a first-order low-pass filter.

Volume control: pin VOL

The loudspeaker amplifier gain can be adjusted with the potentiometer R_{VOL}. A linear potentiometer can be used to obtain logarithmic control of the gain at the loudspeaker amplifier. Each 1.9 kΩ increase of R_{VOL} results in a gain loss of 3 dB. The maximum gain reduction with the volume control is internally limited to the switching range.

Dynamic limiter: pin DLC

The dynamic limiter of the TEA1099H prevents clipping of the loudspeaker output stage and protects the operation of the circuit when the supply voltage at V_{BB} falls below 2.7 V.

Hard clipping of the loudspeaker output stage is prevented by rapidly reducing the gain when the output stage starts to saturate. The time in which gain reduction is effected (clipping attack time) is approximately a few milliseconds. The circuit stays in the reduced gain mode until the peaks of the loudspeaker signals no longer cause saturation. The gain of the loudspeaker amplifier then returns to its normal value within the clipping release time (typically 250 ms). Both attack and release times are proportional to the value of the capacitor C_{DLC}. The total harmonic distortion of the loudspeaker output stage, in reduced gain mode, stays below 5% up to 10 dB (minimum) of input voltage overdrive [providing V_{HFRX} is below 450 mV (RMS)].

When the supply voltage drops below an internal threshold voltage of 2.7 V, the gain of the loudspeaker amplifier is rapidly reduced (approximately 1 ms). When the supply voltage exceeds 2.7 V, the gain of the loudspeaker amplifier is increased again.

By forcing a level lower than 0.2 V on pin DLC, the loudspeaker amplifier is muted and the TEA1099H is automatically forced into the transmit mode.

RX amplifier using AUXO

In some cordless applications, the handset may be used to perform hands-free function (instead of the base). As the TEA1099H is in the base and the active loudspeaker in the handset, a second receive output is required. The amplifier using HFRX as an input and AUXO as output will be used for communication with the RF IC, sending information to the handset. It will be controlled by the duplex controller in the same way as the loudspeaker amplifier.

The voltage gain between pins HFRX and AUXO is equal to 3 dB. The amplifier can manage the same input signal as the loudspeaker amplifier. It has a rail-to-rail output, biased at two diodes, designed for use with high ohmic (real) loads (larger than 10 kΩ). The volume control and the dynamic limiter don't have any action on this channel.

DUPLEX CONTROLLER

Signal and noise envelope detectors: pins TSEN, TENV, TNOI, RSEN, RENV and RNOI

The signal envelopes are used to monitor the signal level strength in both channels. The noise envelopes are used to monitor background noise in both channels. The signal and noise envelopes provide inputs for the decision logic. The signal and noise envelope detectors are shown in Fig.7.

For the transmit channel, the input signal at TXIN is 40 dB amplified to TSEN. For the receive channel, the input signal at HFRX is 0 dB amplified to RSEN. The signals from TSEN and RSEN are logarithmically compressed and buffered to TENV and RENV respectively. The sensitivity of the envelope detectors is set with R_{TSEN} and R_{RSEN}. The capacitors connected in series with the two resistors block any DC component and form a first-order high-pass filter. In the basic

application, see Fig.12, it is assumed that V_{TXIN} = 1 mV (RMS) and V_{HFRX} = 100 mV (RMS) nominal and both R_{TSEN} and R_{RSEN} have a value of 10 kΩ. With the value of C_{TSEN} and C_{RSEN} at 100 nF, the cut-off frequency is at 160 Hz.

The buffer amplifiers leading the compressed signals to TENV and RENV have a maximum source current of 120 μA and a maximum sink current of 1 μA. Together with the capacitor C_{TENV} and C_{RENV}, the timing of the signal envelope monitors can be set. In the basic application, the value of both capacitors is 470 nF. Because of the logarithmic compression, each 6 dB signal increase means 18 mV increase of the voltage on the envelopes TENV or RENV at room temperature. Thus, timings can be expressed in dB/ms. At room temperature, the 120 μA sourced current corresponds to a maximum rise-slope of the signal envelope of 85 dB/ms. This is sufficient to track normal speech signals. The 1 μA current sunk by TENV or RENV corresponds to a maximum fall-slope of 0.7 dB/ms. This is sufficient for a smooth envelope and also eliminates the effect of echoes on switching behaviour.

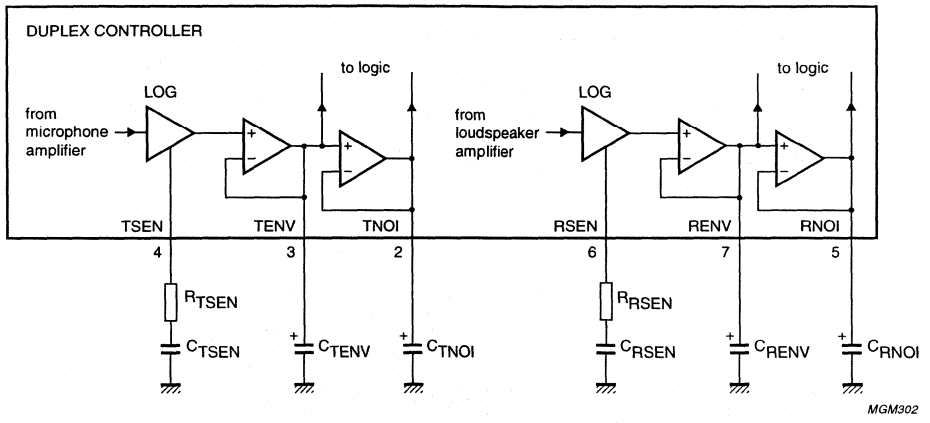


Fig.7 Signal and noise envelope detectors.

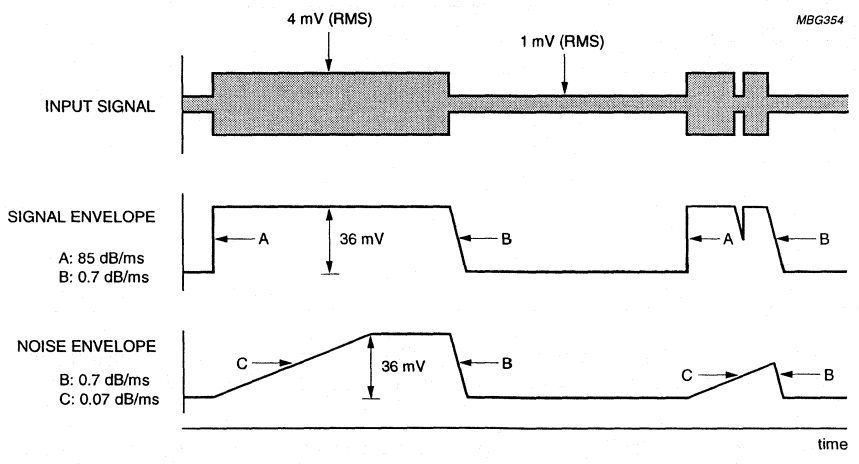
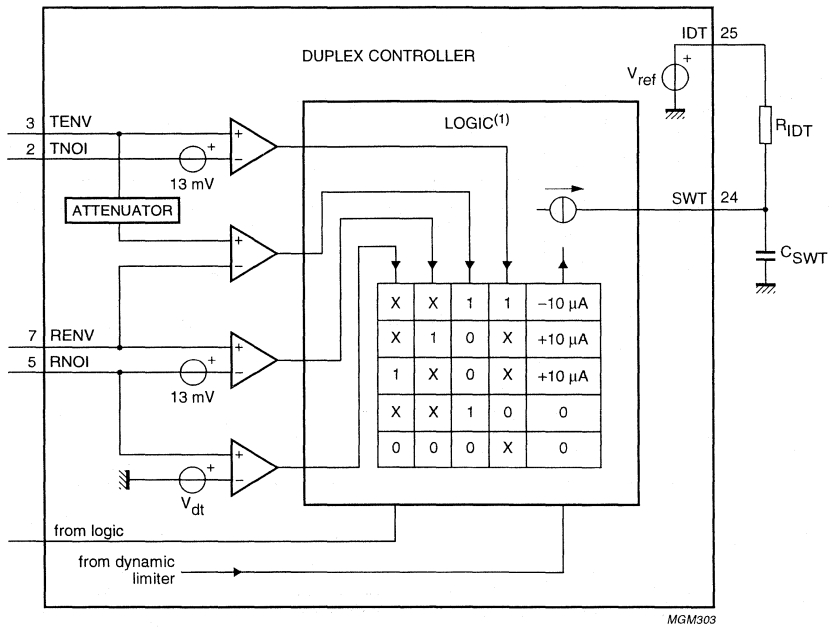


Fig.8 Signal and noise envelope waveforms.

To determine the noise level, the signals on TENV and RENV are buffered to TNOI and RNOI. These buffers have a maximum source current of 1 μA and a maximum sink current of 120 μA. Together with the capacitors C_{TNOI} and C_{RNOI}, the timing can be set. In the basic application, see Fig.12, the value of both capacitors is 4.7 μF. At room temperature, the 1 μA sourced current corresponds to a maximum rise-slope of the noise envelope of approximately 0.07 dB/ms.

This is small enough to track background noise and not to be influenced by speech bursts. The 120 μA current that is sunk corresponds to a maximum fall-slope of approximately 8.5 dB/ms. However, during the decrease of the signal envelope, the noise envelope tracks the signal envelope so it will never fall faster than approximately 0.7 dB/ms. The behaviour of the signal envelope and noise envelope monitors is illustrated in Fig.8.

Decision logic: pins IDT and SWT



(1) When DLC < 0.2 V, −10 μA is forced.

Fig.9 Decision logic.

The TEA1099H selects its mode of operation (transmit, receive or idle mode) by comparing the signal and the noise envelopes of both channels. This is executed by the decision logic. The resulting voltage on pin SWT is the input for the voice-switch.

To facilitate the distinction between signal and noise, the signal is considered as speech when its envelope is more than 4.3 dB above the noise envelope. At room temperature, this is equal to a voltage difference $V_{ENV} - V_{NOI} = 13$ mV. This so called speech/noise threshold is implemented in both channels.

The signal on pin TXIN contains both speech and the signal coming from the loudspeaker (acoustic coupling). When receiving, the contribution from the loudspeaker overrules the speech. As a result, the signal envelope on TENV is formed mainly by the loudspeaker signal. To correct this, an attenuator is connected between TENV and the TENV/RENV comparator. Its attenuation equals that applied to the microphone amplifier.

When a dial tone is present on the line, without monitoring, the tone would be recognized as noise because it is a signal with a constant amplitude. This would cause the TEA1099H to go into the idle mode and the user of the set would hear the dial tone fade away. To prevent this, a dial tone detector is incorporated which, in standard applications, does not consider input signals between HFRX and GND as noise when they have a level greater than 25 mV (RMS). This level is proportional to R_{RSEN}.

In the same way, a transmit detector is integrated which, in standard applications, does not consider input signals between TXIN and GNDTX as noise when they have a level greater than 0.75 mV (RMS). This level is proportional to R_{TSEN}.

As can be seen from Fig.9, the output of the decision logic is a current source. The logic table gives the relationship between the inputs and the value of the current source. It can charge or discharge the capacitor C_{SWT} with a current of 10 μA (switch-over). If the current is zero, the voltage on SWT becomes equal to the voltage on IDT via the high-ohmic resistor R_{IDT} (idling). The resulting voltage difference between SWT and IDT determines the mode of the TEA1099H and can vary between −400 and +400 mV (see Table 1).

Table 1 Modes of TEA1099H

$V_{SWT} - V_{IDT}$ (mV)	MODE
<−180	transmit mode
0	idle mode
>180	receive mode

The switch-over timing can be set with C_{SWT}, the idle mode timing with C_{SWT} and R_{IDT}. In the basic application given in Fig.12, C_{SWT} is 220 nF and R_{IDT} is 2.2 MΩ. This enables a switch-over time from transmit to receive mode or vice-versa of approximately 13 ms (580 mV swing on SWT). The switch-over time from idle mode to transmit mode or receive mode is approximately 4 ms (180 mV swing on SWT).

The switch-over time, from receive mode or transmit mode to idle mode is equal to $4 \times R_{IDT}C_{SWT}$ and is approximately 2 seconds (idle mode time).

The input DLC overrules the decision logic. When the voltage on pin DLC goes lower than 0.2 V, the capacitor C_{SWT} is discharged with 10 μA thus resulting in the transmit mode.

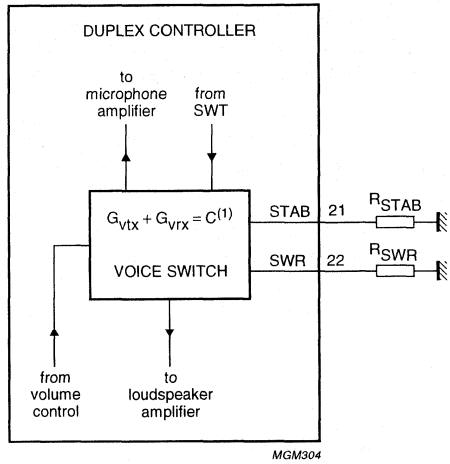
Voice-switch: pins STAB and SWR

A diagram of the voice-switch is illustrated in Fig.10. With the voltage on SWT, the TEA1099H voice-switch regulates the gains of the transmit and the receive channels so that the sum of both is kept constant.

In the transmit mode, the gain of the microphone amplifier is at its maximum and the gain of the loudspeaker amplifier is at its minimum. In the receive mode, the opposite applies. In the idle mode, both microphone and loudspeaker amplifier gains are halfway. The difference between maximum and minimum is the so called switching range. This range is determined by the ratio of R_{SWR} and R_{STAB} and is adjustable between 0 and 52 dB. R_{STAB} should be 3.65 kΩ and sets an internally used reference current. In the basic application diagram given in Fig.12, R_{SWR} is 365 kΩ which results in a switching range of 40 dB. The switch-over behaviour is illustrated in Fig.11.

In the receive mode, the gain of the loudspeaker amplifier can be reduced using the volume control. Since the voice-switch keeps the sum of the gains constant, the gain of the microphone amplifier is increased at the same time (see dashed curves in Fig.11). In the transmit mode, however, the volume control has no influence on the gain of the

microphone amplifier or the gain of the loudspeaker amplifier. Consequently, the switching range is reduced when the volume is reduced. At maximum reduction of volume, the switching range becomes 0 dB.



(1) C = constant.

Fig.10 Voice switch.

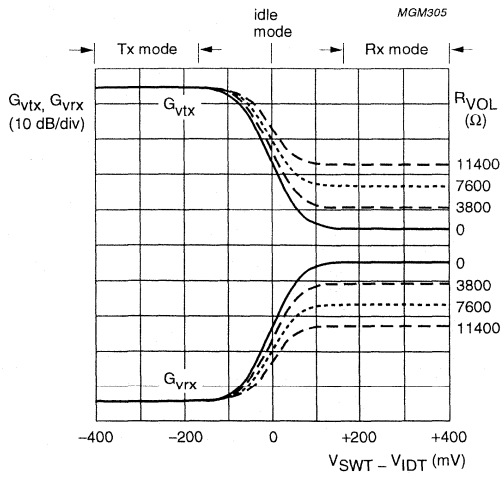


Fig.11 Switch-over behaviour.

Logic inputs

Table 2 Selection of transmit and receive channels for 13 different application modes.

LOGIC INPUTS					FEATURES	APPLICATION EXAMPLES
$\overline{PD}$	HFC	$\overline{MUTT}$	$\overline{MUTR}$	AUXC		
0	X	X	X	1	HFRX to LSAO	ringer mode
0	X	X	X	0		flash, DC dialling
1	0	0	0	0	DTMF to LN; DTMF to RECO; QR; MICS	DTMF dialling (tel. set)
1	0	0	1	0	MIC to AUXO; RAUX to RECO; QR; MICS	cordless intercom with handset
1	0	1	1	0	MICS to LN; IR to RECO; IR to AUXO MIC to TXOUT; QR; MICS	handset conversation (tel. set)
1	0	1	0	1	TXAUX to LN; IR to AUXO	conversation using auxiliary I/O
1	1	1	1	1	TXIN to TXOUT; HFTX to LN; IR to RECO; HFRX to AUXO	cordless: HF mode in handset
1	1	0	1	1	RAUX to RECO; HFRX to LSAO	listening on the loudspeaker
1	1	0	0	1	TXAUX to LN; IR to AUXO; RAUX to RECO; HFRX to LSAO	answering machine: play and record messages; listen the recorded message on the loudspeaker
1	1	0	0	0	DTMF to LN; DTMF to RECO; HFRX to LSAO; QR; MICS	DTMF dialling in HF/GL modes
1	1	1	0	1	TXAUX to LN; IR to AUXO; IR to RECO; HFRX to LSAO	answering machine: play and record messages while listening in the loudspeaker
1	1	0	1	0	TXIN to TXOUT; HFTX to AUXO; RAUX to RECO; HFRX to LSAO; MICS	cordless intercom with base
1	1	1	1	0	TXIN to TXOUT; HFTX to LN; IR to RECO; IR to AUXO; HFRX to LSAO; MICS	HF conversation mode
1	1	1	0	0	MIC to LN; IR to RECO; IR to AUXO; HFRX to LSAO; MIC to TXOUT; QR; MICS	handset conversation with listening-in

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{LN}	positive continuous line voltage		GND–0.4	12	V
	repetitive line voltage during switch-on or line interruption		GND–0.4	13.2	V
V_{ESI}	positive continuous voltage on pin ESI		GND–0.4	5.5	V
I_{ESI}	input current at pin ESI		–	140	mA
$V_{n(max)}$	maximum voltage on pins REG, SLPE, IR, AGC		GND–0.4	V_{LN}+0.4	V
	maximum voltage on all other pins except V_{DD}		GND–0.4	V_{BB}+0.4	V
I_{line}	maximum line current		–	140	mA
P_{tot}	total power dissipation	T_{amb} = 75 °C	–	720	mW
T_{stg}	IC storage temperature		–40	125	°C
T_{amb}	operating ambient temperature		–25	75	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	69	K/W

CHARACTERISTICS

I_{line} = 15 mA; R_{slpe} = 20 Ω; Z_{line} = 600 Ω; f = 1 kHz; T_{amb} = 25°C; AGC pin connected to LN; $\overline{PD}$ = HIGH; HFC = LOW; AUXC = LOW; $\overline{MUTT}$ = HIGH; $\overline{MUTR}$ = HIGH; measured according to test circuits; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
LINE INTERFACE AND INTERNAL SUPPLY (PINS LN, SLPE, REG AND V_{BB})						
V_{SLPE}	stabilized voltage between SLPE and GND	I_{line} = 15 mA	tbf	3.5	tbf	V
		I_{line} = 70 mA	tbf	5.9	tbf	V
V_{BB}	regulated supply voltage for internal circuitry	I_{line} = 15 mA	tbf	3.0	tbf	V
		I_{line} = 70 mA	tbf	5.3	tbf	V
I_{line}	line current for voltage increase					
	start current		–	18	–	mA
	stop current		–	45	–	mA
$\Delta V_{SLPE(T)}$	stabilized voltage variation with temperature referred to 25°C	T_{amb} = −25 to +75°C	–	±40	–	mV
$\Delta V_{BB(T)}$	regulated voltage variation with temperature referred to 25°C	T_{amb} = −25 to +75°C	–	±30	–	mV
I_{BB}	current available on V_{BB}					
	speech mode		–	11.5	–	mA
	handsfree mode		–	9	–	mA
V_{LN}	line voltage	I_{line} = 1 mA	–	1.6	–	V
		I_{line} = 4 mA	–	2.5	–	V
		I_{line} = 15 mA	tbf	3.8	tbf	V
		I_{line} = 140 mA	–	8.7	9.5	V
EXTERNAL SUPPLY (PIN ESI)						
V_{ESI}	external voltage supply allowed on pin ESI		–	–	5.5	V
I_{ESI}	input current on pin ESI	V_{ESI} = 3.5 V	–	3.2	–	mA
		V_{ESI} = 5.5 V	–	8.3	–	mA
I_{ESI}	external current supply allowed on pin ESI		–	–	140	mA
V_{ESI}	voltage on pin ESI when supplied by a current source	I_{ESI} = 100 mA	–	6	–	V
SUPPLY FOR PERIPHERALS (PIN V_{DD})						
V_{DD}	regulated supply voltage on V_{DD}	V_{BB} > 3.3 V + 0.25 V (typ.)	–	3.3	3.6	V
		otherwise	–	V_{BB} − 0.25	–	V
$\Delta V_{DD(T)}$	regulated voltage variation with temperature referred to 25°C	T_{amb} = −25 to +75°C; V_{BB} > 3.3 V + 0.25 V (typ.)	–	±30	–	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DD}	current consumption on V_{DD}	in trickle mode; I_{line} = 0 mA; V_{DD} = 1.5 V; V_{BB} discharging	–	–	0.15	µA
		V_{DD} > 3.3 V	–	120	–	µA
$I_{DD(o)}$	current available for peripherals	V_{DD} = 3.3 V	–	–	–2	mA
SUPPLY FOR MICROPHONE (PIN MICS)						
V_{MICS}	supply voltage for a microphone		–	2	–	V
I_{MICS}	current available on MICS		–	–	–1	mA
POWER DOWN INPUT (PIN $\overline{PD}$)						
V_{IL}	low level input voltage		GND–0.4	–	GND+0.3	V
V_{IH}	high level input voltage		GND+1.8	–	V_{BB} +0.4	V
$I_{\overline{PD}}$	input current		–	–2.5	–5	µA
$I_{BB(PD)}$	current consumption on V_{BB} during power down phase	$\overline{PD}$ = LOW; AUXC = LOW	–	500	–	µA
Preamplifier inputs (pins MIC+, MIC–, IR, DTMF, TXIN, HFTX, HFRX, TXAUX, RAUX)						
$\lvert Z_{i(MIC)} \rvert$	input impedance					
	differential between pins MIC+ and MIC–		–	70	–	kΩ
	single-ended between pins MIC+/MIC– and GNDTX		–	35	–	kΩ
$\lvert Z_{i(IR)} \rvert$	input impedance between pins IR and LN		–	20	–	kΩ
$\lvert Z_{i(DTMF)} \rvert$	input impedance between pins DTMF and GND		–	20	–	kΩ
$\lvert Z_{i(TXIN)} \rvert$	input impedance between pins TXIN and GND		–	20	–	kΩ
$\lvert Z_{i(HFTX)} \rvert$	input impedance between pins HFTX and GND		–	20	–	kΩ
$\lvert Z_{i(HFRX)} \rvert$	input impedance between pins HFRX and GND		–	20	–	kΩ
$\lvert Z_{i(TXAUX)} \rvert$	input impedance between pins TXAUX and GND		–	20	–	kΩ
$\lvert Z_{i(RAUX)} \rvert$	input impedance between pins RAUX and GND		–	20	–	kΩ
TX amplifiers						
TX HANDSET MICROPHONE AMPLIFIER (PINS MIC+, MIC– AND LN)						
$G_{v(MIC-LN)}$	voltage gain from pin MIC+/MIC– to LN	V_{MIC} = 4 mV (RMS)	tbf	44	tbf	dB
$\Delta G_{v(f)}$	gain variation with frequency referred to 1 kHz	f = 300 to 3400 Hz	–	±0.25	–	dB
$\Delta G_{v(T)}$	gain variation with temperature referred to 25°C	T_{amb} = –25 to +75°C	–	±0.25	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CMRR	common mode rejection ratio		–	80	–	dB
THD	total harmonic distortion at LN	V_{LN} = 1.4 V (RMS)	–	–	2	%
		I_{line} = 4 mA; V_{LN} = tbf V (RMS)	–	–	10	%
$V_{no(LN)}$	noise output voltage at pin LN; pins MIC+/MIC– shorted through 200 Ω	psophometrically weighted (p53 curve)	–	–76	–	dBmp
$\Delta G_{v(m)}$	gain reduction if not activated	see table 2	60	80	–	dB
DTMF AMPLIFIER (PINS DTMF, LN AND RECO)						
$G_{v(DTMF-LN)}$	voltage gain from pin DTMF to LN	V_{DTMF} = 50 mV (RMS)	tbf	25.5	tbf	dB
$\Delta G_{v(f)}$	gain variation with frequency referred to 1 kHz	f = 300 to 3400 Hz	–	±0.25	–	dB
$\Delta G_{v(T)}$	gain variation with temperature referred to 25°C	T_{amb} = –25 to +75°C	–	±0.25	–	dB
$\Delta G_{v(m)}$	gain reduction if not activated	see table 2	60	80	–	dB
$G_{v(DTMF-RECO)}$	voltage gain from pin DTMF to RECO	V_{DTMF} = 50 mV (RMS)	–	–17	–	dB
TX AUXILIARY AMPLIFIER USING TXAUX (PINS TXAUX AND LN)						
$G_{v(TXAUX-LN)}$	voltage gain from pin TXAUX to LN	V_{TXAUX} = 0.1 V (RMS)	tbf	12	tbf	dB
$\Delta G_{v(f)}$	gain variation with frequency referred to 1 kHz	f = 300 to 3400 Hz	–	±0.25	–	dB
$\Delta G_{v(T)}$	gain variation with temperature referred to 25°C	T_{amb} = –25 to +75°C	–	±0.25	–	dB
THD	Total harmonic distortion at LN	V_{LN} = 1.4 V (RMS)	–	–	2	%
		I_{line} = 70 mA; V_{TXAUX} = 0.9 V (RMS)	–	–	2	%
$V_{no(LN)}$	noise output voltage at pin LN; pin TXAUX shorted to GND through 200 Ω in series with 10 µF	psophometrically weighted (p53 curve)	–	–80	–	dBmp
$\Delta G_{v(m)}$	gain reduction if not activated	see table 2	60	80	–	dB
TX AMPLIFIER USING HFTX (PINS HFTX AND LN)						
$G_{v(HFTX-LN)}$	voltage gain from pin HFTX to LN	V_{HFTX} = 10 mV (RMS)	tbf	34	tbf	dB
$\Delta G_{v(f)}$	gain variation with frequency referred to 1 kHz	f = 300 to 3400 Hz	–	±0.25	–	dB
$\Delta G_{v(T)}$	gain variation with temperature referred to 25°C	T_{amb} = –25 to +75°C	–	±0.25	–	dB
THD	total harmonic distortion at LN	V_{LN} = 1.4 V (RMS)	–	–	2	%
		I_{line} = 70 mA; V_{HFTX} = 75 mV (RMS)	–	–	2	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{no(LN)}$	noise output voltage at pin LN; pin HFTX shorted to GND through 200 Ω in series with 10 μF	psophometrically weighted (p53 curve)	–	–76	–	dBmp
$\Delta G_{v(m)}$	gain reduction if not activated	see table 2	60	80	–	dB
MICROPHONE MONITORING ON TXOUT (PINS MIC+, MIC– AND TXOUT)						
$G_{v(MIC-TXOUT)}$	voltage gain from pin MIC+/MIC– to TXOUT	V_{MIC} = 2 mV (RMS)	tbf	49	tbf	dB
$\Delta G_{v(f)}$	gain variation with frequency referred to 1 kHz	f = 300 to 3400 Hz	–	±0.25	–	dB
$\Delta G_{v(T)}$	gain variation with temperature referred to 25°C	T_{amb} = –25 to +75°C	–	±0.25	–	dB
$\Delta G_{v(m)}$	gain reduction if not activated	see table 2	60	80	–	dB
RX amplifiers						
RX AMPLIFIERS USING IR (PINS IR AND RECO)						
$G_{v(IR-RECO)}$	voltage gain from pin IR (referred to LN) to RECO	V_{IR} = 4 mV (RMS)	tbf	29	tbf	dB
$\Delta G_{v(f)}$	gain variation with frequency referred to 1 kHz	f = 300 to 3400 Hz	–	±0.25	–	dB
$\Delta G_{v(T)}$	gain variation with temperature referred to 25°C	T_{amb} = –25 to +75°C	–	±0.25	–	dB
THD	total harmonic distortion at RECO	V_{RECO} = 0.85 V (RMS)	–	–	2	%
$V_{no(RECO)(rms)}$	noise output voltage at pin RECO; pin IR is an open circuit (RMS value)	psophometrically weighted (p53 curve)	–	–88	–	dBVp
$\Delta G_{v(m)}$	gain reduction if not activated	see table 2	60	80	–	dB
RX EARPIECE AMPLIFIER (PINS GARX AND QR)						
$\Delta G_{v(QR)}$	gain voltage range between pins RECO and QR		–3	–	+15	dB
$V_{QR(rms)}$	maximum output voltage on QR (RMS value)	sine wave drive; R_L = 150 Ω; THD < 2%	0.65	0.85	–	V
$V_{no(QR)(rms)}$	noise output voltage at pin QR; pin IR is an open circuit (RMS value)	$G_{v(QR)}$ = 0 dB; psophometrically weighted (p53 curve)	–	–88	–	dBVp
$\Delta G_{v(m)}$	gain reduction if not activated	see table 2	60	80	–	dB
RX AMPLIFIER USING RAUX (PINS RAUX AND RECO)						
$G_{v(RAUX-RECO)}$	voltage gain from pin RAUX to RECO	V_{RAUX} = 0.1 V (RMS)	tbf	–3	tbf	dB
$\Delta G_{v(f)}$	gain variation with frequency referred to 1 kHz	f = 300 to 3400 Hz	–	±0.25	–	dB
$\Delta G_{v(T)}$	gain variation with temperature referred to 25°C	T_{amb} = –25 to +75°C	–	±0.25	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
THD	total harmonic distortion at RECO	V_{AUXO} = 0.9 V (RMS)	–	–	2	%
$V_{no(RECO)(rms)}$	noise output voltage at pin RECO; pin RAUX shorted to GND through 200 Ω in series with 10 μF (RMS value)	psophometrically weighted (p53 curve)	–	–99	–	dBVp
$\Delta G_{v(m)}$	gain reduction if not activated	see table 2	60	80	–	dB
Auxiliary amplifiers using AUXO						
TX AUXILIARY AMPLIFIER USING MIC+ AND MIC– (PINS MIC+, MIC– AND AUXO)						
$G_{v(MIC-AUXO)}$	voltage gain from pin MIC+/MIC– to AUXO	V_{MIC} = 4 mV (RMS)	tbf	25	tbf	dB
$\Delta G_{v(f)}$	gain variation with frequency referred to 1 kHz	f = 300 to 3400 Hz	–	±0.25	–	dB
$\Delta G_{v(T)}$	gain variation with temperature referred to 25°C	T_{amb} = –25 to +75°C	–	±0.25	–	dB
THD	total harmonic distortion at AUXO	V_{MIC} = 18 mV (RMS)	–	–	2	%
$V_{no(AUXO)}$	noise output voltage at pin AUXO; pins MIC+/MIC– shorted to GNDTX through 200 Ω in series with 10 μF (RMS value)	psophometrically weighted (p53 curve)	–	–90	–	dBVp
TX AUXILIARY AMPLIFIER USING HFTX (PINS HFTX AND AUXO)						
$G_{v(HFTX-AUXO)}$	voltage gain from pin HFTX to AUXO	V_{HFTX} = 50 mV (RMS)	tbf	15	tbf	dB
$\Delta G_{v(f)}$	gain variation with frequency referred to 1 kHz	f = 300 to 3400 Hz	–	±0.25	–	dB
$\Delta G_{v(T)}$	gain variation with temperature referred to 25°C	T_{amb} = –25 to +75°C	–	±0.25	–	dB
THD	total harmonic distortion at AUXO	V_{HFTX} = 0.15 V (RMS)	–	–	2	%
$V_{no(AUXO)}$	noise output voltage at pin AUXO; pin TXAUX shorted to GND through 200 Ω in series with 10 μF (RMS value)	psophometrically weighted (p53 curve)	–	–90	–	dBVp
$\Delta G_{v(m)}$	gain reduction if not activated	see table 2	60	80	–	dB
RX AMPLIFIER USING IR (PINS IR AND AUXO)						
$G_{v(IR-AUXO)}$	voltage gain from pin IR (referred to LN) to AUXO	V_{RAUX} = 4 mV (RMS)	tbf	32	tbf	dB
$\Delta G_{v(f)}$	gain variation with frequency referred to 1 kHz	f = 300 to 3400 Hz	–	±0.25	–	dB
$\Delta G_{v(T)}$	gain variation with temperature referred to 25°C	T_{amb} = –25 to +75°C	–	±0.25	–	dB
THD	total harmonic distortion at AUXO	V_{AUXO} = 0.85 V (RMS)	–	–	2	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{no(AUXO)(rms)}$	noise output voltage at pin AUXO; pin IR is an open circuit (RMS value)	psophometrically weighted (p53 curve)	–	–85	–	dBVp
$\Delta G_{v(m)}$	gain reduction if not activated	see table 2	60	80	–	dB
Automatic Gain Control (pin AGC)						
$\Delta G_{v(trx)}$	gain control range for transmit and receive amplifiers affected by the AGC; with respect to I_{line} = 15 mA	I_{line} = 70 mA	tbf	6.5	tbf	dB
I_{start}	highest line current for maximum gain		–	23	–	mA
I_{stop}	lowest line current for maximum gain		–	57	–	mA
Logic inputs (pins HFC, AUXC, $\overline{MUTT}$, $\overline{MUTR}$)						
V_{IL}	low level input voltage		GND–0.4	–	GND+0.3	V
V_{IH}	high level input voltage		GND+1.8	–	V_{BB}+0.4	V
I	input current					
	for pins HFC and AUXC		–	2.5	5	μA
	for pins $\overline{MUTT}$ and $\overline{MUTR}$		–	–2.5	–5	μA
Handsfree						
HF MICROPHONE AMPLIFIER (PINS TXIN, TXOUT AND GATX)						
$G_{v(TXIN-TXOUT)}$	voltage gain from pin TXIN to TXOUT	V_{TXIN} = 4 mV (RMS); R_{GATX} = 30.1 kΩ	–	15	–	dB
ΔG_v	voltage gain adjustment with R_{GATX}		–15	–	+16	dB
$\Delta G_{v(f)}$	gain variation with frequency referred to 1 kHz	f = 300 to 3400 Hz	–	±0.3	–	dB
$\Delta G_{v(T)}$	gain variation with temperature referred to 25°C	T_{amb} = –25 to +75°C	–	±0.3	–	dB
$V_{no(TXOUT)(rms)}$	noise output voltage at pin TXOUT; pin TXIN is shorted through 200 Ω in series with 10 μF to GNDTX (RMS value)	psophometrically weighted (p53 curve)	–	–100	–	dBmp
$\Delta G_{v(m)}$	gain reduction if not activated	see table 2	60	80	–	dB
HF LOUDSPEAKER AMPLIFIER (PINS HFRX, LSAO, GALS AND VOL)						
$G_{v(HFRX-LSAO)}$	voltage gain from pin HFRX to LSAO	V_{HFRX} = 30 mV (RMS); R_{GALS} = 255 kΩ	tbf	28	tbf	dB
ΔG_v	voltage gain adjustment with R_{GALS}		–28	–	+7	dB
$\Delta G_{v(f)}$	gain variation with frequency referred to 1 kHz	f = 300 to 3400 Hz	–	±0.3	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\Delta G_{v(T)}$	gain variation with temperature referred to 25°C	T_{amb} = –25 to +75°C	–	±0.3	–	dB
$\Delta G_{v(vol)}$	voltage gain variation related to ΔR_{VOL} = 1.9 kΩ	when total attenuation does not exceed the switching range	–	–3	–	dB
$V_{HFRX(rms)}$	maximum input voltage at pin HFRX (RMS value)	R_{GALS} = 33 kΩ; for 2% THD in the input stage	–	450	–	mV
$V_{no(LSAO)(rms)}$	noise output voltage at pin LSAO; pin HFRX is open circuit (RMS value)	psophometrically weighted (p53 curve)	–	tbf	–	dBVp
$\Delta G_{v(m)}$	gain reduction if not activated	see table 2	60	80	–	dB
$V_{LSAO(rms)}$	output voltage (RMS value)	I_{BB} = 0 mA; I_{DD} = 1 mA				
		I_{line} = 18 mA	–	0.4	–	V
		I_{line} = 30 mA	–	0.9	–	V
		I_{line} > 50 mA	–	1.5	–	V
$I_{LSAO(max)}$	maximum output current at pin LSAO (peak value)		150	–	–	mA
DYNAMIC LIMITER (PINS LSAO AND DLC)						
t_{att}	attack time	when V_{HFRX} jumps from 20 mV to 20 mV + 10 dB	–	–	5	ms
		when V_{BB} jumps below $V_{BB(th)}$	–	1	–	ms
t_{rel}	release time	when V_{HFRX} jumps from 20 mV + 10 dB to 20 mV	–	250	–	ms
THD	Total Harmonic Distortion at V_{HFRX} = 20 mV + 10 dB	$t > t_{att}$	–	1	5	%
$V_{BB(th)}$	V_{BB} limiter threshold		–	2.7	–	V
MUTE RECEIVE (PIN DLC)						
$V_{DLC(th)}$	threshold voltage required on pin DLC to obtain mute receive condition		GND–0.4	–	GND+0.2	V
$I_{DLC(th)}$	threshold current sourced by pin DLC in mute receive condition	V_{DLC} = 0.2 V	–	100	–	µA
$\Delta G_{vrx(m)}$	voltage gain reduction in mute receive condition	V_{DLC} = 0.2 V	60	80	–	dB
RX AMPLIFIER USING HFRX (PINS HFRX AND AUXO)						
$G_{v(HFRX-AUXO)}$	voltage gain from pin HFRX to AUXO	V_{HFRX} = 0.1 V (RMS)	tbf	3	tbf	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\Delta G_{v(f)}$	gain variation with frequency referred to 1 kHz	f = 300 to 3400 Hz	–	±0.25	–	dB
$\Delta G_{v(T)}$	gain variation with temperature referred to 25°C	T_{amb} = −25 to +75°C	–	±0.25	–	dB
THD	total harmonic distortion at RX	V_{HFRX} = 0.48 V (RMS)	–	–	2	%
$V_{no(AUXO)(rms)}$	noise output voltage at pin AUXO; pin HFRX is an open circuit (RMS value)	psophometrically weighted (p53 curve)	–	−96	–	dBVp
$\Delta G_{v(m)}$	gain reduction if not activated	see table 2	60	80	–	dB
TX AND RX ENVELOPE AND NOISE DETECTORS (PINS TSEN, TENV, TNOI, RSEN, RENV AND RNOI)						
Preamplifiers						
$G_{v(TSEN)}$	voltage gain from pin TXIN to TSEN		–	40	–	dB
$G_{v(RSEN)}$	voltage gain from pin HFRX to RSEN		–	0	–	dB
Logarithmic compressor and sensitivity adjustment						
$\Delta V_{det(TSEN)}$	sensitivity detection on pin TSEN; voltage change on pin TENV when doubling the current from TSEN	I_{TSEN} = 0.8 to 160 µA	–	18	–	mV
$\Delta V_{det(RSEN)}$	sensitivity detection on pin RSEN; voltage change on pin RENV when doubling the current from RSEN	I_{RSEN} = 0.8 to 160 µA	–	18	–	mV
Signal envelope detectors						
$I_{source(ENV)}$	maximum current sourced from pin TENV or RENV		–	120	–	µA
$I_{sink(ENV)}$	maximum current sunk by pin TENV or RENV		−1.25	−1	−0.75	µA
ΔV_{ENV}	voltage difference between pins RENV and TENV	note 1; when 10 µA is sourced from both RSEN and TSEN; signal detectors tracking	–	±3	–	mV
Noise envelope detectors						
$I_{source(NOI)}$	maximum current sourced from pin TNOI or RNOI		0.75	1	1.25	µA
$I_{sink(NOI)}$	maximum current sunked by pin TNOI or RNOI		–	−120	–	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ΔV_{NOI}	voltage difference between pins RNOI and TNOI	note 1; when 5 µA is sourced from both RSEN and TSEN; noise detectors tracking	–	±3	–	mV
DIAL TONE DETECTOR						
$V_{HFRX(th)(rms)}$	threshold level at pin HFRX (RMS value)	R_{RSEN} = 10 kΩ	–	25	–	mV
TX LEVEL LIMITER						
$V_{TXIN(th)(rms)}$	threshold level at pin TXIN(RMS value)	R_{TSEN} = 10 kΩ	–	0.75	–	mV
DECISION LOGIC (PINS IDT AND SWT)						
Signal recognition						
$\Delta V_{Srx(th)}$	threshold voltage between pins RENV and RNOI to switch-over from receive to idle mode	note 2; $V_{HFRX} < V_{HFRX(th)}$	–	13	–	mV
$\Delta V_{Stx(th)}$	threshold voltage between pins TENV and TNOI to switch-over from transmit to idle mode	note 2; $V_{TXIN} < V_{TXIN(th)}$	–	13	–	mV
Switch-over						
$I_{source(SWT)}$	current sourced from pin SWT when switching to receive mode		7.5	10	12.5	µA
$I_{sink(SWT)}$	current sunk by pin SWT when switching to transmit mode		–12.5	–10	–7.5	µA
$I_{idle(SWT)}$	current sourced from pin SWT in idle mode		–	0	–	µA
VOICE SWITCH (PINS STAB AND SWR)						
SWRA	switching range		–	40	–	dB
ΔSWRA	switching range adjustment	with R_{SWR} referred to 365 kΩ	–40	–	+12	dB
$\lvert\Delta G_v\rvert$	voltage gain variation from transmit or receive mode to idle mode		–	20	–	dB
G_{tr}	gain tracking ($G_{vtx} + G_{vrx}$) during switching, referred to idle mode		–	0.5	–	dB

Notes

1. corresponds to ±1 dB tracking
2. corresponds to 4.3 dB noise/speech recognition level

APPLICATION INFORMATION

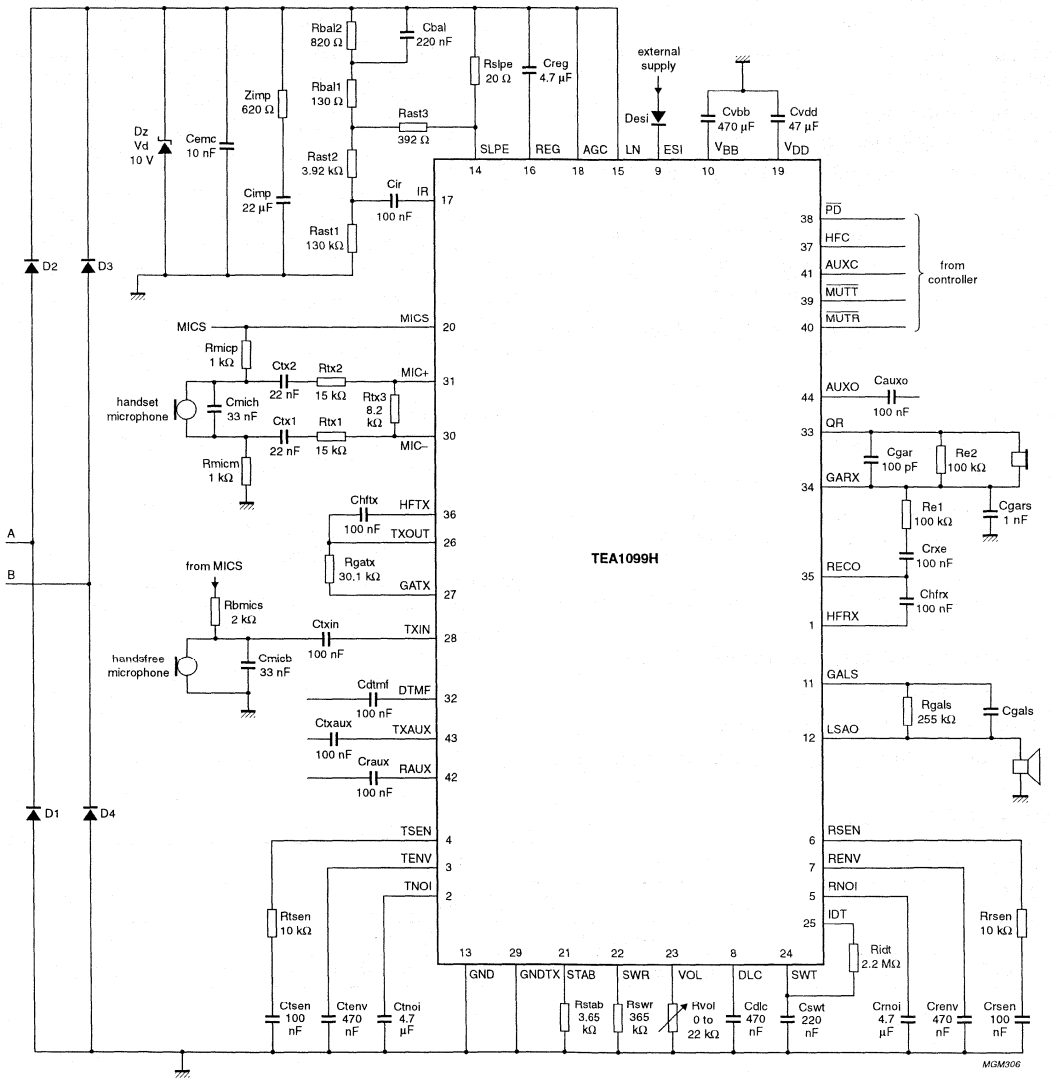


Fig.12 Basic application diagram

Fast charge IC for NiCd, NiMH, SLA and Lilon

TEA1102

FEATURES

- Safe and fast charging of Nickel Cadmium (NiCd), Nickel Metal Hydride (NiMH), Lithium Ion (Lilon), and Sealed Lead Acid (SLA) batteries
- Three charge states for NiCd or NiMH; fast, top-off and trickle or voltage regulation (optional)
- Two charge states for Lilon or SLA; current and voltage limited
- Adjustable fast charge current [0.5CA to 5CA nominal (CA = Capacity Amperes)]
- DC top-off and pulsating trickle charge current (NiCd and NiMH)
- Temperature dependent $\Delta T/\Delta t$ battery full detection
- Automatic switch-over to accurate peak voltage detection ($-1/4$%) if no NTC is applied
- Possibility to use both $\Delta T/\Delta t$ and peak voltage detection as main fast charge termination
- Support of inhibit during all charging states
- Manual refresh with regulated adjustable discharge current (NiCd and NiMH)
- Voltage regulation in the event of no battery
- Support of battery voltage based charge indication and buzzer signalling at battery insertion, end of refresh and at full detection
- Single, dual and separate LED outputs for indication of charge status state
- Minimum and maximum temperature protection
- Time-out protection
- Short-circuit battery voltage protection
- Can be applied with few low-cost external components.

GENERAL DESCRIPTION

The TEA1102; TEA1102T are fast charge ICs which are able fast charge NiCd and NiMH, SLA and Lilon batteries.

The main fast charge termination for NiCd and NiMH batteries are $\Delta T/\Delta t$ and peak voltage detection, both of which are well proven techniques. The TEA1102; TEA1102T automatically switches over from $\Delta T/\Delta t$ to peak voltage detection if the thermistor fails or is not present. The $\Delta T/\Delta t$ detection sensitivity is temperature dependent, thus avoiding false charge termination. Three charge states can be distinguished; fast, top-off and trickle.

Charging Lilon and SLA batteries is completely different. When the batteries reach their maximum voltage (adjustable), the TEA1102; TEA1102T switches over from current regulation to voltage regulation. After a defined time period, which is dependent on battery capacity and charge current, charge is terminated. Due to small self discharge rates of Lilon and SLA batteries, trickle charge can be omitted.

Several LEDs, as well as a buzzer, can be connected to the TEA1102; TEA1102T for indicating battery insertion, charge states, battery full condition and protection mode.

The TEA1102; TEA1102T are contained in a 20-pin package and are manufactured in a BiCMOS process, essentially for integrating the complex mix of requirements in a single chip solution. Only a few external low cost components are required in order to build a state of the art charger.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA1102	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT 146-1
TEA1102T	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

Full Data Sheet: on CD-ROM/WWW (Internet) or FOD-system (details in front Section/back of this HB), or updated Loose leaf or Parent HB

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		5.45	–	11.5	V
I_P	supply current	outputs off	–	4	–	mA
$\Delta V_{NTC}/V_{NTC}$	temperature rate dependent ($\Delta T/\Delta t$) detection level	V_{NTC} = 2 V T_j = 0 to 50 °C	–	–0.25	–	%
$\Delta V_{bat}/V_{bat}$	voltage peak detection level with respect to top value	V_{bat} = 2 V T_j = 0 to 50 °C	–	–0.25	–	%
I_{Vbat}	input current battery monitor	V_{bat} = 0.3 to 1.9 V	–	1	–	nA
$V_{bat(l)}$	voltage at pin 19 for detecting low battery voltage		–	0.30	–	V
I_{IB}	battery charge current	fast charge	10	–	100	µA
		top-off mode	–	3	–	µA
$I_{IB(max)}$	maximum battery charge current	voltage regulation full NiCd and NiMH battery	–	10	–	µA
$I_{IB(Lmax)}$	maximum load current	no battery	–	40	–	µA
f_{osc}	oscillator frequency		10	–	200	kHz
V_{reg}	regulating voltage	Lilon	–	1.37	–	V
		SLA	–	1.63	–	V
		NiCd and NiMH (pin V_{stb} open-circuit)	–	1.325 or V_{stb}	–	V
		open battery	–	1.9	–	V

BLOCK DIAGRAM

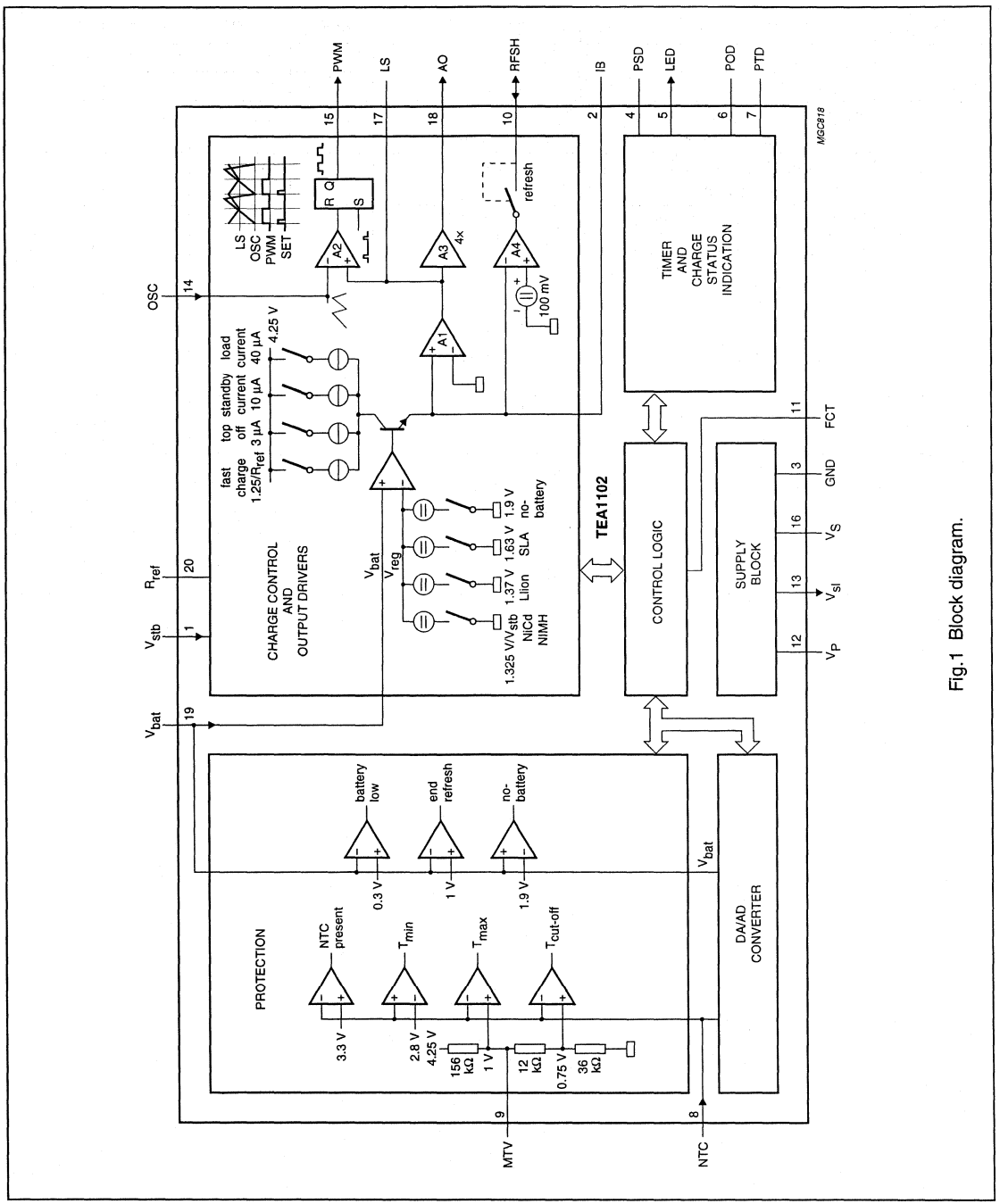


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{stb}	1	standby regulation voltage input (NiCd and NiMH)
IB	2	charge current setting
GND	3	ground
PSD	4	program pin sample divider
LED	5	LED output
POD	6	program pin oscillator divider
PTD	7	program pin time-out divider
NTC	8	temperature sensing input
MTV	9	maximum temperature voltage
RFSH	10	refresh input/output
FCT	11	fast charge termination and battery chemistry identification
V_P	12	positive supply voltage
V_{sl}	13	switched reference voltage output
OSC	14	oscillator input
PWM	15	pulse width modulator output
V_S	16	stabilized reference voltage
LS	17	loop stability pin
AO	18	analog output
V_{bat}	19	single-cell battery voltage input
R_{ref}	20	reference resistor pin

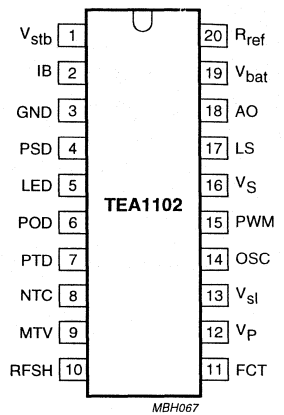


Fig.2 Pin configuration.

Cost effective battery monitor and fast charge IC for NiCd and NiMH chargers

TEA1104

FEATURES

- Accurate detection of fully charged batteries by currentless peak voltage sensing
- Switch-over from fast to safe trickle charge current at battery full detection
- Fast charge termination back-up by maximum time and maximum temperature detection
- Several trickle charge drive possibilities for mains isolated and non-mains isolated systems
- Battery checking to protect against short-circuited and open batteries
- Battery monitor allows recharging of different battery packs in the same charger
- Dual LED indicator provision
- External regulator not required because of large input voltage range
- Few low cost external components required.

APPLICATIONS

- Portable telephone
- Portable computer
- Portable audio
- Portable video.

GENERAL DESCRIPTION

The TEA1104 is manufactured in a BiCMOS process intended to be used as a battery monitor circuit in charge systems for NiCd and NiMH batteries. It is especially designed for cost effective compact consumer applications.

The circuit is able to detect fully charged batteries by currentless battery voltage sensing. Several output drive functions are available to control the (reduced) trickle charge current to keep the batteries full with maximum life expectations.

The battery full detection is backed up by two independent mechanisms to make the system fail safe; maximum time and maximum temperature.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		5.45	–	11.5	V
I_P	supply current	outputs off	–	–	3	mA
V_{bat}	voltage range of battery full detection		0.81	–	3.6	V
$\Delta V_{bat}/V_{bat}$	voltage peak detection level with respect to top value		–	0.25	–	%
I_{bat}	battery monitor input current		–	–	1	nA
$V_{bat(l)}$	battery voltage protection low		–	0.81	0.91	V
$V_{bat(h)}$	battery voltage protection high		3.5	3.6	–	V
f_{osc}	oscillator frequency		10	–	100	kHz

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA1104	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
TEA1104T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

Full Data Sheet: on CD-ROM/WWW (Internet) or FOD-system (details in front Section/back of this HB), or updated Loose leaf or Parent HB

Cost effective battery monitor and fast charge IC for NiCd and NiMH chargers

TEA1104

BLOCK DIAGRAM

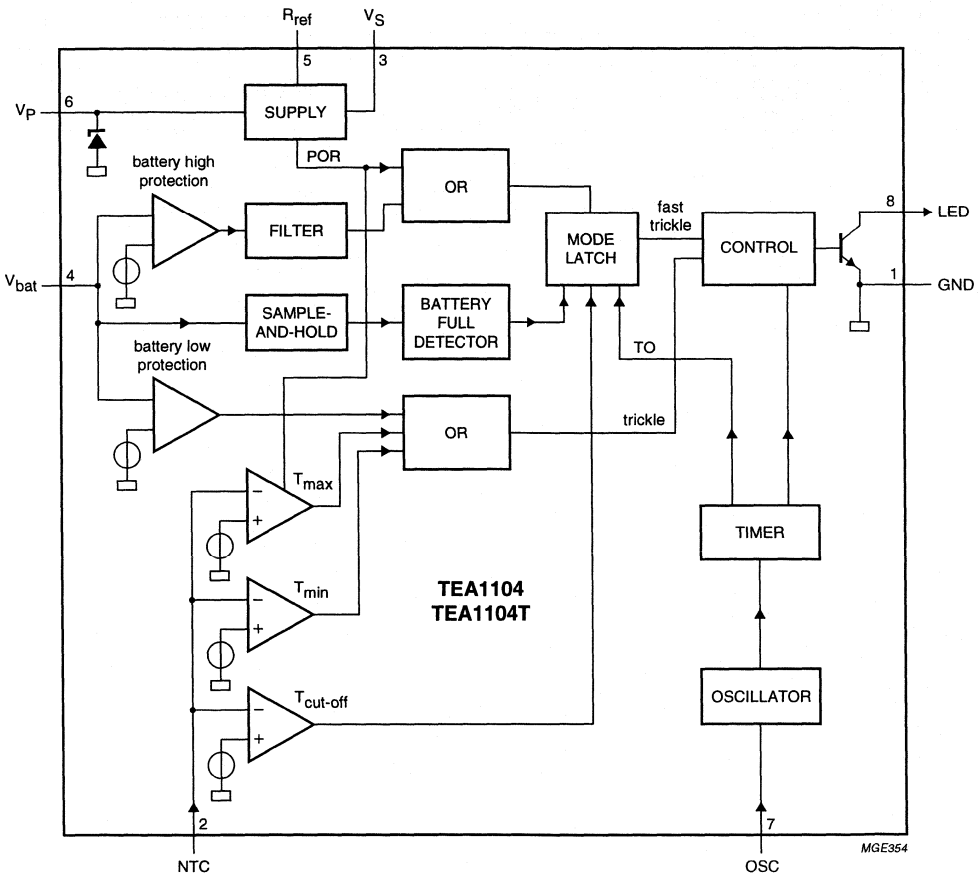


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
GND	1	ground
NTC	2	negative temperature coefficient resistor input
V_S	3	stabilized supply voltage
V_{bat}	4	battery voltage sensing
R_{ref}	5	reference resistor
V_P	6	positive supply voltage
OSC	7	oscillator input
LED	8	LED output

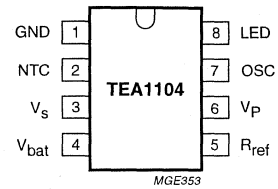


Fig.2 Pin configuration.

Versatile cordless transmisssion circuit TEA1118; TEA1118A

FEATURES

- Low DC line voltage; operates down to 1.6 V (excluding polarity guard)
- Voltage regulator with adjustable DC voltage
- Provides a supply for external circuits
- Symmetrical high impedance transmit inputs (62.5 kΩ) with large signals handling capabilities [up to 1 V (RMS value) with less than 2% THD]
- Receive amplifier for dynamic, magnetic or piezoelectric earpieces
- AGC line loss compensation for transmit and earpiece amplifiers
- DTMF input with confidence tone (TEA1118A only)
- MUTE input for pulse or DTMF dialling (TEA1118A only)
- Transmit mute function, also enabling the DTMF input (TEA1118A only).

APPLICATIONS

- Cordless telephone base stations
- Fax machines
- Answering machines.

GENERAL DESCRIPTION

The TEA1118 and TEA1118A are bipolar integrated circuits that perform all speech and line interface functions required in cordless telephone base stations. The ICs operate at a line voltage down to 1.6 V DC (with reduced performance) to facilitate the use of telephone sets connected in parallel.

The TEA1118A offers in addition to the TEA1118 electronic switching between speech and dialling. Moreover the transmit amplifier can be disabled during speech condition by means of a transmit mute function.

All statements and values refer to all versions unless otherwise specified.

QUICK REFERENCE DATA

I_{line} = 15 mA; V_{EE} = 0 V; R_{SLPE} = 20 Ω; AGC pin connected to V_{EE}; Z_{line} = 600 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{line}	line current operating range	normal operation	11	–	140	mA
		with reduced performance	1	–	11	mA
V_{LN}	DC line voltage		3.35	3.65	3.95	V
I_{CC}	internal current consumption	V_{CC} = 2.9 V	–	1.15	1.4	mA
V_{CC}	supply voltage for peripherals	I_P = 0 mA	–	2.9	–	V
G_{vtrx}	typical voltage gain range					
	transmit amplifier (TEA1118A only)	V_{TX} = 200 mV (RMS)	–	–	11.3	dB
	transmit amplifier (TEA1118 only)	V_{TX} = 200 mV (RMS)	5.3	–	11.3	dB
	receive amplifier	V_{IR} = 4 mV (RMS)	19	–	31	dB
ΔG_{vtrx}	gain control range for transmit and receive amplifiers with respect to I_{line} = 15 mA	I_{line} = 75 mA	–	5.8	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA1118M	SSOP16	plastic shrink small outline package; 16 leads; body width 4.4 mm	SOT369-1
TEA1118T	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
TEA1118AM	SSOP16	plastic shrink small outline package; 16 leads; body width 4.4 mm	SOT369-1
TEA1118AT	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1

BLOCK DIAGRAMS

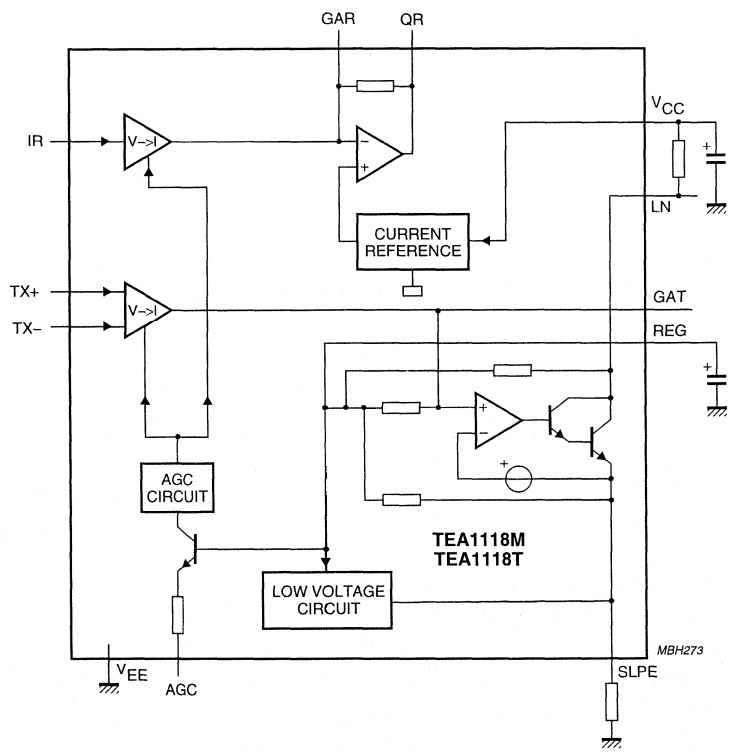


Fig.1 Block diagram (TEA1118).

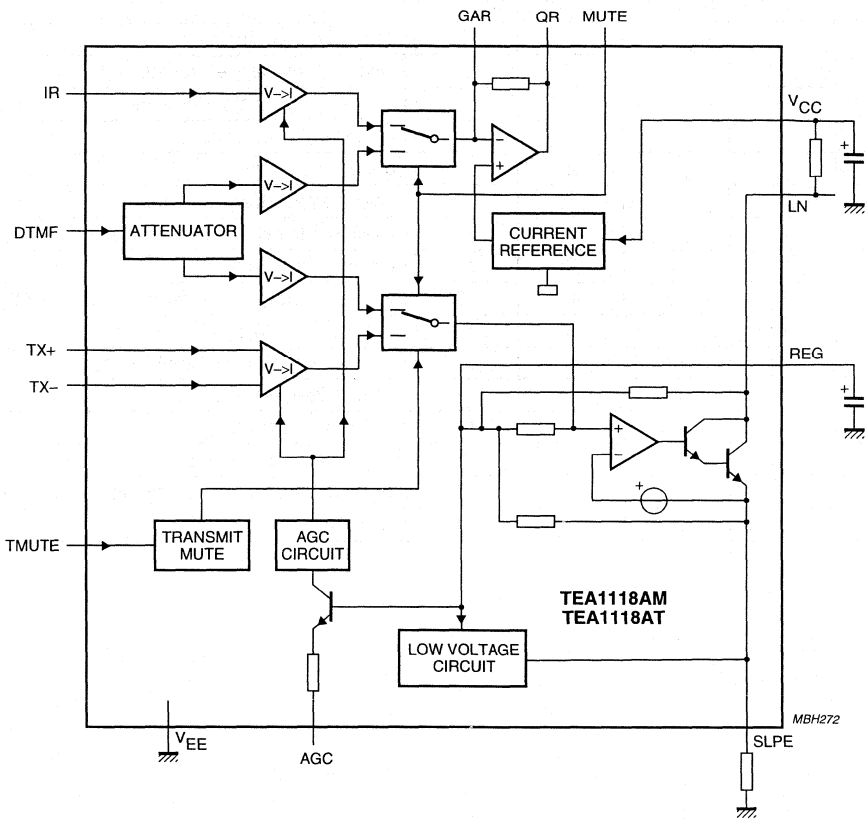


Fig.2 Block diagram (TEA1118A).

PINNING

SYMBOL	TEA1118		TEA1118A		DESCRIPTION
	SO14	SSOP16	SO14	SSOP16	
LN	1	1	1	1	positive line terminal
SLPE	2	2	2	2	slope (DC resistance) adjustment
REG	3	3	3	3	line voltage regulator decoupling
GAT	4	4	–	–	transmit gain adjustment
TMUTE	–	–	4	5	transmit mute input
DTMF	–	–	5	6	dual-tone multi-frequency input
MUTE	–	–	6	8	mute input to select speech or dialling mode
IR	7	9	7	9	receive amplifier input
AGC	8	10	8	10	automatic gain control/line loss compensation
TX–	9	11	9	11	inverting transmit amplifier input
TX+	10	12	10	12	non-inverting transmit amplifier input
V_{EE}	11	13	11	13	negative line terminal
QR	12	14	12	14	receive amplifier output
GAR	13	15	13	15	receive gain adjustment
V_{CC}	14	16	14	16	supply voltage for speech circuit and peripherals
n.c.	5 and 6	5 to 8	–	4 and 7	not connected

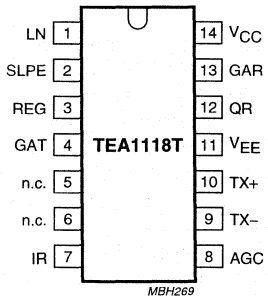


Fig.3 Pin configuration (TEA1118T).

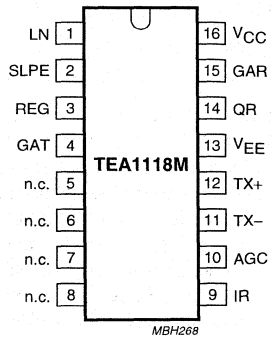


Fig.4 Pin configuration (TEA1118M).

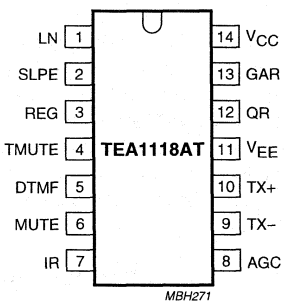


Fig.5 Pin configuration (TEA1118AT).

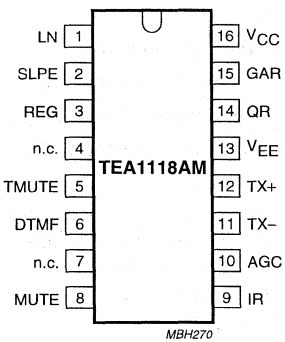


Fig.6 Pin configuration (TEA1118AM).

FUNCTIONAL DESCRIPTION

All data given in this chapter are typical values, except when otherwise specified.

Supplies (pins LN, SLPE, V_{CC} and REG)

The supply for the TEA1118 and TEA1118A and their peripherals is obtained from the telephone line.

The ICs generate a stabilized reference voltage (V_{ref}) between pins LN and SLPE. This reference voltage is equal to 3.35 V, is temperature compensated and can be adjusted by means of an external resistor (R_{VA}). It can be increased by connecting the R_{VA} resistor between pins REG and SLPE (see Fig.11), or decreased by connecting the R_{VA} resistor between pins REG and LN. The voltage at pin REG is used by the internal regulator to generate the stabilized reference voltage and is decoupled by a capacitor (C_{REG}) which is connected to V_{EE}. This capacitor, converted into an equivalent inductance (see Section "Set impedance"), realizes the set impedance conversion from its DC value (R_{SLPE}) to its AC value (R_{CC} in the audio-frequency range). The voltage at pin SLPE is proportional to the line current. Figure 7 illustrates the supply configuration.

The ICs regulate the line voltage at pin LN, and it can be calculated as follows:

$$V_{LN} = V_{ref} + R_{SLPE} \times I_{SLPE}$$

$$I_{SLPE} = I_{line} - I_{CC} - I_P - I^* = I_{sh}$$

where:

I_{line}: line current

I_{CC}: current consumption of the IC

I_P: supply current for peripheral circuits

I^*: current consumed between LN and V_{EE}

I_{sh}: the excess line current shunted to SLPE (and V_{EE}) via LN.

The preferred value for R_{SLPE} is 20 Ω. Changing R_{SLPE} will affect more than the DC characteristics; it also influences the transmit gain and the DTMF gain (TEA1118A only), the gain control characteristics, the sidetone level and the maximum output swing on the line.

The internal circuitry of the TEA1118 and TEA1118A is supplied from pin V_{CC}. This voltage supply is derived from the line voltage by means of a resistor (R_{CC}) and must be decoupled by a capacitor C_{VCC}. It may also be used to supply peripheral circuits such as dialling or control circuits. The V_{CC} voltage depends on the current consumed by the IC and the peripheral circuits as shown by the formula (see also Figs 8 and 9). R_{CCint} is the internal equivalent resistance of the voltage supply point, and I_{rec} is the current consumed by the output stage of the earpiece amplifier.

$$V_{CC} = V_{CC0} - R_{CCint} \times (I_P - I_{rec})$$

$$V_{CC0} = V_{LN} - R_{CC} \times I_{CC}$$

The DC line current flowing into the set is determined by the exchange supply voltage (V_{exch}), the feeding bridge resistance (R_{exch}), the DC resistance of the telephone line (R_{line}) and the reference voltage (V_{ref}). With line currents below 7.5 mA, the internal reference voltage (generating V_{ref}) is automatically adjusted to a lower value. This means that more sets can operate in parallel with DC line voltages (excluding the polarity guard) down to an absolute minimum voltage of 1.6 V. At currents below 7.5 mA, the circuit has limited transmit and receive levels. This is called the low voltage area.

Set impedance

In the audio frequency range, the dynamic impedance is mainly determined by the R_{CC} resistor. The equivalent impedance of the circuits is illustrated in Fig.10.

Transmit amplifier (pins TX+, TX– and GAT)

The TEA1118 and TEA1118A have symmetrical transmit inputs. The input impedance between pins TX+ and TX– is equal to 62.5 kΩ; the input impedance between pins TX+/TX– and V_{EE} is equal 36.5 kΩ. The voltage gain from pins TX+/TX– to pin LN is set at 11.3 dB.

Automatic gain control is provided on this amplifier for line loss compensation.

The gain of the TEA1118 can be decreased by connecting an external resistor R_{GAT} between pins GAT and REG. The adjustment range is equal to 6 dB. A capacitor C_{GAT} connected between pins GAT and REG can be used to provide a first-order low-pass filter. The cut-off frequency corresponds to the time constant $C_{GAT} \times (R_{GATint} // R_{GAT})$. R_{GATint} is the internal resistor which sets the gain with a typical value of 27 kΩ.

Transmit mute (pin TMUTE; TEA1118A only)

The transmit amplifier can be disabled by activating the transmit mute function. When TMUTE is LOW, the normal speech mode is entered, depending on the level on MUTE. When TMUTE is HIGH, the transmit amplifier inputs are disabled while the DTMF input is enabled (no confidence tone is provided). The voltage gain between LN and TX+/TX– is attenuated; the gain reduction is 80 dB.

Receive amplifier (pins IR, GAR and QR)

The receive amplifier has one input (IR) and one output (QR). The input impedance between pins IR and V_{EE} is 20 kΩ. The voltage gain from pin IR to pin QR is set at 31 dB. The gain can be decreased by connecting an external resistor R_{GAR} between pins GAR and QR; the adjustment range is 12 dB. Two external capacitors C_{GAR} (connected between GAR and QR) and C_{GARS} (connected between GAR and V_{EE}) ensure stability.

The C_{GAR} capacitor provides a first-order low-pass filter. The cut-off frequency corresponds to the time constant $C_{GAR} \times (R_{GARint} // R_{GAR})$. R_{GARint} is the internal resistor which sets the gain with a typical value of 100 kΩ. The condition $C_{GARS} = 10 \times C_{GAR}$ must be fulfilled to ensure stability.

Automatic gain control is provided on this amplifier for line loss compensation.

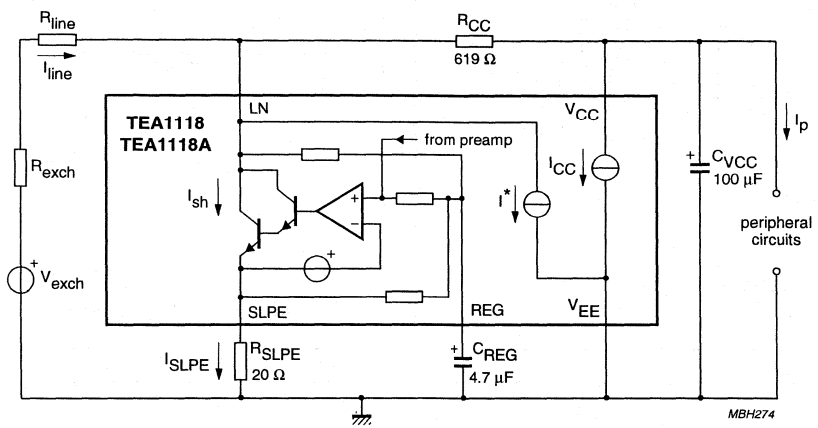
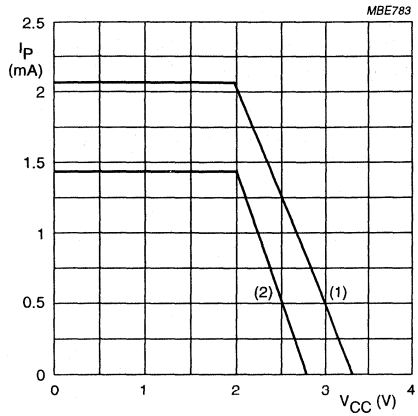


Fig.7 Supply configuration.



(1) With R_{VA} resistor.
(2) Without R_{VA} resistor.

Fig.8 Typical current I_P available from V_{CC} for peripheral circuits at I_{line} = 15 mA.

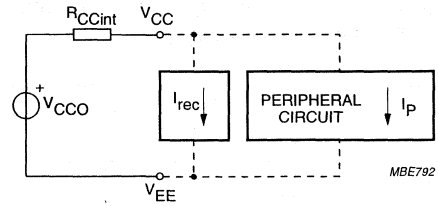
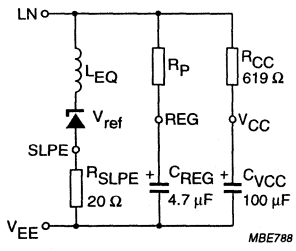
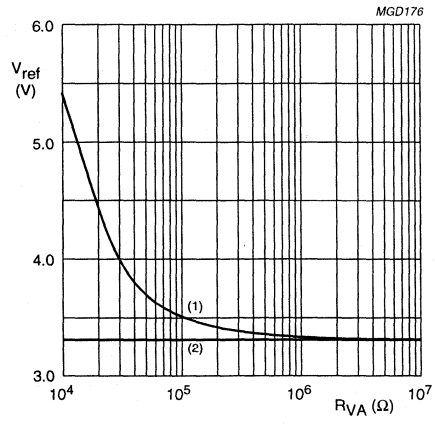


Fig.9 V_{CC} voltage supply for peripheral.



$L_{EQ} = C_{REG} \times R_{SLPE} \times R_P$.
R_P = internal resistance (15.5 kΩ).

Fig.10 Equivalent impedance between LN and V_{EE}.



(1) Influence of R_{VA} on V_{ref}.
(2) V_{ref} without influence of R_{VA}.

Fig.11 Reference voltage adjustment by R_{VA}.

Automatic Gain Control (pin AGC)

The TEA1118 and TEA1118A perform automatic line loss compensation. The automatic gain control varies the gain of the transmit amplifier and the gain of the receive amplifier in accordance with the DC line current.
The control range is 5.8 dB (which corresponds approximately to a line length of 5 km for a 0.5 mm diameter twisted-pair copper cable with a DC resistance of 176 Ω/km and an average attenuation of 1.2 dB/km).
The ICs can be used with different configurations of feeding bridge (supply voltage and bridge resistance) by connecting an external resistor R_{AGC} between pins AGC and V_{EE}. This resistor enables the I_{start} and I_{stop} line currents to be increased (the ratio between I_{start} and I_{stop} is not affected by the resistor). The AGC function is disabled when pin AGC is left open-circuit.

DTMF amplifier (pin DTMF; TEA1118A only)

When the DTMF amplifier is enabled, dialling tones may be sent on line. These tones can be heard in the earpiece at a low level (confidence tone).

The TEA1118A has an asymmetrical DTMF input.
The input impedance between DTMF and V_{EE} is 20 kΩ.
The voltage gain from pin DTMF to pin LN is 17.4 dB.

The automatic gain control has no effect on the DTMF amplifier.

Mute function (pin MUTE; TEA1118A only)

The mute function performs the switching action between the speech mode and the dialling mode. When MUTE is LOW or open-circuit, the transmit and receive amplifiers inputs are enabled while the DTMF input is disabled, depending on the TMUTE level. When MUTE is HIGH, the DTMF input is enabled and the transmit and receive amplifiers inputs are disabled.

Sidetone suppression

The TEA1118 and TEA1118A anti-sidetone network comprising $R_{CC}//Z_{line}$, R_{ast1}, R_{ast2}, R_{ast3}, R_{SLPE} and Z_{bal} (see Fig.12) suppresses the transmitted signal in the earpiece. Maximum compensation is obtained when the following conditions are fulfilled:

$$R_{SLPE} \times R_{ast1} = R_{CC} \times (R_{ast2} + R_{ast3})$$

$$k = \frac{[R_{ast2} \times (R_{ast3} + R_{SLPE})]}{(R_{ast1} \times R_{SLPE})}$$

$$Z_{bal} = k \times Z_{line}$$

The scale factor k is chosen to meet the compatibility with a standard capacitor from the E6 or E12 range for Z_{bal}.

In practice, Z_{line} varies considerably with the line type and the line length. Therefore, the value chosen for Z_{bal} should be for an average line length which gives satisfactory sidetone suppression with short and long lines.
The suppression also depends on the accuracy of the match between Z_{bal} and the impedance of the average line.

The anti-sidetone network for the TEA1118 and TEA1118A (as shown in Fig.16) attenuates the receive signal from the line by 32 dB before it enters the receive amplifier.
The attenuation is almost constant over the whole audio frequency range.

A Wheatstone bridge configuration (see Fig.13) may also be used.

More information on the balancing of an anti-sidetone bridge can be obtained in our publication *"Applications Handbook for Wired Telecom Systems, IC03b"*, order number 9397 750 00811.

MUTE and TMUTE levels for different modes (TEA1118A only)

Table 1 Required MUTE and TMUTE levels to enable the different possible modes

MODE	CHANNEL				MUTE	TMUTE
	TRANSMIT	RECEIVE	DTMF	CONFIDENCE TONE		
Speech	on	on	off	off	LOW	LOW
DTMF dialling	off	off	on	on	HIGH	X[1]
Transmit mute	off	on	on	off	LOW	HIGH

Note

1. X = don't care.

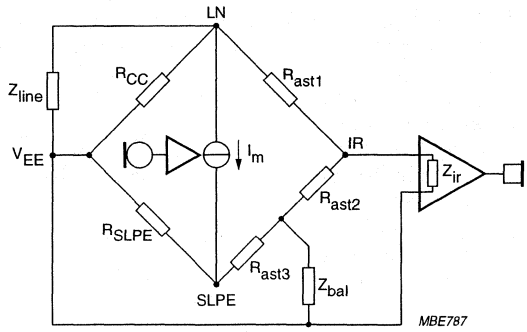


Fig.12 Equivalent circuit of TEA1118 and TEA1118A family anti-sidetone bridge.

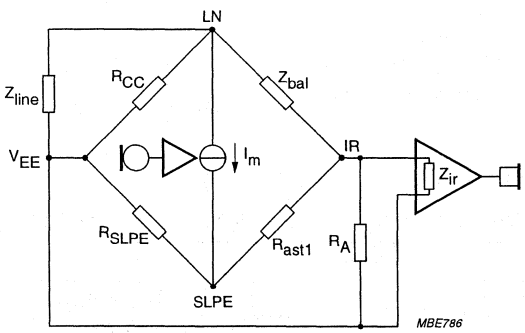


Fig.13 Equivalent circuit of an anti-sidetone network in a Wheatstone bridge configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

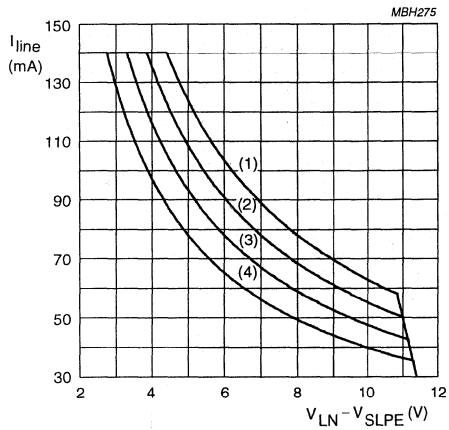
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{LN}	positive continuous line voltage		V_{EE} – 0.4	12	V
	repetitive line voltage during switch-on or line interruption		V_{EE} – 0.4	13.2	V
$V_{n(max)}$	maximum voltage on all pins		V_{EE} – 0.4	V_{CC} + 0.4	V
I_{line}	line current	R_{SLPE} = 20 Ω; see Figs 14 and 15	–	140	mA
P_{tot}	total power dissipation	T_{amb} = 75 °C; see Figs 14 and 15			
	TEA1118T; TEA1118AT		–	384	mW
	TEA1118M; TEA1118AM		–	312	mW
T_{stg}	IC storage temperature		–40	+125	°C
T_{amb}	operating ambient temperature		–25	+75	°C

HANDLING

This device meets class 2 ESD test requirements [Human Body Model (HBM)], in accordance with *"MIL STD 883C - method 3015"*.

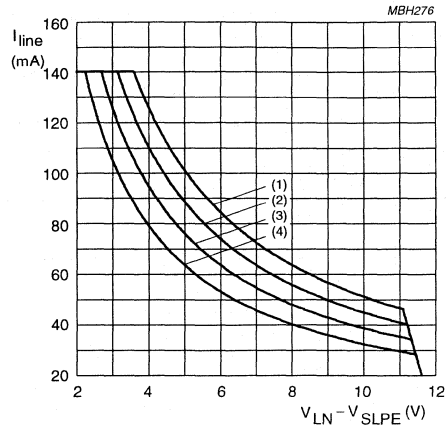
THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air			
	TEA1118T; TEA1118AT		130	K/W
	TEA1118M; TEA1118AM	mounted on epoxy board 40.1 × 19.1 × 1.5 mm	160	K/W



(1) T_{amb} = 45 °C; P_{tot} = 615 mW.
(2) T_{amb} = 55 °C; P_{tot} = 538 mW.
(3) T_{amb} = 65 °C; P_{tot} = 461 mW.
(4) T_{amb} = 75 °C; P_{tot} = 384 mW.

Fig.14 SO14 safe operating area.



(1) T_{amb} = 45 °C; P_{tot} = 500 mW.
(2) T_{amb} = 55 °C; P_{tot} = 437 mW.
(3) T_{amb} = 65 °C; P_{tot} = 375 mW.
(4) T_{amb} = 75 °C; P_{tot} = 312 mW.

Fig.15 SSOP16 safe operating area.

CHARACTERISTICS

I_{line} = 15 mA; V_{EE} = 0 V; R_{SLPE} = 20 Ω; AGC pin connected to V_{EE}; Z_{line} = 600 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies (pins V_{LN}, V_{CC}, SLPE and REG)						
V_{ref}	stabilized voltage between LN and SLPE		3.1	3.35	3.6	V
V_{LN}	DC line voltage	I_{line} = 1 mA	–	1.6	–	V
		I_{line} = 4 mA	–	2.45	–	V
		I_{line} = 15 mA	3.35	3.65	3.95	V
		I_{line} = 140 mA	–	–	6.9	V
$V_{LN(exR)}$	DC line voltage with an external resistor R_{VA}	$R_{VA(SLPE-REG)}$ = 27 kΩ	–	4.4	–	V
$\Delta V_{LN(T)}$	DC line voltage variation with temperature referenced to 25 °C	T_{amb} = −25 to +75 °C	–	±30	–	mV
I_{CC}	internal current consumption	V_{CC} = 2.9 V	–	1.15	1.4	mA
V_{CC}	supply voltage for peripherals	I_P = 0 mA	–	2.9	–	V
R_{CCint}	equivalent supply voltage resistance	I_P = 0.5 mA	–	550	620	Ω

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Transmit amplifier (pins TX+, TX– and GAT)						
$\|Z_i\|$	input impedance					
	differential between pins TX+ and TX–		–	62.5	–	kΩ
	single-ended between pins TX+/TX– and V_{EE}		–	36.5	–	kΩ
G_{vtx}	voltage gain from TX+/TX– to LN	V_{TX} = 200 mV (RMS)	10.1	11.3	12.5	dB
$\Delta G_{vtx(f)}$	gain variation with frequency referred to 1 kHz	f = 300 to 3400 Hz	–	±0.2	–	dB
$\Delta G_{vtx(T)}$	gain variation with temperature referred to 25 °C	T_{amb} = –25 to +75 °C	–	±0.3	–	dB
CMRR	common mode rejection ratio		–	60	–	dB
ΔG_{vtxr}	gain voltage reduction range (TEA1118 only)	external resistor connected between GAT and REG	–	–	6	dB
$V_{LN(max)}$	maximum sending signal (RMS value)	I_{line} = 15 mA; THD = 2%	1.4	1.7	–	V
		I_{line} = 4 mA; THD = 10%	–	0.8	–	V
$V_{TX(max)}$	maximum transmit input voltage (RMS value)	I_{line} = 15 mA; THD = 2%	–	0.45	–	V
		I_{line} = 75 mA; THD = 2%	–	0.9	–	V
V_{notx}	noise output voltage at pin LN; pins TX+/TX– shorted through 200 Ω	psophometrically weighted (P53 curve)	–	–84	–	dBmp
Transmit mute (pin TMUTE; TEA1118A only)						
ΔG_{vtxm}	gain reduction	TMUTE = HIGH	–	80	–	dB
V_{IL}	LOW level input voltage		V_{EE} – 0.4	–	V_{EE} + 0.3	V
V_{IH}	HIGH level input voltage		V_{EE} + 1.5	–	V_{CC} + 0.4	V
I_{TMUTE}	input current	input level = HIGH	–	1.25	3	µA
Receive amplifier (pins IR, QR and GAR)						
$\|Z_i\|$	input impedance		–	20	–	kΩ
G_{vrx}	voltage gain from IR to QR	V_{IR} = 4 mV (RMS)	29.8	31	32.2	dB
$\Delta G_{vrx(f)}$	gain variation with frequency referenced to 1 kHz	f = 300 to 3400 Hz	–	±0.2	–	dB
$\Delta G_{vrx(T)}$	gain variation with temperature referenced to 25 °C	T_{amb} = –25 to +75 °C	–	±0.3	–	dB
ΔG_{vrxr}	gain voltage reduction range	external resistor connected between GAR and QR	–	–	12	dB
$V_{o(rms)}$	maximum receive signal (RMS value)	I_P = 0 mA sine wave drive; R_L = 150 Ω; THD = 2%	–	0.25	–	V
		I_P = 0 mA sine wave drive; R_L = 450 Ω; THD = 2%	–	0.35	–	V
$V_{norx(rms)}$	noise output voltage at pin QR (RMS value)	IR open-circuit; R_L = 150 Ω; psophometrically weighted (P53 curve)				
	TEA1118		–	–89	–	dBVp
	TEA1118A		–	–86	–	dBVp

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Automatic gain control (pin AGC)						
ΔG_{vtrx}	gain control range for transmit and receive amplifiers with respect to I_{line} = 15 mA	I_{line} = 75 mA;	–	5.8	–	dB
I_{start}	highest line current for maximum gain		–	26	–	mA
I_{stop}	lowest line current for minimum gain		–	61	–	mA
DTMF amplifier (pin DTMF; TEA1118A only)						
$\|Z_i\|$	input impedance		–	20	–	kΩ
G_{vdtmf}	voltage gain from DTMF to LN	V_{DTMF} = 100 mV (RMS); MUTE or TMUTE = HIGH	16.2	17.4	18.6	dB
$\Delta G_{vdtmf(f)}$	gain variation with frequency referenced to 1 kHz	f = 300 to 3400 Hz	–	±0.2	–	dB
$\Delta G_{vdtmf(T)}$	gain variation with temperature referenced to 25 °C	T_{amb} = −25 to + 75 °C	–	±0.4	–	dB
G_{vct}	voltage gain from DTMF to QR (confidence tone)	V_{DTMF} = 100 mV (RMS); R_L = 150 Ω	–	−18	–	dB
Mute function (pin MUTE; TEA1118A only)						
V_{IL}	LOW level input voltage		V_{EE} − 0.4	–	V_{EE} + 0.3	V
V_{IH}	HIGH level input voltage		V_{EE} + 1.5	–	V_{CC} + 0.4	V
I_{MUTE}	input current	input level = HIGH	–	1.25	3	µA
ΔG_{trxm}	gain reduction for transmit and receive amplifiers	MUTE = HIGH	–	80	–	dB

APPLICATION INFORMATION

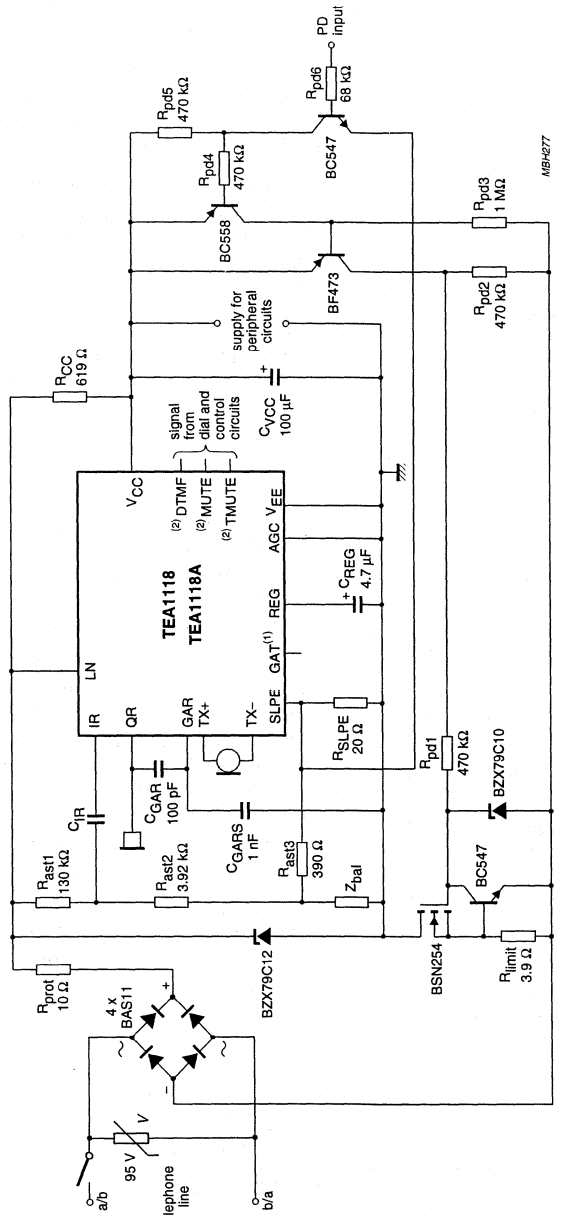


Fig.16 Typical application of the TEA1118 and TEA1118A in sets with pulse dialling or flash facilities.

(1) TEA1118 only.
(2) TEA1118A only.

Image reject 1800 MHz transceiver for DECT applications

UAA2067G

FEATURES

- Receiver with:
  - low noise amplifier
  - dual quadrature mixers for image rejection (lower sideband)
  - I and Q combining networks at a fixed IF
- Both high-frequency and low-frequency VCOs including buffers with good isolation for low pulling
- Transmitter with:
  - dual quadrature mixers for image rejection (lower sideband)
  - amplitude ramping circuit
  - amplifier with high output power.

APPLICATIONS

- 1800 MHz transceiver for DECT hand-portable equipment
- TDMA systems.

GENERAL DESCRIPTION

The UAA2067G is a low-power transceiver intended for use in portable and base station transceivers complying with the DECT system. The IC performs in accordance with specifications in the –30 to +85°C temperature range.

The UAA2067G contains a front-end receiver for the 1800 to 1900 MHz frequency range, a high-frequency VCO for the 1650 to 1850 MHz range, a low-frequency VCO for the 100 to 140 MHz frequency range and a transmitter with a high-output power amplifier driver stage for the 1800 to 1900 MHz frequency range. Designed in an advanced BiCMOS process, it combines high performance with low-power consumption and a high degree of integration, thus reducing external component costs and total radio size.

Its first advantage is to provide typically 34 dB of image rejection in the receiver path. Thus, the image filter between the LNA and the mixer is redundant and consequently can be removed. The receive section consists of a low-noise amplifier that drives a quadrature mixer pair. Image rejection is achieved by this RF mixer pair and the two phase shifters in the I and Q channels that phase shift the IF by 45° and 135° respectively. The two phase shifted IFs are recombined and buffered to furnish the IF output signal.

Signals presented at the RF input at LO – IF frequency are rejected through this signal processing while signals at LO + IF frequency can form the IF signal.

Its second advantage is to provide a good buffered high-frequency VCO signal to the RX and TX mixers and to the synthesizer-prescaler. Switching the receive or transmit section **on** gives a very small change in VCO frequency.

Its third advantage is to provide a good buffered low-frequency VCO signal to the TX mixers, to the synthesizer-prescaler and the second down conversion mixer in a double conversion receiver. Switching the transmit section **on** gives a very small change in VCO frequency.

The frequency of each VCO is determined by a resonator network that is external to the IC. Each VCO has a regulated power supply voltage that has been designed specifically for minimizing a change in frequency due to changes in the power supply voltage, which may be caused for instance by switching **on** the power amplifier.

Its fourth advantage is to provide typically 33 dBc of image rejection in the single-sideband up-conversion mixer. Thus the image filter between the power amplifier and the antenna is redundant and may consequently be removed. Image rejection is achieved in the internal architecture by two RF mixers in quadrature and two phase shifters in the low-frequency VCO signal that shifts the phase to 0° and 90°. The output signals of the mixers are summed to form the single-upper-sideband output signal.

The output stage is a high-level output buffer with an output power of approximately 4 dBm. The output level is sufficient to drive a three-stage bipolar preamplifier for DECT.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UAA2067G	LQFP32	plastic low profile quad flat package; 32 leads; body 5 × 5 × 1.4 mm	SOT401-1

QUICK REFERENCE DATA

For conditions see Chapters "DC characteristics" and "AC characteristics".

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	3.0	3.6	5.5	V
$I_{CC(RX)}$	receive supply current	–	24	–	mA
$I_{CC(TX)}$	transmit supply current	–	42	–	mA
$I_{CC(RFLO)}$	RF oscillator supply current	–	15	–	mA
$I_{CC(IFLO)}$	IF oscillator supply current	–	7	–	mA
NF_{RX}	receive noise figure	–	–	7.0	dB
G_{CP}	conversion power gain	–	30	–	dB
IR_{RX}	receive image frequency rejection	–	34	–	dB
f_{RFLO}	RFLO frequency range	1.65	–	1.85	GHz
f_{IFLO}	IFLO frequency range	100	–	140	MHz
P_{out}	output transmit power	–	4	–	dBm
IR_{TX}	transmit image frequency rejection	–	33	–	dBc
T_{amb}	operating ambient temperature	–30	+25	+85	°C

BLOCK DIAGRAM

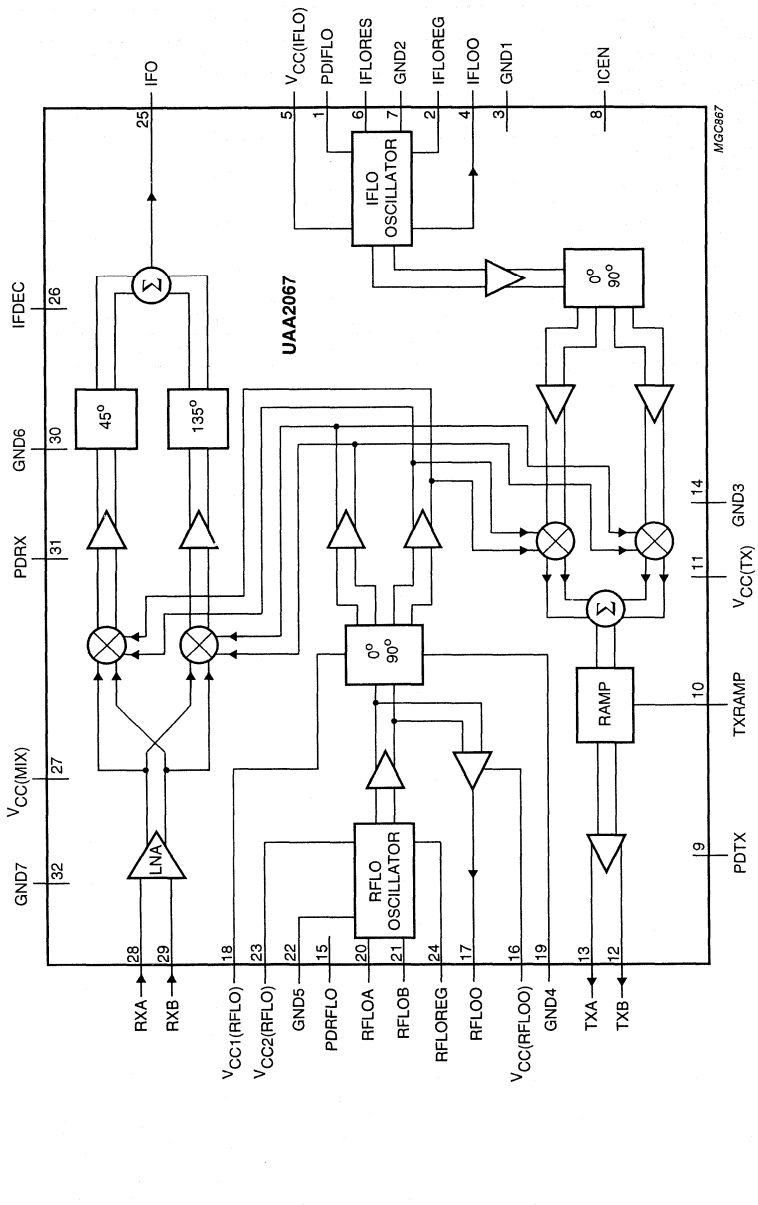


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
PDIFLO	1	power-down for IFLO
IFLOREG	2	regulator decoupling for IFLO
GND1	3	ground for IFLO; note 1
IFLOO	4	IFLO output
$V_{CC(IFLO)}$	5	supply voltage for IFLO
IFLORES	6	IFLO resonator
GND2	7	ground for IFLO resonator; note 1
ICEN	8	IC enable
PDTX	9	power-down for transmitter
TXRAMP	10	power ramping transmitter
$V_{CC(TX)}$	11	supply voltage for transmitter output stage; note 2
TXB	12	transmitter RF output B
TXA	13	transmitter RF output A
GND3	14	ground for transmitter output stage
PDRFLO	15	power-down for RFLO
$V_{CC(RFLOO)}$	16	supply voltage for RFLO output
RFLOO	17	RFLO output
$V_{CC1(RFLO)}$	18	supply voltage for RFLO oscillator; note 3
GND4	19	ground for RFLO oscillator; note 4
RFLOA	20	RFLO resonator
RFLOB	21	RFLO resonator
GND5	22	ground for RFLO oscillator; note 4
$V_{CC2(RFLO)}$	23	supply voltage for RFLO oscillator; note 3
RFLOREG	24	regulator decoupling for RFLO
IFO	25	receiver IF output
IFDEC	26	IF decoupling
$V_{CC(MIX)}$	27	supply voltage for receive and transmit mixers; note 2
RXA	28	receiver RF input A
RXB	29	receiver RF input B
GND6	30	ground for receive and transmit mixers
PDRX	31	power-down for receiver
GND7	32	die-pad ground

Notes

1. Pins 3 and 7 are internally short-circuited.
2. Pins 11 and 27 should be at the same DC voltage.
3. Pins 18 and 23 are internally short-circuited.
4. Pins 19 and 22 are internally short-circuited.

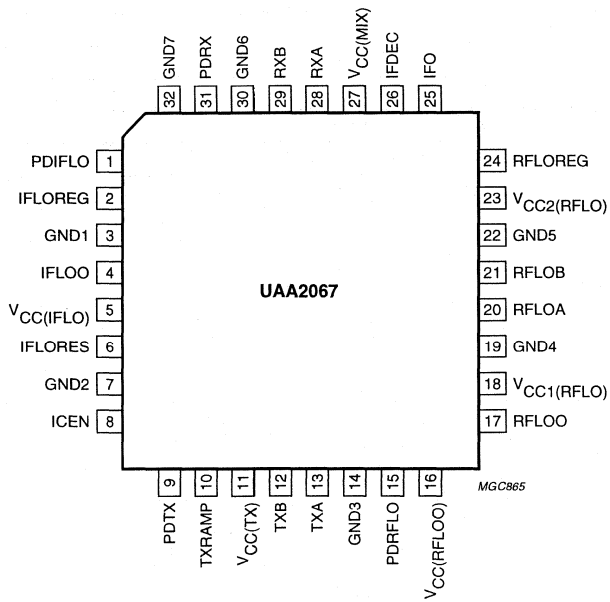


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Receive section

The circuit contains a balanced low-noise amplifier followed by two high dynamic range mixers. The local oscillator signals, shifted in phase to 0 and 90° mix the amplified RF signal to the I and Q channels.These two channels are buffered, phase shifted by 45° and 135° respectively, amplified and recombined internally to realize the image rejection. Signals at the RF input at RFLO – IF frequencies are rejected through the signal processing while signals at the RFLO + IF frequencies form the IF signals.

An image rejection of typically 34 dB is obtained for an IF between 100 and 120 MHz.

Balanced signals are used for minimizing crosstalk due to package parasitics. The IF output is single-ended. The typical load is 50 Ω.

Fast switching, **on/off** of the receive section is controlled by the hardware input PDRX.

RFLO section

The high-frequency oscillator (RFLO oscillator) supplies the local oscillator signal for the down-conversion (receive) and up-conversion (transmit) mixers. This VCO uses an on-chip regulator for a power-supply voltage-independent output frequency. The buffered VCO signal is fed into a phase shifter and an off-chip prescaler-synthesizer. The output signal of the phase-shifter is used for driving the RX and TX mixers. Due to the good isolation in the buffer stages, a very small change in VCO frequency is obtained when switching the RX and TX mixers **on**.

Fast switching, **on/off** of the oscillator section is controlled by the hardware input PDRFLO.

IFLO section

The low-frequency oscillator (IFLO oscillator) internally supplies the local oscillator signal to the single-sideband transmit mixer. The buffered VCO signal is fed into a phase shifter. The output signal of the phase-shifter is used for driving the TX mixers.

Due to the good isolation in the buffer stages, a very small change in VCO frequency is obtained when switching the TX mixer **on**.

Fast switching **on/off** of the oscillator section is controlled by the hardware input PDIFLO input.

Transmit section

The circuit contains two balanced mixers, each of which is driven by the RFLO and IFLO signals. The output signal of the two mixers is summed and buffered to obtain the single upper-sideband signal at frequency RFLO + IFLO.

With the use of an off-chip time constant, the ramping circuit defines the power ramp-up and ramp-down of the pre-amplifier output signal.

Balanced signals are used for minimizing crosstalk due to package parasitics.

Fast switching, **on/off**, of the transmit section is controlled by the hardware input PDTX.

The power supply voltage of the transmit mixers, the adding circuit and ramping circuit is taken from the $V_{CC(MIX)}$ and GND6 for maximum isolation from the preamplifier output stage.

OPERATING MODES

To use the IC, **all** V_{CC} pins must be connected to the supply voltage.

For transceiving a DECT signal, the RFLO and IFLO sections should be powered-on. After a stable frequency has been reached (mainly determined by the synthesizer design), the receiver or transmitter can be powered-on.

GMSK data modulation can be supplied in two different ways: the data is directly modulated on IFLO or RFLO.

The ramping of the power level can be set with a time constant that is external to the IC.

Table 1 gives the definition of the polarity of the switching signals on the receive, the RFLO, the IFLO and the transmit sections.

ing signals on the receiver

SIGNAL	SECTION	LEVEL	on/off
PDRX	receive section powered-on	LOW	on(1)
	receive section powered-off	HIGH	off
PDRFLO	RFLO section powered-on	LOW	on(1)
	RFLO section powered-off	HIGH	off
PDIFLO	IFLO section powered-on	LOW	on(1)
	IFLO section powered-off	HIGH	off
PDTX	transmit section powered-on	LOW	on(1)
	transmit section powered-off	HIGH	off
ICEN	all sections disabled	LOW	off
	all sections enabled	HIGH	on

Note

1. Active when ICEN is enabled.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–	6	V
ΔGND	difference in ground supply voltage applied between all grounds	note 1	–	+ 0.3	V
$P_{I(max)}$	maximum power input		–	+20	dBm
$T_{j(max)}$	maximum operating junction temperature		–	+150	°C
$P_{dis(max)}$	maximum power dissipation in stagnant air at 25°C		–	500	mW
T_{stg}	storage temperature		–65	+150	°C

Note

1. Pins short-circuited internally must be short-circuited externally.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	90	K/W

HANDLING

Every pin withstands the ESD test in accordance with *"MIL-STD-883C class 2 (method 3015.5)"*.

DC CHARACTERISTICS

V_{CC} = 3.6 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pins: $V_{CC(MIX)}$, $V_{CC(TX)}$, $V_{CC(IFLO)}$, $V_{CC1(RFLO)}$, $V_{CC2(RFLO)}$ and $V_{CC(RFLOO)}$						
V_{CC}	supply voltage	over full temperature range	3.0	3.6	5.5	V
$I_{CC(RX)}$	supply current	receive section **on**; DC tested	18	24	30	mA
$I_{CC(RFLO)}$	supply current RFLO	RFLO section **on**; DC tested	11	15	20	mA
$I_{CC(IFLO)}$	supply current IFLO	IFLO section **on**; DC tested	5	7	9	mA
$I_{CC(TX)}$	supply current	transmit section **on**; DC tested	34	42	54	mA
$I_{CC(PD)}$	supply current	power-down mode; DC tested	–	2	50	µA
Pins: PDRX, PDTX, PDRFLO, PDIFLO and ICEN						
V_{IH}	HIGH level input voltage		2.1	–	V_{CC} + 0.3	V
V_{IL}	LOW level input voltage		−0.3	–	0.8	V
I_{IH}	HIGH level static input current	pin at V_{CC} − 0.4 V	−1	–	+1	µA
I_{IL}	LOW level static input current	pin at 0.4 V	−1	–	+1	µA
Pins: RXA, RXB, IFO and IFDEC						
$V_{RXA,B}$	DC input voltage level	receive section **on**	2.1	2.4	2.7	V
V_{IFO}	DC output voltage level	receive section **on**	0.9	1.1	1.3	V
V_{IFDEC}	DC level	receive section **on**	2.45	2.65	2.85	V
Pins: RFLOA, RFLOB, RFLOREG and RFLOO						
$I_{RFLOA,B}$	DC current	RFLO section **on**	1	2	3	mA
$V_{RFLOREG}$	DC level	RFLO section **on**	2.45	2.65	2.85	V
V_{RFLOO}	DC output voltage level	RFLO section **on**	2.8	3.1	3.4	V
Pins: IFLORES, IFLOREG and IFLOO						
$V_{IFLORES}$	DC level	IFLO section **on**	1.85	2.1	2.3	V
$V_{IFLOREG}$	DC level	IFLO section **on**	2.35	2.55	2.8	V
V_{IFLOO}	DC output voltage level	IFLO section **on**	2.2	2.45	2.7	V
Pins: TXA, TXB and TXRAMP						
$I_{TXA,B}$	DC output current	transmit section **on**	2	10	18	mA
I_{TXRAMP}	DC input current	V_{TXRAMP} = 3 V; transmit section **on**	–	–	200	µA

AC CHARACTERISTICS

V_{CC} = 3.0 to 5.5 V; T_{amb} = –30 to +85°C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Receive mode (receive and RFLO sections powered-on)						
f_{RFI}	RF input frequency		1800	–	1900	MHz
R_{iRF}	RF input resistance (real part of the parallel input impedance)	balanced; at 1890 MHz	–	190	–	Ω
C_{iRF}	RF input capacitance (imaginary part of the parallel input impedance)	balanced; at 1890 MHz	–	0.8	–	pF
$PRFLO_{RX}$	RFLO level at input to RX balun	note 1	–	–70	–40	dBm
$DES3_{RX}$	RF interference for 3 dB desensitization	interference frequency offset 6 MHz; note 1	–	–35	–	dBm
G_{CP}	conversion power gain	RF input to IF output (typical load)				
		over full temperature range	24	30	36	dB
		T_{amb} = 25 °C	27	30	33	dB
$CP1_{RX}$	1 dB input compression point	referenced to RF input; note 1	–36	–33	–	dBm
$P_{o(RX)}$	IF power for $CP1_{RX} < P_{in} < +8$ dBm	referenced to IF power at $CP1_{RX}$; note 1	–6	–	+6	dB
t_{rec}	recovery time for P_{in} = +12 dBm	note 1	–	2	30	µs
$IP2\text{-}2_{RX}$	mixer 2-2 spurious intercept point	referenced to the RF input; note 1	–6	+2	–	dBm
$IP3_{RX}$	3rd order intercept point	referenced to the RF input; note 1	–30	–25	–	dBm
NF_{RX}	overall noise figure	RF input to IF output; note 1	–	5.8	7	dB
f_{IF}	IF frequency range		100	110	120	MHz
$Z_{L(IF)}$	typical application IF output load impedance	f_{IF} = 110 MHz	–	50	–	Ω
IR_{RX}	image frequency rejection	over full temperature range	20	34	–	dB
		T_{amb} = 25 °C	23	34	–	dB
PSRR	power supply rejection ratio	note 1; typical load; at 110 MHz	35	–	–	dB

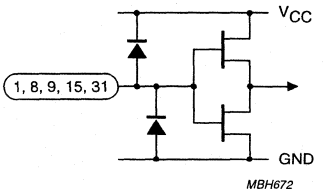
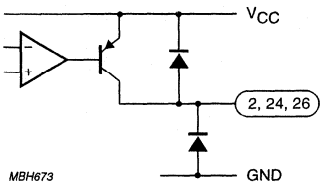
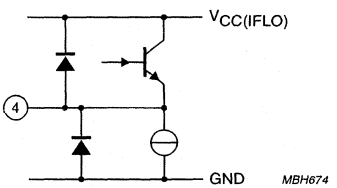
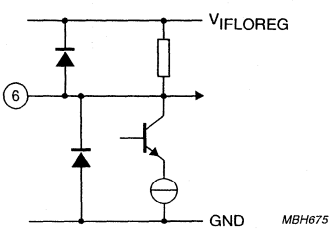
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RF local oscillator (RFLO section powered-on)						
$f_{RFLO(min)}$	minimum oscillator frequency range		1650	–	1850	MHz
$R_{i(RFLO)}$	oscillator input resistance (real part of the parallel input impedance)	balanced; at 1.77 GHz	–	–250	–	Ω
$C_{i(RFLO)}$	oscillator input capacitance (imaginary part of the parallel input impedance)	balanced; at 1.77 GHz	–	2.7	–	pF
$V_{o(RFLO)}$	local oscillator output level at pin 17; RMS value	note 2; typical load resistance	50	75	–	mV
$Z_{o(RFLO)}$	local oscillator output impedance at pin 17	at 1.77 GHz	–	30 – 60j	–	Ω
$R_{L(RFLO)}$	typical load resistance		–	300	–	Ω
$HAR_{(RFLO)}$	harmonic levels at RFLO output (pin 17)	note 1	–	–	–20	dBc
IF local oscillator (IFLO section powered-on)						
$f_{IFLO(min)}$	minimum oscillator frequency range		100	120	140	MHz
$R_{i(IFLO)}$	oscillator input resistance (real part of the parallel input impedance)		–	–480	–	Ω
$C_{i(IFLO)}$	oscillator input capacitance (imaginary part of the parallel input impedance)		–	2.1	–	pF
$V_{o(IFLO)}$	IF local oscillator output level at pin 4; RMS value		100	160	–	mV
$Z_{o(IFLO)}$	local oscillator output impedance (real part)		–	–	100	Ω
$R_{L(IFLO)}$	typical load resistance		–	5	–	kΩ
$C_{L(IFLO)}$	typical load capacitance		–	7	–	pF
$HAR_{(IFLO)}$	harmonic levels at IFLO output	note 1	–	–	–15	dBc

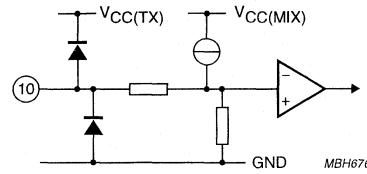
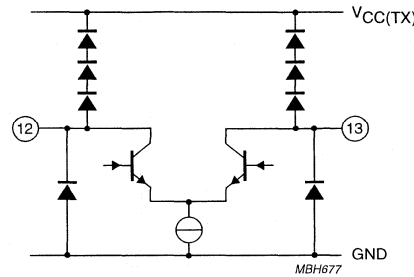
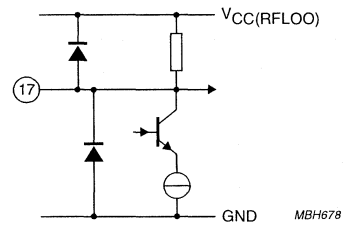
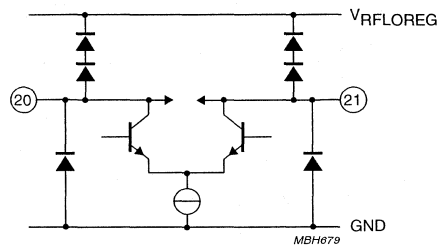
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Transmit mode (transmit, RFLO and IFLO sections powered-on)						
f_{TX}	RF output frequency		1800	–	1900	MHz
$R_{o(TX)}$	RF output resistance (real part of the parallel output impedance)	balanced; note 1	–	110	–	Ω
$C_{o(TX)}$	RF output capacitance (imaginary part of the parallel output impedance)	balanced; note 1	–	0.6	–	pF
$FTRFLO_{TX}$	RFLO feedthrough at the TX output	referenced to the desired frequency; T_{amb} = 25 °C; note 1	–	–25	–23	dBc
Pout	output transmit power	V_{TXRAMP} = 0 V; note 1				
		over full temperature range	–2	4	8	dBm
		T_{amb} = 25 °C	1	4	7	dBm
IR_{TX}	image frequency rejection	referenced to the desired frequency; note 1				
		over full temperature range	20	33	–	dBc
		T_{amb} = 25 °C	23	33	–	dBc
$Z_{inTXRAMP}$	input impedance at pin TXRAMP		10	–	–	kΩ
$C_{inTXRAMP}$	input capacitance at pin TXRAMP		–	–	10	pF
$V_{TXRAMP(max)}$	ramp voltage for $P_{out} = P_{max}$		–	0		V
$V_{TXRAMP(min)}$	ramp voltage for $P_{out} = P_{max} - 30$ dB		–	3.0	–	V
CNR_{TX}	carrier-to-noise ratio at TX output	T_{amb} = 25 °C; notes 1 and 3	+130	+133	–	dBc/Hz
Timing						
t_{up}	start-up/power-down time of each block	over full temperature range	–	5	10	µs
C_i	input capacitance of logic inputs	over full temperature range	–	–	5	pF

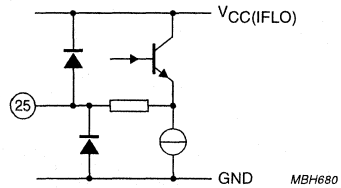
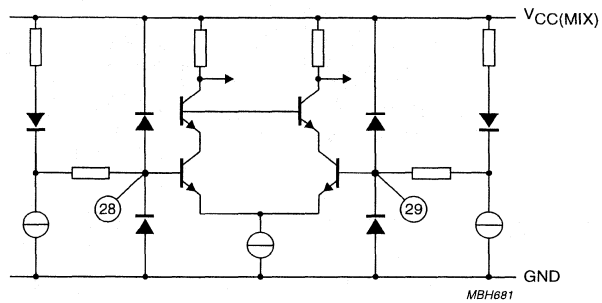
Notes

1. Measured and guaranteed only on the Philips demonstration board, including PCB and balun.
2. The imaginary part of the load impedance has been tuned out. A power match is assumed.
3. A simplified DECT type approval measurement is used; the spectrum analyser has the following settings: RBW = 100 kHz, VBW = 100 Hz, use delta marker and add 50 dB (correction for RBW = 100 kHz), f_{RFLO} = 1.77 GHz and f_{IFLO} = 120 MHz, Δf = 4.686 MHz.

INTERNAL PIN CONFIGURATION

SYMBOL	PIN	DC VOLTAGE (V)	EQUIVALENT CIRCUIT
PDIFLO	1	–	
ICEN	8	–	
PDTX	9	–	
PDRFLO	15	–	
PDRX	31	–	
IFLOREG	2	2.55	
RFLOREG	24	2.65	
IFDEC	26	2.65	
GND	3, 7, 14, 19, 22, 30, 32	0	
IFLOO	4	2.45	
V_{CC}	5, 11, 16, 18, 23, 27	3.6	
IFLORES	6	2.1	

SYMBOL	PIN	DC VOLTAGE (V)	EQUIVALENT CIRCUIT
TXRAMP	10	–	
TXB	12	V_{CC}	
TXA	13	V_{CC}	
RFLOO	17	3.1	
RFLOA	20	2.0	
RFLOB	21	2.0	

SYMBOL	PIN	DC VOLTAGE (V)	EQUIVALENT CIRCUIT
IFO	25	1.1	
RXA	28	2.4	
RXB	29	2.4	

APPLICATION INFORMATION

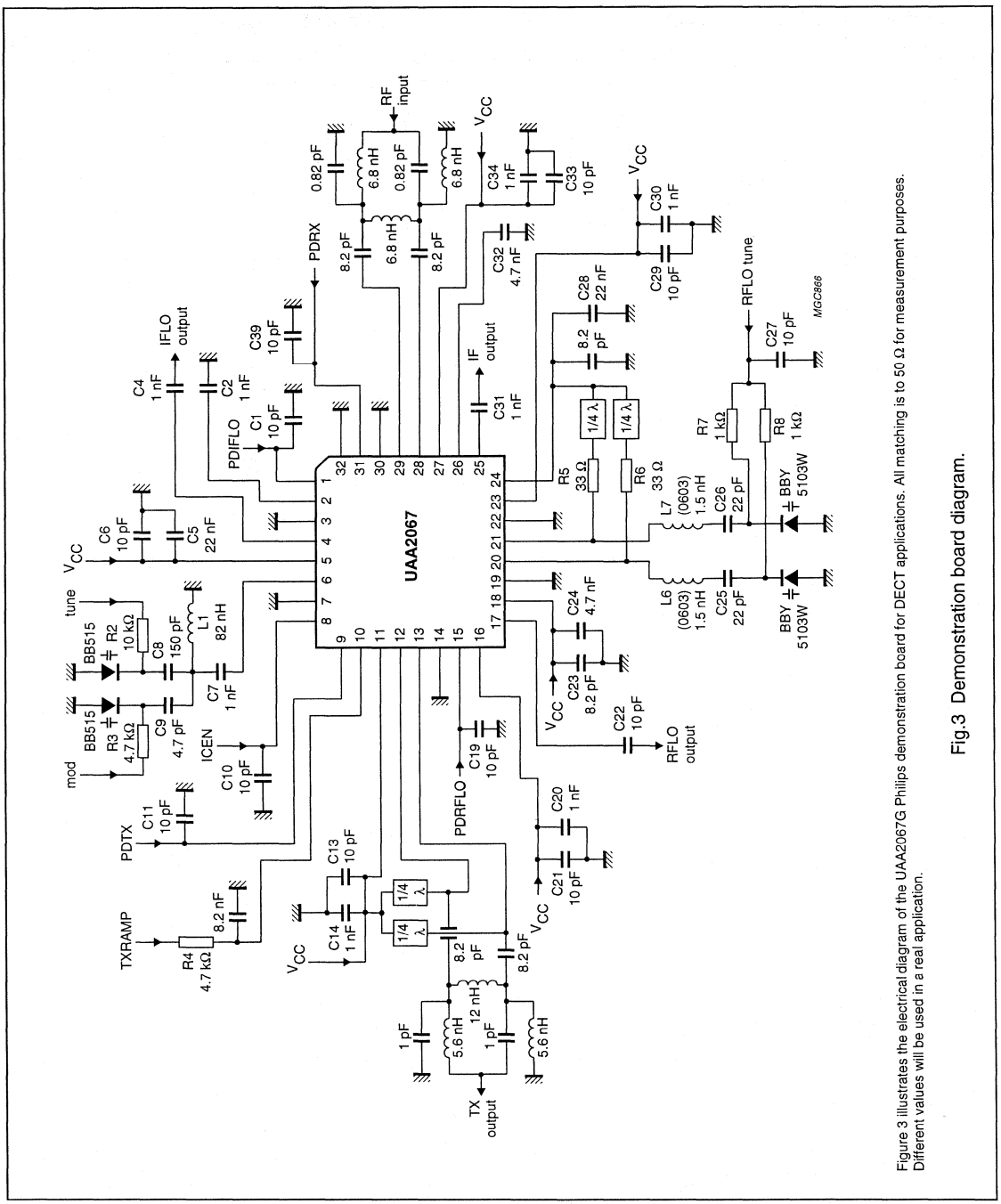


Fig.3 Demonstration board diagram.

Figure 3 illustrates the electrical diagram of the UAA2067G Philips demonstration board for DECT applications. All matching is to 50 Ω for measurement purposes. Different values will be used in a real application.

Application-indicative values

Measured on the Philips demonstration board, including PCB and balun at T_{amb} = 25 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RF local oscillator (RFLO section powered-on)						
CNR_{RFLO}	carrier-to-noise ratio	Δf = 864 kHz	–	117	–	dBc/Hz
		Δf = 2500 kHz	–	128	–	dBc/Hz
		Δf = 4686 kHz	–	134	–	dBc/Hz
$PULL_{RFLO}$	pulling due to enabling RX or TX	V_{TXRAMP} = 3 V	–	5	–	kHz
$SHIFT_{RFLO}$	frequency shift due to 200 mV V_{CC} change		–	5	–	kHz
IF local oscillator (IFLO section powered-on)						
CNR_{IFLO}	carrier-to-noise ratio	Δf = 4686 kHz	–	140	–	dBc/Hz
$SPUR_{IFLO}$	spurious signal modulation due to 0.5 mV (RMS value) on the power supply	Δf = 4686 kHz; measured at TX output	–	–60	–	dBc
$PULL_{IFLO}$	pulling due to enabling TX		–	1	–	kHz
$SHIFT_{IFLO}$	frequency shift due to 200 mV V_{CC} change		–	2.5	–	kHz
Transmit mode (transmit, RFLO and IFLO sections powered-on)						
$PSRR_{TX}$	spurious signal modulation due to 0.5 mV (RMS value) on $V_{CC(MIX)}$, $V_{CC(TX)}$ and $V_{CC(RFLO)}$ only	Δf = 4686 kHz; note 1	–	–74	–	dBc
$SPUR_{TX}$	spurious signals	RFLO – 3IFLO	–	–40	–	dBc
		RFLO + 2IFLO	–	–35	–	dBc
		RFLO + 5IFLO	–	–51	–	dBc
N_{TX}	white noise level at the output		–	135	–	dBc/Hz

Note

1. Including PSRR of the RFLO circuitry.

Image rejecting front-end for GSM applications

UAA2073AM

FEATURES

- Low-noise, wide dynamic range amplifier
- Very low noise figure
- Dual balanced mixer for at least 30 dB on-chip image rejection
- IF I/Q combination network for 175 MHz
- Down-conversion mixer for closed-loop transmitters
- Independent TX/RX fast **on/off** power-down modes
- Very small outline packaging
- Very small application (no image filter).

APPLICATIONS

- 900 MHz front-end for GSM hand-portable equipment
- Compact digital mobile communication equipment
- TDMA receivers.

GENERAL DESCRIPTION

UAA2073AM contains both a receiver front-end and a high frequency transmit mixer intended for GSM (Global System for Mobile communications) cellular telephones. Designed in an advanced BiCMOS process it combines high performance with low power consumption and a high degree of integration, thus reducing external component costs and total front-end size.

The main advantage of the UAA2073AM is its ability to provide over 30 dB of image rejection. Consequently, the image filter between the LNA and the mixer is suppressed and the duplexer design is eased, compared with a conventional front-end design.

Image rejection is achieved in the internal architecture by two RF mixers in quadrature and two all-pass filters in I and Q IF channels that phase shift the IF by 45° and 135° respectively. The two phase shifted IFs are recombined and buffered to furnish the IF output signal.

This means that signals presented at the RF input at LO – IF frequency are rejected through this signal processing while signals at LO + IF frequency can form the IF signal.

The receiver section consists of a low-noise amplifier that drives a quadrature mixer pair. The IF amplifier has on-chip 45° and 135° phase shifting and a combining network for image rejection.The IF driver has differential open-collector type outputs.

The LO part consists of an internal all-pass type phase shifter to provide quadrature LO signals to the receive mixers. The all-pass filters outputs are buffered before being fed to the receive mixers.

The transmit section consists of a down-conversion mixer and a transmit IF driver stage. In the transmit mode an internal LO buffer is used to drive the transmit IF down-conversion mixer.

All RF and IF inputs or outputs are balanced to reduce EMC issues.

Fast power-up switching is possible. A synthesizer-on (SX) mode enables LO buffers independent of the other circuits. When SXON pin is HIGH, all internal buffers on the LO path of the circuit are turned **on**, thus minimizing LO pulling when remainder of receive chain is powered-up.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UAA2073AM	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

QUICK REFERENCE DATA

Note 1.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	3.6	3.75	5.3	V
$I_{CC(RX)}$	receive supply current	21	26	32	mA
$I_{CC(TX)}$	transmit supply current	9	12	15	mA
NF_{RX}	noise figure on demonstration board (including matching and PCB losses)	–	3.6	4.7	dB
G_{CPRX}	conversion power gain	19	22	25	dB
IR	image frequency rejection	30	45	–	dB
T_{amb}	operating ambient temperature	−30	+25	+75	°C

Note

1. For conditions see Chapters "DC characteristics" and "AC characteristics".

BLOCK DIAGRAM

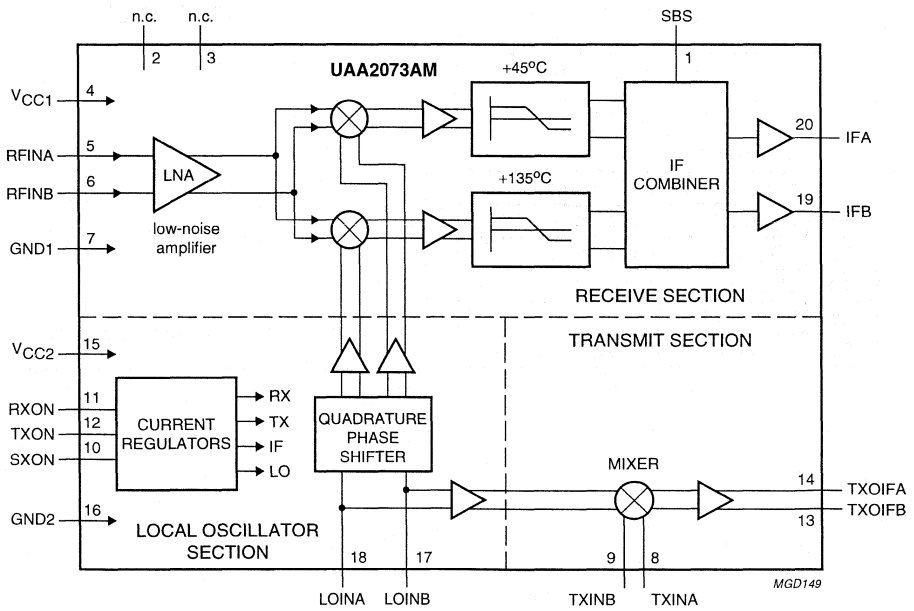


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SBS	1	sideband selection (should be grounded for $f_{LO} < f_{RF}$)
n.c.	2	not connected
n.c.	3	not connected
V_{CC1}	4	supply voltage for receive and transmit sections
RFINA	5	RF input A (balanced)
RFINB	6	RF input B (balanced)
GND1	7	ground 1 for receive and transmit sections
TXINA	8	transmit mixer input A (balanced)
TXINB	9	transmit mixer input B (balanced)
SXON	10	hardware power-on of LO section (including buffers to RX and TX)
RXON	11	hardware power-on for receive section and LO buffers to RX
TXON	12	hardware power-on for transmit section and LO buffers to TX
TXOIFB	13	transmit mixer IF output B (balanced)
TXOIFA	14	transmit mixer IF output A (balanced)
V_{CC2}	15	supply voltage for LO section
GND2	16	ground 2 for LO section
LOINB	17	LO input B (balanced)
LOINA	18	LO input A (balanced)
IFB	19	IF output B (balanced)
IFA	20	IF output A (balanced)

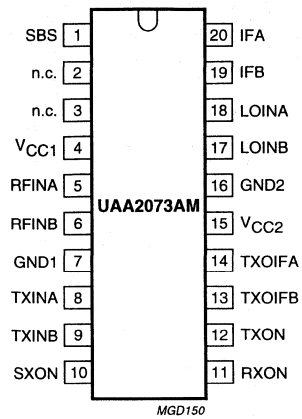


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Receive section

The circuit contains a low-noise amplifier followed by two high dynamic range mixers. These mixers are of the Gilbert-cell type. The whole internal architecture is fully differential.

The local oscillator, shifted in phase to 45° and 135°, mixes the amplified RF to create I and Q channels. The two I and Q channels are buffered, phase shifted by 45° and 135° respectively, amplified and recombined internally to realize the image rejection.

Pin SBS allows sideband selection:

- $f_{LO} > f_{RF}$ (SBS = 1)
- $f_{LO} < f_{RF}$ (SBS = 0).

Where f_{RF} is the frequency of the wanted signal.

Balanced signal interfaces are used for minimizing crosstalk due to package parasitics. The RF differential input impedance is 150 Ω (parallel real part), chosen to minimize current consumption at best noise performance.

The IF output is differential and of the open-collector type, tuned for 175 MHz. Typical application will load the output with a 680 Ω resistor load at each IF output, plus a 1 kΩ load consisting in the input impedance of the IF filter or in the input impedance of the matching network for the IF filter. The power gain refers to the available power on this 1 kΩ load. The path to V_{CC} for the DC current should be achieved via tuning inductors. The output voltage is limited to $V_{CC} + 3V_{be}$ or 3 diode forward voltage drops.

Fast switching, **on/off**, of the receive section is controlled by the hardware input RXON.

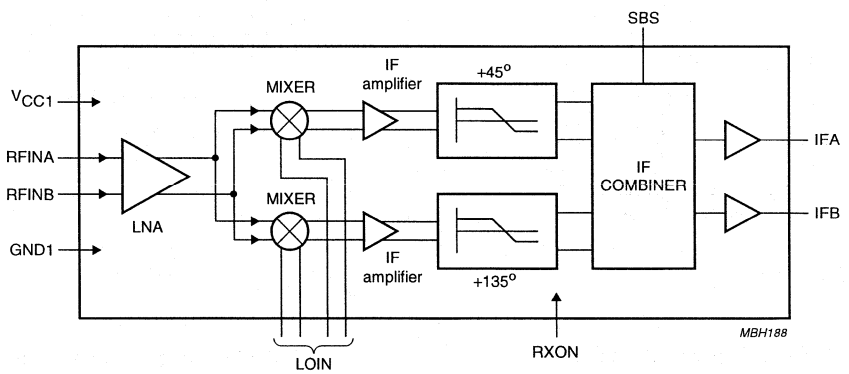


Fig.3 Block diagram, receive section.

Local oscillator section

The Local Oscillator (LO) input directly drives the two internal all-pass networks to provide quadrature LO to the receive mixers.

The LO differential input impedance is 50 Ω (parallel real part).

A synthesizer-on (SX) mode is used to power-up the buffering on the LO inputs, minimizing the pulling effect on the external VCO when entering transmit or receive modes.

This mode is active when the SXON input is HIGH. Table 1 shows status of circuit in accordance with TXON, RXON and SXON inputs.

Transmit mixer

This mixer is used for down-conversion to the transmit IF. Its inputs are coupled to the transmit RF and down-convert it to a modulated transmit IF frequency which is phase locked with the baseband modulation.

The transmit mixer provides a differential input at 200 Ω and a differential output driver buffer for a 1 kΩ load. The IF outputs are low impedance (emitter followers).

Fast switching, **on/off**, of the transmit section is controlled by the hardware input TXON.

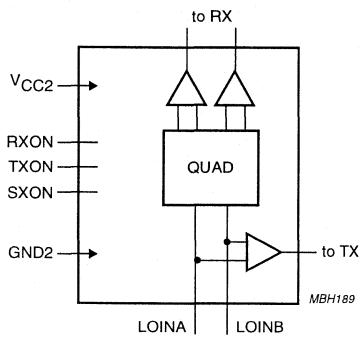


Fig.4 Block diagram, LO section.

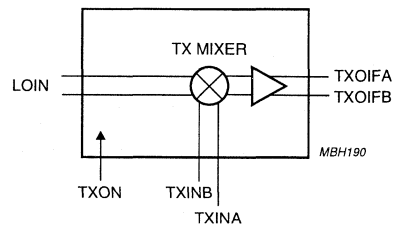


Fig.5 Block diagram, transmit mixer.

Table 1 Control of power status

EXTERNAL PIN LEVEL			CIRCUIT MODE OF OPERATION
TXON	RXON	SXON	
LOW	LOW	LOW	power-down mode
LOW	HIGH	LOW	RX mode: receive section and LO buffers to RX **on**
HIGH	LOW	LOW	TX mode: transmit section and LO buffers to TX **on**
LOW	LOW	HIGH	SX mode: complete LO section **on**
LOW	HIGH	HIGH	SRX mode: receive section **on** and SX mode active
HIGH	LOW	HIGH	STX mode: transmit section **on** and SX mode active
HIGH	HIGH	LOW	receive and transmit sections **on**; specification not guaranteed
HIGH	HIGH	HIGH	receive and transmit sections **on**; specification not guaranteed

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	–	9	V
ΔGND	difference in ground supply voltage applied between GND1 and GND2	–	0.6	V
$P_{i(max)}$	maximum power input	–	+20	dBm
$T_{j(max)}$	maximum operating junction temperature	–	+150	°C
$P_{dis(max)}$	maximum power dissipation in stagnant air	–	250	mW
T_{stg}	IC storage temperature	–65	+150	°C

HANDLING

Every pin withstands the ESD test in accordance with MIL-STD-883C class 2 (method 3015.5).

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	120	K/W

DC CHARACTERISTICS

V_{CC} = 3.75 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pins: V_{CC1} and V_{CC2}						
V_{CC}	supply voltage	over full temperature range	3.6	3.75	5.3	V
$I_{CC(RX)}$	supply current in RX mode		21	26	32	mA
$I_{CC(TX)}$	supply current in TX mode		9	12	15	mA
$I_{CC(SX)}$	supply current in SX mode		4.5	5.8	7.0	mA
$I_{CC(SRX)}$	supply current in SRX mode		23	28	34	mA
$I_{CC(STX)}$	supply current in STX mode		12.5	15.0	19.5	mA
$I_{CC(PD)}$	supply current in power-down mode		–	0.01	50	µA
Pins: SXON, RXON, TXON and SBS						
V_{th}	CMOS threshold voltage	note 1	–	1.25	–	V
V_{IH}	HIGH level input voltage		$0.7V_{CC}$	–	V_{CC}	V
V_{IL}	LOW level input voltage		–0.3	–	0.8	V
I_{IH}	HIGH level static input current	pin at V_{CC} – 0.4 V	–1	–	+1	µA
I_{IL}	LOW level static input current	pin at 0.4 V	–1	–	+1	µA
Pins: RFINA and RFINB						
$V_{I(RFIN)}$	DC input voltage level	receive section **on**	2.0	2.2	2.4	V
Pins: IFA and IFB						
$I_{O(IF)}$	DC output current	receive section **on**	2.3	3.0	3.8	mA
Pins: TXINA and TXINB						
$V_{I(TXIN)}$	DC input voltage level	transmit section **on**	2.1	2.4	2.6	V
Pins: TXOIFA and TXOIFB						
$V_{O(TXOIF)}$	DC output voltage level	transmit section **on**	1.8	1.9	2.1	V
Pins: LOINA and LOINB						
$V_{I(LOIN)}$	DC input voltage level	receive section **on**	2.3	2.5	2.8	V
		transmit section **on**	2.3	2.5	2.8	V

Note

1. The referenced inputs should be connected to a valid CMOS input level.

AC CHARACTERISTICS

V_{CC} = 3.75 V; T_{amb} = −30 to +75 °C; f_{IF} = 175 MHz; unless otherwise specified.

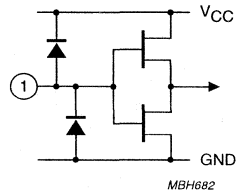
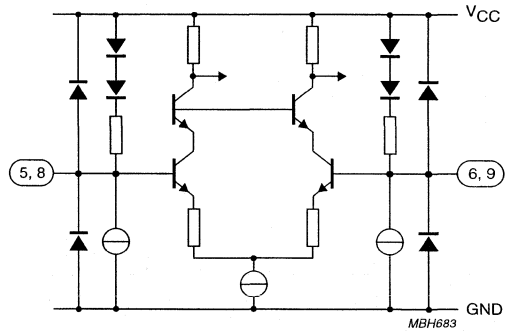
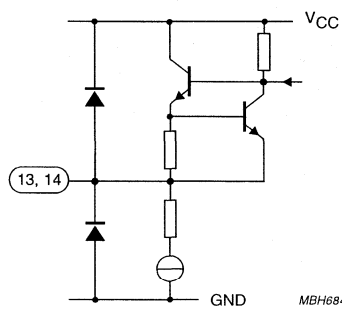
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Receive section (receive section on)						
R_{iRX}	RF input resistance (real part of the parallel input impedance)	balanced; at 942.5 MHz	–	150	–	Ω
C_{iRX}	RF input capacitance (imaginary part of the parallel input impedance)	balanced; at 942.5 MHz	–	1	–	pF
f_{iRX}	RF input frequency		925	–	960	MHz
RL_{iRX}	return loss on matched RF input	note 1	15	20	–	dB
G_{CPRX}	conversion power gain	differential RF input to differential IF output matched to 1 kΩ differential	19	22	25	dB
G_{rip}	gain ripple as a function of RF frequency	note 2	–	0.2	0.5	dB
ΔG/T	gain variation with temperature	note 2	−20	−15	−10	mdB/K
DES1	1 dB desensitization input power	interferer frequency offset 3 MHz	–	−30	–	dBm
$CP1_{RX}$	1 dB input compression point	note 1	−25	−23.0	–	dBm
$IP2D_{RX}$	half IF spurious rejection ($f_{RF} = f_{LO} + 0.5f_{IF}$)	note 2	60	–	–	dB
$IP3_{RX}$	3rd order intercept point referenced to the RF input	note 2	−21.5	−15	–	dBm
NF_{RX}	overall noise figure	RF input to differential IF output; note 3				
		T_{amb} = +25°C	–	3.6	4.0	dB
		over full temperature range	–	–	4.7	dB
R_{LRX}	typical application IF output load impedance	balanced	–	1000	–	Ω
C_{LRX}	IF output load capacitance	unbalanced	–	–	2	pF
f_{oRX}	IF frequency range		–	175	–	MHz
IR	image frequency rejection	$f_{LO} < f_{RF}$	30	45	–	dB

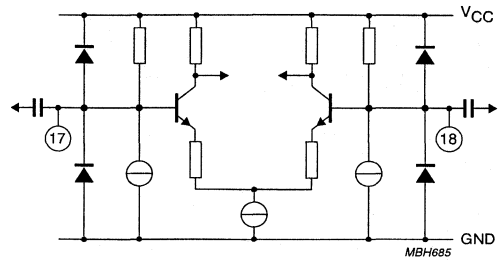
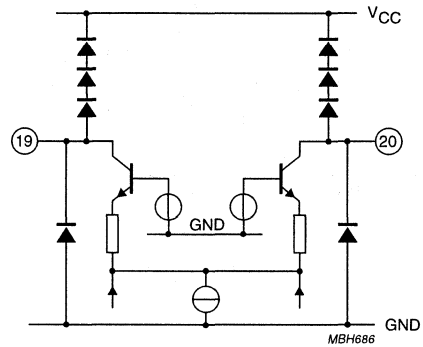
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Local oscillator section (RXON or TXON or SXON = 1)						
f_{iLO}	LO input frequency		750	–	785	MHz
R_{iLO}	LO input resistance (real part of the parallel input impedance)	balanced; at 767.5 MHz	–	80	–	Ω
C_{iLO}	LO input capacitance (imaginary part of the parallel input impedance)	balanced; at 767.5 MHz	–	2	–	pF
RL_{iLO}	return loss on matched input (including power-down mode)	note 2	10	15	–	dB
ΔRL_{iLO}	return loss variation between SX, SRX and STX modes	linear S_{11} variation; note 1	–	20	–	mU
P_{iLO}	LO input power level		–7	–4	0	dBm
RI_{LO}	reverse isolation	LOIN to RFIN at LO frequency; note 2	40	–	–	dB
Transmit section (transmit section on)						
Z_{oTX}	TX IF output impedance		–	–	200	Ω
Z_{LTX}	TX IF load impedance		–	1	–	kΩ
C_{LTX}	TX IF load capacitance		–	–	2	pF
R_{iTX}	TX RF input resistance (real part of the parallel input impedance)	balanced; at 897.5 MHz	–	200	–	Ω
C_{iTX}	TX RF input capacitance (imaginary part of the parallel input impedance)	balanced; at 897.5 MHz	–	1	–	pF
f_{iTX}	TX input frequency		880	–	915	MHz
RL_{iTX}	return loss on matched TX input	note 1	15	20	–	dB
G_{CPTX}	conversion power gain	from 200 Ω to 1 kΩ output; note 2	5	7.4	10	dB
f_{oTX}	TX output frequency		40	–	200	MHz
$CP1_{TX}$	1 dB input compression point	note 1	–22	–17.5	–	dBm
$IP2_{TX}$	2nd order intercept point		–	+20	–	dBm
$IP3_{TX}$	3rd order intercept point		–12	–9	–	dBm
NF_{TX}	noise figure	double sideband; notes 2 and 3	–	9.8	12	dB
RI_{TX}	reverse isolation	TXIN to LOIN; note 2	40	–	–	dB
I_{TX}	isolation	LOIN to TXIN; note 2	40	–	–	dB
Timing						
t_{start}	start-up time of each block		1	5	20	µs

Notes

1. Measured and guaranteed only on Philips UAA2073AM demonstration board at T_{amb} = 25 °C.
2. Measured and guaranteed only on Philips UAA2073AM demonstration board.
3. This value includes printed-circuit board and balun losses on Philips UAA2073AM demonstration board over full temperature range.

INTERNAL PIN CONFIGURATION

PIN	SYMBOL	DC VOLTAGE (V)	EQUIVALENT CIRCUIT
1	SBS		
10	SXON		
11	RXON		
12	TXON		
4	V_{CC1}	+3.75	
15	V_{CC2}	+3.75	
7	GND1	0	
16	GND2	0	
5	RFINA	+2.2	
6	RFINB	+2.2	
8	TXINA	+2.4	
9	TXINB	+2.4	
13	TXOIFB	+1.9	
14	TXOIFA	+1.9	

PIN	SYMBOL	DC VOLTAGE (V)	EQUIVALENT CIRCUIT
17	LOINB	+2.5	
18	LOINA	+2.5	
19	IFB	+3.0	
20	IFA	+3.0	

APPLICATION INFORMATION

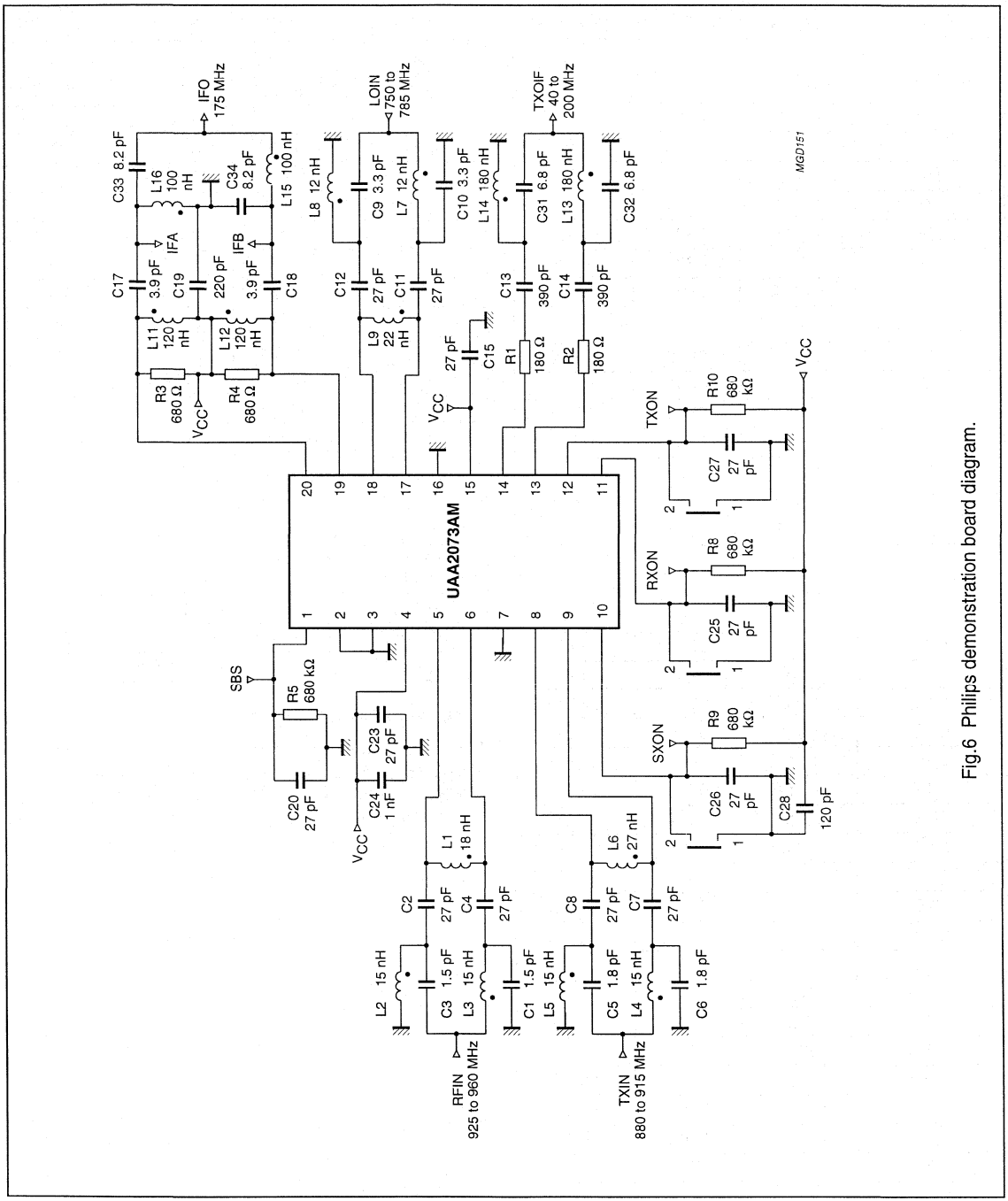


Fig.6 Philips demonstration board diagram.

Table 2 UAA2073AM demonstration board parts list

PART	VALUE	SIZE	LOCATION
Resistors			
R1	180 Ω	0805	TXOIF
R2	180 Ω	0805	TXOIF
R3	680 Ω	0805	IFO
R4	680 Ω	0805	IFO
R5	680 kΩ	0805	SBS
R8	680 kΩ	0805	RXON
R9	680 kΩ	0805	SXON
R10	680 kΩ	0805	TXON
Capacitors			
C1	1.5 pF	0805	RFIN
C2	27 pF	0805	RFIN
C3	1.5 pF	0805	RFIN
C4	27 pF	0805	RFIN
C5	1.8 pF	0805	TXIN
C6	1.8 pF	0805	TXIN
C7	27 pF	0805	TXIN
C8	27 pF	0805	TXIN
C9	3.3 pF	0805	LOIN
C10	3.3 pF	0805	LOIN
C11	27 pF	0805	LOIN
C12	27 pF	0805	LOIN
C13	390 pF	0805	TXOIF
C14	390 pF	0805	TXOIF
C15	27 pF	0805	V_{CCLO}
C17	3.9 pF	0805	IFO
C18	3.9 pF	0805	IFO
C19	220 pF	0805	IF/V_{CC}
C20	27 pF	0805	SBS
C23	27 pF	0805	V_{CCLNA}
C24	1 nF	0805	V_{CCLNA}
C25	27 pF	0805	RXON
C26	27 pF	0805	SXON
C27	27 pF	0805	TXON
C28	120 pF	0805	V_{CC}
C31	6.8 pF	0805	TXOIF
C32	6.8 pF	0805	TXOIF
C33	8.2 pF	0805	IFO
C34	8.2 pF	0805	IFO

PART	VALUE	SIZE	LOCATION
Inductors			
L1	18 nH	0805	RFIN
L2	15 nH	0805	RFIN
L3	15 nH	0805	RFIN
L4	15 nH	0805	TXIN
L5	15 nH	0805	TXIN
L6	27 nH	0805	TXIN
L7	12 nH	0805	LOIN
L8	12 nH	0805	LOIN
L9	22 nH	0805	LOIN
L11	120 nH	1008	IFO
L12	120 nH	1008	IFO
L13	180 nH	0805	TXOIF
L14	180 nH	0805	TXOIF
L15	100 nH	1008	IFO
L16	100 nH	1008	IFO

Other components

COMPONENT	DESCRIPTIONS
IC1	UAA2073AM
SMA/RIM	sockets for RF and IF inputs/outputs
SMB	V_{CC} socket

Component manufacturers

All surface mounted resistors and capacitors are from Philips Components. The small value capacitors are multilayer ceramic with NPO dielectric. The inductors are from Coilcraft UK.

Image rejecting front-end for GSM applications

UAA2073M

FEATURES

- Low-noise, wide dynamic range amplifier
- Very low noise figure
- Dual balanced mixer for at least 30 dB; on-chip image rejection
- IF I/Q combination network for 50 to 100 MHz
- Down-conversion mixer for closed-loop transmitters
- Independent TX/RX fast **on/off** power-down modes
- Very small outline packaging
- Very small application (no image filter).

APPLICATIONS

- 900 MHz front-end for GSM hand-portable equipment
- Compact digital mobile communication equipment
- TDMA receivers.

GENERAL DESCRIPTION

UAA2073M contains both a receiver front-end and a high frequency transmit mixer intended for GSM (Global System for Mobile communications) cellular telephones. Designed in an advanced BiCMOS process it combines high performance with low power consumption and a high degree of integration, thus reducing external component costs and total front-end size.

The main advantage of the UAA2073M is its ability to provide over 30 dB of image rejection. Consequently, the image filter between the LNA and the mixer is suppressed and the duplexer design is eased, compared with a conventional front-end design.

Image rejection is achieved in the internal architecture by two RF mixers in quadrature and two all-pass filters in I and Q IF channels that phase shift the IF by 45° and 135° respectively. The two phase shifted IFs are recombined and buffered to furnish the IF output signal.

For instance, signals presented at the RF input at LO + IF frequency are rejected through this signal processing while signals at LO – IF frequency can form the IF signal. An internal switch allows to reject the upper or lower image frequency. Image rejection is at an optimum when the IF is 71 MHz and local oscillator is above the wanted signal.

The receiver section consists of a low-noise amplifier that drives a quadrature mixer pair. The IF amplifier has on-chip 45° and 135° phase shifting and a combining network for image rejection.The IF driver has differential open-collector type outputs.

The LO part consists of an internal all-pass type phase shifter to provide quadrature LO signals to the receive mixers. The all-pass filters outputs are buffered before been fed to the receive mixers.

The transmit section consists of a down-conversion mixer and a transmit IF driver stage. In the transmit mode an internal LO buffer is used to drive the transmit IF down-conversion mixer.

All RF and IF inputs or outputs are balanced to reduce EMC issues.

Fast power-up switching is possible. A synthesizer-on (synthon) mode enables LO buffers independent of the other circuits. When SYNTHON pin is HIGH, all internal buffers on the LO path of the circuit are turned **on**, thus minimizing LO pulling when remainder of receive chain is powered-up.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UAA2073M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

QUICK REFERENCE DATA

Note 1.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	3.6	3.75	5.3	V
$I_{CC(RX)}$	receive supply current	21	26	32	mA
$I_{CC(TX)}$	transmit supply current	9	12	15	mA
NF	noise figure on demonstration board (including matching and PCB losses)	–	3.25	4.3	dB
G_{CP}	conversion power gain	20	23	26	dB
IR	image frequency rejection	30	37	–	dB
T_{amb}	operating ambient temperature	−30	+25	+85	°C

Note

1. For conditions see Chapters "DC characteristics" and "AC characteristics".

BLOCK DIAGRAM

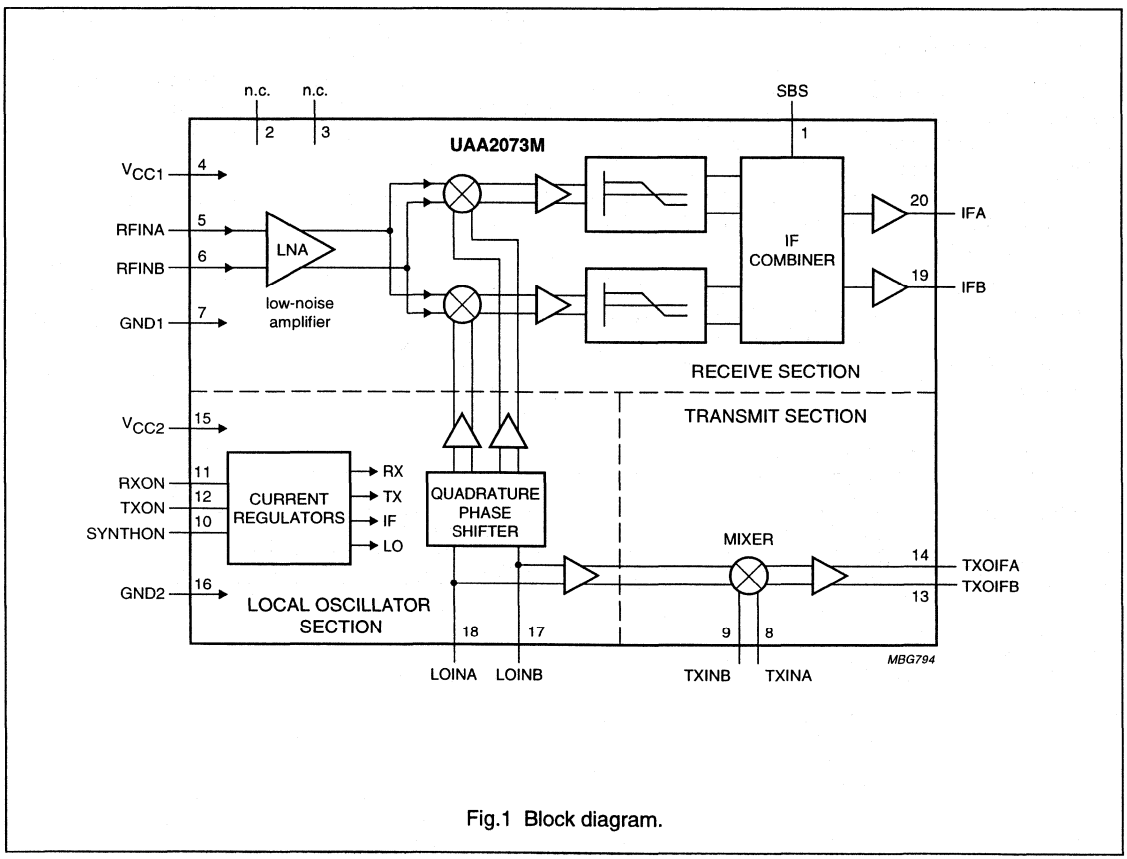


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SBS	1	sideband selection
n.c.	2	not connected
n.c.	3	not connected
V_{CC1}	4	supply voltage for receive and transmit sections
RFINA	5	RF input A (balanced)
RFINB	6	RF input B (balanced)
GND1	7	ground 1 for receive and transmit sections
TXINA	8	transmit mixer input A (balanced)
TXINB	9	transmit mixer input B (balanced)
SYNTHON	10	hardware power-on of LO section (including buffers to RX and TX)
RXON	11	hardware power-on for receive section and LO buffers to RX
TXON	12	hardware power-on for transmit section and LO buffers to TX
TXOIFB	13	transmit mixer IF output B (balanced)
TXOIFA	14	transmit mixer IF output A (balanced)
V_{CC2}	15	supply voltage for LO section
GND2	16	ground 2 for LO section
LOINB	17	LO input B (balanced)
LOINA	18	LO input A (balanced)
IFB	19	IF output B (balanced)
IFA	20	IF output A (balanced)

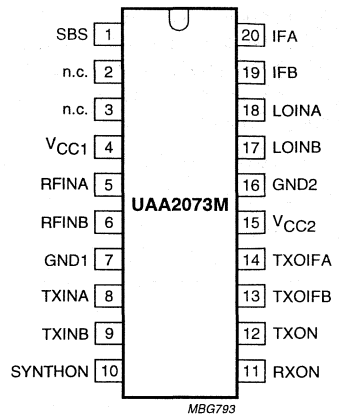


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Receive section

The circuit contains a low-noise amplifier followed by two high dynamic range mixers. These mixers are of the Gilbert-cell type. The whole internal architecture is fully differential.

The local oscillator, shifted in phase to 45° and 135°, mixes the amplified RF to create I and Q channels. The two I and Q channels are buffered, phase shifted by 45° and 135° respectively, amplified and recombined internally to realize the image rejection.

Pin SBS allows sideband selection:

- $f_{LO} < f_{RF}$ (SBS = 1)
- $f_{LO} > f_{RF}$ (SBS = 0).

Balanced signal interfaces are used for minimizing crosstalk due to package parasitics. The RF differential input impedance is 150 Ω (parallel real part), choosen to minimize current consumption at best noise performance.

The IF output is differential and of the open-collector type, tuned for 71 MHz. Typical application will load the output with a differential 500 Ω load; i.e. a 500 Ω resistor load at each IF output, plus a 1 kΩ to x Ω narrow band matching network (x Ω being the input impedance of the IF filter). The path to V_{CC} for the DC current is achieved via tuning inductors. The output voltage is limited to $V_{CC} + 3V_{be}$ or 3 diode forward voltage drops.

Fast switching, **on/off**, of the receive section is controlled by the hardware input RXON.

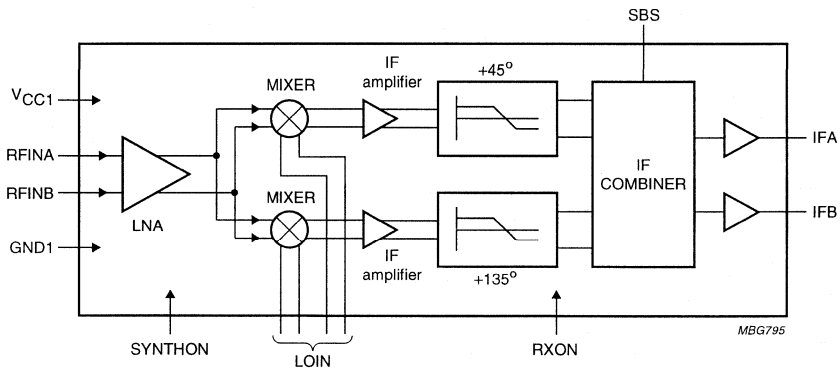


Fig.3 Block diagram, receive section.

Local oscillator section

The local oscillator (LO) input directly drives the two internal all-pass networks to provide quadrature LO to the receive mixers.

The LO differential input impedance is 50 Ω (parallel real part).

A synthesizer-on (synthon) mode is used to power-up the buffering on the LO inputs, minimizing the pulling effect on the external VCO when entering transmit or receive modes.

This mode is active when the SYNTHON input is HIGH. Table 1 shows status of circuit in accordance with TXON, RXON and SYNTHON inputs.

Transmit mixer

This mixer is used for down-conversion to the transmit IF. Its inputs are coupled to the transmit RF and down-convert it to a modulated transmit IF frequency which is phase locked with the baseband modulation.

The transmit mixer provides a differential input at 200 Ω and a differential output driver buffer for a 1 kΩ load. The IF outputs are low impedance (emitter followers).

Fast switching, **on/off**, of the transmit section is controlled by the hardware input TXON.

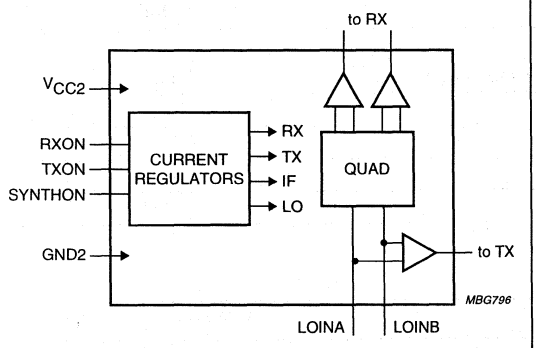


Fig.4 Block diagram, LO section.

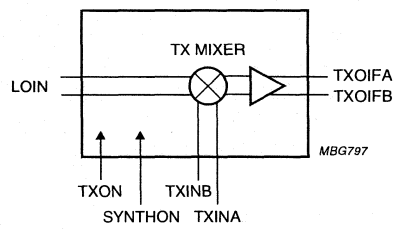


Fig.5 Block diagram, transmit mixer.

Table 1 Control of power status

EXTERNAL PIN LEVEL			CIRCUIT MODE OF OPERATION
TXON	RXON	SYNTHON	
LOW	LOW	LOW	power-down mode
LOW	HIGH	LOW	RX mode: receive section and LO buffers to RX **on**
HIGH	LOW	LOW	TX mode: transmit section and LO buffers to TX **on**
LOW	LOW	HIGH	synthon mode: complete LO section **on**
LOW	HIGH	HIGH	SRX mode: receive section **on** and synthon mode active
HIGH	LOW	HIGH	STX mode: transmit section **on** and synthon mode active
HIGH	HIGH	LOW	receive and transmit sections **on**; specification not guaranteed
HIGH	HIGH	HIGH	receive and transmit sections **on**; specification not guaranteed

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	–	9	V
ΔGND	difference in ground supply voltage applied between GND1 and GND2	–	0.6	V
$P_{I(max)}$	maximum power input	–	+20	dBm
$P_{dis(max)}$	maximum power dissipation in quiet air	–	250	mW
$T_{j(max)}$	maximum operating junction temperature	–	+150	°C
T_{stg}	storage temperature	–65	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	120	K/W

HANDLING

Every pin withstands the ESD test in accordance with MIL-STD-883C class 2 (method 3015.5).

DC CHARACTERISTICS

V_{CC} = 3.75 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pins V_{CC1} and V_{CC2}						
V_{CC}	supply voltage	over full temperature range	3.6	3.75	5.3	V
$I_{CC(RX)}$	supply current in RX mode		21	26	32	mA
$I_{CC(TX)}$	supply current in TX mode		9	12	15	mA
$I_{CC(SX)}$	supply current in synthon mode		4.4	5.6	6.6	mA
$I_{CC(SRX)}$	supply current in SRX mode		23	28	34	mA
$I_{CC(STX)}$	supply current in STX mode		12.5	15.0	19.5	mA
$I_{CC(PD)}$	supply current in power-down mode		–	0.01	50	µA
Pins SYNTHON, RXON, TXON and SBS						
V_{th}	CMOS threshold voltage	note 1	–	1.25	–	V
V_{IH}	HIGH level input voltage		$0.7V_{CC}$	–	V_{CC}	V
V_{IL}	LOW level input voltage		−0.3	–	0.8	V
I_{IH}	HIGH level static input current	pin at V_{CC} − 0.4 V	−1	–	+1	µA
I_{IL}	LOW level static input current	pin at 0.4 V	−1	–	+1	µA
Pins RFINA and RFINB						
$V_{I(RFIN)}$	DC input voltage level	receive section **on**	2.0	2.2	2.4	V
Pins IFA and IFB						
$I_{O(IF)}$	DC output current	receive section **on**	2.3	3.0	3.8	mA
Pins TXINA and TXINB						
$V_{I(TXIN)}$	DC input voltage level	transmit section **on**	2.1	2.4	2.6	V
Pins TXOIFA and TXOIFB						
$V_{O(TXOIF)}$	DC output voltage level	transmit section **on**	1.8	1.9	2.1	V
Pins LOINA and LOINB						
$V_{I(LOIN)}$	DC input voltage level	receive section **on**	2.3	2.5	2.8	V
		transmit section **on**	2.3	2.5	2.8	V

Note

1. The referenced inputs should be connected to a valid CMOS input level.

AC CHARACTERISTICS

V_{CC} = 3.75 V; T_{amb} = −30 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Receive section (receive section on)						
Z_{RF}	RF input impedance (real part)	balanced parallel	–	150	–	Ω
f_{RF}	RF input frequency		925	–	960	MHz
RL_{RF}	return loss on matched RF input	note 1	15	20	–	dB
G_{CP}	conversion power gain	differential RF input to differential IF output matched to 1 kΩ differential	20	23	26	dB
G_{rip}	gain ripple as a function of RF frequency	note 2	–	0.2	0.5	dB
ΔG/T	gain variation with temperature	note 2	−20	−15	−10	mdB/K
DES1	1 dB desensitization input power	interferer frequency offset 3 MHz	–	−30	–	dBm
$CP1_{RX}$	1 dB input compression point	note 1	−24.5	−23.0	–	dBm
$IP2D_{RX}$	2nd order intercept point referenced to the RF differential input	differential output; note 2	+30	+40	–	dBm
$IP3_{RX}$	3rd order intercept point referenced to the RF input	note 2	−18	−15	–	dBm
NF_{RX}	overall noise figure	RF input to differential IF output; notes 2 and 3	–	3.25	4.30	dB
$R_{L(IF)}$	typical application IF output load resistor	between pin and V_{CC}	–	500	–	Ω
$C_{L(IF)}$	IF output load capacitance	unbalanced	–	–	2	pF
f_{IF}	IF frequency range	$f_{LO} > f_{RF}$	50	71	100	MHz
		$f_{LO} < f_{RF}$	50	71	100	MHz
IR	image frequency rejection		30	37	–	dB
Local oscillator section (RXON or TXON or SYNTHON = 1)						
f_{LO}	LO input frequency		850	–	1100	MHz
Z_{LO}	LO input impedance	balanced	–	50	–	Ω
ΔZ_{LO}	impedance change when switching from synthon mode to SRX or STX mode	mUnits measured on Smith chart; note 1	–	20	–	Ω
RL_{LO}	return loss on matched input (including power-down mode)	note 2	10	15	–	dB
$P_{i(LO)}$	LO input power level		−7	−4	0	dBm
RI_{LO}	reverse isolation	LOIN to RFIN at LO frequency; note 2	40	–	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Transmit section (transmit section on)						
$Z_{O(TX)}$	TX IF output impedance		–	–	200	Ω
$Z_{L(TX)}$	TX IF load impedance		–	1	–	kΩ
$C_{L(TX)}$	TX IF load capacitance		–	–	2	pF
$Z_{i(TX)}$	TX RF input impedance	balanced	–	200	–	Ω
$f_{i(TX)}$	TX input frequency		880	–	915	MHz
RL_{TX}	return loss on matched TX input	note 1	15	20	–	dB
G_{CP}	conversion power gain	from 200 Ω to 1 kΩ output; note 2	5	7.4	10	dB
$f_{o(TX)}$	TX output frequency		40	–	200	MHz
$CP1_{TX}$	1 dB input compression point	note 1	–22	–17.5	–	dBm
$IP2_{TX}$	2nd order intercept point		–	+20	–	dBm
$IP3_{TX}$	3rd order intercept point		–12	–9	–	dBm
NF_{TX}	noise figure	double sideband; notes 2 and 3	–	9.8	12	dB
RI_{TX}	reverse isolation	TXIN to LOIN; note 2	40	–	–	dB
I_{TX}	isolation	LOIN to TXIN; note 2	40	–	–	dB
Timing						
t_{start}	start-up time of each block		1	5	20	µs

Notes

1. Measured and guaranteed only on Philips UAA2073M demonstration board at T_{amb} = +25 °C.
2. Measured and guaranteed only on Philips UAA2073M demonstration board.
3. This value includes printed-circuit board and balun losses on Philips UAA2073M demonstration board over full temperature range.

APPLICATION INFORMATION

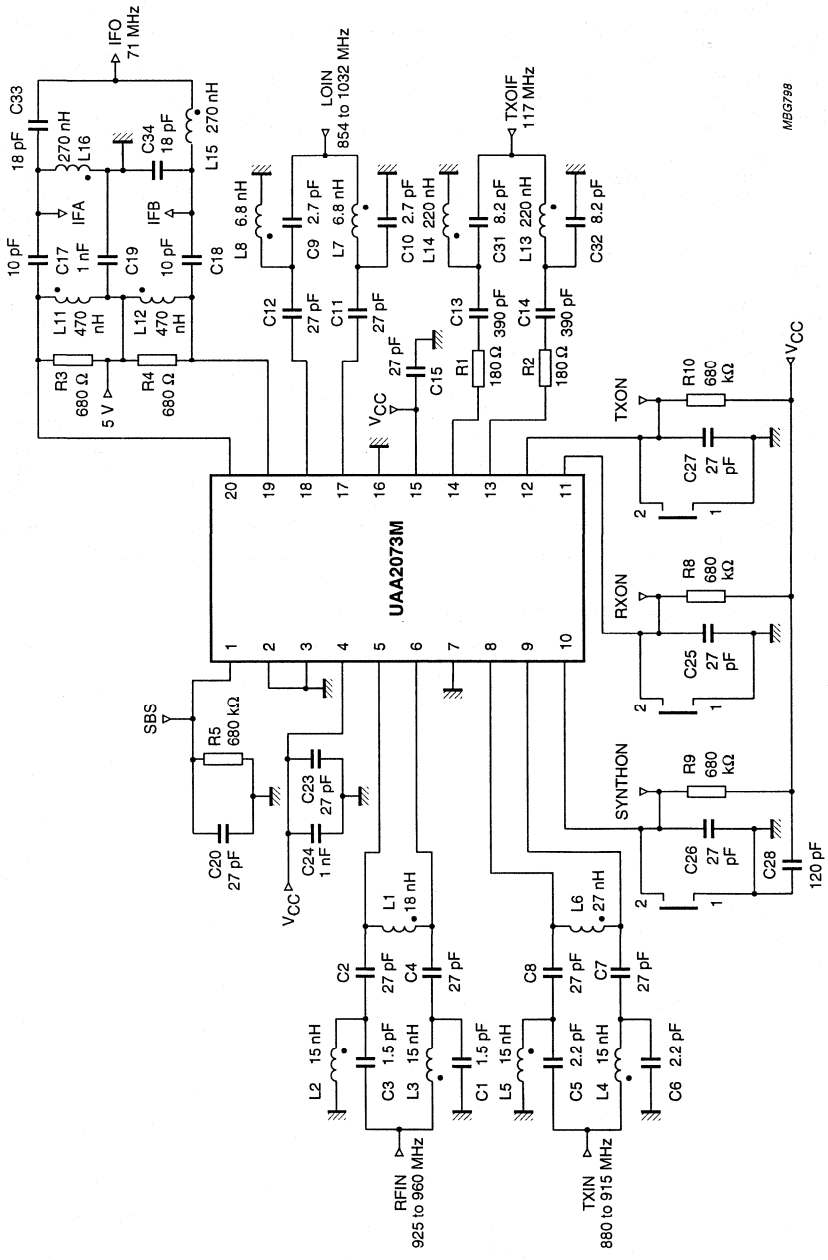


Fig.6 Philips demonstration board diagram for GSM applications.

All matching is to 50 Ω for measurement purposes.
Different values will be used in a real application.

Table 2 UAA2073M demonstration board parts list

PART	VALUE	SIZE	LOCATION
Resistors			
R1	180 Ω	0805	TXOIF
R2	180 Ω	0805	TXOIF
R3	680 Ω	0805	IFO
R4	680 Ω	0805	IFO
R5	680 kΩ	0805	SBS
R8	680 kΩ	0805	RXON
R9	680 kΩ	0805	SYNTHON
R10	680 kΩ	0805	TXON
Capacitors			
C1	1.5 pF	0805	RFIN
C2	27 pF	0805	RFIN
C3	1.5 pF	0805	RFIN
C4	27 pF	0805	RFIN
C5	2.2 pF	0805	TXIN
C6	2.2 pF	0805	TXIN
C7	27 pF	0805	TXIN
C8	27 pF	0805	TXIN
C9	2.7 pF	0805	LOIN
C10	2.7 pF	0805	LOIN
C11	27 pF	0805	LOIN
C12	27 pF	0805	LOIN
C13	390 pF	0805	TXOIF
C14	390 pF	0805	TXOIF
C15	27 pF	0805	V_{CCLO}
C17	10 pF	0805	IFO
C18	10 pF	0805	IFO
C19	1 nF	0805	IF/V_{CC}
C20	27 pF	0805	SBS
C23	27 pF	0805	V_{CCLNA}
C24	1 nF	0805	V_{CCLNA}
C25	27 pF	0805	RXON
C26	27 pF	0805	SYNTHON
C27	27 pF	0805	TXON
C28	120 pF	0805	V_{CC}
C31	8.2 pF	0805	TXOIF
C32	8.2 pF	0805	TXOIF
C33	18 pF	0805	IFO
C34	18 pF	0805	IFO

PART	VALUE	SIZE	LOCATION
Inductors			
L1	18 nH	0805	RFIN
L2	15 nH	0805	RFIN
L3	15 nH	0805	RFIN
L4	15 nH	0805	TXIN
L5	15 nH	0805	TXIN
L6	27 nH	0805	TXIN
L7	6.8 nH	0805	LOIN
L8	6.8 nH	0805	LOIN
L11	470 nH	1008	IFO
L12	470 nH	1008	IFO
L13	220 nH	0805	TXOIF
L14	220 nH	0805	TXOIF
L15	270 nH	1008	IFO
L16	270 nH	1008	IFO

Other components

COMPONENT	DESCRIPTIONS
IC1	UAA2073M
SMA/RIM	sockets for RF and IF inputs/outputs
SMB	V_{CC} socket

Component manufacturers

All surface mounted resistors and capacitors are from Philips Components. The small value capacitors are multilayer ceramic with NPO dielectric. The inductors are from Coilcraft UK.

Image rejecting front-end for DECT applications

UAA2077AM

FEATURES

- Low-noise, wide dynamic range amplifier
- Very low noise figure
- Dual balanced mixer for over 25 dB on-chip image rejection
- IF I/Q combiner at 110 MHz
- On-chip quadrature network
- RX fast **on/off** power-down mode
- Shrink small outline packaging
- Very small application (no image filter).

APPLICATIONS

- 1800 MHz front-end for DECT hand-portable equipment
- Compact digital mobile communication equipment
- TDMA receivers.

GENERAL DESCRIPTION

UAA2077AM contains a high frequency low noise receiver front-end intended to be used in DECT mobile telephones. Designed in an advanced BiCMOS process it combines high performance with low power consumption and a high degree of integration, thus reducing external component costs and total front-end size.

The main advantage of the UAA2077AM is its ability to provide over 25 dB of image rejection. Consequently, the image filter between the LNA and the mixer is suppressed.

Image rejection is achieved in the internal architecture by two RF mixers in quadrature and two all-pass filters in I and Q IF channels that phase shift the IF by 45° and 135° respectively. The two phase shifted IFs are recombined and buffered to furnish the IF output signal.

For instance, signals presented at the RF input at LO + IF frequency are rejected through this signal processing while signals at LO – IF frequency can form the IF signal. An internal switch enables the upper or lower image frequency to be rejected.

The receiver section consists of a low-noise amplifier that drives a quadrature mixer pair. The IF amplifier has on-chip 45° and 135° phase shifting and a combining network for image rejection. The IF driver has differential open-collector type outputs.

The LO part consists of an internal all-pass type phase shifter to provide quadrature LO signals to the receive mixers.The centre frequency of the phase shifter is adjustable for maximum image rejection in a given band. The all-pass filters outputs are buffered before being fed to the receive mixers. All RF and IF inputs or outputs are balanced.

Two pins RXON and SXON are used to control the different power-down modes. A special mode of operation called synthesizer-on mode (SX mode), controlled by pin SXON can be used to minimize the LO pulling when the receiver is turned **on**. When SXON is HIGH, all internal buffers on the LO path are turned **on**. Pin SBS allows a selection of whether to reject the upper or lower image frequency. Special care has been taken for fast power-up switching.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	T_{amb} = 0 to +70 °C	3.15	4.0	5.3	V
		over full temperature range	3.6	4.0	5.3	V
$I_{CC(RX)}$	receive supply current		21.5	26.5	33.5	mA
$I_{CC(PD)}$	supply current in power-down		–	0.2	50	µA
T_{amb}	operating ambient temperature		–30	+25	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UAA2077AM	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

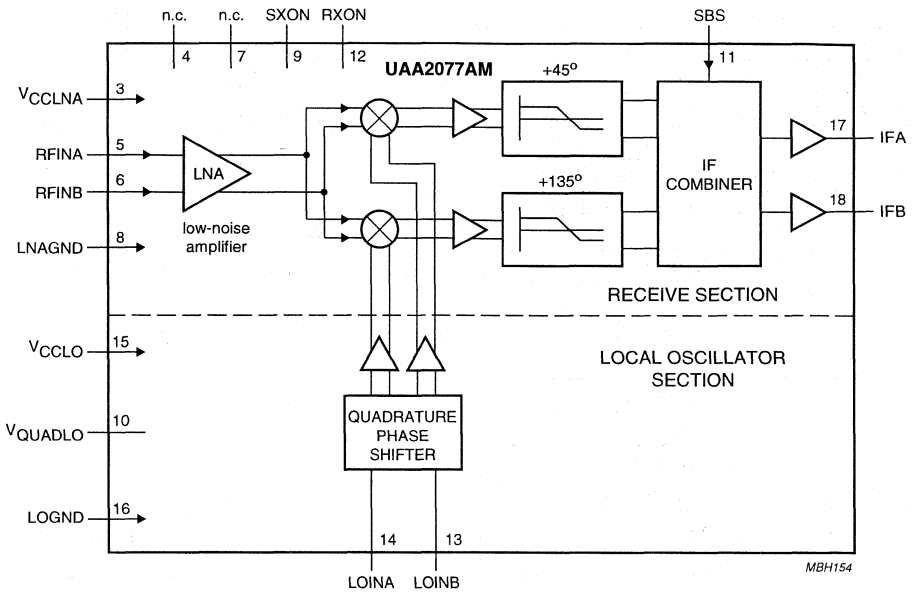


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
n.c.	2	not connected
V_{CCLNA}	3	supply voltage for LNA and IF parts
n.c.	4	not connected
RFINA	5	RF input A (balanced)
RFINB	6	RF input B (balanced)
n.c.	7	not connected
LNAGND	8	ground for LNA and IF parts
SXON	9	SX mode enable (see Table 1)
V_{QUADLO}	10	input voltage for LO quadrature trimming
SBS	11	sideband selection
RXON	12	RX mode enable (see Table 1)
LOINB	13	LO input B (balanced)
LOINA	14	LO input A (balanced)
V_{CCLO}	15	supply voltage for LO parts
LOGND	16	ground for LO parts
IFA	17	IF output A (balanced)
IFB	18	IF output B (balanced)
n.c.	19	not connected
n.c.	20	not connected

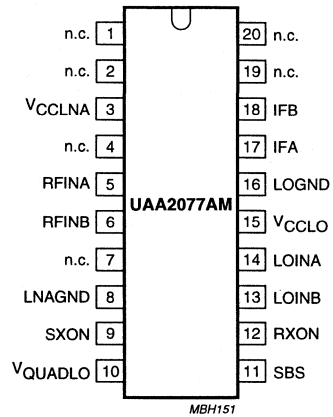


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Receive section

The circuit contains a low-noise amplifier followed by two high dynamic range mixers. These mixers are of the Gilbert-cell type, the whole internal architecture is fully differential.

The local oscillator, shifted in phase to 45° and 135°, mixes the amplified RF to create I and Q channels.
The two I and Q channels are buffered, phase shifted by 45° and 135° respectively, amplified and recombined internally to realize the image rejection.

Pin SBS allows sideband selection:

- $f_{LO} > f_{RF}$ (SBS = 1)
- $f_{LO} < f_{RF}$ (SBS = 0).

where f_{RF} is the frequency of the wanted signal.

Balanced signal interfaces are used for minimizing crosstalk due to package parasitics.

The IF output is differential and of the open-collector type. Typical application will load the output with a differential 1 kΩ load; for example, a 1 kΩ resistor load at each IF output, plus a differential 2 kΩ load consisting of the input impedance of the IF filter or the input impedance of the matching network for the IF filter. The power gain refers to the available power on this 2 kΩ load. The path to V_{CC} for the DC current should be achieved via tuning inductors. The output voltage is limited to $V_{CC} + 3V_{be}$ or 3 diode forward voltage drops.

Fast switching, **on/off**, of the receive section is controlled by the hardware input RXON.

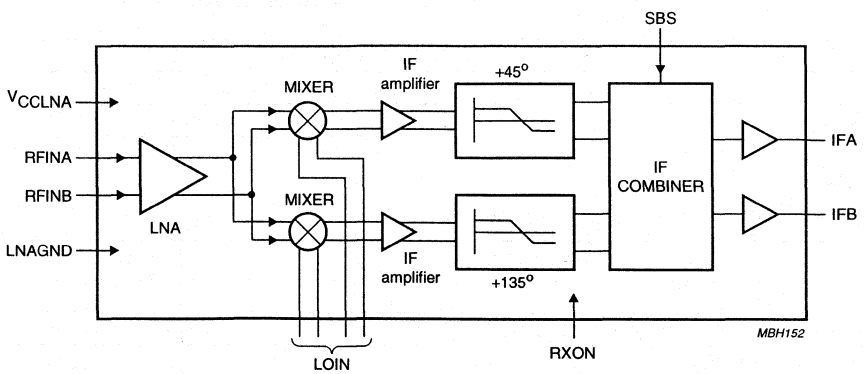


Fig.3 Block diagram, receive section.

Local oscillator section

The local oscillator (LO) input directly drives the two internal all-pass networks to provide quadrature LO to the receive mixers.

The centre frequency of the receive band is adjustable by the voltage on pin V_{QUADLO}. This should be achieved by connecting a resistor between V_{QUADLO} and V_{CC}. Over 25 dB of image rejection can be obtained by an optimum resistor value.

A synthesizer-on (SX) mode is used to power-up the LO input buffers, thus minimizing the pulling effect on the external VCO when entering receive mode. This mode is active when SXON = 1.

There are no internal biassing components attached to the pins LOINA and LOINB. These pins are connected by capacitors to the internal phase shifting network.

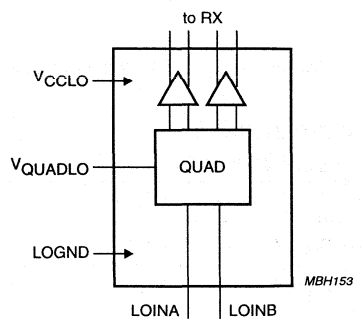


Fig.4 Block diagram, LO section.

Table 1 Control of power status

EXTERNAL PIN LEVEL		CIRCUIT MODE OF OPERATION
RXON	SXON	
LOW	LOW	power-down mode
HIGH	X	RX mode (receive and LO sections **on**)
LOW	HIGH	SX mode (only LO section **on**)

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	–	9	V
ΔGND	difference in ground supply voltage applied between LOGND and LNAGND	–	0.6	V
$P_{I(max)}$	maximum power input	–	20	dBm
$T_{j(max)}$	maximum operating junction temperature	–	150	°C
P_{max}	maximum power dissipation	–	250	mW
T_{stg}	IC storage temperature	−65	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	120	K/W

HANDLING

Every pin withstands the ESD test in accordance with *"MIL-STD-883C Class 2 (method 3015.5)"*.

DC CHARACTERISTICS

V_{CC} = 4.0 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pins V_{CCLNA} and V_{CCLO}						
V_{CC}	supply voltage	T_{amb} = 0 to +70 °C	3.15	4.0	5.3	V
		over full temperature range	3.6	4.0	5.3	V
$I_{CC(RX)}$	supply current in RX mode		21.5	26.5	33.5	mA
$I_{CC(PD)}$	supply current in power-down mode		–	0.2	50	μA
$I_{CC(SX)}$	supply current in SX mode		3	5	7	mA
Pins RXON, SXON and SBS						
V_{th}	CMOS threshold voltage	note 1	–	1.25	–	V
V_{IH}	HIGH level input voltage		$0.7V_{CC}$	–	V_{CC}	V
V_{IL}	LOW level input voltage		−0.3	–	+0.8	V
I_{IH}	HIGH level static input current	pin at V_{CC} − 0.4 V	−1	–	+1	μA
I_{IL}	LOW level static input current	pin at 0.4 V	−1	–	+1	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pins RFINA and RFINB						
V_I	DC input voltage level	receive section **on**	–	2.0	–	V
Pins IFA and IFB						
I_O	DC output current	receive section **on**	–	2.5	–	mA

Note

1. The referenced inputs should be connected to a valid CMOS input level.

AC CHARACTERISTICS

V_{CC} = 4.0 V; T_{amb} = –30 to +85 °C; unless otherwise specified.

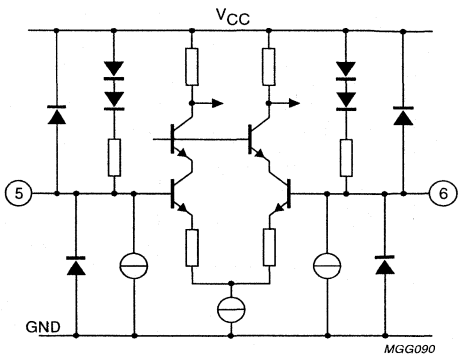
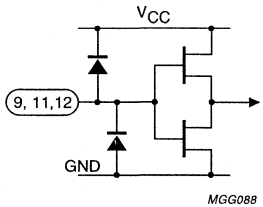
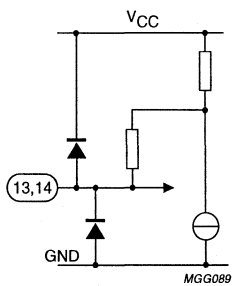
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Receive section (receive section enabled)						
R_{iRX}	RF input resistance (real part of the parallel input impedance)	balanced; at 1890 MHz	–	60	–	Ω
C_{iRX}	RF input capacitance (imaginary part of the parallel input impedance)	balanced; at 1890 MHz	–	1	–	pF
f_{iRX}	RF input frequency		1880	–	1900	MHz
RL_{iRX}	return loss on matched RF input	balanced; note 1	11	15	–	dB
G_{CP}	conversion power gain	differential RF inputs to differential IF outputs loaded to 1 kΩ differential	17	20	23	dB
G_{rip}	gain ripple as a function of RF frequency	note 2	–	0.2	–	dB
ΔG/T	gain variation with temperature	T_{amb} = –30 to +25 °C; note 2	–20	0	+10	mdB/°C
		T_{amb} = +25 to +85 °C; note 2	–40	–30	–20	mdB/°C
$CP1_{RX}$	1 dB compression point	differential RF inputs to differential IF outputs; note 1	–26	–23	–	dBm
DES3	3 dB desensitisation point	interferer frequency offset: 3 MHz; differential RF inputs to differential IF outputs; note 1	–	–30	–	dBm
		interferer frequency offset: 20 MHz; differential RF inputs to differential IF outputs; note 1	–	–28	–	dBm
$IP2D_{RX}$	2nd order intercept point	differential RF inputs to differential IF outputs; note 2	15	30	–	dBm
$IP3_{RX}$	3rd order intercept point	differential RF inputs to differential IF outputs; note 2	–23	–17	–	dBm
NF_{RX}	overall noise figure	differential RF inputs to differential IF outputs; notes 2 and 3	–	4.3	5.0	dB

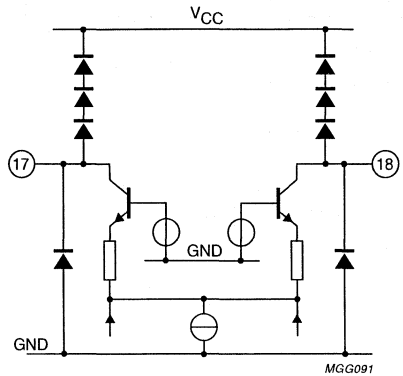
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Z_{LRX}	typical application IF output load impedance	balanced	–	1	–	kΩ
RL_{oRX}	return loss on matched IF output	balanced; note 1	11	15	–	dB
f_{oRX}	IF frequency		–	110	–	MHz
IR	rejection of image frequency	$f_{LO} < f_{RF}$; f_{IF} = 110 MHz; note 4	26	32	–	dB
Local oscillator section (receive section enabled)						
f_{iLO}	LO input frequency		1770	–	2010	MHz
R_{iLO}	LO input resistance (real part of the parallel input impedance)	balanced; at 1780 MHz	–	40	–	Ω
C_{iLO}	LO input capacitance (imaginary part of the parallel input impedance)	balanced; at 1780 MHz	–	2	–	pF
RL_{iLO}	return loss on matched LO input (including power-down mode)	note 1	9	12	–	dB
ΔRL_{iLO}	return loss variation ratio between SX and RX modes	linear S_{11} variation; note 1	–	5	–	mU
P_{iLO}	LO input power level		–6	–3	+3	dBm
RI_{LO}	reverse isolation	LOIN to RFIN at LO frequency; note 2	40	–	–	dB
Timing						
t_{start}	start-up time of each block		1	5	20	µs

Notes

1. Measured and guaranteed only on UAA2077AM demonstration board at T_{amb} = 25 °C.
2. Measured and guaranteed only on UAA2077AM demonstration board.
3. This value includes printed-circuit board and balun losses.
4. Measured and guaranteed only on UAA2077AM demonstration board at T_{amb} = 25 °C. V_{QUADLO} open-circuit.

INTERNAL PIN CONFIGURATION

SYMBOL	PIN	DC VOLTAGE (V)	EQUIVALENT CIRCUIT
V_{CCLNA}	3	4.0	
RFINA	5	2.0	
RFINB	6	2.0	
LNAGND	8	0	
SXON	9	–	
SBS	11	–	
RXON	12	–	
LOINB	13	–	
LOINA	14	–	
V_{CCLO}	15	4.0	

SYMBOL	PIN	DC VOLTAGE (V)	EQUIVALENT CIRCUIT
LOGND	16	0	
IFA	17	2.5	
IFB	18	2.5	

APPLICATION INFORMATION

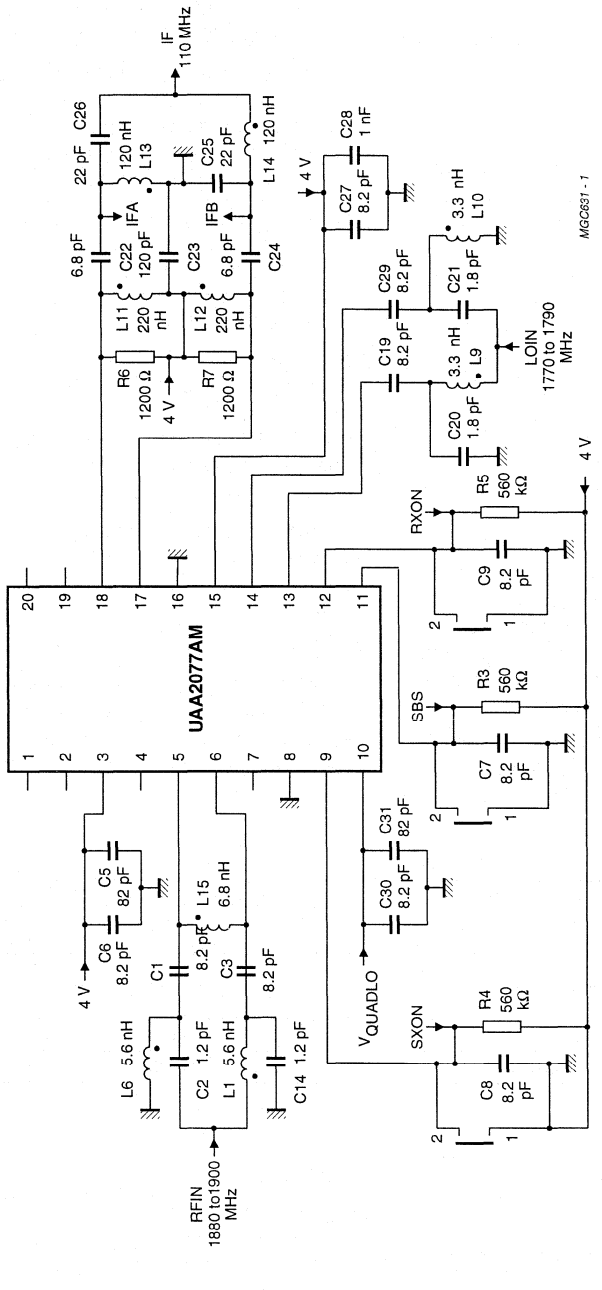


Fig.5 Application diagram.

Figure 5 illustrates the electrical diagram of the UAA2077AM Philips demonstration board for DECT applications. All matching is to 50 Ω for measurement purposes. Different values will be used in a real application.

2 GHz image rejecting front-end UAA2077BM

FEATURES

- Low-noise, wide dynamic range amplifier
- Very low noise figure
- Dual balanced mixer for over 25 dB on-chip image rejection
- IF I/Q combiner at 188 MHz
- On-chip quadrature network
- Down-conversion mixer for closed-loop transmitters
- Independent TX/RX fast ON/OFF power-down modes
- Very small outline packaging
- Very small application (no image filter).

APPLICATIONS

- 1800 MHz front-end for DCS1800 hand-portable equipment
- Compact digital mobile communication equipment
- TDMA receivers e.g. PCS and RF-LANS.

GENERAL DESCRIPTION

UAA2077BM contains both a receiver front-end and a high frequency transmit mixer intended to be used in mobile telephones. Designed in an advanced BiCMOS process it combines high performance with low power consumption and a high degree of integration, thus reducing external component costs and total front-end size.

The main advantage of the UAA2077BM is its ability to provide over 25 dB of image rejection. Consequently, the image filter between the LNA and the mixer is suppressed.

Image rejection is achieved in the internal architecture by two RF mixers in quadrature and two all-pass filters in I and Q IF channels that phase shift the IF by 45° and 135° respectively. The two phase shifted IFs are recombined and buffered to furnish the IF output signal.

For instance, signals presented at the RF input at the LO + IF frequency are rejected through this signal processing while signals at the LO – IF frequency can form the IF signal. An internal switch enables the upper or lower image frequency to be rejected.

The receiver section consists of a low-noise amplifier that drives a quadrature mixer pair. The IF amplifier has on-chip 45° and 135° phase shifting and a combining network for image rejection. The IF driver has differential open-collector type outputs.

The LO part consists of an internal all-pass type phase shifter to provide quadrature LO signals to the receive mixers. The centre frequency of the phase shifter is adjustable for maximum image rejection in a given band. The all-pass filters outputs are buffered before being fed to the receive mixers.

The transmit section consists of a low-noise amplifier and a down-conversion mixer. In the transmit mode an internal LO buffer is used to drive the transmit IF down-conversion mixer.

All RF and IF inputs or outputs are balanced.

Pins RXON, TXON and SXON enable a selection to be made of whether to reject the upper or lower image frequency and control of the different power-down modes. Special care has been taken for fast power-up switching.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	3.6	4.0	5.3	V
$I_{CC(RX)}$	receive supply current	21.5	26.5	33.5	mA
$I_{CC(TX)}$	transmit supply current	10.5	13.5	18	mA
$I_{CC(PD)}$	supply current in power-down	–	0.2	50	µA
T_{amb}	operating ambient temperature	–30	+25	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UAA2077BM	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

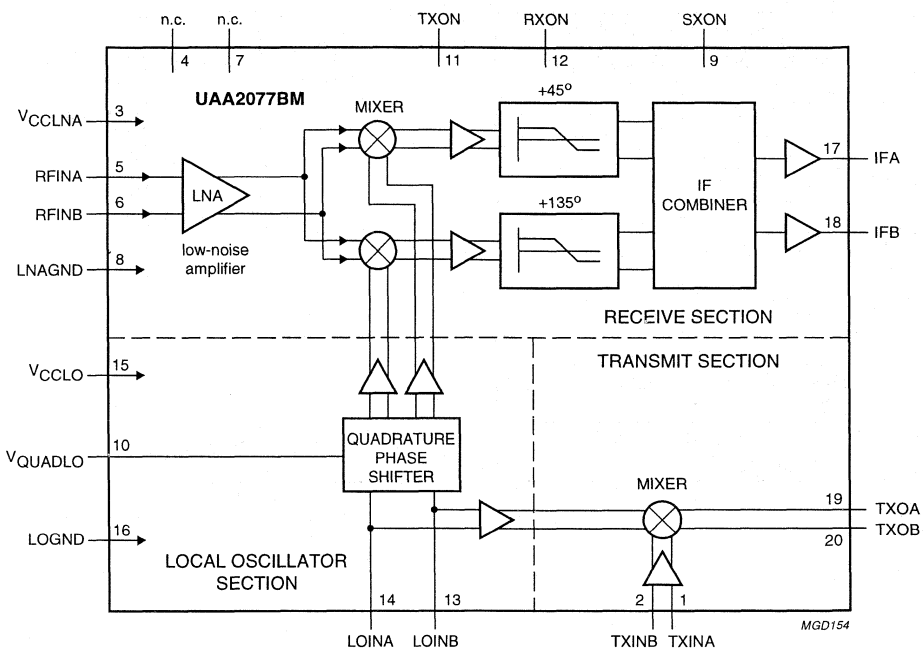


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
TXINA	1	transmit mixer input A (balanced)
TXINB	2	transmit mixer input B (balanced)
V_{CCLNA}	3	supply voltage for LNA, IF parts and TX mixer
n.c.	4	not connected
RFINA	5	RF input A (balanced)
RFINB	6	RF input B (balanced)
n.c.	7	not connected
LNAGND	8	ground for LNA, IF parts and TX mixer
SXON	9	SX mode enable (see Table 1)
V_{QUADLO}	10	input voltage for LO quadrature trimming
TXON	11	TX mode enable (see Table 1)
RXON	12	RX mode enable (see Table 1)
LOINB	13	LO input B (balanced)
LOINA	14	LO input A (balanced)
V_{CCLO}	15	supply voltage for LO parts
LOGND	16	ground for LO parts
IFA	17	IF output A (balanced)
IFB	18	IF output B (balanced)
TXOA	19	transmit mixer IF output A (balanced)
TXOB	20	transmit mixer IF output B (balanced)

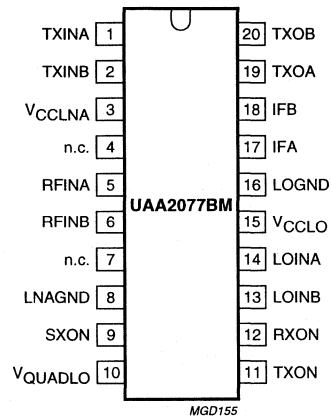


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Receive section

The circuit contains a low-noise amplifier followed by two high dynamic range mixers. These mixers are of the Gilbert-cell type, the whole internal architecture is fully differential.

The local oscillator, shifted in phase to 45° and 135°, mixes the amplified RF to create I and Q channels. The two I and Q channels are buffered, phase shifted by 45° and 135° respectively, amplified and recombined internally to realize the image rejection.

Balanced signal interfaces are used for minimizing crosstalk due to package parasitics.

The IF output is differential and of the open-collector type. Typical application will load the output with a differential 1 kΩ load; for example, a 1 kΩ resistor load at each IF output, plus a differential 2 kΩ load consisting of the input impedance of the IF filter or the input impedance of the matching network for the IF filter. The power gain refers to the available power on this 2 kΩ load. The path to V_{CC} for the DC current should be achieved via tuning inductors. The output voltage is limited to $V_{CC} + 3V_{be}$ or 3 diode forward voltage drops.

Fast switching, ON/OFF, of the receive section is controlled by the hardware input RXON.

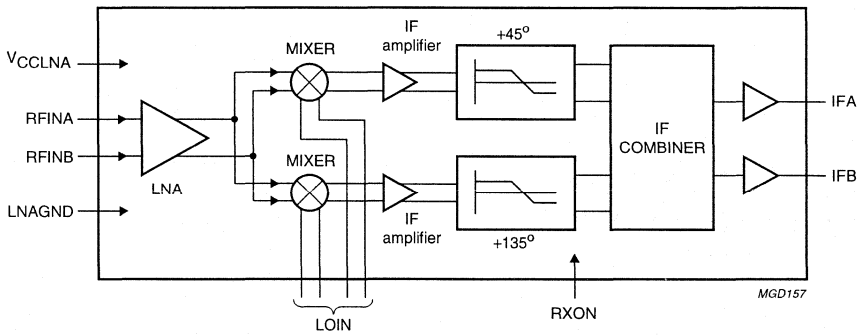


Fig.3 Block diagram, receive section.

Local oscillator section

The local oscillator (LO) input directly drives the two internal all-pass networks to provide quadrature LO to the receive mixers.

The centre frequency of the receive band is adjustable by the voltage on pin V_{QUADLO}. This should be achieved by connecting a resistor between V_{QUADLO} and V_{CC}. Over 25 dB of image rejection can be obtained by an optimum resistor value.

A synthesizer-ON mode (SX mode) is used to power-up all LO input buffers, thus minimizing the pulling effect on the external VCO when entering the receive or transmit mode. This mode is active when SXON = 1.

Transmit mixer

This mixer is used for down-conversion to the transmit IF. Its inputs are coupled to the transmit RF which is down-converted to a modulated transmit IF frequency, phase-locked with the baseband modulation.

The IF outputs are high-impedance (open-collector type). Typical application will load the output with a differential 500 Ω load; for example, a 500 Ω resistor load, connected to V_{CC} for DC path, at each TX output, plus a differential 1 kΩ consisting of the input impedance of the matching network for the following TX part. The mixer can also be used for frequency up-conversion.

Fast switching ON/OFF, of the transmit section is controlled by the hardware input TXON.

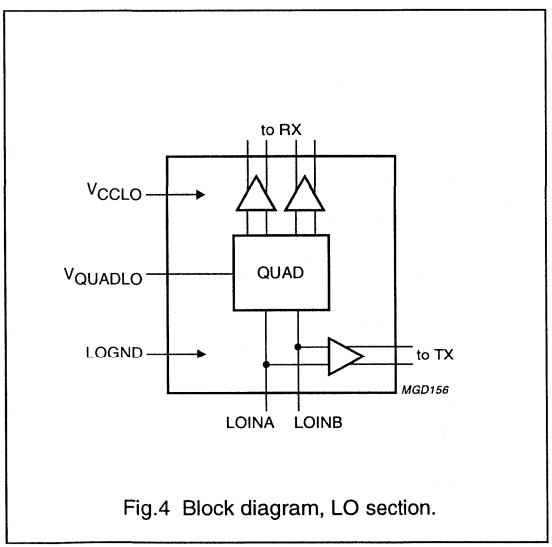


Fig.4 Block diagram, LO section.

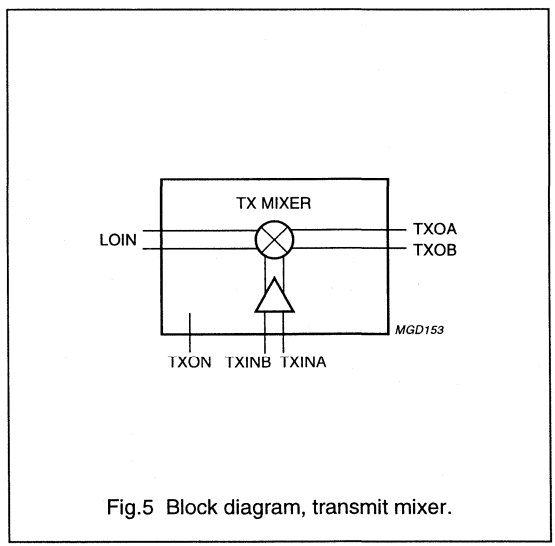


Fig.5 Block diagram, transmit mixer.

Table 1 Control of power status

EXTERNAL PIN LEVEL			CIRCUIT MODE OF OPERATION
TXON	RXON	SXON	
LOW	LOW	LOW	power-down mode
LOW	HIGH	LOW	RX mode, $f_{LO} < f_{RF}$: receive section and LO buffers to RX on
HIGH	LOW	LOW	TX mode: transmit section and LO buffers to TX on
LOW	LOW	HIGH	SX mode: complete LO section on
LOW	HIGH	HIGH	SRX mode, $f_{LO} < f_{RF}$: receive section on and SX mode active
HIGH	LOW	HIGH	STX mode: transmit section on and SX mode active
HIGH	HIGH	LOW	RX mode, $f_{LO} > f_{RF}$: receive section and LO buffers to RX on
HIGH	HIGH	HIGH	SRX mode, $f_{LO} > f_{RF}$: receive section on and SX mode active

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	–	9.0	V
ΔGND	difference in ground supply voltage applied between LOGND and LNAGND	–	0.6	V
$P_{i(max)}$	maximum power input	–	+20	dBm
$T_{j(max)}$	maximum operating junction temperature	–	+150	°C
$P_{dis(max)}$	maximum power dissipation in quiet air	–	250	mW
T_{stg}	storage temperature	−65	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	120	K/W

HANDLING

All pins withstand the ESD test in accordance with MIL-STD-883C class 2 (method 3015.5), except pins LOINA and LOINB which withstand 1500 V (class 1).

DC CHARACTERISTICS

V_{CC} = 4 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pins: V_{CCLNA} and V_{CCLO}						
V_{CC}	supply voltage	over full temperature range	3.6	4.0	5.3	V
$I_{CC(RX)}$	supply current in RX mode		21.5	26.5	33.5	mA
$I_{CC(TX)}$	supply current in TX mode		10.5	13.5	18	mA
$I_{CC(PD)}$	supply current in power-down mode		–	0.2	50	µA
$I_{CC(SX)}$	supply current in SX mode		5.5	7.5	10	mA
$I_{CC(SRX)}$	supply current in SRX mode		–	29	–	mA
$I_{CC(STX)}$	supply current in STX mode		–	18	–	mA
Pins: RXON, TXON and SXON						
V_{th}	CMOS threshold voltage	note 1	–	1.25	–	V
V_{IH}	HIGH level input voltage		$0.7V_{CC}$	–	V_{CC}	V
V_{IL}	LOW level input voltage		–0.3	–	0.8	V
I_{IH}	HIGH level static input current	pins at V_{CC} – 0.4 V	–1	–	+1	µA
I_{IL}	LOW level static input current	pins at 0.4 V	–1	–	+1	µA
Pins: RFINA and RFINB						
V_I	DC input voltage level	receive section on	–	2.0	–	V
Pins: IFA and IFB						
I_O	DC output current	receive section on	–	2.5	–	mA
Pins: TXINA and TXINB						
V_I	DC input voltage level	transmit section on	–	2.0	–	V
Pins: TXOA and TXOB						
I_O	DC output current	transmit section on	–	0.9	–	mA
Pins: LOINA and LOINB						
V_{LOIN}	DC input voltage level	RXON, TXON or SXON HIGH	–	3.3	–	V

Note

1. The referenced inputs should be connected to a valid CMOS input level.

AC CHARACTERISTICS

V_{CC} = 4 V; T_{amb} = −30 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Receive section (receive section enabled)						
R_{iRX}	RF input resistance (real part of the parallel input impedance)	balanced; at 1850 MHz	–	60	–	Ω
C_{iRX}	RF input capacitance (imaginary part of the parallel input impedance)	balanced; at 1850 MHz	–	1	–	pF
f_{iRX}	RF input frequency		1800	–	2000	MHz
RL_{iRX}	return loss on matched RF input	balanced; note 1	11	15	–	dB
G_{CPRX}	conversion power gain	differential RF inputs to differential IF outputs loaded to 1 kΩ differential	17	20	23	dB
G_{rip}	gain ripple as a function of RF frequency	between 1805 and 1880 MHz; note 2	–	0.2	–	dB
ΔG/T	gain variation with temperature	T_{amb} = −30 to +25 °C; note 2	−20	0	+10	mdB/°C
		T_{amb} = +25 to +85 °C; note 2	−40	−30	−20	mdB/°C
$CP1_{RX}$	1 dB compression point	differential RF inputs to differential IF outputs; note 1	−26	−23	–	dBm
DES3	3 dB desensitisation point	interferer frequency offset: 3 MHz; differential RF inputs to differential IF outputs; note 1	–	−30	–	dBm
		interferer frequency offset: 20 MHz; differential RF inputs to differential IF outputs; note 1	–	−27	–	dBm
$IP2D_{RX}$	2nd-order intercept point	differential RF inputs to differential IF outputs; note 2	+15	+22	–	dBm
$IP3_{RX}$	3rd-order intercept point	differential RF inputs to differential IF outputs; note 2	−23	−17	–	dBm
NF_{RX}	overall noise figure	differential RF inputs to differential IF outputs; notes 2 and 3	–	4.3	5.0	dB
Z_{LRX}	typical application IF output load impedance	balanced	–	1	–	kΩ
RL_{oRX}	return loss on matched IF output	balanced; note 1	11	15	–	dB
f_{oRX}	IF frequency range		170	188	210	MHz
IR_{RX}	rejection of image frequency	V_{QUADLO} tuned	20	–	–	dB
		$f_{LO} < f_{RF}$; f_{IF} = 188 MHz; note 4	25	32	–	dB
Local oscillator section (receive section enabled)						
f_{iLO}	LO input frequency		1600	–	2200	MHz
R_{iLO}	LO input resistance (real part of the parallel input impedance)	balanced; at 1662 MHz	–	45	–	Ω

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{iLO}	LO input capacitance (imaginary part of the parallel input impedance)	balanced; at 1662 MHz	–	2	–	pF
RL_{iLO}	return loss on matched input (including standby mode)	note 1	9	12	–	dB
ΔRL_{iLO}	return loss variation between SX, SRX and STX modes	linear S_{11} variation; note 1	–	5	–	mU
P_{iLO}	LO input power level		–6	–3	+3	dBm
RI_{LO}	reverse isolation	LOIN to RFIN at LO frequency; note 1	40	–	–	dB
R_{tune}	image rejection tuning resistor	connected between V_{QUADLO} and V_{CC}	0	4.7	–	kΩ
Transmit section (transmit section enabled)						
Z_{LTX}	TX IF typical load impedance	balanced	–	500	–	Ω
RL_{oTX}	return loss on matched TX IF output	note 1	11	15	–	dB
R_{iTX}	TX RF input resistance (real part of the parallel input impedance)	balanced; at 1750 MHz	–	65	–	Ω
C_{iTX}	TX RF input capacitance (imaginary part of the parallel input impedance)	balanced; at 1750 MHz	–	1	–	pF
f_{iTX}	TX input frequency		1600	–	2000	MHz
RL_{iTX}	return loss on matched TX input	note 1	10	15	–	dB
G_{CPTX}	conversion power gain	differential transmitter inputs to differential transmitter IF outputs loaded with 500 Ω differential	6	9	12	dB
f_{oTX}	TX output frequency		50	–	400	MHz
$CP1_{TX}$	1 dB input compression point	note 2	–25	–22	–	dBm
$IP2_{TX}$	2nd-order intercept point	note 2	–	+22	–	dBm
$IP3_{TX}$	3rd-order intercept point	note 2	–20	–16	–	dBm
NF_{TX}	noise figure	double sideband; notes 2 and 3	–	5	9	dB
I_{TX}	isolation	LOIN to TXIN; note 1	40	–	–	dB
RI_{TX}	reverse isolation	TXIN to LOIN; note 1	40	–	–	dB
Timing						
t_{stu}	start-up time of each block		1	5	20	µs

Notes

1. Measured and guaranteed only on UAA2077BM demonstration board at T_{amb} = +25 °C.
2. Measured and guaranteed only on UAA2077BM demonstration board.
3. This value includes printed-circuit board and balun losses.
4. Measured and guaranteed only on UAA2077BM demonstration board at T_{amb} = +25 °C, with a 4.7 kΩ resistor connected between V_{QUADLO} and V_{CC}.

APPLICATION INFORMATION

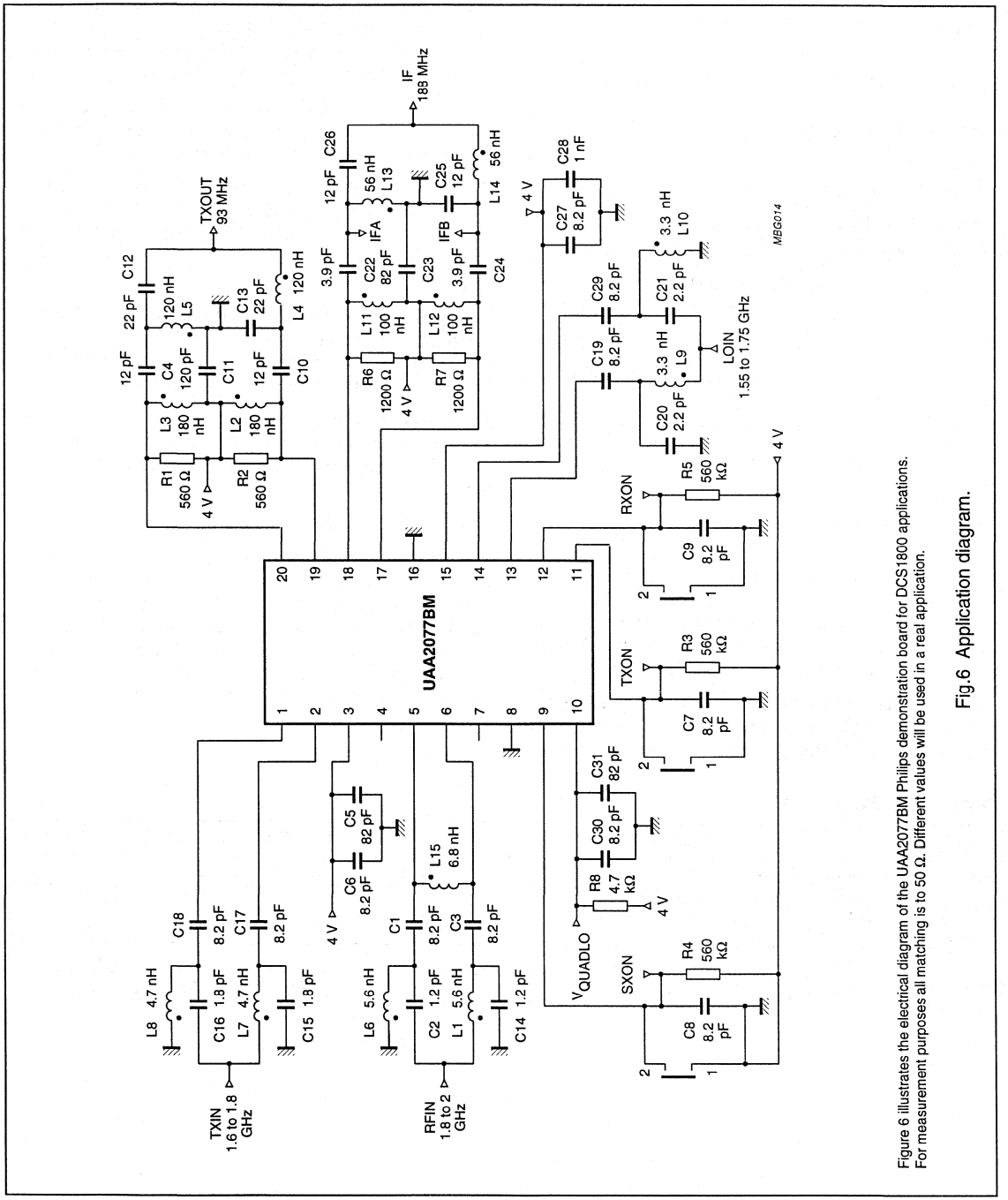


Fig.6 Application diagram.

Figure 6 illustrates the electrical diagram of the UAA2077BM Philips demonstration board for DCS1800 applications. For measurement purposes all matching is to 50 Ω. Different values will be used in a real application.

2 GHz image rejecting front-end UAA2077CM

FEATURES

- Low-noise, wide dynamic range amplifier
- Very low noise figure
- Dual balanced mixer for over 30 dB on-chip image rejection
- IF I/Q combiner at 188 MHz
- On-chip quadrature network
- Down-conversion mixer for closed-loop transmitters
- Independent TX/RX fast ON/OFF power-down modes
- Very small outline packaging
- Very small application (no image filter).

APPLICATIONS

- High frequency front-end for DCS1800/PCS1900 hand-portable equipment
- Compact digital mobile communication equipment
- TDMA receivers e.g. RF-LANS.

GENERAL DESCRIPTION

UAA2077CM contains both a receiver front-end and a high frequency transmit mixer intended to be used in mobile telephones. Designed in an advanced BiCMOS process it combines high performance with low power consumption and a high degree of integration, thus reducing external component costs and total front-end size.

The main advantage of the UAA2077CM is its ability to provide over 30 dB of image rejection. Consequently, the image filter between the LNA and the mixer is suppressed.

Image rejection is achieved in the internal architecture by two RF mixers in quadrature and two all-pass filters in I and Q IF channels that phase shift the IF by 45° and 135° respectively. The two phase shifted IFs are recombined and buffered to furnish the IF output signal.

Signals presented at the RF input at LO + IF frequency are rejected through this signal processing while signals at LO – IF frequency can form the IF signal.

The receiver section consists of a low-noise amplifier that drives a quadrature mixer pair. The IF amplifier has on-chip 45° and 135° phase shifting and a combining network for image rejection. The IF driver has differential open-collector type outputs.

The LO part consists of an internal all-pass type phase shifter to provide quadrature LO signals to the receive mixers. The all-pass filters outputs are buffered before being fed to the receive mixers.

The transmit section consists of a low-noise amplifier, and a down-conversion mixer. In the transmit mode, an internal LO buffer is used to drive the transmit IF down-conversion mixer.

All RF and IF inputs or outputs are balanced.

Pins RXON, TXON and SXON allow to control the different power-down modes. A synthesizer-on (SX) mode enables LO buffers independent of the other circuits. When pin SXON is HIGH, all internal buffers on the LO path of the circuit are turned on, thus minimizing LO pulling when remainder of the receive or transmit chain is powered up. Special care has been taken for fast power-up switching.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	3.6	3.75	5.3	V
$I_{CC(RX)}$	receive supply current	27.5	36	44.5	mA
$I_{CC(TX)}$	transmit supply current	11	14	17.5	mA
$I_{CC(PD)}$	supply current in power-down	–	–	50	µA
T_{amb}	operating ambient temperature	–30	+25	+75	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UAA2077CM	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

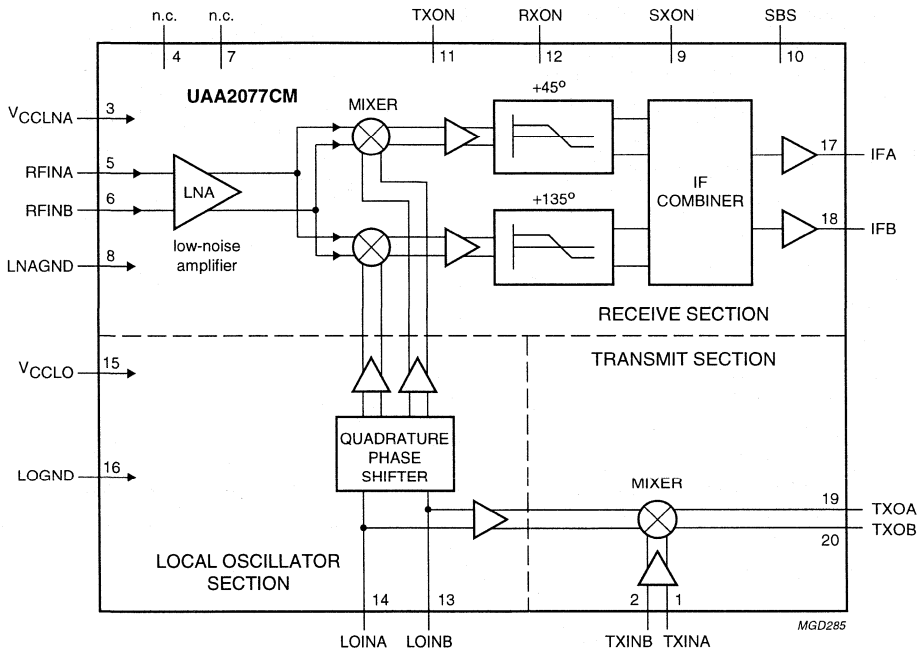


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
TXINA	1	transmit mixer input A (balanced)
TXINB	2	transmit mixer input B (balanced)
V_{CCLNA}	3	supply voltage for LNA, IF parts and TX mixer
n.c.	4	not connected
RFINA	5	RF input A (balanced)
RFINB	6	RF input B (balanced)
n.c.	7	not connected
LNAGND	8	ground for LNA, IF parts and TX mixer
SXON	9	SX mode enable (see Table 1)
SBS	10	sideband selection (should be grounded for $f_{LO} < f_{RF}$)
TXON	11	TX mode enable (see Table 1)
RXON	12	RX mode enable (see Table 1)
LOINB	13	LO input B (balanced)
LOINA	14	LO input A (balanced)
V_{CCLO}	15	supply voltage for LO parts
LOGND	16	ground for LO parts
IFA	17	IF output A (balanced)
IFB	18	IF output B (balanced)
TXOA	19	transmit mixer IF output A (balanced)
TXOB	20	transmit mixer IF output B (balanced)

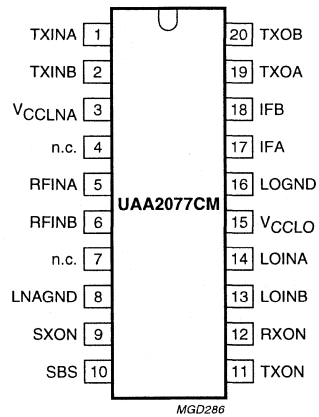


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Receive section

The circuit contains a low-noise amplifier followed by two high dynamic range mixers. These mixers are of the Gilbert-cell type, the whole internal architecture is fully differential.

The local oscillator, shifted in phase to 45° and 135°, mixes the amplified RF to create I and Q channels. The two I and Q channels are buffered, phase shifted by 45° and 135° respectively, amplified and recombined internally to realize the image rejection.

Pin SBS allows sideband selection:

- $f_{LO} > f_{RF}$ (SBS = 1)
- $f_{LO} < f_{RF}$ (SBS = 0).

Where f_{RF} is the frequency of the wanted signal.

Balanced signal interfaces are used for minimizing crosstalk due to package parasitics.

The IF output is differential and of the open-collector type. Typical application will load the output with a 680 Ω resistor load at each IF output, plus a differential 1 kΩ load made of the input impedance of the IF filter or the input impedance of the matching network for the IF filter. The power gain refers to the available power on this 1 kΩ load. The path to V_{CC} for the DC current should be achieved via tuning inductors. The output voltage is limited to $V_{CC} + 3V_{be}$ or 3 diode forward voltage drops.

Fast switching, ON/OFF, of the receive section is controlled by the hardware input RXON.

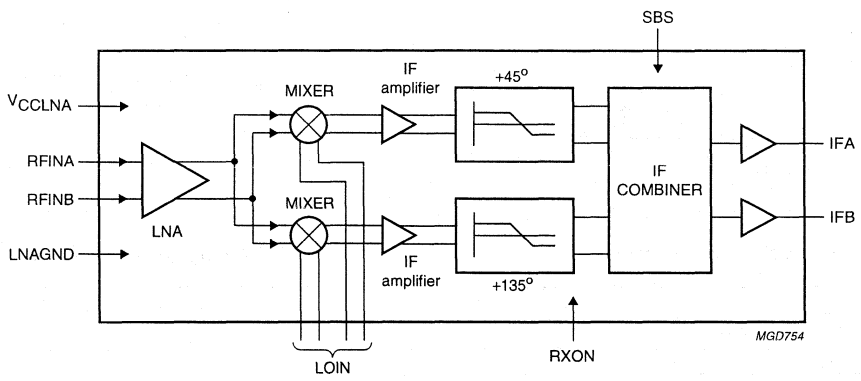


Fig.3 Block diagram, receive section.

Local oscillator section

The Local Oscillator (LO) input directly drives the two internal all-pass networks to provide quadrature LO to the receive mixers.

A synthesizer-ON mode (SX mode) is used to power-up all LO input buffers, thus minimizing the pulling effect on the external VCO when entering receive or transmit mode. This mode is active when SXON = 1.

Transmit mixer

This mixer is used for down-conversion to the transmit IF. Its inputs are coupled to the transmit RF which is down-converted to a modulated transmit IF frequency, phase locked with the baseband modulation.

The IF outputs are HIGH impedance (open-collector type).Typical application will load the output with a 560 Ω resistor load, connected to V_{CC} for DC path, at each TX output, plus a differential 1 kΩ made of the input impedance of the matching network for the following TX part. The mixer can also be used for frequency up-conversion.

Fast switching, ON/OFF, of the transmit section is controlled by the hardware input TXON.

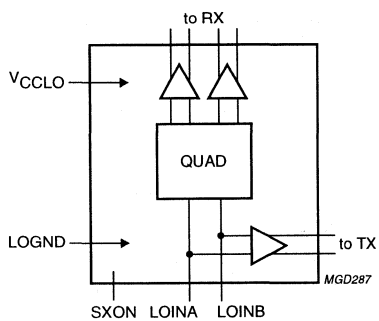


Fig.4 Block diagram, LO section.

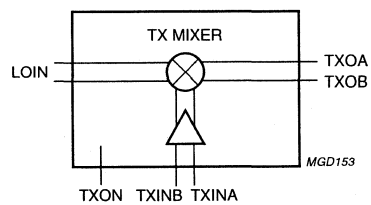


Fig.5 Block diagram, transmit mixer.

Table 1 Control of power status

EXTERNAL PIN LEVEL			CIRCUIT MODE OF OPERATION
TXON	RXON	SXON	
LOW	LOW	LOW	power-down mode
LOW	HIGH	LOW	RX mode: receive section and LO buffers to RX on
HIGH	LOW	LOW	TX mode: transmit section and LO buffers to TX on
LOW	LOW	HIGH	SX mode: complete LO section on
LOW	HIGH	HIGH	SRX mode: receive section on and SX mode active
HIGH	LOW	HIGH	STX mode: transmit section on and SX mode active
HIGH	HIGH	X	receive section and transmit section on; specification not guaranteed

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	–	9	V
ΔGND	difference in ground supply voltage applied between LOGND and LNAGND	–	0.6	V
$P_{i(max)}$	maximum power input	–	+20	dBm
$T_{j(max)}$	maximum operating junction temperature	–	+150	°C
$P_{dis(max)}$	maximum power dissipation in quiet air	–	250	mW
T_{stg}	storage temperature	−65	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	120	K/W

HANDLING

All pins withstand 1500 V ESD test in accordance with *"MIL-STD-883C class 1 (method 3015.5)"*.

DC CHARACTERISTICS

V_{CC} = 3.75 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pins: V_{CCLNA} and V_{CCLO}						
V_{CC}	supply voltage	over full temperature range	3.6	3.75	5.3	V
$I_{CC(RX)}$	supply current in RX mode		27.5	36	44.5	mA
$I_{CC(TX)}$	supply current in TX mode		11	14	17.5	mA
$I_{CC(PD)}$	supply current in power-down mode		–	–	50	µA
$I_{CC(SX)}$	supply current in SX mode		6.5	8.5	10.5	mA
$I_{CC(SRX)}$	supply current in SRX mode		29.5	38.5	47.5	mA
$I_{CC(STX)}$	supply current in STX mode		15	19.5	24	mA
Pins: RXON, TXON, SXON and SBS						
V_{th}	CMOS threshold voltage	note 1	–	1.25	–	V
V_{IH}	HIGH level input voltage		$0.7V_{CC}$	–	V_{CC}	V
V_{IL}	LOW level input voltage		–0.3	–	+0.8	V
I_{IH}	HIGH level static input current	pins at V_{CC} – 0.4 V	–1	–	+1	µA
I_{IL}	LOW level static input current	pins at 0.4 V	–1	–	+1	µA
Pins: RFINA and RFINB						
V_I	DC input voltage level	receive section on	1.8	2.0	2.2	V
Pins: IFA and IFB						
I_O	DC output current	receive section on	2.3	3.0	3.8	mA
Pins: TXINA and TXINB						
V_I	DC input voltage level	transmit section on	1.9	2.15	2.4	V
Pins: TXOA and TXOB						
I_O	DC output current	transmit section on	0.8	1.0	1.2	mA
Pins: LOINA and LOINB						
V_{LOIN}	DC input voltage level	RXON, TXON or SXON HIGH	2.6	2.9	3.2	V

Note

1. The referenced inputs should be connected to a valid CMOS input level.

AC CHARACTERISTICS

V_{CC} = 3.75 V; T_{amb} = −30 to +75 °C; f_{oRX} = 188 MHz; unless otherwise specified.

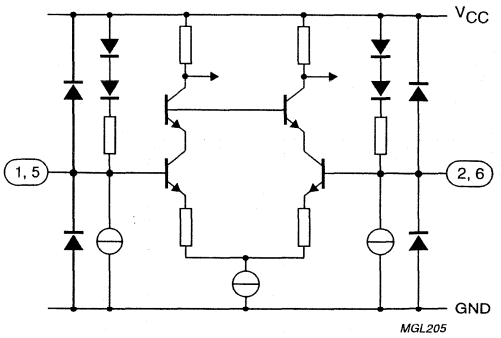
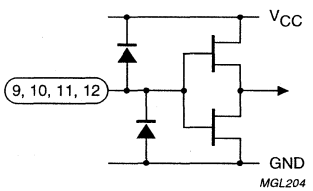
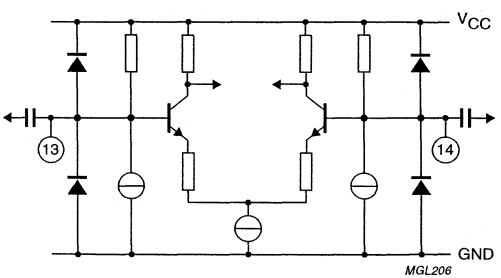
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Receive section (receive section enabled)						
R_{iRX}	RF input resistance (real part of the parallel input impedance)	balanced; at 1960 MHz	–	60	–	Ω
C_{iRX}	RF input capacitance (imaginary part of the parallel input impedance)	balanced; at 1960 MHz	–	0.8	–	pF
f_{iRX}	RF input frequency		1805	–	1990	MHz
RL_{iRX}	return loss on matched RF input	balanced; note 1	15	20	–	dB
G_{CPRX}	conversion power gain	differential RF inputs to differential IF outputs loaded to 1 kΩ differential	19	22	25	dB
G_{rip}	gain ripple as a function of RF frequency	within 100 MHz bandwidth; note 2	–	0.2	0.5	dB
ΔG/T	gain variation with temperature	note 2	−10	−15	−20	mdB/K
$CP1_{RX}$	1 dB compression point	differential RF inputs to differential IF outputs; note 1	−25.5	−24	–	dB
DES	desensitisation	interferer frequency offset: 3 MHz; P_{in} = −26 dBm; interferer frequency offset: 20 MHz, P_{in} = −23 dBm differential RF inputs to differential IF outputs; note 1	–	–	5	dB
$IP2D_{RX}$	half IF spurious attenuation for −52 dBm input power ($f_{RF} = f_{LO} + 0.5 \times f_{IF}$)	differential RF inputs to differential IF outputs; note 2	37	–	–	dB
$IP3_{RX}$	3rd order intercept point	differential RF inputs to differential IF outputs; note 2	−21.5	−17	–	dBm
NF_{RX}	overall noise figure	differential RF inputs to differential IF outputs				
		T_{amb} = 25 °C; DCS frequency range; note 3	–	3.8	–	dB
		T_{amb} = 25 °C; PCS frequency range; notes 2 and 3	–	4.0	4.4	dB
		T_{amb} = −30 to +65 °C; PCS frequency range; notes 2 and 3	–	–	5.0	dB
Z_{LRX}	typical application IF output load impedance	balanced	–	1000	–	Ω
RL_{oRX}	return loss on matched IF output	balanced; note 1	15	20	–	dB
f_{oRX}	IF frequency range		–	188	–	MHz
IR	rejection of image frequency	$f_{RF} > f_{LO}$; f_{RF} is the frequency of the wanted signal	30	38	–	dB

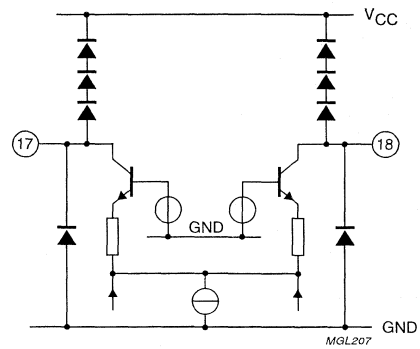
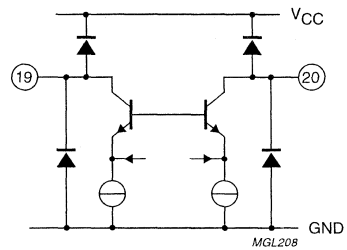
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Local oscillator section (receive section enabled)						
f_{iLO}	LO input frequency		1617	–	1802	MHz
R_{iLO}	LO input resistance (real part of the parallel input impedance)	balanced; at 1770 MHz	–	90	–	Ω
C_{iLO}	LO input inductance (imaginary part of the parallel input impedance)	balanced; at 1770 MHz	–	5	–	nH
RL_{iLO}	return loss on matched input (including standby mode)	note 1	10	15	–	dB
ΔRL_{iLO}	return loss variation between SX, SRX and STX modes	linear S_{11} variation; note 1	–	20	–	mU
P_{iLO}	LO input power level		–10	–6	0	dBm
RI_{LO}	reverse isolation	LOIN to RFIN at LO frequency; note 2	40	–	–	dB
Transmit section (transmit section enabled)						
Z_{LTX}	TX IF typical load impedance	balanced	–	500	–	Ω
RL_{oTX}	return loss on matched transmitter IF output	note 1	11	15	–	dB
R_{iTX}	TX RF input resistance (real part of the parallel input impedance)	balanced; at 1880 MHz	–	60	–	Ω
C_{iTX}	TX RF input capacitance (imaginary part of the parallel input impedance)	balanced; at 1880 MHz	–	1	–	pF
f_{iTX}	TX mixer input frequency		1600	–	2000	MHz
RL_{iTX}	return loss on matched TX input	note 1	10	15	–	dB
G_{CPTX}	conversion power gain	differential transmitter inputs to differential transmitter IF outputs loaded with 500 Ω differential	6	9	12	dB
f_{oTX}	TX output frequency		50	–	400	MHz
$CP1_{TX}$	1 dB input compression point	note 1	–25	–22	–	dBm
$IP2_{TX}$	2nd order intercept point	note 2	–	+22	–	dBm
$IP3_{TX}$	3rd order intercept point	note 2	–20	–16	–	dBm
NF_{TX}	noise figure	double sideband; notes 2 and 3	–	5	9	dB
I_{TX}	isolation	LOIN to TXIN; note 2	40	–	–	dB
RI_{TX}	reverse isolation	TXIN to LOIN; note 2	38	–	–	dB
Timing						
t_{stu}	start-up time of each block		1	5	20	µs

Notes

1. Measured and guaranteed only on UAA2077CM PCS demonstration board at T_{amb} = 25 °C.
2. Measured and guaranteed only on UAA2077CM PCS demonstration board.
3. This value includes printed-circuit board and balun losses.

INTERNAL PIN CONFIGURATION

PIN	SYMBOL	DC VOLTAGE (V)	EQUIVALENT CIRCUIT
1	TXINA	2.15	
2	TXINB	2.15	
5	RFINA	2.0	
6	RFINB	2.0	
3	V_{CCLNA}	3.75	
8	LNAGND	0	
9	SXON		
10	SBS		
11	TXON		
12	RXON		
13	LOINB	2.9	
14	LOINA	2.9	
15	V_{CCLO}	3.75	
16	LOGND	0	

PIN	SYMBOL	DC VOLTAGE (V)	EQUIVALENT CIRCUIT
17	IFA		
18	IFB		
19	TXOA		
20	TXOB		

APPLICATION INFORMATION

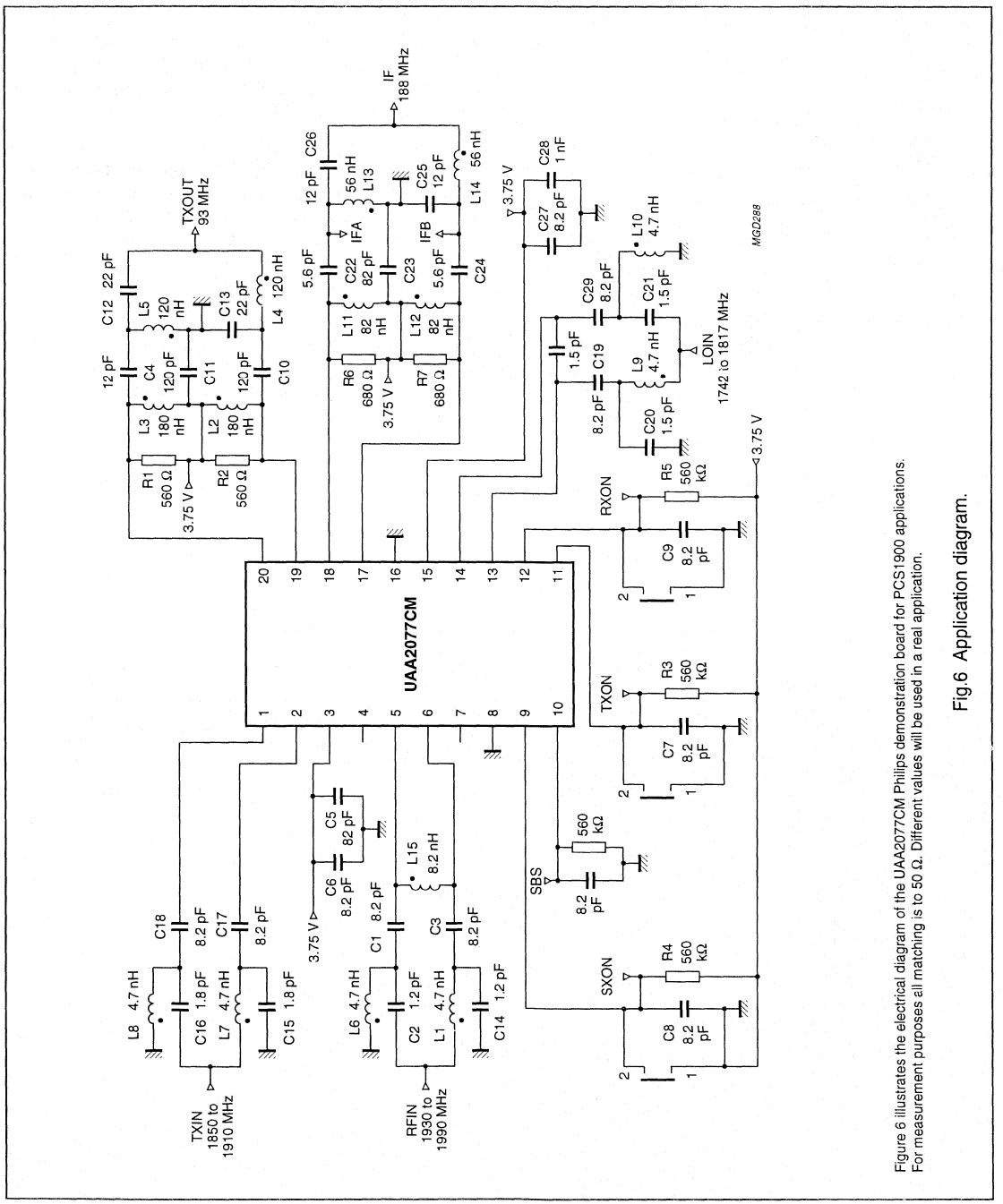


Figure 6 illustrates the electrical diagram of the UAA2077CM Philips demonstration board for PCS1900 applications. For measurement purposes all matching is to 50 Ω. Different values will be used in a real application.

Fig.6 Application diagram.

Advanced pager receiver UAA2080

FEATURES

- Wide frequency range: VHF, UHF and 900 MHz bands
- High sensitivity
- High dynamic range
- Electronically adjustable filters on chip
- Suitable for data rates up to 2400 bits/s
- Wide frequency offset and deviation range
- Fully POCSAG compatible FSK receiver
- Power on/off mode selectable by the chip enable input
- Low supply voltage; low power consumption
- High integration level
- Interfaces directly to the PCA5000A, PCF5001 and PCD5003 POCSAG decoders.

APPLICATIONS

- Wide area paging
- On-site paging
- Telemetry
- RF security systems
- Low bit-rate wireless data links.

GENERAL DESCRIPTION

The UAA2080 is a high-performance low-power radio receiver circuit primarily intended for VHF, UHF and 900 MHz pager receivers for wide area digital paging systems, employing direct FM non-return-to-zero (NRZ) frequency shift keying (FSK).

The receiver design is based on the direct conversion principle where the input signal is mixed directly down to the baseband by a local oscillator on the signal frequency. Two complete signal paths with signals of 90° phase difference are required to demodulate the signal.
All channel selectivity is provided by the built-in IF filters. The circuit makes extensive use of on-chip capacitors to minimize the number of external components.

The UAA2080 was designed to operate together with the PCA5000A, PCF5001 or PCD5003 POCSAG decoders, which contain a digital input filter for optimum call success rate.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UAA2080H	LQFP32	plastic low profile quad flat package; 32 leads; body 7 × 7 × 1.4 mm	SOT358-1
UAA2080T	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
UAA2080U	28 pads	naked die; see Fig.9	

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		1.9	2.05	3.5	V
I_P	supply current		2.3	2.7	3.2	mA
$I_{P(off)}$	stand-by current		–	–	3	μA
$P_{i(ref)}$	RF input sensitivity	BER ≤ $^3/_{100}$; ±4 kHz deviation; data rate 1200 bits/s; T_{amb} = 25 °C				
		$f_{i(RF)}$ = 173 MHz	–	−126.5	−123.5	dBm
		$f_{i(RF)}$ = 470 MHz	–	−124.5	−121.5	dBm
		$f_{i(RF)}$ = 930 MHz	–	−120.0	−114.0	dBm
$P_{i(mix)}$	mixer input sensitivity	BER ≤ $^3/_{100}$; $f_{i(RF)}$ = 470 MHz; ±4 kHz deviation; data rate 1200 bits/s; T_{amb} = 25 °C	–	−115.0	−110.0	dBm
V_{th}	detection threshold for battery LOW indicator		1.95	2.05	2.15	V
T_{amb}	operating ambient temperature		−10	–	+70	°C

BLOCK AND TEST DIAGRAMS (173 MHz)

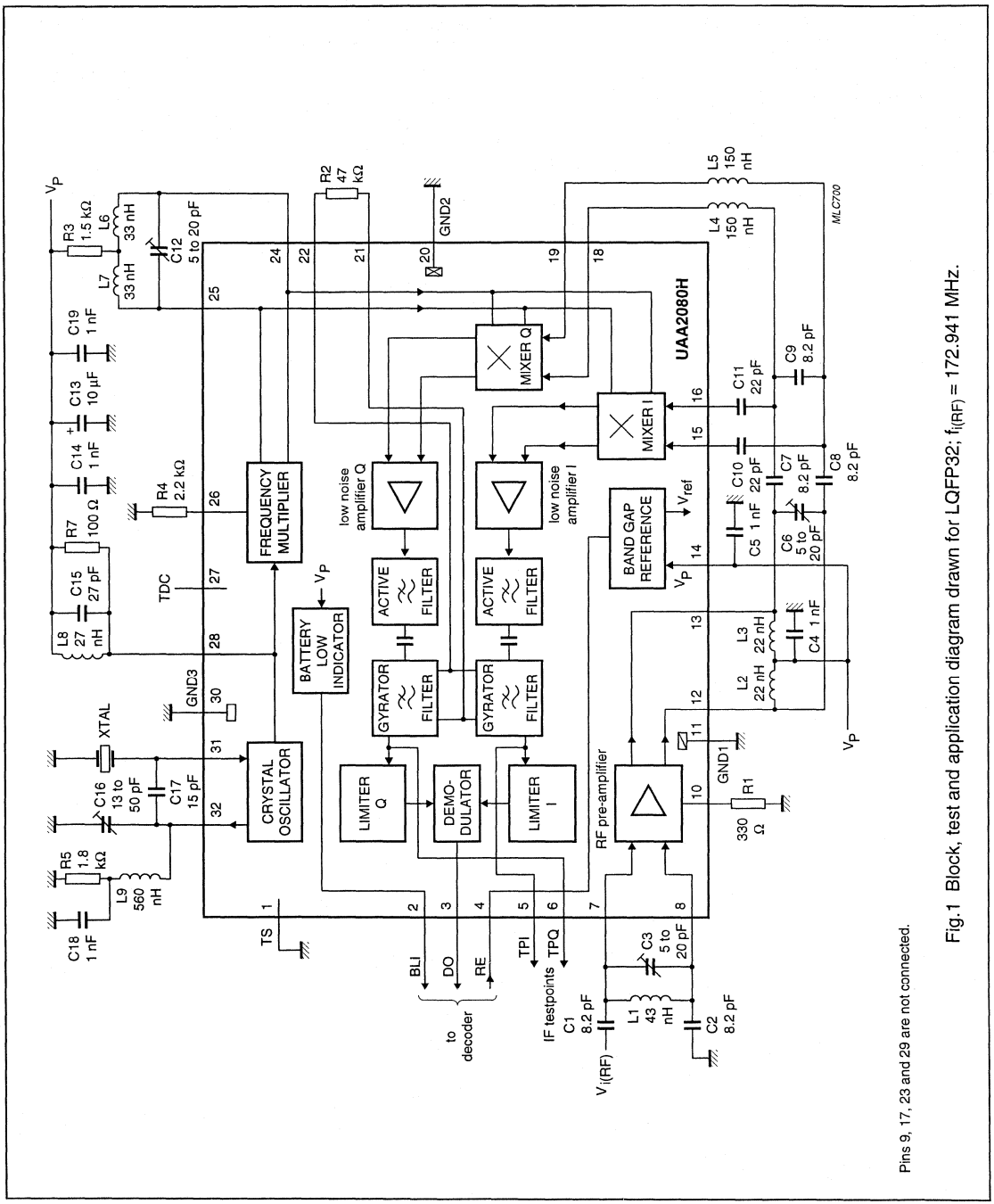


Fig.1 Block, test and application diagram drawn for LQFP32; $f_{i(RF)}$ = 172.941 MHz.

Pins 9, 17, 23 and 29 are not connected.

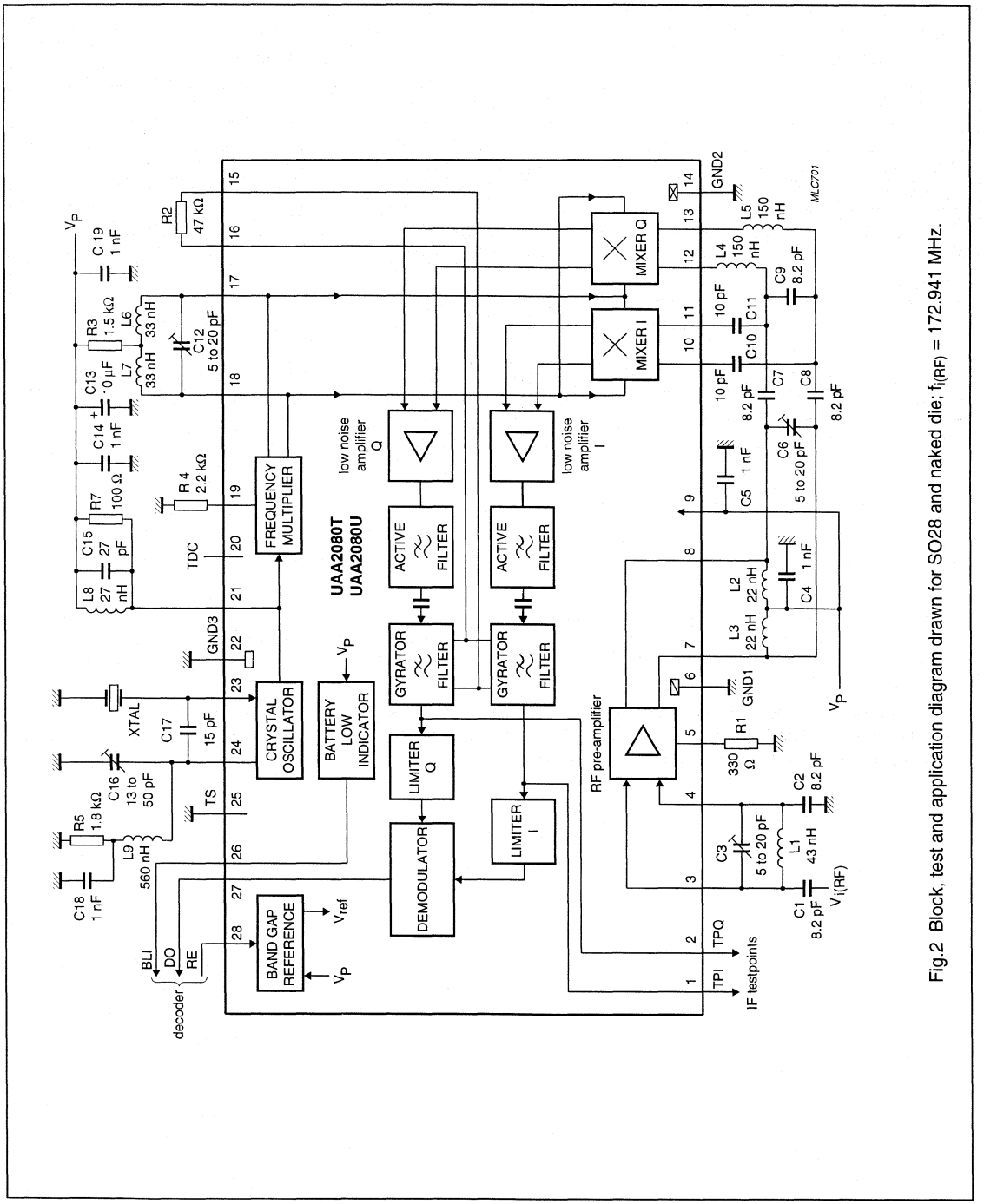


Fig.2 Block, test and application diagram drawn for SO28 and naked die; $f_{i(RF)}$ = 172.941 MHz.

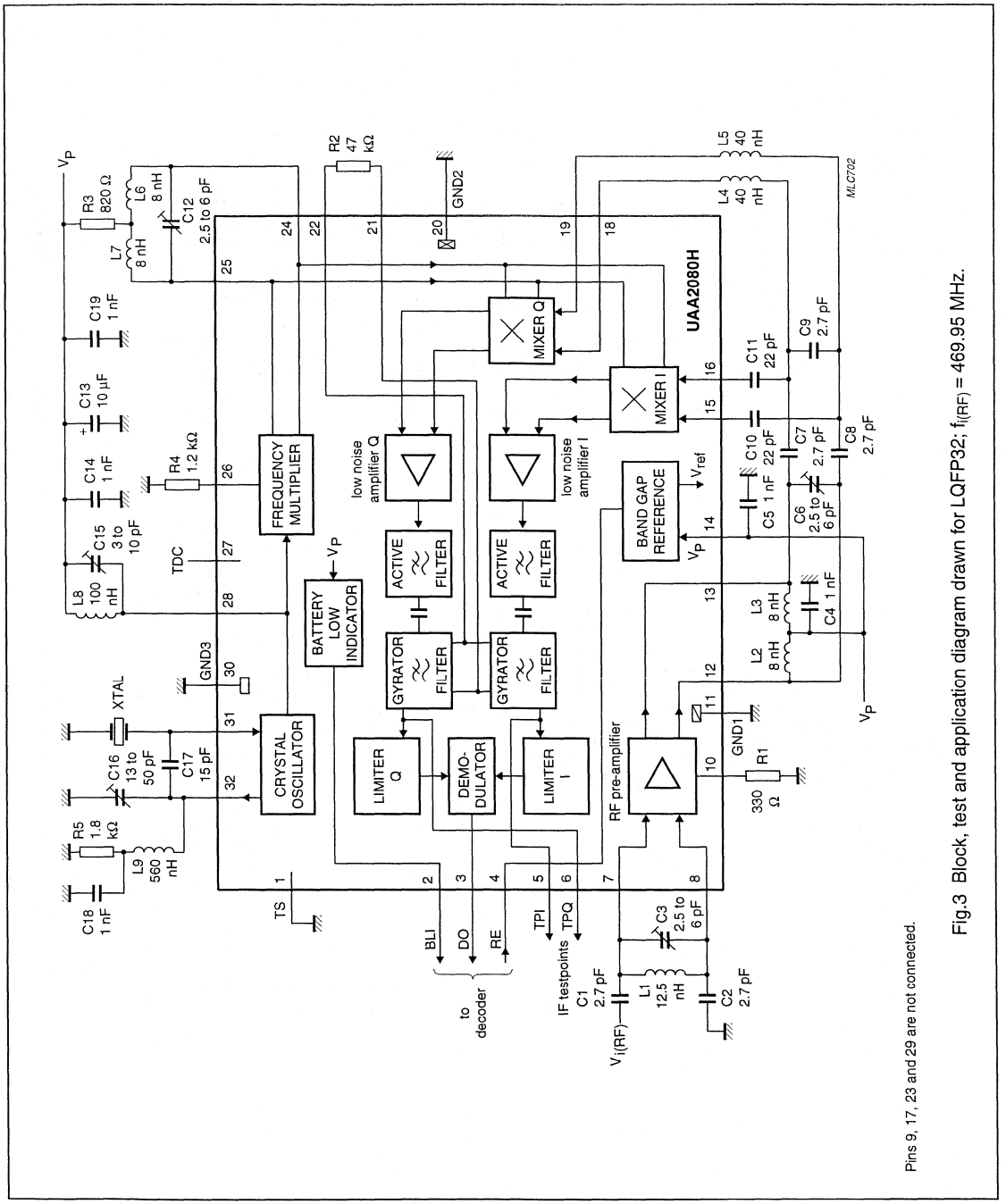
Table 1 Tolerances of components shown in Figs 1 and 2 (notes 1 and 2)

COMPONENT	TOLERANCE (%)	REMARK
Inductances		
L1	±5	Q_{min} = 100 at 173 MHz
L2, L3, L6, L7	±20	Q_{min} = 50 at 173 MHz; TC = (+25 to +125) × 10^{-6}/K
L4, L5	±10	Q_{min} = 30 at 173 MHz; TC = (+25 to +125) × 10^{-6}/K
L8	±20	Q_{min} = 30 at 173 MHz; TC = (+25 to +125) × 10^{-6}/K
L9	±10	Q_{min} = 30 at 57 MHz; TC = (+25 to +125) × 10^{-6}/K
Resistors		
R1 to R7	±2	TC = +50 × 10^{-6}/K
Capacitors		
C1, C2, C7, C8, C9, C15	±5	TC = (0 ±30) × 10^{-6}/K; tan δ ≤ 30 × 10^{-4} at 1 MHz
C3, C6, C12	–	TC = (−750 ±300) × 10^{-6}/K; tan δ ≤ 50 × 10^{-4} at 1 MHz
C4, C5, C14, C18, C19	±10	TC = (0 ±30) × 10^{-6}/K; tan δ ≤ 10 × 10^{-4} at 1 MHz
C10, C11	±5	TC = (0 ±30) × 10^{-6}/K; tan δ ≤ 21 × 10^{-4} at 1 MHz
C13	±20	
C16	–	TC = (−1700 ±500) × 10^{-6}/K; tan δ ≤ 50 × 10^{-4} at 1 MHz
C17	±5	TC = (0 ±30) × 10^{-6}/K; tan δ ≤ 26 × 10^{-4} at 1 MHz

Notes

1. Recommended crystal: f_{XTAL} = 57.647 MHz (crystal with 8 pF load), 3rd overtone, pullability >2.75 × 10^{-6}/pF (change in frequency between series resonance and resonance with 8 pF series capacitor at 25 °C), dynamic resistance R1 < 40 Ω, Δf = ±5 × 10^{-6} for T_{amb} = −10 to +55 °C with 25 °C reference, calibration plus aging tolerance: −5 × 10^{-6} to +15 × 10^{-6}.
2. This crystal recommendation is based on economic aspects and practical experience. Normally the spreads for R1, pullability and calibration do not show their worst case limits simultaneously in one crystal. In such a rare event, the tuning range will be reduced to an insufficient level.

BLOCK AND TEST DIAGRAMS (470 MHz)



Pins 9, 17, 23 and 29 are not connected.

Fig.3 Block, test and application diagram drawn for LQFP32; $f_{i(RF)}$ = 469.95 MHz.

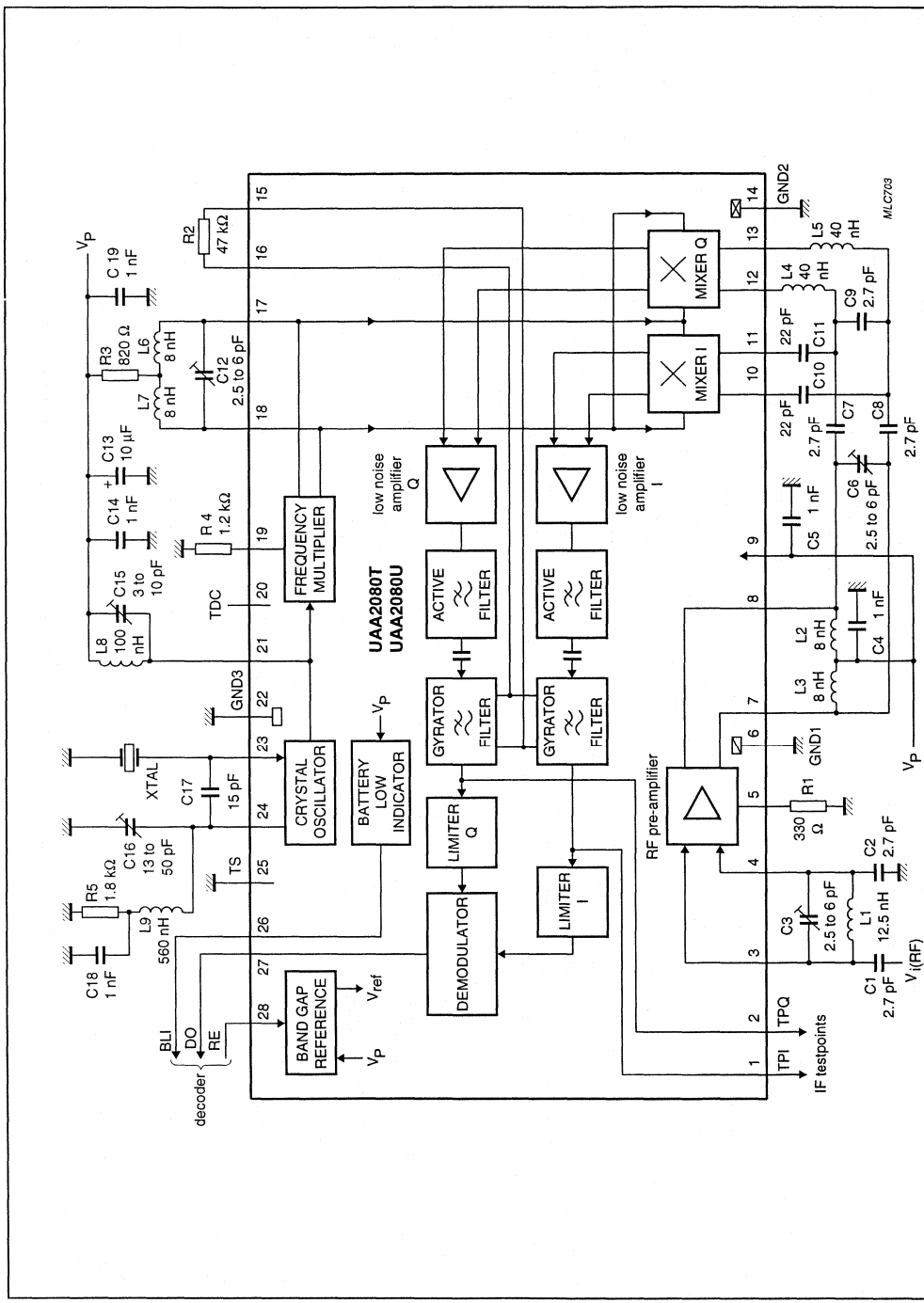


Fig.4 Block, test and application diagram drawn for SO28 and naked die; $f_{i(RF)}$ = 469.95 MHz.

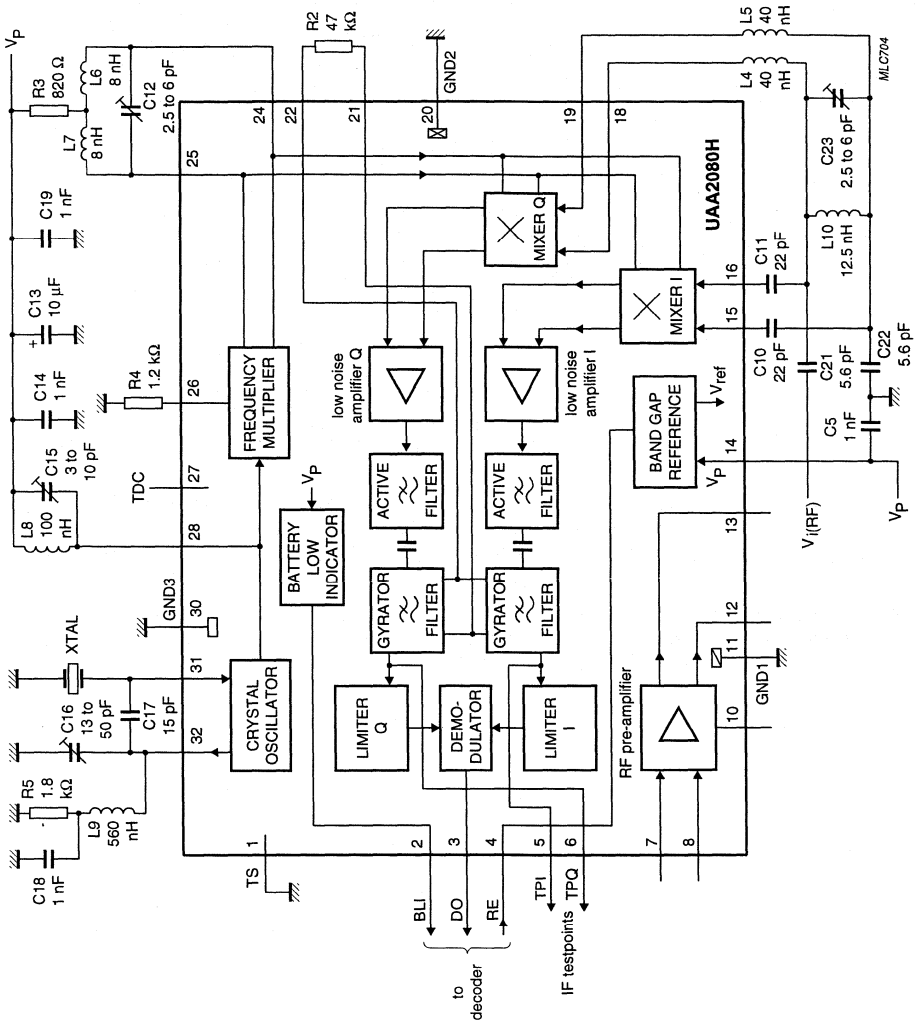


Fig.5 Mixer input sensitivity test circuit; $f_{i(RF)}$ = 469.95 MHz.

Table 2 Tolerances of components shown in Figs 3, 4 and 5 (notes 1 and 2)

COMPONENT	TOLERANCE (%)	REMARK
Inductances		
L1, L10	±5	Q_{min} = 145 at 470 MHz
L2, L3, L6, L7	±20	Q_{min} = 50 at 470 MHz; TC = (+25 to +125) × 10^{-6}/K
L4, L5	±10	Q_{min} = 40 at 470 MHz; TC = (+25 to +125) × 10^{-6}/K
L8	±10	Q_{min} = 30 at 156 MHz; TC = (+25 to +125) × 10^{-6}/K
L9	±10	Q_{min} = 40 at 78 MHz; TC = (+25 to +125) × 10^{-6}/K
Resistors		
R1 to R5	±2	TC = +50 × 10^{-6}/K
Capacitors		
C1, C2, C7, C8, C9	±5	TC = (0 ±30) × 10^{-6}/K; tan δ ≤ 30 × 10^{-4} at 1 MHz
C3, C6, C12, C23	–	TC = (−750 ±300) × 10^{-6}/K; tan δ ≤ 50 × 10^{-4} at 1 MHz
C4, C5, C14, C18 to C22	±10	TC = (0 ±30) × 10^{-6}/K; tan δ ≤ 10 × 10^{-4} at 1 MHz
C10, C11	±5	TC = (0 ±30) × 10^{-6}/K; tan δ ≤ 21 × 10^{-4} at 1 MHz
C13	±20	
C16	–	TC = (−1700 ±500) × 10^{-6}/K; tan δ ≤ 50 × 10^{-4} at 1 MHz
C17	±5	TC = (0 ±30) × 10^{-6}/K; tan δ ≤ 26 × 10^{-4} at 1 MHz

Notes

1. Recommended crystal: f_{XTAL} = 78.325 MHz (crystal with 8 pF load), 3rd overtone, pullability >2.75 × 10^{-6}/pF (change in frequency between series resonance and resonance with 8 pF capacitor at 25 °C), dynamic resistance R1 < 30 Ω, Δf = ±5 × 10^{-6} for T_{amb} = −10 to +55 °C with 25 °C reference, calibration plus aging tolerance: −5 × 10^{-6} to +15 × 10^{-6}.
2. This crystal recommendation is based on economic aspects and practical experience. Normally the spreads for R1, pullability and calibration do not show their worst case limits simultaneously in one crystal. In such a rare event, the tuning range will be reduced to an insufficient level.

BLOCK AND TEST DIAGRAM (930 MHz)

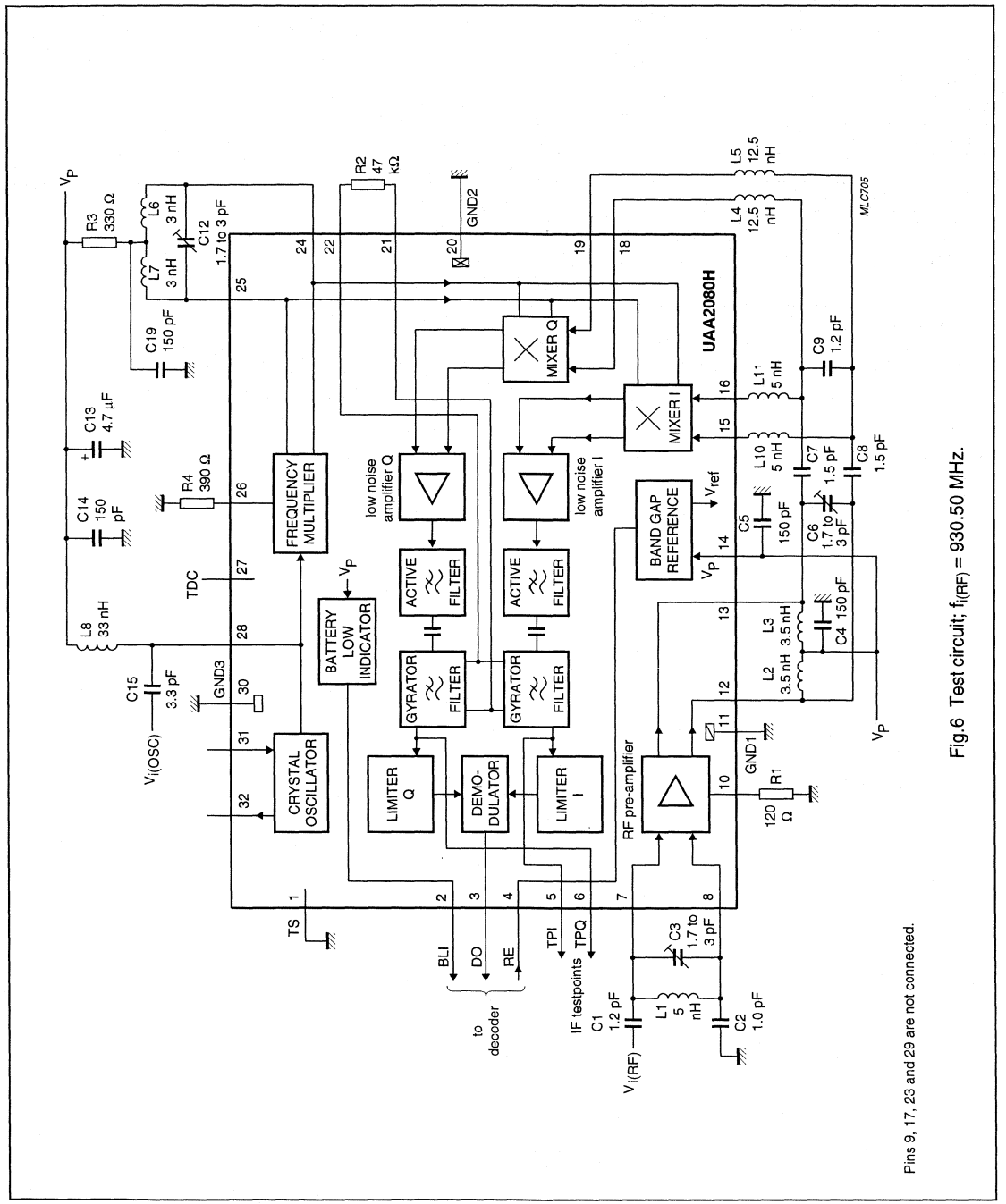


Fig.6 Test circuit; $f_{i(RF)}$ = 930.50 MHz.

Table 3 Tolerances of components shown in Fig.6 (note 1)

COMPONENT	TOLERANCE (%)	REMARK
Inductances		
L1	±10	Q_{typ} = 150 at 930 MHz
L2, L3, L6, L7	–	microstrip inductor
L4, L5	±5	Q_{typ} = 100 at 930 MHz
L8	±10	Q_{typ} = 65 at 310 MHz
L10, L11	±10	Q_{typ} = 150 at 930 MHz
Resistors		
R1 to R4	±2	TC = (0 ±200) × 10^{-6}/K;
Capacitors		
C1, C2, C7, C8, C9, C15	±5	TC = (0 ±30) × 10^{-6}/K; tan δ ≤ 30 × 10^{-4} at 1 MHz
C3, C6, C12	–	TC = (0 ±200) × 10^{-6}/K; tan δ ≤ 30 × 10^{-4} at 1 MHz
C4, C5, C14, C19	±10	TC = (0 ±30) × 10^{-6}/K; tan δ ≤ 10 × 10^{-4} at 1 MHz
C13	±20	

Note

1. The external oscillator signal $V_{i(OSC)}$ has a frequency of f_{OSC} = 310.1667 MHz.

PINNING (LQFP32)

SYMBOL	PIN	DESCRIPTION
TS	1	test switch; connection to ground for normal operation
BLI	2	battery LOW indicator output
DO	3	data output
RE	4	receiver enable input
TPI	5	IF test point; I channel
TPQ	6	IF test point; Q channel
VI1RF	7	pre-amplifier RF input 1
VI2RF	8	pre-amplifier RF input 2
n.c.	9	not connected
RRFA	10	external emitter resistor for pre-amplifier
GND1	11	ground 1 (0 V)
VO2RF	12	pre-amplifier RF output 2
VO1RF	13	pre-amplifier RF output 1
V_P	14	supply voltage
VI2MI	15	I channel mixer input 2
VI1MI	16	I channel mixer input 1
n.c.	17	not connected
VI1MQ	18	Q channel mixer input 1
VI2MQ	19	Q channel mixer input 2
GND2	20	ground 2 (0 V)
COM	21	gyrator filter resistor; common line
RGYR	22	gyrator filter resistor
n.c.	23	not connected
VO1MUL	24	frequency multiplier output 1
VO2MUL	25	frequency multiplier output 2
RMUL	26	external emitter resistor for frequency multiplier
TDC	27	DC test point; no external connection for normal operation
OSC	28	oscillator collector
n.c.	29	not connected
GND3	30	ground 3 (0 V)
OSB	31	oscillator base; crystal input
OSE	32	oscillator emitter

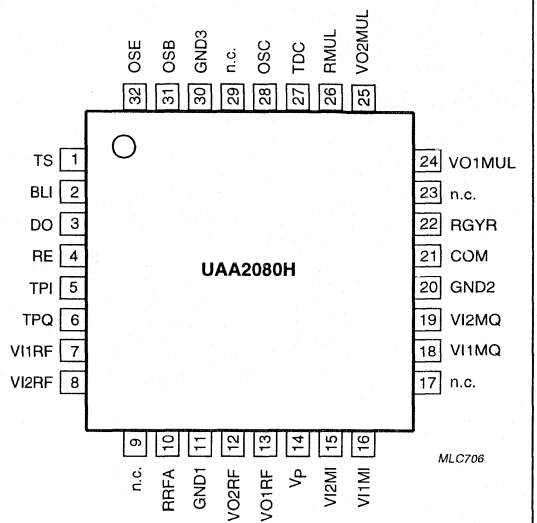


Fig.7 Pin configuration; LQFP32.

PINNING (SO28)

SYMBOL	PIN	DESCRIPTION
TPI	1	IF test point; I channel
TPQ	2	IF test point; Q channel
VI1RF	3	pre-amplifier RF input 1
VI2RF	4	pre-amplifier RF input 2
RRFA	5	external emitter resistor for pre-amplifier
GND1	6	ground 1 (0 V)
VO2RF	7	pre-amplifier RF output 2
VO1RF	8	pre-amplifier RF output 1
V_P	9	supply voltage
VI2MI	10	I channel mixer input 2
VI1MI	11	I channel mixer input 1
VI1MQ	12	Q channel mixer input 1
VI2MQ	13	Q channel mixer input 2
GND2	14	ground 2 (0 V)
COM	15	gyrator filter resistor; common line
RGYR	16	gyrator filter resistor
VO1MUL	17	frequency multiplier output 1
VO2MUL	18	frequency multiplier output 2
RMUL	19	external emitter resistor for frequency multiplier
TDC	20	DC test point; no external connection for normal operation
OSC	21	oscillator collector
GND3	22	ground 3 (0 V)
OSB	23	oscillator base; crystal input
OSE	24	oscillator emitter
TS	25	test switch; connection to ground for normal operation
BLI	26	battery LOW indicator output
DO	27	data output
RE	28	receiver enable input

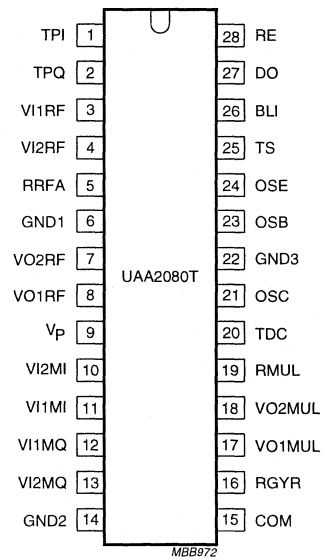
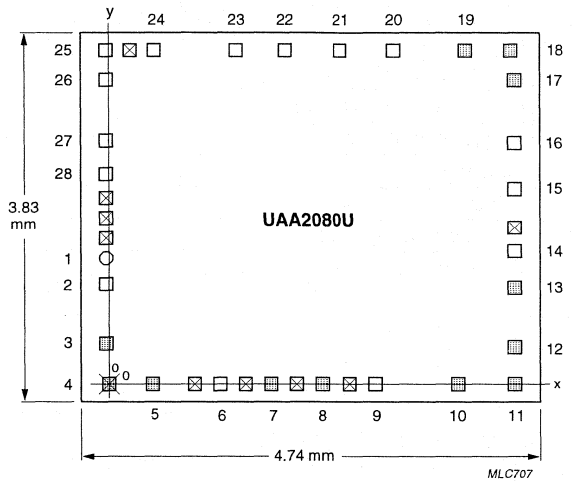


Fig.8 Pin configuration; SO28.

CHIP DIMENSIONS AND BONDING PAD LOCATIONS

See Table 4 for bonding pad description and locations for x/y co-ordinates.



Where:

- ○ Pad number 1 (diameter 124 µm)
- □ Pad 124 µm x 124 µm
- ⊠ Pad not used
- ▨ Pad 100 µm x 100 µm
- ⊠ Pad 100 µm x 100 µm with reference point

Chip area: 18.15 mm^2.
Chip thickness: 380 ±20 µm.
Drawing not to scale.

Fig.9 Bonding pad locations.

Table 4 Bonding pad centre locations (dimensions in μm)

SYMBOL	PAD	DESCRIPTION	x	y
TPI	1	IF test point; I channel	−32	1296
TPQ	2	IF test point; Q channel	−32	1000
VI1RF	3	pre-amplifier RF input 1	−32	360
VI2RF	4	pre-amplifier RF input 2; note 1	0	0
RRFA	5	external emitter resistor for pre-amplifier	472	0
GND1	6	ground 1 (0 V)	1160	0
VO2RF	7	pre-amplifier RF output 2	1688	0
VO1RF	8	pre-amplifier RF output 1	2232	0
V_P	9	supply voltage	2760	0
VI2MI	10	I channel mixer input 2	3608	0
VI1MI	11	I channel mixer input 1	4216	0
VI1MQ	12	Q channel mixer input 1	4216	360
VI2MQ	13	Q channel mixer input 2	4216	960
GND2	14	ground 2 (0 V)	4216	1360
COM	15	gyrator filter resistor; common line	4216	2024
RGYR	16	gyrator filter resistor	4216	2496
VO1MUL	17	frequency multiplier output 1	4216	3136
VO2MUL	18	frequency multiplier output 2	4176	3456
RMUL	19	external emitter resistor for frequency multiplier	3668	3458
TDC	20	DC test point; no external connection for normal operation	2952	3456
OSC	21	oscillator collector	2312	3456
GND3	22	ground 3 (0 V)	1832	3456
OSB	23	oscillator base; crystal input	1328	3456
OSE	24	oscillator emitter	432	3456
TS	25	test switch; connection to ground for normal operation	−32	3456
BLI	26	battery LOW indicator output	−32	3136
DO	27	data output	−32	2512
RE	28	receiver enable input	−32	2152
		lower left corner of chip (typical values)	−278	−186

Note

1. All x/y co-ordinates are referenced to the centre of pad 4 (VI2RF); see Fig.9.

INTERNAL CIRCUITS

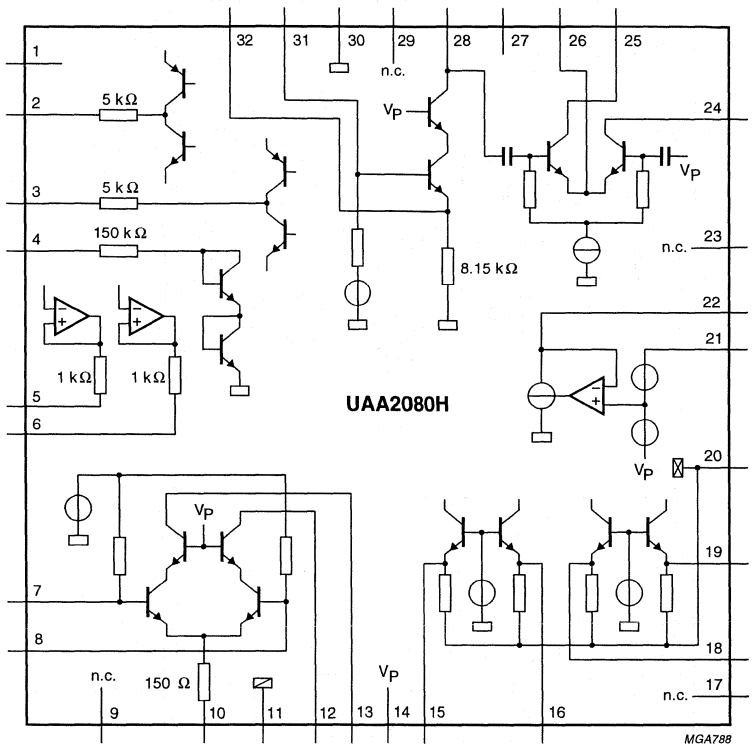


Fig.10 Internal circuits drawn for LQFP32.

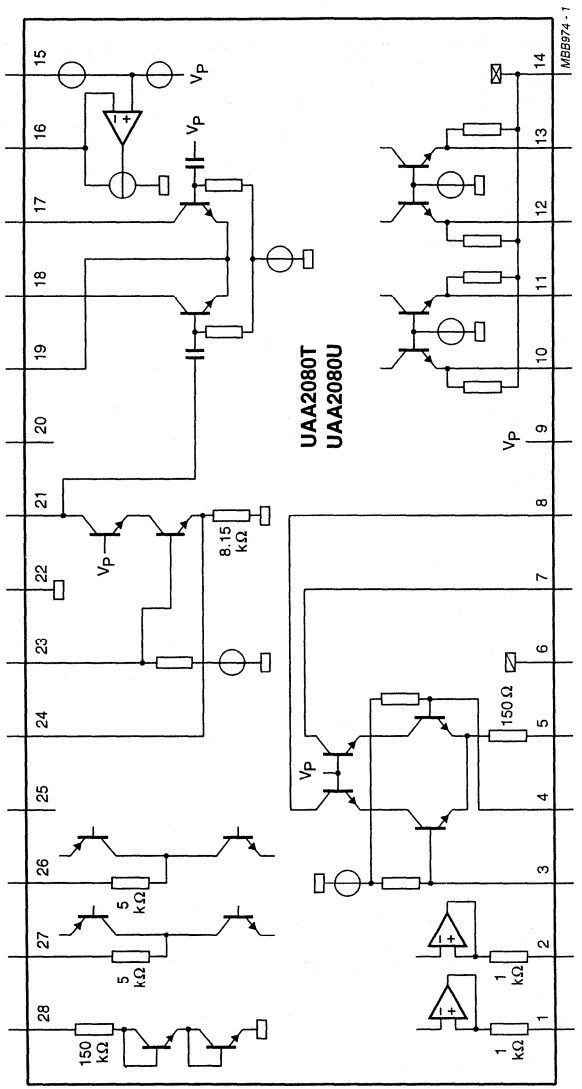


Fig.11 Internal circuits drawn for SO28 and naked die.

FUNCTIONAL DESCRIPTION

The complete circuit consists of the following functional blocks as shown in Figs 1 to 6.

Radio frequency amplifier

The RF amplifier is an emitter-coupled pair driving a balanced cascode stage, which drives an external balanced tuned circuit. Its bias current is set by an external 300 Ω resistor R1 to typically 770 μA. With this bias current the optimum source resistance is 1.3 kΩ at VHF and 1.0 kΩ at UHF. At 930 MHz a higher bias current is required to achieve optimum gain. A value of 120 Ω is used for R1, which corresponds with a bias current of approximately 1.3 mA and an optimum source resistance of approximately 600 Ω.The capacitors C1 and C2 transform a 50 Ω source resistance to this optimum value. The output drives a tuned circuit with capacitive divider (C7, C8 and C9) to provide maximum power transfer to the phase-splitting network and the mixers.

Mixers

The double balanced mixers consist of common base input stages and upper switching stages driven from the frequency multiplier. The 300 Ω input impedance of each mixer acts together with external components (C10, C11; L4, L5 respectively) as phase shifter/power splitter to provide a differential phase shift of 90 degrees between the I channel and the Q channel. At 930 MHz all external phase shifter components are inductive (L10, L11; L4, L5).

Oscillator

The oscillator is based on a transistor in common collector configuration. It is followed by a cascode stage driving a tuned circuit which provides the signal for the frequency multiplier. The oscillator bias current (typically 250 μA) is determined by the 1.8 kΩ external resistor R5.
The oscillator frequency is controlled by an external 3rd overtone crystal in parallel resonance mode. External capacitors between base and emitter (C17) and from emitter to ground (C16) make the oscillator transistor appear as having a negative resistance for small signals; this causes the oscillator to start. Inductance L9 connected in parallel with capacitor C16 to the emitter of the oscillator transistor prevents oscillation at the fundamental frequency of the crystal.

The resonant circuit at output pin OSC selects the second harmonic of the oscillator frequency. In other applications a different multiplication factor may be chosen.

At 930 MHz an external oscillator circuit is required to provide sufficient local oscillator signal for the frequency multiplier.

Frequency multiplier

The frequency multiplier is an emitter-coupled pair driving an external balanced tuned circuit. Its bias current is set by external resistor R4 to typically 190 μA (173 MHz), 350 μA (470 MHz) and 1 mA (930 MHz). The oscillator signal is internally AC coupled to one input of the emitter-coupled pair while the other input is internally grounded via a capacitor. The frequency multiplier output signal between pins VO1MUL and VO2MUL drives the upper switching stages of the mixers. The bias voltage on pins VO1MUL and VO2MUL is set by external resistor R3 to allow sufficient voltage swing at the mixer outputs. The value of R3 depends on the operating frequency: 1.5 kΩ (173 MHz), 820 Ω (470 MHz) and 330 Ω (930 MHz).

Low noise amplifiers, active filters and gyrator filters

The low noise amplifiers ensure that the noise of the following stages does not affect the overall noise figure. The following active filters before the gyrator filters reduce the levels of large signals from adjacent channels. Internal AC couplings block DC offsets from the gyrator filter inputs.

The gyrator filters implement the transfer function of a 7th order elliptic filter. Their cut-off frequencies are determined by the 47 kΩ external resistor R2 between pins RGYR and COM. The gyrator filter output signals are available on IF test pins TPI and TPQ.

Limiters

The gyrator filter output signals are amplified in the limiter amplifiers to obtain IF signals with removed amplitude information.

Demodulator

The limiter amplifier output signals are fed to the demodulator. The demodulator output DO is going LOW or HIGH depending upon which of the input signals has a phase lead.

Battery LOW indicator

The battery LOW indicator senses the supply voltage and sets its output HIGH when the supply voltage is less than V_{th} (typically 2.05 V). Low battery warning is available at BLI.

Band gap reference

The whole chip can be powered-up and powered-down by enabling and disabling the band gap reference via the receiver enable pin RE.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).
Ground pins GND1, GND2 and GND3 connected together.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage	−0.3	+8.0	V
V_{es}	electrostatic handling (note 1)			
	pins VI1RF and VI2RF	−1500	+2000	V
	pin RRFA	−500	+2000	V
	pins VO1RF and VO2RF	−2000	+250	V
	pins V_P and OSB	−500	+500	V
	pins OSC and OSE	−2000	+500	V
	other pins	−2000	+2000	V
T_{stg}	storage temperature	−55	+125	°C
T_{amb}	operating ambient temperature	−10	+70	°C

Note

1. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ resistor.

DC CHARACTERISTICS

V_P = 2.05 V; T_{amb} = −10 to +70 °C (typical values at T_{amb} = 25 °C); measurements taken in test circuit Figs 1, 2, 3 or 4 with crystal at pin OSB disconnected; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage		1.9	2.05	3.5	V
I_P	supply current	V_{RE} = HIGH; $f_{i(RF)}$ = 173 and 470 MHz	2.3	2.7	3.2	mA
		V_{RE} = HIGH; $f_{i(RF)}$ = 930 MHz	2.9	3.4	3.9	mA
$I_{P(off)}$	stand-by current	V_{RE} = LOW	–	–	3	µA
Receiver enable input (pin RE)						
V_{IH}	HIGH level input voltage		1.4	–	V_P	V
V_{IL}	LOW level input voltage		0	–	0.3	V
I_{IH}	HIGH level input current	V_{IH} = V_P = 3.5 V	–	–	20	µA
V_{IL}	LOW level input current	V_{IL} = 0 V	0	–	−1.0	µA
Battery LOW indicator output (pin BLI)						
V_{OH}	HIGH level output voltage	$V_P < V_{th}$; I_{BLI} = −10 µA	V_P − 0.5	–	–	V
V_{OL}	LOW level output voltage	$V_P > V_{th}$; I_{BLI} = +10 µA	–	–	0.5	V
V_{th}	voltage threshold for battery LOW indicator		1.95	2.05	2.15	V
Demodulator output (pin DO)						
V_{OH}	HIGH level output voltage	I_{DO} = −10 µA	V_P − 0.5	–	–	V
V_{OL}	LOW level output voltage	I_{DO} = +10 µA	–	–	0.5	V

AC CHARACTERISTICS (173 MHz)

V_P = 2.05 V; T_{amb} = 25 °C; test circuit Figs 1 or 2; $f_{i(RF)}$ = 172.941 MHz with ±4.0 kHz deviation; 1200 baud pseudo random bit sequence modulation (t_r = 250 ±25 µs measured between 10% and 90% of voltage amplitude) and 20 kHz channel spacing; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Radio frequency input						
$P_{i(ref)}$	input sensitivity ($P_{i(ref)}$ is the maximum available power at the RF input of the test board)	BER ≤ $^3/_{100}$; note 1	–	–126.5	–123.5	dBm
		T_{amb} = –10 to +70 °C; note 2	–	–	–120.5	dBm
		V_P = 1.9 V	–	–	–117.5	dBm
Mixers to demodulator						
α_{acs}	adjacent channel selectivity	T_{amb} = 25 °C	69	72	–	dB
		T_{amb} = –10 to +70 °C	67	–	–	dB
α_{ci}	IF filter channel imbalance		–	–	2	dB
α_c	co-channel rejection		–	4	7	dB
α_{sp}	spurious immunity		50	60	–	dB
α_{im}	intermodulation immunity		55	60	–	dB
α_{bl}	blocking immunity	Δf > ±1 MHz; note 3	78	85	–	dB
f_{offset}	frequency offset range (3 dB degradation in sensitivity)	deviation f = ±4.0 kHz	±2.0	–	–	kHz
		deviation f = ±4.5 kHz	±2.5	–	–	kHz
Δf_{dev}	deviation range (3 dB degradation in sensitivity)		2.5	–	7.0	kHz
t_{on}	receiver turn-on time	data valid after setting RE input HIGH; note 4	–	–	5	ms

Notes

1. The bit error rate BER is measured using the test facility shown in Fig.13. Note that the BER test facility contains a digital input filter equivalent to the one used in the PCA5000A, PCF5001 and PCD5003 POCSAG decoders.
2. Capacitor C16 requires re-adjustment to compensate temperature drift.
3. Δf is the frequency offset between the required signal and the interfering signal.
4. Turn-on time is defined as the time from pin RE going HIGH to the reception of valid data on output pin DO. Turn-on time is measured using an external oscillator (turn-on time using the internal oscillator is dependent upon the oscillator circuitry).

AC CHARACTERISTICS (470 MHz)

V_P = 2.05 V; T_{amb} = 25 °C; test circuit Figs 3 or 4; $f_{i(RF)}$ = 469.950 MHz with ±4.0 kHz deviation; 1200 baud pseudo random bit sequence modulation (t_r = 250 ± 25 µs measured between 10% and 90% of voltage amplitude) and 20 kHz channel spacing; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Radio frequency input						
$P_{i(ref)}$	input sensitivity ($P_{i(ref)}$ is the maximum available power at the RF input of the test board)	BER ≤ $^3/_{100}$; note 1	–	–124.5	–121.5	dBm
		T_{amb} = –10 to +70 °C; note 2	–	–	–118.5	dBm
		V_P = 1.9 V	–	–	–115.5	dBm
Mixer input						
$P_{i(mix)}$	input sensitivity	BER ≤ $^3/_{100}$; note 3	–	–115.0	–110.0	dBm
Mixers to demodulator						
α_{acs}	adjacent channel selectivity	T_{amb} = 25 °C	67	70	–	dB
		T_{amb} = –10 to +70 °C	65	–	–	dB
α_{ci}	IF filter channel imbalance		–	–	2	dB
α_c	co-channel rejection		–	4	7	dB
α_{sp}	spurious immunity		50	60	–	dB
α_{im}	intermodulation immunity		55	60	–	dB
α_{bl}	blocking immunity	$\Delta f > \pm 1$ MHz; note 4	75	82	–	dB
f_{offset}	frequency offset range (3 dB degradation in sensitivity)	deviation f = ±4.0 kHz	±2.0	–	–	kHz
		deviation f = ±4.5 kHz	±2.5	–	–	kHz
Δf_{dev}	deviation range (3 dB degradation in sensitivity)		2.5	–	7.0	kHz
t_{on}	receiver turn-on time	data valid after setting RE input HIGH; note 5	–	–	5	ms

Notes

1. The bit error rate BER is measured using the test facility shown in Fig.13. Note that the BER test facility contains a digital input filter equivalent to the one used in the PCA5000A, PCF5001 and PCD5003 POCSAG decoders.
2. Capacitor C16 requires re-adjustment to compensate temperature drift.
3. Test circuit Fig.5. $P_{i(mix)}$ is the maximum available power at the input of the test board. The bit error rate BER is measured using the test facility shown in Fig.13.
4. Δf is the frequency offset between the required signal and the interfering signal.
5. Turn-on time is defined as the time from pin RE going HIGH to the reception of valid data on output pin DO. Turn-on time is measured using an external oscillator (turn-on time using the internal oscillator is dependent upon the oscillator circuitry).

AC CHARACTERISTICS (930 MHz)

V_P = 2.05 V; T_{amb} = 25 °C; test circuit Fig.6 (note 1); $f_{i(RF)}$ = 930.500 MHz with ±4.0 kHz deviation; 1200 baud pseudo random bit sequence modulation (t_r = 250 ± 25 µs measured between 10% and 90% of voltage amplitude) and 20 kHz channel spacing; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Radio frequency input						
$P_{i(ref)}$	input sensitivity ($P_{i(ref)}$ is the maximum available power at the RF input of the test board)	BER ≤ $^3/_{100}$; note 2	–	–120.0	–114.0	dBm
		V_P = 1.9 V	–	–	–108.0	dBm
Mixers to demodulator						
α_{acs}	adjacent channel selectivity	T_{amb} = 25 °C	60	69	–	dB
α_c	co-channel rejection		–	5	10	dB
α_{sp}	spurious immunity		40	60	–	dB
α_{im}	intermodulation immunity		53	60	–	dB
α_{bl}	blocking immunity	$\Delta f > \pm 1$ MHz; note 3	65	74	–	dB
f_{offset}	frequency offset range (3 dB degradation in sensitivity)	deviation f = ±4.0 kHz	±2.0	–	–	kHz
		deviation f = ±4.5 kHz	±2.5	–	–	kHz
Δf_{dev}	deviation range (3 dB degradation in sensitivity)		2.5	–	7.0	kHz
t_{on}	receiver turn-on time	data valid after setting RE input HIGH; note 4	–	–	5	ms

Notes

1. The external oscillator signal $V_{i(OSC)}$ has a frequency of f_{OSC} = 310.1667 MHz and a level of –15 dBm.
2. The bit error rate BER is measured using the test facility shown in Fig.13. Note that the BER test facility contains a digital input filter equivalent to the one used in the PCA5000A, PCF5001 and PCD5003 POCSAG decoders.
3. Δf is the frequency offset between the required signal and the interfering signal.
4. Turn-on time is defined as the time from pin RE going HIGH to the reception of valid data on output pin DO. Turn-on time is measured using an external oscillator (turn-on time using the internal oscillator is dependent upon the oscillator circuitry).

TEST INFORMATION

Tuning procedure for AC tests

1. Turn on the signal generator: $f_{gen} = f_{i(RF)} + 4$ kHz, no modulation, $V_{i(RF)} = 1$ mV (RMS).
2. Measure the IF with a counter connected to test pin TPI. Tune C16 to set the crystal oscillator to achieve $f_{IF} = 4$ kHz Change the generator frequency to $f_{gen} = f_{i(RF)} - 4$ kHz and check that f_{IF} is also 4 kHz. For a received input frequency $f_{i(RF)} = 172.941$ MHz the crystal frequency is $f_{XTAL} = 57.647$ MHz, while for $f_{i(RF)} = 469.950$ MHz the crystal frequency is $f_{XTAL} = 78.325$ MHz. For a received input frequency $f_{i(RF)} = 930.500$ MHz an external oscillator signal must be used with $f_{i(OSC)} = 310.1667$ MHz and a level of −15 dBm (for definition of crystal frequency, see Table 1).
3. Set the signal generator to nominal frequency ($f_{i(RF)}$) and turn on the modulation deviation ±4.0 kHz, 600 Hz square wave modulation, $V_{i(RF)} = 1$ mV (RMS). Note that the RF signal should be reduced in the following tests, as the receiver is tuned, to ensure $V_{o(IF)} = 10$ to 50 mV (p-p) on test pins TPI or TPQ.
4. Tune C15 (oscillator output circuit) and C12 (frequency multiplier output) to obtain a peak audio voltage on pin TPI.
5. Tune C3 and C6 (RF input and mixer input) to obtain a peak audio voltage on pin TPI. When testing the mixer input sensitivity tune C23 instead of C3 and C6 (test circuit Fig.5).
6. Check that the output signal on pin TPQ is within 3 dB in amplitude and at 90° (±20°) relative phase of the signal on pin TPI.
7. Check that data signal appears on output pin DO and proceed with the AC test.

AC test conditions

Table 5 Definitions for AC test conditions (see Table 6)

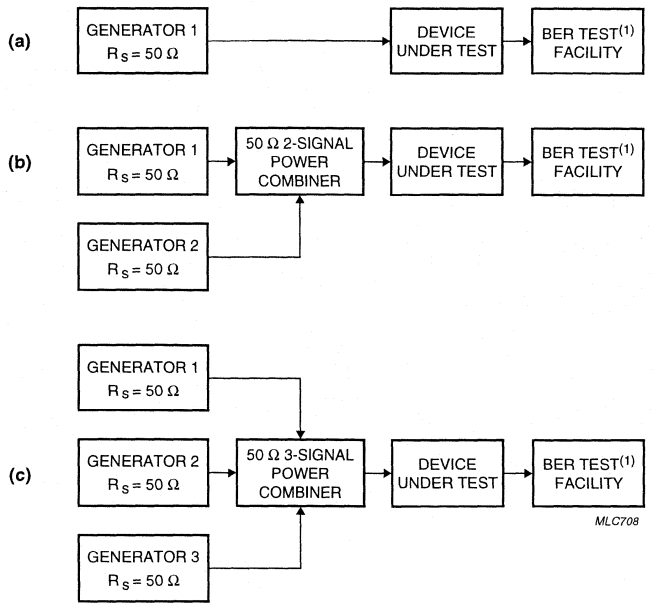
SIGNAL	DESCRIPTION
Modulated test signal 1	
Frequency	172.941, 469.950 or 930.500 MHz
Deviation	±4.0 kHz
Modulation	1200 baud pseudo random bit sequence
Rise time	250 ±25 µs (between 10% and 90% of final value)
Modulated test signal 2	
Deviation	±2.4 kHz
Modulation	400 Hz sinewave
Other definitions	
f_1	frequency of signal generator 1
f_2	frequency of signal generator 2
f_3	frequency of signal generator 3
Δf_{cs}	channel spacing (20 kHz)
P_1	maximum available power from signal generator 1 at the test board input
P_2	maximum available power from signal generator 2 at the test board input
P_3	maximum available power from signal generator 3 at the test board input
$P_{i(ref)}$	maximum available power at the test board input to give a Bit Error Rate (BER) $\leq 3/100$ for the modulated test signal 1, in the absence of interfering signals and under the conditions as specified in Chapters "AC characteristics (173 MHz)", "AC characteristics (470 MHz)" and "AC characteristics (930 MHz)"

Table 6 AC test conditions (notes 1 and 2)

SYMBOL	PARAMETER	CONDITIONS	TEST SIGNALS
α_a	adjacent channel selectivity; Fig.12(b)	$f_2 = f_1 \pm \Delta f_{CS}$ generator 1: modulated test signal 1 generator 2: modulated test signal 2	 $P_1 = P_{i(ref)} + 3$ dB $P_2 = P_1 + \alpha_{a(min)}$
α_c	co-channel rejection; Fig.12(b)	$f_2 = f_1 \pm$ up to 3 kHz generator 1: modulated test signal 1 generator 2: modulated test signal 2	 $P_1 = P_{i(ref)} + 3$ dB $P_2 = P_1 - \alpha_{c(max)}$
α_{sp}	spurious immunity; Fig.12(b)	f_2 = 100 kHz to 2 GHz generator 1: modulated test signal 1 generator 2: modulated test signal 2	 $P_1 = P_{i(ref)} + 3$ dB $P_2 = P_1 + \alpha_{sp(min)}$
α_{im}	intermodulation immunity; Fig.12(c)	$f_2 = f_1 \pm \Delta f_{cs}$; $f_3 = f_1 \pm 2\Delta f_{cs}$ generator 1: modulated test signal 1 generator 2: unmodulated generator 3: modulated test signal 2	 $P_1 = P_{i(ref)} + 3$ dB $P_2 = P_1 + \alpha_{im(min)}$ $P_3 = P_2$
α_{bl}	blocking immunity; Fig.12(b)	$f_2 = f_1 \pm 1$ MHz generator 1: modulated test signal 1 generator 2: modulated test signal 2	 $P_1 = P_{i(ref)} + 3$ dB $P_2 = P_1 + \alpha_{bl(min)}$
f_{offset}	frequency offset range; Fig.12(a)	deviation = ±4.0 kHz, $f_1 = f_{i(RF)} \pm 2$ kHz ($f_{offset(min)}$) generator 1: modulated test signal 1	 $P_1 = P_{i(ref)} + 3$ dB
Δf_{dev}	deviation range; Fig.12(a)	deviation = ±2.5 to ±7 kHz; ($\Delta f_{dev(min)}$ to $\Delta f_{dev(max)}$) generator 1: modulated test signal 1	 $P_1 = P_{i(ref)} + 3$ dB
t_{on}	receiver turn-on time; Fig.12(a)	note 3 generator 1: modulated test signal 1	 $P_1 = P_{i(ref)} + 10$ dB

Notes

1. The tests are executed without load on pins TPI and TPQ.
2. All minimum and maximum values correspond to a bit error rate (BER) $\leq 3/100$ in the wanted signal (P_1).
3. The BER measurement is started 5 ms ($t_{on(max)}$) after V_{RE} goes HIGH; BER is then measured for 100 bits (BER $\leq 3/100$).



(a) One generator.
(b) Two generators.
(c) Three generators.
(1) See Fig.13.

Fig.12 Test configurations.

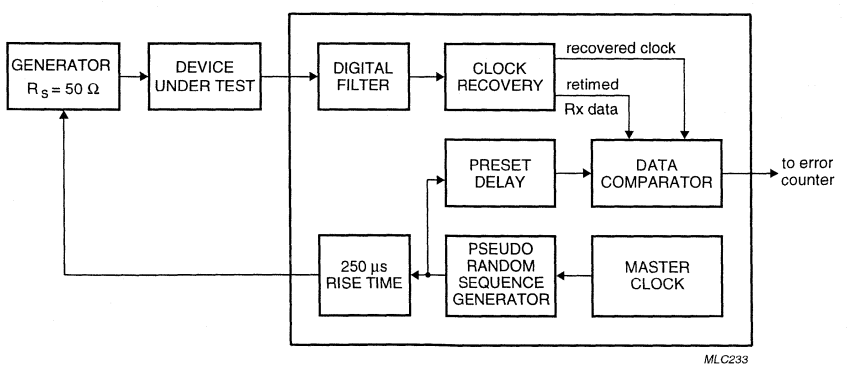


Fig.13 BER test facility.

PRINTED-CIRCUIT BOARDS

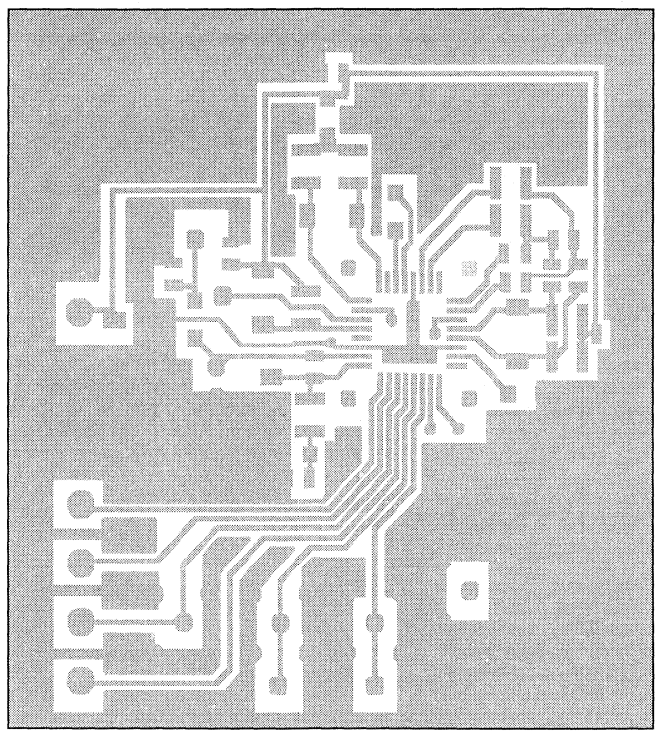


Fig.14 PCB top view for LQFP32; test circuit Figs 1 and 3.

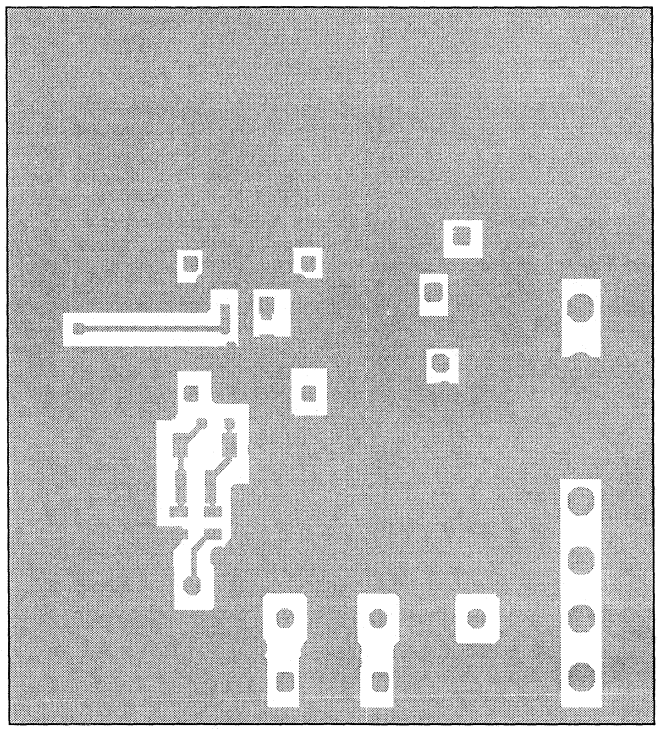
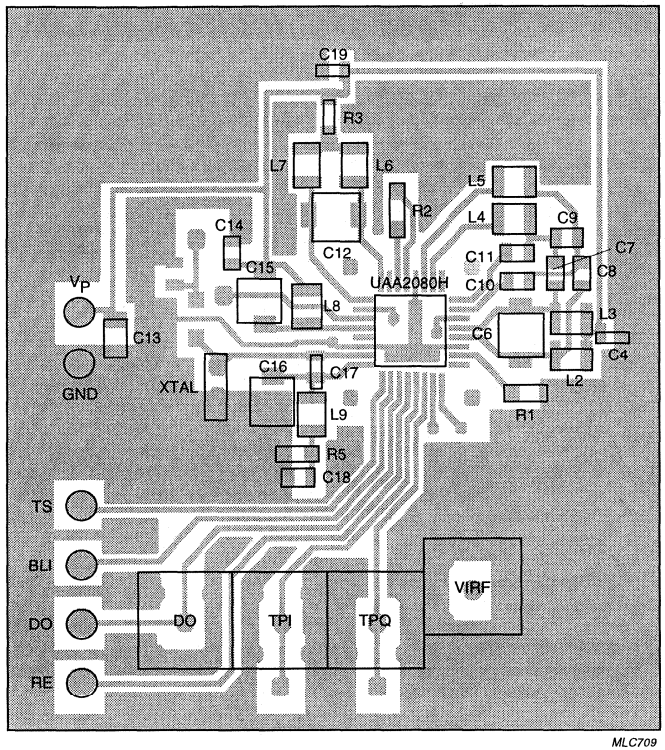


Fig.15 PCB bottom view for LQFP32; test circuit Figs 1 and 3.



V_{EE} = GND; V_C = V_P.

Fig.16 PCB top view with components for LQFP32; test circuit Fig.3.

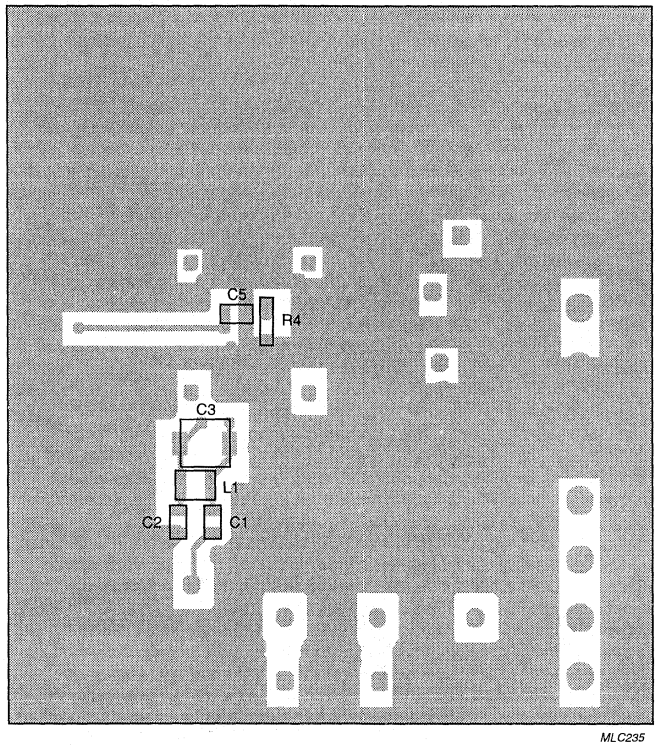


Fig.17 PCB bottom view with components for LQFP32; test circuit Fig.3.

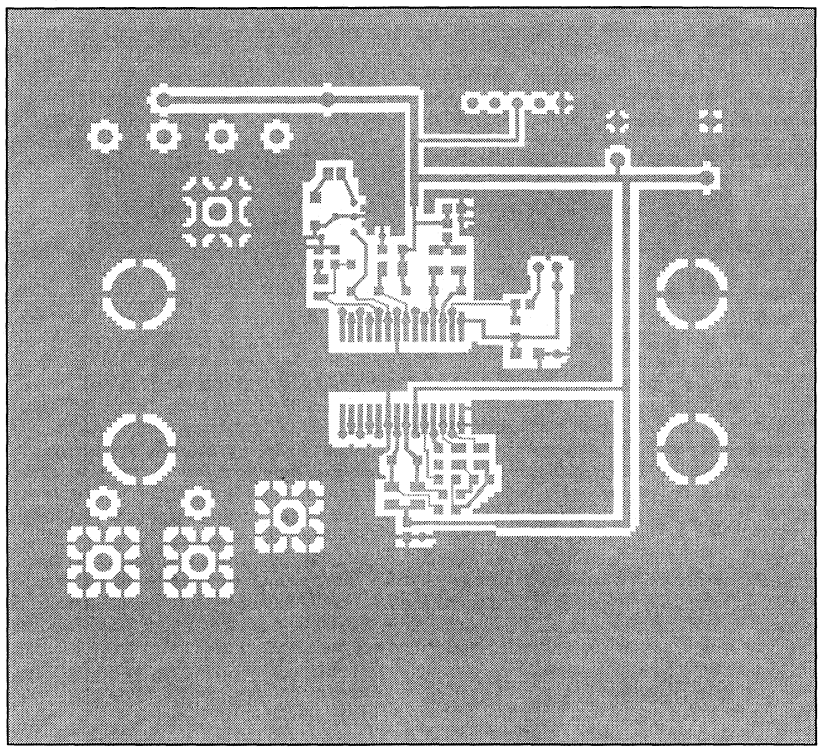


Fig.18 PCB top view for SO28; test circuit Figs 2 and 4.

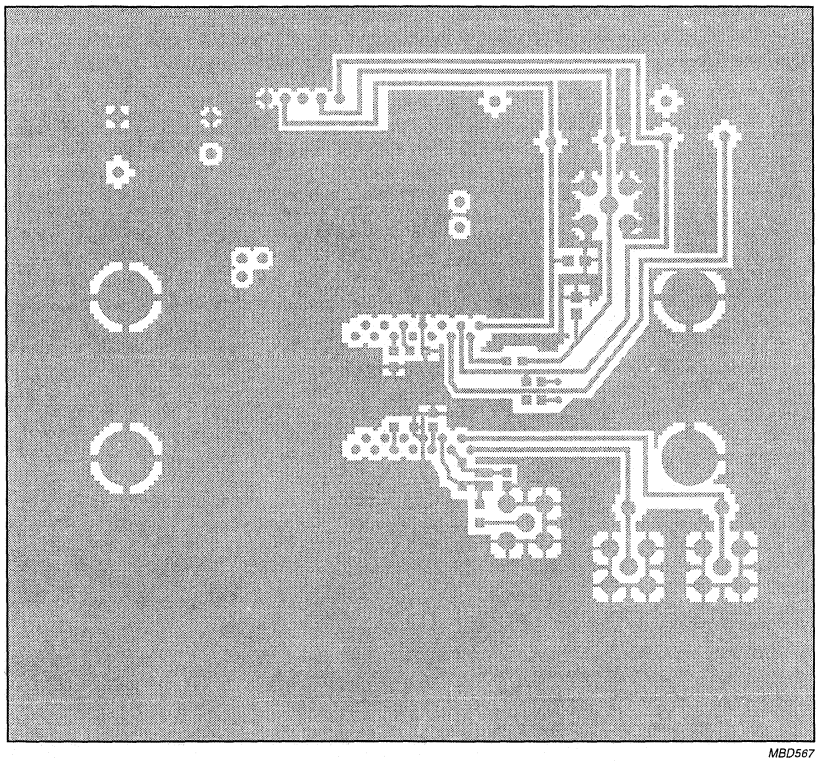
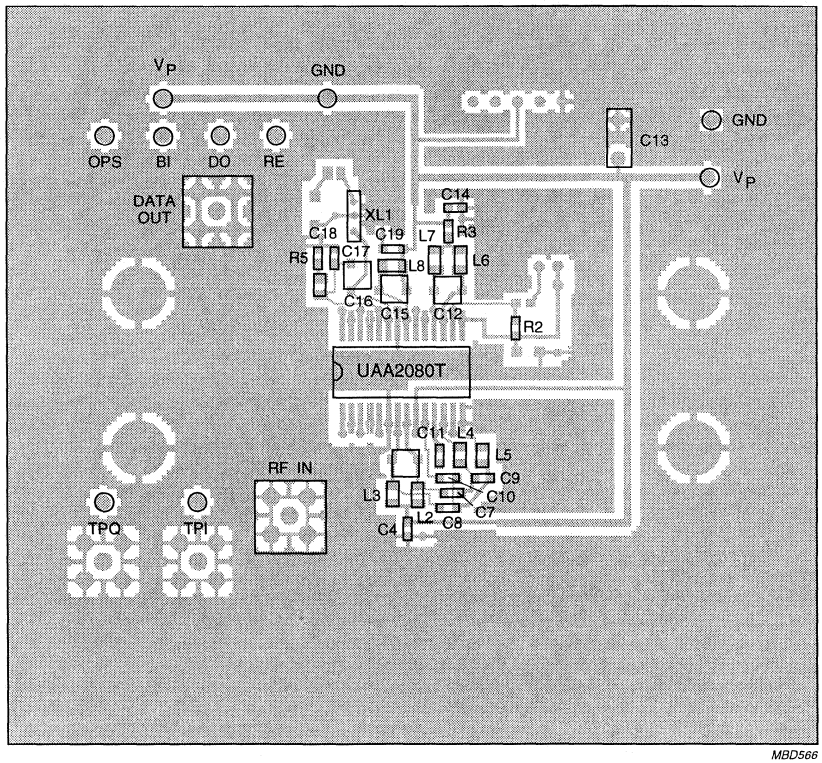


Fig.19 PCB bottom view for SO28; test circuit Figs 2 and 4.



V_{EE} = GND; V_{CC} = V_P; BI = BLI; OPS = TS.

Fig.20 PCB top view with components for SO28; test circuit Fig.4.

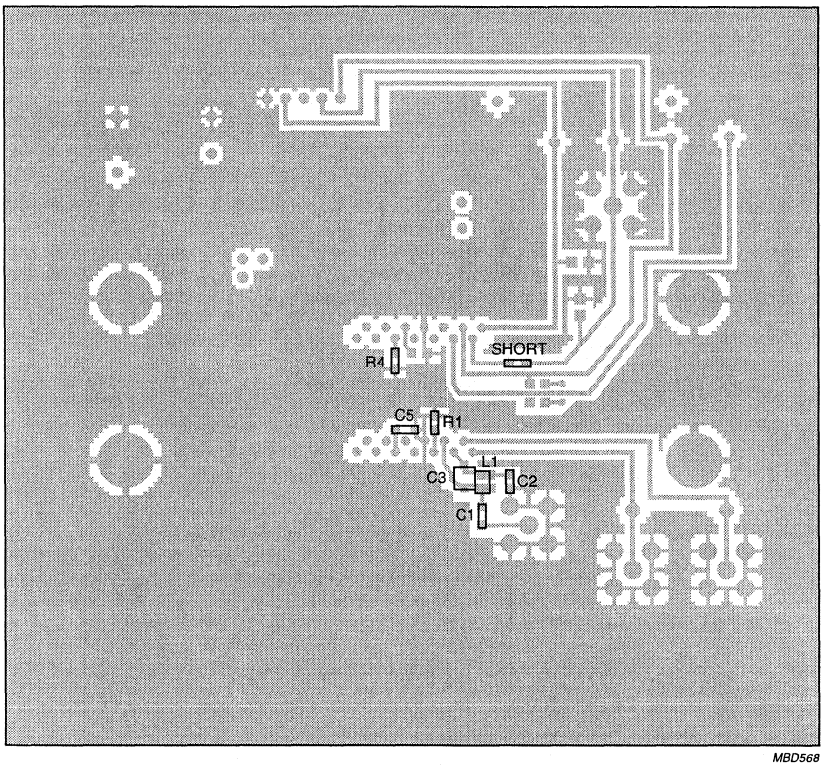


Fig.21 PCB bottom view with components for SO28; test circuit Fig.4.

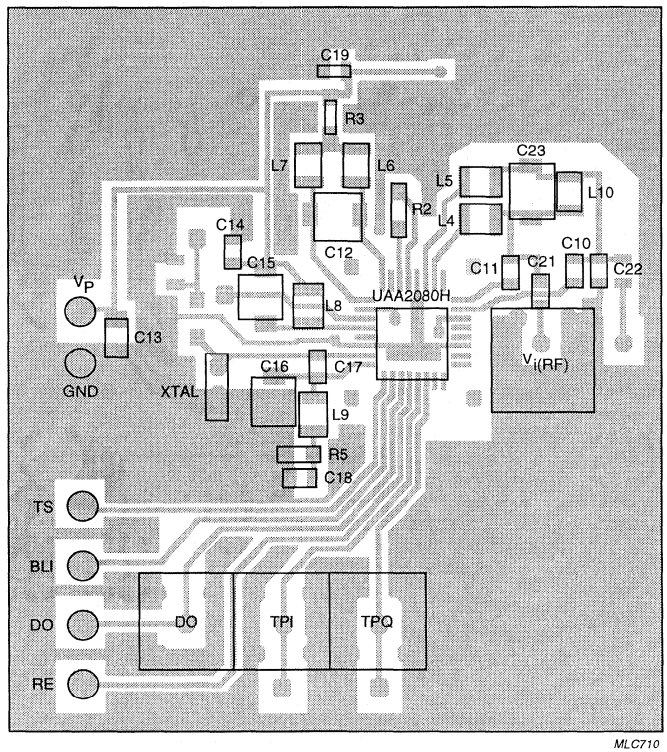


Fig.22 PCB top view with components for LQFP32; test circuit Fig.5.

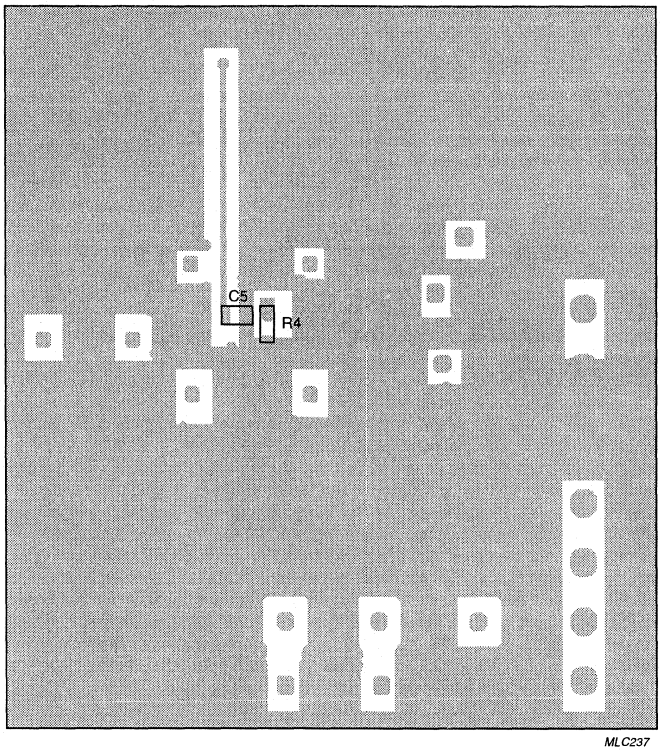


Fig.23 PCB bottom view with components for LQFP32; test circuit Fig.5.

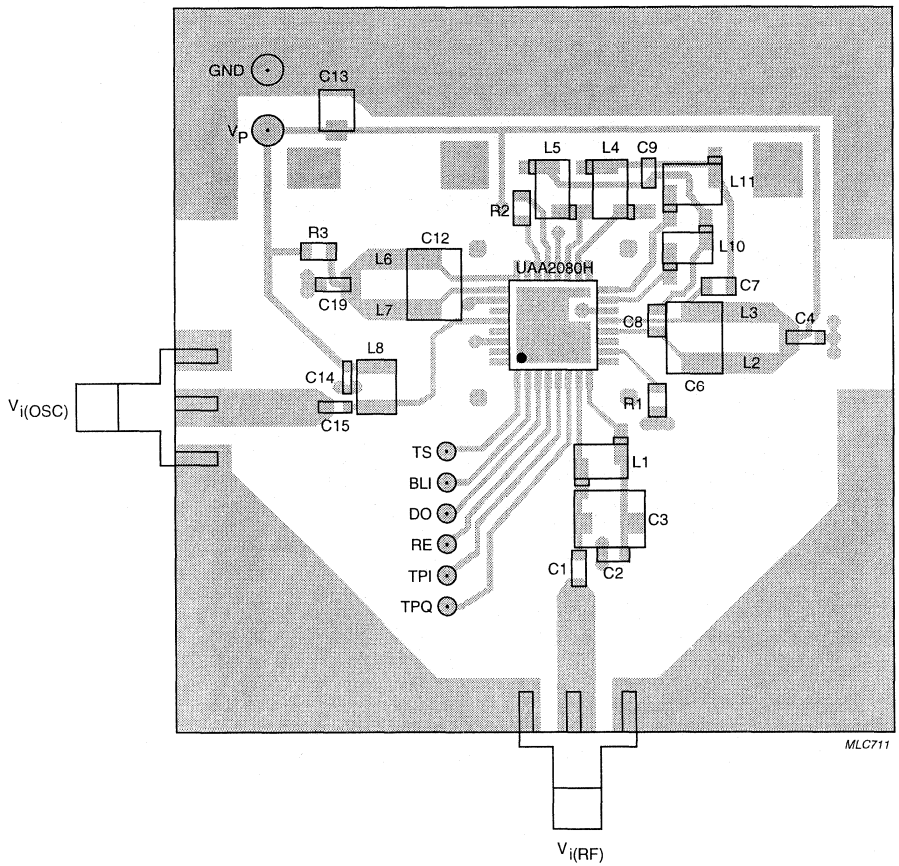


Fig.24 PCB top view with components for LQFP32; test circuit Fig.6.

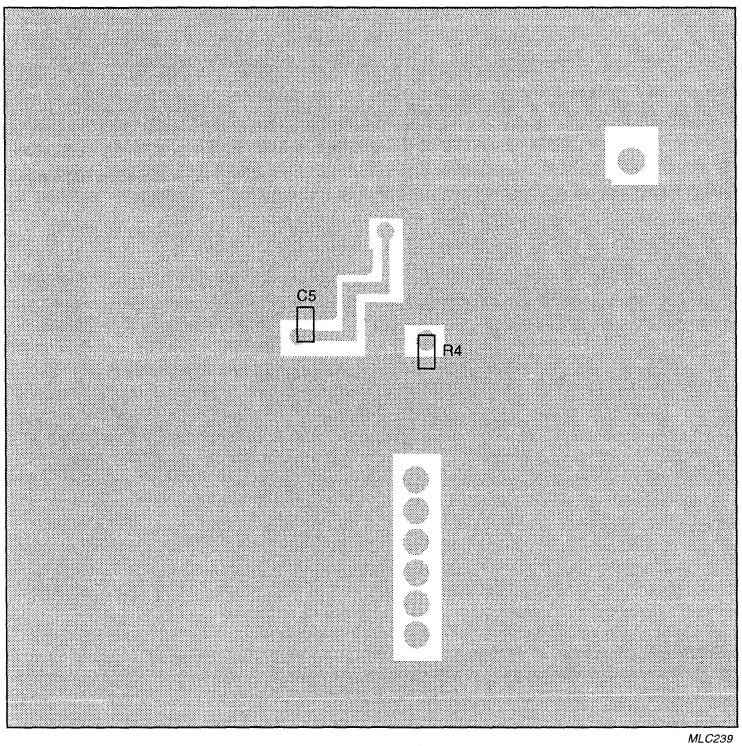


Fig.25 PCB bottom view with components for LQFP32; test circuit Fig.6.

Advanced pager receiver UAA2082

FEATURES

- Wide frequency range: VHF, UHF and 900 MHz bands
- High sensitivity
- High dynamic range
- Electronically adjustable filters on chip
- Suitable for data rates up to 2400 bits/s
- Wide frequency offset and deviation range
- Fully POCSAG compatible FSK receiver
- Power on/off mode selectable by the chip enable input
- Low supply voltage; low power consumption
- 1-cell battery-low detection circuit
- High integration level
- Interfaces directly to the PCA5000A, PCF5001 and PCD5003 POCSAG decoders.

APPLICATIONS

- Wide area paging
- On-site paging
- Telemetry
- RF security systems
- Low bit-rate wireless data links.

GENERAL DESCRIPTION

The UAA2082 is a high-performance low-power radio receiver circuit primarily intended for VHF, UHF and 900 MHz pager receivers for wide area digital paging systems, employing direct FM non-return-to-zero (NRZ) frequency shift keying (FSK).

The receiver design is based on the direct conversion principle where the input signal is mixed directly down to the baseband by a local oscillator on the signal frequency. Two complete signal paths with signals of 90° phase difference are required to demodulate the signal.
All channel selectivity is provided by the built-in IF filters. The circuit makes extensive use of on-chip capacitors to minimize the number of external components.

The battery monitoring circuit has an external sense input and a 1.1 V detection threshold for easy operation in a single-cell supply concept.

The UAA2082 was designed to operate together with the PCA5000A, PCF5001 or PCD5003 POCSAG decoders, which contain a digital input filter for optimum call success rate.

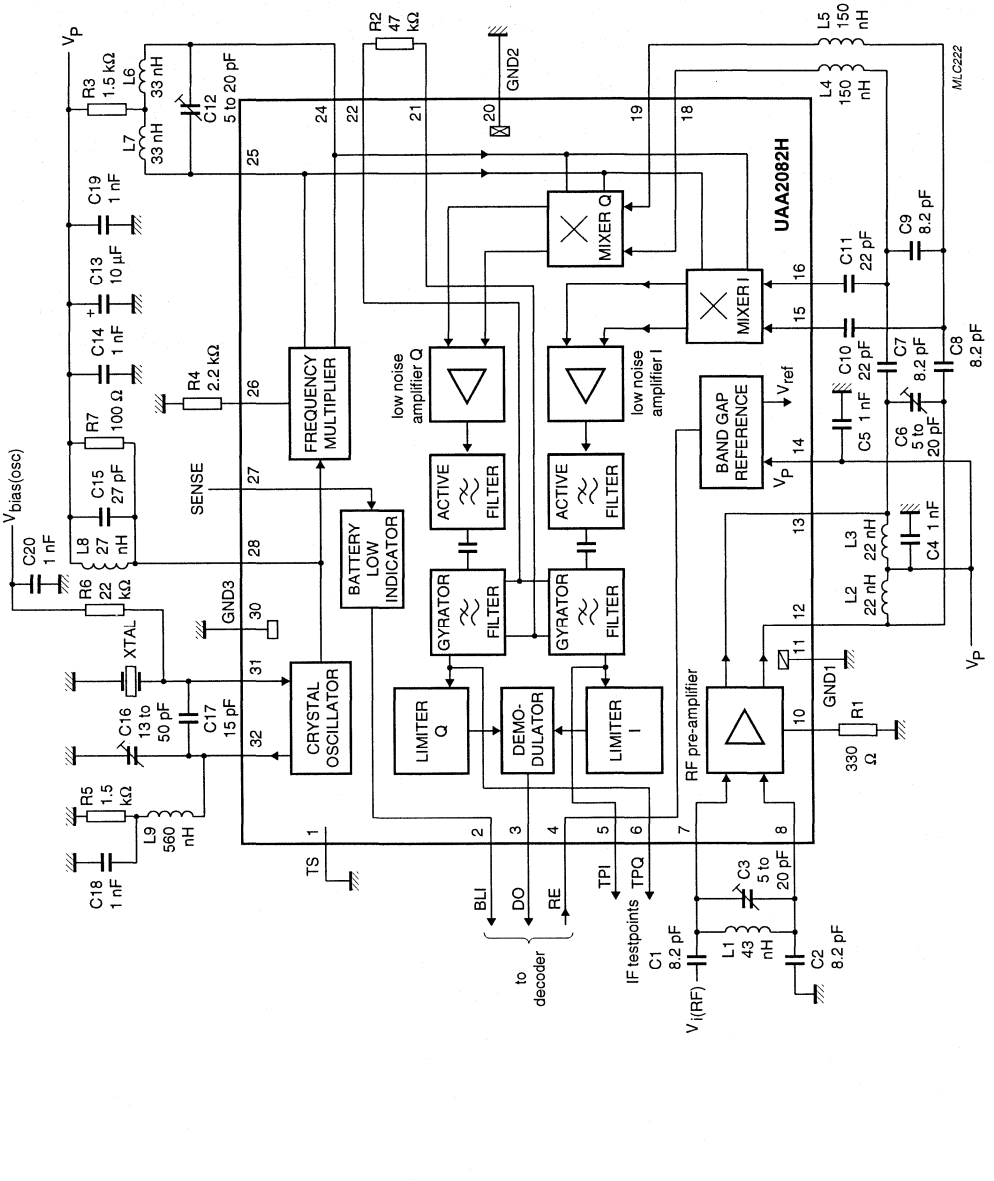
ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UAA2082H	LQFP32	plastic low profile quad flat package; 32 leads; body 7 × 7 × 1.4 mm	SOT358-1
UAA2082U	28 pads	naked die; see Fig.8	

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		1.9	2.05	3.5	V
I_P	supply current		2.3	2.7	3.2	mA
$I_{P(off)}$	stand-by current		–	–	3	µA
$P_{i(ref)}$	RF input sensitivity	BER ≤ $^3/_{100}$; ±4 kHz deviation; data rate 1200 bits/s; T_{amb} = 25 °C				
		$f_{i(RF)}$ = 173 MHz	–	−126.5	−123.5	dBm
		$f_{i(RF)}$ = 470 MHz	–	−124.5	−121.5	dBm
		$f_{i(RF)}$ = 930 MHz	–	−120.0	−114.0	dBm
$P_{i(mix)}$	mixer input sensitivity	BER ≤ $^3/_{100}$; $f_{i(RF)}$ = 470 MHz; ±4 kHz deviation; data rate 1200 bits/s; T_{amb} = 25 °C	–	−115.0	−110.0	dBm
V_{th}	detection threshold for battery LOW indicator	T_{amb} = 25 °C	1.05	1.10	1.15	V
		T_{amb} = −10 to +70 °C	1.03	1.10	1.17	V
T_{amb}	operating ambient temperature		−10	–	+70	°C

BLOCK DIAGRAMS (173 MHz)



Pins 9, 17, 23 and 29 are not connected.

Fig.1 Block, test and application diagram drawn for LQFP32; $f_{i(RF)} = 172.941$ MHz.

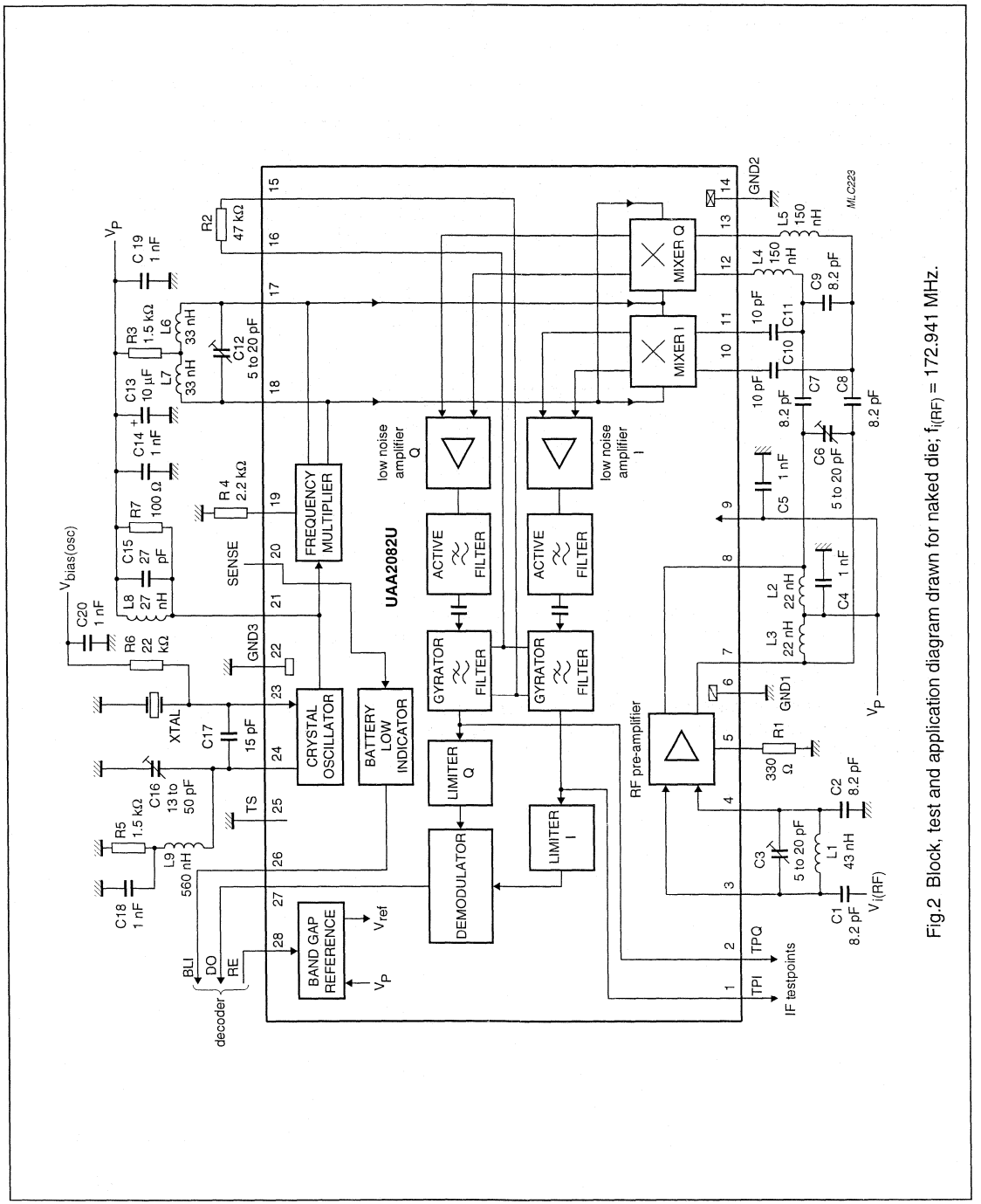


Fig.2 Block, test and application diagram drawn for naked die; $f_{i(RF)}$ = 172.941 MHz.

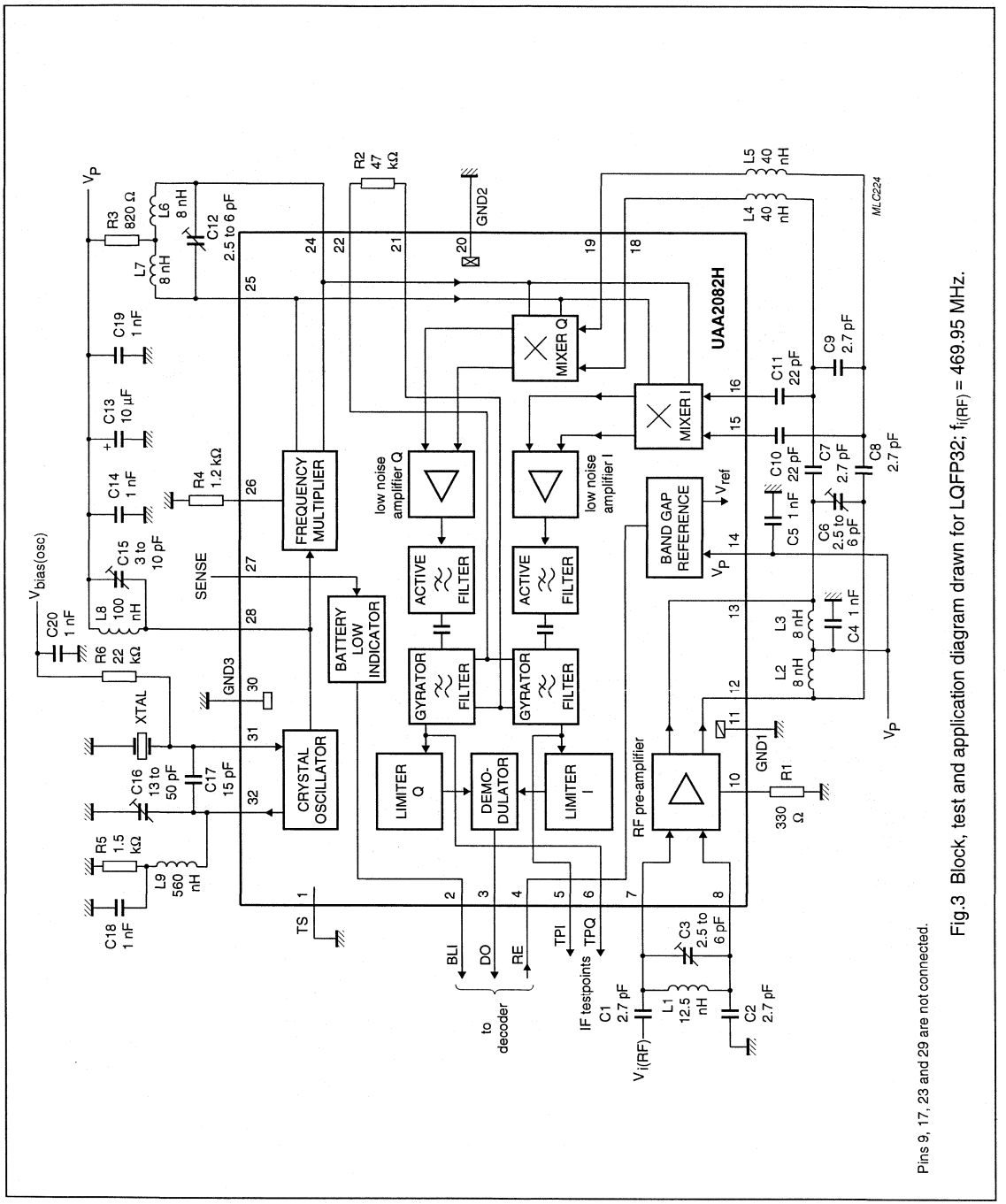
Table 1 Tolerances of components shown in Figs 1 and 2 (notes 1 and 2)

COMPONENT	TOLERANCE (%)	REMARK
Inductances		
L1	±5	Q_{min} = 100 at 173 MHz
L2, L3, L6, L7	±20	Q_{min} = 50 at 173 MHz; TC = (+25 to +125) × 10^{-6}/K
L4, L5	±10	Q_{min} = 30 at 173 MHz; TC = (+25 to +125) × 10^{-6}/K
L8	±20	Q_{min} = 30 at 173 MHz; TC = (+25 to +125) × 10^{-6}/K
L9	±10	Q_{min} = 30 at 57 MHz; TC = (+25 to +125) × 10^{-6}/K
Resistors		
R1 to R7	±2	TC = +50 × 10^{-6}/K
Capacitors		
C1, C2, C7, C8, C9, C15	±5	TC = (0 ±30) × 10^{-6}/K; tan δ ≤ 30 × 10^{-4} at 1 MHz
C3, C6, C12	–	TC = (−750 ±300) × 10^{-6}/K; tan δ ≤ 50 × 10^{-4} at 1 MHz
C4, C5, C14, C18, C19, C20	±10	TC = (0 ±30) × 10^{-6}/K; tan δ ≤ 10 × 10^{-4} at 1 MHz
C10, C11	±5	TC = (0 ±30) × 10^{-6}/K; tan δ ≤ 21 × 10^{-4} at 1 MHz
C13	±20	
C16	–	TC = (−1700 ±500) × 10^{-6}/K; tan δ ≤ 50 × 10^{-4} at 1 MHz
C17	±5	TC = (0 ±30) × 10^{-6}/K; tan δ ≤ 26 × 10^{-4} at 1 MHz

Notes

1. Recommended crystal: f_{XTAL} = 57.647 MHz (crystal with 8 pF load), 3rd overtone, pullability >2.75 × 10^{-6}/pF (change in frequency between series resonance and resonance with 8 pF series capacitor at 25 °C), dynamic resistance R1 < 40 Ω, Δf = ±5 × 10^{-6} for T_{amb} = −10 to +55 °C with 25 °C reference, calibration plus aging tolerance: −5 × 10^{-6} to +15 × 10^{-6}.
2. This crystal recommendation is based on economic aspects and practical experience. Normally the spreads for R1, pullability and calibration do not show their worst case limits simultaneously in one crystal. In such a rare event, the tuning range will be reduced to an insufficient level.

BLOCK AND TEST DIAGRAMS (470 MHz)



Pins 9, 17, 23 and 29 are not connected.

Fig.3 Block, test and application diagram drawn for LQFP32; $f_{i(RF)}$ = 469.95 MHz.

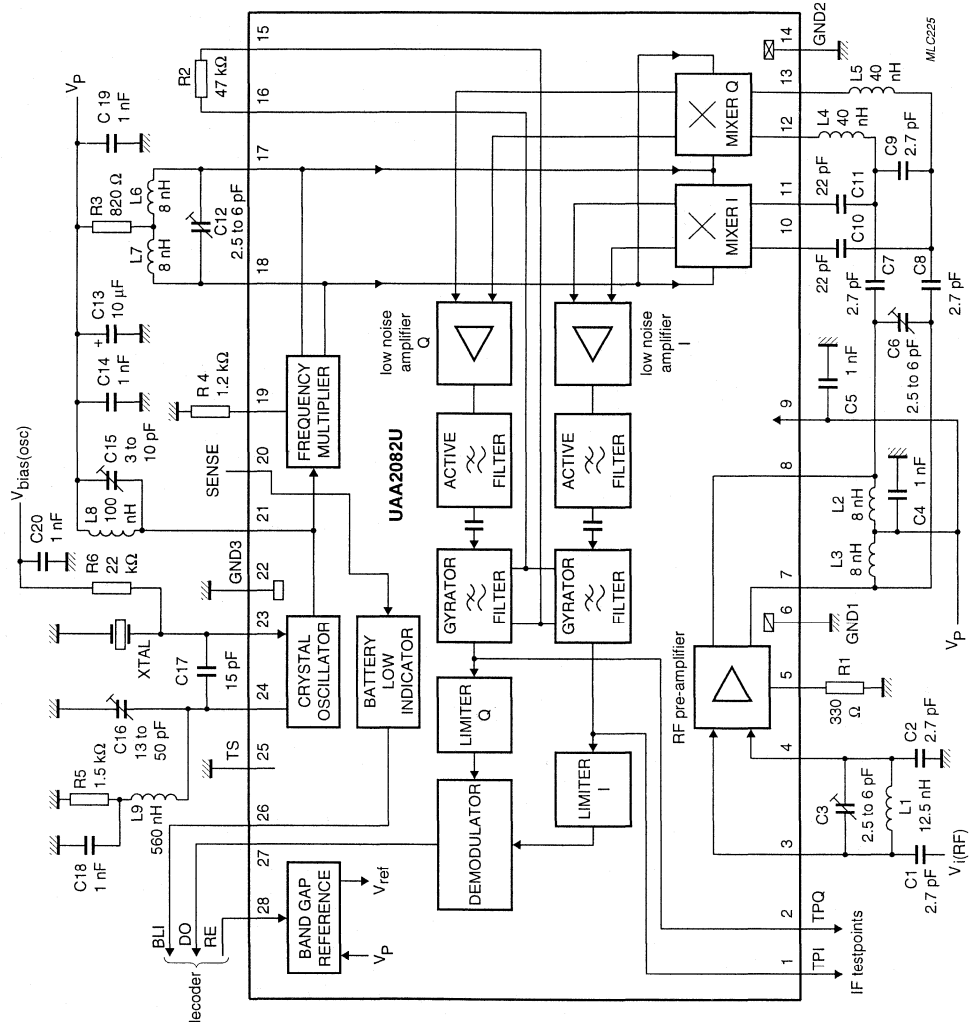


Fig.4 Block, test and application diagram drawn for naked die; $f_{i(RF)}$ = 469.95 MHz.

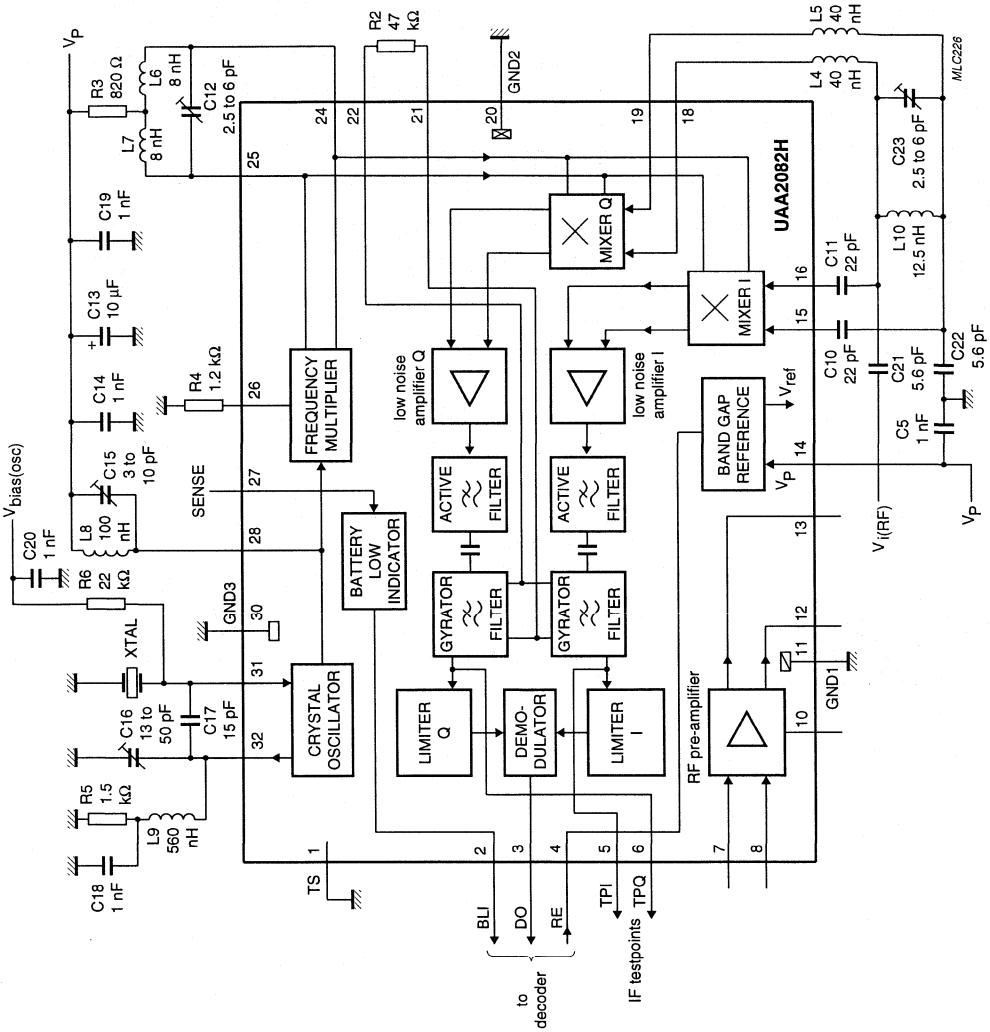


Fig.5 Mixer input sensitivity test circuit; $f_{i(RF)}$ = 469.95 MHz.

Table 2 Tolerances of components shown in Figs 3, 4 and 5 (notes 1 and 2)

COMPONENT	TOLERANCE (%)	REMARK
Inductances		
L1, L10	±5	Q_{min} = 145 at 470 MHz
L2, L3, L6, L7	±20	Q_{min} = 50 at 470 MHz; TC = (+25 to +125) × 10^{-6}/K
L4, L5	±10	Q_{min} = 40 at 470 MHz; TC = (+25 to +125) × 10^{-6}/K
L8	±10	Q_{min} = 30 at 156 MHz; TC = (+25 to +125) × 10^{-6}/K
L9	±10	Q_{min} = 40 at 78 MHz; TC = (+25 to +125) × 10^{-6}/K
Resistors		
R1 to R6	±2	TC = +50 × 10^{-6}/K
Capacitors		
C1, C2, C7, C8, C9	±5	TC = (0 ±30) × 10^{-6}/K; tan δ ≤ 30 × 10^{-4} at 1 MHz
C3, C6, C12, C23	–	TC = (−750 ±300) × 10^{-6}/K; tan δ ≤ 50 × 10^{-4} at 1 MHz
C4, C5, C14, C18 to C22	±10	TC = (0 ±30) × 10^{-6}/K; tan δ ≤ 10 × 10^{-4} at 1 MHz
C10, C11	±5	TC = (0 ±30) × 10^{-6}/K; tan δ ≤ 21 × 10^{-4} at 1 MHz
C13	±20	
C16	–	TC = (−1700 ±500) × 10^{-6}/K; tan δ ≤ 50 × 10^{-4} at 1 MHz
C17	±5	TC = (0 ±30) × 10^{-6}/K; tan δ ≤ 26 × 10^{-4} at 1 MHz

Notes

1. Recommended crystal: f_{XTAL} = 78.325 MHz (crystal with 8 pF load), 3rd overtone, pullability >2.75 × 10^{-6}/pF (change in frequency between series resonance and resonance with 8 pF capacitor at 25 °C), dynamic resistance R1 < 30 Ω, Δf = ±5 × 10^{-6} for T_{amb} = −10 to +55 °C with 25 °C reference, calibration plus aging tolerance: −5 × 10^{-6} to +15 × 10^{-6}.
2. This crystal recommendation is based on economic aspects and practical experience. Normally the spreads for R1, pullability and calibration do not show their worst case limits simultaneously in one crystal. In such a rare event, the tuning range will be reduced to an insufficient level.

BLOCK AND TEST DIAGRAM (930 MHz)

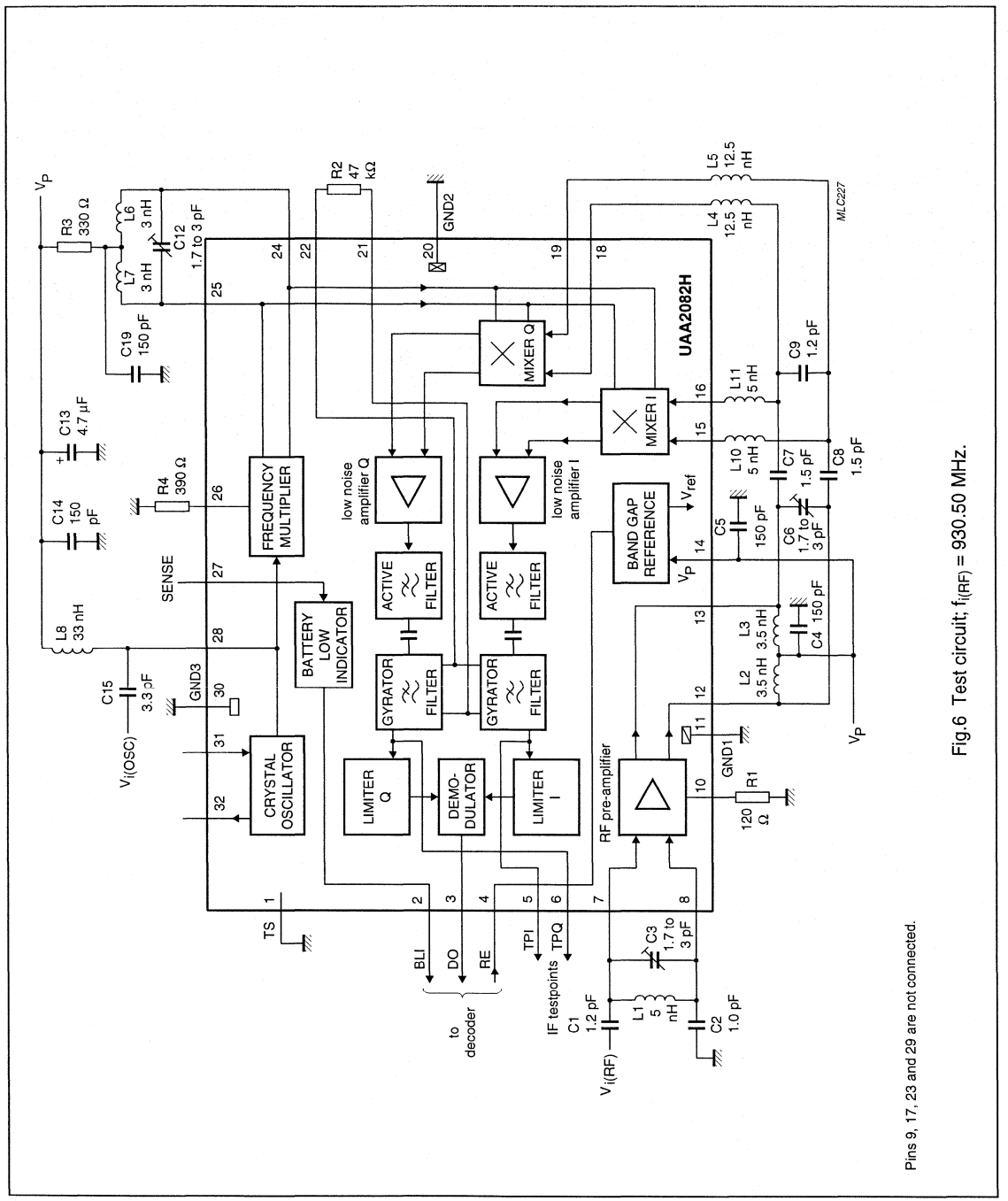


Fig.6 Test circuit; $f_{i(RF)}$ = 930.50 MHz.

Pins 9, 17, 23 and 29 are not connected.

Table 3 Tolerances of components shown in Fig.6 (note 1)

COMPONENT	TOLERANCE (%)	REMARK
Inductances		
L1	±10	Q_{typ} = 150 at 930 MHz
L2, L3, L6, L7	–	microstrip inductor
L4, L5	±5	Q_{typ} = 100 at 930 MHz
L8	±10	Q_{typ} = 65 at 310 MHz
L10, L11	±10	Q_{typ} = 150 at 930 MHz
Resistors		
R1 to R4	±2	TC = (0 ±200) × 10^{-6}/K
Capacitors		
C1, C2, C7, C8, C9, C15	±5	TC = (0 ±30) × 10^{-6}/K; tan $\delta \leq 30 \times 10^{-4}$ at 1 MHz
C3, C6, C12	–	TC = (0 ±200) × 10^{-6}/K; tan $\delta \leq 30 \times 10^{-4}$ at 1 MHz
C4, C5, C14, C19	±10	TC = (0 ±30) × 10^{-6}/K; tan $\delta \leq 10 \times 10^{-4}$ at 1 MHz
C13	±20	

Note

1. The external oscillator signal $V_{i(OSC)}$ has a frequency of f_{OSC} = 310.1667 MHz.

PINNING (LQFP32)

SYMBOL	PIN	DESCRIPTION
TS	1	test switch; connection to ground for normal operation
BLI	2	battery LOW indicator output
DO	3	data output
RE	4	receiver enable input
TPI	5	IF test point; I channel
TPQ	6	IF test point; Q channel
VI1RF	7	pre-amplifier RF input 1
VI2RF	8	pre-amplifier RF input 2
n.c.	9	not connected
RRFA	10	external emitter resistor for pre-amplifier
GND1	11	ground 1 (0 V)
VO2RF	12	pre-amplifier RF output 2
VO1RF	13	pre-amplifier RF output 1
V_P	14	supply voltage
VI2MI	15	I channel mixer input 2
VI1MI	16	I channel mixer input 1
n.c.	17	not connected
VI1MQ	18	Q channel mixer input 1
VI2MQ	19	Q channel mixer input 2
GND2	20	ground 2 (0 V)
COM	21	gyrator filter resistor; common line
RGYR	22	gyrator filter resistor
n.c.	23	not connected
VO1MUL	24	frequency multiplier output 1
VO2MUL	25	frequency multiplier output 2
RMUL	26	external emitter resistor for frequency multiplier
SENSE	27	battery LOW detector sense input
OSC	28	oscillator collector
n.c.	29	not connected
GND3	30	ground 3 (0 V)
OSB	31	oscillator base; crystal input
OSE	32	oscillator emitter

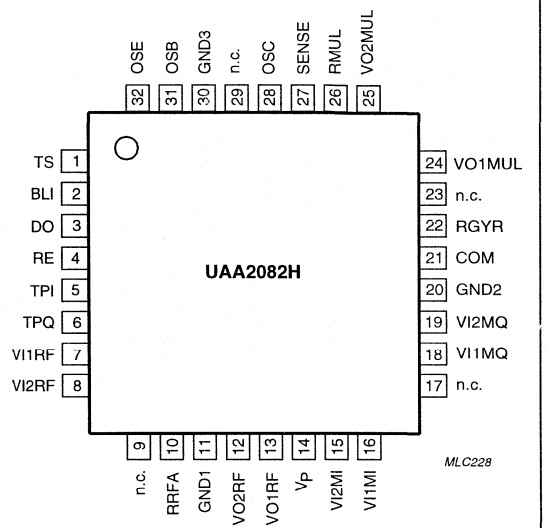
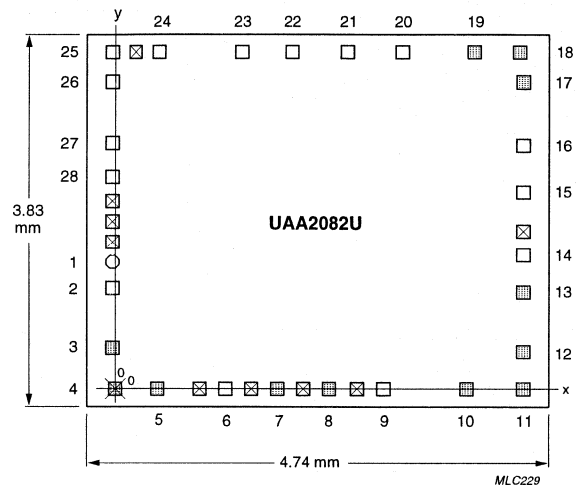


Fig.7 Pin configuration; LQFP32.

CHIP DIMENSIONS AND BONDING PAD LOCATIONS

See Table 4 for bonding pad description and locations for x/y co-ordinates.



Where:

- ○ Pad number 1 (diameter 124 µm)
- □ Pad 124 µm x 124 µm
- ☒ Pad not used
- ▨ Pad 100 µm x 100 µm
- ⊠ Pad 100 µm x 100 µm with reference point

Chip area: 18.15 mm^2
Chip thickness: 380 ±20 µm.
Drawing not to scale.

Fig.8 Bonding pad locations.

Table 4 Bonding pad centre locations (dimensions in μm)

SYMBOL	PAD	DESCRIPTION	x	y
TPI	1	IF test point; I channel	−32	1296
TPQ	2	IF test point; Q channel	−32	1000
VI1RF	3	pre-amplifier RF input 1	−32	360
VI2RF	4	pre-amplifier RF input 2; note 1	0	0
RRFA	5	external emitter resistor for pre-amplifier	472	0
GND1	6	ground 1 (0 V)	1160	0
VO2RF	7	pre-amplifier RF output 2	1688	0
VO1RF	8	pre-amplifier RF output 1	2232	0
V_P	9	supply voltage	2760	0
VI2MI	10	I channel mixer input 2	3608	0
VI1MI	11	I channel mixer input 1	4216	0
VI1MQ	12	Q channel mixer input 1	4216	360
VI2MQ	13	Q channel mixer input 2	4216	960
GND2	14	ground 2 (0 V)	4216	1360
COM	15	gyrator filter resistor; common line	4216	2024
RGYR	16	gyrator filter resistor	4216	2496
VO1MUL	17	frequency multiplier output 1	4216	3136
VO2MUL	18	frequency multiplier output 2	4176	3456
RMUL	19	external emitter resistor for frequency multiplier	3668	3458
SENSE	20	battery LOW detector sense input	2952	3456
OSC	21	oscillator collector	2312	3456
GND3	22	ground 3 (0 V)	1832	3456
OSB	23	oscillator base; crystal input	1328	3456
OSE	24	oscillator emitter	432	3456
TS	25	test switch; connection to ground for normal operation	−32	3456
BLI	26	battery LOW indicator output	−32	3136
DO	27	data output	−32	2512
RE	28	receiver enable input	−32	2152
		lower left corner of chip (typical values)	−278	−186

Note

1. All x/y co-ordinates are referenced to the centre of pad 4 (VI2RF); see Fig.8.

INTERNAL CIRCUITS

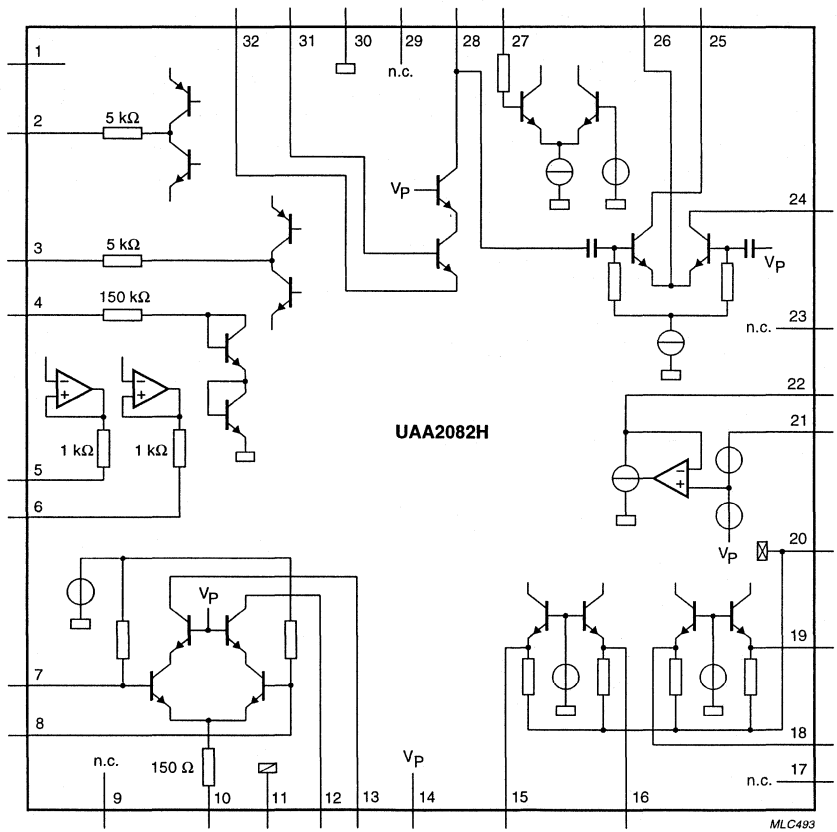


Fig.9 Internal circuits drawn for LQFP32.

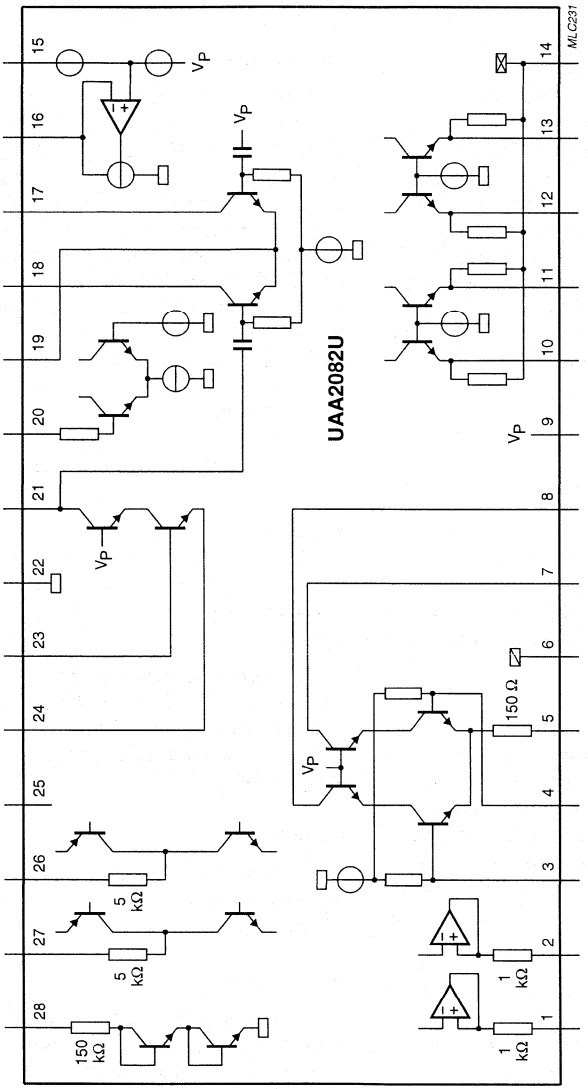


Fig.10 Internal circuits drawn for naked die.

FUNCTIONAL DESCRIPTION

The complete circuit consists of the following functional blocks as shown in Figs 1 to 6.

Radio frequency amplifier

The RF amplifier is an emitter-coupled pair driving a balanced cascode stage, which drives an external balanced tuned circuit. Its bias current is set by an external 300 Ω resistor R1 to typically 770 μA. With this bias current the optimum source resistance is 1.3 kΩ at VHF and 1.0 kΩ at UHF. At 930 MHz a higher bias current is required to achieve optimum gain. A value of 120 Ω is used for R1, which corresponds with a bias current of approximately 1.3 mA and an optimum source resistance of approximately 600 Ω.The capacitors C1 and C2 transform a 50 Ω source resistance to this optimum value. The output drives a tuned circuit with capacitive divider (C7, C8 and C9) to provide maximum power transfer to the phase-splitting network and the mixers.

Mixers

The double balanced mixers consist of common base input stages and upper switching stages driven from the frequency multiplier. The 300 Ω input impedance of each mixer acts together with external components (C10, C11; L4, L5 respectively) as phase shifter/power splitter to provide a differential phase shift of 90 degrees between the I channel and the Q channel. At 930 MHz all external phase shifter components are inductive (L10, L11; L4, L5).

Oscillator

The oscillator is based on a transistor in common collector configuration. It is followed by a cascode stage driving a tuned circuit which provides the signal for the frequency multiplier. The oscillator transistor requires an external bias voltage $V_{bias(osc)}$ (1.22 V typ.). The oscillator bias current (typically 250 μA) is determined by the 1.5 kΩ external resistor R5. The oscillator frequency is controlled by an external 3rd overtone crystal in parallel resonance mode. External capacitors between base and emitter (C17) and from emitter to ground (C16) make the oscillator transistor appear as having a negative resistance for small signals; this causes the oscillator to start. Inductance L9 connected in parallel with capacitor C16 to the emitter of the oscillator transistor prevents oscillation at the fundamental frequency of the crystal.

The resonant circuit at output pin OSC selects the second harmonic of the oscillator frequency. In other applications a different multiplication factor may be chosen.

At 930 MHz an external oscillator circuit is required to provide sufficient local oscillator signal for the frequency multiplier.

Frequency multiplier

The frequency multiplier is an emitter-coupled pair driving an external balanced tuned circuit. Its bias current is set by external resistor R4 to typically 190 μA (173 MHz), 350 μA (470 MHz) and 1 mA (930 MHz). The oscillator signal is internally AC coupled to one input of the emitter-coupled pair while the other input is internally grounded via a capacitor. The frequency multiplier output signal between pins VO1MUL and VO2MUL drives the upper switching stages of the mixers. The bias voltage on pins VO1MUL and VO2MUL is set by external resistor R3 to allow sufficient voltage swing at the mixer outputs. The value of R3 depends on the operating frequency: 1.5 kΩ (173 MHz), 820 Ω (470 MHz) and 330 Ω (930 MHz).

Low noise amplifiers, active filters and gyrator filters

The low noise amplifiers ensure that the noise of the following stages does not affect the overall noise figure. The following active filters before the gyrator filters reduce the levels of large signals from adjacent channels. Internal AC couplings block DC offsets from the gyrator filter inputs.

The gyrator filters implement the transfer function of a 7th order elliptic filter. Their cut-off frequencies are determined by the 47 kΩ external resistor R2 between pins RGYR and COM. The gyrator filter output signals are available on IF test pins TPI and TPQ.

Limiters

The gyrator filter output signals are amplified in the limiter amplifiers to obtain IF signals with removed amplitude information.

Demodulator

The limiter amplifier output signals are fed to the demodulator. The demodulator output DO is going LOW or HIGH depending upon which of the input signals has a phase lead.

Battery LOW indicator

The battery LOW indicator senses the supply voltage and sets its output HIGH when the voltage at input SENSE is less than V_{th} (typically 1.10 V). Low battery warning is available at BLI.

Band gap reference

The whole chip except the oscillator section can be powered-up and powered-down by enabling and disabling the band gap reference via the receiver enable pin RE.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).
Ground pins GND1, GND2 and GND3 connected together.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage	−0.3	+8.0	V
T_{stg}	storage temperature	−55	+125	°C
T_{amb}	operating ambient temperature	−10	+70	°C
V_{es}	electrostatic handling; note 1			
	pins VI1RF and VI2RF	−1500	+2000	V
	pin RRFA	−500	+2000	V
	pins VO1RF and VO2RF	−2000	+250	V
	pins V_P and OSB	−500	+500	V
	pins OSC and OSE	−2000	+500	V
	other pins	−2000	+2000	V

Note

1. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ resistor.

DC CHARACTERISTICS

V_P = 2.05 V; T_{amb} = −10 to +70 °C (typical values at T_{amb} = 25 °C); measurements taken in test circuit Figs 1, 2, 3 or 4 with crystal at pin OSB disconnected; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage		1.9	2.05	3.5	V
I_P	supply current	V_{RE} = HIGH; $f_{i(RF)}$ = 173 and 470 MHz	2.3	2.7	3.2	mA
		V_{RE} = HIGH; $f_{i(RF)}$ = 930 MHz	2.9	3.4	3.9	mA
$I_{P(off)}$	stand-by current	V_{RE} = LOW	–	–	3	µA
$V_{bias(osc)}$	oscillator bias voltage		1.20	1.22	1.24	V
Receiver enable input (pin RE)						
V_{IH}	HIGH level input voltage		1.4	–	V_P	V
V_{IL}	LOW level input voltage		0	–	0.3	V
I_{IH}	HIGH level input current	$V_{IH} = V_P$ = 3.5 V	–	–	20	µA
V_{IL}	LOW level input current	V_{IL} = 0 V	0	–	−1.0	µA
Battery LOW indicator output (pin BLI)						
V_{OH}	HIGH level output voltage	$V_{SENSE} < V_{th}$; I_{BLI} = −10 µA	V_P − 0.5	–	–	V
V_{OL}	LOW level output voltage	$V_{SENSE} > V_{th}$; I_{BLI} = +10 µA	–	–	0.5	V
V_{th}	voltage threshold for battery LOW indicator	V_P = 2.05 V; T_{amb} = 25 °C	1.05	1.10	1.15	V
		V_P = 2.05 to 3.5 V; T_{amb} = −10 to +70 °C	1.03	1.10	1.17	V
Demodulator output (pin DO)						
V_{OH}	HIGH level output voltage	I_{DO} = −10 µA	V_P − 0.5	–	–	V
V_{OL}	LOW level output voltage	I_{DO} = +10 µA	–	–	0.5	V

AC CHARACTERISTICS (173 MHz)

V_P = 2.05 V; T_{amb} = 25 °C; test circuit Figs 1 or 2; $f_{i(RF)}$ = 172.941 MHz with ±4.0 kHz deviation; 1200 baud pseudo random bit sequence modulation (t_r = 250 ±25 µs measured between 10% and 90% of voltage amplitude) and 20 kHz channel spacing; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Radio frequency input						
$P_{i(ref)}$	input sensitivity ($P_{i(ref)}$ is the maximum available power at the RF input of the test board)	BER ≤ $^3/_{100}$; note 1	–	–126.5	–123.5	dBm
		T_{amb} = –10 to +70 °C; note 2	–	–	–120.5	dBm
		V_P = 1.9 V	–	–	–117.5	dBm
Mixers to demodulator						
α_{acs}	adjacent channel selectivity	T_{amb} = 25 °C	69	72	–	dB
		T_{amb} = –10 to +70 °C	67	–	–	dB
α_{ci}	IF filter channel imbalance		–	–	2	dB
α_c	co-channel rejection		–	4	7	dB
α_{sp}	spurious immunity		50	60	–	dB
α_{im}	intermodulation immunity		55	60	–	dB
α_{bl}	blocking immunity	Δf > ±1 MHz; note 3	78	85	–	dB
f_{offset}	frequency offset range (3 dB degradation in sensitivity)	deviation f = ±4.0 kHz	±2.0	–	–	kHz
		deviation f = ±4.5 kHz	±2.5	–	–	kHz
Δf_{dev}	deviation range (3 dB degradation in sensitivity)		2.5	–	7.0	kHz
t_{on}	receiver turn-on time	data valid after setting RE input HIGH; note 4	–	–	5	ms

Notes

1. The bit error rate BER is measured using the test facility shown in Fig.12. Note that the BER test facility contains a digital input filter equivalent to the one used in the PCA5000A, PCF5001 and PCD5003 POCSAG decoders.
2. Capacitor C16 requires re-adjustment to compensate temperature drift.
3. Δf is the frequency offset between the required signal and the interfering signal.
4. Turn-on time is defined as the time from pin RE going HIGH to the reception of valid data on output pin DO. Turn-on time is measured using an external oscillator (turn-on time using the internal oscillator is dependent upon the oscillator circuitry).

AC CHARACTERISTICS (470 MHz)

V_P = 2.05 V; T_{amb} = 25 °C; test circuit Figs 3 or 4; $f_{i(RF)}$ = 469.950 MHz with ±4.0 kHz deviation; 1200 baud pseudo random bit sequence modulation (t_r = 250 ± 25 µs measured between 10% and 90% of voltage amplitude) and 20 kHz channel spacing; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Radio frequency input						
$P_{i(ref)}$	input sensitivity ($P_{i(ref)}$ is the maximum available power at the RF input of the test board)	BER ≤ $^3/_{100}$; note 1	–	–124.5	–121.5	dBm
		T_{amb} = –10 to +70 °C; note 2	–	–	–118.5	dBm
		V_P = 1.9 V	–	–	–115.5	dBm
Mixer input						
$P_{i(mix)}$	input sensitivity	BER ≤ $^3/_{100}$; note 3	–	–115.0	–110.0	dBm
Mixers to demodulator						
α_{acs}	adjacent channel selectivity	T_{amb} = 25 °C	67	70	–	dB
		T_{amb} = –10 to +70 °C	65	–	–	dB
α_{ci}	IF filter channel imbalance		–	–	2	dB
α_c	co-channel rejection		–	4	7	dB
α_{sp}	spurious immunity		50	60	–	dB
α_{im}	intermodulation immunity		55	60	–	dB
α_{bl}	blocking immunity	Δf > ±1 MHz; note 4	75	82	–	dB
f_{offset}	frequency offset range (3 dB degradation in sensitivity)	deviation f = ±4.0 kHz	±2.0	–	–	kHz
		deviation f = ±4.5 kHz	±2.5	–	–	kHz
Δf_{dev}	deviation range (3 dB degradation in sensitivity)		2.5	–	7.0	kHz
t_{on}	receiver turn-on time	data valid after setting RE input HIGH; note 5	–	–	5	ms

Notes

1. The bit error rate BER is measured using the test facility shown in Fig.12. Note that the BER test facility contains a digital input filter equivalent to the one used in the PCA5000A, PCF5001 and PCD5003 POCSAG decoders.
2. Capacitor C16 requires re-adjustment to compensate temperature drift.
3. Test circuit Fig.5. $P_{i(mix)}$ is the maximum available power at the input of the test board. The bit error rate BER is measured using the test facility shown in Fig.12.
4. Δf is the frequency offset between the required signal and the interfering signal.
5. Turn-on time is defined as the time from pin RE going HIGH to the reception of valid data on output pin DO. Turn-on time is measured using an external oscillator (turn-on time using the internal oscillator is dependent upon the oscillator circuitry).

AC CHARACTERISTICS (930 MHz)

V_P = 2.05 V; T_{amb} = 25 °C; test circuit Fig.6; note 1; $f_{i(RF)}$ = 930.500 MHz with ±4.0 kHz deviation; 1200 baud pseudo random bit sequence modulation (t_r = 250 ± 25 µs measured between 10% and 90% of voltage amplitude) and 20 kHz channel spacing; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Radio frequency input						
$P_{i(ref)}$	input sensitivity ($P_{i(ref)}$ is the maximum available power at the RF input of the test board)	BER ≤ $^3/_{100}$; note 2	–	–120.0	–114.0	dBm
		V_P = 1.9 V	–	–	–108.0	dBm
Mixers to demodulator						
α_{acs}	adjacent channel selectivity	T_{amb} = 25 °C	60	69	–	dB
α_c	co-channel rejection		–	5	10	dB
α_{sp}	spurious immunity		40	60	–	dB
α_{im}	intermodulation immunity		53	60	–	dB
α_{bl}	blocking immunity	Δf > ±1 MHz; note 3	65	74	–	dB
f_{offset}	frequency offset range (3 dB degradation in sensitivity)	deviation f = ±4.0 kHz	±2.0	–	–	kHz
		deviation f = ±4.5 kHz	±2.5	–	–	kHz
Δf_{dev}	deviation range (3 dB degradation in sensitivity)		2.5	–	7.0	kHz
t_{on}	receiver turn-on time	data valid after setting RE input HIGH; note 4	–	–	5	ms

Notes

1. The external oscillator signal $V_{i(OSC)}$ has a frequency of f_{OSC} = 310.1667 MHz and a level of –15 dBm.
2. The bit error rate BER is measured using the test facility shown in Fig.12. Note that the BER test facility contains a digital input filter equivalent to the one used in the PCA5000A, PCF5001 and PCD5003 POCSAG decoders.
3. Δf is the frequency offset between the required signal and the interfering signal.
4. Turn-on time is defined as the time from pin RE going HIGH to the reception of valid data on output pin DO. Turn-on time is measured using an external oscillator (turn-on time using the internal oscillator is dependent upon the oscillator circuitry).

TEST INFORMATION

Tuning procedure for AC tests

1. Turn on the signal generator: $f_{gen} = f_{i(RF)} + 4$ kHz, no modulation, $V_{i(RF)} = 1$ mV (RMS).
2. Measure the IF with a counter connected to test pin TPI. Tune C16 to set the crystal oscillator to achieve $f_{IF} = 4$ kHz Change the generator frequency to $f_{gen} = f_{i(RF)} - 4$ kHz and check that f_{IF} is also 4 kHz. For a received input frequency $f_{i(RF)} = 172.941$ MHz the crystal frequency is $f_{XTAL} = 57.647$ MHz, while for $f_{i(RF)} = 469.950$ MHz the crystal frequency is $f_{XTAL} = 78.325$ MHz. For a received input frequency $f_{i(RF)} = 930.500$ MHz an external oscillator signal must be used with $f_{i(OSC)} = 310.1667$ MHz and a level of –15 dBm (for definition of crystal frequency, see Table 1).
3. Set the signal generator to nominal frequency ($f_{i(RF)}$) and turn on the modulation deviation ±4.0 kHz, 600 Hz square wave modulation, $V_{i(RF)} = 1$ mV (RMS). Note that the RF signal should be reduced in the following tests, as the receiver is tuned, to ensure $V_{o(IF)} = 10$ to 50 mV (p-p) on test pins TPI or TPQ.
4. Tune C15 (oscillator output circuit) and C12 (frequency multiplier output) to obtain a peak audio voltage on pin TPI.
5. Tune C3 and C6 (RF input and mixer input) to obtain a peak audio voltage on pin TPI. When testing the mixer input sensitivity tune C23 instead of C3 and C6 (test circuit Fig.5).
6. Check that the output signal on pin TPQ is within 3 dB in amplitude and at 90° (±20°) relative phase of the signal on pin TPI.
7. Check that data signal appears on output pin DO and proceed with the AC test.

AC test conditions

Table 5 Definitions for AC test conditions (see Table 6)

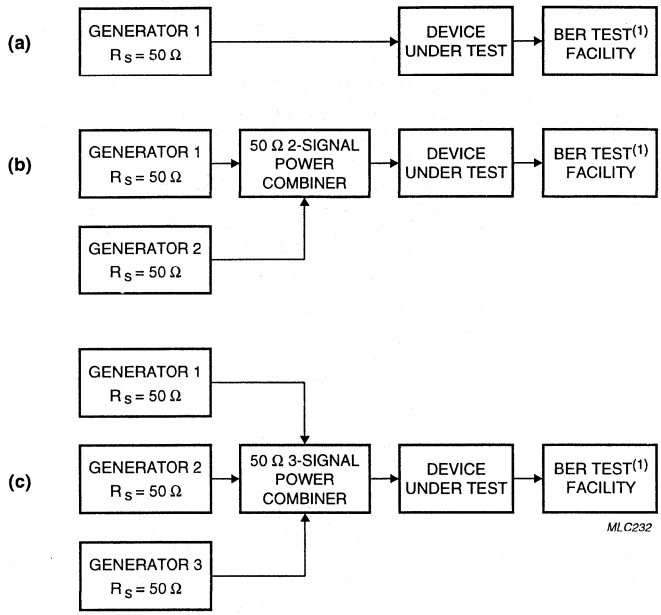
SIGNAL	DESCRIPTION
Modulated test signal 1	
Frequency	172.941, 469.950 or 930.500 MHz
Deviation	±4.0 kHz
Modulation	1200 baud pseudo random bit sequence
Rise time	250 ±25 µs (between 10% and 90% of final value)
Modulated test signal 2	
Deviation	±2.4 kHz
Modulation	400 Hz sine wave
Other definitions	
f_1	frequency of signal generator 1
f_2	frequency of signal generator 2
f_3	frequency of signal generator 3
Δf_{cs}	channel spacing (20 kHz)
P_1	maximum available power from signal generator 1 at the test board input
P_2	maximum available power from signal generator 2 at the test board input
P_3	maximum available power from signal generator 3 at the test board input
$P_{i(ref)}$	maximum available power at the test board input to give a Bit Error Rate (BER) $\leq 3/100$ for the modulated test signal 1, in the absence of interfering signals and under the conditions as specified in Chapters "AC characteristics (173 MHz)", "AC characteristics (470 MHz)" and "AC characteristics (930 MHz)"

Table 6 AC test conditions; notes 1 and 2

SYMBOL	PARAMETER	CONDITIONS	TEST SIGNALS
α_a	adjacent channel selectivity; Fig.11(b)	$f_2 = f_1 \pm \Delta f_{CS}$	
		generator 1: modulated test signal 1	$P_1 = P_{i(ref)} + 3$ dB
		generator 2: modulated test signal 2	$P_2 = P_1 + \alpha_{a(min)}$
α_c	co-channel rejection; Fig.11(b)	$f_2 = f_1 \pm$ up to 3 kHz	
		generator 1: modulated test signal 1	$P_1 = P_{i(ref)} + 3$ dB
		generator 2: modulated test signal 2	$P_2 = P_1 - \alpha_{c(max)}$
α_{sp}	spurious immunity; Fig.11(b)	f_2 = 100 kHz to 2 GHz	
		generator 1: modulated test signal 1	$P_1 = P_{i(ref)} + 3$ dB
		generator 2: modulated test signal 2	$P_2 = P_1 + \alpha_{sp(min)}$
α_{im}	intermodulation immunity; Fig.11(c)	$f_2 = f_1 \pm \Delta f_{cs}$; $f_3 = f_1 \pm 2\Delta f_{cs}$	
		generator 1: modulated test signal 1	$P_1 = P_{i(ref)} + 3$ dB
		generator 2: unmodulated	$P_2 = P_1 + \alpha_{im(min)}$
		generator 3: modulated test signal 2	$P_3 = P_2$
α_{bl}	blocking immunity; Fig.11(b)	$f_2 = f_1 \pm 1$ MHz	
		generator 1: modulated test signal 1	$P_1 = P_{i(ref)} + 3$ dB
		generator 2: modulated test signal 2	$P_2 = P_1 + \alpha_{bl(min)}$
f_{offset}	frequency offset range; Fig.11(a)	deviation = ±4.0 kHz, $f_1 = f_{i(RF)} \pm 2$ kHz ($f_{offset(min)}$)	
		generator 1: modulated test signal 1	$P_1 = P_{i(ref)} + 3$ dB
Δf_{dev}	deviation range; Fig.11(a)	deviation = ±2.5 to ±7 kHz; ($\Delta f_{dev(min)}$ to $\Delta f_{dev(max)}$)	
		generator 1: modulated test signal 1	$P_1 = P_{i(ref)} + 3$ dB
t_{on}	receiver turn-on time; Fig.11(a)	note 3	
		generator 1: modulated test signal 1	$P_1 = P_{i(ref)} + 10$ dB

Notes

1. The tests are executed without load on pins TPI and TPQ.
2. All minimum and maximum values correspond to a bit error rate (BER) $\leq 3/100$ in the wanted signal (P_1).
3. The BER measurement is started 5 ms ($t_{on(max)}$) after V_{RE} goes HIGH; BER is then measured for 100 bits (BER $\leq 3/100$).



(a) One generator.
(b) Two generators.
(c) Three generators.
(1) See Fig.12.

Fig.11 Test configurations.

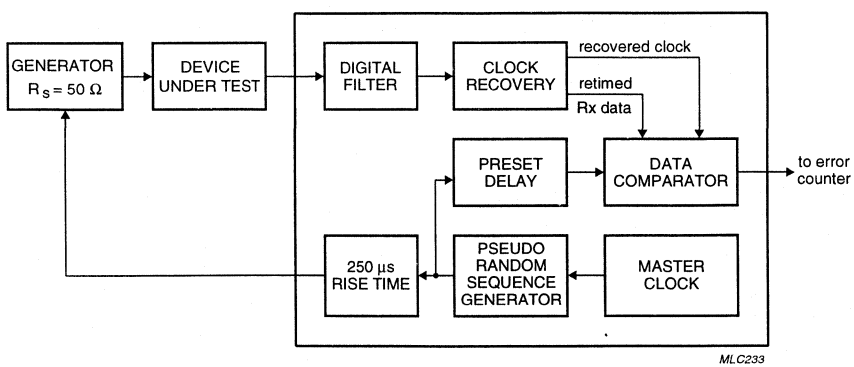


Fig.12 BER test facility.

PRINTED-CIRCUIT BOARDS

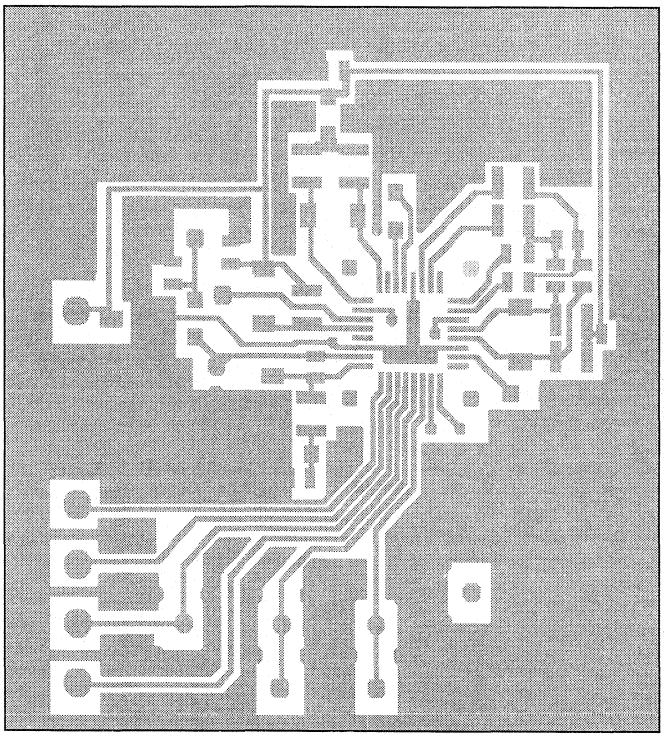


Fig.13 PCB top view for LQFP32; test circuit Figs 1 and 3.

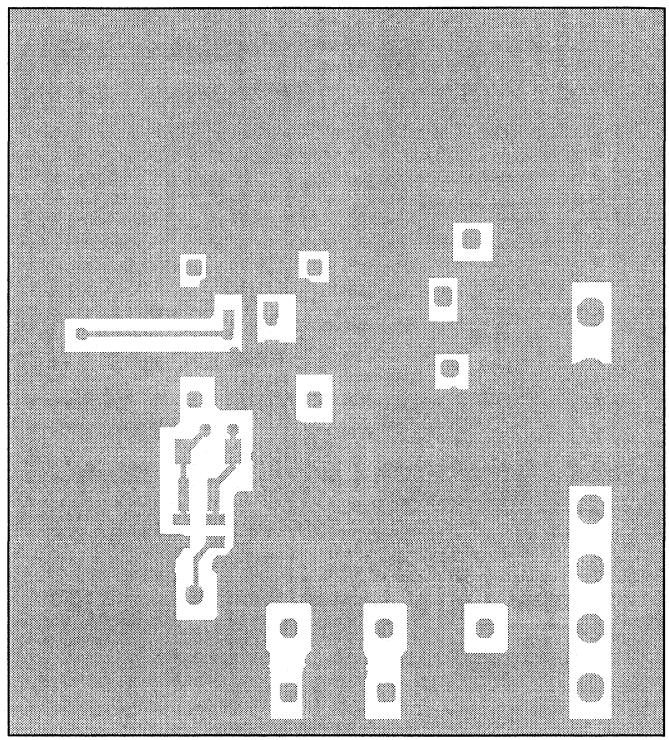
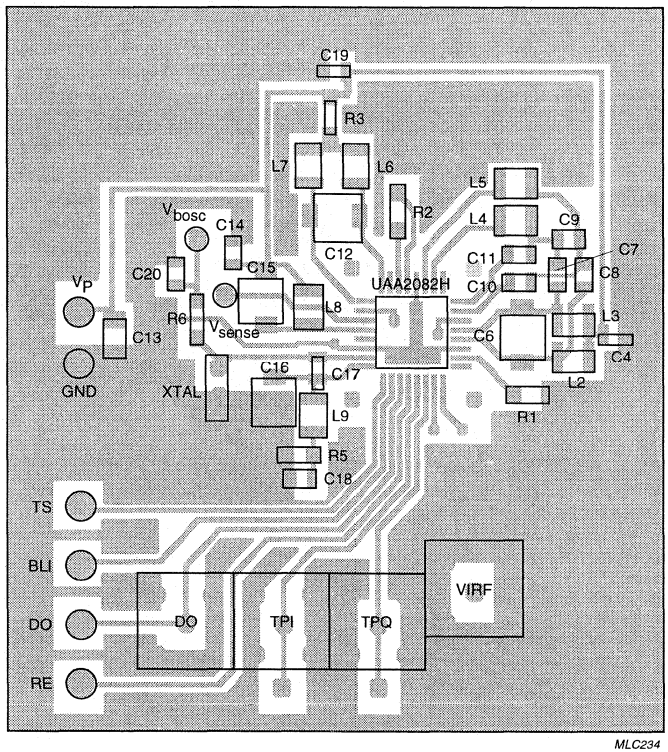


Fig.14 PCB bottom view for LQFP32; test circuit Figs 1 and 3.



V_{EE} = GND; V_C = V_P.

Fig.15 PCB top view with components for LQFP32; test circuit Fig.3.

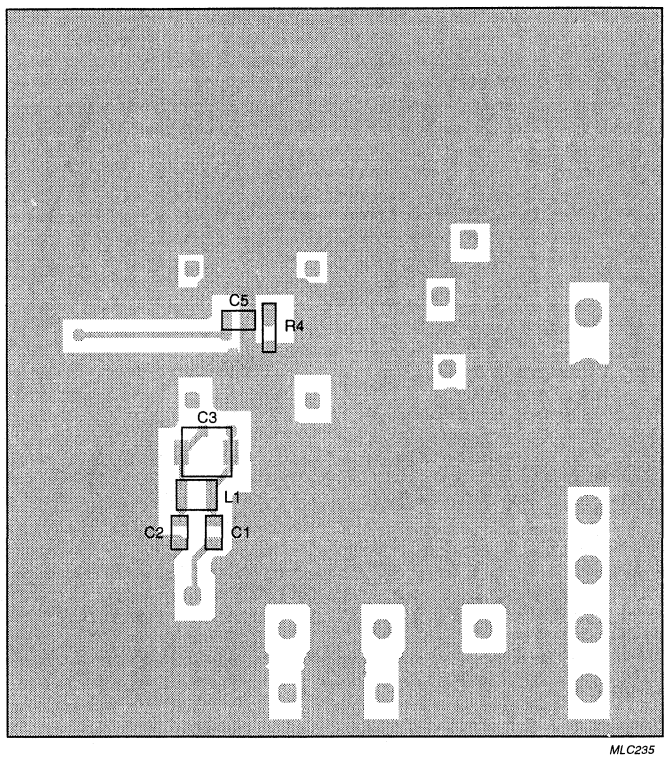


Fig.16 PCB bottom view with components for LQFP32; test circuit Fig.3.

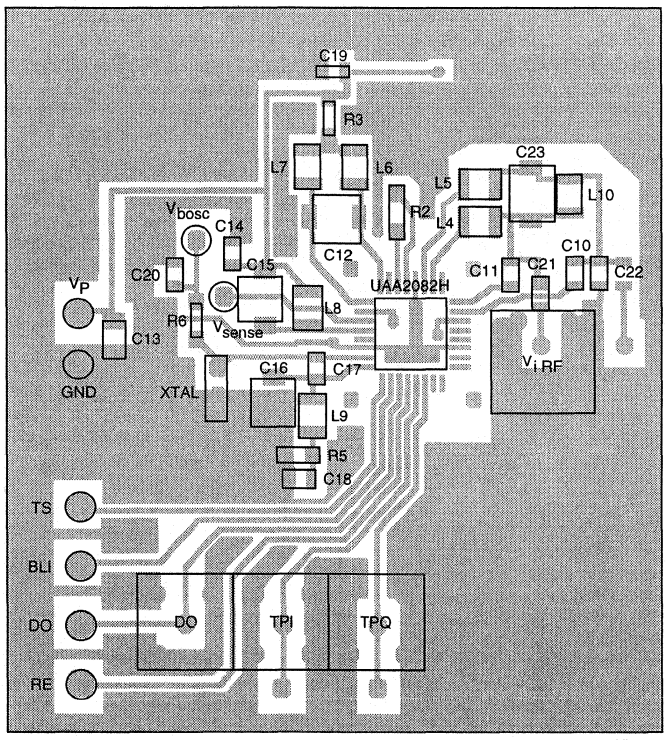


Fig.17 PCB top view with components for LQFP32; test circuit Fig.5.

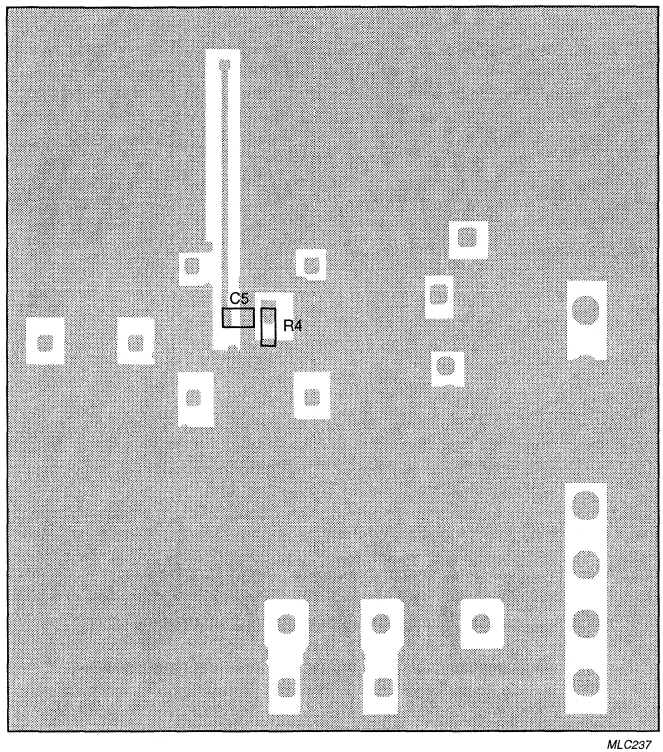


Fig.18 PCB bottom view with components for LQFP32; test circuit Fig.5.

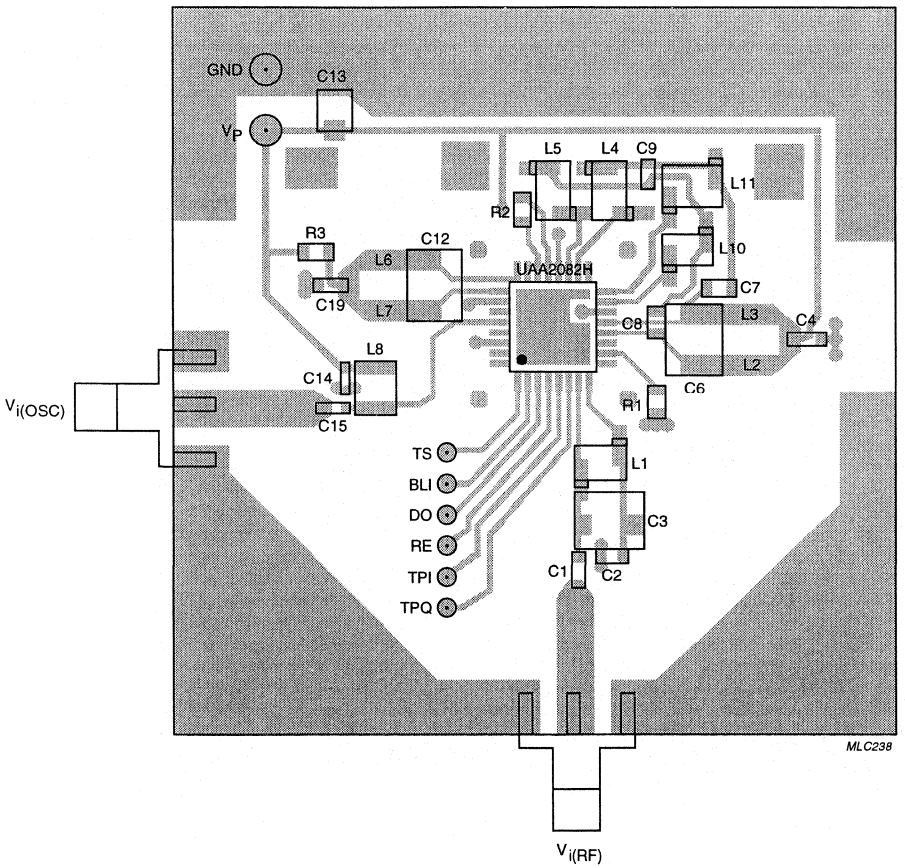


Fig.19 PCB top view with components for LQFP32; test circuit Fig.6.

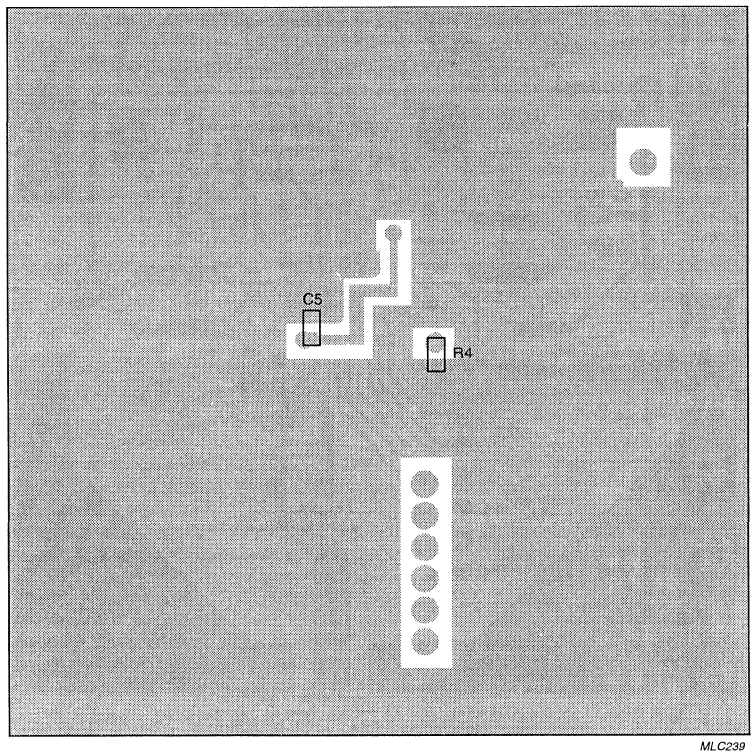


Fig.20 PCB bottom view with components for LQFP32; test circuit Fig.6.

Cordless telephone, answering machine line interface

UBA1707

FEATURES

Line interface

- Low DC line voltage; operates down to 1.2 V (excluding polarity guard)
- Voltage regulator with adjustable DC voltage
- DC mask for voltage and current regulation
- Line current limitation for protection
- Electronic hook switch control input
- Transmit amplifier with:
  - Symmetrical inputs
  - Fixed gain
  - Large signals handling capability.
- Receive amplifier with fixed gain
- Transmit and receive amplifiers AGC for line loss compensation.

Auxiliary amplifier

- Fixed gain.

Loudspeaker channel

- Dual inputs
- Rail-to-rail output stage for single-ended load drive
- High output current capability
- Dynamic limiter to prevent distortion
- Digital volume control
- Fixed maximum gain.

General purpose switches

- Three switches with open-collector.

3-wires serial bus interface

Allows to control:

- DC mask (voltage or current regulation)
- Receive amplifier mute function
- AGC:
  - On/off
  - Slope
  - I_{start} line current.
- Auxiliary amplifier mute function
- Loudspeaker channel:
  - Input selection
  - Volume setting
  - Dynamic limiter inhibition
  - Power-down mode.
- General purpose switches state
- Global power-down mode.

Supply

Operates with external supply voltage from 3.0 to 5.5 V.

APPLICATIONS

- Cordless base stations
- Answering machines
- Mains or battery-powered telephone sets.

GENERAL DESCRIPTION

The UBA1707 is a BiCMOS integrated circuit intended for use in mains-powered telecom terminals. It performs all speech and line interface functions, DC mask for voltage or current regulation and electronic hook switch control. The device includes an auxiliary amplifier, a loudspeaker channel and general purpose switches.

Most of the characteristics are programmable via a 3-wire serial bus interface.

ORDERING INFORMATION

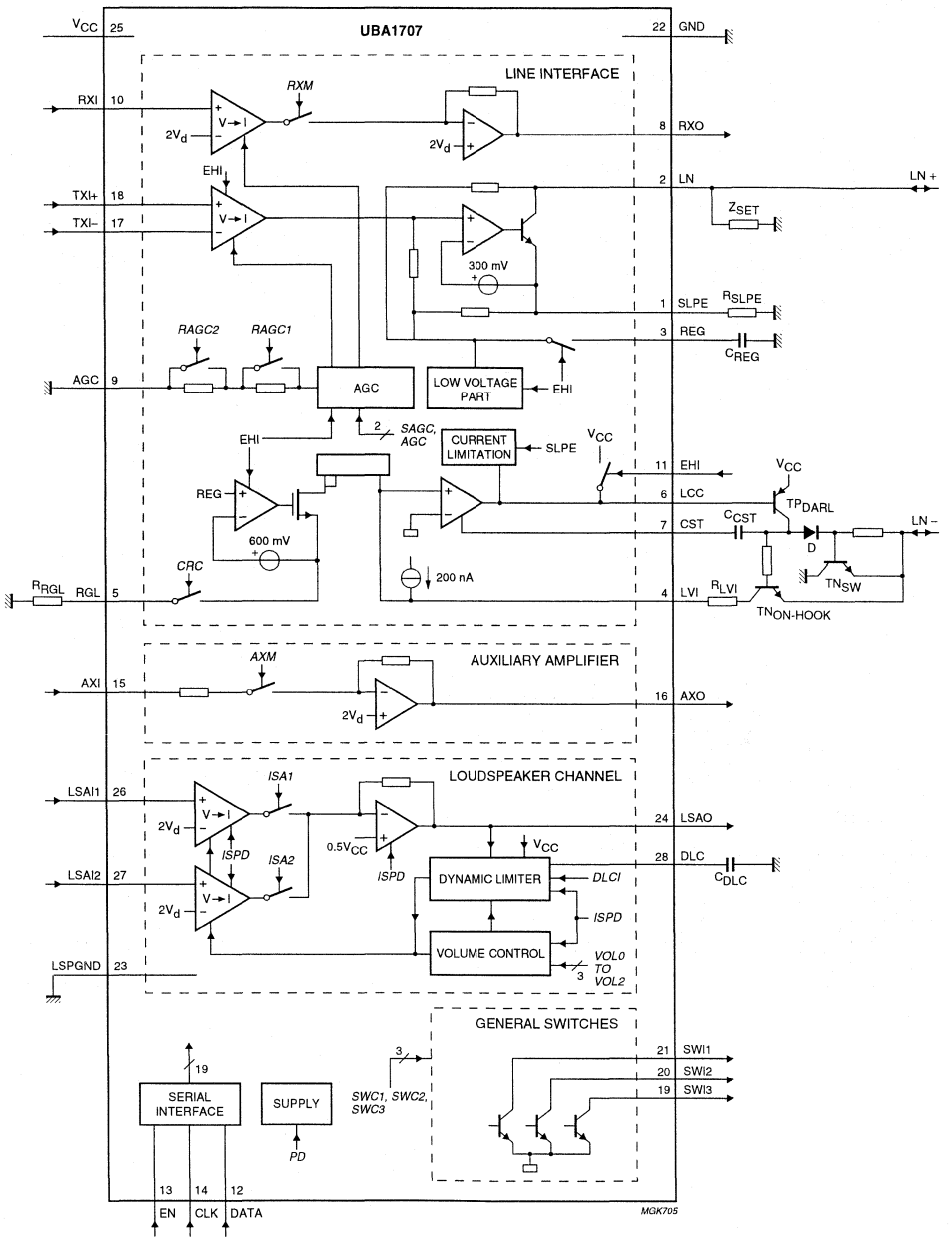
TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UBA1707T	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
UBA1707TS	SSOP28	plastic shrink small outline package; 28 leads; body width 5.3 mm	SOT341-1

QUICK REFERENCE DATA

I_{line} = 15 mA; V_{CC} = 3.3 V; R_{SLPE} = 10 Ω; AGC pin connected to GND; Z_{line} = 600 Ω; Z_{SET} = 619 Ω; EHI = HIGH; f = 1 kHz; T_{amb} = 25 °C; bit AGC at logic 1, all other configuration bits at logic 0; measured in test circuit of Fig.17; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	operating voltage range		3.0	–	5.5	V
I_{CC}	current consumption from pin V_{CC}	normal operation; bit PD = 0	–	2.2	tbf	mA
		power-down mode; bit PD = 1	–	110	tbf	μA
I_{line}	line current operating range	normal operation	11	–	130	mA
		with reduced performance	tbf	–	11	mA
V_{LN}	DC line voltage		tbf	3.1	tbf	V
R_{REGC}	DC mask slope in current regulation mode	I_{line} > 35 mA (typical); R_{LVI} = 1 MΩ; R_{RGL} = 7.15 kΩ; bit CRC = 1	–	1.4	–	kΩ
$G_{v(trx)}$	voltage gain					
	transmit amplifier from TXI to LN	V_{TXI} = 50 mV (RMS)	11	12	13	dB
	receive amplifier from RXI to RXO	V_{RXI} = 2 mV (RMS)	37	38	39	dB
$\Delta G_{v(trx)}$	gain control range for transmit and receive amplifiers with respect to I_{line} = 15 mA	I_{line} = 90 mA	–	6.5	–	dB
$G_{v(AX)}$	voltage gain from AXI to AXO	V_{AXI} = 2 mV (RMS)	30.5	32	33.5	dB
$G_{v(LSA)}$	voltage gain from LSAI1 or LSAI2 to LSAO for maximum volume	V_{LSAI} = 8 mV (RMS); bits LSA1 = 1 and LSA2 = 1	26.5	28	29.5	dB
$\Delta G_{v(LSA)}$	voltage gain adjustment range for loudspeaker channel	bits (VOL0, VOL1 and VOL2) from (0, 0, 0) to (1, 1, 1)	–	21	–	dB
$\Delta G_{v(LSA)s}$	voltage gain adjustment step for loudspeaker channel	VOL0 from 0 to 1	–	3	–	dB

BLOCK DIAGRAM



Bit names are given in italics.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SLPE	1	connection for slope resistor
LN	2	positive line terminal
REG	3	line voltage regulator decoupling
LVI	4	negative line voltage sense input
RGL	5	reference for current regulation mode
LCC	6	line current control output
CST	7	input for stability capacitor
RXO	8	receive amplifier output
AGC	9	automatic gain control/line loss compensation adjustment
RXI	10	receiver amplifier input
EHI	11	electronic hook switch control input
DATA	12	serial bus data input
EN	13	programming serial bus enable input
CLK	14	serial bus clock input
AXI	15	auxiliary amplifier input
AXO	16	auxiliary amplifier output
TXI–	17	inverted transmit amplifier input
TXI+	18	non-inverted transmit amplifier input
SWI3	19	NPN open-collector output 3
SWI2	20	NPN open-collector output 2
SWI1	21	NPN open-collector output 1
GND	22	ground reference
LSPGND	23	ground reference for the loudspeaker amplifier
LSAO	24	loudspeaker amplifier output
V_{CC}	25	supply voltage
LSAI1	26	loudspeaker amplifier input 1
LSAI2	27	loudspeaker amplifier input 2
DLC	28	dynamic limiter timing adjustment

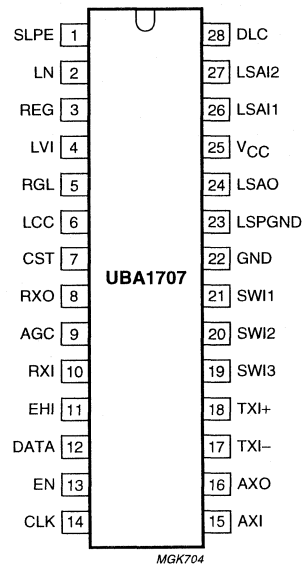


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

All data given in this chapter are typical values, except when otherwise specified.

Supply (pins V_{CC} and GND; bits PD and LSPD)

The UBA1707 must be supplied with an external stabilized voltage source between pins V_{CC} and GND.

Pins GND and LSPGND must be connected together.

Without any signal, with the loudspeaker channel enabled at minimum volume and without any general purpose switch selected, the internal current consumption is 2.2 mA at V_{CC} = 3.3 V. Each selected switch (pins SWI1, SWI2, or SWI3) increases the current consumption by 530 µA.

The supply current can be reduced when the loudspeaker channel is not used by switching it off (bit LSPD at logic 1). The current consumption is then decreased by approximately 800 µA at minimum volume.

To drastically reduce current consumption, the UBA1707 is provided with a power-down mode controlled by bit PD. When bit PD is at logic 1, the current consumption from V_{CC} becomes 110 µA. In this mode, the serial interface is the only function which remains active.

Line interface

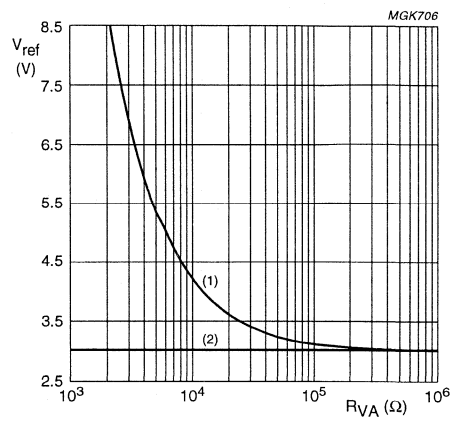
DC CHARACTERISTICS (PINS LN, SLPE, REG, CST, LVI, LCC, RGL AND GND; BIT CRC)

The IC generates a stabilized reference voltage (V_{ref}) between pins LN and SLPE. This reference voltage is equal to 3.0 V, is temperature compensated and can be adjusted by means of an external resistor (R_{VA}). It can be increased by connecting the R_{VA} resistor between pins REG and SLPE (see Fig.3).

The voltage at pin REG is used by the internal regulator to generate the stabilized reference voltage and is decoupled by a capacitor (C_{REG}) which is connected to GND. This capacitor, converted into an equivalent inductance (see Section "Set impedance") realizes the set impedance conversion from its DC value (R_{SLPE}) to its AC value (Z_{SET} in the audio-frequency range). Figure 4 illustrates the reference voltage supply configuration. As can be seen from Fig.4, part of the line current flows into the Z_{SET} impedance network and is not sensed by the UBA1707. Therefore using the R_{VA} resistor to change value of the reference voltage will also modify all parameters related to the line current such as:

- The automatic gain control
- The DC mask management
- The low voltage area characteristics.

In the same way, changing the value of Z_{SET} also affects the characteristics. The IC has been optimized for V_{ref} = 3.0 V and Z_{SET} = 619 Ω.



(1) Influence of R_{VA} on V_{ref}.
(2) V_{ref} without influence of R_{VA}.

Fig.3 Reference voltage adjustment with R_{VA}.

The IC regulates the line voltage at pin LN which can be calculated as follows:

$$V_{LN} = V_{ref} + R_{SLPE} \times I_{SLPE}$$

$$I_{SLPE} = I_{line} - I_{ZSET} - I^* \cong I_{line} - I_{ZSET}$$

Where:

I_{line} = line current

I_{ZSET} = current flowing through Z_{SET}

I^* = current consumed between LN and GND (approximately 100 µA).

The preferred value for R_{SLPE} is 10 Ω. Changing R_{SLPE} will affect more than the DC characteristics; it also influences the transmit gain, the gain control characteristics, the sidetone level and the maximum output swing on the line.

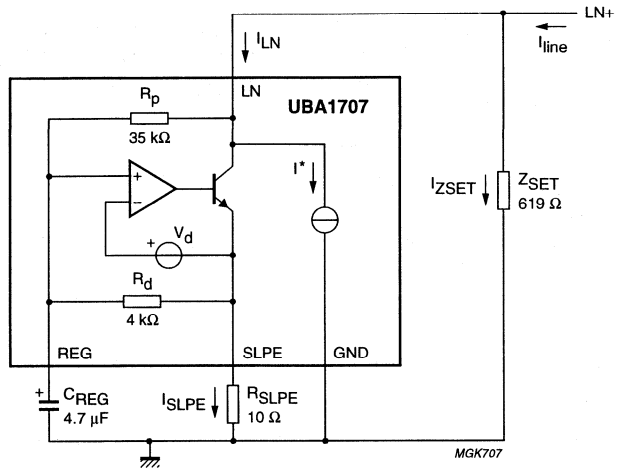


Fig.4 Reference voltage supply configuration.

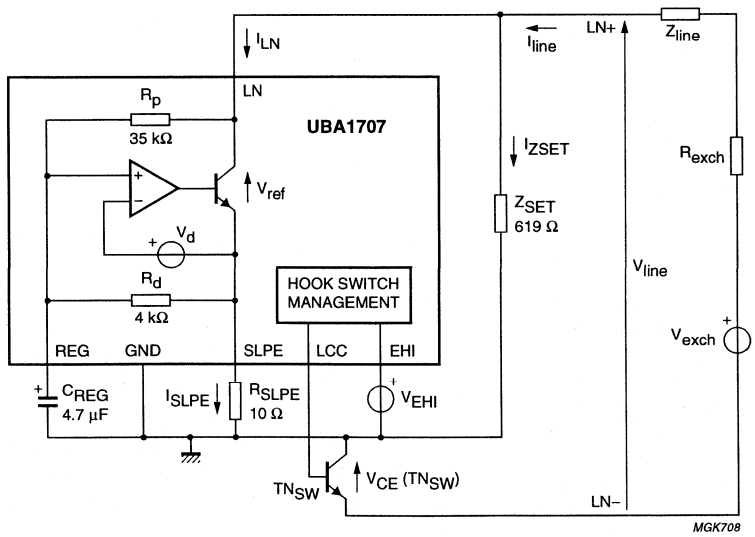


Fig.5 Line current settling simplified configuration.

The DC line current flowing into the set is determined by the exchange supply voltage (V_{exch}), the feeding bridge resistance (R_{exch}), the DC resistors of the telephone line (R_{line}) and the set (R_{SET}), the reference voltage (V_{ref}) and the voltage introduced by the transistor (TN_{SW}) used as line interrupter (see Fig.5). With a line current below I_{low} (8 mA with Z_{SET} = 619 Ω), the internal reference voltage (V_{ref}) is automatically adjusted to a lower value. This means that more sets can operate in parallel with DC line voltages (excluding the polarity guard) down to 1.2 V. At line current below I_{low}, the circuit has limited transmit and receive levels. This is called the low voltage area.

Figure 6 shows in more details how the UBA1707, in association with some external components, manages the line interrupter (TN_{SW} external transistor).

In on-hook conditions (voltage at pin EHI is LOW), the voltage at pin LCC is pulled-up to the supply voltage level (V_{CC}) to turn off the TP_{DARL} transistor. As a result, because of the R_{PLD} resistor, the TN_{SW} and $TN_{ON\text{-}HOOK}$ transistors are switched off. The $TN_{ON\text{-}HOOK}$ transistor disconnects the R_{LVI} resistor from the LN– line terminal in order to guarantee a high on-hook impedance.

In off-hook conditions (voltage at pin EHI is HIGH), an operational amplifier drives (at pin LCC) the base of TP_{DARL} which forms a current amplifier structure in association with TN_{SW}. The line current flows through TN_{SW} transistor. The $TN_{ON\text{-}HOOK}$ transistor is forced into deep saturation. A virtual ground is created at pin LVI because of the operational amplifier. A DC current (I_{LVI}) is sourced from pin LVI into the R_{LVI} resistor in order to generate a voltage source. Thus the voltage between pin GND and the negative line terminal (LN–) becomes:

$$V_{CE}(TN_{SW}) = R_{LVI} \times I_{LVI} + V_{CE}(TN_{ON\text{-}HOOK}) \cong R_{LVI} \times I_{LVI}$$

The voltage V_{line} between the line terminals LN+ and LN– can be calculated as follows:

$$V_{line} \cong V_{ref} + R_{SLPE} \times (I_{line} - I_{ZSET}) + V_{CE}(TN_{SW})$$

Where:

I_{line} = line current

I_{ZSET} = current flowing through Z_{SET}.

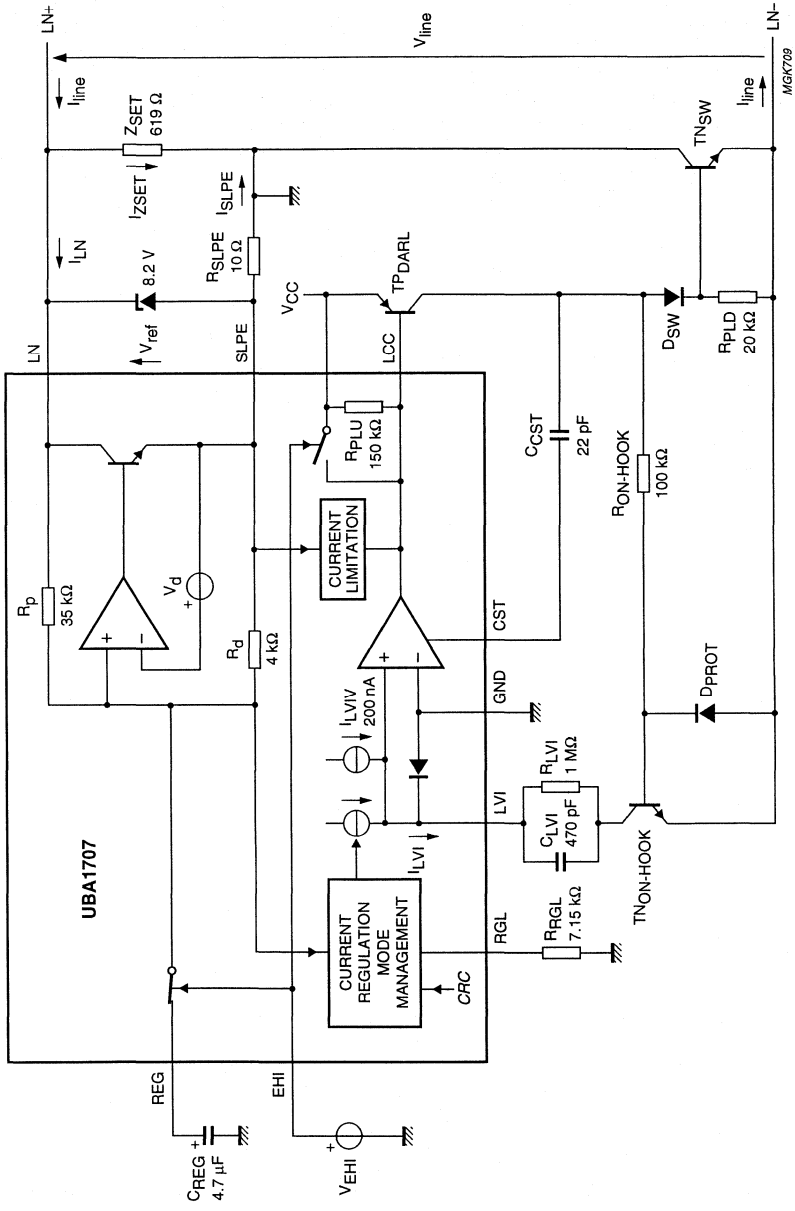
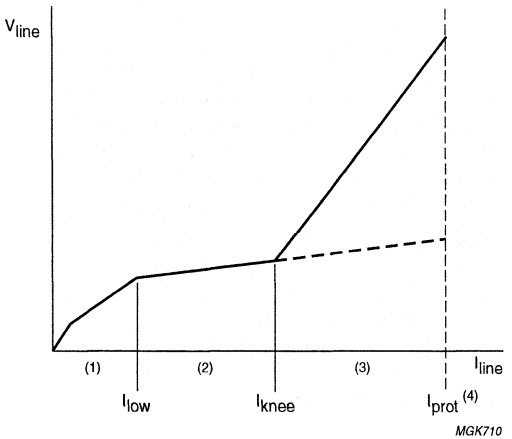


Fig.6 Line interrupter management and DC mask regulation configuration.

Bit names are given in italics.

The UBA1707 offers the possibility to choose two kinds of regulations for the DC characteristic between the line terminals LN+ and LN– (see Fig.7):

- Voltage regulation mode
- Current regulation mode.



(1) Low voltage area.
(2) Small slope (determined by R_{SLPE}).
(3) Small slope (dashed line; determined by R_{SLPE}) in voltage regulation mode.
High slope (full line; determined by R_{SLPE}, R_{LVI} and R_{RGL}) in current regulation mode.
(4) Current limitation.

Fig.7 General form of the DC mask as a function of regulation mode.

The regulation mode is selected by the bit CRC via the serial interface.

The DC mask regulation is realised by adjusting the DC voltage V_{CE} (TN_{SW}) between pin GND and line terminal LN– as a function of the line current.

Voltage regulation mode

In voltage regulation mode (bit CRC at logic 0), V_{CE} (TN_{SW}) voltage is fixed by means of a 200 nA DC constant current I_{LVIV} flowing through R_{LVI}.

Therefore V_{CE} (TN_{SW}) $\cong R_{LVI} \times I_{LVIV}$ = 200 mV in typical application (see Fig.18).

The slope $\Delta V_{line}/\Delta I_{line}$ of the V_{line}, I_{line} characteristic is $R_{REGV} \cong R_{SLPE}$.

Current regulation mode

In current regulation mode (bit CRC at logic 1), when the line current is lower than I_{knee} = 35 mA (with Z_{SET} = 619 Ω), V_{CE} (TN_{SW}) is fixed by means of a 200 nA DC constant current I_{LVIV} flowing through R_{LVI}. When the line current is higher than 35 mA, an additional current (proportional to the line current) flows through R_{LVI}. As a result, TN_{SW} works as a DC voltage source increasing with the line current. V_{CE} (TN_{SW}) can be calculated as follows:

$$V_{CE}(TN_{SW}) \cong R_{LVI} \times \left(\frac{R_{SLPE}}{R_{RGL}} \times (I_{line} - I_{knee}) + I_{LVIV} \right)$$

Where:

I_{line} = line current

R_{RGL} = resistor connected at pin RGL.

The slope $\Delta V_{line}/\Delta I_{line}$ of the V_{line}, I_{line} characteristic is determined by the ratio of resistors connected at pins SLPE, LVI and RGL, as follows:

$$R_{REGC} \cong R_{SLPE} + R_{LVI} \times \frac{R_{SLPE}}{R_{RGL}} = 1400\ \Omega \text{ in typical}$$

application (see Fig.18).

Current limitation

Whatever the selected mode is, the line current is limited to approximately 140 mA. This current is sensed on SLPE, for this purpose the external zener diode must be connected between pins LN and SLPE. The speech function no longer operates in this condition.

ELECTRONIC HOOK SWITCH CONTROL (PIN EHI)

The electronic hook switch input (EHI) controls the state of TP_{DARL} transistor. When the voltage applied at pin EHI is LOW, TP_{DARL} transistor is turned off. Voltage at pin LCC is pulled up to supply voltage (V_{CC}). TN_{SW} and $TN_{ON\text{-}HOOK}$ transistors are also turned off by means of a pull-down resistor (R_{PLD}). When the voltage applied at pin EHI is HIGH, TP_{DARL} transistor is driven by the operational amplifier at pin LCC and the regulation mode selected is operating. An internal 150 kΩ pull-up resistor is connected between pins LCC and V_{CC}.

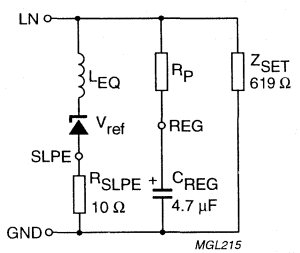
The EHI input can also be used for pulse dialling or register recall (timed loop break). During line breaks (voltage at pin EHI is LOW or open-circuit), the voltage regulator is switched off and the capacitor at pin REG is internally disconnected to prevent its discharge. As a result, the voltage stabilizer will have negligible switch-on delay after line interruptions. This minimizes the contribution of the IC to the current waveform during pulse dialling or register recall.

When the UBA1707 is in power-down mode (bit PD at logic 1), the TP_{DARL} transistor is forced to be turned off whatever the voltage applied at pin EHI.

Set impedance

In the audio frequency range, the dynamic impedance between pins LN and GND (illustrated in Fig.8) is mainly determined by the Z_{SET} impedance.

The impedance introduced by the external TN_{SW} transistor connected between pin GND and the negative line terminal (LN–) is negligible.



$L_{eq} = C_{REG} \times R_{SLPE} \times R_P$
R_P = internal resistance = 35 kΩ.

Fig.8 Equivalent impedance between LN and GND.

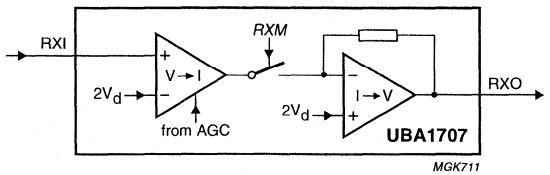
Transmit amplifier (pins TXI+ and TXI–)

The UBA1707 has symmetrical transmit inputs TXI+ and TXI–. The input impedance between pins TXI+ or TXI– and GND is 20 kΩ. The voltage gain from pins TXI+ or TXI– to pin LN is set at 12 dB with 600 Ω line load (Z_{line}) and 619 Ω set impedance. The inputs are biased at $2 \times V_d \cong 1.4$ V, with V_d representing the diode voltage. Automatic gain control is provided on this amplifier for line loss compensation.

Receive amplifier (pins RXI and RXO; bit RXM)

The receive amplifier (see Fig.9) has one input (RXI) and one output (RXO). The input impedance between pins RXI and GND is 20 kΩ. The rail-to-rail output stage is designed to drive a 500 µA peak current. The output impedance at pin RXO is approximately 100 Ω.

The voltage gain from pin RXI to pin RXO is set at 38 dB. This gain value compensates typically the attenuation of the anti-sidetone network (see Fig.10). The output as well as the input are biased at $2 \times V_d \cong 1.4$ V. Automatic gain control is provided on this amplifier for line loss compensation. This amplifier can be muted by activating the receive mute function (bit RXM at logic 1).



Bit names are given in italics.

Fig.9 Receive amplifier.

SIDETONE SUPPRESSION

The UBA1707 anti-sidetone network comprising $Z_{SET}//Z_{line}$, R_{ast1}, R_{ast2}, R_{ast3}, R_{SLPE} and Z_{bal} (see Fig.10) suppresses the transmitted signal in the received signal. Maximum compensation is obtained when the following conditions are fulfilled:

$$R_{SLPE} \times R_{ast1} = Z_{SET} \times (R_{ast2} + R_{ast3})$$

$$k = \frac{(R_{ast2} \times (R_{ast3} + R_{SLPE}))}{(R_{ast1} \times R_{SLPE})}$$

$$Z_{bal} = k \times Z_{line}$$

The scale factor 'k' is chosen to meet the compatibility with a standard capacitor from the E6 or E12 range for Z_{bal}.

In practice, Z_{line} varies considerably with the line type and the line length.

Therefore, the value chosen for Z_{bal} should be for an average line length which gives satisfactory sidetone suppression with short and long lines.

The suppression also depends on the accuracy of the match between Z_{bal} and the impedance of the average line.

The anti-sidetone network for the UBA1707 (see Fig.18) attenuates the receiving signal from the line by 38 dB before it enters the receiving amplifier. The attenuation is almost constant over the whole audio frequency range. A Wheatstone bridge configuration (see Fig.11) may also be used.

More information on the balancing of an anti-sidetone bridge can be obtained in our publication *"Applications Handbook for Wired Telecom Systems, IC03b"*, order number 9397 750 00811.

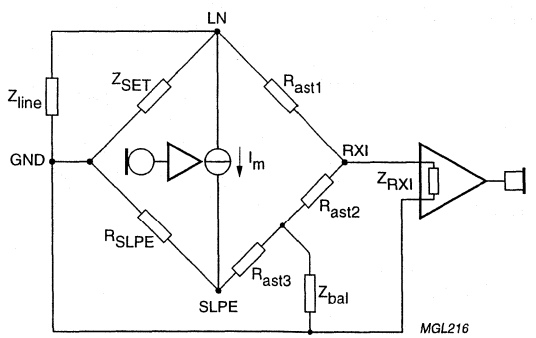


Fig.10 Equivalent circuit of UBA1707 anti-sidetone bridge.

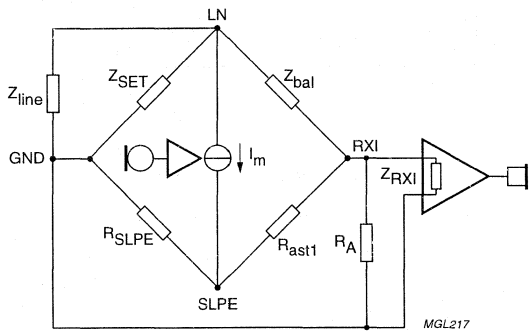


Fig.11 Equivalent circuit of an anti-sidetone network in a Wheatstone bridge configuration.

AUTOMATIC GAIN CONTROL (PIN AGC; BITS RAGC1, RAGC2, SAGC AND AGC)

The UBA1707 performs automatic line loss compensation. The automatic gain control varies the gain of the transmit amplifier and the gain of the receive amplifier in accordance with the DC line current. The control range is 6.5 dB (which roughly corresponds to a line length of 5.5 km for a 0.5 mm diameter twisted-pair copper cable with a DC resistance of 176 Ω/km and an average attenuation of 1.2 dB/km).

When the line current is greater than I_{stop}, the voltage gains are minimum. When the line current is less than I_{start}, the voltage gains are maximum. When the AGC pin is connected to pin GND, the start line current (I_{start}) can be chosen between 23 and 30 mA via bits RAGC1 and RAGC2 through the serial interface. Two values for the I_{stop}/I_{start} ratio (slope of the AGC) are possible via the bit SAGC through the serial interface. When bit SAGC is at logic 0 then $I_{stop} = 2.7 \times I_{start}$ (optimized for voltage regulation mode). When SAGC is at logic 1 then $I_{stop} = 1.9 \times I_{start}$ (optimized for current regulation mode).

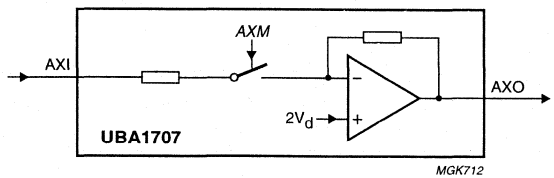
An external resistor R_{AGC} (connected between pins GND and AGC) enables the I_{start} and I_{stop} line currents to be increased (the ratio between I_{start} and I_{stop} is not affected by this external resistor). So internal and external adjustments of the automatic gain control allow optimization of the IC for many configurations of exchange supply voltage and feeding bridge resistance. Part of the line current flows into the Z_{SET} impedance network. The IC has been optimized for Z_{SET} = 619 Ω. Changing this 619 Ω value slightly modifies I_{stop} and I_{start} line currents as well as the value of the two AGC slopes.

The automatic gain control function can be disabled by setting the AGC bit to logic 0 via the serial interface or when pin AGC is left open-circuit. In this case both of the voltage gains are maximum.

Auxiliary amplifier (pins AXI and AXO; bit AXM)

The auxiliary amplifier (see Fig.12) has one input (AXI) and one output (AXO). The input impedance between pins AXI and GND is 3.65 kΩ. The rail-to-rail output stage is designed to drive a 500 μA peak current. The output impedance at pin AXO is approximately 100 Ω.

The output as well as the input are biased at $2 \times V_d \cong 1.4$ V DC voltage. The voltage gain from pin AXI to pin AXO is set at 32 dB.The amplifier can be muted by setting bit AXM at logic 1 via the serial interface. In this case, the input impedance between pins AXI and GND is infinite.



Bit names are given in italics.

Fig.12 Auxiliary amplifier.

Loudspeaker channel (see Fig.13)

LOUDSPEAKER AMPLIFIER (PINS LSAI1, LSAI2, LSAO AND LSPGND; BITS LSPD, LSA1 AND LSA2)

The loudspeaker amplifier has two symmetrical inputs LSAI1 and LSAI2 selectable independently by the bits LSA1 and LSA2 respectively. The input impedance between pins LSAI1or LSAI2 and GND is typically 20 kΩ. Each of these two inputs stages can accommodate signals up to 500 mV (RMS) at room temperature for less than 2% of Total Harmonic Distortion (THD) at minimum voltage gain.

The inputs are biased at $2 \times V_d \cong 1.4$ V DC voltage (whatever the state of bits LSA1 and LSA2).

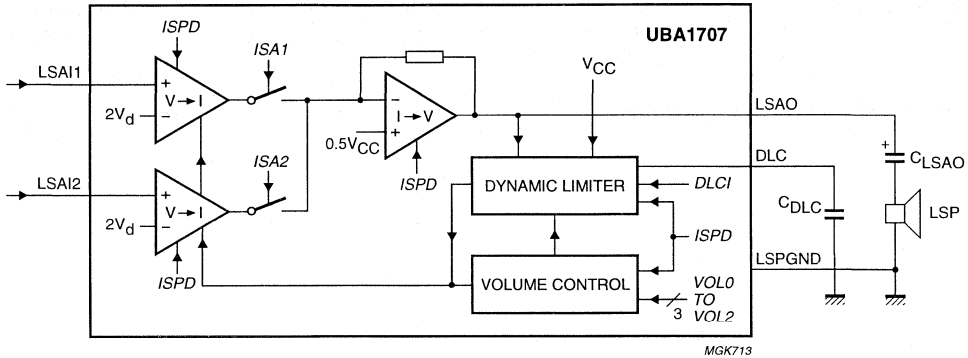
The rail-to-rail output stage is designed to power a loudspeaker connected as a single-ended load (between pins LSAO and LSPGND). The output LSAO is able to drive a 150 mA peak current.

As a result, it can drive loudspeaker loads down to 8 Ω at $V_{CC} = 3.3$ V and 16 Ω at $V_{CC} = 5.0$ V. The output is biased at $\frac{1}{2}V_{CC}$. Its output voltage capability is specified for continuous wave drive and depends on the value of V_{CC}.

In order to avoid crosstalk from the loudspeaker to other amplifiers, the loudspeaker current flows via pin LSPGND. This pin must be externally connected to pin GND.

The nominal value of the voltage gain for maximum volume from pins LSAI1 or LSAI2 to pin LSAO is set at 28 dB.

This amplifier is no longer supplied by setting the LSPD bit at logic 1 via the serial interface.



Bit names are given in italics.

Fig.13 Loudspeaker channel.

DYNAMIC LIMITER (PIN DLC; BIT DLCI)

The dynamic limiter of the UBA1707 prevents clipping of the loudspeaker output stage and protects the operation of the circuit when the supply voltage at V_{CC} falls below 2.7 V.

Hard clipping of the loudspeaker output stage is prevented by rapidly reducing the gain when the output stage starts to saturate. The time in which gain reduction is effected (clipping attack time) is approximately a few milliseconds. The circuit stays in the reduced gain mode until the peaks of the loudspeaker signals no longer cause saturation. The gain of the loudspeaker amplifier then returns to its normal value within the clipping release time (typically 250 ms). Both attack and release times are proportional to the value of the capacitor C_{DLC}. The total harmonic distortion of the loudspeaker output stage, in reduced gain mode, stays below 5% up to 10 dB (minimum) of input voltage overdrive [providing V_{LSAI} is below 500 mV (RMS)].

When the supply voltage drops below an internal threshold voltage of 2.7 V, the gain of the loudspeaker amplifier is rapidly reduced (approximately 1 ms). When the supply voltage exceeds 2.7 V, the gain of the loudspeaker amplifier is increased again.

The hard clipping of the dynamic limiter can be inhibited by setting the DLCI bit at logic 1, via the serial interface.

The dynamic limiter is no longer supplied by setting the LSPD bit at logic 1. In this case, the C_{DLC} capacitor charge is maintained to allow the gain of the loudspeaker amplifier to return to its nominal value as soon as the loudspeaker channel is supplied again.

VOLUME CONTROL (BITS VOL0, VOL1 AND VOL2)

The loudspeaker amplifier voltage gain can be reduced in steps of 3 dB via the serial interface (via bits VOL0, VOL1 and VOL2). These bits provide 7 steps of voltage gain adjustment. The voltage gain is maximum when all bits are at logic 1 and is reduced by 21 dB when all bits are at logic 0.

General purpose switches (pins SWI1, SWI2 and SWI3; bits SWC1, SWC2 and SWC3)

The UBA1707 is equipped with 3 general purpose open-collector switches which short the pins SWI1, SWI2 and SWI3 to ground. They are respectively controlled by bits SWC1, SWC2 and SWC3 and have an operating voltage limited to 12 V. The outputs have to be current biased.

For a bias current between 2 and 20 mA, the AC impedance is 30 Ω maximum.

Serial interface (pins DATA, CLK and EN)

A simple 3-wire unidirectional serial bus is used to program the circuit. The 3 wires of the bus are EN, CLK and DATA. The data sent to the device is loaded in bursts framed by EN. Programming clock edges (falling edges) and their appropriate data bits are ignored until EN goes active HIGH. The programmed information is loaded into the addressed register when EN returns inactive (LOW) or left open-circuit.

During normal operation, EN should be kept LOW. Only the last 8 bits serially clocked into the device are retained within the programming register. Additional leading bits are ignored and no check is made on the number of clock pulses. It can always capture new programming data even during global power-down (bit PD at logic 1).

Data is entered with the most significant bit first. The leading 6 bits make up the data field (bits D0 to D5) while the trailing 2 bits are the address field (bits ADO and AD1). The first bit entered is D5, the last bit AD0. This organisation allows to send only the number of bits of the addressed register.

Figure 16 shows the serial timing diagram. Table 1 gives the list of registers.

When the supply voltage V_{CC} drops below 2.5 V, all register files are set in the initial state (see Table 1) defined by the power-up reset. At start-up, the circuit is in power-down mode.

In the event that the IC is used in a noisy environment, it is advised to periodically refresh the content of registers.

Table 1 Register description

BIT NAME	FUNCTION	POLARITY	DATA	ADDRESS	STATE AT POWER-UP RESET
Register 0: general purpose switches state and DC mask regulation mode					
SWC1	SWI1 output connection	0: SWI1 switched-off	D0	(AD1, AD0) = (0,0)	0
		1: SWI1 switched-on			
SWC2	SWI2 output connection	0: SWI2 switched-off	D1		0
		1: SWI2 switched-on			
SWC3	SWI3 output connection	0: SWI3 switched-off	D2		0
		1: SWI3 switched-on			
un	unused	must be set to logic 0	D3		0
CRC	current regulation mode	0: voltage regulation	D4		0
		1: current regulation			
Register 1: automatic gain control					
RAGC1	AGC range selection 1		D0	(AD1, AD0) = (0,1)	0
RAGC2	AGC range selection 2		D1		0
SAGC	AGC slope selection	0: 2.7 type slope; note 1	D2		0
		1: 1.9 type slope; note 1			
AGC	line loss compensation mode	0: AGC inhibited	D3		0
		1: AGC enabled			
Register 2: loudspeaker channel					
LSA1	loudspeaker channel input 1 selection	0: LSAI1 unselected	D0	(AD1, AD0) = (1,0)	0
		1: LSAI1 selected			
LSA2	loudspeaker channel input 2 selection	0: LSAI2 unselected	D1		0
		1: LSAI2 selected			
LSPD	loudspeaker channel power-down	0: channel on	D2		0
		1: channel in power-down			
VOL0	volume control (least significant bit)		D3		0
VOL1	volume control		D4		0
VOL2	volume control (most significant bit)		D5		0
Register 3: mute functions and power-down					
AXM	auxiliary amplifier mute	0: amplifier enabled	D0	(AD1, AD0) = (1,1)	0
		1: amplifier muted			
RXM	receive amplifier mute	0: amplifier enabled	D1		0
		1: amplifier muted			
PD	reduced consumption mode	0: normal operating mode	D2		1
		1: power-down mode			
DLCI	dynamic limiter inhibit	0: limiter enabled	D3		0
		1: limiter inhibited			

Note

1. See Section "Automatic gain control (pin AGC; bits RAGC1, RAGC2, SAGC and AGC)".

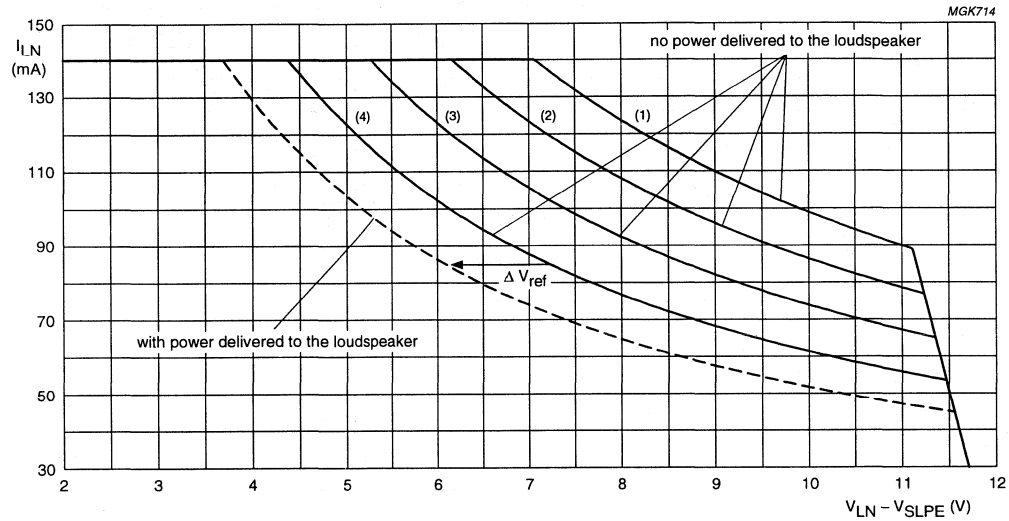
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage on pin V_{CC}		GND – 0.4	5.5	V
V_{LN}	positive continuous line voltage on pin LN		GND – 0.4	12.0	V
	repetitive line voltage during switch-on or line interruption		GND – 0.4	13.2	V
V_{SWIn}	voltage on pins SWI1, SWI2, and SWI3	continuous	GND – 0.4	12.0	V
		during switching	GND – 0.4	13.2	V
$V_{n(max)}$	maximum voltage on all other pins		GND – 0.4	V_{CC} + 0.4	V
I_{LN}	current sunk by pin LN	see Figs 14 and 15	–	150	mA
I_{SWIn}	continuous current sunk by pins SWI1, SWI2, and SWI3	bit SWCn = 1	–	20	mA
P_{tot}	total power dissipation	T_{amb} = 75 °C; see Figs 14 and 15			
	UBA1707T		–	625	mW
	UBA1707TS		–	416	mW
T_{stg}	IC storage temperature		–40	+125	°C
T_{amb}	operating ambient temperature		–25	+75	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	in free air		
	UBA1707T		80	K/W
	UBA1707TS		120	K/W



LINE	T_{amb} (°C)	P_{tot} (mW)
(1)	45	1000
(2)	55	875
(3)	65	750
(4)	75	625

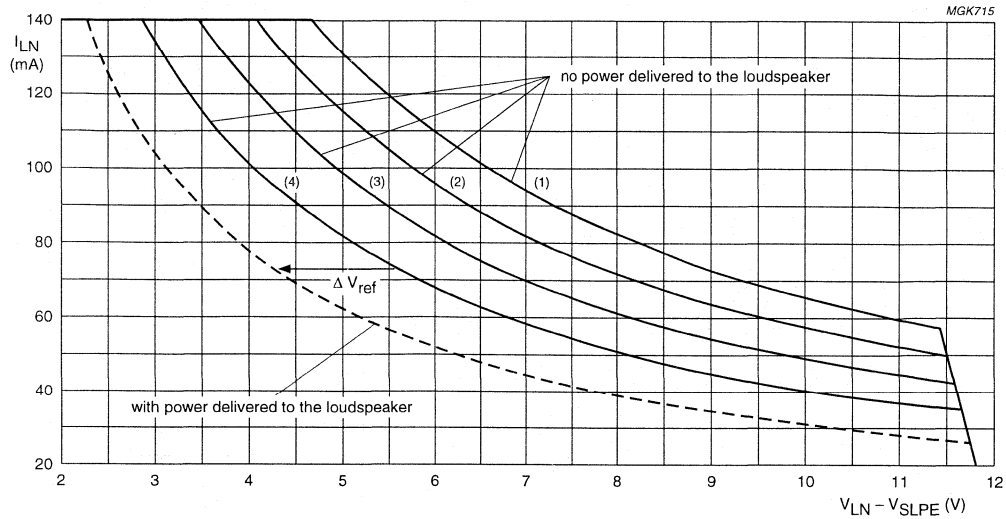
The line current value can be calculated from I_{LN} value as follows:

$$I_{line} = \frac{I_{LN} \times (R_{SET} + R_{SLPE}) + V_{LN} - V_{SLPE}}{R_{SET}}$$ where R_{SET} is the resistive part of Z_{SET}.

When power is delivered to a loudspeaker with R_L impedance, the curves must be shifted to the left by:

$$\Delta V_{ref} = \frac{V_{CC}^2}{2 \times \pi^2 \times R_L \times I_{LN}}$$ with maximum power dissipated by the loudspeaker amplifier (dotted line given for V_{CC} = 5.5 V, R_L = 16 Ω).

Fig.14 Safe operating area (UBA1707T).



LINE	T_{amb} (°C)	P_{tot} (mW)
(1)	45	666
(2)	55	583
(3)	65	500
(4)	75	416

The line current value can be calculated from I_{LN} value as follows:

$$I_{line} = \frac{I_{LN} \times (R_{SET} + R_{SLPE}) + V_{LN} - V_{SLPE}}{R_{SET}}$$ where R_{SET} is the resistive part of Z_{SET}.

When power is delivered to a loudspeaker with R_L impedance, the curves must be shifted to the left by:

$$\Delta V_{ref} = \frac{V_{CC}^2}{2 \times \pi^2 \times R_L \times I_{LN}}$$ with maximum power dissipated by the loudspeaker amplifier (dotted line given for V_{CC} = 5.5 V, R_L = 16 Ω).

Fig.15 Safe operating area (UBA1707TS).

CHARACTERISTICS

I_{line} = 15 mA; V_{CC} = 3.3 V; R_{SLPE} = 10 Ω; AGC pin connected to GND; Z_{line} = 600 Ω; Z_{SET} = 619 Ω; EHI = HIGH; f = 1 kHz; T_{amb} = 25 °C; bit AGC at logic 1, all other configuration bits at logic 0; measured in test circuit of Fig.17; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pins V_{CC} and GND; bit PD)						
V_{CC}	operating supply voltage		3.0	–	5.5	V
I_{CC}	current consumption from pin V_{CC}		–	2.2	tbf	mA
$I_{CC(pd)}$	current consumption from pin V_{CC} in power-down mode	bit PD = 1	–	110	tbf	µA
Line interface (pins LN, SLPE and REG)						
DC CHARACTERISTICS						
V_{ref}	stabilized voltage between pins LN and SLPE	I_{line} = 11 to 140 mA	tbf	3.0	tbf	V
V_{LN}	DC line voltage between pins LN and GND	I_{line} = 2 mA	–	1.2	–	V
		I_{line} = 4 mA	–	1.8	–	V
		I_{line} = 15 mA	tbf	3.1	tbf	V
		I_{line} = 140 mA	–	4.35	–	V
$V_{LN(Rext)}$	DC line voltage between pins LN and SLPE with an external resistor R_{VA}	$R_{VA(SLPE-REG)}$ = 8 kΩ	–	4.5	–	V
$\Delta V_{LN(T)}$	DC line voltage variation with temperature referenced to 25 °C	T_{amb} = −25 to +75 °C	–	tbf	–	mV
Masks regulation (pins LCC, LVI, CST and RGL; bit CRC)						
DC CHARACTERISTICS						
$I_{LCC(max)}$	maximum current sunk by pin LCC		200	–	–	µA
$R_{int(LCC)}$	internal resistance between pins V_{CC} and LCC		–	150	–	kΩ
Voltage regulation mode						
I_{LVIV}	current sourced from pin LVI	bit CRC = 0	–	200	–	nA
Current regulation mode						
I_{knee}	start line current for current regulation mode	bit CRC = 1	–	35	–	mA
R_{REGC}	DC mask slope in current regulation mode	$I_{line} > I_{knee}$; R_{LVI} = 1 MΩ; R_{RGL} = 7.15 kΩ; bit CRC = 1	–	1.4	–	kΩ
Current limitation						
I_{prot}	current limitation level		–	140	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Electronic hook-switch control (pin EHI)						
V_{IH}	HIGH-level input voltage		2.3	–	V_{CC} + 0.4	V
V_{IL}	LOW-level input voltage	V_{CC} = 3.0 to 5.5 V	GND – 0.4	–	0.3V_{CC}	V
I_{bias}	input bias current	input level = HIGH	0	1.5	3	µA
Transmit amplifier (pins TXI+, TXI– and LN)						
$\|Z_i\|$	input impedance	between pins TXI+ and GND or TXI– and GND	–	20	–	kΩ
		between pins TXI+ and TXI–	–	36	–	kΩ
$G_{v(TX)}$	voltage gain from TXI+/TXI– to LN	V_{TXI} = 50 mV (RMS)	11	12	13	dB
$\Delta G_{v(TX)(f)}$	voltage gain variation with frequency referenced to 1 kHz	f = 300 to 3400 Hz	–	±0.3	–	dB
$\Delta G_{v(TX)(T)}$	voltage gain variation with temperature referenced to 25 °C	T_{amb} = –25 to +75 °C	–	±0.3	–	dB
CMRR	common mode rejection ratio		–	tbf	–	dB
PSRR	power supply rejection ratio		–	36	–	dB
$V_{LN(max)(rms)}$	maximum sending signal (RMS value)	I_{line} = 15 mA; THD = 2%	1.2	1.4	–	V
		I_{line} = 4 mA; THD = 10%	–	0.26	–	V
$V_{iTX(max)(rms)}$	maximum transmit input voltage (RMS value) for 2% THD on pin LN	I_{line} = 15 mA	–	0.35	–	V
		I_{line} = 90 mA	–	0.75	–	V
$V_{no(LN)}$	noise output voltage at pin LN	pins TXI+ and TXI– short-circuited through 200 Ω in series with 10 µF; psophometrically weighted (P53 curve)	–	–74	–	dBmp
Receive amplifier (pins RXI and RXO; bit RXM)						
$\|Z_i\|$	input impedance between pins RXI and GND		–	20	–	kΩ
$G_{v(RX)}$	voltage gain from RXI to RXO	V_{RXI} = 2 mV (RMS)	37	38	39	dB
$\Delta G_{v(RX)(f)}$	voltage gain variation with frequency referenced to 1 kHz	f = 300 to 3400 Hz	–	±0.3	–	dB
$\Delta G_{v(RX)(T)}$	voltage gain variation with temperature referenced to 25 °C	T_{amb} = –25 to +75 °C	–	±0.3	–	dB
PSRR	power supply rejection ratio		–	70	–	dB
THD	total harmonic distortion	V_{RXI} = 2 mV (RMS)	–	0.03	–	%
		V_{RXI} = 12.5 mV (RMS)	–	2	–	%
		V_{RXI} = 19.5 mV (RMS); I_{line} = 90 mA	–	2	–	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{no(RXO)(rms)}$	noise output voltage at pin RXO (RMS value)	RXI open-circuit; psophometrically weighted (P53 curve)	–	–81	–	dBVp
$\Delta G_{v(RX)(m)}$	voltage gain reduction from pin RXI to RXO when muted	V_{RXI} = 10 mV (RMS); bit RXM = 1	–	80	–	dB
Automatic gain control (pin AGC; bits RAGC1, RAGC2, SAGC and AGC)						
$\Delta G_{v(trx)}$	gain control range for transmit and receive amplifiers with respect to I_{line} = 15 mA	I_{line} = 90 mA	–	6.5	–	dB
I_{start}	highest line current for maximum gain	bits RAGC1 = 1; RAGC2 = 1	–	23	–	mA
		bits RAGC1 = 1; RAGC2 = 0	–	25.5	–	mA
		bits RAGC1 = 0; RAGC2 = 1	–	27.5	–	mA
		bits RAGC1 = 0; RAGC2 = 0	–	30	–	mA
I_{stop}	lowest line current for minimum gain when I_{start} = 23 mA	bits SAGC = 0; RAGC1 = 1; RAGC2 = 1	–	62	–	mA
		bits SAGC = 1; RAGC1 = 1; RAGC2 = 1	–	44	–	mA
$\Delta G_{v(trxoff)}$	gain variation for transmit and receive amplifiers when AGC is off	bit AGC = 0; I_{line} = 15 to 140 mA	–	–	±0.2	dB
Amplifiers						
AUXILIARY AMPLIFIER (PINS AXI AND AXO; BIT AXM)						
$\|Z_i\|$	input impedance between pins AXI and GND		–	3.65	–	kΩ
$G_{v(AX)}$	voltage gain from pin AXI to AXO	V_{AXI} = 2 mV (RMS)	30.5	32	33.5	dB
$\Delta G_{v(AX)(f)}$	voltage gain variation with frequency referenced to 1 kHz	f = 300 to 3400 Hz	–	±0.3	–	dB
$\Delta G_{v(AX)(T)}$	voltage gain variation with temperature referenced to 25 °C	T_{amb} = –25 to +75 °C	–	±0.3	–	dB
PSRR	power supply rejection ratio		–	82	–	dB
$V_{no(AXO)(rms)}$	noise output voltage at pin AXO (RMS value)	pin AXI connected to pin GND through 200 Ω in series with 10 µF; psophometrically weighted (P53 curve)	–	–83	–	dBVp
$\Delta G_{v(AX)(m)}$	voltage gain reduction from pin AXI to AXO when amplifier muted	V_{AXI} = 10 mV (RMS); bit AXM = 1	–	80	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
LOUDSPEAKER CHANNEL (PINS LSAI1, LSAI2, LSAO, DLC AND LSPGND; BITS LSA1, LSA2, LSPD, VOL0, VOL1, VOL2 AND DLCI)						
Loudspeaker amplifier						
$\|Z_i\|$	input impedance between pins LSAI1 or LSAI2 and GND	bits LSA1 = 1, LSA2 = 1	–	20	–	kΩ
$G_{v(LSA)}$	voltage gain from LSAI1 or LSAI2 to LSAO for maximum volume	V_{LSAI} = 8 mV (RMS); bits LSA1 = 1, LSA2 = 1	26.5	28	29.5	dB
$\Delta G_{v(LSA)(f)}$	voltage gain variation with frequency referenced to 1 kHz	V_{LSAI} = 8 mV (RMS); f = 300 to 3400 Hz	–	±0.3	–	dB
$\Delta G_{v(LSA)(T)}$	voltage gain variation with temperature referenced to 25 °C	T_{amb} = −25 to +75 °C	–	±0.3	–	dB
$V_{LSAI(rms)}$	maximum input voltage between pins LSAI1 or LSAI2 and GND (RMS value)	V_{CC} = 5.0 V; $G_{v(LSA)}$ = 7 dB; for 2% of THD in input stage	–	500	–	mV
$V_{no(LSAO)(rms)}$	noise output voltage at pin LSAO (RMS value)	pin LSAI1 (with bits LSA1 = 1, LSA2 = 0) or pin LSAI2 (with bits LSA1 = 0, LSA2 = 1) connected to pin GND through 200 Ω in series with 10 µF; psophometrically weighted (P53 curve)	–	−80	–	dBVp
Output capability						
$V_{LSAO(p-p)}$	output voltage capability at pin LSAO (peak-to-peak value)	V_{CC} = 5.0 V; $G_{v(LSA)}$ = 28 dB; V_{LSAI} = 100 mV (RMS); R_L = 16 Ω	3.5	4.0	–	V
		V_{CC} = 3.3 V; $G_{v(LSA)}$ = 28 dB; V_{LSAI} = 100 mV (RMS); R_L = 8 Ω	–	2.4	–	V
$\|I_{LSAO(max)}\|$	maximum current capability at pin LSAO (peak value)		150	–	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Dynamic limiter						
t_{att}	attack time	V_{CC} = 3 V; $G_{v(LSA)}$ = 28 dB				
		when V_{LSAI} jumps from 20 mV (RMS) to 20 mV (RMS) + 10 dB; bit DLCI = 0	–	–	5	ms
		when V_{CC} drops below 2.7 V; bit DLCI = don't care	–	1	–	ms
t_{rel}	release time	V_{CC} = 3 V; $G_{v(LSA)}$ = 28 dB; when V_{LSAI} jumps from 20 mV (RMS) + 10 dB to 20 mV (RMS); bit DLCI = 0	–	250	–	ms
THD	total harmonic distortion at V_{LSAI} = 20 mV (RMS) + 10 dB	V_{CC} = 3 V; $G_{v(LSA)}$ = 28 dB; $t > t_{att}$	–	0.5	5	%
Volume control						
$\Delta G_{v(LSA)}$	voltage gain adjustment range	bits (VOL0, VOL1, VOL2)from (0, 0, 0) to (1, 1, 1)	–	21	–	dB
$\Delta G_{v(LSA)(s)}$	voltage gain adjustment step	VOL0 from 0 to 1	–	3	–	dB
Switches (pins SWI1, SWI2 and SWI3; bits SWC1, SWC2 and SWC3)						
$\lvert Z_{i(off)} \rvert$	AC impedance between pins SWIn and GND when not selected	bit SWCn = 0	50	–	–	kΩ
$\lvert Z_{i(on)} \rvert$	AC impedance between pins SWIn and GND when selected	2 mA < I_{SWIn} < 20 mA; bit SWCn = 1	–	–	30	Ω
Serial interface (pins DATA, CLK and EN)						
V_{IH}	HIGH-level input voltage		2.3	–	V_{CC} + 0.4	V
V_{IL}	LOW-level input voltage	V_{CC} = 3 to 5.5 V	GND – 0.4	–	0.3V_{CC}	V
I_{bias}	input bias current	input level = HIGH	0	1.5	3	µA
C_i	input capacitance at pins DATA, CLK and EN		–	tbf	–	pF

SERIAL BUS TIMING CHARACTERISTICS

V_{CC} = 3.3 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
Serial programming clock; pin CLK				
f_{clk}	clock frequency	0	300	kHz
Enable programming; pin EN				
t_{START}	delay to falling clock edge	tbf	–	µs
t_{END}	delay from last rising clock edge	tbf	–	µs
$t_{W(min)}$	minimum inactive pulse width	tbf	–	µs
$t_{SU;EN}$	enable set-up time to next clock edge	tbf	–	µs
Serial data; pin DATA				
$t_{SU;DATA}$	input data to clock set-up time	tbf	–	µs
$t_{HD;DATA}$	input data to clock hold time	tbf	–	µs

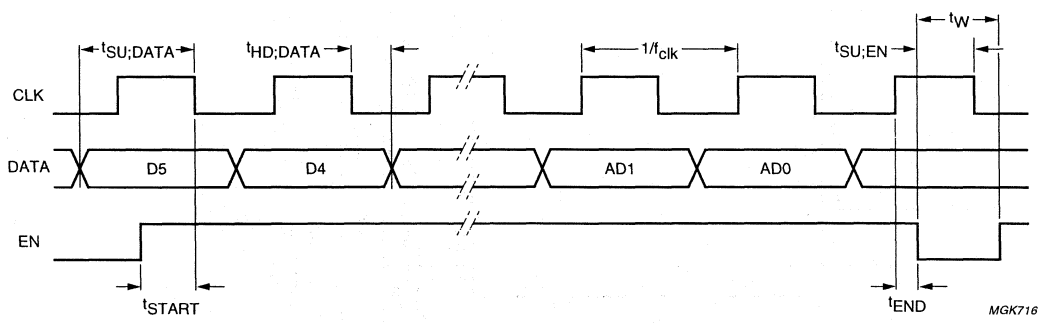


Fig.16 Serial bus timing diagram.

TEST AND APPLICATION INFORMATION

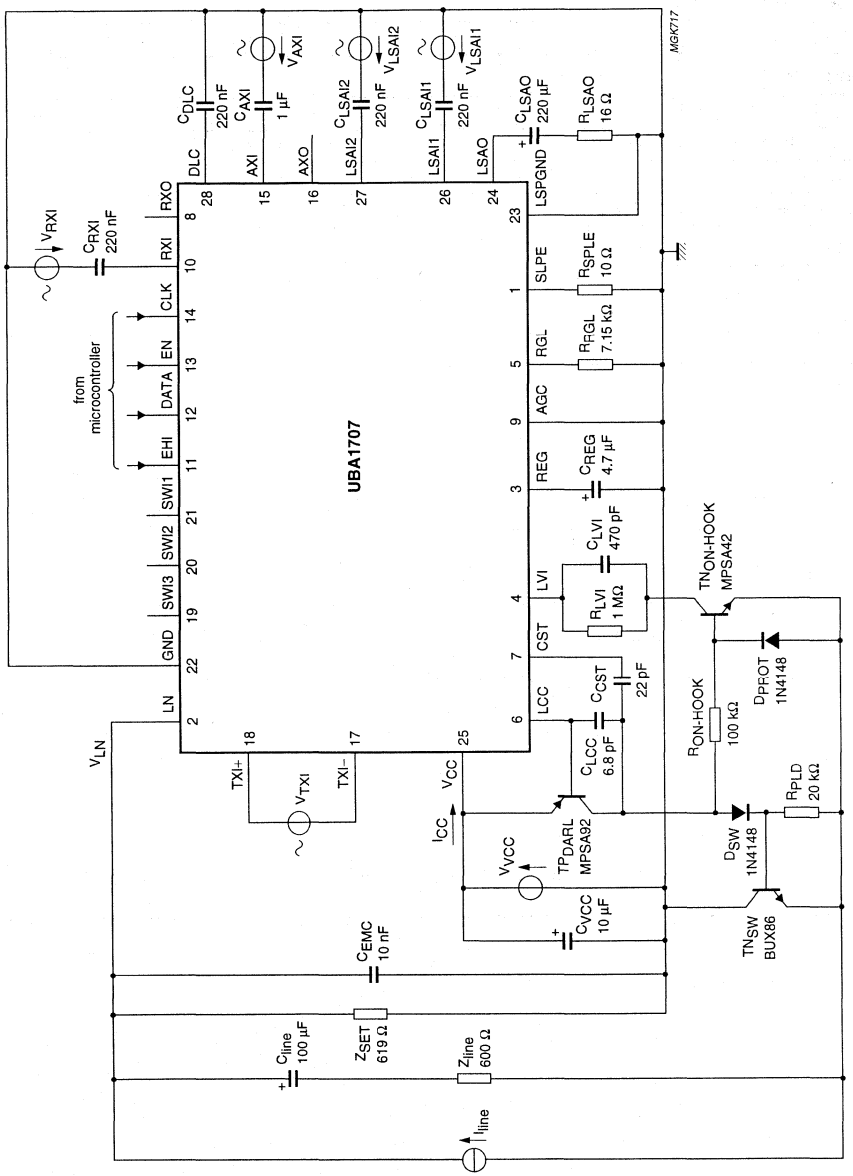


Fig.17 Test circuit.

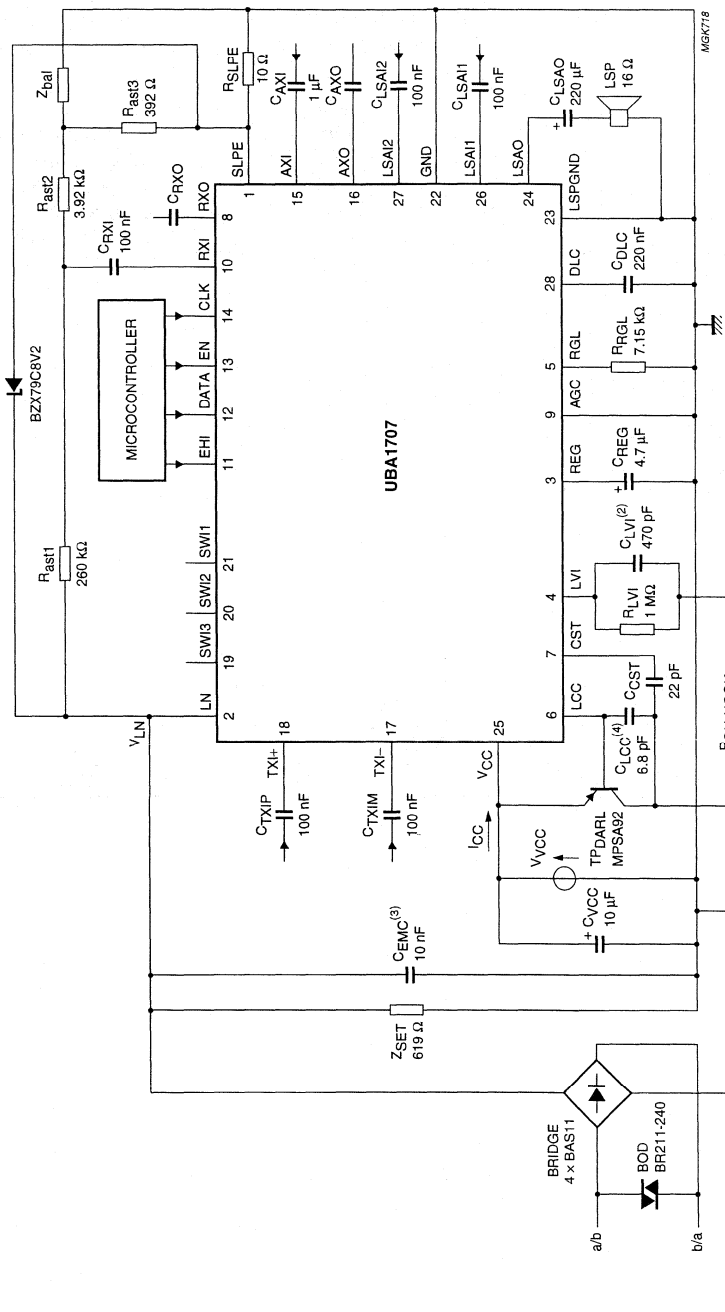


Fig.18 Typical application.

Modulator for GaAs power amplifiers UBA1710M

FEATURES

- Power MOS modulators for control of GaAs power amplifier drain voltage
- Power control loop amplifier and MOS driver
- Voltage tripler for supply of MOS driver
- Positive-to-negative DC converter for GaAs power amplifier gate biasing.

APPLICATIONS

- Control of GaAs power amplifiers for GSM and DCS hand-held transceivers.

GENERAL DESCRIPTION

The UBA1710M integrates the functions required to operate the GaAs Power Amplifiers (PAs) from the CGY20xx family which are intended for GSM and DCS applications.

It includes a negative supply for PA gate biasing and most of the functions required to implement power control so that only a very few external component are required. The power control section integrates two power MOS devices for control of the PA drain voltages, an MOS driver and a feedback loop amplifier. The MOS driver is supplied from an on-chip voltage tripler.

QUICK REFERENCE DATA

SYMBOL	PARAMETER[1]	MIN.	TYP.	MAX.	UNIT
V_{CC}	analog supply voltage	4.2	4.8	7.5	V
V_{DD}	digital supply voltage	4.2	4.8	7.5	V
$I_{CC} + I_{DD}$	peak supply current in power-up mode	–	12	–	mA
T_{amb}	operating ambient temperature	–20	–	+85	°C

Note

1. For conditions, see Chapter "Characteristics".

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UBA1710M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

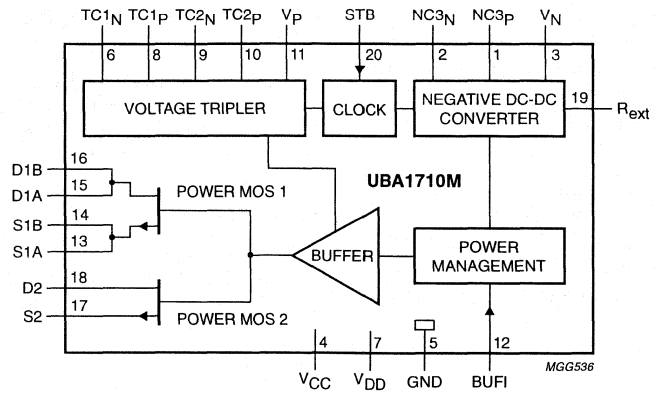


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$NC3_P$	1	charge pump tank capacitor
$NC3_N$	2	charge pump tank capacitor
V_N	3	negative bias voltage
V_{CC}	4	analog supply voltage
GND	5	ground
$TC1_N$	6	charge pump tank capacitor
V_{DD}	7	digital supply voltage
$TC1_P$	8	charge pump tank capacitor
$TC2_N$	9	charge pump tank capacitor
$TC2_P$	10	charge pump tank capacitor
V_P	11	positive tripler voltage
BUFI	12	buffer input
S1A	13	power MOS 1 source A
S1B	14	power MOS 1 source B
D1A	15	power MOS 1 drain A
D1B	16	power MOS 1 drain B
S2	17	power MOS 2 source
D2	18	power MOS 2 drain
R_{ext}	19	external resistance for V_N
STB	20	standby input (active HIGH)

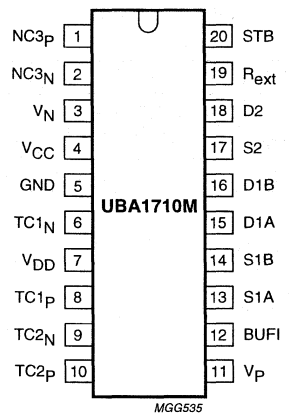


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Power control section

Power control for GaAs PAs from the CGY20xx family is achieved by varying the drain voltage. This is achieved with the UBA1710M by means of the two power MOS devices integrated on-chip. They enable separate control of the PA output stage from the pre-amplifier stages. They have a very low 'on' resistance for low drop voltage at high RF output power.

The MOS devices are driven by a buffer. The buffer amplifier, in association with power MOS, is included in a feedback loop to exhibit a high cut-off frequency (3 MHz) over the whole control dynamic range. This buffer allows fast switching of the MOS in accordance with GSM power ramping requirements.

DC-DC converters

One DC-DC converter is required to provide negative gate biasing to the GaAs PA.

The standard value is typically –2 V, without any external resistor connected. The other one is a voltage tripler and is required to supply the MOS driver. The driver is required to raise the MOS gate voltage well above the battery voltage in order to open the MOS switches ('high side' driver).

These DC-DC converters are operated at a typical frequency of 600 kHz supplied by an internal oscillator. Five external capacitors with a typical value of 0.1 µF (0603 SMD) are required to operate these converters.

Power management

The power management disables the PA drain voltage and prevents the PA from burnout if drain voltage is supplied before the negative gate voltage is available.

Standby mode

An additional feature includes a standby mode, reducing the current consumption to a maximum value of 1 µA.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); general operating conditions applied.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	analog supply voltage	–0.5	+9.0	V
V_{DD}	digital supply voltage	–0.5	+9.0	V
V_I	DC input voltage			
	all pins (except BUFI)	–0.5	+9.0	V
	pin BUFI	–0.5	+5.0	V
I_I	DC current into any signal pin	–10	+10	mA
P_{tot}	total power dissipation	–	0.65	W
T_{stg}	storage temperature	–65	+150	°C
T_{amb}	operating ambient temperature	–20	+85	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	100	K/W

CHARACTERISTICS

$V_{CC} = V_{DD} = 4.8$ V; $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
$I_{CC} + I_{DD}$	peak supply current	power-up mode; PA on	–	12	–	mA
		power-down mode; PA off	–	5	–	mA
I_{stb}	standby current	standby mode	–	0.1	1	µA
Power MOS 1						
R_{DSon1}	on resistance	$I_{DS} = 1.3$ A	–	0.18	–	Ω
Power MOS 2						
R_{DSon2}	on resistance	$I_{DS} = 0.4$ A	–	0.5	–	Ω
Clock circuit						
f_{clk}	clock frequency		–	600	–	kHz
Voltage tripler						
V_{Po}	output voltage	with $I_{Po} = 2$ mA	11.3	11.8	12.3	V
$V_{R(p-p)}$	amplitude ripple (peak-to-peak value)	with $I_{Po} = 2$ mA; C1 = C2 = 100 nF; $C_P = 100$ nF	–	20	–	mV
t_{on}	turn-on time		–	100	–	µs
Negative DC/DC converter						
V_{No}	output voltage	with $I_{No} = 250$ µA; $R_{ext} = 470$ kΩ	–1.5	–1.8	–2.0	V
$V_{R(p-p)}$	amplitude ripple (peak-to-peak value)	with $I_{No} = 250$ µA; C3 = 100 nF; $C_N = 100$ nF	–	2	–	mV
t_{on}	turn-on time		–	280	–	µs
MOS buffer amplifier						
V_{IL}	LOW level input voltage		–	1.2	–	V
V_{IH}	HIGH level input voltage		–	3.4	–	V
t_{sw}	switching time from 0 to 4.5 V	2 Ω load at MOS outputs	–	1	–	µs

APPLICATION INFORMATION

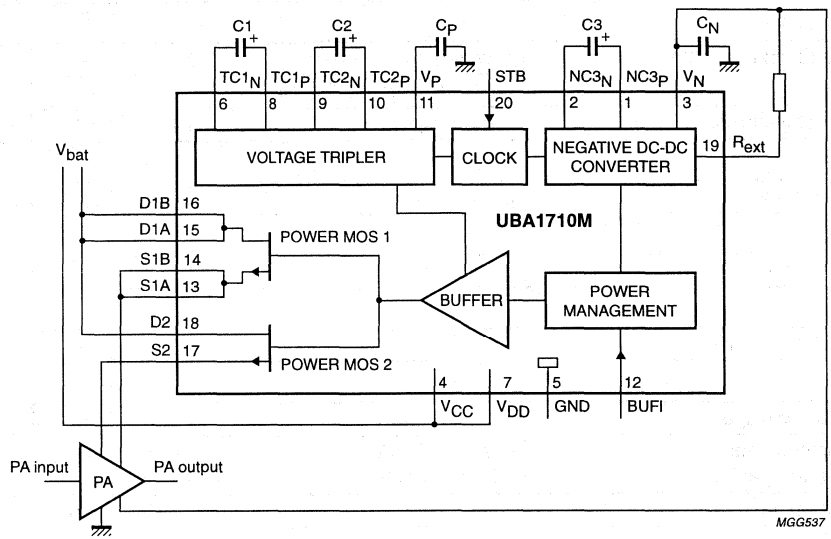


Fig.3 Application diagram.

Data processor for cellular radio (DPROC2)

UMA1002

FEATURES

- Single chip solution to all the data handling and supervisory functions
- Configuration to both AMPS and TACS
- Additional JTACS option
- I²C-bus serial control
- All analog interface and filtering functions fully implemented on chip
- Error handling in hardware reduces software requirements
- Robust SAT decoding and transponding circuitry
- Low current consumption by on-chip power-down modes
- Reduced system current consumption by new integrated power-saving features
  - Majority voting includes more intelligence
  - On-chip control filler word filter
  - BCH error filter
  - Possibility to program ESCC bits
- Small physical size: SO28 or LQFP32
- External peripheral component count reduced
  - On-chip selectable clock divider
  - Integrated pull-up resistor at TXLINE
- Simplified reset and abort software routines possible
- The SO28 version is fully compatible with UMA1000LT and UMF1000T.

GENERAL DESCRIPTION

The UMA1002 is a low power CMOS LSI device incorporating the data transceiving, data processing, and SAT functions (including on-chip filtering) for an AMPS or TACS hand-held portable cellular radio telephone.

In this data sheet, the UMA1002 is often referred to by the descriptive term 'DPROC2'.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	2.7	3.0	5.5	V
I_{DD}	supply current normal operation with external clock	–	1.3	1.8	mA
T_{amb}	operating ambient temperature	−30	–	+70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UMA1002T	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
UMA1002H	LQFP32	plastic low profile quad flat package; 32 leads; body 7 × 7 × 1.4 mm	SOT358-1

BLOCK DIAGRAM

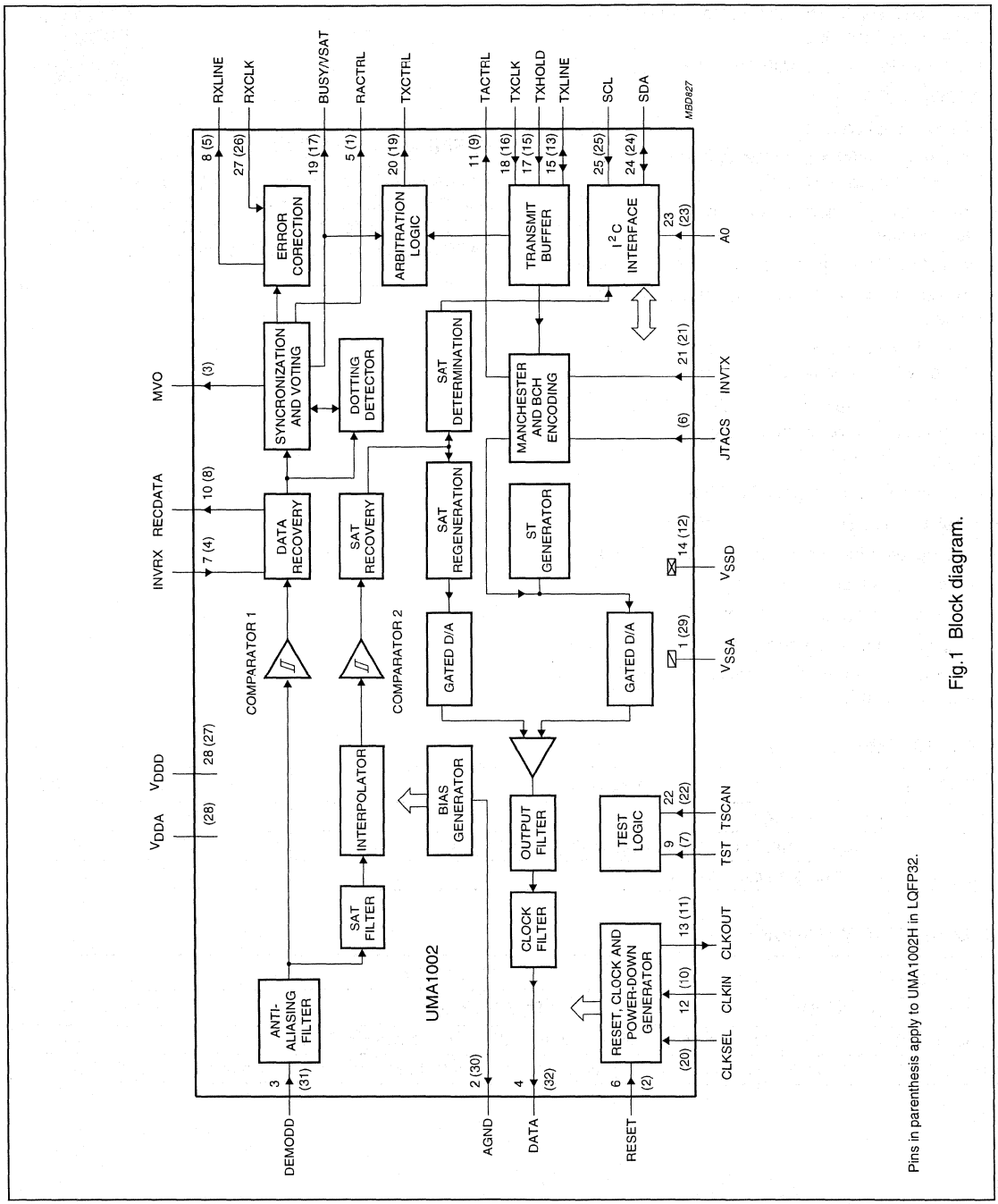


Fig.1 Block diagram.

Pins in parenthesis apply to UMA1002H in LQFP32.

PINNING

SYMBOL	PIN		DESCRIPTION
	SO28	LQFP32	
V_{SSA}	1	29	Negative analog supply (0 V). To be connected low-ohmic to V_{SSD}.
AGND	2	30	Internally generated analog signal ground. Voltage level = $\frac{1}{2}V_{DDA}$. This pin should be connected to a blocking capacitor, no DC load allowed.
DEMODD	3	31	DEMODD inputs analog data and SAT signals from the RF demodulator. This pin should normally be AC-coupled. See Chapter "AC characteristics".
DATA	4	32	Data is an analog output which provides the Manchester encoded and filtered data signal, SAT and signalling tone. This signal should normally be AC-coupled into the Audio/Data summer. See Chapter "AC characteristics".
RACTRL	5	1	Received audio control output. Open-drain output used to blank the audio path to the earpiece when a sequence of dotting followed by a synchronization word or 2 synchronization words separated by 77 bits is detected. RACTRL and TACTRL functions can be combined using one line. Output level LOW means audio muted.
RESET	6	2	Master reset input resetting all internal flip-flops to the specified state. This input has no influence on analog parts, but must be controlled by an active HIGH microcontroller port.
INVRX	7	4	This input inverts the sense of received data stream, which allows RF demodulators with high or low local oscillators to be used. The AMPS and TACS specifications define NRZ encoded logic 1 as a LOW-to-HIGH transition in the centre of a data bit period. The polarity of the demodulated data stream into DPROC2 depends on the receiver local oscillator. Input LOW means data normal.
RXLINE	8	5	Received data signal output to the system controller.
TST	9	7	Test input pin (note 1).
RECDATA	10	8	Output of the recovered digital data signal (note 1).
TACTRL	11	9	Transmitter audio control output. This open-drain output is used to blank the audio path and enable the data path to the modulator during data bursts on the RVC. Output level LOW means audio muted.
CLKIN	12	10	1.2 MHz or 9.6 MHz external master clock input. This input signal should be accurate to 100×10^{-6} and have a worst case 60 : 40 mark-space ratio.
CLKOUT	13	11	Output of 1.2 MHz clock signal (for APROC) derived from CLKIN.
V_{SSD}	14	12	Negative digital supply (0 V), internally connected to substrate. To be connected low-ohmic to V_{SSA}.
TXLINE	15	13	Open-drain bidirectional data line to the system controller (internal 100 kΩ pull-up).
n.c.	16	14	Not connected.
TXHOLD	17	15	This input holds off transmission of data when set to HIGH.
TXCLK	18	16	Transmitted data clock input from the system controller.
BUSY/VSAT	19	17	Output indicating the status of the RECC by providing output information based on a majority decision on the last 3 consecutive Busy/Idle bits (FVC = logic 0). Output level LOW means channel idle. Indicating the result of the comparison of the measured SAT and the expected SAT colour-code bits (I^2C-bus register) in the voice channel mode (FVC = logic 1 and ENSM = logic 1). Output level LOW means incoming SAT not equal to expected SAT.

SYMBOL	PIN		DESCRIPTION
	SO28	LQFP32	
TXCTRL	20	19	Transmitter control open-drain output used to disable the transmitter during an RECC access failure. Output level LOW means RF disabled.
INVTX	21	21	This input inverts the sense of transmitted data stream, which allows RF modulators with high or low local oscillators to be used. The AMPS and TACS specifications define NRZ encoded logic 1 as a LOW-to-HIGH transition in the centre of a data bit period. The polarity of the modulated data stream depends on the transmitter local oscillator. Input LOW means data inverted.
TSCAN	22	22	Test switch input, only enabled if TST = logic 1, but should have a defined state.
A0	23	23	Input to select the least significant bit of the I^2C-bus address.
SDA	24	24	Serial data input/output (I^2C-bus).
SCL	25	25	Serial clock input (I^2C-bus).
n.c.	26	18	Not connected.
RXCLK	27	26	Received data clock input from the system controller.
V_{DDD}	28	27	Digital supply voltage (+3 V).
V_{DDA}	–	28	Analog supply voltage (+3 V).
MVO	–	3	Majority voting output indicating that on FOCC the first 3 received words do not differ from each other and thus the majority decision over 5 words can already be carried out. Because of the required speed, indication is at this pin (and not via the I^2C-bus) which can be monitored by the system controller. Output LOW means the receiver can be switched off.
JTACS	–	6	Digital input signal for JTACS, input HIGH means that data is routed from TXLINE directly without processing to gated D/A converter (if enabled by STEN bit).
CLKSEL	–	20	Input switch for internal divide-by-8 or divide-by-1 divider between CLKIN and CLKOUT (internal pull-down → divide-by-1 is default if not bonded out in SO28 package).

Note

1. Must not be connected in existing applications.

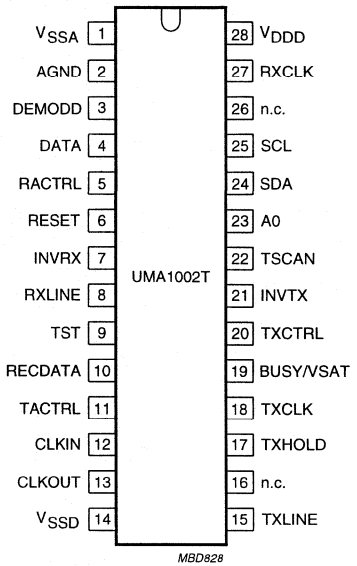


Fig.2 Pin configuration for SO28, SOT136-1.

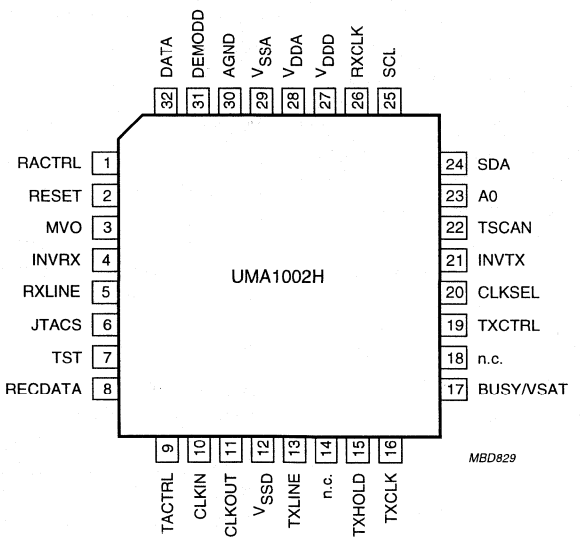


Fig.3 Pin configuration for LQFP32, SOT358-1.

FUNCTIONAL DESCRIPTION

General

The UMA1002 (DPROC2) is a single-chip CMOS device which handles the data and supervisory functions of an AMPS or TACS subscriber set.

These functions are:

- Data reception and transmission
- Control and voice channel exchanges
- Error detection, correction, decoding and encoding
- Supervisory Audio Tone decoding and transponding
- Signalling Tone generation.

In an AMPS or TACS cellular telephone system, mobile stations communicate with a base over full duplex RF channels. A call is initially set up using one out of a number of dedicated control channels. This establishes a duplex voice connection using a pair of voice channels.
Any further transmission of control data occurs on these voice channels by briefly blanking the audio and simultaneously transmitting the data. The data burst is brief and barely noticeable by the user. A data rate of 10 kbits/s is used in the AMPS system and 8 kbits/s in TACS. The signalling formats for both Forward Channels (base to mobile) and Reverse Channels (mobile to base) are shown in Fig.14.

A function known as Supervisory Audio Tone (SAT), a set of 3 audio tones (5970, 6000 and 6030 Hz), is used to indicate the presence of the mobile on the designated voice channel. This signal, which is analogous to the On-Hook signal on land lines, is sent out to the mobile by the base station on the Forward Voice Channel. The signal must be accurately recovered and transponded back to the base station to complete the 'loop'. At the base station this signal is used to ascertain the overall quality of the communication link.

Another voice channel associated signal is Signalling Tone (ST). This tone (8 kHz TACS, 10 kHz AMPS) is generated by the mobile and is sent in conjunction with SAT on the Reverse Voice Channel to serve as an acknowledgement signal to a number of system orders.

The key requirements of a hand-held portable cellular set are:

- Small physical size
- Minimum number of interconnections (serial bus)
- Low power consumption
- Low cost.

The DPROC2 is a member of our Cellular Radio chip set, based on the I^2C-bus, which meets these requirements. A cellular radio system schematic using the chip set is shown in Fig.11.

DPROC2 power-saving features

To support current saving in the application, DPROC2 has three different modes of circuit operation implemented. They are decoded by the I^2C-bus register bit FVC and by activity on the data transfer link (TXCLK and TXLINE). In power-down mode the relevant digital circuits have the clock disabled, the analog circuits have the bias currents and the switched capacitor clock switched off.

- Normal mode: all circuit parts are operating (e.g. on Voice channels)
- Power-down mode 1: the SAT path is in power-down (e.g. during access of the RECC)
- Power-down mode 2: the SAT path and the total data transmit path are in power-down (e.g. for Idle state, DPROC2 operating only on FOCC).

System power-saving features

Besides the above mentioned power-down modes DPROC2 also includes features to reduce system current (e.g. switching off parts of the receiver, and put the system controller into Idle mode for longer periods of time).
All these features are controlled by the I^2C-bus. For further explanation of the following features refer to the Section "I2C-bus serial data link (SDA; SCL)" sub-section "I2C-bus registers".

MAJORITY VOTING (ONLY IN LQFP32)

Majority voting includes more intelligence. This feature is enabled in FOCC with I^2C-bus bit MAJ = logic 1.
If 3 consecutive identical words have been received it is signalled via pin MVO. Therefore during the last 2 frame words the receiver could be switched off to save system current consumption.

CONTROL FILLER WORDS FILTER

System current can be further reduced by an on-chip control filler words filter in FOCC, which enables the detection of consecutive identical control filler words.
If consecutive control filler words are identical (i.e. DCC, CMAC and WFOM) they will not be passed on to the microcontroller. Consequently the system controller can remain in power-saving mode.

PROGRAMMING OF ESCC BITS

There is a possibility to program the expected ESCC bits, so that DPROC2 can compare expected and received SAT and signal any inconsistency to the system controller via BUSY/VSAT pin. Consequently there is no need to read the measured SAT periodically via the I²C-bus.

BCH ERROR FILTER

If this feature is enabled, DPROC2 will not pass on to the microcontroller words with BCH errors. Consequently the microcontroller can remain in power-saving mode. This feature in combination with the control filler feature is defined in Table 8.

SELECTABLE CLOCK DIVIDER (ONLY IN LQFP32)

An on-chip selectable divide-by-8 clock divider reduces external peripheral component count.

Power-up state and master reset (RESET)

RESET should be HIGH as soon as power supply is available.

DPROC2 will not respond reliably to any inputs (including RESET) until 100 µs after the power supply has settled within the specified tolerance. The analog sections of the device will have stabilized within 5 ms. No on-chip power-on reset is provided, therefore before the device can enter normal operation RESET must be held HIGH.

RESET is an active HIGH master reset input, with a minimum active pulse width of 4 µs which may be used to reset the total logic within DPROC2 to a predefined state as illustrated in Tables 1 and 2. It is preferably only used during power-up, during normal operation it is recommended to use the fully synchronous reset signals derived from the I²C-bus bits FVC, STS and TXRST (see Table 4). To ensure correct operation TXCLK must be held HIGH during RESET operation.

Table 1 Predefined state of the digital output pins

OUTPUT	STATE
RXLINE	HIGH
TXCTRL	high-impedance (HIGH)
TACTRL	high-impedance (HIGH)
RACTRL	high-impedance (HIGH)
BUSY/VSAT	HIGH
TXLINE	HIGH (by 100 kΩ internal pull-up resistor)
RECDATA	LOW
MVO	HIGH
SDA	high-impedance (HIGH)

Table 2 Predefined state of the I²C-bus registers

REGISTER	BIT							
	7	6	5	4	3	2	1	0
Status (read)	LOW	LOW	LOW	HIGH	LOW	LOW	HIGH	HIGH
Control 1 (write)	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
Control 2 (write)	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW

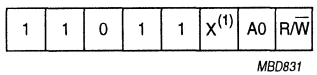
I²C-bus serial data link (SDA; SCL)

SDA is the bidirectional data line, SCL is the clock input from an I²C-bus master. These constitute a typical I²C link and conform to standard I²C-bus characteristics.
A detailed description of the I²C-bus specification, with applications, is given in the brochure *"The I²C-bus and how to use it"*. This brochure may be ordered using the code 9398 393 40011.

- Data rate up to 100 kbits/s.

SLAVE ADDRESS SELECT (A0)

Selection of the device slave address is achieved by connecting A0 to either V_{SS} or V_{DDD}. The slave address is defined in accordance with the I²C-bus specifications as shown in Fig.4.



(1) X = don't care.

Fig.4 Device slave address.

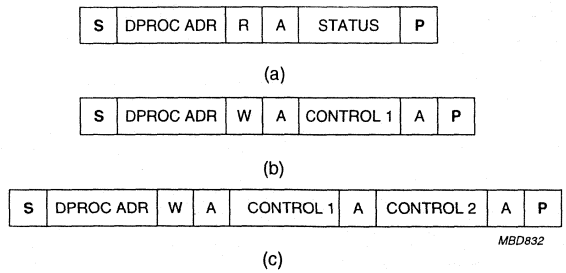
I²C-BUS REGISTERS

The I²C-bus register block resides internally within the I²C-bus interface block and contains various items of status and control information which are transferred to and from DPROC2 via the I²C-bus. The block is organized into three 8-bit registers:

- Status register which contains read only items
- Control registers 1 and 2 which contain write only items.

Table 3 I²C-bus register map

REGISTER	BIT							
	7	6	5	4	3	2	1	0
Status (read)	–	–	WSYNC	BUSY	TXABRT	TXIP	MSCC1	MSCC0
Control 1 (write)	BUFEN	SERV	STS	TXRST	ABREN	FVC	STEN	SATEN
Control 2 (write)	MAJ	MR1	MR0	DBCH	DCFM	ENSM	ESCC1	ESCC0



(a) Read from DPROC2 status register.
(b) Write to DPROC2 control register 1.
(c) Write to all DPROC2 control registers.

Where:
S = START condition
W = read/write bit (logic 0 = write)
R = read/write bit (logic 1 = read)
A = acknowledge bit
P = STOP condition
DPROC ADR = slave address of DPROC2.

Fig.5 I^2C-bus data format.

Table 4 Description of I²C-bus register map

REGISTER BITS	LOGIC LEVEL	DESCRIPTION
Control Register 1		
BUFEN	0	1.2 MHz signal not available at pin CLKOUT
	1	1.2 MHz signal is available at pin CLKOUT
SERV	0	serving system data stream B selected
	1	serving system data stream A selected
STS(1)	0	TACS selected
	1	AMPS selected
TXRST	1	terminates a message being transmitted on the reverse channel; monostable signal causing a reset of the message transmission circuitry and resets the I²C-bus bits TXABRT, TXIP and clears the transmit buffer
ABREN	1	DPROC2 has permission to abort data transmission and disable RF on the RECC following the detection of a channel access attempt collision
	0	no permission for above operations
FVC(2)	0	control channel format selected
	1	voice channel format selected
STEN	0	disables output of signalling tone to pin DATA
	1	enables output of signalling tone to pin DATA if FVC = logic 1
SATEN	0	disables output of SAT transponded signal to pin DATA
	1	enables output of SAT transponded signal to pin DATA if FVC = logic 1
Control Register 2		
MAJ	0	majority voting procedure on FOCC using all 5 frame words, MVO output is always HIGH
	1	majority voting procedure on FOCC using the first 3 frame words, if they are all identical the MVO pin goes LOW (see Fig.6)
MR0, MR1	see Table 5	determines set-up time of MVO signal with respect to beginning of the next dotting (see Fig.6)
DBCH	see Table 8	BCH error filter
DCFM	see Table 8	control filler message filter
ENSM	0	enable SAT monitoring; ESCC bits are not used
	1	enable SAT monitoring; ESCC bits are used for following function
ESCC0, ESCC1	see Table 6	expected SAT colour code bits; the incoming SAT is compared to these bits, the result (expected or not expected SAT frequency) is given out by the BUSY/VSAT pin (when FVC = logic 1), which prevents periodical reading from the I²C-bus status register
Status Register		
WSYNC	0	DPROC2 has not acquired frame synchronization in accordance with FOCC format
	1	DPROC2 has acquired frame synchronization in accordance with FOCC format

REGISTER BITS	LOGIC LEVEL	DESCRIPTION
BUSY		indicates the status of RECC, determined by a majority decision on the result of the last 3 consecutive Busy/Idle bits of the FOCC and is also routed to pin BUSY/VSAT
	0	channel idle
	1	channel busy
		indicates the result of the comparison of the incoming SAT and the stored SAT Colour Code bits in the Voice Channel mode and is also routed to pin BUSY/VSAT
	0	incoming SAT not equal to expected SAT
	1	incoming SAT equal to expected SAT
TXABRT		indicates that a RECC access attempt has been aborted without successful message transmission
	0	no access collision detected
	1	transmission attempt aborted
TXIP	0	no transmission on RECC or RVC in progress
	1	data transmission by DPROC2 on RECC or RVC in progress
MSCC1, MSCC0	see Table 7	provides information about the current measured SAT colour code

Notes

1. Changing this register bit resets internally the receive and transmit logic circuitry.
2. Changing this register bit resets internally the receive logic circuitry.

Table 5 Set-up time of MVO signal

MR0	MR1	t_{MVO} (ms)
0	0	3
0	1	6
1	0	9
1	1	12

Table 6 Expected SAT colour code

ESCC1	ESCC0	SAT FREQUENCY (Hz)
0	0	5970
0	1	6000
1	0	6030
1	1	no valid SAT

Table 7 Measured SAT colour code

MSCC1	MSCC0	SAT FREQUENCY (Hz)
0	0	5970
0	1	6000
1	0	6030
1	1	no valid SAT

Table 8 Conditions for transmission of received words to system controller

DBCH	DCFM	BCH ERROR BIT	CHANGE IN CONTROL FILLER WORD DETECTED	TRANSMISSION OF CONTROL FILLER WORD TO SYSTEM CONTROLLER
0	0	X	X	yes
0	1	0	0	no
0	1	0	1	yes
0	1	1	X	yes
1	0	0	X	yes
1	0	1	X	no
1	1	0	0	no
1	1	0	1	yes
1	1	1	X	no

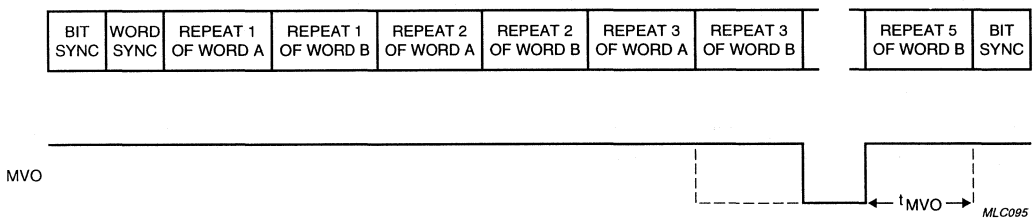


Fig.6 Timing of MVO output.

Digital circuit blocks

General

The majority of the digital circuitry within the DPROC2 device is identical for both AMPS and TACS. The interconnections of the digital blocks discussed below are shown in Fig.1.

Data Recovery

The Data Recovery Block receives wideband Manchester encoded data in sampled and sliced form from the Comparator Block, on which it performs the following functions:

- Clock recovery
- Manchester decoding
- Data regeneration.

The Clock Recovery Block extracts an 8 or 10 kHz (TACS or AMPS) phase-locked clock signal from the Manchester encoded data stream. This is implemented using a digital-phase-locked-loop (PLL) which has an adjustable 'bandwidth' to provide both fast acquisition and low jitter.

Manchester decoding is performed by exclusive ORing the recovered Manchester encoded data with the recovered clock.

The NRZ data regeneration is performed by a digital integrate and dump circuit. This consists of an up/down counter that counts 1.2 MHz cycles during the data period. The sense of the count is determined by the result of the Manchester Decoder output. The number of counts is sampled at the end of a data period. If this number exceeds a threshold the data is latched as a logic 1 otherwise it is latched as a logic 0.

SAT recovery

The SAT Recovery Block receives a filtered and sliced SAT signal which must be recovered before being routed to the Determination and Regeneration Blocks.

The recovery is performed using a digital phase-locked loop.

SAT determination

The SAT Determination Block indicates which, if any, of the valid SAT tones is detected from the recovered SAT. The AMPS and TACS specifications require that a determination is made at least every 250 ms. Determination involves counting the number of cycles of the regenerated SAT in this time period. This count is then compared to a set of four known counts which define the boundaries between the SAT frequencies and SAT-not-valid events. The result is then coded into the I^2C status registers MSCC0 and MSCC1.

SAT regeneration

The SAT Regeneration Block generates a digital SAT stream for transponding back to the base station. The transponded SAT is phase-locked to the recovered SAT by means of a second digital phase-locked-loop. To minimize the total harmonic distortion of the output signal the transponded SAT is then processed by a delta modulator before being passed on to the Gated Digital-to-Analog (D/A) converter.

Dotting Detector

The Dotting Detector Block determines whether a data inversion (dotting) pattern has been received on the Forward Voice Channel. The detection of data inversion indicates that the Clock Recovery Block has acquired bit synchronization and that the narrow bandwidth mode on the clock recovery phase-locked-loop is selected. This signal is also used to indicate that a data burst is expected and activates the audio mute RACTRL, after a Word Synchronization Block has been received, for the duration of the burst.

Word Synchronization Detector

The Word Synchronization Block performs the following functions:

- Frame Synchronization
- Reverse Control Channel status (B/I determination)
- Valid Serving System determination.

These functions are associated solely with the Forward Control Channel and have no meaning on the Forward Voice Channel.

Information in a data stream is identified by its position with respect to a unique synchronization word.
This synchronization word is an 11-bit Barker code which has a low probability of simulation in an error environment, and can be easily detected. Data received is only considered valid at times when DPROC2 has achieved frame synchronization.

In this condition the block leaves its search mode and enters its lock mode. This is indicated by bit WSYNC being set HIGH. In order to achieve this two consecutive synchronization words separated by 463 bits must be detected. Once in lock mode, the synchronization word detector is examined every 463 bits and only loses frame synchronization after 5 consecutive unsuccessful attempts at detecting the synchronization word have been made. At this point bit WSYNC is cleared and the device is returned to its search mode.

Information detailing the status of the Reverse Control Channel is given by the Busy/Idle bits. These occur at intervals of 11 bits within the frame, the first occurring immediately following the synchronization word.
The status of the channel is determined by a majority decision on the last three consecutive Busy/Idle bits.

FVC: After detection of 2 consecutive sync words the circuit leaves its Search Mode and enters the Lock Mode. The data word in between is considered as valid and already stored for Majority Voting. Whenever a sync word was found the incoming data stream is examined 88 bits later for sync again. Whenever a valid sync word is detected the following data word is given to the Majority Voting block. After missing two consecutive sync words the circuit goes back to the search mode (scanning for sync every bit). If a sync word is then detected again, the following data word is immediately accepted (and not only after two correctly timed sync words). The detection process of sync words is independent of the detection of dotting. The audio mute via pin RACTRL is activated either by receiving a sync word after detection of a dotting sequence or by entering Lock Mode.

Majority Voting Block

The Majority Voting Block performs the following functions:

- Identifying position and validity of frames in the received data stream
- Extracting five repeats of each word from a valid frame
- Performing a bit-wise majority decision on the five repeats of the data word.

The validity of the frames is determined by setting a counter in operation which times out and resets the circuitry after 920 or 463 bit periods from detecting valid word synchronization. The time out period selected depends on whether DPROC2 is monitoring the Forward Voice or Control Channel respectively.

Up to five repeats of the message word are searched for and extracted by DPROC2. On the Forward Voice Channel the extraction of a data word for majority voting is described in the Section "Word Synchronization Detector".

DPROC2 enables two mechanisms for Majority Voting. The first is based on 5 words and is described above. The other mechanism is based on 3 consecutive identical words and thus enabling switch-off of parts of the receiver during reception of the remaining two words (see Table 5 and Fig.6).

Error Correction Block

The Error Correction Block performs:

- Extraction of a valid message from the Majority-Voted Word
- Computation of the S1 and S3 syndromes
- Correction of up to one error in the word
- Communication of received data to the System Controller via the Received Data Serial Link.

Interpretation of parity of a received word is obtained from knowledge of the syndromes of the word. The syndromes are calculated using feedback shift registers with two characteristic polynomials:

$1 + x + x^6$ and $1 + x + x^2 + x^4 + x^6$

Once the syndromes of a received word are known, it is possible to determine if a correctable error is present. DPROC2 only corrects up to one error although the code used has a Hamming distance of five. The occurrence of two or more errors is signalled by setting the BCH error flag, which is communicated to the System Controller via the Received Data Serial Link.

Received Data Serial Link

The Received Data Serial Link transfers data and control information from DPROC2 to the System Controller. The data is transferred on RXLINE under control of a clock signal RXCLK, generated by the System Controller. The system controller is informed of the arrival of a decoded data word in the DPROC2 output register by RXLINE being driven LOW. If the system controller chooses to ignore the received data or only partially clock the data out, the DPROC2 will reset the receive buffer for the next word after the period RWIN (see Fig.8).

Data format

Each Received Data word consists of 4 bytes. The word format is shown in Fig.7(a). The sense and function of the fields is shown in Table 9.

Link protocol

The Received Data protocol is described by the timing diagram Fig.8(a) and has the following parameters:

- Maximum receive window (RWIN)
  - Control Channel (TACS) = 47 ms; MAJ = 0
  - Control Channel (TACS) = 30.5 ms; MAJ = 1 (in FOCC only)
  - Control Channel (AMPS) = 37 ms; MAJ = 0
  - Control Channel (AMPS) = 23.8 ms; MAJ = 1 (in FOCC only)
- Minimum clock period (t_{CLKmin}) = 2 µs
- Minimum clock hold-off (t_{WAIT}) = 2 µs.

Transmit Data Serial Interface

The Transmit Data Serial Link performs reception of data from the System Controller to DPROC2 over a dedicated line TXLINE. The transfer of data is synchronous with a clock signal TXCLK, generated by the System Controller.

Data format

Each Transmit Data word consists of 5 bytes. The word format is shown in Fig.7(b). The sense and function of the fields is shown in Table 10.

Link protocol

Messages are normally up to 5 words in length on the Reverse Control Channel and up to 2 words in length on the Reverse Voice Channel. However, DPROC2 will transmit messages of any word length. These must be transmitted on the data stream without interruption. To avoid the need for large buffer areas, a flexible protocol is used to allow DPROC2 to control the transfer of data words. DPROC2 has an on-chip buffer which can hold one complete word of a message. While new words are being loaded into DPROC2, within the time period Buffer clear to end of TWIN, DPROC2 will maintain uninterrupted data transmission. The System Controller can abort the transmission of a message at any point activating the I^2C-bus signal TXRST. This signal causes the interface to return to its power-up state and resets TXIP and TXABRT (see Table 4). On completion of these tasks TXRST will return to its inactive state. The Transmit Data Protocol is described by the timing diagram shown in Fig.8(b) and has the following parameters:

- Maximum transmit window (TWIN)
  - voice channel (TACS) = 60 ms
  - voice channel (AMPS) = 48 ms
  - control channel (TACS) = 29 ms
  - control channel (AMPS) = 23 ms
- Minimum clock period (t_{CLKmin}) = 2 µs
- Minimum wait period (t_{WAIT}) = 2 µs.

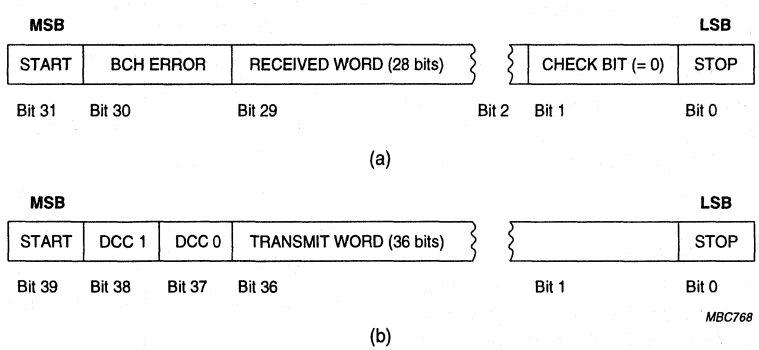
Note that TXRST will clear the transmit buffer.

Table 9 Received data word

BIT	TITLE	SENSE	FUNCTION
31	start	LOW	identifies start of word
30	BCH error	active HIGH	indicates that an uncorrected BCH error is associated with the word
29 to 2	received data	binary data	received data word
1	RXLINE error	active HIGH	indicates that a transmission error has occurred on the microprocessor to DPROC2 serial link
0	stop	HIGH	identifies end of the word

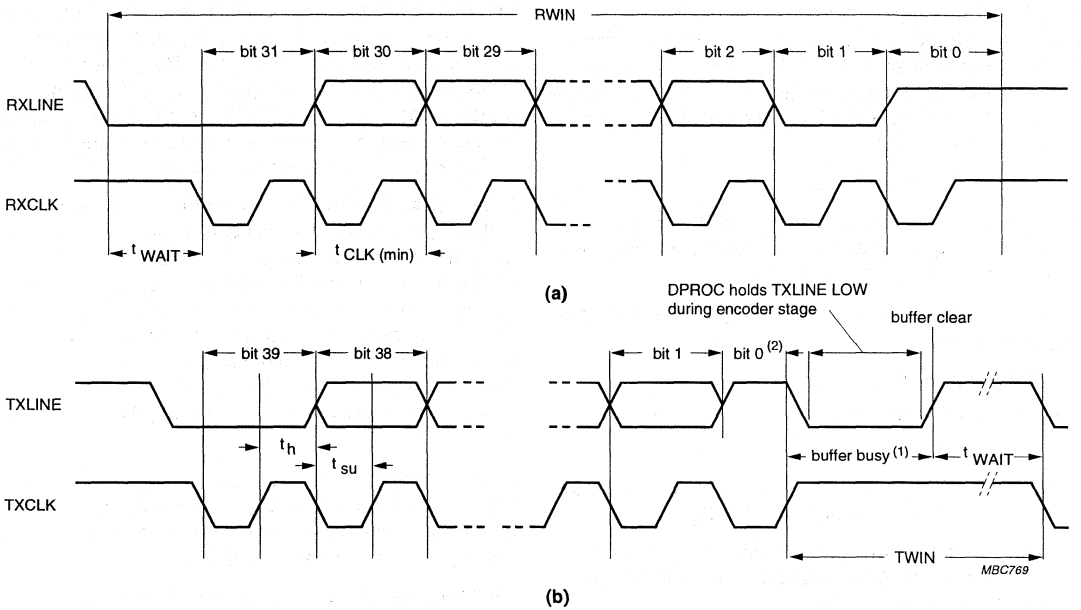
Table 10 Transmit data word

BIT	TITLE	SENSE	FUNCTION
39	start	LOW	identifies start of word
38 and 37	DCC	binary data	digital colour code (see Table 11)
36 to 1	transmit data	binary data	transmit data word
0	stop	HIGH	identifies end of the word



(a) Received data word.
(b) Transmit data word.

Fig.7 Data word formats.



(1) The buffer time depends on whether the first or subsequent words are being loaded.

(2) The system controller should monitor the TXLINE during bit 0, if the status of TXLINE does not change from a HIGH-to-LOW on the rising edge of TXCLK, then a framing error has occurred. This can be caused by glitches on the clock line or if an arbitration error occurred while the DPROC2 transmit register was being loaded. The system controller should recover the situation by holding TXLINE HIGH and supplying clocks on TXCLK until TXLINE goes LOW. Then the situation should be treated as a normal channel arbitration failure as described in Section "Reverse Control Channel Access Arbitration" - "Abort procedure (see Fig.10)".

(a) DPROC2 to microcontroller link; receive data timing.

(b) Microcontroller to DPROC2 link; transmit data timing.

Where:
t_h > 100 ns
t_{su} > 500 ns.

Fig.8 Data timing diagrams.

BCH and Manchester Encoding Block

The functions performed by this circuit block include:

- Reception of data from the System Controller
- Parity generation
- Message construction
- Manchester encoding.

Each 36-bit Information Word sent on the Reverse Voice and Control Channels is coded into a 48-bit code word. The code word consists of the 36-bit word followed by 12 parity bits. These parity bits are formed by clocking the information word into a 12-bit feedback shift register with characteristic polynomial:

$1 + x^3 + x^4 + x^5 + x^8 + x^{10} + x^{12}$

The BCH Encoder Block constructs the Reverse Voice and Control Channel data streams from the information it receives from the System Controller.

The streams are formed out of the four possible field types:

- Dotting (data inversions)
- 11-bit Synchronization Word
- Digital Colour Code (see Table 11)
- 48-bit code word.

The 2 bits of DCC received from the System Controller are coded into a 7-bit word as shown in Table 11.

The data sense for Manchester Encoding has a NRZ logic 1 encoded as a 0-to-1 transition and a NRZ logic 0 encoded as a 1-to-0 transition.

Reverse Control Channel Access Arbitration

The AMPS and TACS specifications require a method of arbitration on the Reverse Control Channel to prevent two mobiles from transmitting on the same channel at the same time.
This function is performed by DPROC2 monitoring the Busy/Idle stream sent on the Forward Control Channel.

The AMPS and TACS specifications state that once the mobile has commenced transmitting on the Reverse Control Channel it must monitor the Busy/Idle stream. If this stream becomes active outside a predetermined 'window', measured from the start of the transmission of the message, the mobile must terminate its transmission and disable the transmitter immediately.

In the Cellular Radio chip-set there are two levels of control of the RF transmitter; the first is absolute control by the System Controller, the second is conditional by other devices in the set. In DPROC2 the conditional control of the transmitter is performed via the output TXCTRL. This line is effectively wired ORed together, using open-drain outputs, with other devices which may wish to control the transmitter. When these devices do not wish to disable the transmitter their output is in a HIGH impedance state.

An exception to this procedure occurs when the Serving System instructs the mobile not to monitor the Busy/Idle bits. In this event the arbitration logic can be disabled by clearing I²C-bus register bit ABREN.

The flow of events during a Control Channel Access attempt is as follows:

Initial state

- Transmitter disabled
- DPROC2 transmit circuitry in power-up state
- TXCTRL line HIGH.

Table 11 Digital colour code; 7-bit word

DCC1	DCC0	CODED DCC						
0	0	0	0	0	0	0	0	0
0	1	0	0	1	1	1	1	1
1	0	1	1	0	0	0	1	1
1	1	1	1	1	1	1	0	0

Access attempt procedure

1. System Controller decides to send message(1).
2. System Controller drives TXCTRL LOW directly.
3. System Controller switches transmitter power-on and waits for power-up for the transmitter module (RF transmitter is still disabled by TXCTRL).
4. System Controller sets TXRST via I²C-bus to DPROC2.
5. System Controller sets ABREN via I²C (if required) allowing DPROC2 to control the transmitter.
6. System Controller determines status of Reverse Control Channel by monitoring the Busy/Idle bit. If busy, waits a random time then tries again.
7. System Controller releases TXCTRL allowing it to be pulled HIGH enabling the transmitter output.
8. System Controller transfers the first word of the message to DPROC2 via serial link(1).
9. DPROC2 sets I²C-bus signal TXIP and starts sending message while monitoring Busy/Idle status.
10. If channel becomes busy before 56 bits and ABREN is set then perform Abort Procedure.
11. If channel remains idle after 104 bits and ABREN is set then perform Abort Procedure.
12. System controller loads the subsequent words of the message into DPROC2 when the buffer becomes clear as shown in Fig.8(b).
13. On completion of entire message DPROC2 clears TXIP and 25 ms later the System Controller disables transmitter via I²C-bus.
14. System Controller finally sends TXRST to prepare DPROC2 for next transmission.

Abort procedure (see Fig.10)

1. DPROC2 immediately disables transmitter output by driving TXCTRL LOW.
2. DPROC2 sets TXABRT.
3. System Controller detects failure by monitoring TXCTRL and TXABRT.
4. System Controller disables transmitter via RF power amplifier.
5. System Controller sends TXRST to prepare DPROC2 for next transmission.

Signal Tone Generation (ST)

The 8 or 10 kHz (TACS or AMPS) tone generated from the Manchester Encoding Block is used as the Signalling Tone stream.

(1) At stage 1 the system controller may choose to preload DPROC2 with the first word of the message and hold it from transmission until stage 7 using the TXHOLD line. This gives a lower time overhead between detecting an IDLE channel and commencing the transmission. To use this feature TXHOLD must be driven HIGH before the last bit of data has been transferred into DPROC2. Figure 9 illustrates the DPROC2 data transmission timing.

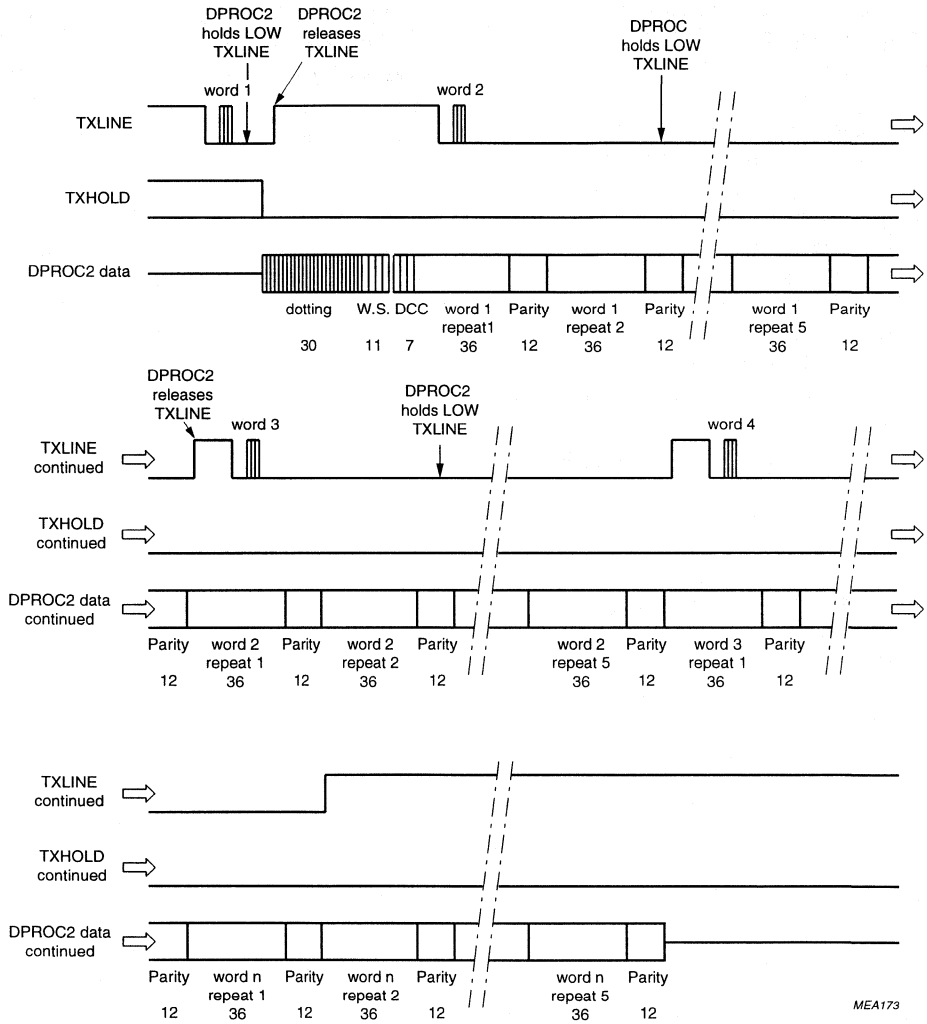


Fig.9 DPROC2 data transmission timing/microcontroller interface.

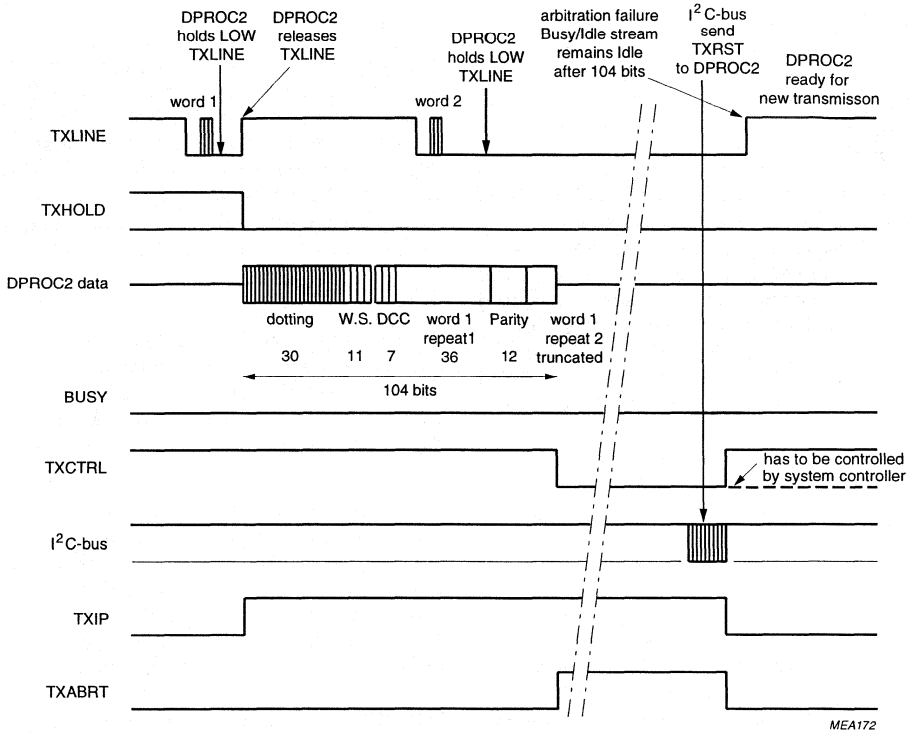


Fig.10 DPROC data transmission timing/microcontroller interface during arbitration failure.

Analog circuit blocks

General

The analog signal processing functions on DPROC2 are implemented using switched-capacitor techniques. The main filtering functions are operated at 300 kHz, and these circuits are 'interfaced' to the continuous time and sampled digital domains by RC active filters, passive interpolators and comparators.

The RC sections, the Anti-Alias Filter and the Clock Filter, are non-critical and are designed to tolerate process spreads. The critical filtering in the SAT Filter and the Output Filter, is performed by 300 kHz switched-capacitor circuitry. The Passive Interpolator increases the sampling rate from 300 kHz to 1.2 MHz. The sampled analog signals from the Passive Interpolator is converted to a sampled 2-state digital signal by a Comparator. The Gated D/A converter blocks and Analog Summer block together perform resynchronization and sub-sampling of the digitally generated DPROC2 output signals, and conversion to the sampled analog domain.

These analog sections of the device are shown in Fig.1.

Bias Generator

The Bias Generator generates the analog ground reference voltage (AGND) used internally within the DPROC2 device. To minimize noise AGND must be externally decoupled to V_{SSA} as shown in Fig.12. It also contains a current reference to generate all bias currents for the analog circuits.

Anti-Aliasing Filter

The Anti-Aliasing Filter is placed before the SAT filter block to prevent any unwanted signals or high-frequency noise present on the DEMODD pin being aliased into the pass-band by the sampling action of the switched-capacitor filter. To achieve this the Anti-Aliasing Filter is a time-continuous RC-active low-pass filter.

SAT Input Filter

The SAT Input Filter is a switched-capacitor filter which provides band-pass filtering of the SAT signals from the DEMODD pin to improve the SAT signal-to-noise ratio prior to recovery and transponding.

Passive Interpolator

The function of the Passive Interpolator is to increase the sampling rate at the output of the SAT filter. This reduces the coarseness of the zero-crossing information which would otherwise cause unacceptable isochronous distortion in the recovered signal.

Comparators

The Comparators form the analog-to-digital interface for the received data and SAT signals from the DEMODD pin. These comparators act as limiting amplifiers which convert the filtered sampled analog signals into 2-state sampled digital signals containing only the zero-crossing information from the analog signal. To prevent unwanted signals being processed by the digital circuitry both comparators have a hysteresis implemented

Gated D/A converters and Analog Summer

The Gated D/A converters and Analog Summer form the interface between the digital and analog circuitry on the transmit path of DPROC2. It is at this point that the three sampled digital signals, containing SAT, ST and encoded digital data, are combined to form a composite signal.

The data streams are enabled by the I^2C signals STEN, SATEN and the internal signal DATAEN respectively (DATAEN disables SAT and ST when data is being transmitted). The digital-to-analog conversion and sub-sampling operation is performed by the Gated D/A converters and Analog Summer.
The typical relative signal weights applied in the summer (with respect to the data path) are shown in Table 12.

Table 12 Typical relative signal weight

SIGNAL	RELATIVE OUTPUT LEVEL AMPS AND TACS
ST or DATA	1.0
SAT	0.25

Output Filter

The Output Filter is a switched-capacitor filter which performs band-limiting of the DPROC2 output signals in accordance with the AMPS and TACS specifications. The required below band roll-off is achieved via external AC-coupling from the DATA pin.

Clock Filter

The Clock Noise Filter is a non-critical continuous time RC-active low-pass filter used to remove any switching transient residues from the output signal. It contains an output driver stage to provide a low output impedance and sufficient driving capability for the pin DATA.

APPLICATION INFORMATION

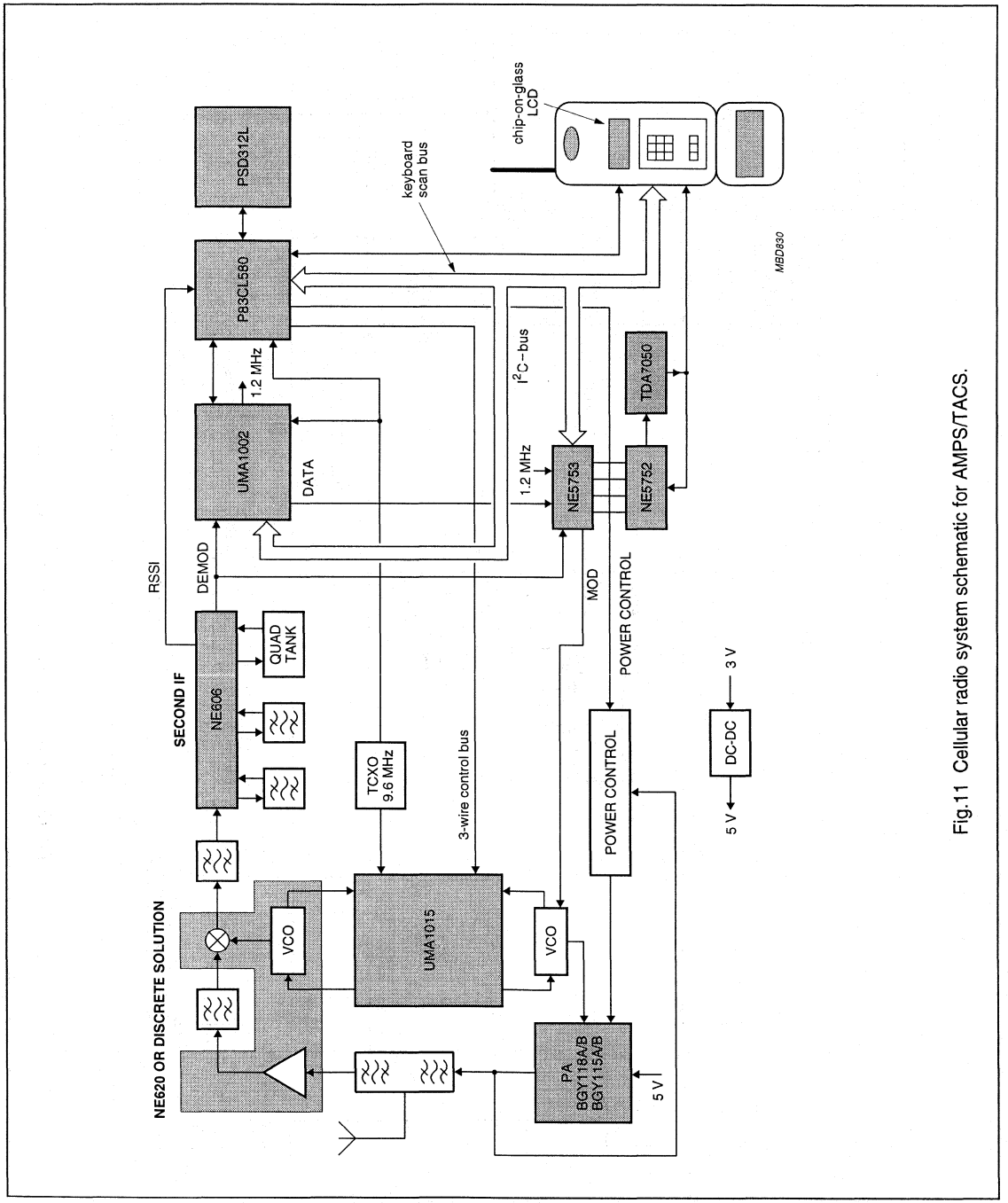


Fig.11 Cellular radio system schematic for AMPS/TACS.

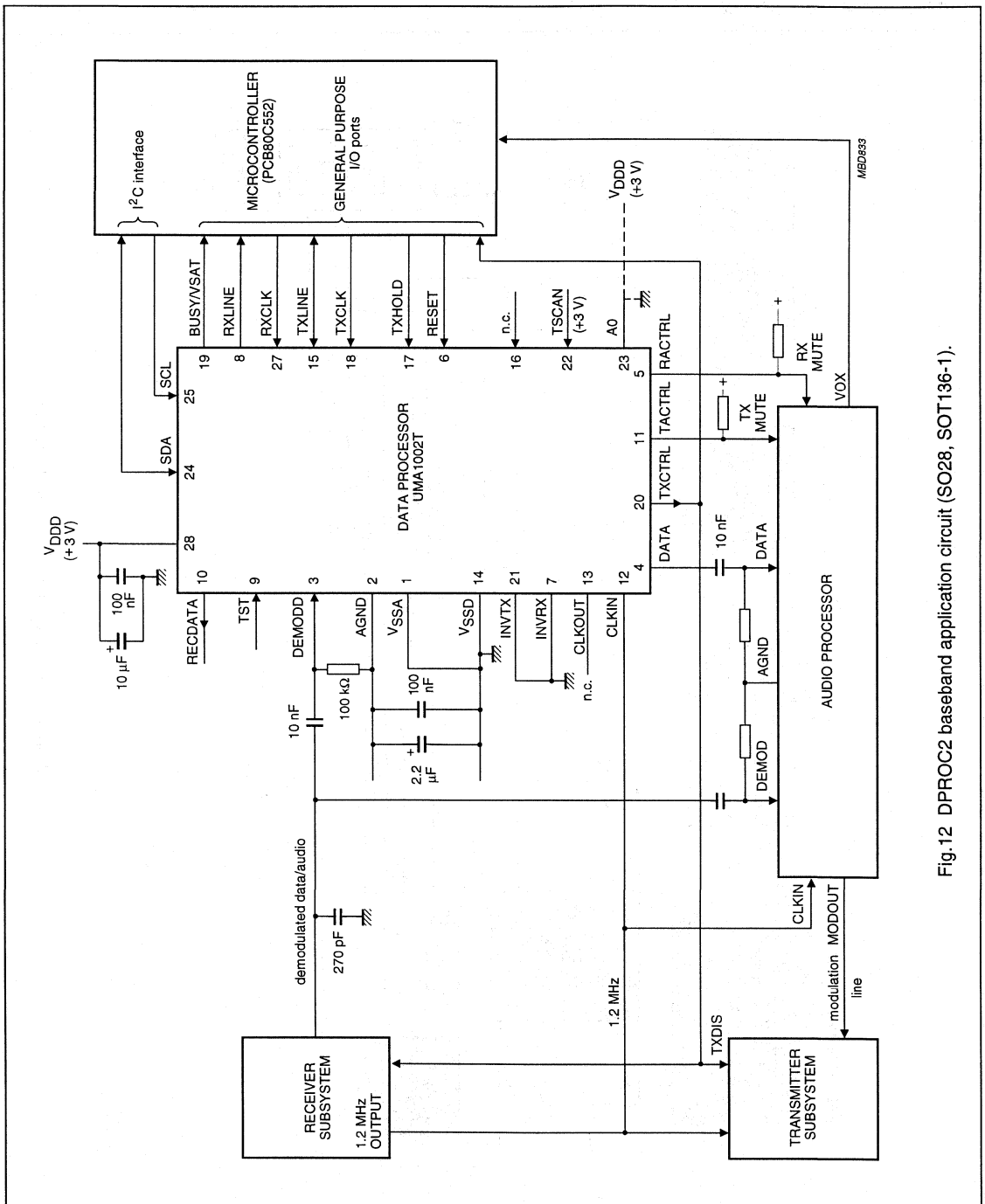


Fig.12 DPROC2 baseband application circuit (SO28, SOT136-1).

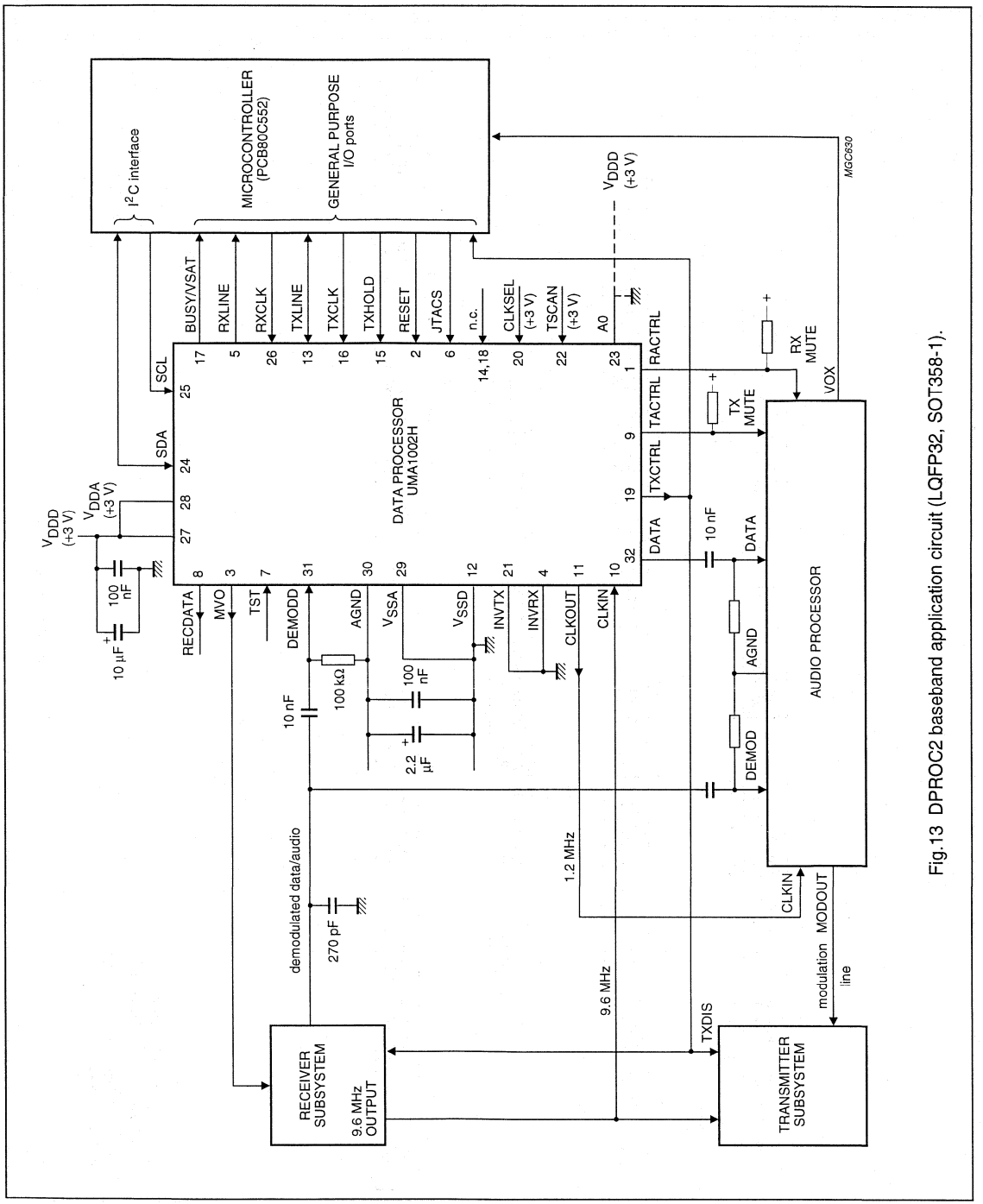
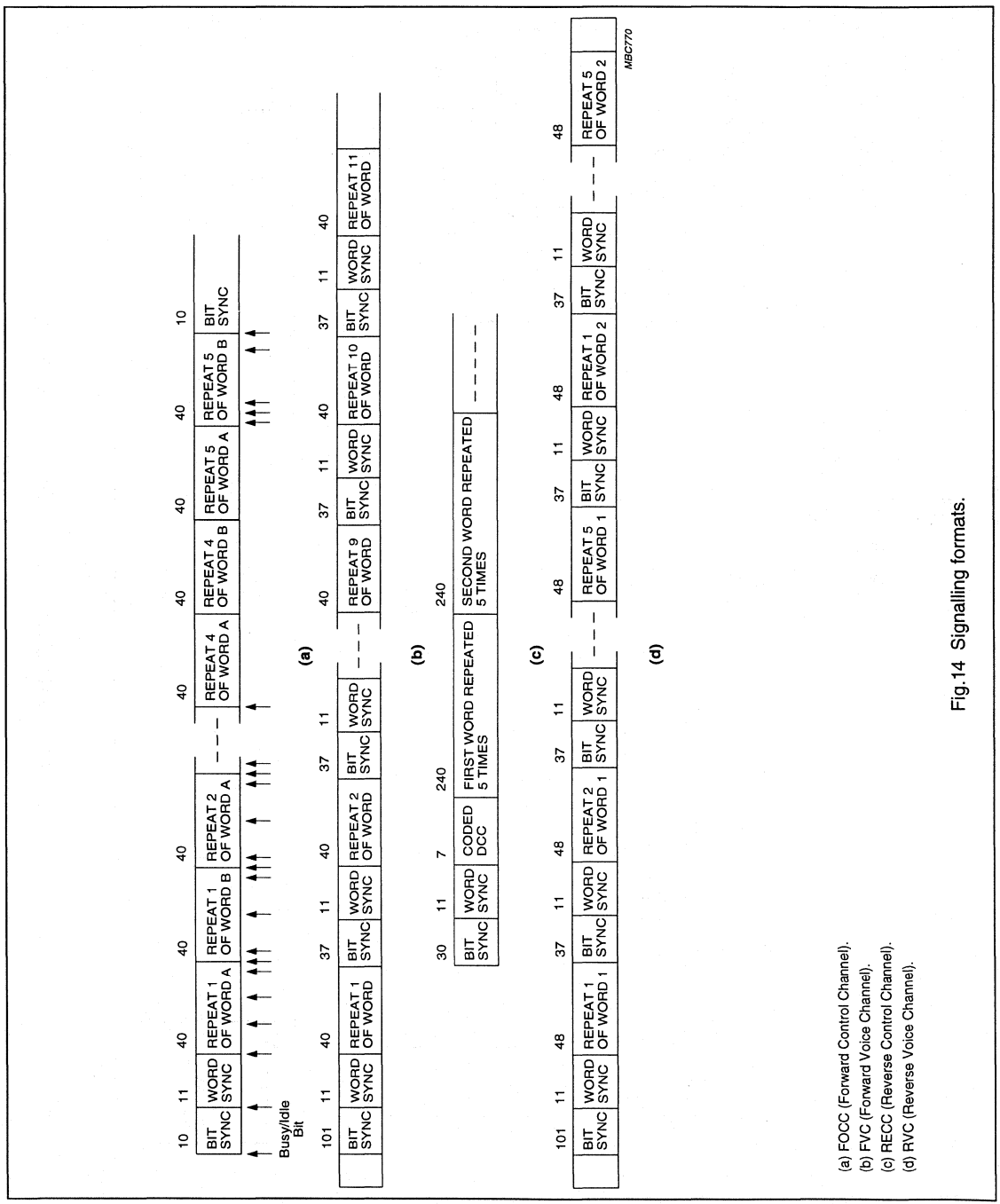


Fig.13 DPROC2 baseband application circuit (LQFP32, SOT358-1).

SIGNALLING FORMATS



(a) FOCC (Forward Control Channel).
(b) FVC (Forward Voice Channel).
(c) RECC (Reverse Control Channel).
(d) RVC (Reverse Voice Channel).

Fig.14 Signalling formats.

LIMITING VALUES

In accordance with Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		−0.5	+6.5	V
I_{DD}	supply current		–	50	mA
I_I	DC input current (any input)		–	±10	mA
I_O	DC output current (any output)		–	±10	mA
V_I	input voltages (all inputs)	$V_{DD(max)}$ = 6 V	−0.5	V_{DD} + 0.5	V
P_{tot}	total power dissipation		–	300	mW
P_o	power dissipation per output		–	10	mW
T_{amb}	operating ambient temperature		−30	+70	°C
T_{stg}	storage temperature		−65	+150	°C

DC CHARACTERISTICS

V_{DD} = 3 V (V_{DDA} and V_{DDD} externally connected); T_{amb} = −30 to +70 °C; f_{CLKIN} = 1.2 MHz (if CLKSEL = logic 0); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		2.7	3.0	5.5	V
I_{DD}	operating supply current at pins V_{DDD} and V_{DDA}	in FVC	–	1.3	1.8	mA
		in FOCC	–	0.4	–	mA
Digital inputs: INVRX, INVTX, CLKSEL, TXHOLD, TXCLK, A0, RESET, RXCLK, TST, TSCAN, CLKIN and JTACS						
V_{IL}	LOW level input voltage		−0.3	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD} + 0.3	V
I_{LI}	LOW/HIGH level input leakage current	pins without pull-down	–	–	1	µA
$R_{pdCLKSEL}$	CLKSEL internal pull-down resistance		–	200	–	kΩ
$R_{pdJTACS}$	JTACS internal pull-down resistance		–	200	–	kΩ
R_{pdTST}	TST internal pull-down resistance		–	200	–	kΩ
Digital push-pull outputs: RXLINE, BUSY/VSAT, RECDATA, MVO and CLKOUT						
V_{OL}	LOW level output voltage	I_{sink} = 1 mA	–	–	0.4	V
V_{OH}	HIGH level output voltage	I_{source} = −1 mA	V_{DD} − 0.4	–	–	V
Open-drain n-channel outputs: TXCTRL, TACTRL and RACTRL						
V_{OL}	LOW level output voltage	I_{sink} = 2 mA	–	–	0.4	V
Open-drain n-channel input/output: TXLINE						
V_{OL}	LOW level output voltage	I_{sink} = 2 mA	–	–	0.4	V
V_{IL}	LOW level input voltage		−0.3	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD} + 0.3	V
$R_{puTXLINE}$	internal pull-up resistance		–	100	–	kΩ
I^2C-bus pins: SCL and SDA						
t_{data}	data conversion rate		–	–	100	kbits/s
Analog reference pin: AGND						
V_{AGND}	DC voltage level	for V_{DD} = 2.7 to 5.5 V	–	$0.5V_{DD}$	–	V

AC CHARACTERISTICS

V_{DD} = 3 V (V_{DDA} and V_{DDD} externally connected); T_{amb} = −30 to +70 °C; f_{CLKIN} = 1.2 MHz (if CLKSEL = logic 0); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data rate of data transfer link: RXCLK, RXLINE, TXCLK, TXLINE						
t_{data}	data conversion rate		–	–	500	kbit/s
Clock input: CLKIN (CLKSEL = logic 0)						
C_i	input capacitance		–	5	–	pF
T_{CLKIN}	clock input period time		833.25	833.33	833.42	ns
t_{CLKINH}	clock input HIGH time		40	50	60	$\%T_{CLKIN}$
t_r	clock input rise time		–	50	–	ns
t_f	clock input fall time		–	50	–	ns
Clock input: CLKIN (CLKSEL = logic 1)						
T_{CLKIN}	clock input period time		–	104.17	–	ns
t_{CLKINH}	clock input HIGH time		40	50	60	$\%T_{CLKIN}$
t_r	clock input rise time		–	5	–	ns
t_f	clock input fall time		–	5	–	ns
Analog output: DATA						
V_{DATA}	DC output voltage level		–	V_{AGND}	–	V
$V_{o(p-p)}$	output voltage level for signalling tone (peak-to-peak value)	V_{DD} = 3 V; note 1	1.14	1.2	1.26	V
		V_{DD} = 5 V; note 1	1.9	2.0	2.1	V
THD	total harmonic distortion for Supervisory Audio Tone (SAT)		–	–	10	%
R_L	allowed load resistance to AC ground		10	–	–	kΩ
C_L	allowed load capacitance to AC ground		–	–	100	pF
Analog input: DEMODD						
V_{DEMODD}	DC input voltage level	100 kΩ resistor external to AGND	–	V_{AGND}	–	V
$V_{i(p-p)}$	data input voltage level (peak-to-peak value)	input via a 10 nF capacitor	200	250	600	mV
$V_{i(p-p)}$	SAT input voltage level (peak-to-peak value)		50	–	–	mV
Z_i	input impedance		1	–	–	MΩ

Note

1. Plus supply voltage variation (ΔV_{DD}), R_L = 10 kΩ.

Low-power dual frequency synthesizer for radio communications

UMA1015AM

FEATURES

- Two fully programmable RF dividers up to 1.1 GHz
- Fully programmable reference divider up to 35 MHz
- 2 : 1 or 1 : 1 ratio of selectable reference frequencies
- Fast three-line serial bus interface
- Adjustable phase comparator gain
- Programmable out-of-lock indication for both loops
- On-chip voltage doubler
- Low current consumption from 3 V supply
- Separate power-down mode for each synthesizer
- Up to 4 open-drain output ports
- Crystal input frequency signal inverted and buffered output on separate pin.

APPLICATIONS

- Cordless telephone
- Hand-held mobile radio.

GENERAL DESCRIPTION

The UMA1015AM is a low-power dual frequency synthesizer for radio communications which operates in the 50 to 1100 MHz frequency range. Each synthesizer consists of a fully programmable main divider, a phase and frequency detector and a charge pump. There is a fully programmable reference divider common to both synthesizers which operates up to 35 MHz.

The device is programmed via a 3-wire serial bus which operates up to 10 MHz. The charge pump currents (gains) are fixed by an external resistance at pin 20 (I_{SET}). The BiCMOS device is designed to operate from 2.7 V (3 NiCd cells) to 5.5 V at low current. Digital supplies V_{DD1} and V_{DD2} must be at the same potential. The charge pump supply (V_{CC}) can be provided by an external source or on-chip voltage doubler. V_{CC} must be equal to or higher than V_{DD1}.

Each synthesizer can be powered-down independently via the serial bus to save current. It is also possible to power-down the device via the HPD input (pin 5).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD1}, V_{DD2}	digital supply voltage	$V_{DD1} = V_{DD2}$	2.7	–	5.5	V
V_{CC}	charge pump supply voltage	external supply; doubler disabled; $V_{CC} \geq V_{DD}$	2.7	–	6.0	V
V_{CCvd}	charge pump supply from voltage doubler	doubler enabled	–	$2V_{DD1} - 0.6$	6.0	V
$I_{DD1} + I_{DD2} + I_{CC}$	operating supply current	both synthesizers ON; doubler disabled; $V_{DD1} = V_{DD2} = 3$ V	–	8.7	–	mA
$I_{DDpd} + I_{CCpd}$	total current in power-down mode	doubler disabled; $V_{DD1} = V_{DD2} = 3$ V	–	3	–	µA
I_{DDpd}	current in power-down mode from supply V_{DD1} and V_{DD2}	doubler enabled; $V_{DD1} = V_{DD2} = 3$ V	–	0.25	–	mA
f_{RF}	RF input frequency for each synthesizer		50	–	1100	MHz
f_{XTALIN}	crystal input frequency		3	–	35	MHz
$f_{pc(min)}$	minimum phase comparator frequency		–	10	–	kHz
$f_{pc(max)}$	maximum phase comparator frequency		–	750	–	kHz
T_{amb}	operating ambient temperature		–30	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UMA1015AM	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

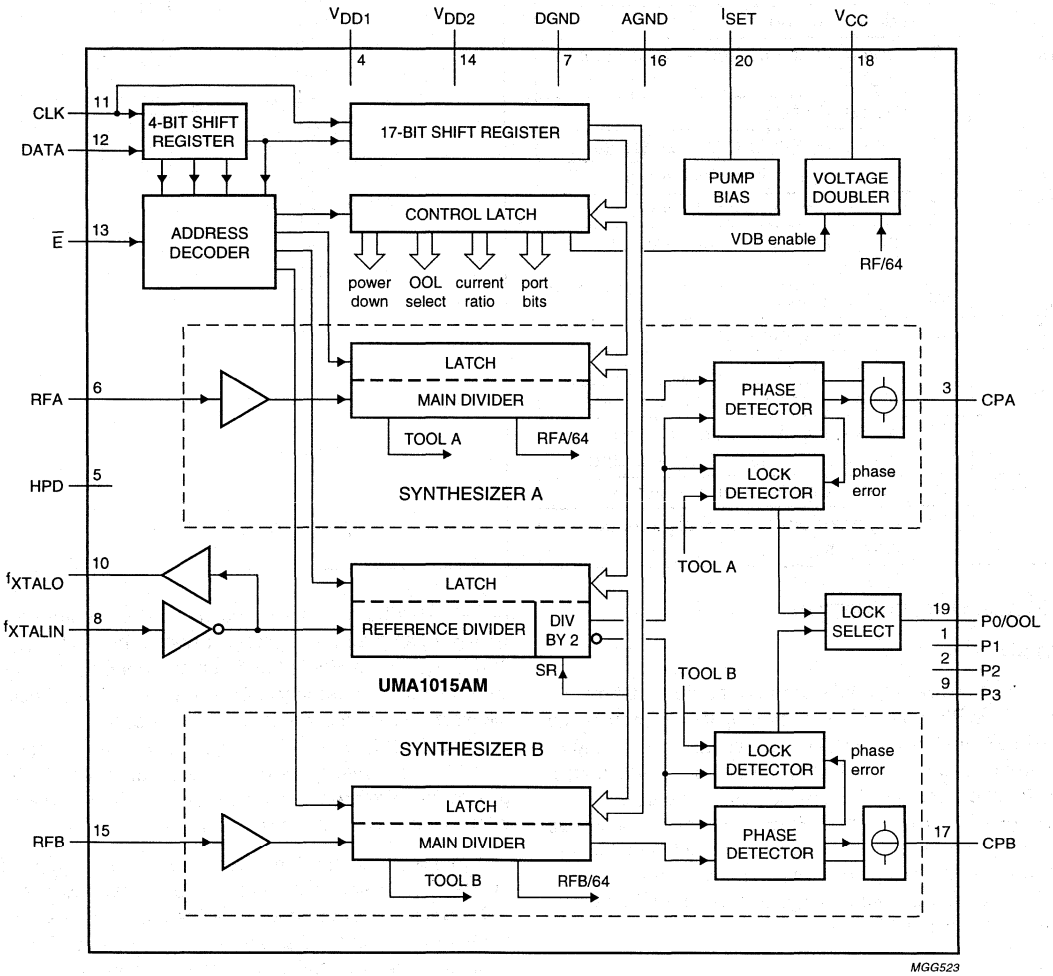


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
P1	1	output Port 1
P2	2	output Port 2
CPA	3	charge pump output synthesizer A
V_{DD1}	4	digital supply voltage 1
HPD	5	hardware power-down (input LOW = power-down)
RFA	6	RF input synthesizer A
DGND	7	digital ground
f_{XTALIN}	8	common crystal frequency input from TCXO
P3	9	output Port 3
f_{XTALO}	10	open-drain output of f_{XTAL} signal
CLK	11	programming bus clock input
DATA	12	programming bus data input
$\overline{E}$	13	programming bus enable input (active LOW)
V_{DD2}	14	digital supply voltage 2
RFB	15	RF input synthesizer B
AGND	16	analog ground to charge pumps
CPB	17	charge pump output synthesizer B
V_{CC}	18	analog supply to charge pump; external or voltage doubler output
P0/OOL	19	Port output 0/out-of-lock output
I_{SET}	20	regulator pin to set charge pump currents

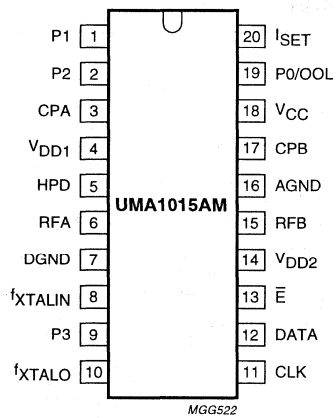


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Main dividers

Each synthesizer has a fully programmable 17-bit main divider. The RF input drives a pre-amplifier to provide the clock to the first divider bit. The pre-amplifier has a high input impedance, dominated by pin and pad capacitance. The circuit operates with signal levels from below 50 mV (RMS) up to 250 mV (RMS), and at frequencies up to 1.1 GHz. The high frequency sections of the divider are implemented using bipolar transistors, while the slower section uses CMOS technology. The range of division ratios is 512 to 131071.

Reference divider

There is a common fully programmable 12-bit reference divider for the two synthesizers. The input f_{XTALIN} drives a pre-amplifier to provide the clock input for the reference divider. This clock signal is also inverted and output on pin f_{XTALO} (open drain). A crystal connected between f_{XTALIN} and f_{XTALO} with suitable feedback components can be used to make an oscillator. An extra divide-by-2 block allows a reference comparison frequency for synthesizer B to be half the frequency of synthesizer A. This feature is selectable using the program bit SR. If the programmed reference divider ratio is R then the ratio for each synthesizer is as given in Table 1.

The range for the division ratio R is 8 to 4095. Opposite edges of the divider output are used to drive the phase detectors to ensure that active edges arrive at the phase detectors of each synthesizer at different times. This minimizes the potential for interference between the charge pumps of each loop. The reference divider consists of CMOS devices operating beyond 35 MHz.

Table 1 Synthesizer ratio of reference divider

SR	SYNTHESIZER A	SYNTHESIZER B
0	R	R
1	R	2R

Phase comparators

For each synthesizer, the outputs of the main and reference dividers drive a phase comparator where a charge pump produces phase error current pulses for integration in an external loop filter. The charge pump current is set by an external resistance R_{SET} at pin I_{SET}, where a temperature-independent voltage of 1.1 V is generated. R_{SET} should be between 12 and 60 kΩ.
The charge pump current, I_{CP}, can be programmed to be either $(12 \times I_{SET})$ or $(24 \times I_{SET})$ with a maximum of 2.3 mA.
The dead zone, caused by finite switching of current pulses, is cancelled by an internal delay in the phase detector thus giving improved linearity. The charge pump has a separate supply, V_{CC}, which helps to reduce the interference on the charge pump output from other parts of the circuit. V_{CC} can be higher than V_{DD1} if a wider range on the VCO input is required. V_{CC} must not be less than V_{DD1}.

Voltage doubler

If required, there is a voltage doubler on-chip to supply the charge pumps at a higher level than the nominal available supply. The doubler operates from the digital supply V_{DD1}, and is internally limited to a maximum output of 6 V.
An external capacitor is required on pin V_{CC} for smoothing, the capacitor required to develop the extra voltage is integrated on-chip. To minimize the noise being introduced to the charge pump output from the voltage doubler, the doubler clock is suppressed (provided both loops are in-lock) for the short time that the charge pumps are active. The doubler clock (RF/64) is derived from whichever main divider is operating (synthesizer A has priority). While both synthesizers are powered down (and the doubler is enabled), the doubler clock is supplied by a low-current internal oscillator. The doubler can be disabled by programming the bit VDON to logic 0, in order to allow an external charge pump supply to be used.

Out-of-lock indication/output ports

There is a common lock detector on-chip for the synthesizers. The lock condition of each, or both loops, is output via an open-drain transistor which drives pin P0/OOL (when out-of-lock, the transistor is turned on and therefore the output is forced LOW). The lock condition output is software selectable (see Table 4).

An out-of-lock condition is flagged when the phase error is greater than T_{OOL}, which is approximately 30 ns.
The out-of-lock flag is only released after the first reference cycle where the phase error is less than T_{OOL}.
The out-of-lock function can be disabled, via the serial bus, and the pin P0/OOL can be used as a port output. Three other port outputs P1, P2 and P3 (open-drain transistors) are also available.

Serial programming bus

A simple 3-line unidirectional serial bus is used to program the circuit. The 3 lines are DATA, CLK and $\overline{E}$ (enable). The data sent to the device is loaded in bursts framed by $\overline{E}$. Programming clock edges are ignored until $\overline{E}$ goes active LOW. The programmed information is loaded into the addressed latch when $\overline{E}$ returns inactive (HIGH). This is allowed when CLK is in either state without causing any consequences to the register data. Only the last 21 bits serially clocked into the device are retained within the programming register. Additional leading bits are ignored, and no check is made on the number of clock pulses. The fully static CMOS design uses virtually no current when the bus is inactive. It can always capture new programming data even during power-down of both synthesizers.

However when either synthesizer A or synthesizer B or both are powered-on, the presence of a TCXO signal is required at pin 8 (f_{XTALIN}) for correct programming.

Data format

Data is entered with the most significant bit first.
The leading bits make up the data field, while the trailing four bits are an address field. The address bits are decoded on the rising edge of $\overline{E}$. This produces an internal load pulse to store the data in the addressed latch.
To ensure that data is correctly loaded on first power-up, $\overline{E}$ should be held LOW and only taken HIGH after having programmed an appropriate register. To avoid erroneous divider ratios, the pulse is inhibited during the period when data is read by the frequency dividers. This condition is guaranteed by respecting a minimum $\overline{E}$ pulse width after data transfer. The data format and register bit allocations are shown in Table 2.

Table 2 Bit allocation

FIRST	REGISTER BIT ALLOCATION																			LAST
p1	p2	p3	p4	p5	p6	p7	p8	p9	p10	p11	p12	p13	p14	p15	p16	p17	p18	p19	p20	p21
dt16	dt15	dt14	dt13	dt12	DATA FIELD							dt4	dt3	dt2	dt1	dt0	ADDRESS			
X	X	VDON	PO	OLA	OLB	CRA	CRB	X	X	sPDA	sPDB	P3	P2	P1	X	X	0	0	0	1
MA16	SYNTHESIZER A MAIN DIVIDER COEFFICIENT															MA0	0	1	0	0
0	0	0	0	SR	R11	REFERENCE DIVIDER COEFFICIENT										R0	0	1	0	1
MB16	SYNTHESIZER B MAIN DIVIDER COEFFICIENT															MB0	0	1	1	0
RESERVED FOR TEST(1)																	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	sPBF	0	0	1	0	0	0

Note

1. The test register should not be programmed with any other values except all zeros for normal operation.

Table 3 Bit allocation description

SYMBOL	DESCRIPTION
sPDA, sPDB	software power-down for synthesizers A and B (0 = power-down)
sPBF	software power-on for f_{xtal} buffer (1 = buffer on)
P3, P2, P1 and P0	bits output to pins 1, 2, 9 and 19 (1 = high impedance)
VDON	voltage doubler enable (1 = doubler enabled)
OLA, OLB	out-of-lock select; selects signal output to pin 19 (see Table 4)
CRA, CRB	charge pump A/B current to I_{SET} ratio select (see Table 5)
SR	reference frequency ratio select (see Table 6)

Table 4 Out-of-lock select

OLA	OLB	OUTPUT AT PIN 19
0	0	P0
0	1	lock status of loop B; OOLB
1	0	lock status of loop A; OOLA
1	1	logic OR function of loops A and B

Table 5 Charge pump current ratio

CRA/CRB	CURRENT AT PUMP
0	$I_{CP} = 12 \times I_{SET}$
1	$I_{CP} = 24 \times I_{SET}$

Table 6 Reference division ratio

SR	SYNTHESIZER A	SYNTHESIZER B
0	R	R
1	R	2R

Power-down modes

The device can be powered down either via pin HPD (active LOW = power-down) or via the serial bus (bits sPDA and sPDB, logic 0 = power-down).

The synthesizers are powered up when both hardware and software Power-down signals are at logic 1. When only one synthesizer is powered down, the functions common to both will be maintained (independent of the state of sPBF). When both synthesizers are powered down, the f_{xtal} buffer can be maintained in an active state by setting sPBF to logic 1. This will allow any system clock derived from the f_{XTALO} buffered output to remain on in power-down. Note that sPBF is independent of the state of HPD. When both synthesizers are switched off, the voltage doubler (if enabled) will remain active drawing a reduced current. An internal oscillator will drive the doubler in this situation. If both synthesizers have been in a power-down condition, then when one or both synthesizers are reactivated, the reference and main dividers restart in such a way as to avoid large random phase errors at the phase comparator.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD1}, V_{DD2}	DC range of digital power supply voltage with respect to DGND	−0.3	+6.0	V
V_{CC}	DC charge pump supply voltage with respect to AGND	−0.3	+6.0	V
ΔV_{CC-DD}	difference in voltage between V_{CC} and V_{DD1}, V_{DD2}	−0.3	+6.0	V
V_n	DC voltage at pins 1, 2, 5, 6, 8 to 15, 19 and 20 with respect to DGND	−0.3	V_{DD1} + 0.3	V
$V_{3, 17}$	DC voltage at pins 3 and 17 with respect to AGND	−0.3	V_{CC} + 0.3	V
ΔV_{GND}	difference in voltage between AGND and DGND (these pins should be connected together)	−0.3	+0.3	V
T_{stg}	storage temperature	−55	+125	°C
T_{amb}	operating ambient temperature	−30	+85	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

CHARACTERISTICS

$V_{DD1} = V_{DD2} = 2.7$ to 5.5 V; $V_{CC} = 2.7$ to 6.0 V; $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies; (V_{DD1}, V_{DD2} and V_{CC}) voltage doubler disabled, external supply on V_{CC}						
V_{DD1}, V_{DD2}	digital supply voltage	$V_{DD1} = V_{DD2}$	2.7	–	5.5	V
$I_{DD1} + I_{DD2}$	total digital supply current from V_{DD1} and V_{DD2}	f_{XTAL} = 12.8 MHz; both synthesizers on; $V_{DD1} = V_{DD2}$ = 3 V	–	8.7	–	mA
		f_{XTAL} = 12.8 MHz; both synthesizers on; $V_{DD1} = V_{DD2}$ = 5.5 V	–	–	12.5	mA
I_{DDpda}, I_{DDpdb}	total digital supply current from V_{DD1} and V_{DD2} with one synthesizer in power-down mode	f_{XTAL} = 12.8 MHz; one synthesizer powered down; $V_{DD1} = V_{DD2}$ = 3 V	–	5.0	–	mA
		f_{XTAL} = 12.8 MHz; one synthesizer powered down; $V_{DD1} = V_{DD2}$ = 5.5 V	–	–	7.5	mA
$I_{DD(xtal)}$	digital supply current from V_{DD1} with both synthesizers powered down and crystal buffer on	f_{XTAL} = 12.8 MHz; V_{HPD} = 0 V; sPBF = 1; $V_{DD1} = V_{DD2}$ = 3 V	–	0.5	–	mA
		f_{XTAL} = 12.8 MHz; V_{HPD} = 0 V; sPBF = 1; $V_{DD1} = V_{DD2}$ = 5.5 V	–	–	1.15	mA
I_{DDpd}	digital supply current in power-down mode	both synthesizers powered down; V_{HPD} = 0 V; sPBF = 0	–	–	60	µA
V_{CC}	charge pump supply voltage	$V_{CC} \geq V_{DD}$	2.7	–	6.0	V
I_{CC}	charge pump supply current	both synthesizers on and in lock; f_{ref} = 12.5 kHz	–	–	25	µA
I_{CCpd}	charge pump supply current in power-down mode	both synthesizers powered down	–	–	25	µA
Voltage doubler enabled						
I_{DD}	total digital supply current from V_{DD1} and V_{DD2}	f_{XTAL} = 12.8 MHz; both synthesizers on and in lock; V_{DD1} = 3 V; f_{RF} = 900 MHz	–	9.2	12	mA
I_{DDpd}	total digital supply current in power-down mode from V_{DD1} and V_{DD2}	both synthesizers powered down; V_{DD1} = 3 V; V_{HPD} = 0 V; sPBF = 0	–	0.25	0.4	mA
V_{CCvd}	charge pump supply voltage	DC current drawn from V_{CC} = 50 µA; f_{RF} > 100 MHz	4.2	$2V_{DD1} - 0.6$	6.0	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RF main divider input; RFA and RFB						
f_{RF}	RF input frequency		50	–	1100	MHz
$V_{RF(rms)}$	RF input signal voltage (RMS value; AC coupled)	R_s = 50 Ω; f_{RF} = 400 to 1100 MHz	50	–	250	mV
		R_s = 50 Ω; f_{RF} = 80 to 400 MHz	150	–	400	mV
		R_s = 50 Ω; f_{RF} = 50 to 80 MHz	225	–	400	mV
Z_I	input impedance (real part)	f_{RF} = 1 GHz; indicative, not tested	–	300	–	Ω
C_I	input capacitance	indicative, not tested	–	1	–	pF
R_{pm}	principle main divider ratio		512	–	131071	
Reference divider input; f_{XTALIN}						
f_{XTALIN}	reference input frequency from crystal		3	–	35	MHz
$V_{XTALIN(rms)}$	sinusoidal input voltage (RMS value)		100	–	500	mV
Z_I	input impedance (real part)	f_{XTALIN} = 12.8 MHz; indicative, not tested	–	10	–	kΩ
C_I	input capacitance	indicative, not tested	–	1	–	pF
R_{rd}	reference divider ratio		8	–	4095	
Charge pump current setting resistor input; I_{SET}						
V_{SET}	voltage output on I_{SET}	R_{SET} = 12 to 60 kΩ	–	1.1	–	V
Charge pump outputs; CPA and CPB						
I_{cp}	charge pump sink or source current	R_{SET} = 15 kΩ; CRA/CRB = logic 1; $I_{cp} = I_{SET} \times 24$; V_{cp} = 0.4 V to V_{CC} – 0.5 V	1.3	1.75	2.3	mA
		R_{SET} = 15 kΩ; CRA/CRB = logic 0; $I_{cp} = I_{SET} \times 12$; V_{cp} = 0.4 V to V_{CC} – 0.5 V	0.7	0.9	1.2	mA
I_{LI}	charge pump off leakage current	V_{cp} = 0.4 V to V_{CC} – 0.5 V	–5	±1	+5	nA
Logic input signal levels; DATA, CLK, $\overline{E}$ and HPD						
V_{IH}	HIGH level input voltage	at logic 1	$0.7V_{DD1}$	–	V_{DD1} + 0.3	V
V_{IL}	LOW level input voltage	at logic 0	–0.3	–	$0.3V_{DD1}$	V
I_{bias}	input bias currents	at logic 1 or logic 0	–5	–	+5	μA
C_I	input capacitance	indicative, not tested	–	1	–	pF
Port outputs/Out-of-lock; P0/OOL, P1, P2, P3 and f_{XTALO} - open drain outputs						
V_{OL}	LOW level output voltage	I_{sink} < 0.4 mA	–	–	0.4	V

SERIAL TIMING CHARACTERISTICS

V_{DD1} = 3 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Serial programming clock; CLK					
t_r, t_f	input rise and fall times	–	10	40	ns
T_{cy}	clock period	100	–	–	ns
Enable programming; $\overline{E}$					
t_{START}	delay to rising clock edge	40	–	–	ns
t_{END}	delay from last falling clock edge	–20	–	–	ns
t_W	minimum inactive pulse width	4000	–	–	ns
$t_{SU;\overline{E}}$	enable set-up time to next clock edge	20	–	–	ns
Register serial input data; DATA					
$t_{SU;DAT}$	input data to clock set-up time	20	–	–	ns
$t_{HD;DAT}$	input data to clock hold time	20	–	–	ns

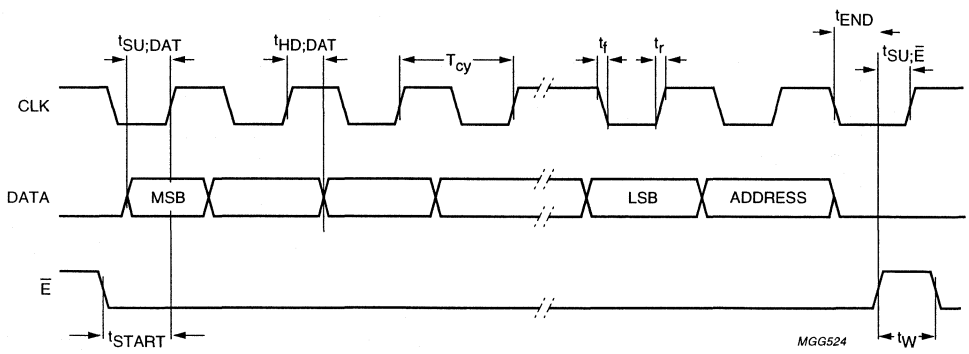
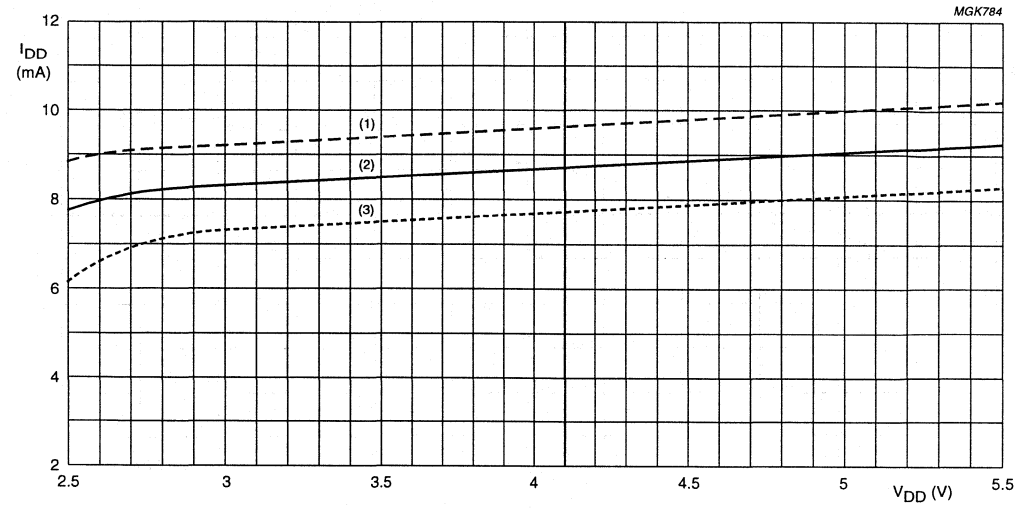


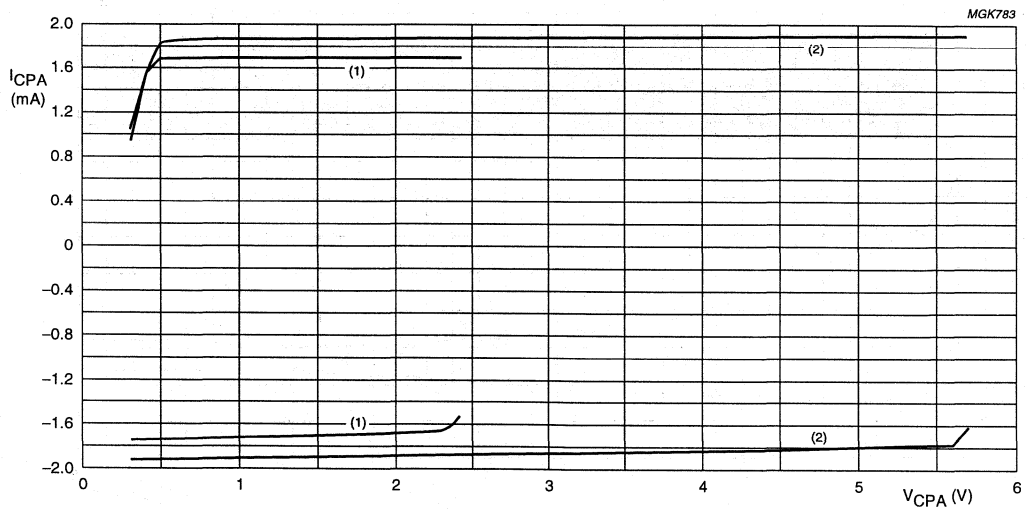
Fig.3 Serial bus timing diagram.

TYPICAL PERFORMANCE CHARACTERISTICS



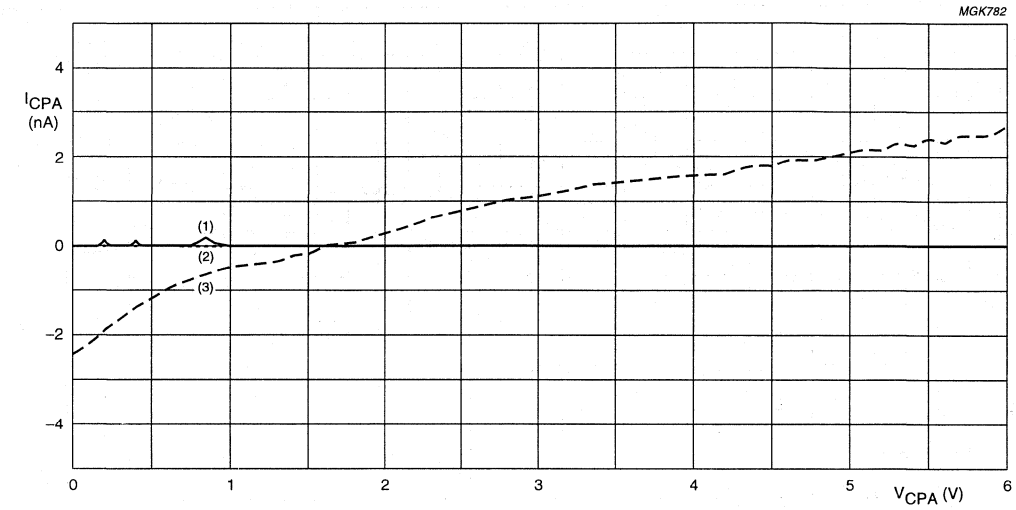
(1) T_{amb} = +90 °C. (2) T_{amb} = +25 °C. (3) T_{amb} = −35 °C.

Fig.4 Typical I_{DD} as a function of V_{DD} with both synthesizers on and voltage doubler disabled.



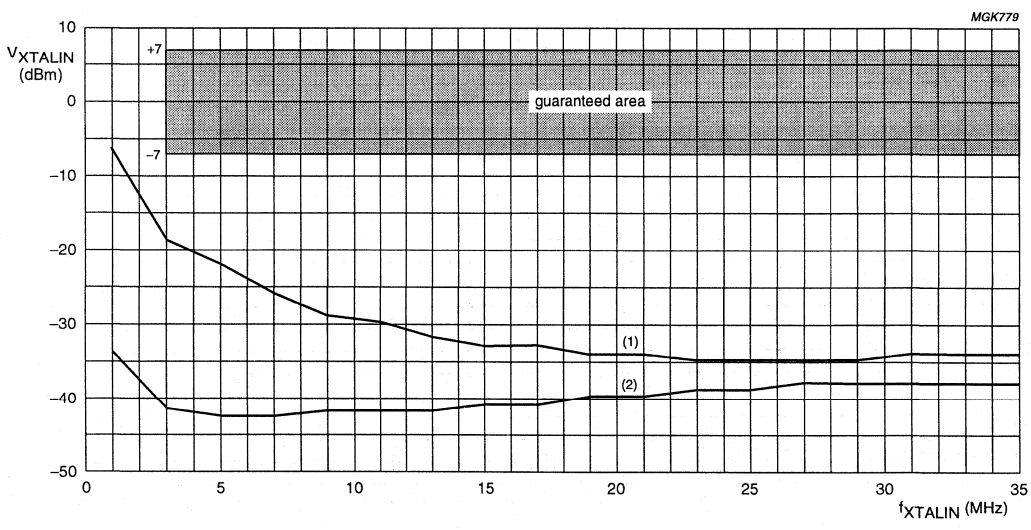
R_{SET} = 15 kΩ;
CRA = 1. (1) V_{CC} = 2.7 V. (2) V_{CC} = 6.0 V.

Fig.5 Typical charge pump current as a function of CPA voltage with T_{amb} = 25 °C.



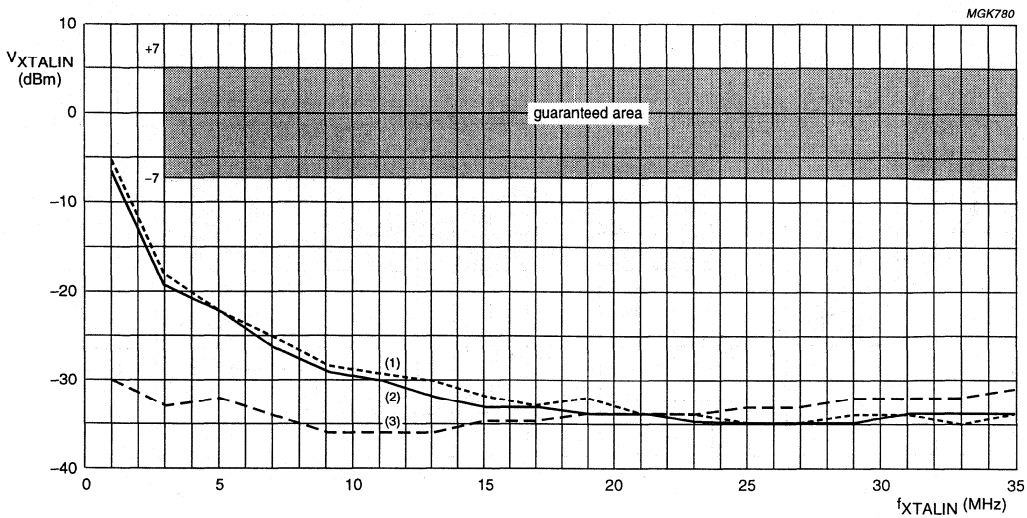
$V_{CC} = V_{DD} = 6$ V; $R_{SET} = 15$ kΩ; CRA = 1. (1) $T_{amb} = +25$ °C. (2) $T_{amb} = -35$ °C. (3) $T_{amb} = +90$ °C.

Fig.6 Typical charge pump 3-state current as a function of CPA voltage.



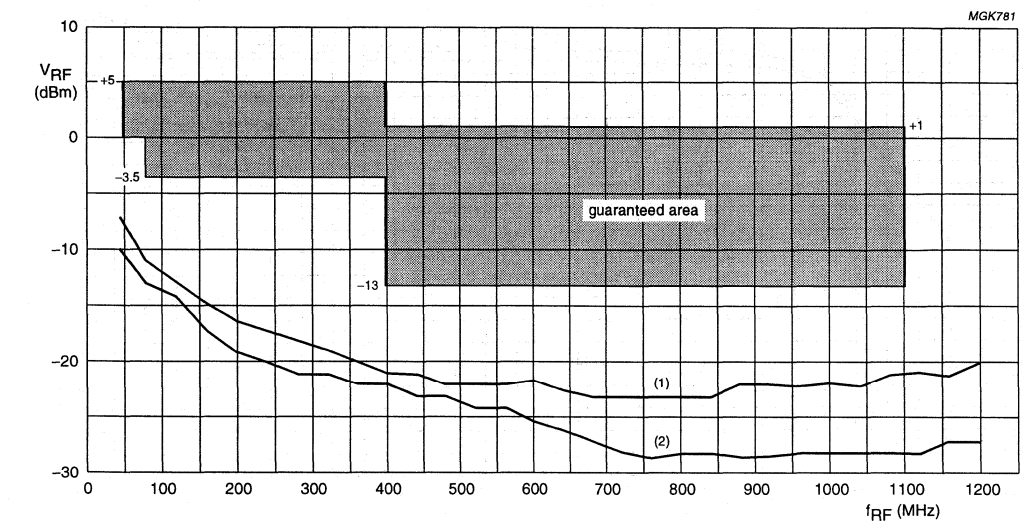
f_{XTALIN} externally terminated by 50 Ω load; AC-coupled. (1) $V_{DD} = 5.5$ V. (2) $V_{DD} = 2.7$ V.

Fig.7 Typical crystal input sensitivity as a function of input frequency with $T_{amb} = 25$ °C.



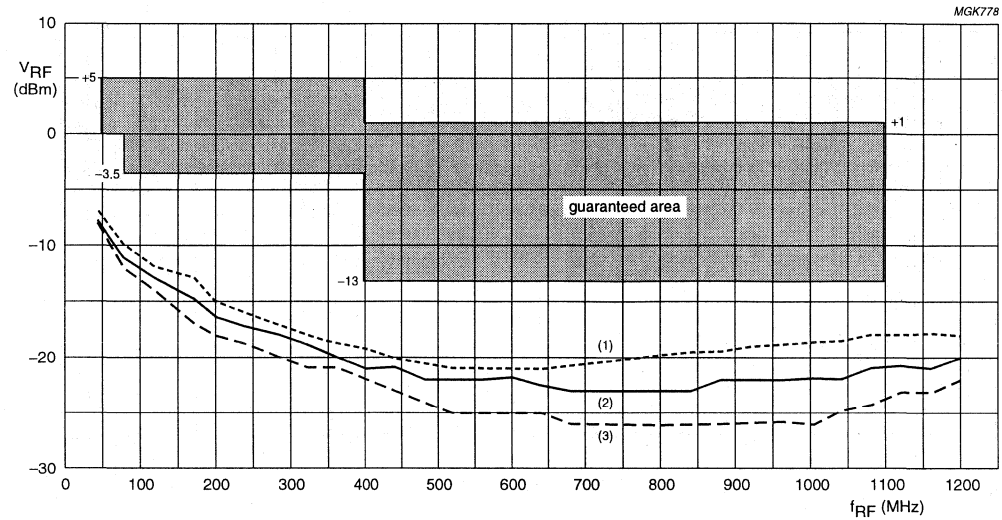
f_{XTALIN} externally terminated by 50 Ω load; AC-coupled. (1) T_{amb} = −35 °C. (2) T_{amb} = +25 °C. (3) T_{amb} = +90 °C.

Fig.8 Typical crystal input sensitivity as a function of input frequency with V_{DD} = 5.5 V.



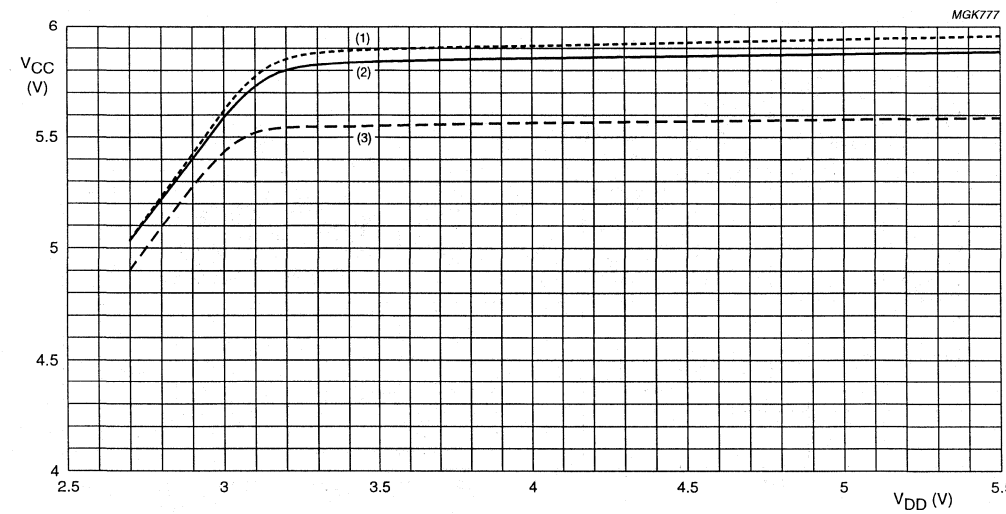
RF input externally terminated by 50 Ω load; AC-coupled. (1) V_{DD} = 5.5 V. (2) V_{DD} = 2.7 V.

Fig.9 Typical RF input sensitivity as a function of input frequency with T_{amb} = 25 °C.



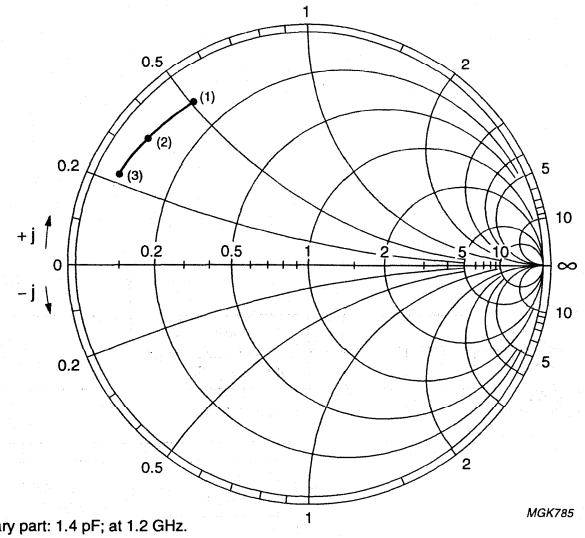
RF input externally terminated by 50 Ω load; AC-coupled. (1) T_{amb} = −35 °C. (2) T_{amb} = +25 °C. (3) T_{amb} = +90 °C.

Fig.10 Typical RF input sensitivity as a function of input frequency with V_{DD} = 5.5 V.



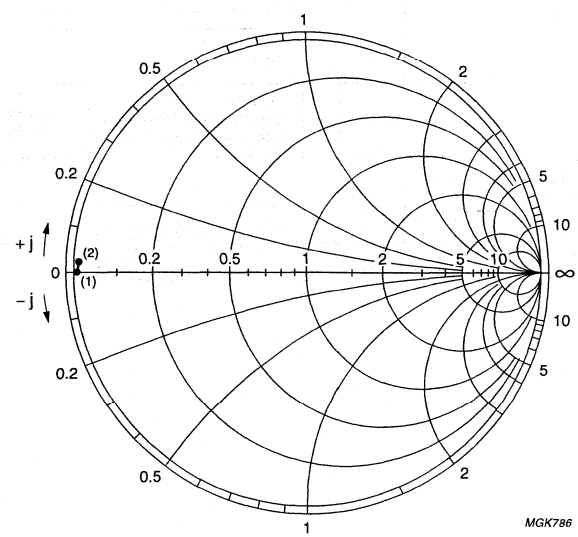
(1) T_{amb} = −35 °C. (2) T_{amb} = +25 °C. (3) T_{amb} = +90 °C.

Fig.11 Typical charge pump supply voltage as a function of V_{DD} voltage with voltage doubler enabled.



(1) Real part: 500 Ω; imaginary part: 1.4 pF; at 1.2 GHz.
(2) Real part: 800 Ω; imaginary part: 1.1 pF; at 1.0 GHz. (3) Real part: 830 Ω; imaginary part: 0.9 pF; at 800 MHz.

Fig.12 Typical RF input admittance (IC powered on).



(1) Real part: 7.8 kΩ; imaginary part: 0.9 pF; at 3 MHz. (2) Real part: 9.8 kΩ; imaginary part: 1.0 pF; at 35 MHz.

Fig.13 Typical crystal input admittance (IC powered on).

APPLICATION INFORMATION

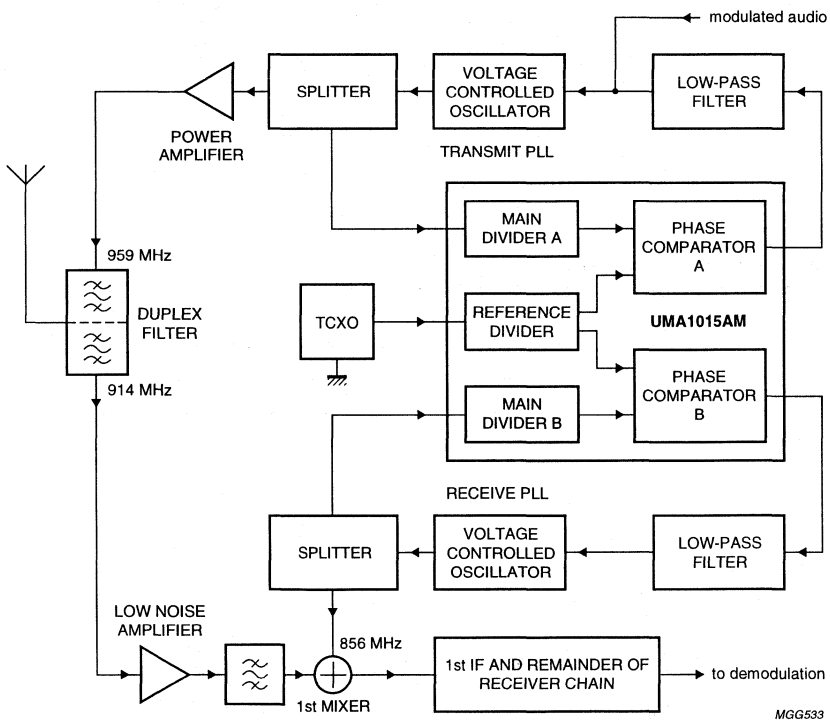


Fig.14 Typical application block diagram.

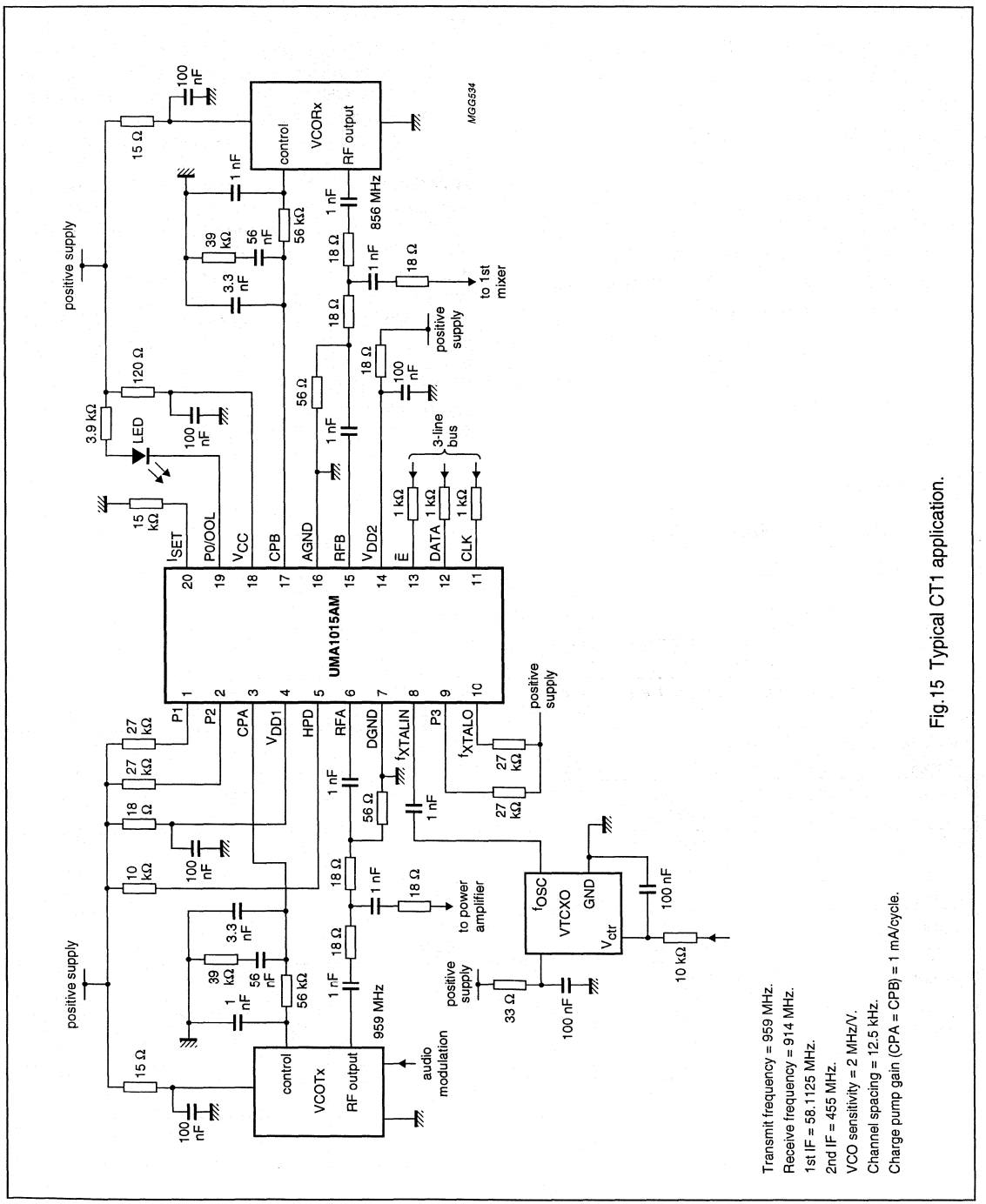


Fig.15 Typical CT1 application.

Transmit frequency = 959 MHz.
Receive frequency = 914 MHz.
1st IF = 58.1125 MHz.
2nd IF = 455 MHz.
VCO sensitivity = 2 MHz/V.
Channel spacing = 12.5 kHz.
Charge pump gain (CPA = CPB) = 1 mA/cycle.

Low-power dual frequency synthesizer for radio communications

UMA1015M

FEATURES

- Two fully programmable RF dividers up to 1.1 GHz
- Fully programmable reference divider up to 35 MHz
- 2 : 1 or 1 : 1 ratio of selectable reference frequencies
- Fast three-line serial bus interface
- Adjustable phase comparator gain
- Programmable out-of-lock indication for both loops
- On-chip voltage doubler
- Low current consumption from 3 V supply
- Separate power-down mode for each synthesizer
- Up to 4 open-drain output ports.

APPLICATIONS

- Cordless telephone
- Hand-held mobile radio.

GENERAL DESCRIPTION

The UMA1015M is a low-power dual frequency synthesizer for radio communications which operates in the 50 to 1100 MHz frequency range. Each synthesizer consists of a fully programmable main divider, a phase and frequency detector and a charge pump. There is a fully programmable reference divider common to both synthesizers which operates up to 35 MHz. The device is programmed via a 3-wire serial bus which operates up to 10 MHz. The charge pump currents (gains) are fixed by an external resistance at pin 20 (I_{SET}). The BiCMOS device is designed to operate from 2.6 V (3 Ni-Cd cells) to 5.5 V at low current. Digital supplies V_{DD1} and V_{DD2} must be at the same potential. The charge pump supply (V_{CC}) can be provided by an external source or on-chip voltage doubler. V_{CC} must be equal to or higher than V_{DD1}. Each synthesizer can be powered-down independently via the serial bus to save current. It is also possible to power-down the device via the HPD input (pin 5).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD1}, V_{DD2}	digital supply voltage	$V_{DD1} = V_{DD2}$	2.6	–	5.5	V
V_{CC}	charge pump supply voltage	external supply; doubler disabled; $V_{CC} \geq V_{DD}$	2.6	–	6.0	V
V_{CCvd}	charge pump supply from voltage doubler	doubler enabled	–	$2V_{DD1} - 0.6$	6.0	V
$I_{DDO1} + I_{DDO2} + I_{CCO}$	operating supply current	both synthesizers ON; doubler disabled; $V_{DD1} = V_{DD2} = 5.5$ V	–	9.6	–	mA
$I_{DD1pd} + I_{DD2pd} + I_{CCpd}$	current in power-down mode per supply	doubler disabled; $V_{DD1} = V_{DD2} = 5.5$ V	–	0.01	–	mA
I_{DD1pd}	current in power-down mode from supply V_{DD}	doubler enabled; $V_{DD1} = V_{DD2} = 3$ V	–	0.15	–	mA
f_{RFA}, f_{RFB}	RF input frequency for each synthesizer		50	–	1100	MHz
f_{XTALIN}	crystal input frequency		3	–	35	MHz
$f_{pc(min)}$	minimum phase comparator frequency	f_{RF} = 50 to 1100 MHz; f_{XTALIN} = 3 to 35 MHz	–	10	–	kHz
$f_{pc(max)}$	maximum phase comparator frequency	f_{RF} = 50 to 1100 MHz; f_{XTALIN} = 3 to 35 MHz	–	750	–	kHz
T_{amb}	operating ambient temperature	synthesizer A $2.6 \text{ V} \leq V_{DD} \leq 5.5$ V	−30	–	+85	°C
		synthesizer B $2.6 \text{ V} \leq V_{DD} \leq 4.5$ V	−30	–	+85	°C
		synthesizer B $2.6 \text{ V} \leq V_{DD} \leq 5.0$ V	0	–	+85	°C

Low-power dual frequency synthesizer for radio communications

UMA1015M

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
UMA1015M/C2	20	SSOP20	plastic	SOT266-1

BLOCK DIAGRAM

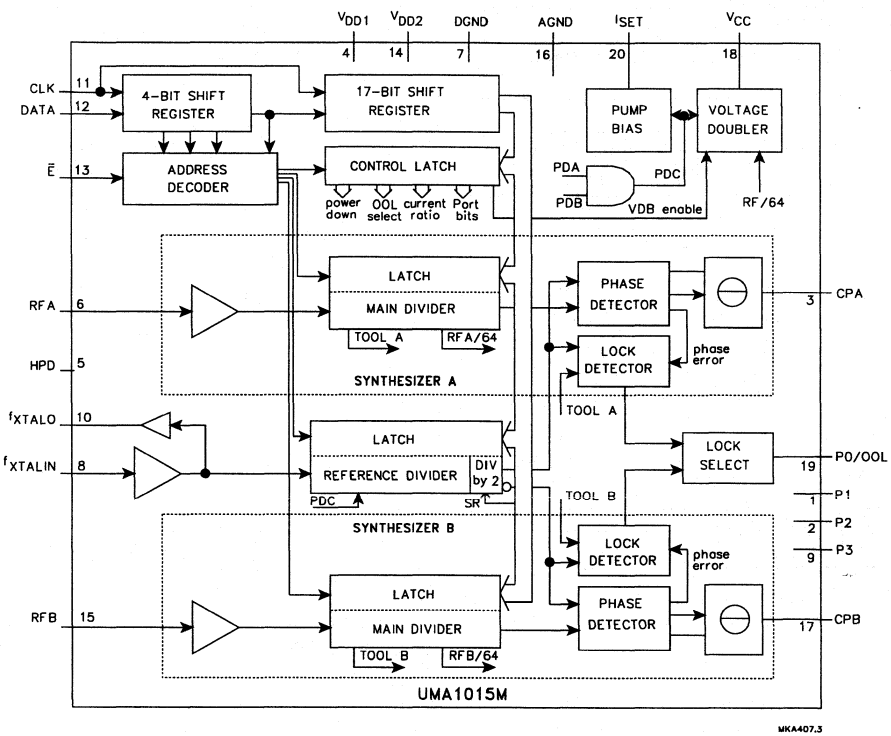


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
P1	1	output Port 1
P2	2	output Port 2
CPA	3	charge-pump output synthesizer A
V_{DD1}	4	digital supply voltage 1
HPD	5	hardware power-down (input LOW = power-down)
RFA	6	RF input synthesizer A
DGND	7	digital ground
f_{XTALIN}	8	common crystal frequency input from TCXO
P3	9	output Port 3
f_{XTALO}	10	open-drain output of f_{XTAL} signal
CLK	11	programming bus clock input
DATA	12	programming bus data input
$\overline{E}$	13	programming bus enable input (active LOW)
V_{DD2}	14	digital supply voltage 2
RFB	15	RF input synthesizer B
AGND	16	analog ground to charge pumps
CPB	17	charge pump output synthesizer B
V_{CC}	18	analog supply to charge pump; external or voltage doubler output
P0/OOL	19	Port output 0/out-of-lock output
I_{SET}	20	regulator pin to set charge-pump currents

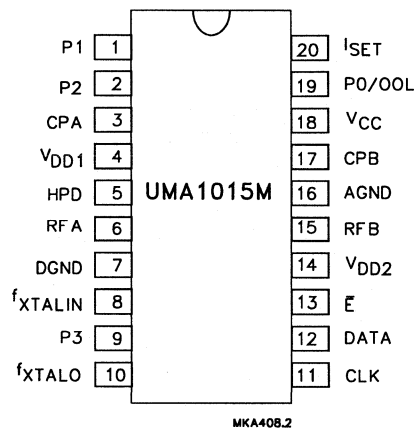


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Main dividers

Each synthesizer has a fully programmable 17-bit main divider. The RF input drives a pre-amplifier to provide the clock to the first divider bit. The pre-amplifier has a high input impedance, dominated by pin and pad capacitance. The circuit operates with signal levels from below 50 mV (RMS) up to 250 mV (RMS), and at frequencies up to 1.1 GHz. The high frequency sections of the divider are implemented using bipolar transistors, while the slower section uses CMOS technology. The range of division ratios is 512 to 131071.

Reference divider

There is a common fully programmable 12-bit reference divider for the two synthesizers. The input f_{XTALIN} drives a pre-amplifier to provide the clock input for the reference divider. This clock signal is also buffered and output on pin f_{XTALO} (open drain). An extra divide-by-2 block allows a reference comparison frequency for synthesizer B to be half that of synthesizer A. This feature is selectable using the program bit SR. If the programmed reference divider ratio is R then the ratio for each synthesizer is as given in Table 1.

The range for the division ratio R is 8 to 4095. Opposite edges of the divider output are used to drive the phase detectors to ensure that active edges arrive at the phase detectors of each synthesizer at different times. This minimizes the potential for interference between the charge pumps of each loop. The reference divider consists of CMOS devices operating beyond 35 MHz.

Table 1 Synthesizer ratio of reference divider

SR	SYNTHESIZER A	SYNTHESIZER B
0	R	R
1	R	2R

Phase comparators

For each synthesizer, the outputs of the main and reference dividers drive a phase comparator where a charge pump produces phase error current pulses for integration in an external loop filter. The charge pump current is set by an external resistance R_{SET} at pin I_{SET}, where a temperature-independent voltage of 1.2 V is generated. R_{SET} should be between 12 kΩ and 60 kΩ (to give an I_{SET} of 100 μA and 20 μA respectively).
The charge-pump current, I_{CP}, can be programmed to be either ($12 \times I_{SET}$) or ($24 \times I_{SET}$) with the maximum being 2.4 mA. The dead zone, caused by finite switching of current pulses, is cancelled by an internal delay in the phase detector thus giving improved linearity. The charge pump has a separate supply, V_{CC}, which helps to reduce the interference on the charge pump output from other parts of the circuit. Also, V_{CC} can be higher than V_{DD1} if a wider range on the VCO input is required. V_{CC} must not be less than V_{DD1}.

Voltage doubler

If required, there is a voltage doubler on-chip to supply the charge pumps at a higher level than the nominal available supply. The doubler operates from the digital supply V_{DD1}, and is internally limited to a maximum output of 6 V.
An external capacitor is required on pin V_{CC} for smoothing, the capacitor required to develop the extra voltage is integrated on-chip. To minimize the noise being introduced to the charge pump output from the voltage doubler, the doubler clock is suppressed (provided both loops are in-lock) for the short time that the charge pumps are active. The doubler clock (RF/64) is derived from whichever main divider is operating (synthesizer A has priority). While both synthesizers are powered down (and the doubler is enabled), the doubler clock is supplied by a low-current internal oscillator. The doubler can be disabled by programming the bit VDON to logic 0, in order to allow an external charge pump supply to be used.

Out-of-lock indication/output ports

There is a lock detector on-chip for each synthesizer. The lock condition of each, or both loops, is output via an open-drain transistor which drives the pin P0/OOL (when out-of-lock, the transistor is turned on and therefore the output is forced LOW). The lock condition output is software selectable (see Table 4). An out-of-lock condition is flagged when the phase error is greater than T_{OOL}, the value of which is approximately equal to 80 cycles of the relevant RF input. The out-of-lock flag is only released after 8 consecutive reference cycles where the phase error is less than T_{OOL}. The out-of-lock function can be disabled, via the serial bus, and the pin P0/OOL can be used as an output port. Three other port outputs P1, P2 and P3 (open-drain transistors) are also available.

Serial programming bus

A simple 3-line unidirectional serial bus is used to program the circuit. The 3 lines are DATA, CLK and $\overline{E}$ (enable). The data sent to the device is loaded in bursts framed by $\overline{E}$. Programming clock edges are ignored until $\overline{E}$ goes active LOW. The programmed information is loaded into the addressed latch when $\overline{E}$ returns inactive HIGH. This is allowed when CLK is in either state without causing any consequences to the register data. Only the last 21 bits serially clocked into the device are retained within the programming register. Additional leading bits are ignored, and no check is made on the number of clock pulses. The fully static CMOS design uses virtually no current when the bus is inactive. It can always capture new programming data even during power-down of both synthesizers.

However when either synthesizer A or synthesizer B or both are powered-on, the presence of a TCXO signal is required at pin 8 (f_{XTALIN}) for correct programming.

Data format

Data is entered with the most significant bit first. The leading bits make up the data field, while the trailing four bits are an address field. The address bits are decoded on the rising edge of $\overline{E}$. This produces an internal load pulse to store the data in the addressed latch. To ensure that data is correctly loaded on first power-up, $\overline{E}$ should be held LOW and only taken HIGH after having programmed an appropriate register. To avoid erroneous divider ratios, the pulse is inhibited during the period when data is read by the frequency dividers. This condition is guaranteed by respecting a minimum $\overline{E}$ pulse width after data transfer. The data format and register bit allocations are shown in Table 2.

Table 2 Bit allocation

FIRST	REGISTER BIT ALLOCATION																			LAST
p1	p2	p3	p4	p5	p6	p7	p8	p9	p10	p11	p12	p13	p14	p15	p16	p17	p18	p19	p20	p21
dt16	dt15	dt14	dt13	dt12	DATA FIELD							dt4	dt3	dt2	dt1	dt0	ADDRESS			
X	X	VDON	PO	OLA	OLB	CRA	CRB	X	X	sPDA	sPDB	P3	P2	P1	X	X	0	0	0	1
MA16	SYNTHESIZER A MAIN DIVIDER COEFFICIENT															MA0	0	1	0	0
0	0	0	0	SR	R11	REFERENCE DIVIDER COEFFICIENT										R0	0	1	0	1
MB16	SYNTHESIZER B MAIN DIVIDER COEFFICIENT															MB0	0	1	1	0
RESERVED FOR TEST(1)																	0	0	0	0

Note

1. The test register should not be programmed with any other values except all zeros for normal operation.

Table 3 Bit allocation description

SYMBOL	DESCRIPTION
sPDA, sPDB	software power-down for synthesizers A and B (0 = power-down)
P3, P2, P1 and P0	bits output to pins 1, 2, 9 and 19 (1 = high impedance)
VDON	voltage doubler enable (1 = doubler enabled)
OLA, OLB	out-of-lock select; selects signal output to pin 19 (see Table 4)
CRA, CRB	charge pump A/B current to I_{SET} ratio select (see Table 5)
SR	reference frequency ratio select (see Table 6)

Table 4 Out-of-lock select

OLA	OLB	OUTPUT AT PIN 19
0	0	P0
0	1	lock status of loop B; OOLB
1	0	lock status of loop A; OOLA
1	1	logic OR function of loops A and B

Table 5 Charge pump current ratio

CRA/CRB	CURRENT AT PUMP
0	$I_{CP} = 12 \times I_{SET}$
1	$I_{CP} = 24 \times I_{SET}$

Table 6 Reference division ratio

SR	SYNTHESIZER A	SYNTHESIZER B
0	R	R
1	R	2R

Power-down modes

The device can be powered down either via pin HPD (active LOW = power-down) or via the serial bus (bits SPDA and SPDB, logic 0 = power-down). The synthesizers are powered up when both hardware and software Power-down signals are at logic 1. When only one synthesizer is powered down, the functions common to both will be maintained. When both synthesizers are switched off, only the voltage doubler (if enabled) will remain active drawing a reduced current. An internal oscillator will drive the doubler in this situation. If both synthesizers have been in a power-down condition, then when one or both synthesizers are reactivated, the reference and main dividers restart in such a way as to avoid large random phase errors at the phase comparator.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD1}, V_{DD2}	DC range of digital power supply voltage with respect to DGND	−0.3	+6.0	V
V_{CC}	DC charge pump supply voltage with respect to AGND	−0.3	+6.0	V
ΔV_{CC-DD}	difference in voltage between V_{CC} and V_{DD1}, V_{DD2}	−0.3	+6.0	V
V_n	DC voltage at pins 1, 2, 5, 6, 8 to 15, 19 and 20 with respect to DGND	−0.3	V_{DD1} + 0.3	V
$V_{3, 17}$	DC voltage at pins 3 and 17 with respect to AGND	−0.3	V_{CC} + 0.3	V
ΔV_{GND}	difference in voltage between AGND and DGND (these pins should be connected together)	−0.3	+0.3	V
T_{stg}	storage temperature	−55	+125	°C
T_{amb}	operating ambient temperature	−30	+85	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

CHARACTERISTICS

$V_{DD1} = V_{DD2} = 2.6$ to 5.5 V; $V_{CC} = 2.6$ to 6.0 V; $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply; (V_{DD1}, V_{DD2} and V_{CC}) voltage doubler disabled, external supply on V_{CC}						
V_{DD1}, V_{DD2}	digital supply voltage	$V_{DD1} = V_{DD2}$	2.6	–	5.5	V
$I_{DD1} + I_{DD2}$	total digital supply current from V_{DD1} and V_{DD2}	f_{XTAL} = 12.8 MHz; both synthesizers on; $V_{DD1} = V_{DD2} = 3$ V	–	8.5	–	mA
		f_{XTAL} = 12.8 MHz; both synthesizers on; $V_{DD1} = V_{DD2} = 5.5$ V	–	–	12.5	mA
I_{DDpda}, I_{DDpdb}	total digital supply current from V_{DD1} and V_{DD2} with one synthesizer in power-down mode	f_{XTAL} = 12.8 MHz; one synthesizer powered down; $V_{DD1} = V_{DD2} = 3$ V	–	5.5	–	mA
		f_{XTAL} = 12.8 MHz; one synthesizer powered down; $V_{DD1} = V_{DD2} = 5.5$ V	–	–	7.5	mA
I_{DDpd}	digital supply current in power-down mode	both synthesizers powered down; $V_{HPD} = 0$ V	–	–	60	µA
V_{CC}	charge pump supply voltage	$V_{CC} \geq V_{DD}$	2.6	–	6.0	V
I_{CC}	charge pump supply current	both synthesizers on and in lock; f_{ref} = 12.5 kHz	–	–	25	µA
I_{CCpd}	charge pump supply current in power-down mode	both synthesizers powered down	–	–	25	µA
Voltage doubler enabled						
I_{DD}	total digital supply current from V_{DD1} and V_{DD2}	f_{XTAL} = 12.8 MHz; both synthesizers on and in lock; $V_{DD1} = 3$ V; $f_{doubler}$ = 16 MHz	–	8.5	12	mA
I_{DDpd}	total digital supply current in power-down mode from V_{DD1} and V_{DD2}	both synthesizers powered down; $V_{DD1} = 3$ V; $V_{HPD} = 0$ V	–	0.25	0.4	mA
V_{CCvd}	charge pump supply voltage	DC current drawn from V_{CC} = 50 µA	$2V_{DD1} - 1.2$	$2V_{DD1} - 0.6$	6.0	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RF main divider input; RFA and RFB						
f_{RF}	RF input frequency		50	–	1100	MHz
$V_{RF(rms)}$	RF input signal voltage (RMS value; AC coupled)	R_s = 50 Ω; $V_{DD1} = V_{DD2}$ = 2.6 to 3.5 V; f_{RF} = 400 to 1100 MHz	50	–	250	mV
		R_s = 50 Ω; $V_{DD1} = V_{DD2}$ = 3.5 to 5.5 V; f_{RF} = 400 to 1100 MHz	100	–	250	mV
		R_s = 50 Ω; $V_{DD1} = V_{DD2}$ = 2.6 to 5.5 V; f_{RF} = 50 to 400 MHz	150	–	400	mV
Z_I	input impedance (real part)	f_{RF} = 1 GHz; indicative, not tested	–	300	–	Ω
C_I	input capacitance	indicative, not tested	–	1	–	pF
R_{pm}	principle main divider ratio		512	–	131071	
Reference divider input; f_{XTALIN}						
f_{XTALIN}	reference input frequency from crystal		3	–	35	MHz
$V_{XTALIN(rms)}$	sinusoidal input voltage (RMS value)		100	–	500	mV
Z_I	input impedance (real part)	f_{XTALIN} = 12.8 MHz; indicative, not tested	–	10	–	kΩ
C_I	input capacitance	indicative, not tested	–	1	–	pF
R_{rd}	reference divider ratio		8	–	4095	
Charge pump current setting resistor input; I_{SET}						
V_{SET}	voltage output on I_{SET}	R_{SET} = 12 to 60 kΩ	–	1.2	–	V
Charge pump outputs; CPA and CPB						
I_{CP}	charge pump sink or source current	R_{SET} = 15 kΩ; CRA/CRB = logic 1; $I_{cp} = I_{SET} \times 24$; V_{cp} = 0.4 V to V_{CC} – 0.5 V	1.4	1.9	2.4	mA
		R_{SET} = 15 kΩ; CRA/CRB = logic 0; $I_{cp} = I_{SET} \times 12$; V_{cp} = 0.4 V to V_{CC} – 0.5 V	0.7	0.96	1.2	mA
I_{LI}	charge pump off leakage current	$V_{cp} = 0.5V_{CC}$	–5	–	+5	nA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Logic input signal levels; DATA, CLK, $\overline{E}$ and HPD						
V_{IH}	HIGH level input voltage	at logic 1	$0.7V_{DD1}$	–	$V_{DD1} + 0.3$	V
V_{IL}	LOW level input voltage	at logic 0	–0.3	–	$0.3V_{DD1}$	V
I_{bias}	input bias currents	at logic 1 or logic 0	–5	–	+5	μA
C_I	input capacitance	indicative, not tested	–	1	–	pF
Port outputs/Out-of-lock; P0/OOL, P1, P2, P3 and f_{XTALO} - open drain outputs						
V_{OL}	LOW level output voltage	I_{sink} = 0.4 mA	–	–	0.4	V

SERIAL TIMING CHARACTERISTICS

V_{DD1} = 3 V; T_{amb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Serial programming clock; CLK					
t_r, t_f	input rise and fall times	–	10	40	ns
t_{cy}	clock period	100	–	–	ns
Enable programming; $\overline{E}$					
t_{START}	delay to rising clock edge	40	–	–	ns
t_{END}	delay from last falling clock edge	–20	–	–	ns
t_W	minimum inactive pulse width	4000	–	–	ns
$t_{SU;\overline{E}}$	enable set-up time to next clock edge	20	–	–	ns
Register serial input data; DATA					
$t_{SU;DAT}$	input data to clock set-up time	20	–	–	ns
$t_{HD;DAT}$	input data to clock hold time	20	–	–	ns

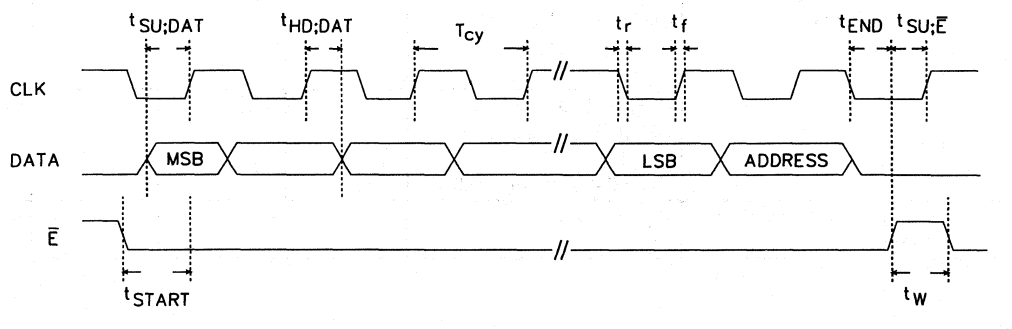
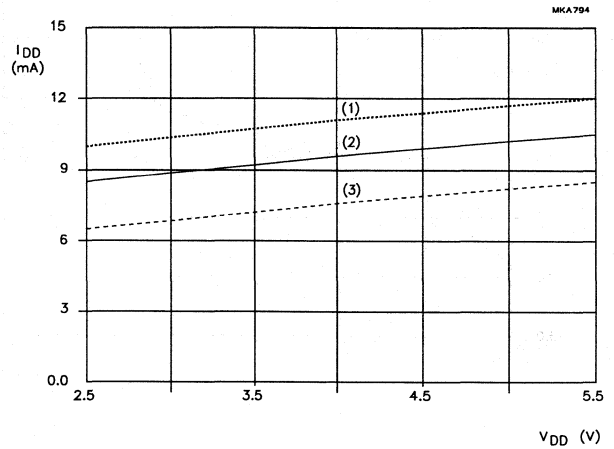


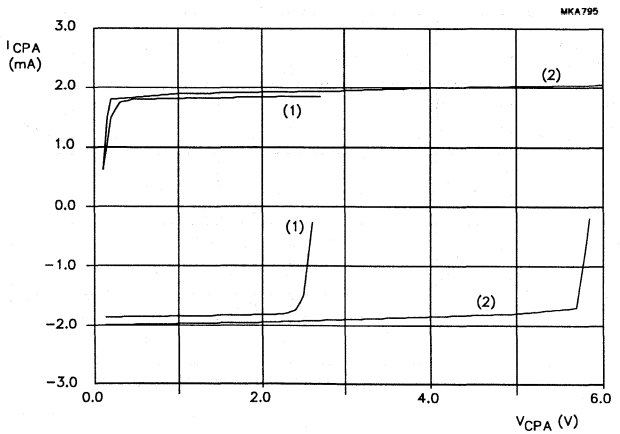
Fig.3 Serial bus timing diagram.

TYPICAL PERFORMANCE CHARACTERISTICS



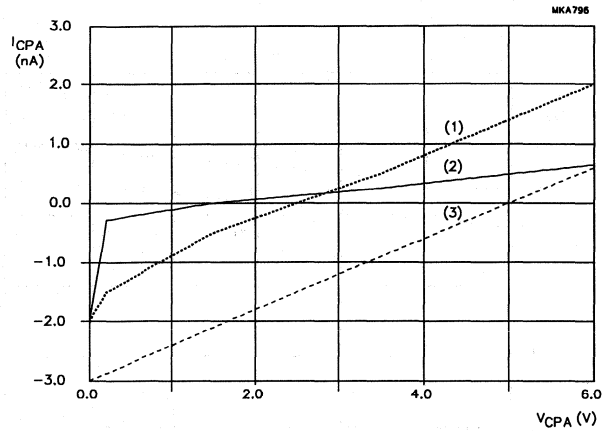
(1) T_{amb} = +85 °C.
(2) T_{amb} = +25 °C.
(3) T_{amb} = −30 °C.

Fig.4 I_{DD} as a function of V_{DD} with both synthesizers on and voltage doubler disabled.



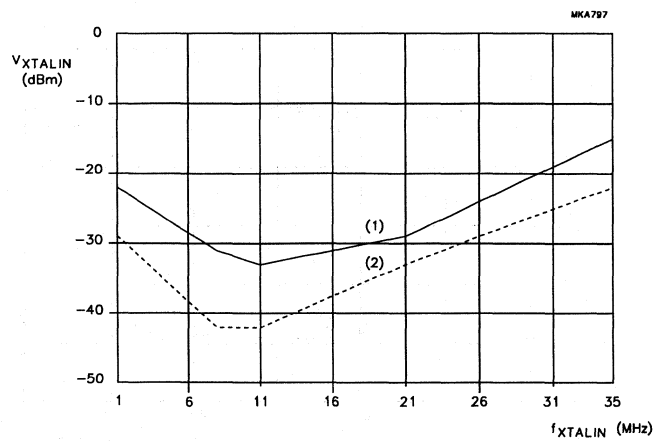
R_{SET} = 15 kΩ; CRA = 1.
(1) V_{CC} = 2.7 V.
(2) V_{CC} = 6.0 V.

Fig.5 Charge pump current as a function of CPA voltage.



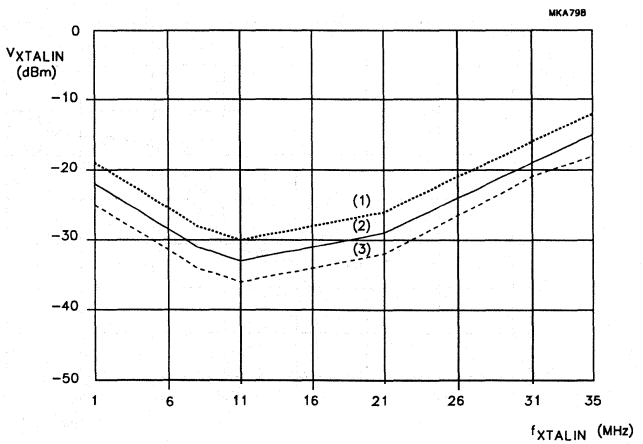
R_{SET} = 15 kΩ; CRA = 1.
(1) T_{amb} = +85 °C.
(2) T_{amb} = +25 °C.
(3) T_{amb} = −30 °C.

Fig.6 Charge pump 3-state current as a function of CPA voltage.



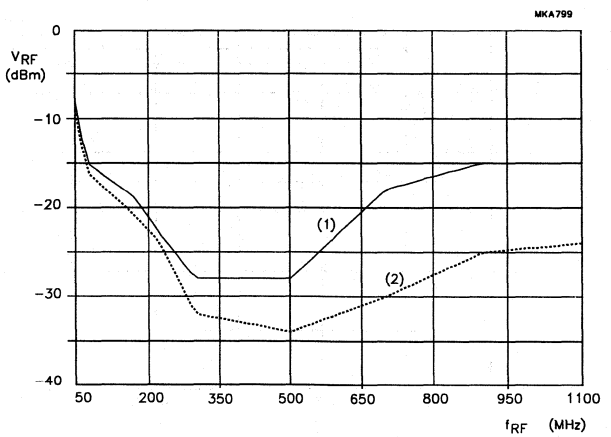
f_{XTALIN} externally terminated by 50 Ω load; AC-coupled.
(1) V_{DD} = 5.5 V.
(2) V_{DD} = 2.7 V.

Fig.7 Crystal input sensitivity as a function of input frequency.



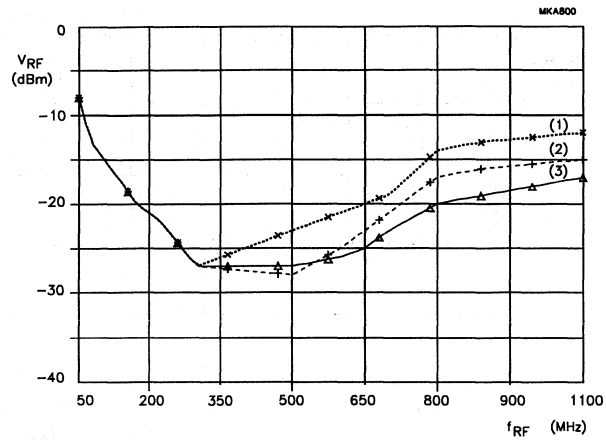
f_{XTALIN} externally terminated by 50 Ω load; AC-coupled.
(1) T_{amb} = −30 °C.
(2) T_{amb} = +25 °C.
(3) T_{amb} = +85 °C.

Fig.8 Crystal input sensitivity as a function of input frequency with V_{DD} = 5.5 V.



RF input externally terminated by 50 Ω load; AC-coupled.
(1) V_{DD} = 5.5 V.
(2) V_{DD} = 2.7 V.

Fig.9 RF input sensitivity as a function of input frequency.



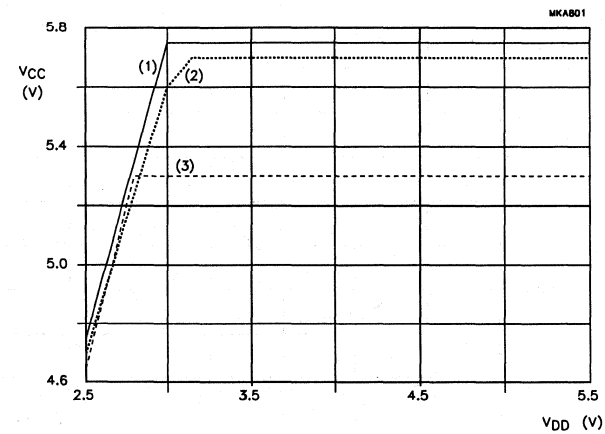
RF input externally terminated by 50 Ω load; AC-coupled.

(1) T_{amb} = −30 °C.

(2) T_{amb} = +25 °C.

(3) T_{amb} = +85 °C.

Fig.10 RF input sensitivity as a function of input frequency with V_{DD} = 5.5 V.

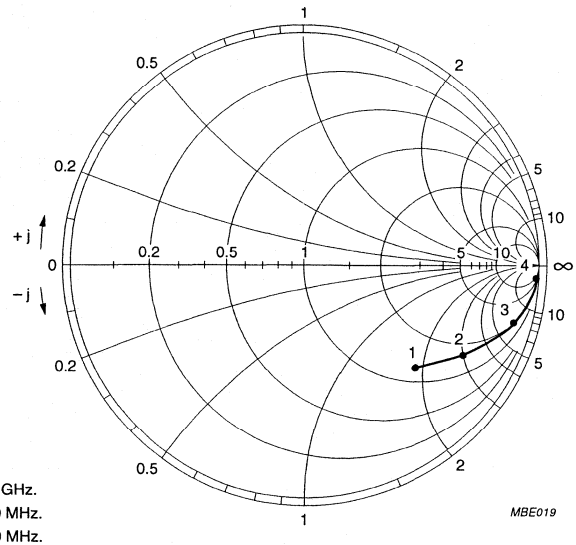


(1) T_{amb} = −30 °C.

(2) T_{amb} = +25 °C.

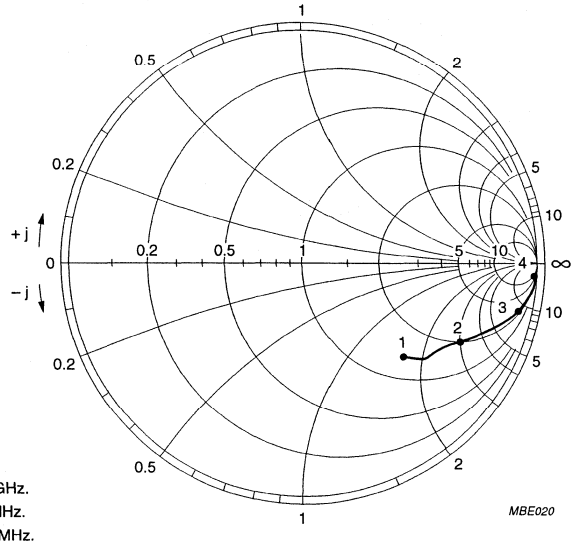
(3) T_{amb} = +85 °C.

Fig.11 Typical charge pump supply voltage as a function of V_{DD} voltage with voltage doubler enabled.



(1) 68.316 Ω, −92.457 Ω at 1.1 GHz.
(2) 85.914 Ω, −152.08 Ω at 800 MHz.
(3) 102.83 Ω, −354.66 Ω at 400 MHz.
(4) 853.75 Ω, −2.7735 kΩ at 50 MHz.

Fig.12 Input impedance as a function of input frequency; synthesizer A.



(1) 69.293 Ω, −78.027 Ω at 1.1 GHz.
(2) 100.2 Ω, −148.37 Ω at 800 MHz.
(3) 128.22 Ω, −378.81 Ω at 400 MHz.
(4) 674.25 Ω, −3.06 kΩ at 50 MHz.

Fig.13 Input impedance as a function of input frequency; synthesizer B.

APPLICATION INFORMATION

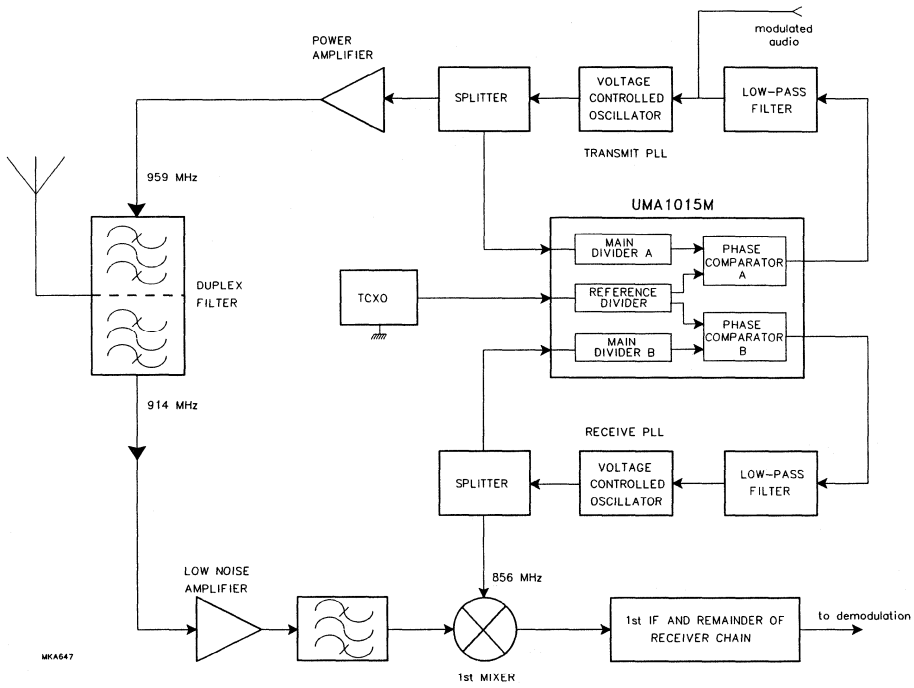


Fig.14 Typical application block diagram.

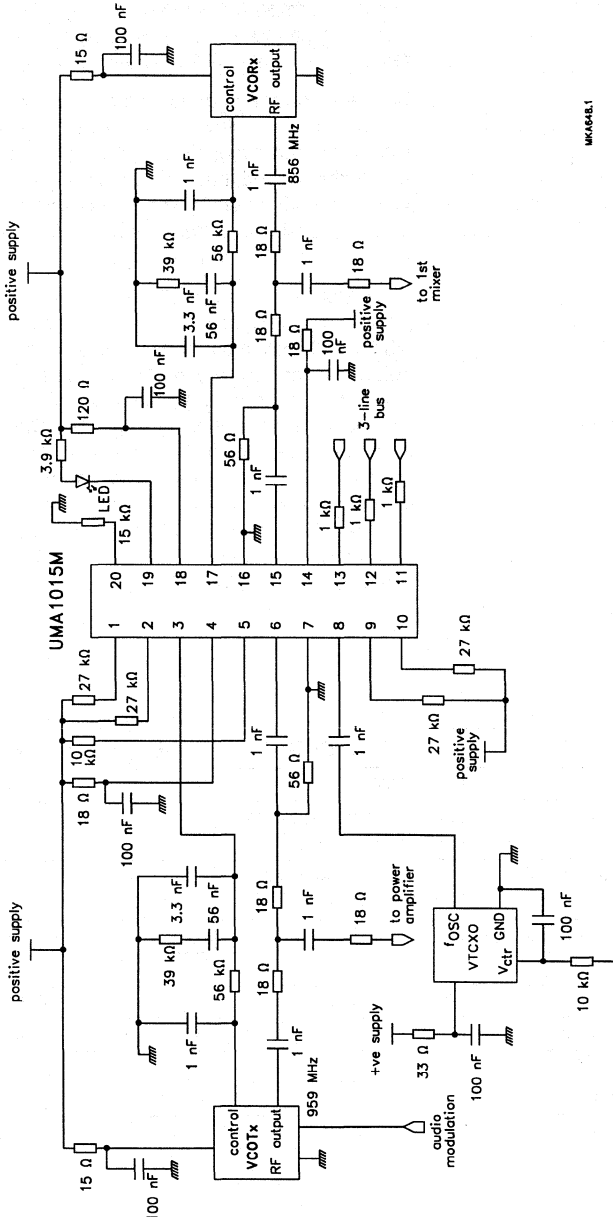


Fig.15 Typical CT1 application.

Transmit frequency = 959 MHz.
Receive frequency = 914 MHz.
1st IF = 58.1125 MHz.
2nd IF = 455 MHz.
VCO sensitivity = 2 MHz/V.
Channel spacing = 12.5 kHz.
Charge pump gain (CPA = CPB) = 1 mA/cycle.

Low-voltage dual frequency synthesizer for radio telephones

UMA1018M

FEATURES

- Low current from 3 V supply
- Fully programmable RF divider
- 3-line serial interface bus
- Second synthesizer to control first IF or offset loop frequency
- Independent fully programmable reference dividers for each loop, driven from external crystal oscillator
- Dual phase detector outputs to allow fast frequency switching
- Integrated digital-to-analog converter
- Dual power-down modes.

APPLICATIONS

- 900 MHz mobile telephones
- Portable battery-powered radio equipment.

GENERAL DESCRIPTION

The UMA1018M BICMOS device integrates prescalers, programmable dividers, and phase comparators to implement two phase-locked loops. The device is designed to operate from 3 NiCd cells, in pocket phones, with low current and nominal 5 V supplies.

The principal synthesizer operates at RF input frequencies up to1.25 GHz the auxiliary synthesizer operates at 300 MHz. The auxiliary loop is intended for the first IF or to transmit offset loop-frequency settings. Each synthesizer has a fully programmable reference divider. All divider ratios are supplied via a 3-wire serial programming bus.

Separate power and ground pins are provided to the analog and digital circuits. The ground leads should be externally short-circuited to prevent large currents flowing across the die and thus causing damage. Digital supplies V_{DD1} and V_{DD2} must also be at the same potential. V_{CC} must be equal to or greater than V_{DD} (i.e. V_{DD} = 3 V and V_{CC} = 5 V for wider tuning range).

The principal synthesizer phase detector uses two charge pumps, one provides normal loop feedback, while the other is only active during fast mode to speed-up switching. The auxiliary loop has a separate phase detector. All charge pump currents (gain) are fixed by an external resistance at pin I_{SET} (pin 14). Only passive loop filters are used; the charge-pumps function within a wide voltage compliance range to improve the overall system performance. An on-chip 7-bit DAC enables adjustment of an external function, such as the temperature compensation of a crystal oscillator in Global System for Mobile communications (GSM).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}, V_{DD}	supply voltage	$V_{CC} \geq V_{DD}$	2.7	–	5.5	V
$I_{CC} + I_{DD}$	principal synthesizer supply current	auxiliary synthesizer in power-down mode	–	7.7	–	mA
	principal and auxiliary synthesizer supply current	principal and auxiliary synthesizers ON	–	10	–	mA
I_{CCPD}, I_{DDPD}	current in power-down mode per supply		–	12	–	µA
f_{VCO}	principal input frequency		50	–	1250	MHz
f_{AI}	auxiliary input frequency		20	–	300	MHz
f_{XTAL}	crystal reference input frequency		3	–	40	MHz
f_{PPC}	principal phase comparator frequency		–	200	–	kHz
f_{APC}	auxiliary phase comparator frequency		–	200	–	kHz
T_{amb}	operating ambient temperature		–30	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UMA1018M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

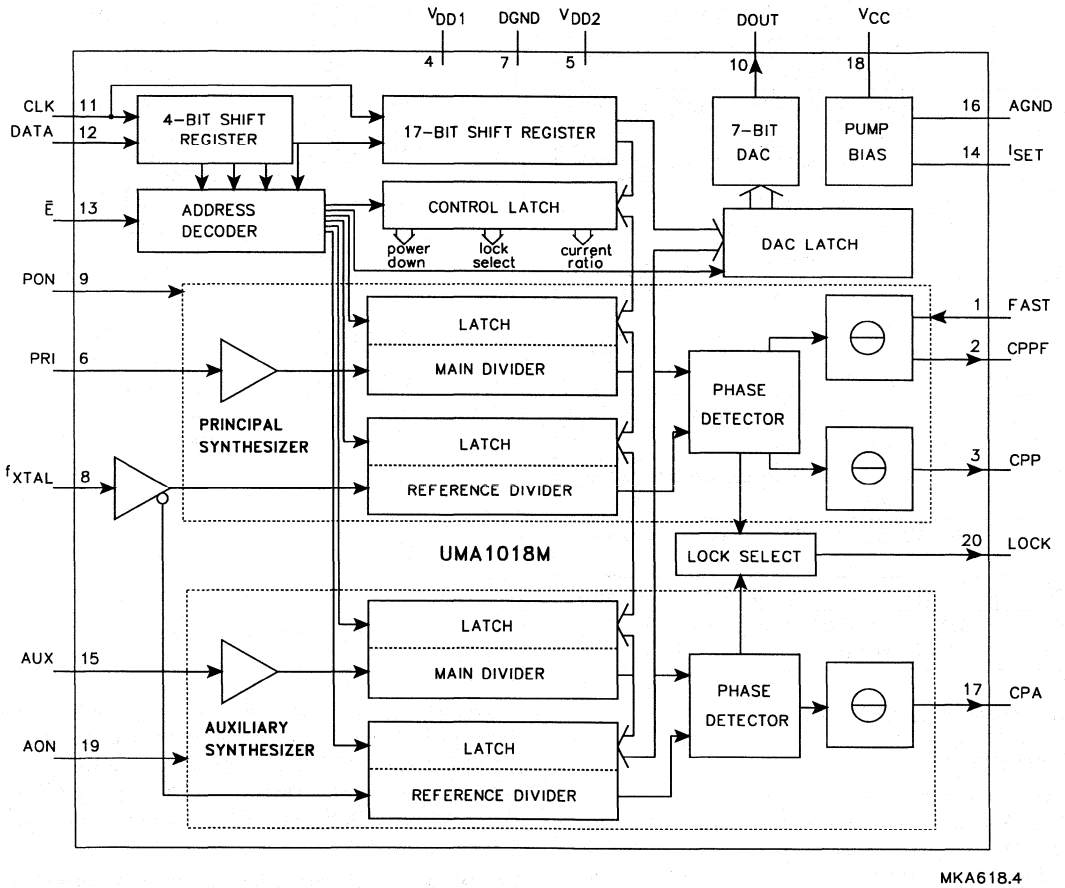


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
FAST	1	control input to speed-up main synthesizer
CPPF	2	principal synthesizer speed-up charge-pump output
CPP	3	principal synthesizer normal charge-pump output
V_{DD1}	4	digital power supply 1
V_{DD2}	5	digital power supply 2
PRI	6	1 GHz principal synthesizer frequency input
DGND	7	digital ground
f_{XTAL}	8	common crystal frequency input from TCXO
PON	9	principal synthesizer power-on input
DOUT	10	7-bit digital-to-analog output
CLK	11	Programming bus clock input
DATA	12	programming bus data input
$\overline{E}$	13	programming bus enable input (active LOW)
I_{SET}	14	regulator pin to set the charge-pump currents
AUX	15	auxiliary synthesizer frequency input
AGND	16	analog ground
CPA	17	auxiliary synthesizer charge-pump output
V_{CC}	18	supply for charge-pump and DAC circuits
AON	19	auxiliary synthesizer power-on input
LOCK	20	in-lock detect output (main PLL); test mode output

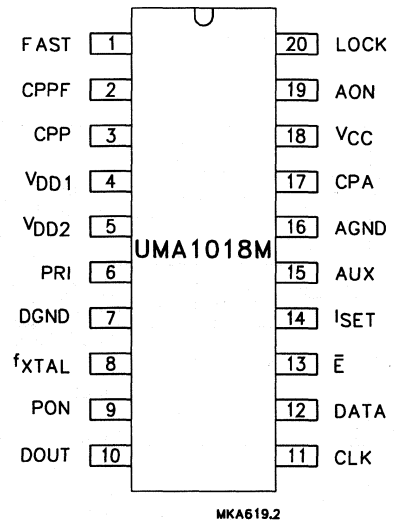


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Principal synthesizer

Programmable reference and main dividers drive the principal PLL phase detector. Two charge pumps produce phase error current pulses for integration in an external loop filter. A hardwired power-down input PON (pin 9) ensures that the dividers and phase comparator circuits can be disabled.

The PRI input (pin 6) drives a pre-amplifier to provide the clock to the first divider stage. The pre-amplifier has a high input impedance, dominated by pin and pad capacitance. The circuit operates with signal levels from 50 mV up to 225 mV (RMS), and at frequencies as high as 1.25 GHz. The high frequency divider circuits use bipolar transistors, slower bits are CMOS. Divider ratios (512 to 131 071) allow a 1 MHz phase comparison with a 500 MHz RF input, and a 10 kHz phase comparison with a 1.25 GHz RF input.

The reference and main divider outputs are connected to a phase/frequency detector that controls two charge pumps. The two pumps have a common bias-setting current that is set by an external resistance. The ratio between currents in fast and normal operating modes can be programmed via the 3-wire serial bus. The low current pump remains active except in power-down.

The high current pump is enabled via the control input FAST (pin 1). By appropriate connection to the loop filter, dual bandwidth loops are provided: short time constant during frequency switching (FAST mode) to speed-up channel changes and low bandwidth in the settled state (on-frequency) to reduce noise and breakthrough levels.

The principal synthesizer speed-up charge pump (CPPF) is controlled by the FAST input in synchronization with phase detector operation in such a way that potential disturbances are minimized. The dead zone (caused by finite time taken to switch the current sources on or off) is cancelled by feedback from the normal pump output to the phase detector thereby improving linearity.

An open drain transistor drives the output pin LOCK (pin 20). It is recommended that the pull-up resistor from this pin to V_{DD} is chosen such that the value is high enough to keep the sink current in the LOW state below 400 μA. The circuit can be programmed to output either the phase error in the principal or auxiliary phase detectors or the combination from both detectors (OR function). The resultant output will be a current pulse with the duration of the selected phase error. By appropriate external filtering and threshold comparison an out-of-lock or an in-lock flag is generated.

Auxiliary synthesizer

The auxiliary synthesizer has a 14-bit main divider and an 11-bit reference divider. A separate power-down input AON (pin 19), disables currents in the auxiliary dividers, phase detector, and charge pump. The auxiliary input signal is amplified and fed to the main divider. The input buffer presents a high impedance, dominated by pin and pad capacitance. First divider stages use bipolar technology operating at input frequencies up to 300 MHz; the slower bits are CMOS. The auxiliary loop phase detector and charge pump use similar circuits to the main loop low-current phase comparator, including dead-zone compensation feedback.

The auxiliary reference divider is clocked on the opposite edge of the principal reference divider to ensure that active edges arrive at the auxiliary and principal phase detectors at different times. This minimizes the potential for interference between the charge pumps of each loop.

Serial programming bus

A simple 3-line unidirectional serial bus is used to program the circuit. The 3 lines are DATA, CLK and $\overline{E}$ (enable). The data sent to the device is loaded in bursts framed by $\overline{E}$. Programming clock edges and their appropriate data bits are ignored until $\overline{E}$ goes active LOW. The programmed information is loaded into the addressed latch when $\overline{E}$ returns inactive HIGH. Only the last 21 bits serially clocked into the device are retained within the programming register. Additional leading bits are ignored, and no check is made on the number of clock pulses. The fully static CMOS design uses virtually no current when the bus is inactive. It can always capture new programmed data even during power-down of main and auxiliary loops.

However, when either principal synthesizer or auxiliary synthesizer or both are powered-on, the presence of a TCXO signal is required at pin 8 (f_{XTAL}) for correct programming.

Data format

Data is entered with the most significant bit first.
The leading bits make up the data field, while the trailing four bits are an address field. The UMA1018M uses 6 of the 16 available addresses. These are chosen to allow direct compatibility with the UAA2072M integrated front-end. The data format is shown in Table 1. The first entered bit is p1, the last bit is p21.

The trailing address bits are decoded on the inactive edge of $\overline{E}$. This produces an internal load pulse to store the data in one of the addressed latches. To ensure that the data is correctly loaded on first power-up, $\overline{E}$ should be held LOW and only taken HIGH after having programmed an appropriate register. To avoid erroneous divider ratios, the pulse is not allowed during data reads by the frequency dividers. This condition is guaranteed by respecting a minimum $\overline{E}$ pulse width after data transfer.
The corresponding relationship between data fields and addresses is given in Table 2.

Table 1 Format of programmed data

LAST IN	PROGRAMMING REGISTER BIT USAGE						FIRST IN
p21	p20	p19	p18	p17	p16	../..	p2	p1
ADD0	ADD1	ADD2	ADD3	DATA0	DATA1	../..	DATA15	DATA16
LATCH ADDRESS				LSB	DATA COEFFICIENT			MSB

Table 2 Bit allocation (note 1)

FT	REGISTER BIT ALLOCATION																				LT
p1	p2	p3	p4	p5	p6	p7	p8	p9	p10	p11	p12	p13	p14	p15	p16	p17	p18	p19	p20	p21
dt16	dt15	dt14	dt13	dt12	DATA FIELD							dt4	dt3	dt2	dt1	dt0	ADDRESS			
TEST BITS[2]																	0	0	0	0
X	X	X	X	OLP	OLA	CR1	CR0	X	X	sPON	sAON	X	X	X	X	X	0	0	0	1
PM16	PRINCIPAL MAIN DIVIDER COEFFICIENT															PM0	0	1	0	0
X	X	X	X	X	X	PR10	PRINCIPAL REFERENCE DIVIDER COEFFICIENT									PR0	0	1	0	1
X	X	X	AM13	AUXILIARY MAIN DIVIDER COEFFICIENT												AM0	0	1	1	0
X	X	X	X	X	X	AR10	AUXILIARY REFERENCE DIVIDER COEFFICIENT									AR0	0	1	1	1
X	X	X	X	X	X	X	X	X	0	DA6	7-BIT DAC					DA0	1	0	0	0

Notes

1. FT = first; LT = last; sPON = software power-up for principal synthesizer (1 = ON); sAON = software power-up for auxiliary synthesizer (1 = ON).
2. The test register should not be programmed with any other value except all zeros for normal operation.

Table 3 Out-of-lock select

OLP	OLA	OUT-OF-LOCK ON PIN 20
0	0	output disabled
0	1	auxiliary phase error
1	0	principal phase error
1	1	both auxiliary and principal

Table 4 Fast and normal charge pumps current ratio (note 1)

CR1	CR0	I_{CPA}	I_{CPP}	I_{CPPF}	$I_{CPPF} : I_{CPP}$
0	0	$4 \times I_{SET}$	$4 \times I_{SET}$	$16 \times I_{SET}$	4 : 1
0	1	$4 \times I_{SET}$	$4 \times I_{SET}$	$32 \times I_{SET}$	8 : 1
1	0	$4 \times I_{SET}$	$2 \times I_{SET}$	$24 \times I_{SET}$	12 : 1
1	1	$4 \times I_{SET}$	$2 \times I_{SET}$	$32 \times I_{SET}$	16 : 1

Note

1. $I_{SET} = \frac{V_{14}}{R_{ext}}$; common bias current for charge pumps and DAC.

Table 5 Power-down modes

AON	PON	FAST	PRINCIPAL DIVIDERS	AUXILIARY DIVIDERS	PUMP CPA	PUMP CPP	PUMP CPPF	DAC AND BIAS
0	0	X	OFF	OFF	OFF	OFF	OFF	OFF
0	1	0	ON	OFF	OFF	ON	OFF	ON
0	1	1	ON	OFF	OFF	ON	ON	ON
1	0	X	OFF	ON	ON	OFF	OFF	ON
1	1	0	ON	ON	ON	ON	OFF	ON
1	1	1	ON	ON	ON	ON	ON	ON

Digital-to-analog converter

The 7-bits loaded via the bus into the appropriate latch drive a digital-to-analog converter. The internal current is scaled by the external resistance (R_{ext}) at pin I_{SET}, similar to the charge pumps. The nominal full-scale current is $2 \times I_{SET}$. The output current is mirrored to produce a full-scale voltage into a user-defined ground referenced resistance, thereby allowing optimum swing from power supply rails within the 2.7 to 5.5 V limits. The band gap reference voltage at pin I_{SET} is temperature and supply independent. The DAC signal is monotonic across the full range of digital input codes to enable fine adjustment of other system blocks. The typical settling time for full-scale switching is 400 ns into a 12 kΩ // 20 pF load. DAC functionality is neither tested nor guaranteed on UMA1018M versions with the /S1 suffix.

Power-down modes

The action of the control inputs on the state of internal blocks is defined by Table 5.

It should be noted that in Table 5, PON and AON can be either the software or hardware power-down signals. The dividers are ON when both hardware and software power-down signals are at logic 1.

When either synthesizer is reactivated after power-down the main and reference dividers of that synthesizer are synchronized to avoid the possibility of random phase errors on power-up.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	digital supply voltage	−0.3	+5.5	V
V_{CC}	analog supply voltage	−0.3	+5.5	V
ΔV_{CC-DD}	difference in voltage between V_{CC} and V_{DD}	−0.3	+5.5	V
V_n	voltage at pins 1, 6, 8 to 15, 19 and 20	−0.3	V_{DD} + 0.3	V
$V_{2, 3, 17}$	voltage at pins 2, 3 and 17	−0.3	V_{CC} + 0.3	V
ΔV_{GND}	difference in voltage between AGND and DGND (these pins should be connected together)	−0.3	+0.3	V
P_{tot}	total power dissipation	–	150	mW
T_{stg}	storage temperature	−55	+125	°C
T_{amb}	operating ambient temperature	−30	+85	°C
T_j	maximum junction temperature	–	95	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air	120	K/W

CHARACTERISTICS

$V_{DD1} = V_{DD2} = 2.7$ to 5.5 V; $V_{CC} = 2.7$ to 5.5 V; $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply; pins 4, 5 and 18						
V_{DD}	digital supply voltage	$V_{DD1} = V_{DD2}$	2.7	–	5.5	V
V_{CC}	analog supply voltage	$V_{CC} \geq V_{DD}$	2.7	–	5.5	V
I_{DD}	principal synthesizer digital supply current	$V_{DD} = 5.5$ V	–	6.5	8.5	mA
	auxiliary synthesizer digital supply current	$V_{DD} = 5.5$ V	–	2.7	4.0	mA
I_{CC}	charge pumps and analog supply current	$V_{CC} = 5.5$ V; $R_{ext} = 12$ kΩ	–	1.2	2.0	mA
I_{CCPD}, I_{DDPD}	current in power-down mode per supply	logic levels 0 V or V_{DD}	–	12	50	µA
RF principal main divider input; pin 6						
f_{VCO}	RF input frequency	$2.7 \text{ V} < V_{DD} < 3.5$ V	50	–	1250	MHz
		$2.7 \text{ V} < V_{DD} < 5.5$ V	50	–	1100	MHz
$V_{6(rms)}$	AC-coupled input signal level (RMS value)	$R_s = 50$ Ω; $2.7 \text{ V} < V_{DD} < 3.5$ V; $0.5 < f_{VCO} < 1.25$ GHz; $T_{amb} = -20$ to +85°C	50	–	225	mV
		$R_s = 50$ Ω; $2.7 \text{ V} < V_{DD} < 5.5$ V; $0.5 < f_{VCO} < 1.1$ GHz; $T_{amb} = -30$ to +85°C	100	–	300	mV
		$R_s = 50$ Ω; $2.7 \text{ V} < V_{DD} < 5.5$ V; $50 < f_{VCO} < 500$ MHz; $T_{amb} = -30$ to +85°C	150	–	300	mV
Z_I	input impedance (real part)	$f_{VCO} = 1$ GHz	–	1	–	kΩ
C_I	typical pin input capacitance	indicative, not tested	–	2	–	pF
R_{pm}	principal main divider ratio		512	–	131071	
f_{PPCmax}	maximum principal phase comparator frequency		–	2000	–	kHz
f_{PPCmin}	minimum principal phase comparator frequency		–	10	–	kHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Auxiliary main divider input; pin 15						
f_{AI}	input frequency		20	–	300	MHz
$V_{15(rms)}$	AC-coupled input signal level (RMS value)	R_s = 50 Ω; 2.7 V < V_{DD} < 4.5 V; T_{amb} = –30 to +85°C	50	–	500	mV
		R_s = 50 Ω; 2.7 V < V_{DD} < 5.5 V; T_{amb} = –20 to +85°C	100	–	500	mV
Z_I	input impedance (real part)	f_{AI} = 100 MHz	–	1	–	kΩ
C_I	typical pin input capacitance	indicative, not tested	–	2	–	pF
R_{am}	auxiliary main divider ratio		64	–	16383	
f_{APCmax}	maximum auxiliary phase comparator frequency		–	2000	–	kHz
f_{APCmin}	minimum auxiliary phase comparator frequency		–	10	–	kHz
Crystal reference divider input; pin 8						
f_{XTAL}	crystal reference input frequency		5	–	40	MHz
$V_{8(rms)}$	sinusoidal input signal level (RMS value)	4.0 V < V_{DD} < 5.5 V	50	–	500	mV
		2.7 V < V_{DD} < 5.5 V	50	–	250	mV
Z_I	input impedance (real part)	f_{XTAL} = 30 MHz	–	6	–	kΩ
C_I	typical pin input capacitance	indicative, not tested	–	2	–	pF
R_{pr}	principal reference divider ratio		8	–	2047	
R_{ar}	auxiliary reference divider ratio		8	–	2047	
Charge pump current setting resistor input; pin 14						
R_{ext}	external resistor from pin 14 to ground		12	–	60	kΩ
V_{14}	regulated voltage at pin 14	R_{ext} = 12 kΩ	–	1.15	–	V
Charge pump outputs; pins 17, 3 and 2; R_{ext} = 12 kΩ						
I_{Ocp}	charge pump output current error		–25	–	+25	%
I_{match}	sink-to-source current matching	V_{cp} in range	–	±5	–	%
I_{Lcp}	charge pump off leakage current	V_{cp} = ½V_{CC}	–5	±1	+5	nA
V_{cp}	charge pump voltage compliance		0.4	–	V_{CC} – 0.4	V
Interface logic input signal levels; pins 13, 12, 11 and 1						
V_{IH}	HIGH level input voltage		0.7V_{DD}	–	V_{DD} + 0.3	V
V_{IL}	LOW level input voltage		–0.3	–	0.3V_{DD}	V
I_{bias}	input bias current	logic 1 or logic 0	–5	–	+5	μA
C_I	input capacitance	indicative, not tested	–	2	–	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DAC output signal levels; pin 10; R_{ext} = 12 to 24 kΩ						
I_{DAC}	DAC full scale output current		$1.5 \times I_{SET}$	$2 \times I_{SET}$	$2.5 \times I_{SET}$	mA
V_{10}	output voltage compliance	all codes	0	–	$V_{DD} - 0.4$	V
I_{10min}	minimum DAC current	00 code	–	2	5	μA
I_{monot}	worst case monotonicity test: $\Delta I \times \frac{128}{2 \times I_{SET}}$	note 1	0.1	–	1.9	
Lock detect output signal; pin 20; open-drain output						
V_{OL}	LOW level output voltage	I_{sink} = 0.4 mA	–	–	0.4	V

Note

1. ΔI is the change in DAC output current when making the code transitions: 3FH/40H or 1FH/20H.

SERIAL BUS TIMING CHARACTERISTICS

$V_{DD} = V_{CC}$ = 3 V; T_{amb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Serial programming clock; CLK					
t_r	input rise time	–	10	40	ns
t_f	input fall time	–	10	40	ns
T_{cy}	clock period	100	–	–	ns
Enable programming; $\overline{E}$					
t_{START}	delay to rising clock edge	40	–	–	ns
t_{END}	delay from last falling clock edge	–20	–	–	ns
t_W	minimum inactive pulse width	4000(1)	–	–	ns
$t_{SU;\overline{E}}$	enable set-up time to next clock edge	20	–	–	ns
Register serial input data; DATA					
$t_{SU;DAT}$	input data to clock set-up time	20	–	–	ns
$t_{HD;DAT}$	input data to clock hold time	20	–	–	ns

Note

1. The minimum pulse width (t_W) can be smaller than 4 μs provided all the following conditions are satisfied:

   a) Principal main divider input frequency $f_{VCO} > \frac{256}{t_W}$

   b) Auxiliary main divider input frequency $f_{AI} > \frac{32}{t_W}$

   c) Reference divider input frequency $f_{XTAL} > \frac{3}{t_W}$

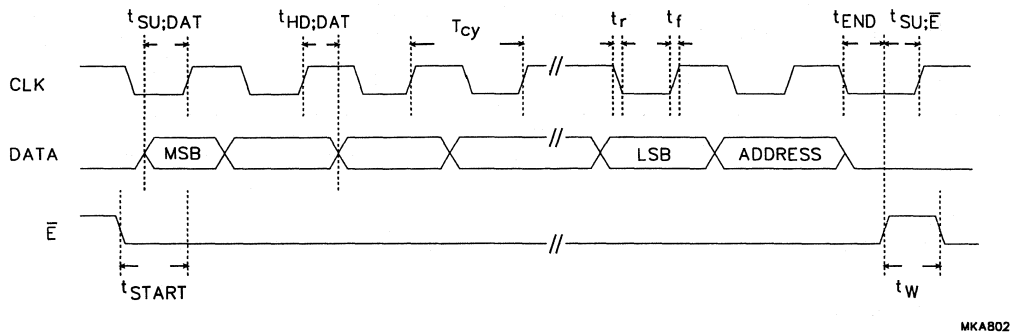


Fig.3 Serial bus timing diagram.

APPLICATION INFORMATION

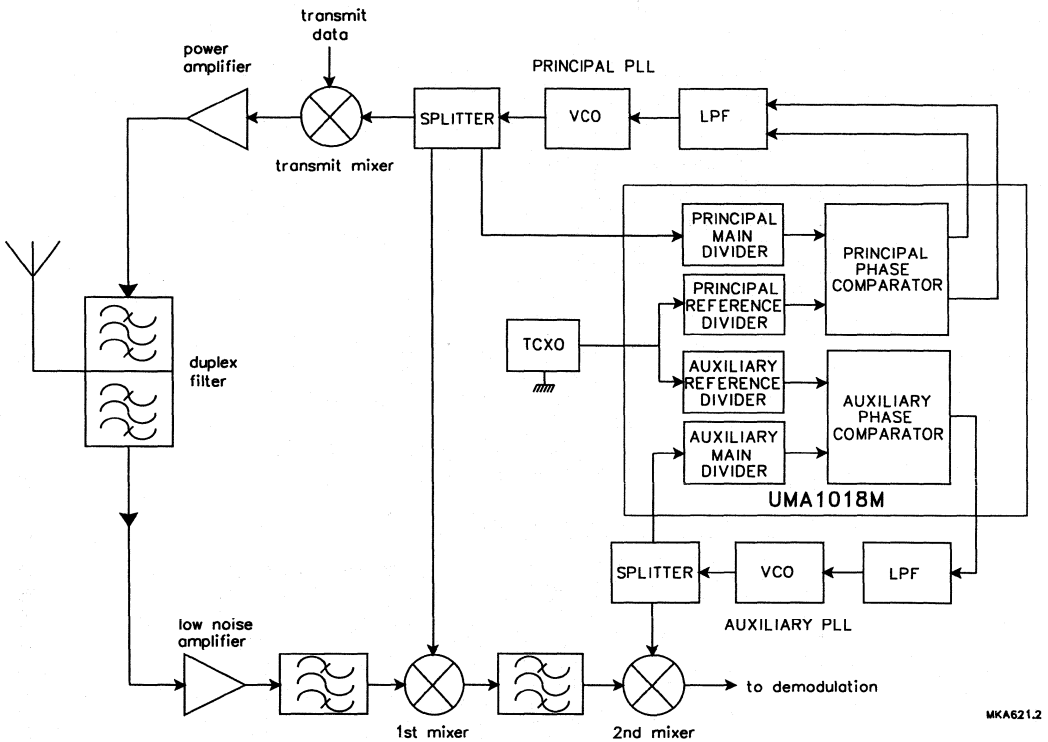


Fig.4 Typical application block diagram.

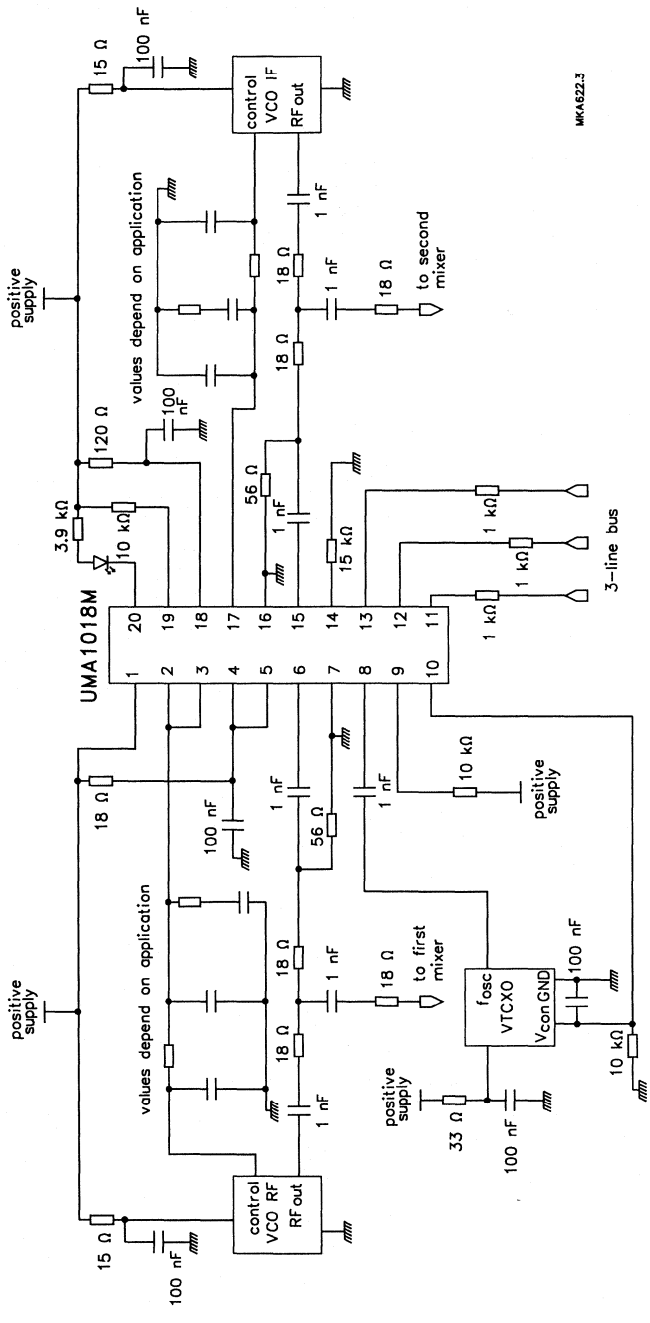


Fig.5 Typical test and application diagram.

Low-voltage dual frequency synthesizer for radio telephones

UMA1020M

FEATURES

- Low current from 3 V supply
- Fully programmable RF divider
- 3-line serial interface bus
- Second synthesizer to control first IF or offset loop frequency
- Independent fully programmable reference dividers for each loop, driven from external crystal oscillator
- Dual phase detector outputs to allow fast frequency switching
- Integrated digital-to-analog converter
- Dual power-down modes.

APPLICATIONS

- 2 GHz mobile telephones
- Portable battery-powered radio equipment.

GENERAL DESCRIPTION

The UMA1020M BICMOS device integrates prescalers, programmable dividers, and phase comparators to implement two phase-locked loops. The device is designed to operate from 3 NiCd cells, in pocket phones, with low current and nominal 5 V supplies.

The principal synthesizer operates at RF input frequencies up to 2.4 GHz the auxiliary synthesizer operates at 300 MHz. The auxiliary loop is intended for the first IF or to transmit offset loop-frequency settings. Each synthesizer has a fully programmable reference divider. All divider ratios are supplied via a 3-wire serial programming bus.

Separate power and ground pins are provided to the analog and digital circuits. The ground leads should be externally short-circuited to prevent large currents flowing across the die and thus causing damage. Digital supplies V_{DD1} and V_{DD2} must also be at the same potential. V_{CC} must be equal to or greater than V_{DD} (i.e. V_{DD} = 3 V and V_{CC} = 5 V for wider tuning range).

The principal synthesizer phase detector uses two charge pumps, one provides normal loop feedback, while the other is only active during fast mode to speed-up switching. The auxiliary loop has a separate phase detector. All charge pump currents (gain) are fixed by an external resistance at pin I_{SET} (pin 14). Only passive loop filters are used; the charge-pumps function within a wide voltage compliance range to improve the overall system performance. An on-chip 7-bit DAC enables adjustment of an external function, such as the temperature compensation of a crystal oscillator.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}, V_{DD}	supply voltage	$V_{CC} \geq V_{DD}$	2.7	–	5.5	V
$I_{CC} + I_{DD}$	principal synthesizer supply current	auxiliary synthesizer in power-down mode	–	9.4	–	mA
	principal and auxiliary synthesizer supply current	principal and auxiliary synthesizers ON	–	12.1	–	mA
I_{CCPD}, I_{DDPD}	current in power-down mode per supply		–	12	–	µA
f_{VCO}	principal input frequency		1700	–	2400	MHz
f_{AI}	auxiliary input frequency		20	–	300	MHz
f_{XTAL}	crystal reference input frequency		3	–	40	MHz
f_{PPC}	principal phase comparator frequency		–	200	–	kHz
f_{APC}	auxiliary phase comparator frequency		–	200	–	kHz
T_{amb}	operating ambient temperature		–30	–	+85	°C

Low-voltage dual frequency synthesizer for radio telephones

UMA1020M

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UMA1020M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

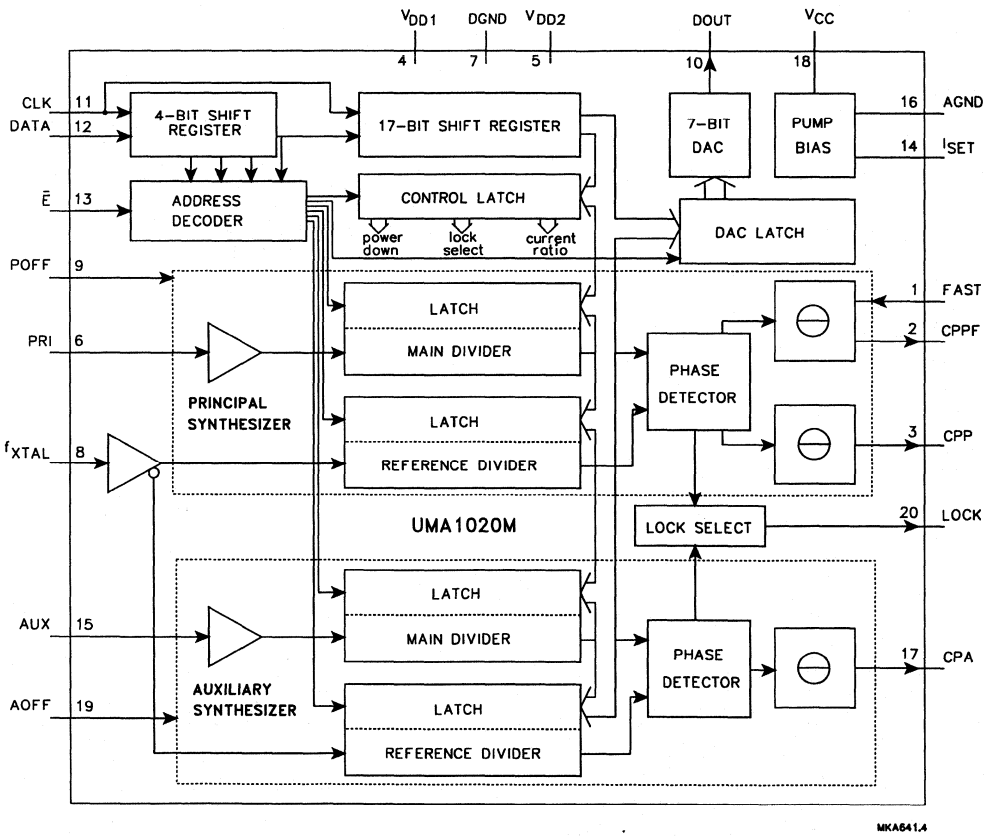


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
FAST	1	control input to speed-up main synthesizer
CPPF	2	principal synthesizer speed-up charge-pump output
CPP	3	principal synthesizer normal charge-pump output
V_{DD1}	4	digital power supply 1
V_{DD2}	5	digital power supply 2
PRI	6	2 GHz principal synthesizer frequency input
DGND	7	digital ground
f_{XTAL}	8	crystal frequency input from TCXO
POFF	9	principal synthesizer power-down input
DOUT	10	7-bit digital-to-analog output
CLK	11	programming bus clock input
DATA	12	programming bus data input
$\overline{E}$	13	programming bus enable input (active LOW)
I_{SET}	14	regulator pin to set the charge-pump currents
AUX	15	auxiliary synthesizer frequency input
AGND	16	analog ground
CPA	17	auxiliary synthesizer charge-pump output
V_{CC}	18	supply for charge-pump and DAC circuits
AOFF	19	auxiliary synthesizer power-down input
LOCK	20	in-lock detect output (main PLL); test mode output

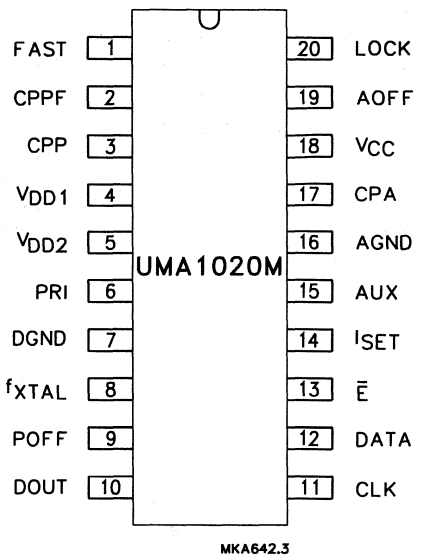


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Principal synthesizer

Programmable reference and main dividers drive the principal PLL phase detector. Two charge pumps produce phase error current pulses for integration in an external loop filter. A hardwired power-down input POFF (pin 9) ensures that the dividers and phase comparator circuits can be disabled.

The PRI input (pin 6) drives a preamplifier to provide the clock to the first divider stage. The preamplifier has a high input impedance, dominated by pin and pad capacitance. The circuit operates with signal levels from 60 mV to 180 mV (RMS), and at frequencies up to 2.4 GHz. The high frequency divider circuits use bipolar transistors, slower bits are CMOS. Divide ratios (512 to 131 071) allow a 2 MHz phase comparison frequency.

The reference and main divider outputs are connected to a phase/frequency detector that controls two charge pumps. The two pumps have a common bias setting current that is set by an external resistance. The ratio between currents in fast and normal operating modes can be programmed via the 3-wire serial bus. The low current pump remains active except in power-down. The high current pump is enabled via the control input FAST (pin 1). By appropriate connection to the loop filter, dual bandwidth loops are provided: short time constant during frequency switching (FAST mode) to speed-up channel changes and low bandwidth in the settled state (on-frequency) to reduce noise and breakthrough levels.

The principal synthesizer speed-up charge pump (CPPF) is controlled by the FAST input in synchronization with phase detector operation in such a way that potential disturbances are minimized. The dead zone (caused by finite time taken to switch the current sources on or off) is cancelled by feedback from the normal pump output to the phase detector thereby improving linearity.

An open drain transistor drives the output pin LOCK (pin 20). It is recommended that the pull-up resistor from this pin to V_{DD} is chosen such that the value is high enough to keep the sink current in the LOW state below 400 μA. The circuit can be programmed to output either the phase error in the principal or auxiliary phase detectors or the combination from both detectors (OR function). The resultant output will be a current pulse with the duration of the selected phase error. By appropriate external filtering and threshold comparison, an out-of-lock or an in-lock flag is generated.

Auxiliary synthesizer

The auxiliary synthesizer has a 14-bit main divider and an 11-bit reference divider. A separate power-down input AOFF (pin 19), disables currents in the auxiliary dividers, phase detector, and charge pump. The auxiliary input signal is amplified and fed to the main divider. The input buffer presents a high impedance, dominated by pin and pad capacitance. First divider stages use bipolar technology operating at input frequencies up to 300 MHz; the slower bits are CMOS. The auxiliary loop phase detector and charge pump use similar circuits to the main loop low-current phase comparator, including dead-zone compensation feedback.

The auxiliary reference divider is clocked on the opposite edge of the principal reference divider to ensure that active edges arrive at the auxiliary and principal phase detectors at different times. This minimizes the potential for interference between the charge pumps of each loop.

Serial programming bus

A simple 3-line unidirectional serial bus is used to program the circuit. The 3 lines are DATA, CLK and $\overline{E}$ (enable). The data sent to the device is loaded in bursts framed by $\overline{E}$. Programming clock edges and their appropriate data bits are ignored until $\overline{E}$ goes active LOW. The programmed information is loaded into the addressed latch when $\overline{E}$ returns inactive HIGH. Only the last 21 bits serially clocked into the device are retained within the programming register. Additional leading bits are ignored, and no check is made on the number of clock pulses. The fully static CMOS design uses virtually no current when the bus is inactive. It can always capture new programmed data even during power-down of main and auxiliary loops.

However when either principal synthesizer or auxiliary synthesizer or both are powered-on, the presence of a TCXO signal is required at pin 8 (f_{XTAL}) for correct programming.

Data format

Data is entered with the most significant bit first. The leading bits make up the data field, while the trailing four bits are an address field. The UMA1020M uses 6 of the 16 available addresses. The data format is shown in Table 1. The first entered bit is p1, the last bit is p21.

The trailing address bits are decoded on the inactive edge of $\overline{E}$. This produces an internal load pulse to store the data in one of the addressed latches. To ensure that the data is correctly loaded on first power-up, $\overline{E}$ should be held LOW and only taken HIGH after having programmed an appropriate register. To avoid erroneous divider ratios, the pulse is not allowed during data reads by the frequency dividers. This condition is guaranteed by respecting a minimum $\overline{E}$ pulse width after data transfer. The corresponding relationship between data fields and addresses is given in Table 2.

Table 1 Format of programmed data

LAST IN	PROGRAMMING REGISTER BIT USAGE							FIRST IN
p21	p20	p19	p18	p17	p16	../..	p2	p1
ADD0	ADD1	ADD2	ADD3	DATA0	DATA1	../..	DATA15	DATA16
LATCH ADDRESS				LSB	DATA COEFFICIENT			MSB

Table 2 Bit allocation (note 1)

FT	REGISTER BIT ALLOCATION																				LT
p1	p2	p3	p4	p5	p6	p7	p8	p9	p10	p11	p12	p13	p14	p15	p16	p17	p18	p19	p20	p21
dt16	dt15	dt14	dt13	dt12	DATA FIELD							dt4	dt3	dt2	dt1	dt0	ADDRESS			
TEST BITS[2]																	0	0	0	0
X	X	X	X	OLP	OLA	CR1	CR0	X	X	sPOFF	sAOFF	X	X	X	X	X	0	0	0	1
PM16	PRINCIPAL MAIN DIVIDER COEFFICIENT															PM0	0	1	0	0
X	X	X	X	X	X	PR10	PRINCIPAL REFERENCE DIVIDER COEFFICIENT									PR0	0	1	0	1
X	X	X	AM13	AUXILIARY MAIN DIVIDER COEFFICIENT												AM0	0	1	1	0
X	X	X	X	X	X	AR10	AUXILIARY REFERENCE DIVIDER COEFFICIENT									AR0	0	1	1	1
X	X	X	X	X	X	X	X	X	0	DA6	7-BIT DAC					DA0	1	0	0	0

Notes

1. FT = first; LT = last; sPOFF = software power-down for principal synthesizer (1 = OFF); sAOFF = software power-down for auxiliary synthesizer (1 = OFF).
2. The test register should not be programmed with any other value except all zeros for normal operation.

Table 3 Out-of-lock select

OLP	OLA	OUT-OF-LOCK ON PIN 20
0	0	output disabled
0	1	auxiliary phase error
1	0	principal phase error
1	1	both auxiliary and principal

Table 4 Fast and normal charge pumps current ratio (note 1)

CR1	CR0	I_{CPA}	I_{CPP}	I_{CPPF}	I_{CPPF}: I_{CPP}
0	0	$4 \times I_{SET}$	$4 \times I_{SET}$	$16 \times I_{SET}$	4 : 1
0	1	$4 \times I_{SET}$	$4 \times I_{SET}$	$32 \times I_{SET}$	8 : 1
1	0	$4 \times I_{SET}$	$2 \times I_{SET}$	$24 \times I_{SET}$	12 : 1
1	1	$4 \times I_{SET}$	$2 \times I_{SET}$	$32 \times I_{SET}$	16 : 1

Note

1. $I_{SET} = \frac{V_{14}}{R_{ext}}$; common bias current for charge pumps and DAC.

Table 5 Power-down modes

AOFF	POFF	FAST	PRINCIPAL DIVIDERS	AUXILIARY DIVIDERS	PUMP CPA	PUMP CPP	PUMP CPPF	DAC AND BIAS
1	1	X	OFF	OFF	OFF	OFF	OFF	OFF
1	0	0	ON	OFF	OFF	ON	OFF	ON
1	0	1	ON	OFF	OFF	ON	ON	ON
0	1	X	OFF	ON	ON	OFF	OFF	ON
0	0	0	ON	ON	ON	ON	OFF	ON
0	0	1	ON	ON	ON	ON	ON	ON

Digital-to-analog converter

The 7-bits loaded via the bus into the appropriate latch drive a digital-to-analog converter. The internal current is scaled by the external resistance (R_{ext}) at pin I_{SET}, similar to the charge pumps. The nominal full-scale current is $2 \times I_{SET}$. The output current is mirrored to produce a full-scale voltage into a user-defined ground referenced resistance, thereby allowing optimum swing from power supply rails within the 2.7 to 5.5 V limits. The bandgap reference voltage at pin I_{SET} is temperature and supply independent. The DAC signal is monotonic across the full range of digital input codes to enable fine adjustment of other system blocks. The typical settling time for full-scale switching is 400 ns into a 12 kΩ // 20 pF load.

Power-down modes

The action of the control inputs on the state of internal blocks is defined by Table 5.

Note that in Table 5, POFF and AOFF can be either the software or hardware power-down signals. The dividers are ON when both hardware and software power-down signals are at logic 0.

When either synthesizer is reactivated after power-down, the main and reference dividers of that synthesizer are synchronized to avoid the possibility of random phase errors on power-up.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	digital supply voltage	−0.3	+5.5	V
V_{CC}	analog supply voltage	−0.3	+5.5	V
ΔV_{CC-DD}	difference in voltage between V_{CC} and V_{DD}	−0.3	+5.5	V
V_n	voltage at pins 1, 6, 8 to 15, 19 and 20	−0.3	V_{DD} + 0.3	V
$V_{2, 3, 17}$	voltage at pins 2, 3 and 17	−0.3	V_{CC} + 0.3	V
ΔV_{GND}	difference in voltage between AGND and DGND (these pins should be connected together)	−0.3	+0.3	V
P_{tot}	total power dissipation	–	150	mW
T_{stg}	storage temperature	−55	+125	°C
T_{amb}	operating ambient temperature	−30	+85	°C
T_j	maximum junction temperature	–	95	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	120	K/W

CHARACTERISTICS

$V_{DD1} = V_{DD2} = 2.7$ to 5.5 V; $V_{CC} = 2.7$ to 5.5 V; $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply; pins 4, 5 and 18						
V_{DD}	digital supply voltage	$V_{DD1} = V_{DD2}$	2.7	–	5.5	V
V_{CC}	analog supply voltage	$V_{CC} \geq V_{DD}$	2.7	–	5.5	V
I_{DD}	principal synthesizer digital supply current	$V_{DD} = 5.5$ V	–	9	12.5	mA
	auxiliary synthesizer digital supply current	$V_{DD} = 5.5$ V	–	2.7	4.0	mA
I_{CC}	charge pumps supply current	$V_{CC} = 5.5$ V; $R_{ext} = 12$ kΩ	–	0.4	1.0	mA
I_{CCPD}, I_{DDPD}	current in power-down mode per supply	logic levels 0 or V_{DD}	–	12	50	μA
RF principal main divider input; pin 6						
f_{VCO}	RF input frequency		1700	–	2400	MHz
$V_{6(rms)}$	AC-coupled input signal level (RMS value)	$R_s = 50$ Ω; 1.7 GHz < f_{VCO} < 2.0 GHz	60	–	400	mV
		$R_s = 50$ Ω; 2.0 GHz < f_{VCO} < 2.4 GHz	60	–	180	mV
Z_I	input impedance (real part)	$f_{VCO} = 2$ GHz	–	300	–	Ω
C_I	typical pin input capacitance	indicative, not tested	–	2	–	pF
R_{pm}	principal main divider ratio		512	–	131071	
f_{PPCmax}	maximum principal phase comparator frequency		–	2000	–	kHz
f_{PPCmin}	minimum principal phase comparator frequency		–	10	–	kHz
Auxiliary main divider input; pin 15						
f_{AI}	input frequency		20	–	300	MHz
$V_{15(rms)}$	AC-coupled input signal level (RMS value)	$R_s = 50$ Ω; 2.7 V < V_{DD} < 3.5 V	50	–	500	mV
		$R_s = 50$ Ω; 3.5 V < V_{DD} < 5.5 V	100	–	500	mV
Z_I	input impedance (real part)	$f_{AI} = 100$ MHz	–	1	–	kΩ
C_I	typical pin input capacitance	indicative, not tested	–	2	–	pF
R_{am}	auxiliary main divider ratio		64	–	16383	
f_{APCmax}	maximum auxiliary phase comparator frequency		–	2000	–	kHz
f_{APCmin}	minimum auxiliary phase comparator frequency		–	10	–	kHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Crystal reference dividers input; pin 8						
f_{XTAL}	input frequency range from crystal		5	–	40	MHz
$V_{8(rms)}$	sinusoidal input signal level (RMS value)	$V_{6(rms)} < 224$ mV	50	–	500	mV
		$V_{6(rms)} > 224$ mV	100	–	500	mV
Z_I	input impedance (real part)	$f_{XTAL} = 30$ MHz	–	2	–	kΩ
C_I	typical pin input capacitance	indicative, not tested	–	2	–	pF
R_{pr}	principal reference division ratio		8	–	2047	
R_{ar}	auxiliary reference division ratio		8	–	2047	
Charge pump current setting resistor input; pin 14						
R_{ext}	external resistor from pin 14 to ground		12	–	60	kΩ
V_{14}	regulated voltage at pin 14	$R_{ext} = 12$ kΩ	–	1.15	–	V
Charge pump outputs; pins 17, 3 and 2; $R_{ext} = 12$ kΩ						
I_{Ocp}	charge pump output current error		−25	–	+25	%
I_{match}	sink-to-source current matching	V_{cp} in range	–	±5	–	%
I_{Lcp}	charge pump off leakage current	$V_{cp} = ½V_{CC}$	−5	±1	+5	nA
V_{cp}	charge pump voltage compliance		0.4	–	$V_{CC} - 0.4$	V
Interface logic input signal levels; pins 13, 12, 11 and 1						
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	$V_{DD} + 0.3$	V
V_{IL}	LOW level input voltage		−0.3	–	$0.3V_{DD}$	V
I_{bias}	input bias current	logic 1 or logic 0	−5	–	+5	µA
C_I	input capacitance	indicative, not tested	–	2	–	pF
DAC output signal levels; pin 10, $R_{ext} = 12$ to 24 kΩ						
I_{DAC}	DAC full scale output current		$1.5 \times I_{SET}$	$2 \times I_{SET}$	$2.5 \times I_{SET}$	mA
V_{10}	output voltage compliance	all codes	0	–	$V_{DD} - 0.4$	V
I_{10min}	minimum DAC current	00 code	–	2	5	µA
I_{monot}	worst case monotonicity test: $\Delta I \times \frac{128}{2 \times I_{SET}}$	note 1	0.1	–	1.9	
Lock detect output signal; pin 20 open-drain output						
V_{OL}	LOW level output voltage	$I_{sink} = 0.4$ mA	–	–	0.4	V

Note

1. ΔI is the change in DAC output current when making the code transitions: 3FH/40H or 1FH/20H.

SERIAL BUS TIMING CHARACTERISTICS

$V_{DD} = V_{CC} = 3$ V; $T_{amb} = 25$ °C unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Serial programming clock; CLK					
t_r	input rise time	–	10	40	ns
t_f	input fall time	–	10	40	ns
T_{cy}	clock period	100	–	–	ns
Enable programming; $\overline{E}$					
t_{START}	delay to rising clock edge	40	–	–	ns
t_{END}	delay from last falling clock edge	–20	–	–	ns
t_W	minimum inactive pulse width	4000[1]	–	–	ns
$t_{SU;\overline{E}}$	enable set-up time to next clock edge	20	–	–	ns
Register serial input data; DATA					
$t_{SU;DAT}$	input data to clock set-up time	20	–	–	ns
$t_{HD;DAT}$	input data to clock hold time	20	–	–	ns

Note

1. The minimum pulse width (t_W) can be smaller than 4 µs provided all the following conditions are satisfied:

   a) Principal main divider input frequency $f_{VCO} > \frac{512}{t_W}$

   b) Auxiliary main divider input frequency $f_{AI} > \frac{32}{t_W}$

   c) Reference dividers input frequency $f_{XTAL} > \frac{3}{t_W}$

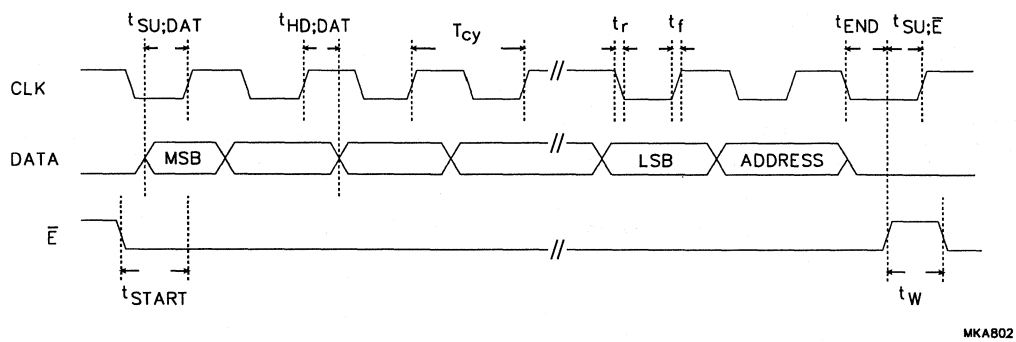


Fig.3 Serial bus timing diagram.

APPLICATION INFORMATION

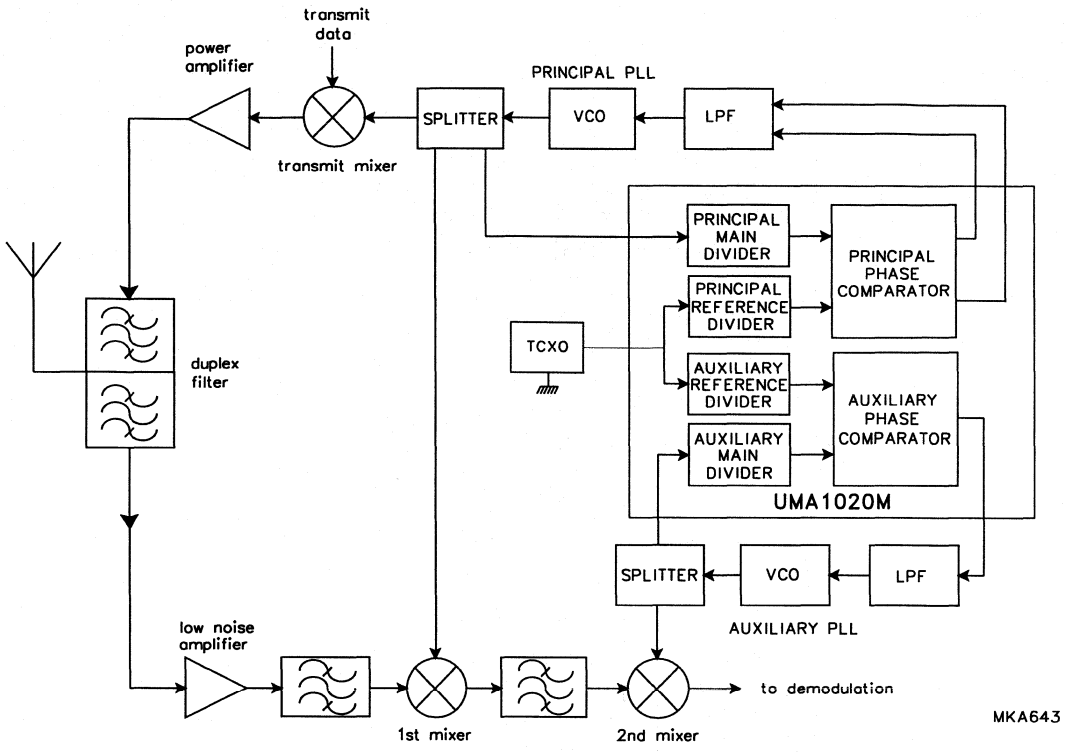


Fig.4 Typical application block diagram.

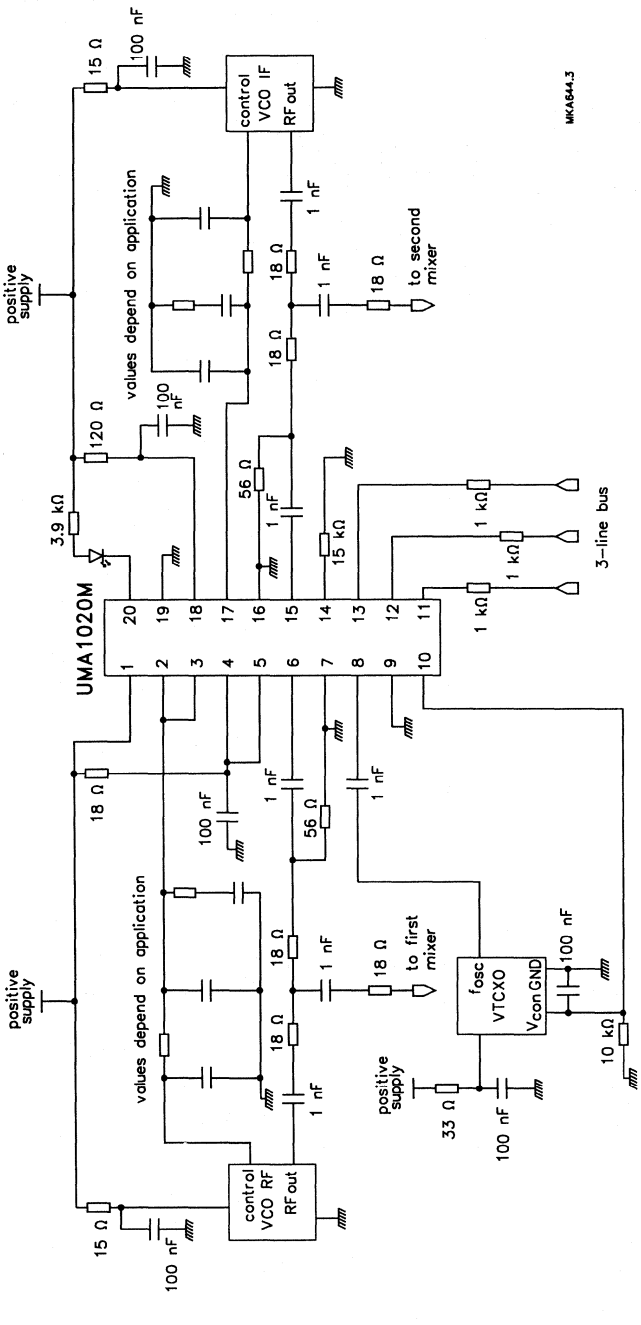


Fig.5 Typical test and application diagram.

Low-voltage frequency synthesizer for radio telephones

UMA1021M

FEATURES

- Low phase noise
- Low current from 3 V supply
- Fully programmable main divider
- 3-line serial interface bus
- Independent fully programmable reference divider, driven from external crystal oscillator
- Dual charge pump outputs
- Hard and soft power-down control.

APPLICATIONS

- 900 MHz and 2 GHz mobile telephones
- Portable battery-powered radio equipment.

GENERAL DESCRIPTION

The UMA1021M BICMOS device integrates a prescaler, programmable dividers, and a phase comparator to implement a phase-locked loop.

The device is designed to operate from 3 NiCd cells, in pocket phones, with low current and nominal 3 V supplies.

The synthesizer operates at RF input frequencies up to 2.2 GHz, with a fully programmable reference divider. All divider ratios are supplied via a 3-wire serial programming bus.

Separate power and ground pins are provided to the analog (charge-pump) and digital circuits. The ground leads should be externally short-circuited to prevent large currents flowing across the die and thus causing damage. V_{DD1} and V_{DD2} must also be at the same potential (V_{DD}). V_{CC} must be equal to or greater than V_{DD} (e.g. V_{DD} = 3 V and V_{CC} = 5 V for wider VCO control voltage range).

The phase detector has two charge-pump outputs, CP and CPF, the latter of which is enabled directly at pin FAST. This permits the design of adaptive loops. The charge pump currents (phase detector gain) are fixed by an external resistance at pin I_{SET} and via the serial interface. Only a passive loop filter is necessary; the charge pumps function within a wide voltage compliance range to improve the overall system performance.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	digital supply voltage	$V_{DD1} = V_{DD2}$; $V_{CC} \geq V_{DD}$	2.7	–	5.5	V
V_{CC}	charge-pump supply voltage	$V_{CC} \geq V_{DD}$	2.7	–	5.5	V
$I_{DD} + I_{CC}$	supply current		–	10	–	mA
$I_{CC(pd)} + I_{DD(pd)}$	total supply current in power-down mode		–	5	–	µA
f_{RF}	RF input frequency		300	–	2200	MHz
f_{xtal}	crystal reference input frequency		3	–	35	MHz
f_{PC}	phase comparator frequency		–	200	–	kHz
T_{amb}	operating ambient temperature		–30	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UMA1021M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

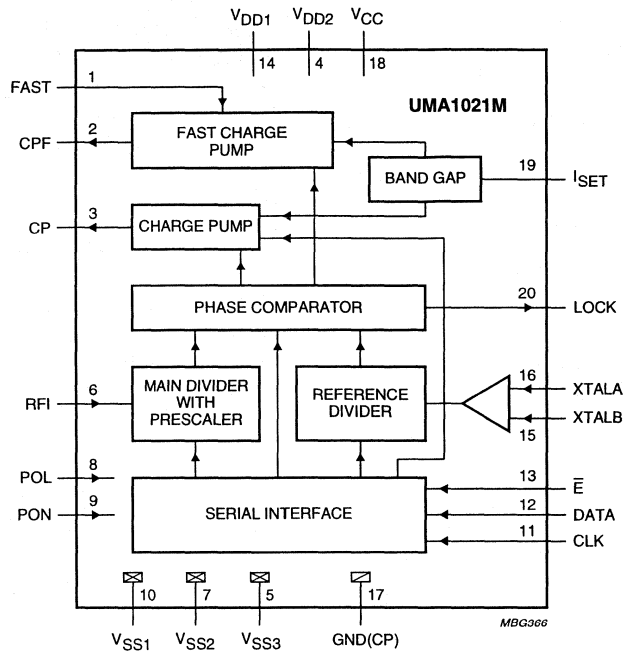


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
FAST	1	enable input for fast charge-pump output CPF
CPF	2	fast charge-pump output
CP	3	normal charge-pump output
V_{DD2}	4	power supply 2
V_{SS3}	5	ground 3
RFI	6	2 GHz main divider input
V_{SS2}	7	ground 2
POL	8	digital input to select polarity of power-on inputs (PON and sPON): POL = 0 for active LOW and POL = 1 for active HIGH
PON	9	power-on input
V_{SS1}	10	ground 1
CLK	11	programming bus clock input
DATA	12	programming bus data input
$\overline{E}$	13	programming bus enable input
V_{DD1}	14	power supply 1
XTALB	15	complementary crystal frequency input from TCXO; if not used should be decoupled to ground
XTALA	16	crystal frequency input from TCXO; if not used should be decoupled to ground
GND(CP)	17	ground for charge-pump
V_{CC}	18	supply for charge-pump
I_{SET}	19	external resistor from this pin to ground sets the charge-pump currents
LOCK	20	out-of-lock detector output

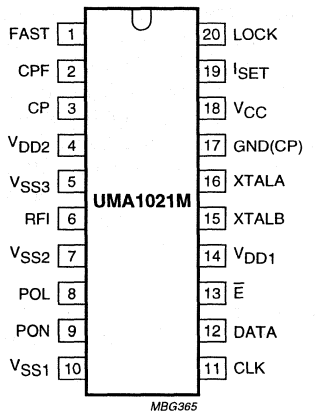


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Main divider

The main divider is clocked at pin RFI by the RF signal which is AC-coupled from an external VCO. The divider operates with signal levels from 50 to 225 mV (RMS), and at frequencies from 300 MHz to 2.2 GHz. It consists of a fully programmable bipolar prescaler followed by a CMOS counter. Any divide ratios from 512 to 131071 inclusive can be programmed.

Reference divider

The reference divider is clocked by the differential signal between pins XTALA and XTALB. If only one of these inputs is used, the other should be decoupled to ground. The applied input signal(s) should be AC-coupled. The circuit operates with levels from 50 up to 500 mV (RMS) and at frequencies from 3 to 35 MHz. Any divide ratios from 8 to 2047 inclusive can be programmed.

Phase detector

The phase detector is driven by the output edges of the main and reference dividers. It produces current pulses at pins CP and CPF whose amplitudes are programmed. The pulse duration is equal to the difference in time of arrival of the edges from the two dividers. If the main divider edge arrives first, CP and CPF sink current. If the reference divider edge arrives first, CP and CPF source current.

The currents at CP and CPF are programmed via the serial bus as multiples of a reference current set by an external resistor connected between pin I_{SET} and V_{SS} (see Table 3). CP remains active except in power-down. CPF is enabled via input pin FAST which is synchronized with respect to the phase detector to prevent output current pulses being interrupted. By appropriate connection to the loop filter, dual bandwidth loops can be designed; short time constant during frequency switching (FAST mode) to speed-up channel changes, and low bandwidth in the settled state to improve noise and breakthrough levels.

Additional circuitry is included to ensure that the gain of the phase detector remains linear even for small phase errors.

Out-of-lock detector

The out-of-lock detector is enabled (disabled) via the serial interface by setting bit OOL HIGH (LOW). An open drain transistor drives the output pin LOCK (pin 20). It is recommended that the pull-up resistor from this pin to V_{DD} is chosen to be of sufficient value to keep the sink current in the LOW state to below 400 μA. When the out-of-lock detector is enabled, LOCK is HIGH if the error at the phase detector input is less than approximately 25 ns, otherwise LOCK is LOW. If the out-of-lock detector is disabled, LOCK remains HIGH.

Serial programming bus

A simple 3-line unidirectional serial bus is used to program the circuit. The 3 lines are DATA, clock (CLK) and enable ($\overline{E}$). The data sent to the device is loaded in bursts framed by $\overline{E}$. Programming clock edges and their appropriate data bits are ignored until $\overline{E}$ goes active LOW. The programmed information is loaded into the addressed latch when $\overline{E}$ returns HIGH.

During normal operation, $\overline{E}$ should be kept HIGH. Only the last 21 bits serially clocked into the device are retained within the programming register. Additional leading bits are ignored, and no check is made on the number of clock pulses. The fully static CMOS design uses virtually no current when the bus is inactive. It can always capture new programmed data even during power-down.

When the synthesizer is powered-on, the presence of a TCXO signal at the reference divider input and a VCO signal at the main divider input is **required** for correct programming.

Data format

The leading bits (dt16 to dt0) make up the data field, while the trailing four bits (ad3 to ad0) are the address field. The UMA1021M uses 4 of the 16 available addresses. These are chosen for compatibility with other Philips Semiconductors radio telephone ICs. The data format is shown in Table 1. The first bit entered is dt16, the last bit is ad0. For the divider ratios, the first bits entered (PM16 and PR10) are the most significant (MSB).

The trailing address bits are decoded on the rising edge of $\overline{E}$. This produces an internal load pulse to store the data in the addressed latch. To avoid erroneous divider ratios, the load pulse is not allowed during data reads by the frequency dividers. This condition is guaranteed by respecting a minimum $\overline{E}$ pulse width after data transfer.

The test register (address 0000) does not normally need to be programmed. However if it is programmed, all bits in the data field should be set to logic 0.

Power-down mode

The synthesizer is on when both the input signals PON and the programmed bit sPON are active. The 'active' level for these two signals is chosen at pin POL (see Table 2). When turned on, the dividers and phase detector are synchronized to avoid random phase errors. When turned off, the phase detector is synchronized to avoid interrupting charge-pump pulses. For synchronisation functions to work correctly on power-up or power-down (using either hardware or software programming), the presence of TCXO and VCO signals is required to drive the appropriate divider inputs. The UMA1021M has a very low current consumption in the power-down mode.

Table 1 Bit allocation; note 1

FIRST IN				REGISTER BIT ALLOCATION												LAST IN			
DATA FIELD																ADDRESS			
dt16	dt15	dt14	dt13	dt12	dt11	dt10	dt9	dt8	dt7	dt6	dt5	dt4	dt3	dt2	dt1	dt0	ad3	ad2	ad1	ad0
Test bits[2]																	0	0	0	0
X	X	X	X	OOL[3]	X	CR1	CR0	X	X	sPON[3]	X	X	X	X	X	X	0	0	0	1
PM16[4]	main divider coefficient															PM0	0	1	0	0
X	X	X	X	X	X	PR10[4]	reference divider coefficient									PR0	0	1	0	1

Notes

1. X = don't care.
2. The test register (address 0000) should not be programmed with any other values except all zeros for normal operation.
3. Bit sPON = software power-up for synthesizer (see Table 2); OOL = Out-Of-Lock (1 = enabled).
4. PM16 is the MSB of the main divider coefficient; PR10 is the MSB of the reference divider coefficient.

Table 2 Power-on programming

POL	PON	sPON	SYNTHESIZER STATE	COMPATIBILITY
0	0	0	on	UMA1019M/UMA1019AM
0	1	X	off	UMA1019M/UMA1019AM
0	X	1	off	UMA1019M/UMA1019AM
1	0	X	off	UMA1017M
1	X	0	off	UMA1017M
1	1	1	on	UMA1017M

Table 3 Fast and normal charge pumps current ratio (note 1)

CR1	CR0	I_{CP}	I_{CPF}	$I_{CPF} : I_{CP}$
0	0	$2 \times I_{SET}$	$8 \times I_{SET}$	4 : 1
0	1	$2 \times I_{SET}$	$16 \times I_{SET}$	8 : 1
1	0	$1 \times I_{SET}$	$12 \times I_{SET}$	12 : 1
1	1	$1 \times I_{SET}$	$16 \times I_{SET}$	16 : 1

Note

1. $I_{SET} = \frac{V_{SET}}{R_{SET}}$; reference current for charge pumps.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	digital supply voltage	−0.3	+5.5	V
V_{CC}	charge-pump supply voltage	−0.3	+5.5	V
$V_{CC} - V_{DD}$	difference in voltage between V_{CC} and V_{DD}	−0.3	+5.5	V
V_n	voltage at pins 6, 8, 9 and 11 to 13	−0.3	V_{DD} + 0.3	V
	voltage at pins 1, 2, 3, 15, 16, 19 and 20	−0.3	V_{CC} + 0.3	V
ΔV_{GND}	difference in voltage between any of GND(CP), V_{SS1}, V_{SS2}, and V_{SS3} (these pins should be connected together)	−0.3	+0.3	V
P_{tot}	total power dissipation	–	150	mW
T_{stg}	storage temperature	−55	+125	°C
T_{amb}	operating ambient temperature	−30	+85	°C
$T_{j(max)}$	maximum junction temperature	–	150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices. This device meets class 2 ESD test requirements [Human Body Model (HBM)], in accordance with *"MIL STD 883C - method 3015"*.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	120	K/W

CHARACTERISTICS

All values refer to the typical measurement circuit of Fig.5; $V_{DD1} = V_{DD2} = 2.7$ to 5.5 V; $V_{CC} = 2.7$ to 5.5 V; $T_{amb} = 25$ °C; unless otherwise specified. Characteristics for which only a typical value is given are not tested.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply; pins 4, 14 and 18						
V_{DD}	digital supply voltage	$V_{DD1} = V_{DD2}$; $V_{CC} \geq V_{DD}$	2.7	–	5.5	V
V_{CC}	charge pump supply voltage	$V_{CC} \geq V_{DD}$	2.7	–	5.5	V
$I_{DD1} + I_{DD2}$	synthesizer digital supply current	$V_{DD} = 5.5$ V	–	7	9.5	mA
I_{CC}	charge pump supply current	$V_{CC} = 5.5$ V; $R_{SET} = 5.6$ kΩ	–	3	3.8	mA
$I_{CC(pd)} + I_{DD(pd)}$	total supply current in power-down mode	logic levels 0 V or V_{DD}	–	5	50	μA
RF main divider input; pin 6						
f_{RF}	RF input frequency		300	–	2200	MHz
$V_{RF(rms)}$	AC-coupled input signal level (RMS value)	$R_s = 50$ Ω	50	–	225	mV
R_m	main divider ratio		512	–	131071	
Z_i	input impedance (real part)	$f_{RF} = 1$ GHz	–	1	–	kΩ
		$f_{RF} = 2$ GHz	–	60	–	Ω
C_i	typical pin input capacitance	$f_{RF} = 1$ GHz	–	1	–	pF
		$f_{RF} = 2$ GHz	–	1	–	pF
Synthesizer reference divider input; pins 15 and 16						
f_{xtal}	crystal reference input frequency		3	–	35	MHz
$V_{xtal(rms)}$	sinusoidal input signal level between pins 15 and 16 (RMS value)		50	–	500	mV
R_{ref}	reference division ratio		8		2047	
Z_i	input impedance (real part)	$f_{xtal} = 13$ MHz	–	10	–	kΩ
C_i	typical pin input capacitance	$f_{xtal} = 13$ MHz	–	1.5	–	pF
Phase detector						
f_{PCmax}	maximum loop comparison frequency		–	2000	–	kHz
Charge pump current setting resistor input; pin 19						
R_{SET}	external resistor connected between pin 19 and ground		5.6	–	12	kΩ
V_{SET}	regulated voltage at pin 19	$R_{SET} = 5.6$ kΩ	–	1.2	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Charge pump outputs; pins 2 and 3; R_{SET} = 5.6 kΩ						
$I_{ocp(err)}$	charge pump output current error		−25	–	+25	%
I_{match}	sink-to-source current matching		–	±5	–	%
I_{LIcp}	charge pump off leakage current	$V_{CP/CPF} = ½V_{CC}$	−5	±1	+5	nA
$V_{CP/CPF}$	charge pump voltage compliance		0.4	–	$V_{CC} - 0.4$	V
Phase noise						
N_{900}	synthesizer's contribution to close-in phase noise of 900 MHz RF signal at 1 kHz offset (GSM)	f_{xtal} = 13 MHz; V_{xtal} = 0 dBm; f_{PC} = 200 kHz	–	−88	–	dBc/Hz
N_{1800}	synthesizer's contribution to close-in phase noise of 1.8 GHz RF signal at 1 kHz offset (DCS1800)	f_{xtal} = 13 MHz; V_{xtal} = 0 dBm; f_{PC} = 200 kHz	–	−82	–	dBc/Hz
Interface logic input signal levels; pins 1, 8, 9, 11, 12 and 13						
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	$V_{DD} + 0.3$	V
V_{IL}	LOW level input voltage		−0.3	–	$0.3V_{DD}$	V
I_{bias}	input bias current	logic 1 or logic 0	−5	–	+5	μA
C_i	input capacitance		–	2	–	pF
Lock detect output signal; pin 20; open-drain output						
V_{OL}	LOW level output voltage	I_{sink} < 0.4 mA	–	–	0.4	V
t_{OOL}	phase error threshold for out-of-lock detector		–	25	–	ns

SERIAL BUS TIMING CHARACTERISTICS

$V_{DD} = V_{CC} = 3$ V; $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Serial programming clock; CLK					
t_r	input rise time	–	10	40	ns
t_f	input fall time	–	10	40	ns
T_{cy}	clock period	100	–	–	ns
Enable programming; $\overline{E}$					
t_{START}	delay to rising clock edge	40	–	–	ns
t_{END}	delay from last falling clock edge	–20	–	–	ns
$t_{W(min)}$	minimum inactive pulse width	4000[1]	–	–	ns
$t_{SU;\overline{E}}$	enable set-up time to next clock edge	20	–	–	ns
Register serial input data; DATA					
$t_{SU;DAT}$	input data to clock set-up time	20	–	–	ns
$t_{HD;DAT}$	input data to clock hold time	20	–	–	ns

Note

1. The minimum pulse width ($t_{W(min)}$) can be smaller than 4 µs provided all the following conditions are fulfilled:

   a) Main divider input frequency $f_{RF} > \frac{447}{t_{W(min)}}$.

   b) Reference divider input frequency $f_{xtal} > \frac{3}{t_{W(min)}}$.

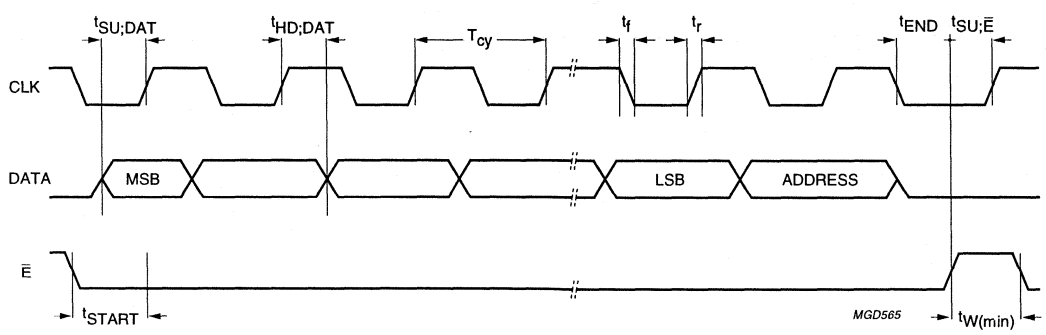


Fig.3 Serial bus timing diagram.

APPLICATION INFORMATION

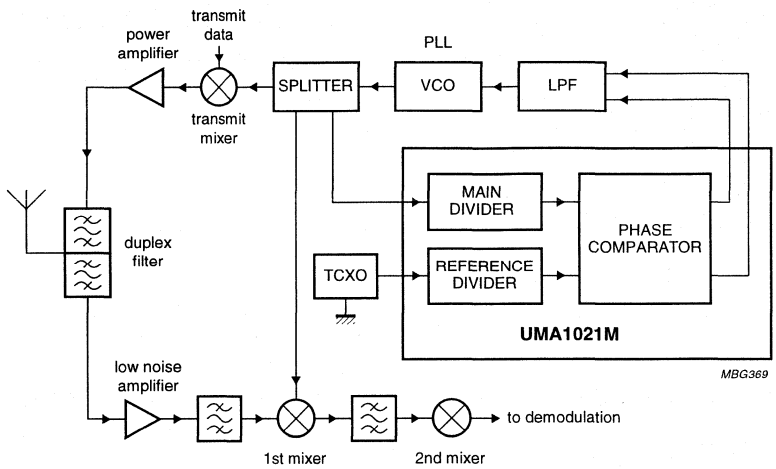
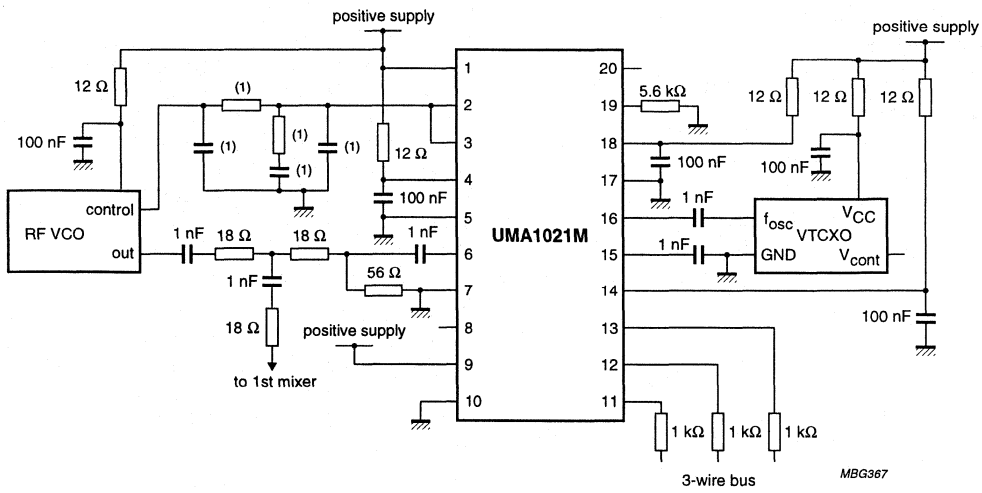


Fig.4 Typical application block diagram.



(1) Values depend on application.

Fig.5 Typical test and application diagram.

Low cost dual frequency synthesizer for radio telephones

UMA1022M

FEATURES

- Low phase noise
- Low current from 3 V supply
- Fully programmable dividers
- 3-line serial interface bus
- Input reference buffer configurable as an oscillator with external crystal resonator
- Wide compliance voltage charge pump outputs
- Two power-down input control pins.

APPLICATIONS

- 900 MHz and 2 GHz digital radio telephones
- Portable battery-powered radio equipment.

GENERAL DESCRIPTION

The UMA1022M BICMOS device integrates prescalers, programmable dividers, a crystal oscillator/buffer and phase comparators to implement two phase-locked loops. The device is designed to operate from 3 NiCd or a single LiIon cell in pocket phones, or from an external 3 V supply.

The synthesizers operate at RF input frequencies up to 2.2 GHz and 500 MHz. All divider ratios are supplied via a 3-wire serial programming bus. The reference divider uses a common, fully programmable part and a separate subdivider section. In this way the comparison frequencies are related to each other allowing optimum isolation between charge pump pulses.

Separate power and ground pins are provided to the analog (charge pump, prescaler) and digital (CMOS) circuits. An independent supply for the crystal oscillator section allows maximum frequency stability. The ground leads should be externally short-circuited to prevent large currents flowing across the die and thus causing damage. V_{DD} and V_{DDX} must be at the same potential. V_{CCA} and V_{CCB} must be equal to each other and equal to or greater than V_{DD} (e.g. V_{DD} = 3 V and V_{CCA} = 5 V for wider VCO control voltage range).

The charge pump currents (phase detector gain) are fixed by internal resistances and controlled by the serial interface. Only passive loop filters are necessary; the charge pumps function within a wide voltage compliance range to improve the overall system performance.

Suitable pin layout is chosen to minimize coupling and interference between signals entering or leaving the chip.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UMA1022M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	digital supply voltage	V_{CCA} and $V_{CCB} \geq V_{DD}$	2.7	–	5.5	V
V_{CCA}, V_{CCB}	analog supply voltages	V_{CCA} and $V_{CCB} \geq V_{DD}$	2.7	–	5.5	V
V_{DDX}	crystal reference supply voltage	$V_{DDX} = V_{DD}$	2.7	–	5.5	V
I_{tot}	all supply currents ($I_{DD} + I_{CCA} + I_{CCB} + I_{DDX}$) in active mode	$V_{CCA} = V_{CCB} = 3.0$ V; $V_{DDX} = V_{DD} = 3.0$ V; XON = 1; crystal oscillator active	–	13	–	mA
$I_{tot(pd)}$	total supply currents in power-down mode		–	30	–	µA
f_{RF}	RF input frequency		300	–	2200	MHz
f_{IF}	IF input frequency		50	–	500	MHz
f_{xtal}	crystal reference oscillator frequency		3	–	30	MHz
f_{PC}	phase comparator frequency		–	200	–	kHz
T_{amb}	operating ambient temperature		–30	–	+85	°C

BLOCK DIAGRAM

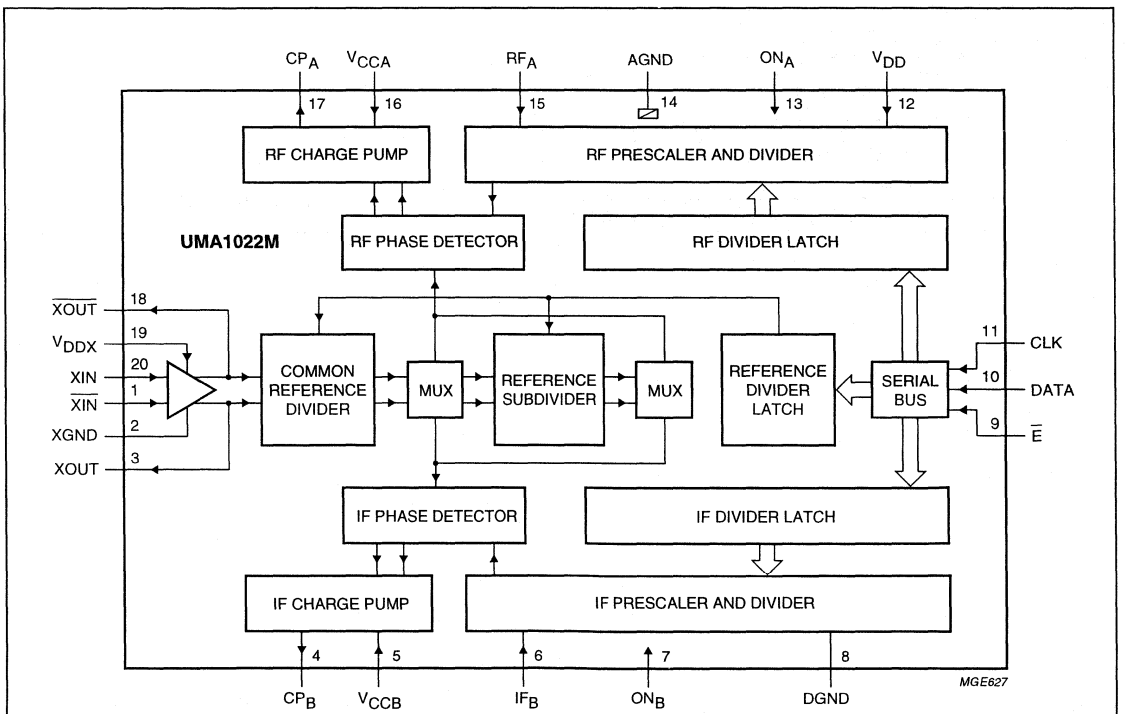


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$\overline{XIN}$	1	inverting crystal reference input
XGND	2	ground for crystal oscillator circuits
XOUT	3	crystal oscillator buffer output
CP_B	4	IF synthesizer charge pump output
V_{CCB}	5	analog supply to IF synthesizer
IF_B	6	IF VCO main divider input
ON_B	7	IF power-on input; ON_B = HIGH means IF PLL is active
DGND	8	digital circuits ground
$\overline{E}$	9	programming bus enable input
DATA	10	programming bus data input
CLK	11	programming bus clock input
V_{DD}	12	digital circuits supply voltage
ON_A	13	RF power-on input; ON_A = HIGH means RF PLL is active
AGND	14	analog circuits ground
RF_A	15	RF VCO main divider input
V_{CCA}	16	analog supply to RF synthesizer
CP_A	17	RF synthesizer charge pump output
$\overline{XOUT}$	18	inverting oscillator buffer output
V_{DDX}	19	supply voltage to crystal oscillator circuits
XIN	20	non-inverting crystal reference input

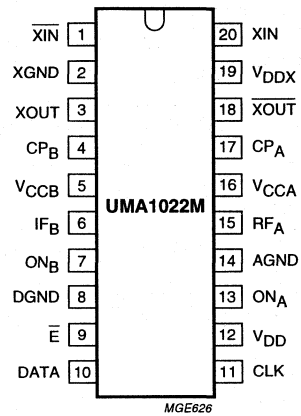


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Main dividers

The main dividers are clocked at pin RF_A by the RF oscillator signal and at pin IF_B by the IF oscillator signal. The inputs are AC coupled through external capacitors. Input impedances are high, dominated by parasitic package capacitances, so matching is off-chip. The sensitive dividers operate with signal levels from 35 to 225 mV (RMS), at frequencies from 300 MHz to 2.2 GHz (RF part) and from 50 to 500 MHz (IF part). Both include programmable bipolar prescalers followed by CMOS counters. The RF main divider allows programmable ratios from 512 to 65535; the IF blocks accept values between 128 and 16383.

Crystal oscillator

A fully differential low-noise amplifier/buffer is integrated providing outputs to drive other circuits, and to build a crystal oscillator; only needed are an external resonance circuit and tuning elements (temperature compensation). A bus controlled power-down mode disables the low-noise amplifier to reduce current if not needed.

The normal differential input pins drive a clock buffer to provide edges to the programmable reference divider at frequencies up to 30 MHz. The inputs are AC coupled through external capacitors, and operate with signals down to 35 mV (RMS) and up to 0.5 V (RMS).

Various crystal oscillator structures can be built using the amplifier. By coupling one output back to the appropriate input through the resonator, and decoupling the other input to ground, the second output becomes available to deliver the reference frequency to other circuits.

Reference dividers

A first common divider circuit produces an output frequency for RF or IF synthesizer phase comparison, depending on the P/A bit. It drives a second independent divider, which delivers the reference edge to the IF or RF synthesizer phase comparator. When P/A is logic 1, the output of the subdivider is connected to the RF phase comparator, whereas the output of the common divider is connected to the IF phase detector.

The phase comparators run at related frequencies with a controlled phase difference to avoid interference when in-lock. The common 10-bit section permits divide ratios from 8 to 1023; the second subdivider allows phase comparison frequency ratios between 1 and 16. Table 2 indicates how to program the corresponding bits to get the wanted ratio.

Phase comparators

The phase detectors are driven by the output edges selected by the main and reference dividers. Each generates lead and lag signals to control the appropriate charge pump. The pumps output current pulses appear at pins CP_A (RF synthesizer) and CP_B (IF synthesizer). The current pulse duration is at least equal to the difference in time of arrival of the edges from the two dividers. If the main divider edge arrives first, CP_A or CP_B sink current. If the reference divider edge arrives first, CP_A or CP_B source current. For correct PLL operation the VCOs need to have a positive frequency/voltage control slope.

The currents at CP_A and CP_B are programmed via the serial bus as multiples of an internally-set reference current. The passage into power-down mode is synchronized with respect to the phase detector to prevent output current pulses being interrupted. Additional circuitry is included to ensure that the gain of the phase comparators remains linear even for small phase errors.

Serial programming bus

A simple 3-line unidirectional serial bus is used to program the circuit. The 3 lines are DATA, clock (CLK) and enable ($\overline{E}$). The data sent to the device is loaded in bursts framed by $\overline{E}$. Programming clock edges and their appropriate data bits are ignored until $\overline{E}$ goes active LOW. The programmed information is loaded into the addressed latch when $\overline{E}$ returns HIGH. During normal operation, $\overline{E}$ should be kept HIGH. Only the last 19 bits serially clocked into the device are retained within the programming register.

Additional leading bits are ignored, and no check is made on the number of clock pulses. The NMOS-rich design uses virtually no current when the bus is inactive; power-up is initiated when enable is taken LOW, and power-down occurs a short time after enable returns HIGH. Bus activity is allowed when either synthesizer is active or in power-down (ON_A and ON_B inputs LOW) mode. Fully static CMOS registers retain programmed data whatever the power-down state, as long as the supply voltage is present.

Data format

The leading bits (dt15 to dt0) make up the data field, while the trailing three bits (ad2 to ad0) comprise an address field. The UMA1022M uses 4 of the 8 available addresses. The data format is shown in Table 1. The first bit entered is dt15, the last bit is ad0. For the divider ratios, the first bits entered (P0 and R0) are the Least Significant Bits (LSB). **This is different from previous Philips synthesizers.**

The trailing address bits are decoded on the rising edge of $\overline{E}$. This produces an internal load pulse to store the data in the addressed latch. To avoid erroneous divider ratios, the load pulse is not allowed during data reads by the frequency dividers. This condition is guaranteed by respecting a minimum $\overline{E}$ pulse width after data transfer.

The test register bits should not normally be programmed active (HIGH); normal operation requires them set LOW. When the supply voltage is established an internal power-up initialization pulse is generated to preconfigure the circuit state. Production testing does not verify that all bits are preconfigured correctly.

Power-down mode

The RF and IF synthesizers are **on** when respectively the input signal ON_A and ON_B are HIGH. When turned **on**, the dividers and phase detector are synchronized to avoid random phase errors. When turned **off**, the phase detector is synchronized to avoid interrupting charge pump pulses. The UMA1022M has a very low current consumption in the power-down mode.

Table 1 Bit allocation; note 1

FIRST IN						REGISTER BIT ALLOCATION										LAST IN		
DATA FIELD																ADDRESS		
dt15	**dt14**	**dt13**	**dt12**	**dt11**	**dt10**	**dt9**	**dt8**	**dt7**	**dt6**	**dt5**	**dt4**	**dt3**	**dt2**	**dt1**	**dt0**	**ad2**	**ad1**	**ad0**
Test bits(2)				CPI	S/D	XON(3)	X	X	X	X	P/A(4)	REFDIV2(5)				0	1	1
P0(6)	RF synthesizer main divider coefficient														P15	0	0	0
X	X	X	X	X	X	R0(6)	reference divider coefficient								R9	0	0	1
X	X	A0(6)	IF synthesizer main divider coefficient												A14	0	1	0

Notes

1. X = don't care.
2. The test bits (at address 011) should not be programmed with any other value except all zeros for normal operation.
3. Bit XON = power-on of crystal oscillator low-noise amplifier; logic 1 turns **on** circuit block.
4. Bit P/A = 1 selects the output of the reference subdivider to the RF synthesizer and the output of the common reference divider to the IF synthesizer.
5. The coefficient REFDIV2 (4 bits) selects the phase comparison ratio (1 to 16) between IF and RF synthesizers (see Table 2).
6. P0 is the LSB of the RF main divider coefficient; R0 is the LSB of the reference divider coefficient; A0 is the LSB of the IF main divider.

Table 2 Programming the coefficient REFDIV2 for reference subdivider

dt3 (LSB)	dt2	dt1	dt0 (MSB)	REFDIV2
0	0	0	0	1
1	0	0	0	2
0	1	0	0	3
1	1	0	0	4
0	0	1	0	5
1	0	1	0	6
0	1	1	0	7
1	1	1	0	8
0	0	0	1	9
1	0	0	1	10
0	1	0	1	11
1	1	0	1	12
0	0	1	1	13
1	0	1	1	14
0	1	1	1	15
1	1	1	1	16

Table 3 RF and IF synthesizer nominal charge pump currents (gain)

CPI	SINGLE/DOUBLE	I_{CPA} (μA)	I_{CPB} (μA)
0	0	400	400
0	1	800	800
1	0	1200	400
1	1	2400	800

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}, V_{DDX}	digital and crystal reference supply voltages	−0.3	+5.5	V
V_{CCA}, V_{CCB}	analog charge pump supply voltages	−0.3	+5.5	V
$V_C - V_D$	difference in voltage between analog and digital supplies	−0.3	+5.5	V
V_n	voltage			
	at pins 9 to 12	−0.3	V_{DD} + 0.3	V
	at pins 1, 3, 18 and 20	−0.3	V_{DDX} + 0.3	V
	at pins 4 and 6	−0.3	V_{CCB} + 0.3	V
	at pins 15 and 17	−0.3	V_{CCA} + 0.3	V
ΔV_{GND}	difference in voltage between any of DGND, AGND and XGND (these pins should be connected together)	−0.3	+0.3	V
P_{tot}	total power dissipation	–	150	mW
T_{stg}	IC storage temperature	−55	+125	°C
T_{amb}	operating ambient temperature	−30	+85	°C
$T_{j(max)}$	maximum junction temperature	–	150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	120	K/W

CHARACTERISTICS

All values refer to the typical measurement circuit; $V_{DD} = V_{DDX} = 2.7$ to 5.5 V; $V_{CCA} = V_{CCB} = 2.7$ to 5.5 V; $T_{amb} = 25\ ^{\circ}C$; unless otherwise specified. Characteristics for which only a typical value is given are not tested.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies; pins 5, 12, 16 and 19						
V_{DD}, V_{DDX}	digital and crystal reference supply voltages	$V_{DD} = V_{DDX}$; V_{CCA} and $V_{CCB} \geq V_{DD}$	2.7	–	5.5	V
V_{CCA}, V_{CCB}	charge pump supply voltages	V_{CCA} and $V_{CCB} \geq V_{DD}$	2.7	–	5.5	V
I_{DD}	synthesizer digital supply current	$V_{DD} = 5.5$ V; $\overline{E} = 0$; ON_A and $ON_B = 1$	–	1.5	2.0	mA
I_{DDX1}	reference block supply current	$V_{DDX} = 5.5$ V; XON = 0	–	0.3	0.4	mA
I_{DDX2}	crystal oscillator and buffer currents	$V_{DDX} = 5.5$ V; XON = 1	–	1.4	1.6	mA
I_{CCA}	RF synthesizer charge pump and prescaler supply currents	$V_{CCA} = 5.5$ V; $ON_B = 0$	–	7.3	8.5	mA
I_{CCB}	IF synthesizer charge pump and prescaler supply currents	$V_{CCB} = 5.5$ V; $ON_A = 0$	–	3.3	4	mA
$I_{tct(pd)}$	total supply currents ($I_{CCA(pd)} + I_{DD(pd)} + I_{CCB(pd)} + I_{DDX(pd)}$) in power-down mode	logic levels 0 V or V_{DD}; ON_A and $ON_B = 1$	–	30	60	µA
RF main divider input; pin 15						
f_{RF}	RF input frequency		300	–	2200	MHz
$V_{RF(rms)}$	AC-coupled input signal level (RMS value)	$R_s = 50\ \Omega$	35	–	225	mV
R_m	main divider ratio		512	–	65535	
Z_i	input impedance (real part)	$f_{RF} = 2$ GHz	–	60	–	Ω
C_i	pin input capacitance		–	2	–	pF
IF main divider input; pin 6						
f_{IF}	IF input frequency		50	–	500	MHz
$V_{IF(rms)}$	AC-coupled input signal level (RMS value)	$R_s = 50\ \Omega$	35	–	225	mV
R_m	main divider ratio		128	–	16383	
Z_i	input impedance (real part)	$f_{IF} = 400$ MHz	–	60	–	Ω
C_i	pin input capacitance		–	2	–	pF
Synthesizers reference divider input; pins 1 and 20						
f_{xtal}	crystal reference oscillator frequency		3	–	30	MHz
$V_{xtal(rms)}$	sinusoidal input signal level between pins 1 and 20 (RMS value)	differential	35	–	500	mV
		single-ended	35	–	250	mV
R_{refc}	common reference division ratio		8	–	1023	
R_{refa}	reference subdivider division ratio		1	–	16	
Z_i	input impedance (real part) per pin	$f_{xtal} = 10$ MHz	–	4	–	kΩ
C_i	typical pin input capacitance		–	2	–	pF
NF	small signal differential input noise figure	matched to a 4 kΩ source; XON = 1	–	4	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Phase detectors						
f_{PCmax}	maximum loop comparison frequency		–	2000	–	kHz
Charge pump outputs; pins 4 and 17						
V_{CPA}	output voltage compliance range; RF synthesizer		0.4	–	$V_{CCA} - 0.4$	V
V_{CPB}	output voltage compliance range; IF synthesizer		0.4	–	$V_{CCB} - 0.4$	V
$I_{ocp(err)}$	charge pump output current error	note 1	–25	–	+25	%
I_{match}	sink-to-source current matching		–	±5	–	%
I_{Lcp}	charge pump **off** leakage current	$V_{CPA} = ½V_{CCA}$; $V_{CPB} = ½V_{CCB}$	–5	±1	+5	nA
Phase noise						
N_{1000}	RF synthesizer's contribution to close-in phase noise of 1 GHz VCO signal at 1 kHz offset	f_{xtal} = 13 MHz; V_{xtal} = 0 dBm; f_{PC} = 200 kHz	–	–83	–	dBc/Hz
N_{1800}	RF synthesizer's contribution to close-in phase noise of 1.8 GHz VCO signal at 1 kHz offset	f_{xtal} = 13 MHz; V_{xtal} = 0 dBm; f_{PC} = 200 kHz	–	–77	–	dBc/Hz
N_{250}	IF synthesizer's contribution to close-in phase noise of 250 MHz VCO signal at 1 kHz offset	f_{xtal} = 13 MHz; V_{xtal} = 0 dBm; f_{PC} = 1000 kHz	–	–102	–	dBc/Hz
Interface logic input signal levels; pins 7, 9, 10, 11 and 13						
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	$V_{DD} + 0.3$	V
V_{IL}	LOW level input voltage		–0.3	–	$0.3V_{DD}$	V
I_{bias}	input bias current	logic 1 or logic 0	–5	–	+5	µA
C_i	input capacitance		–	2	–	pF
Low noise crystal oscillator amplifier output signals; pins 3 and 18						
Z_O	differential output impedance (real part)	f_{xtal} = 10 MHz	–	2	–	kΩ
$G_{v(diff)}$	small signal differential voltage gain	XON = 1; f_{xtal} = 10 MHz	–	20	–	dB
$V_{O(p-p)}$	limiting differential output voltage swing (peak to peak value)	XON = 1	–	2	–	V
$\Delta f/f$ (V_{CC})	frequency tolerance as a function of supply voltage change (reference to initial frequency)	note 2	–	tbf	–	ppm
$\Delta f/f$ (Z)	frequency tolerance as a function of load change (reference to initial frequency)	note 2	–	tbf	–	ppm

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
System specification						
$FTRF_{IF}$	RF frequency and close harmonics feedthrough to IF frequency	note 3	tbf	–	–	dB
$FTIF_{RF}$	IF frequency and close harmonics feedthrough to RF frequency	note 3	50	–	–	dB

Notes

1. Conditions: $0.4 < V_{CPA} < (V_{CCA} - 0.4)$ and $0.4 < V_{CPB} < (V_{CCB} - 0.4)$.
2. This value is directly dependent on the external resonator quality factor. Only guaranteed for the application circuit which is given in Fig.5.
3. Only guaranteed on the Philips application board.

SERIAL BUS TIMING CHARACTERISTICS

$V_{DD} = V_{DDX} = V_{CCA} = V_{CCB} = 3$ V; $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Serial programming clock; CLK					
t_r	input rise time	–	10	40	ns
t_f	input fall time	–	10	40	ns
T_{cy}	clock period	100	–	–	ns
Enable programming; $\overline{E}$					
t_{START}	delay to rising clock edge	100	–	–	ns
t_{END}	delay from last falling clock edge	–20	–	–	ns
$t_{W(min)}$	minimum inactive pulse width	4000[1]	–	–	ns
$t_{SU;\overline{E}}$	enable set-up time to next clock edge	20	–	–	ns
Register serial input data; DATA					
$t_{SU;DAT}$	input data to clock set-up time	20	–	–	ns
$t_{HD;DAT}$	input data to clock hold time	20	–	–	ns

Note

1. The minimum pulse width ($t_{W(min)}$) can be smaller than 4 µs when the following conditions are fulfilled:

   a) Main divider input frequency $f_{RF} > \frac{447}{t_{W(min)}}$

   b) Reference divider input frequency $f_{xtal} > \frac{3}{t_{W(min)}}$

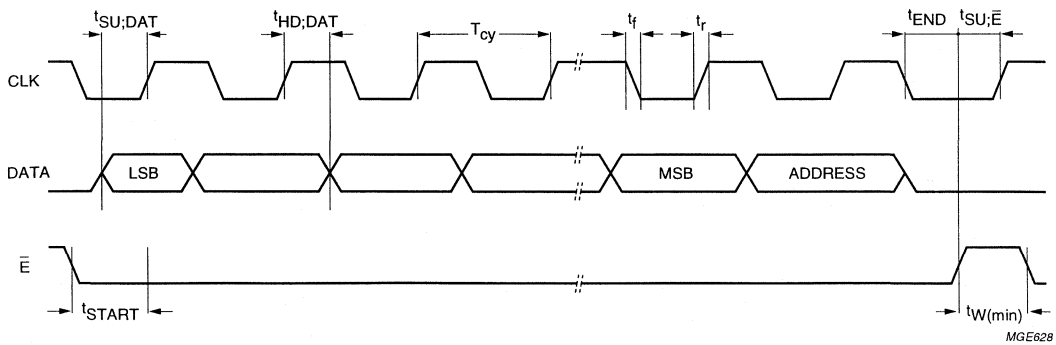


Fig.3 Serial bus timing diagram.

AC TIMING CHARACTERISTICS

$V_{DD} = V_{DDX} = V_{CCA} = V_{CCB} = 3$ V; $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
t_{PUP}	delay for initial power-up	–	tbf	–	ns
t_{PON}	delay from supply voltage to synthesizer power-on	–	–	tbf	ns
t_{START}	time to turn-on either the RF or IF synthesizer from ON_A/ON_B	–	tbf	–	ns
t_{SEND}	waiting time before sending data on the serial bus	–	–	tbf	ns
t_{LOOP}	time between the active edge of the RF signal and the current output of the charge pump	–	tbf	–	ns
t_{PWRDN}	time to turn-off either the RF or IF synthesizer from ON_A/ON_B	–	tbf	–	ns

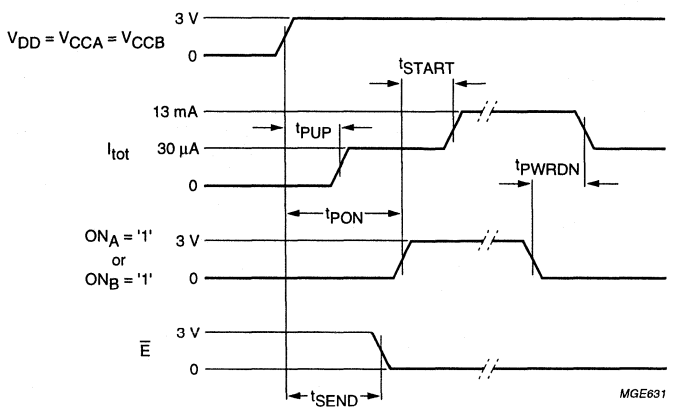
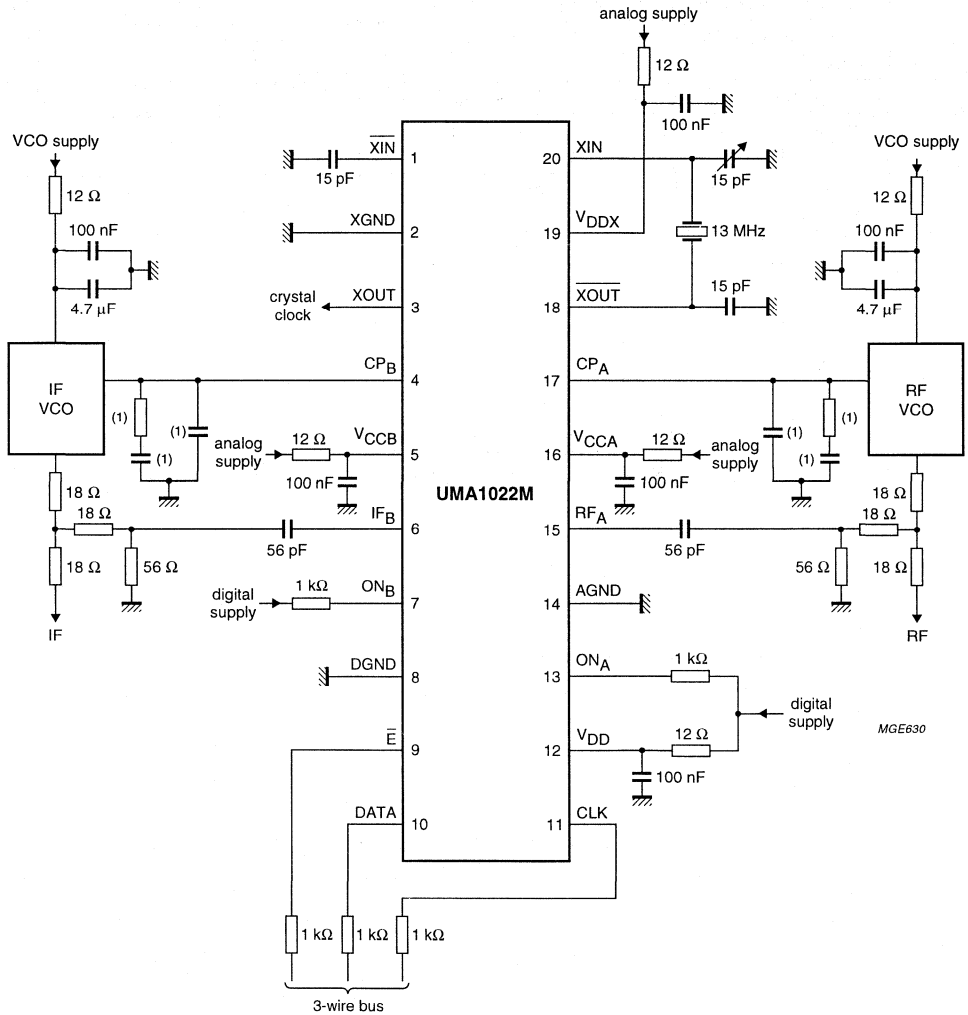


Fig.4 AC timing characteristics.

APPLICATION INFORMATION



(1) Loop filter values depend on the application.

Fig.5 Typical test and application diagram.

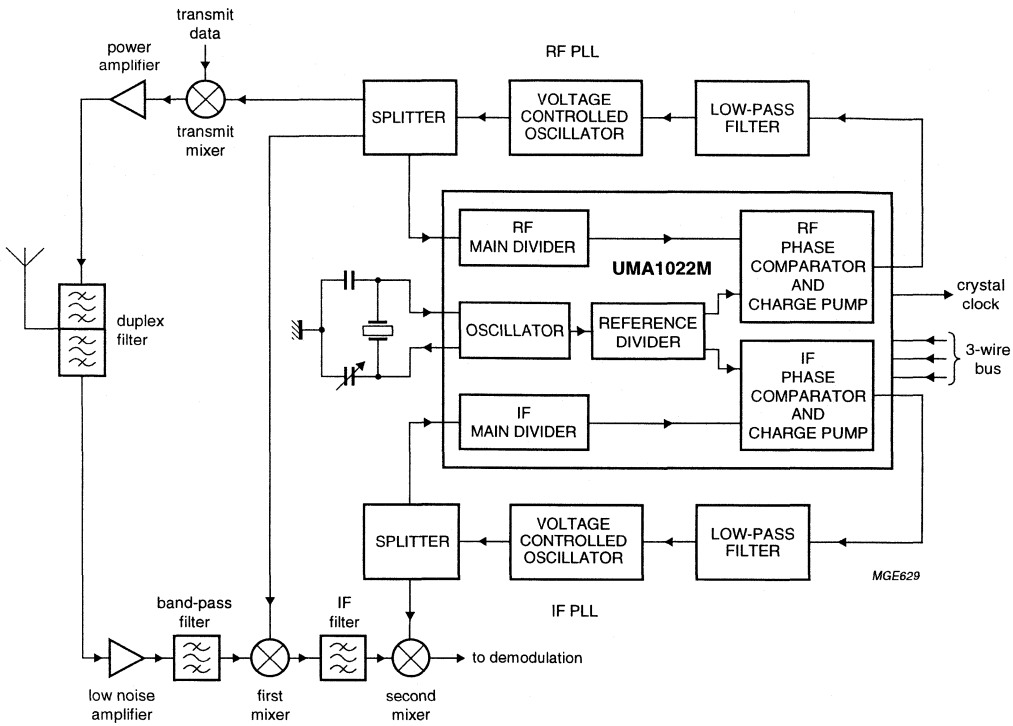


Fig.6 Application block diagram.

PACKAGE INFORMATION

	Page
Index	1950
DIP	1952
LQFP	1960
QFP	1969
SO	1974
SSOP	1981
TSSOP	1985
VSO	1988
Soldering	1990

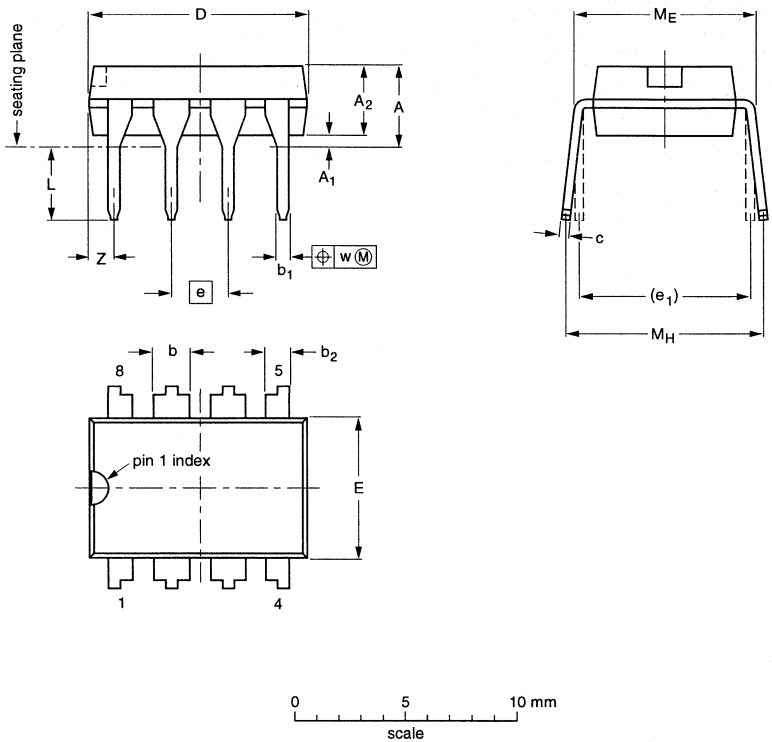
INDEX

NAME	DESCRIPTION	VERSION	PAGE
DIP (dual in-line package)			
DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1	1952
DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1	1953
DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1	1954
DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4	1955
DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1	1956
DIP24	plastic dual in-line package; 24 leads (600 mil)	SOT101-1	1957
DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1	1958
DIP40	plastic dual in-line package; 40 leads (600 mil)	SOT129-1	1959
LQFP (low profile quad flat package)			
LQFP32	plastic low profile quad flat package; 32 leads; body 7 × 7 × 1.4 mm	SOT358-1	1960
LQFP32	plastic low profile quad flat package; 32 leads; body 5 × 5 × 1.4 mm	SOT401-1	1961
LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2	1962
LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2	1963
LQFP64	plastic low profile quad flat package; 64 leads; body 7 × 7 × 1.4 mm	SOT414-1	1964
LQFP80	plastic low profile quad flat package; 80 leads; body 12 × 12 × 1.4 mm	SOT315-1	1965
LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1	1966
LQFP128	plastic low profile quad flat package; 128 leads; body 14 × 14 × 1.4 mm	SOT420-1	1967
LQFP128	plastic low profile quad flat package; 128 leads; body 14 × 20 × 1.4 mm	SOT425-1	1968
QFP (quad flat package)			
QFP44	plastic quad flat package; 44 leads (lead length 2.35 mm); body 14 × 14 × 2.2 mm	SOT205-1	1969
QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2	1970
QFP64	plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 × 20 × 2.7 mm; high stand-off height	SOT319-1	1971
QFP64	plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT319-2	1972
QFP100	plastic quad flat package; 100 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT317-2	1973
SO (small outline)			
SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1	1974
SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1	1975
SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1	1976
SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1	1977
SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1	1978
SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1	1979
SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1	1980

NAME	DESCRIPTION	VERSION	PAGE
SSOP (shrink small outline package)			
SSOP16	plastic shrink small outline package; 16 leads; body width 4.4 mm	SOT369-1	1981
SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1	1982
SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1	1983
SSOP28	plastic shrink small outline package; 28 leads; body width 5.3 mm	SOT341-1	1984
TSSOP (thin shrink small outline package)			
TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1	1985
TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1	1986
TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1	1987
VSO (very small outline)			
VSO40	plastic very small outline package; 40 leads	SOT158-1	1988
VSO56	plastic very small outline package; 56 leads	SOT190-1	1989

DIP

DIP8: plastic dual in-line package; 8 leads (300 mil) SOT97-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

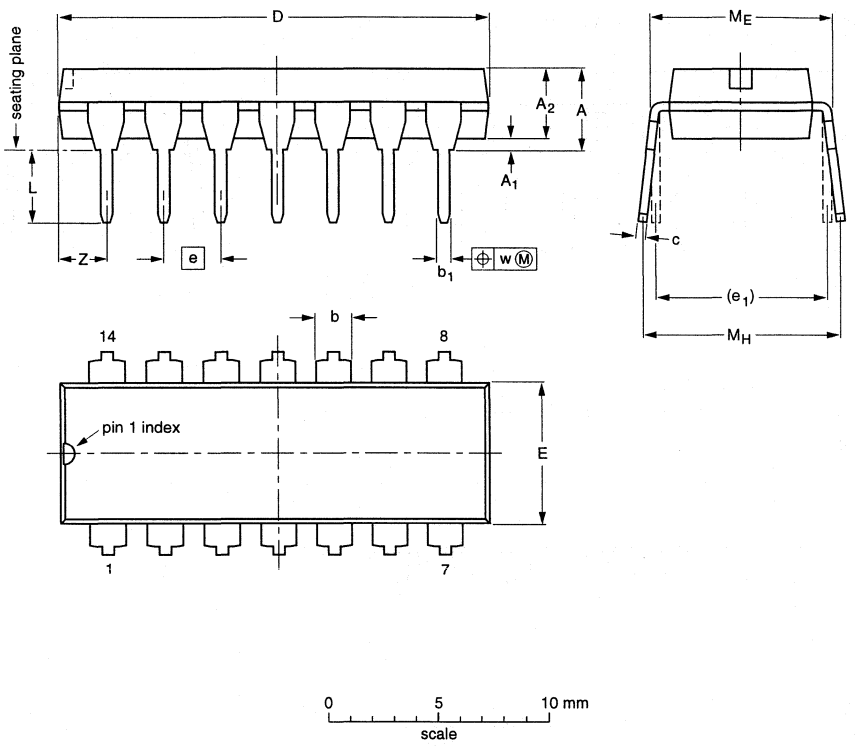
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.020	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT97-1	050G01	MO-001AN				~~92-11-17~~ 95-02-04

DIP14: plastic dual in-line package; 14 leads (300 mil) **SOT27-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

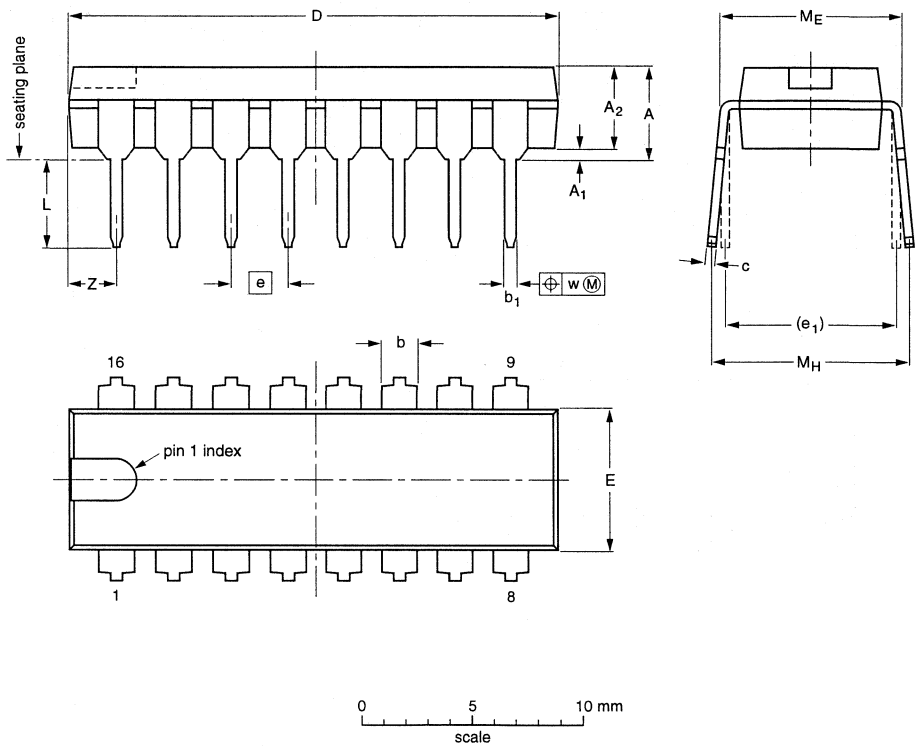
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.020	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT27-1	050G04	MO-001AA				~~92-11-17~~ 95-03-11

DIP16: plastic dual in-line package; 16 leads (300 mil); long body SOT38-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

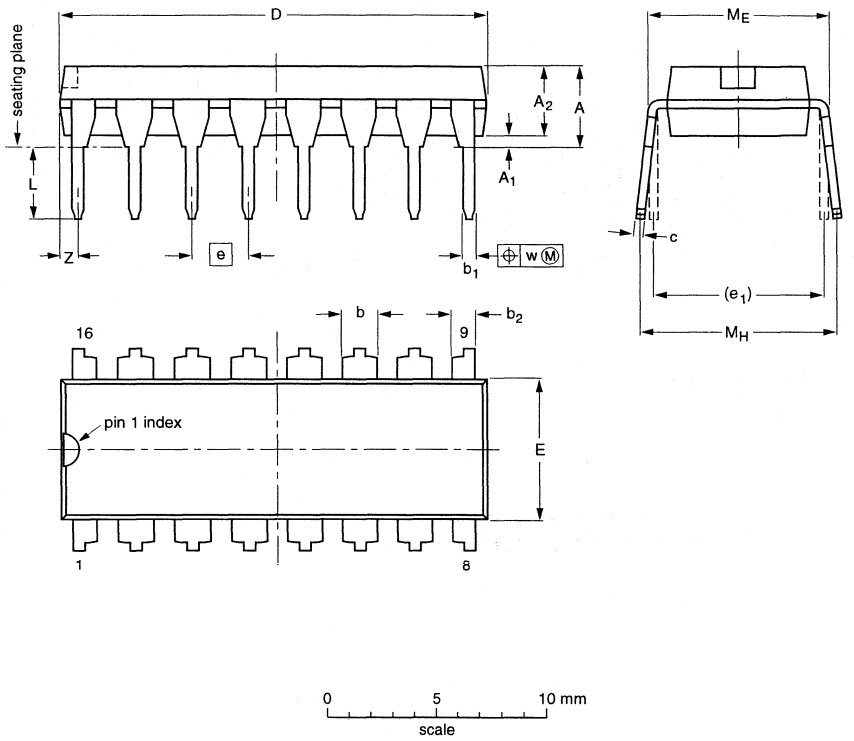
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	2.2
inches	0.19	0.020	0.15	0.055 0.045	0.021 0.015	0.013 0.009	0.86 0.84	0.26 0.24	0.10	0.30	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-1	050G09	MO-001AE				~~92-10-02~~ 95-01-19

DIP16: plastic dual in-line package; 16 leads (300 mil) SOT38-4



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

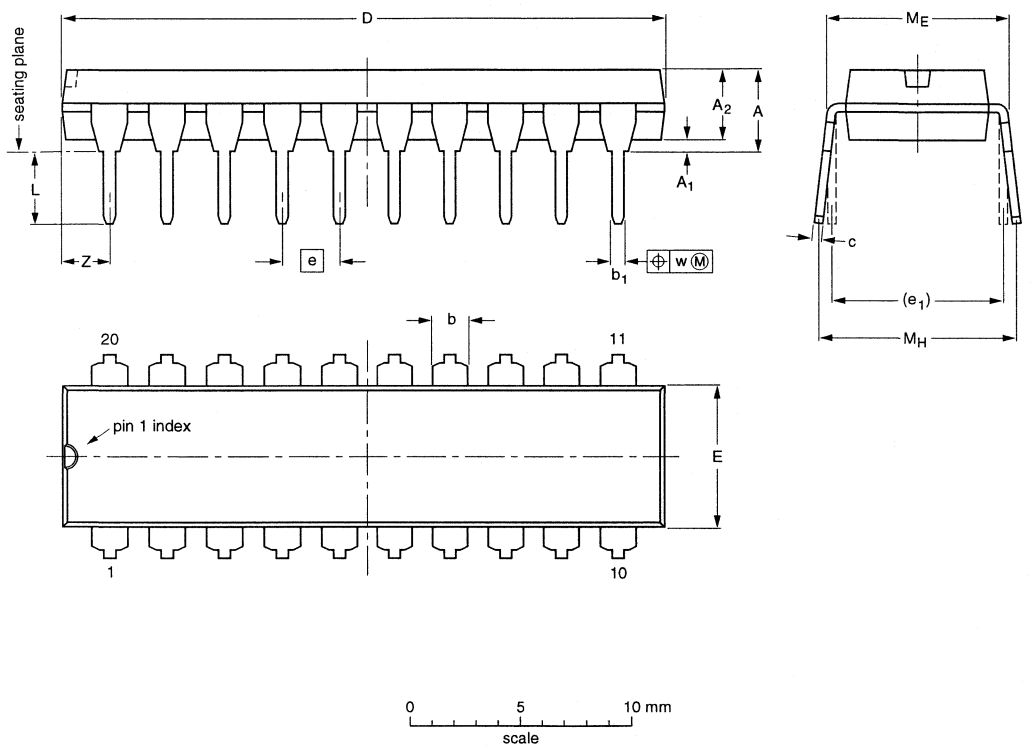
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						~~92-11-17~~ 95-01-14

DIP20: plastic dual in-line package; 20 leads (300 mil) **SOT146-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

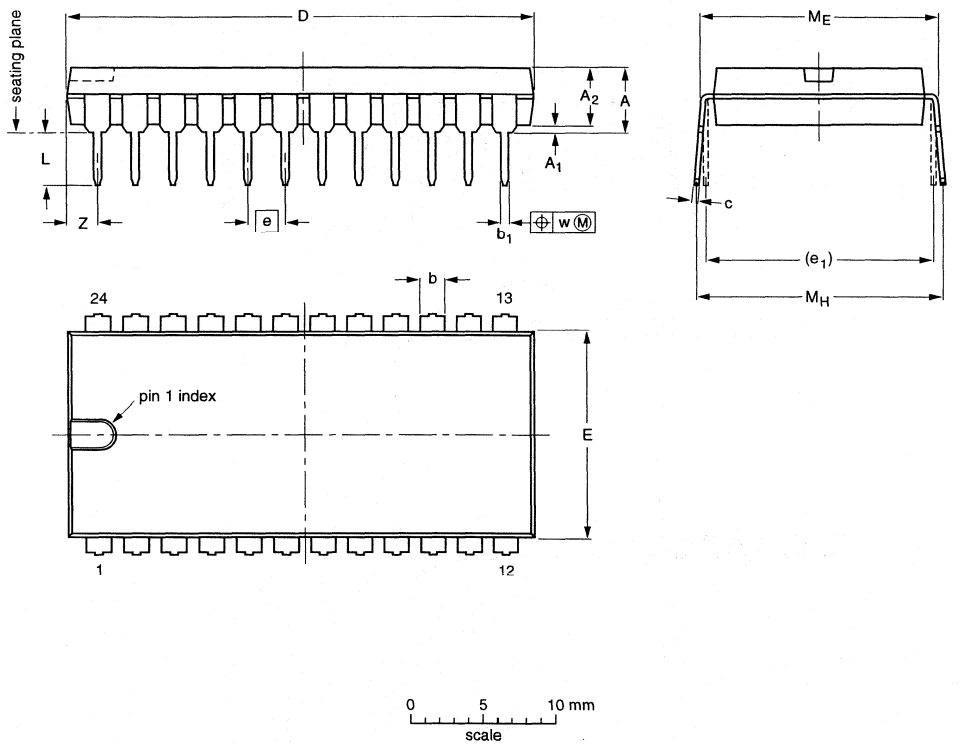
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			~~92-11-17~~ 95-05-24

DIP24: plastic dual in-line package; 24 leads (600 mil) **SOT101-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

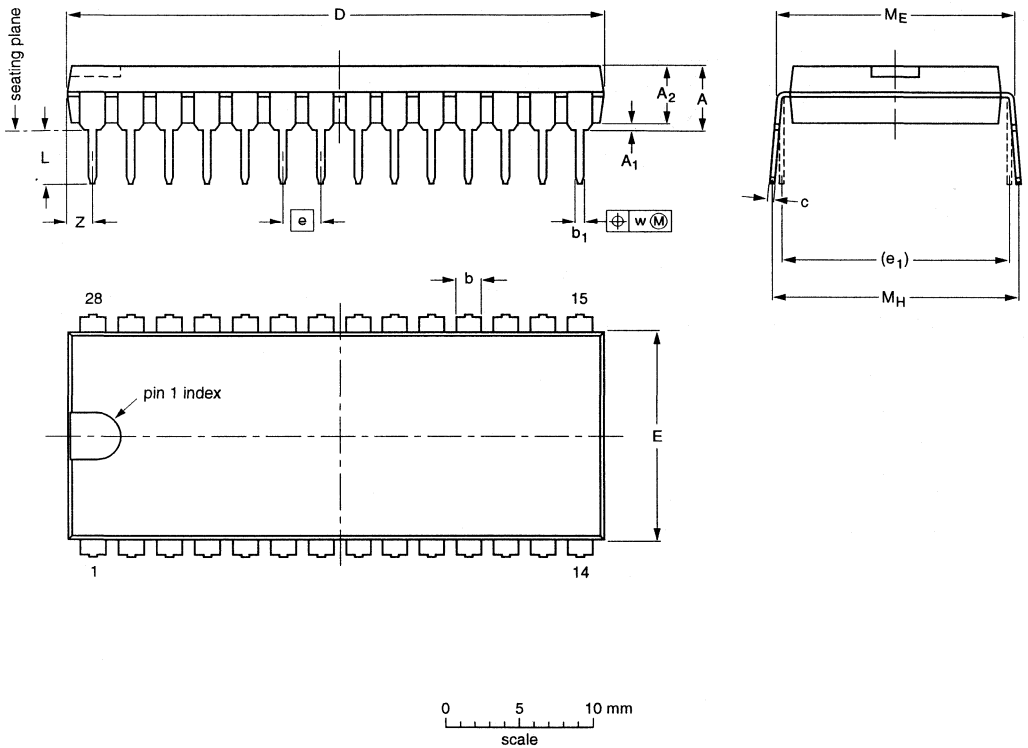
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.1	0.51	4.0	1.7 1.3	0.53 0.38	0.32 0.23	32.0 31.4	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	2.2
inches	0.20	0.020	0.16	0.066 0.051	0.021 0.015	0.013 0.009	1.26 1.24	0.56 0.54	0.10	0.60	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT101-1	051G02	MO-015AD				~~92-11-17~~ 95-01-23

DIP28: plastic dual in-line package; 28 leads (600 mil) **SOT117-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

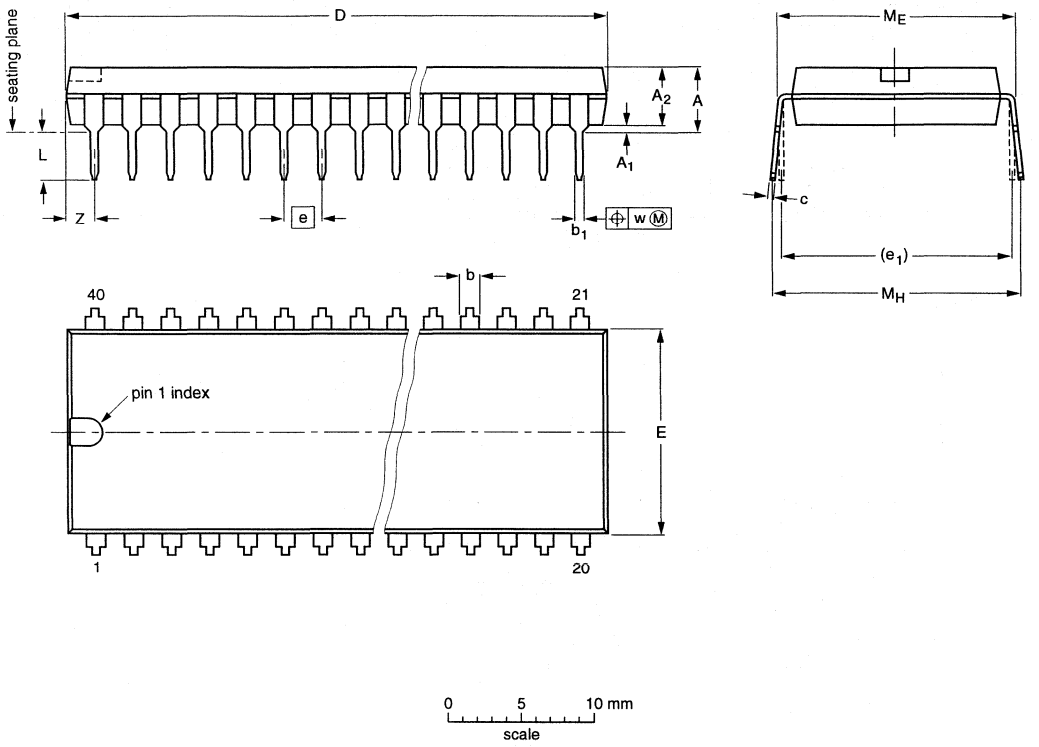
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.1	0.51	4.0	1.7 1.3	0.53 0.38	0.32 0.23	36.0 35.0	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	1.7
inches	0.20	0.020	0.16	0.066 0.051	0.020 0.014	0.013 0.009	1.41 1.34	0.56 0.54	0.10	0.60	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.067

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT117-1	051G05	MO-015AH				~~92-11-17~~ 95-01-14

DIP40: plastic dual in-line package; 40 leads (600 mil) SOT129-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	4.0	1.70 1.14	0.53 0.38	0.36 0.23	52.50 51.50	14.1 13.7	2.54	15.24	3.60 3.05	15.80 15.24	17.42 15.90	0.254	2.25
inches	0.19	0.020	0.16	0.067 0.045	0.021 0.015	0.014 0.009	2.067 2.028	0.56 0.54	0.10	0.60	0.14 0.12	0.62 0.60	0.69 0.63	0.01	0.089

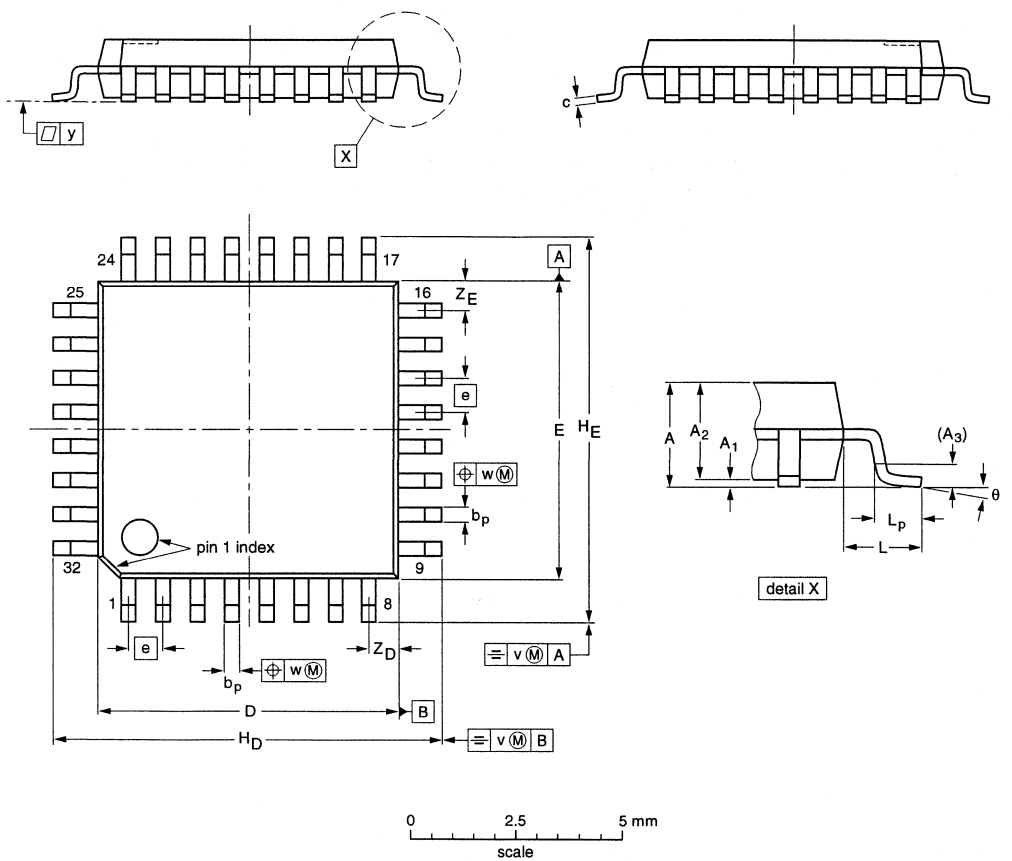
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT129-1	051G08	MO-015AJ				~~92-11-17~~ 95-01-14

LQFP

LQFP32: plastic low profile quad flat package; 32 leads; body 7 x 7 x 1.4 mm SOT358-1



DIMENSIONS (mm are the original dimensions)

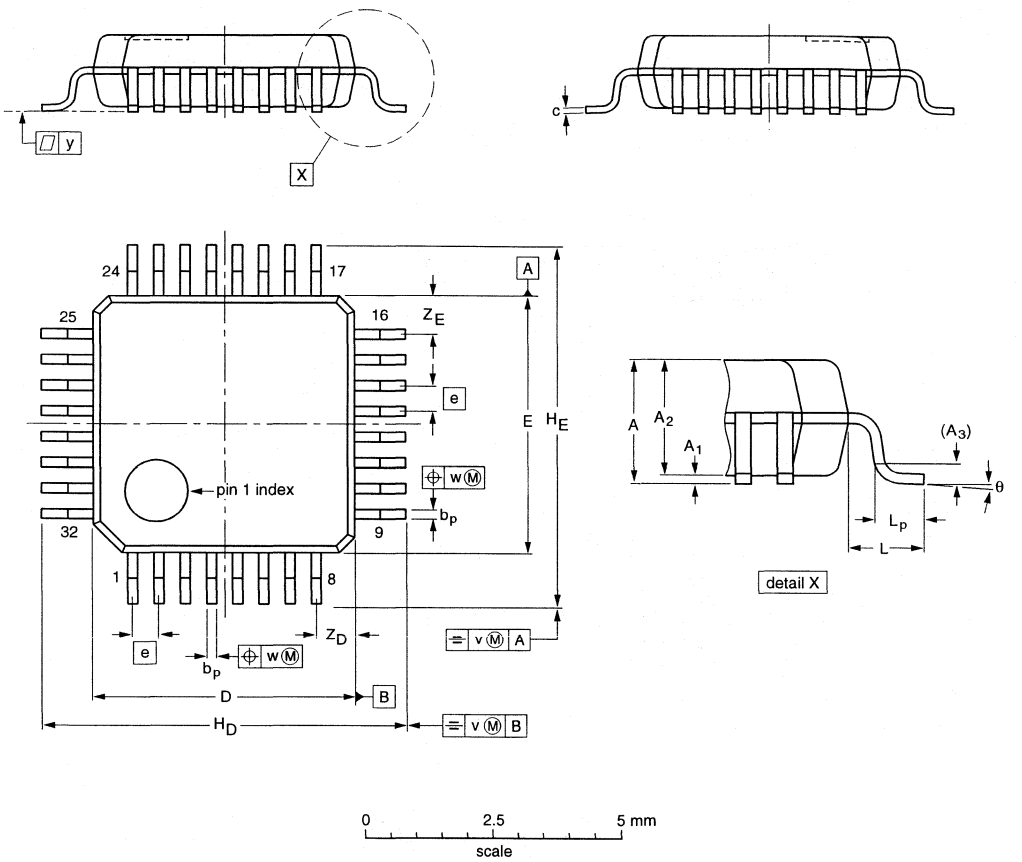
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.4 0.3	0.18 0.12	7.1 6.9	7.1 6.9	0.8	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.2	0.25	0.1	0.9 0.5	0.9 0.5	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT358 -1						~~95-12-19~~ 97-08-04

LQFP32: plastic low profile quad flat package; 32 leads; body 5 x 5 x 1.4 mm **SOT401-1**



DIMENSIONS (mm are the original dimensions)

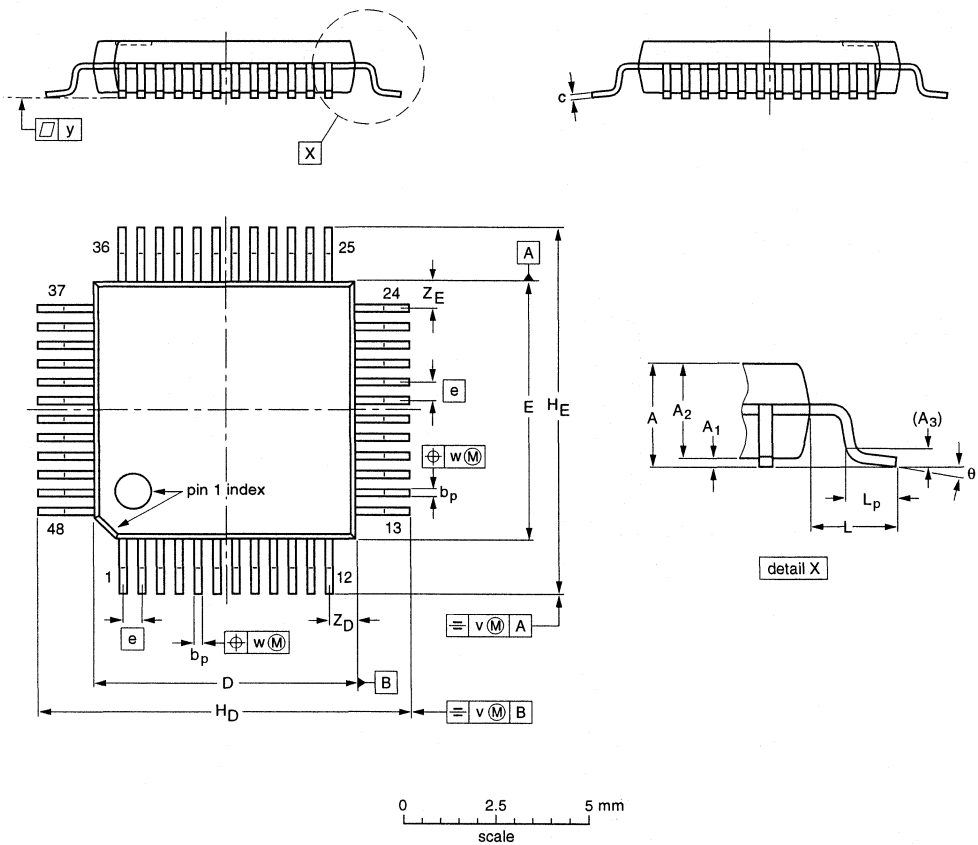
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.15 0.05	1.5 1.3	0.25	0.27 0.17	0.18 0.12	5.1 4.9	5.1 4.9	0.5	7.15 6.85	7.15 6.85	1.0	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT401-1						~~95-12-19~~ 97-08-04

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

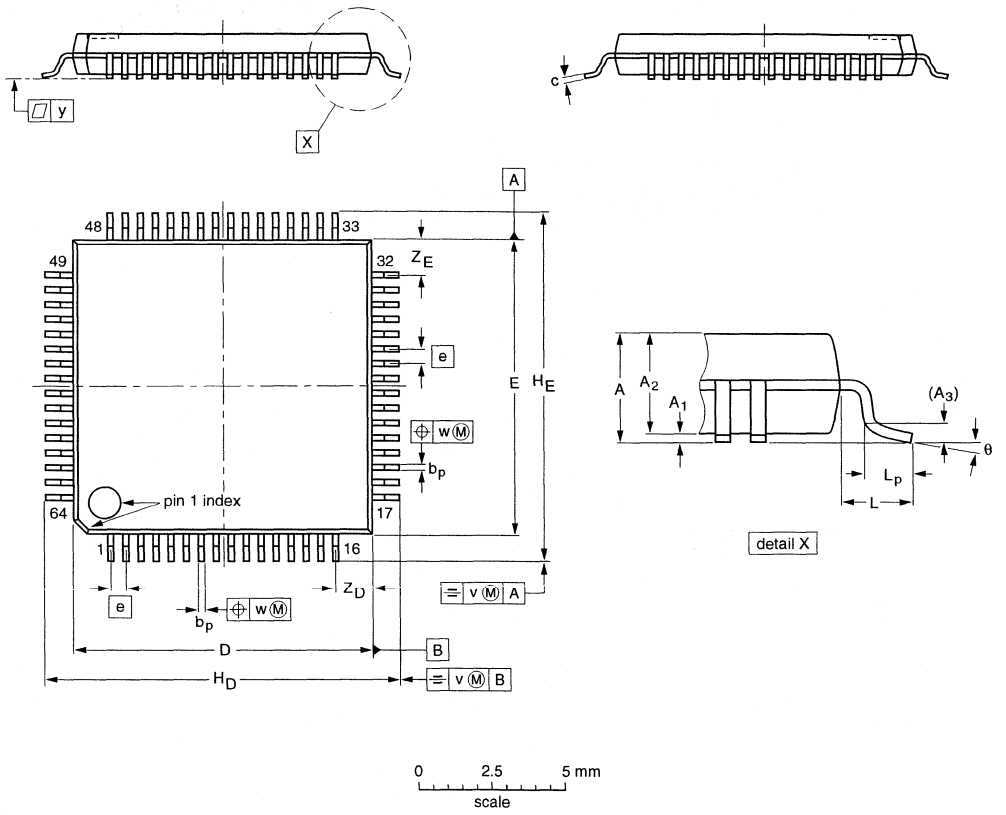
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT313-2						~~94-12-19~~ 97-08-01

LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm **SOT314-2**



DIMENSIONS (mm are the original dimensions)

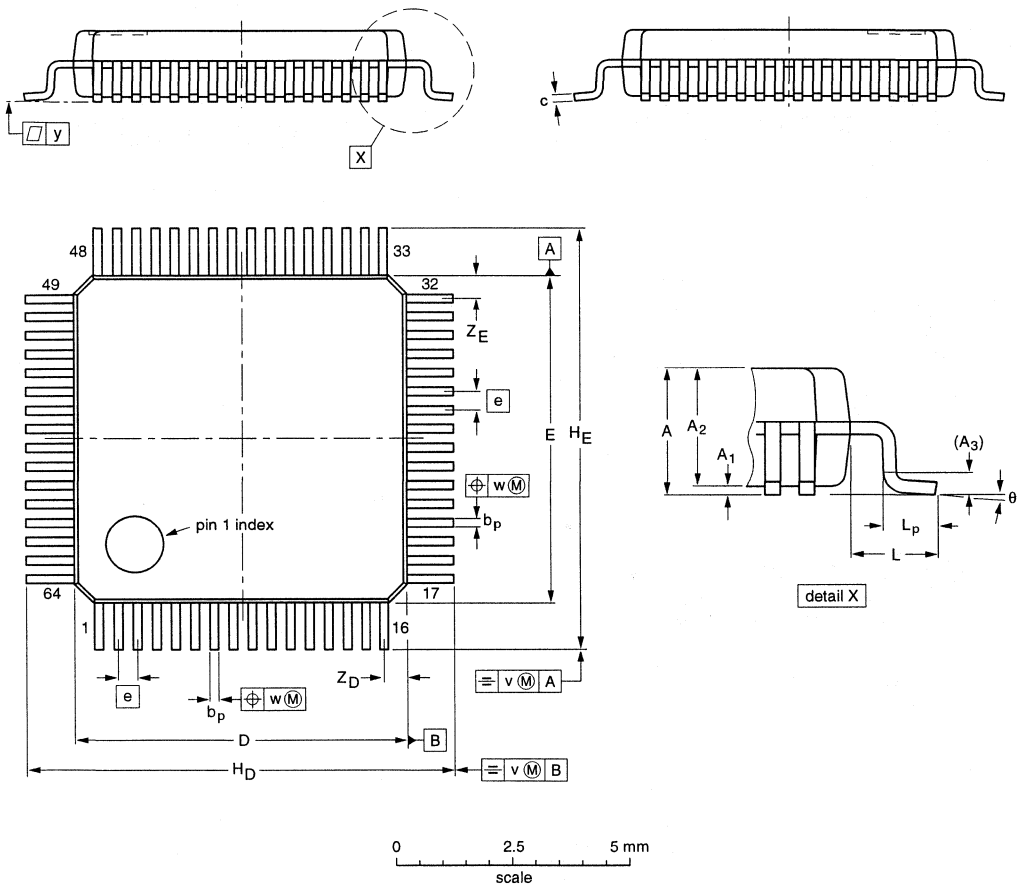
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1.0	0.75 0.45	0.2	0.12	0.1	1.45 1.05	1.45 1.05	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT314-2						~~95-12-19~~ 97-08-01

LQFP64: plastic low profile quad flat package; 64 leads; body 7 x 7 x 1.4 mm **SOT414-1**



DIMENSIONS (mm are the original dimensions)

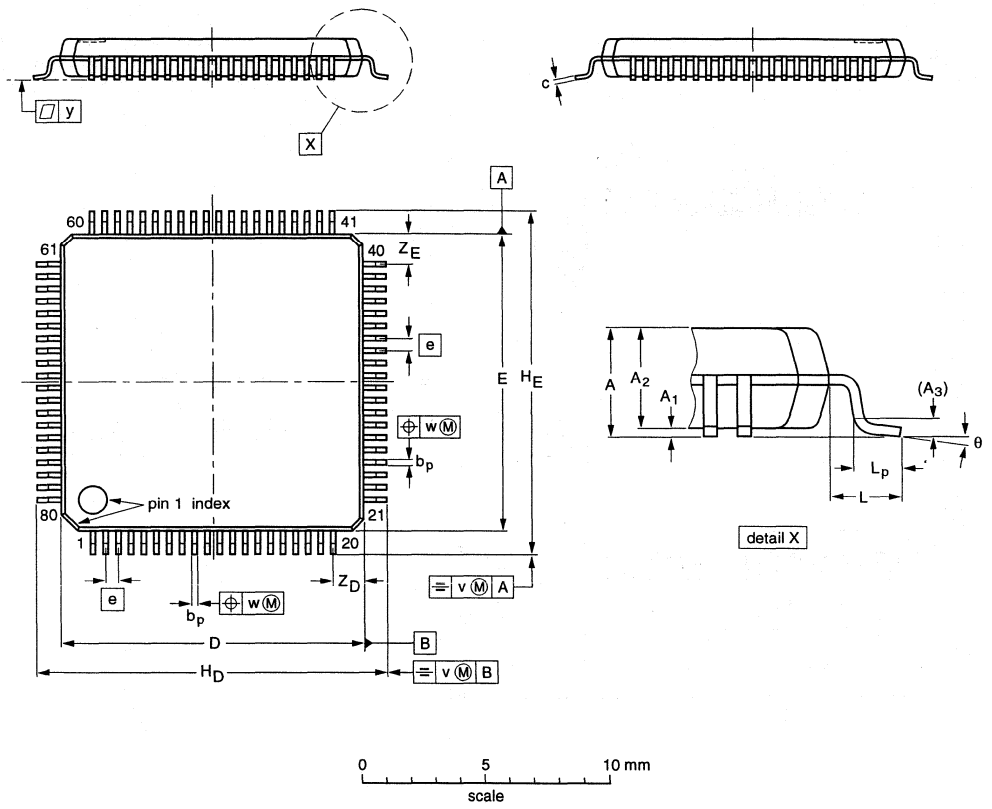
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.23 0.13	0.20 0.09	7.1 6.9	7.1 6.9	0.4	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.2	0.08	0.08	0.64 0.36	0.64 0.36	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT414-1						~~97-08-06~~ 97-08-14

LQFP80: plastic low profile quad flat package; 80 leads; body 12 x 12 x 1.4 mm **SOT315-1**



DIMENSIONS (mm are the original dimensions)

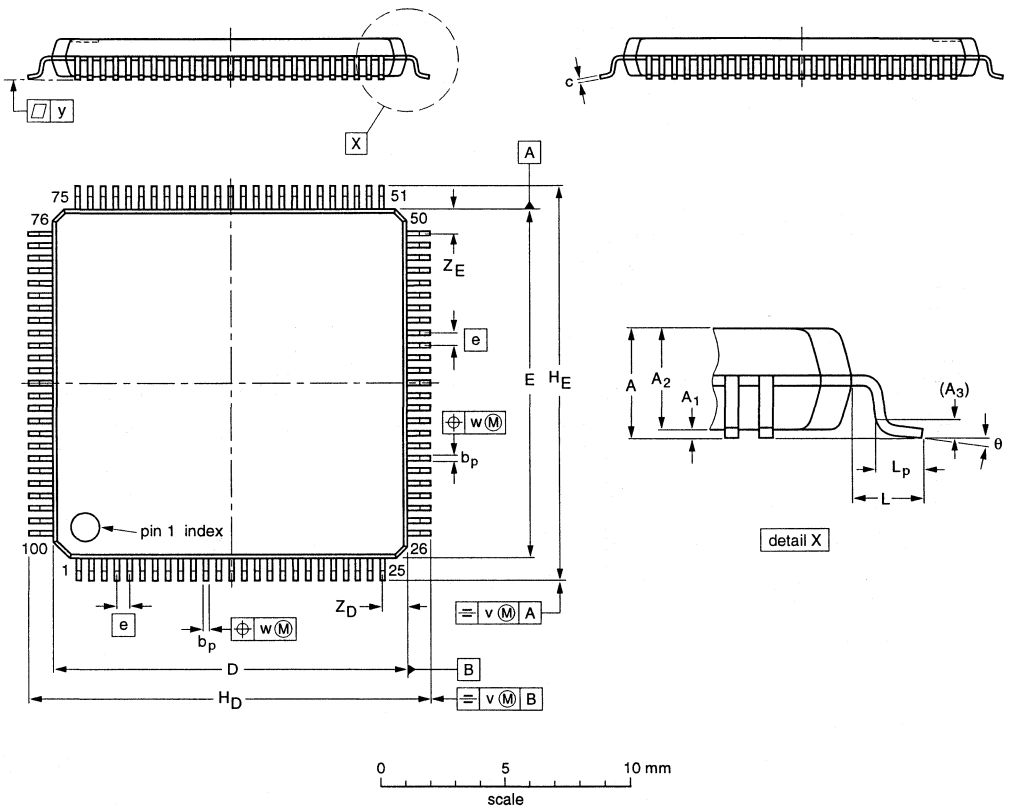
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.16 0.04	1.5 1.3	0.25	0.27 0.13	0.18 0.12	12.1 11.9	12.1 11.9	0.5	14.15 13.85	14.15 13.85	1.0	0.75 0.30	0.2	0.15	0.1	1.45 1.05	1.45 1.05	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT315-1						~~95-12-19~~ 97-07-15

LQFP100: plastic low profile quad flat package; 100 leads; body 14 x 14 x 1.4 mm **SOT407-1**



DIMENSIONS (mm are the original dimensions)

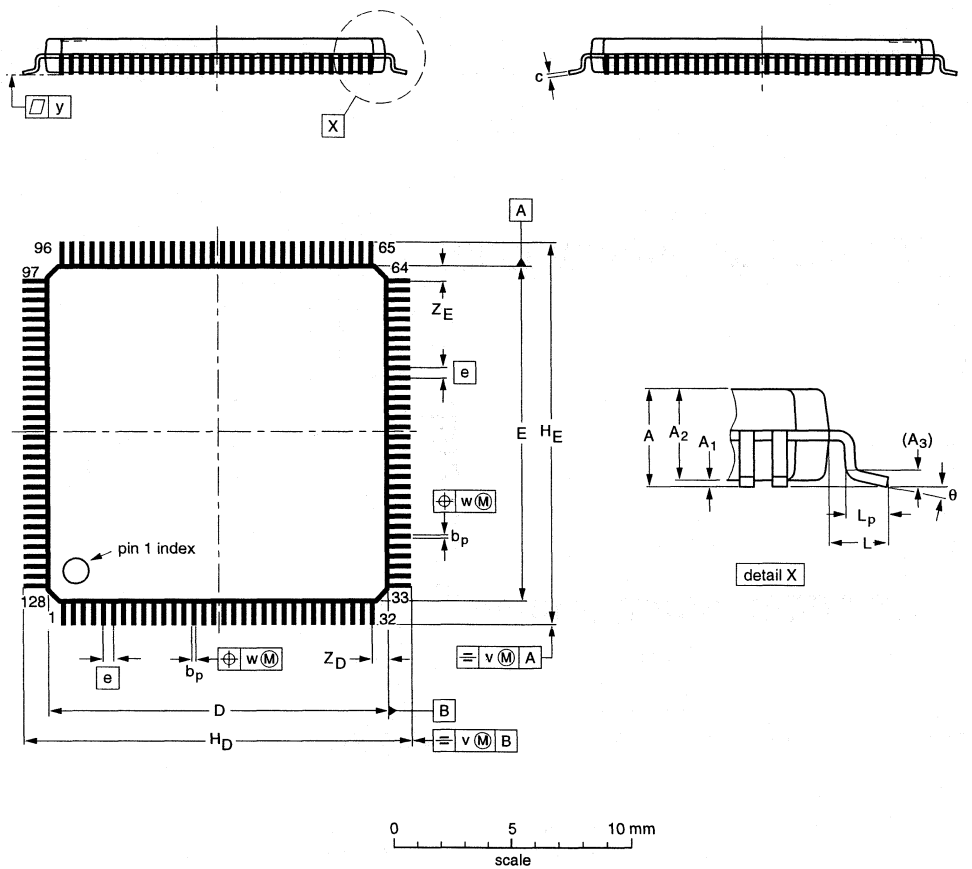
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.5 1.3	0.25	0.28 0.16	0.18 0.12	14.1 13.9	14.1 13.9	0.5	16.25 15.75	16.25 15.75	1.0	0.75 0.45	0.2	0.12	0.1	1.15 0.85	1.15 0.85	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT407-1						~~95-12-19~~ 97-08-04

LQFP128: plastic low profile quad flat package; 128 leads; body 14 x 14 x 1.4 mm **SOT420-1**



DIMENSIONS (mm are the original dimensions)

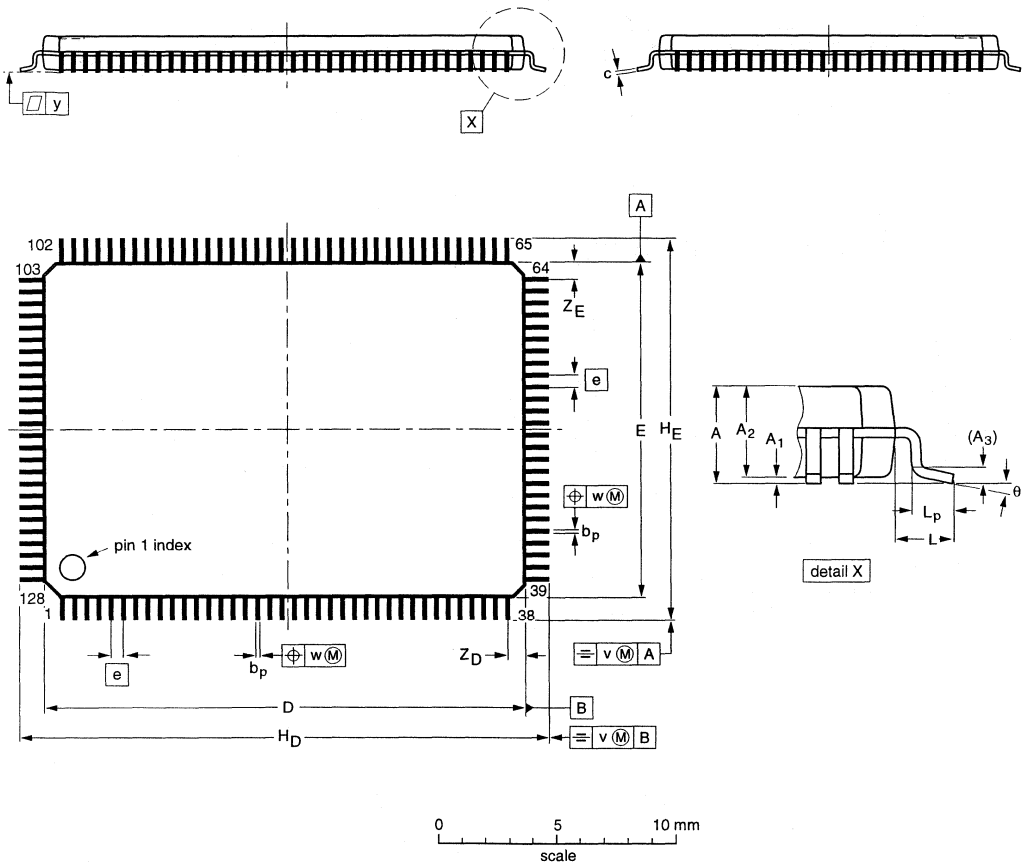
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.23 0.13	0.20 0.09	14.1 13.9	14.1 13.9	0.4	16.15 15.85	16.15 15.85	1.0	0.75 0.45	0.2	0.08	0.08	0.95 0.65	0.95 0.65	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT420-1						~~97-08-04~~ 97-08-14

LQFP128: plastic low profile quad flat package; 128 leads; body 14 x 20 x 1.4 mm **SOT425-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	20.1 19.9	14.1 13.9	0.5	22.15 21.85	16.15 15.85	1.0	0.75 0.45	0.2	0.12	0.1	0.81 0.59	0.81 0.59	7° 0°

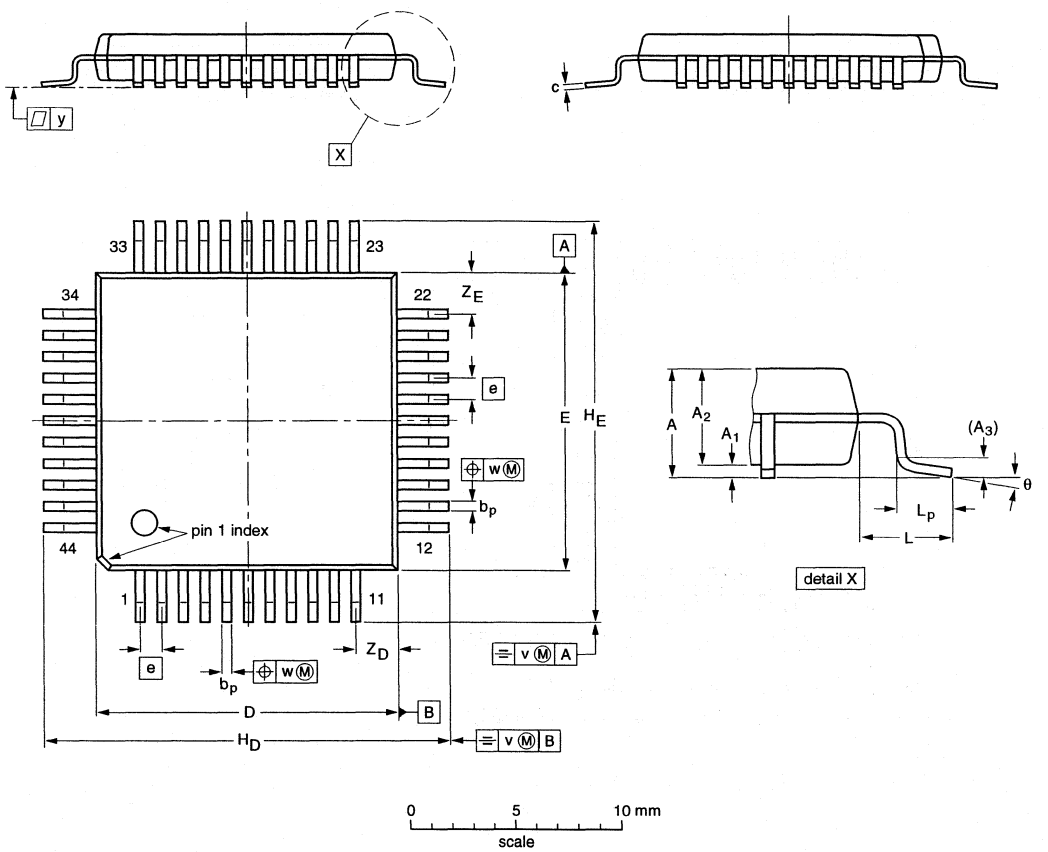
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT425-1						~~96-04-02~~ 97-08-04

QFP

QFP44: plastic quad flat package; 44 leads (lead length 2.35 mm); body 14 x 14 x 2.2 mm SOT205-1



DIMENSIONS (mm are the original dimensions)

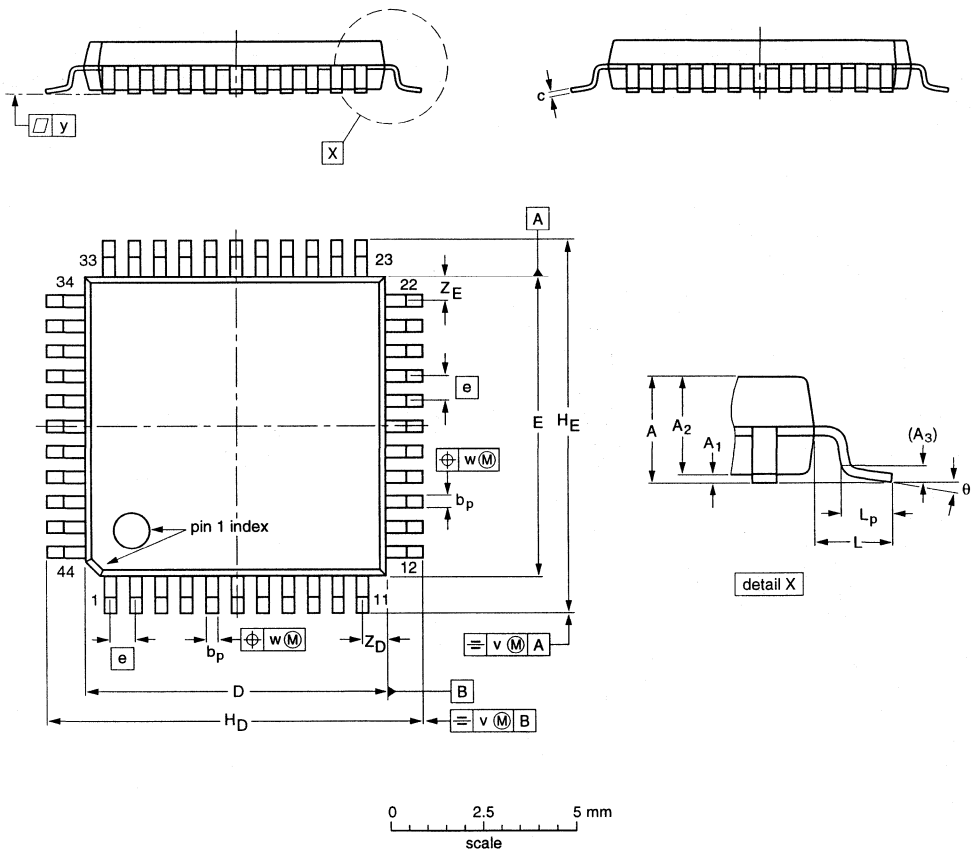
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	2.60	0.25 0.05	2.3 2.1	0.25	0.50 0.35	0.25 0.14	14.1 13.9	14.1 13.9	1	19.2 18.2	19.2 18.2	2.35	2.0 1.2	0.3	0.15	0.1	2.4 1.8	2.4 1.8	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT205-1	133E01A					~~95-02-04~~ 97-08-01

QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm **SOT307-2**



DIMENSIONS (mm are the original dimensions)

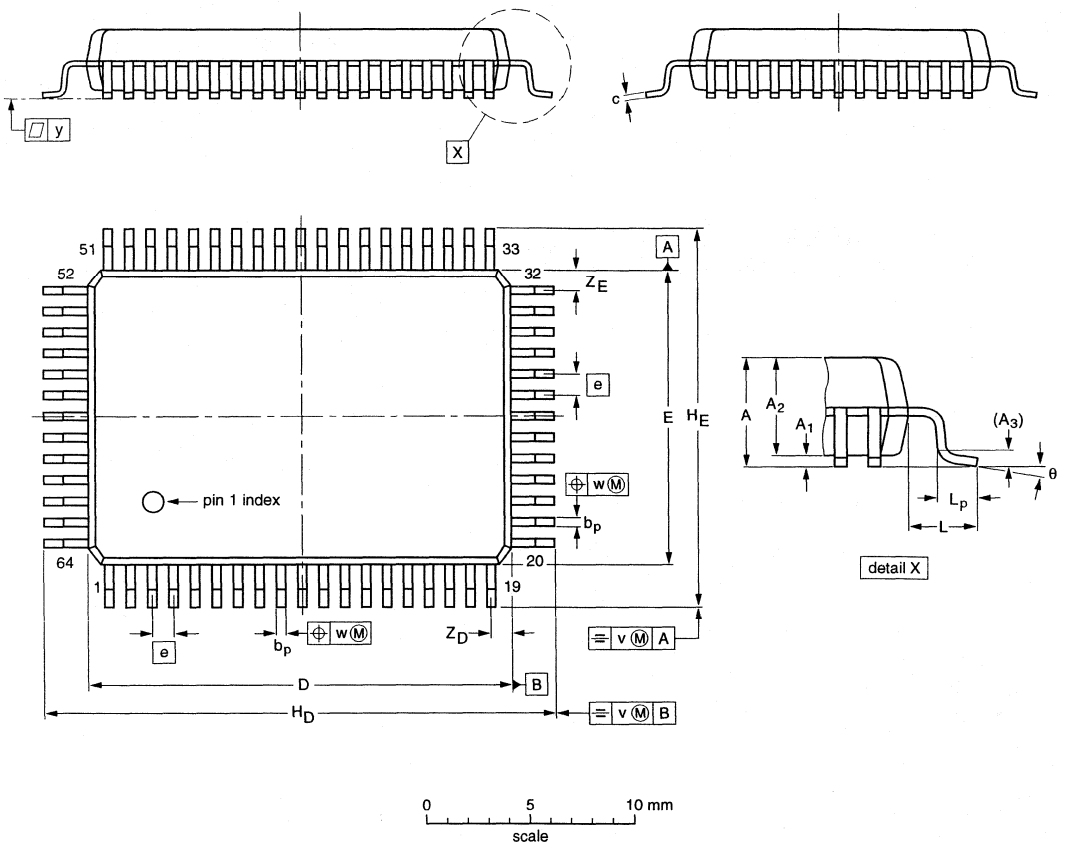
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	2.10	0.25 0.05	1.85 1.65	0.25	0.40 0.20	0.25 0.14	10.1 9.9	10.1 9.9	0.8	12.9 12.3	12.9 12.3	1.3	0.95 0.55	0.15	0.15	0.1	1.2 0.8	1.2 0.8	10° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT307-2						~~95-02-04~~ 97-08-01

QFP64: plastic quad flat package;
64 leads (lead length 1.95 mm); body 14 x 20 x 2.7 mm; high stand-off height **SOT319-1**



DIMENSIONS (mm are the original dimensions)

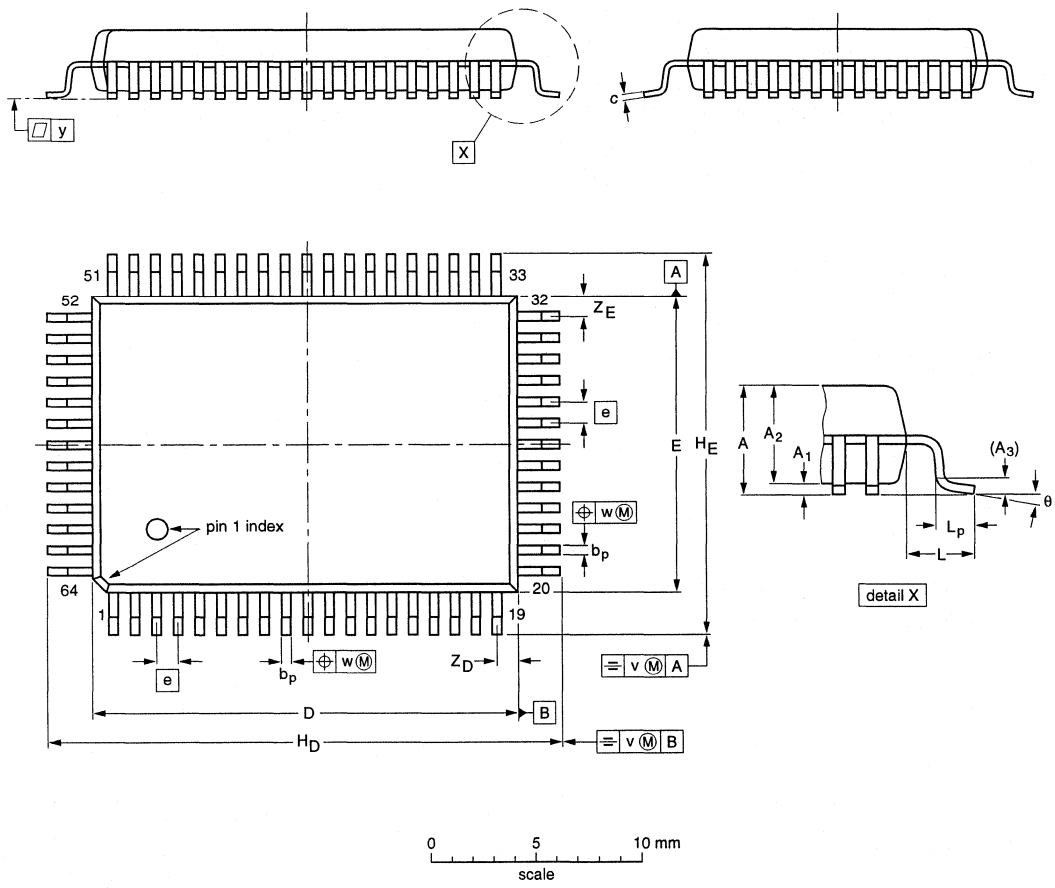
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.3	0.36 0.10	2.87 2.57	0.25	0.50 0.35	0.25 0.13	20.1 19.9	14.1 13.9	1	24.2 23.6	18.2 17.6	1.95	1.0 0.6	0.2	0.2	0.1	1.2 0.8	1.2 0.8	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT319-1						~~95-02-04~~ 97-08-01

QFP64: plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm **SOT319-2**



DIMENSIONS (mm are the original dimensions)

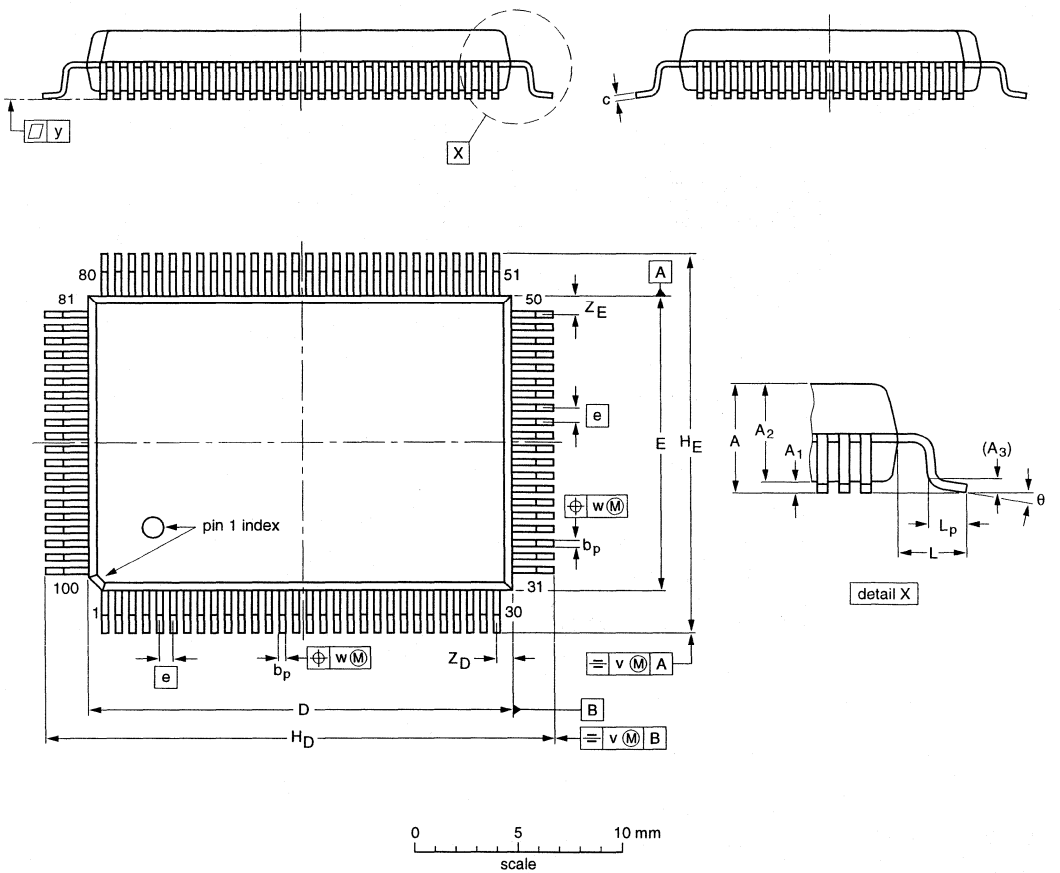
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.20	0.25 0.05	2.90 2.65	0.25	0.50 0.35	0.25 0.14	20.1 19.9	14.1 13.9	1	24.2 23.6	18.2 17.6	1.95	1.0 0.6	0.2	0.2	0.1	1.2 0.8	1.2 0.8	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT319-2						~~95-02-04~~ 97-08-01

QFP100: plastic quad flat package; 100 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm **SOT317-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.20	0.25 0.05	2.90 2.65	0.25	0.40 0.25	0.25 0.14	20.1 19.9	14.1 13.9	0.65	24.2 23.6	18.2 17.6	1.95	1.0 0.6	0.2	0.15	0.1	0.8 0.4	1.0 0.6	7° 0°

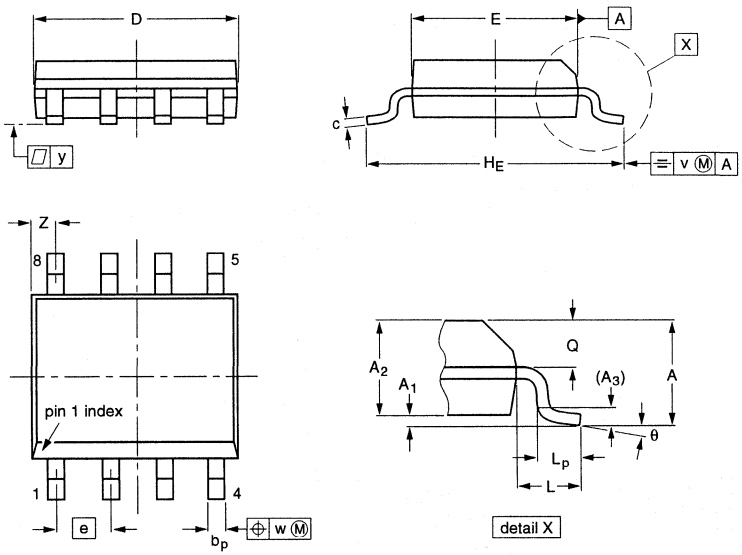
Note

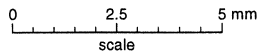
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT317-2						~~95-02-04~~ 97-08-01

SO

SO8: plastic small outline package; 8 leads; body width 3.9 mm SOT96-1





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

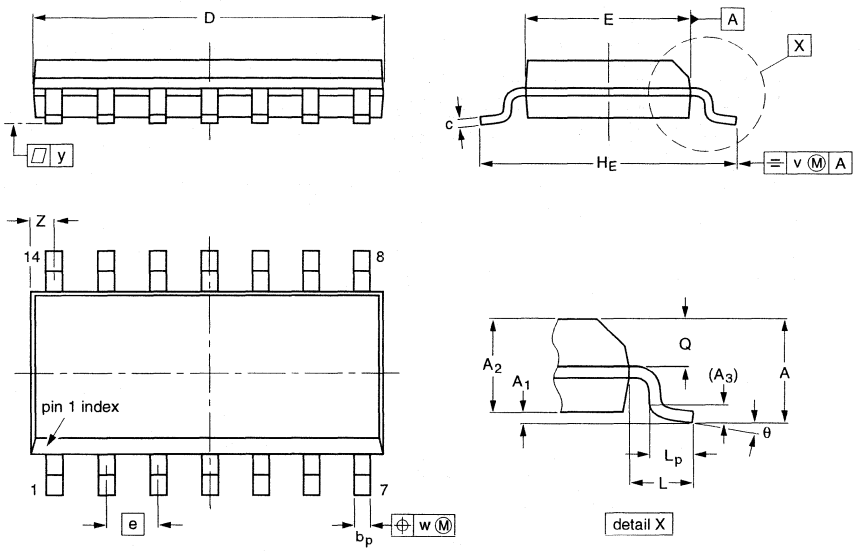
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03S	MS-012AA				~~95-02-04~~ 97-05-22

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

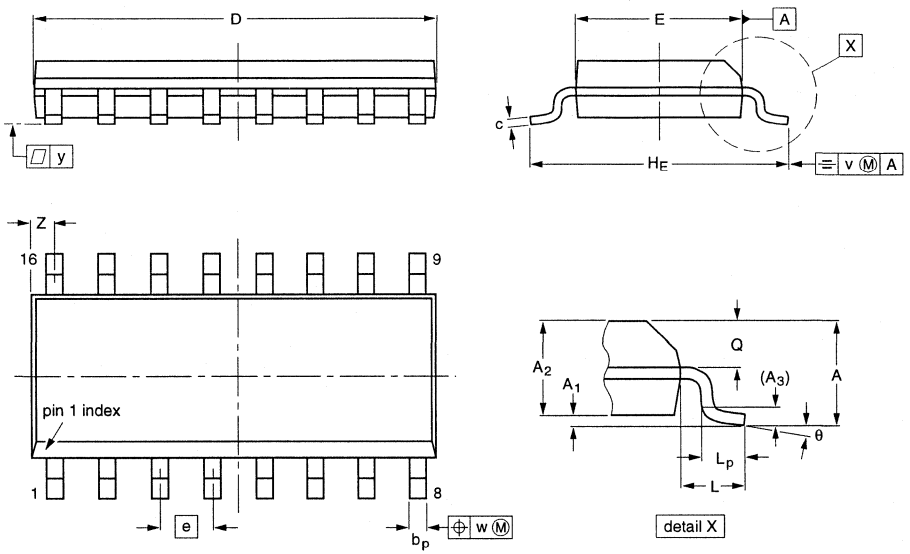
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

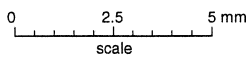
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06S	MS-012AB				~~95-01-23~~ 97-05-22

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

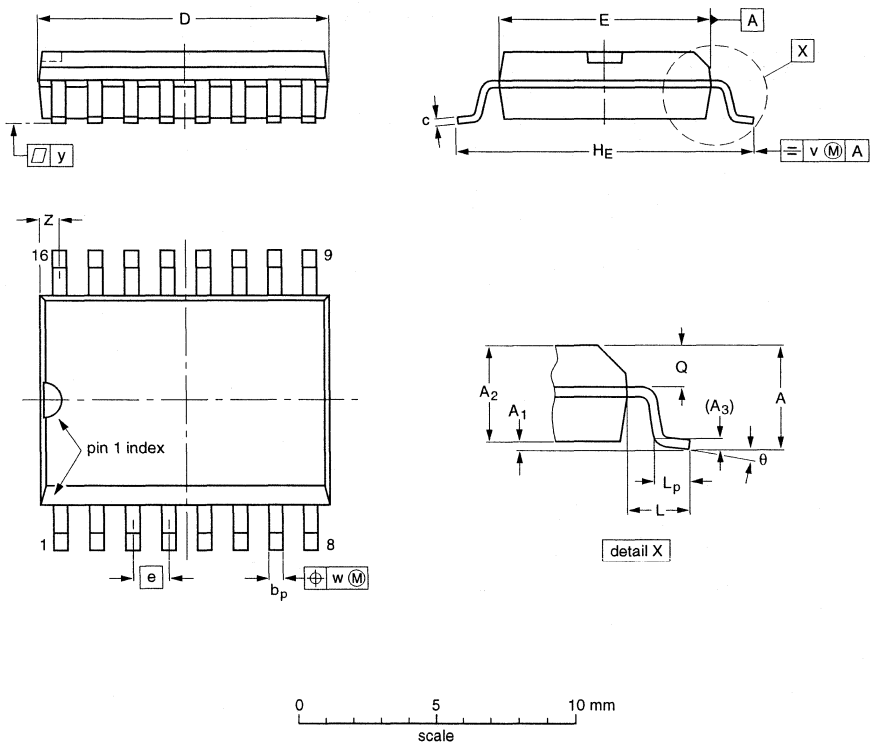
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				~~95-01-23~~ 97-05-22

SO16: plastic small outline package; 16 leads; body width 7.5 mm **SOT162-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

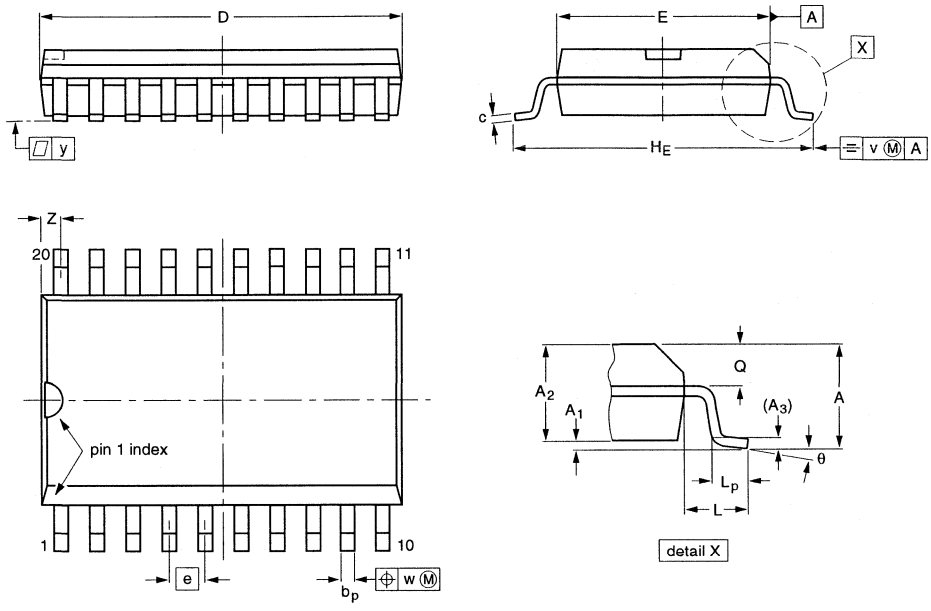
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	10.5 10.1	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.41 0.40	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT162-1	075E03	MS-013AA				~~95-01-24~~ 97-05-22

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

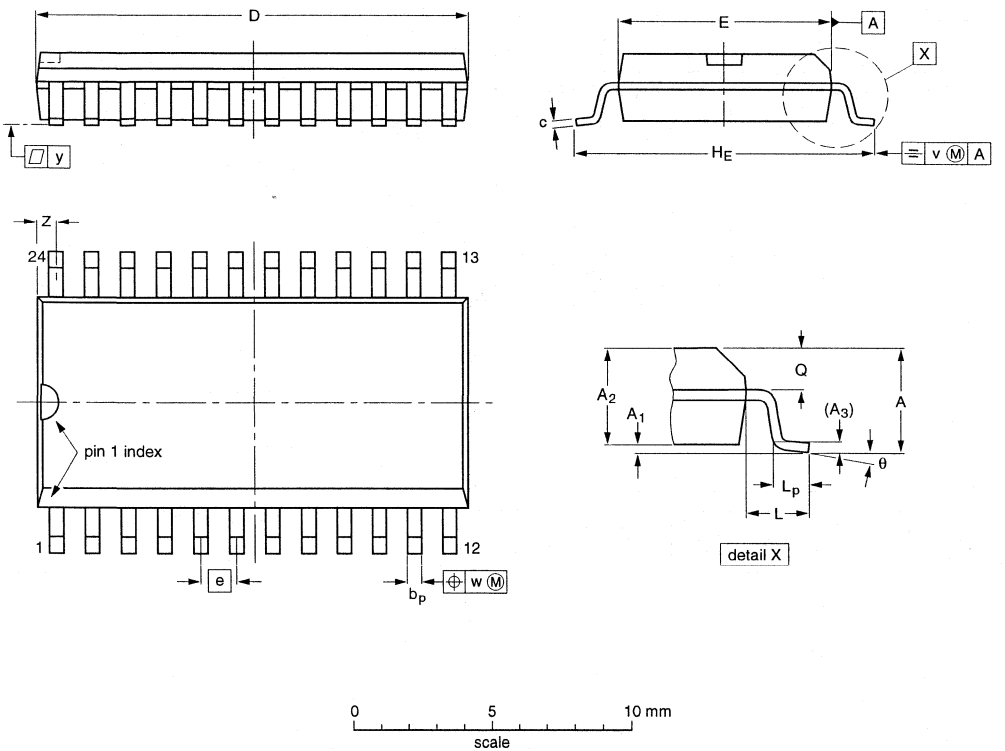
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				~~95-01-24~~ 97-05-22

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

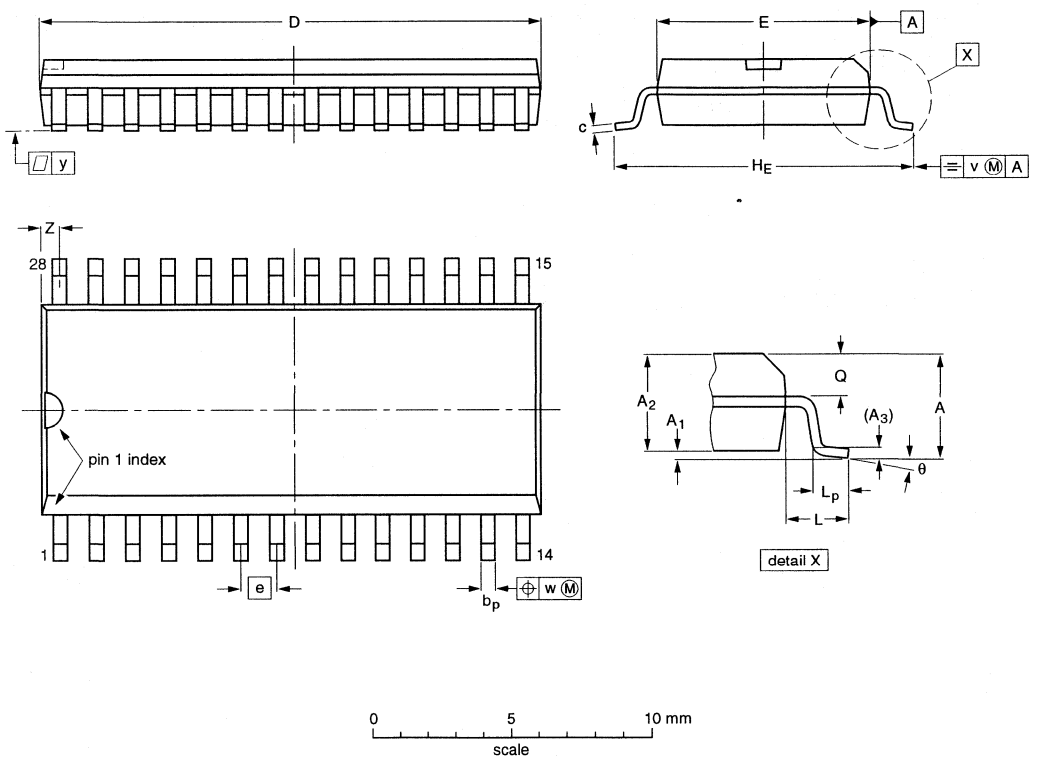
UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				~~95-01-24~~ 97-05-22

SO28: plastic small outline package; 28 leads; body width 7.5 mm **SOT136-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	18.1 17.7	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.71 0.69	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

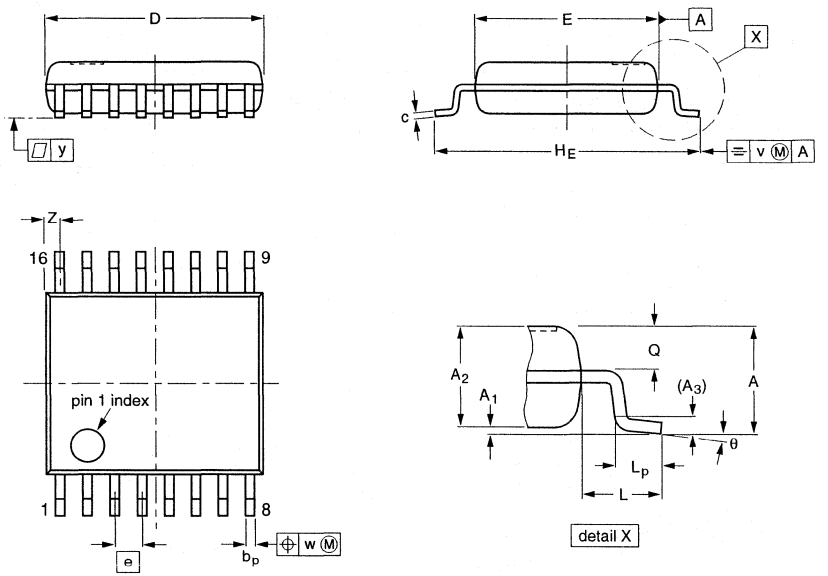
Note

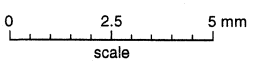
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT136-1	075E06	MS-013AE				~~95-01-24~~ 97-05-22

SSOP

SSOP16: plastic shrink small outline package; 16 leads; body width 4.4 mm SOT369-1





DIMENSIONS (mm are the original dimensions)

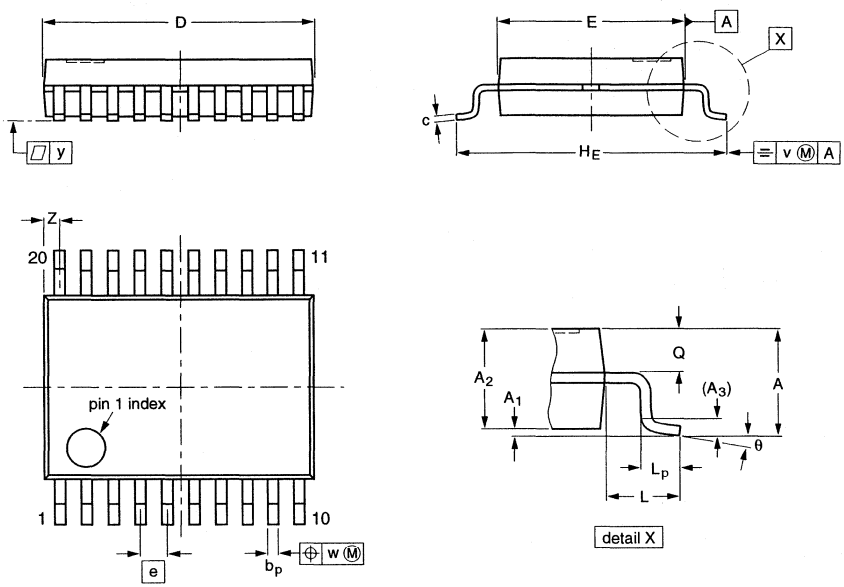
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.5	0.15 0.00	1.4 1.2	0.25	0.32 0.20	0.25 0.13	5.30 5.10	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.45	0.65 0.45	0.2	0.13	0.1	0.48 0.18	10° 0°

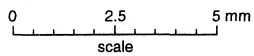
Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT369-1						~~94-04-20~~ 95-02-04

SSOP20: plastic shrink small outline package; 20 leads; body width 4.4 mm **SOT266-1**





DIMENSIONS (mm are the original dimensions)

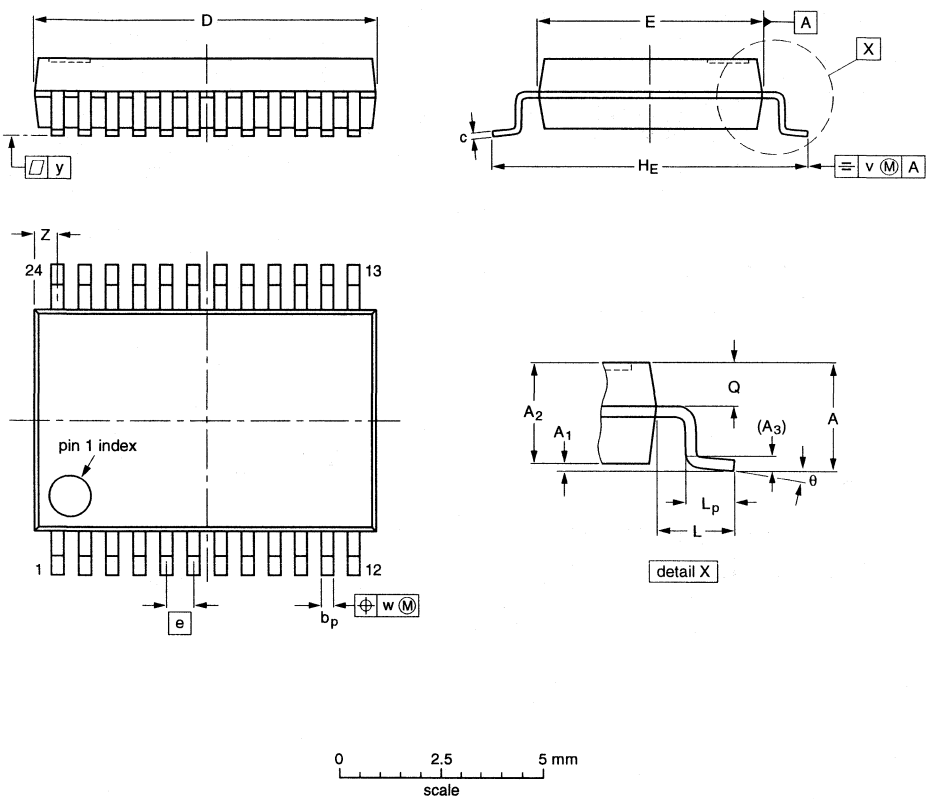
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.5	0.15 0	1.4 1.2	0.25	0.32 0.20	0.20 0.13	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.45	0.65 0.45	0.2	0.13	0.1	0.48 0.18	10° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES					EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ				
SOT266-1							~~90-04-05~~ 95-02-25

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm **SOT340-1**



DIMENSIONS (mm are the original dimensions)

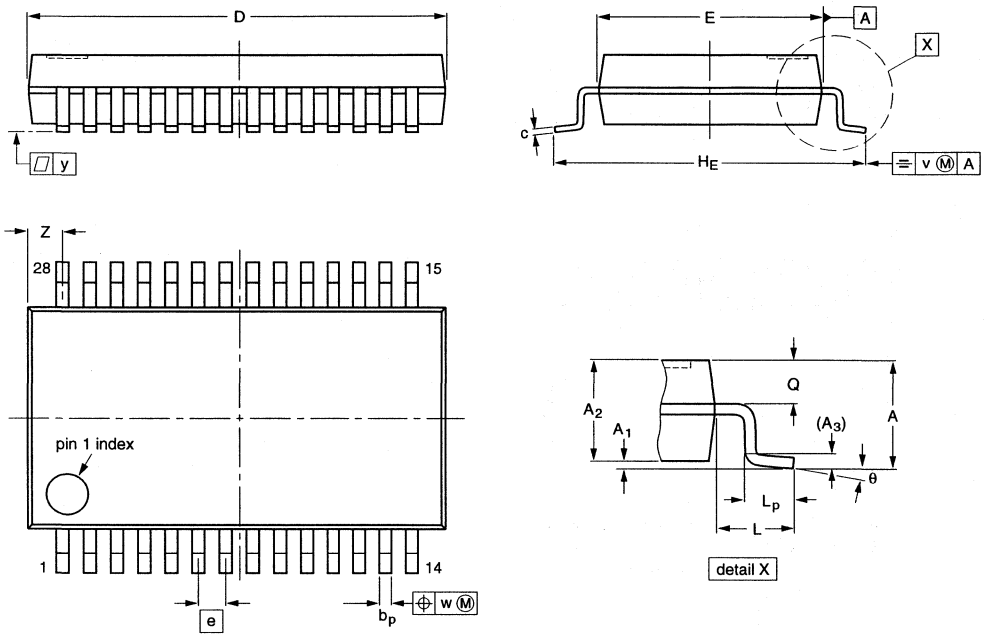
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT340-1		MO-150AG				~~93-09-08~~ 95-02-04

SSOP28: plastic shrink small outline package; 28 leads; body width 5.3 mm **SOT341-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	10.4 10.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.1 0.7	8° 0°

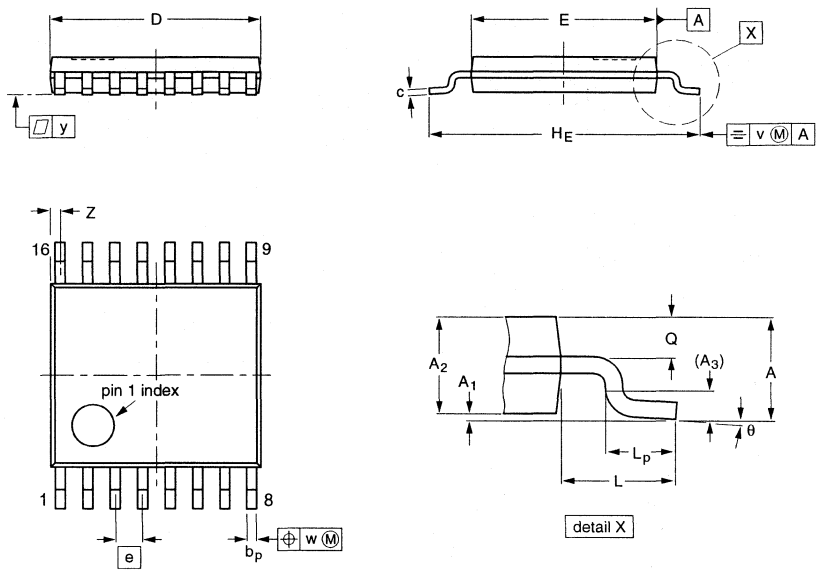
Note

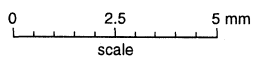
1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT341-1		MO-150AH				~~93-09-08~~ 95-02-04

TSSOP

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm SOT403-1





DIMENSIONS (mm are the original dimensions)

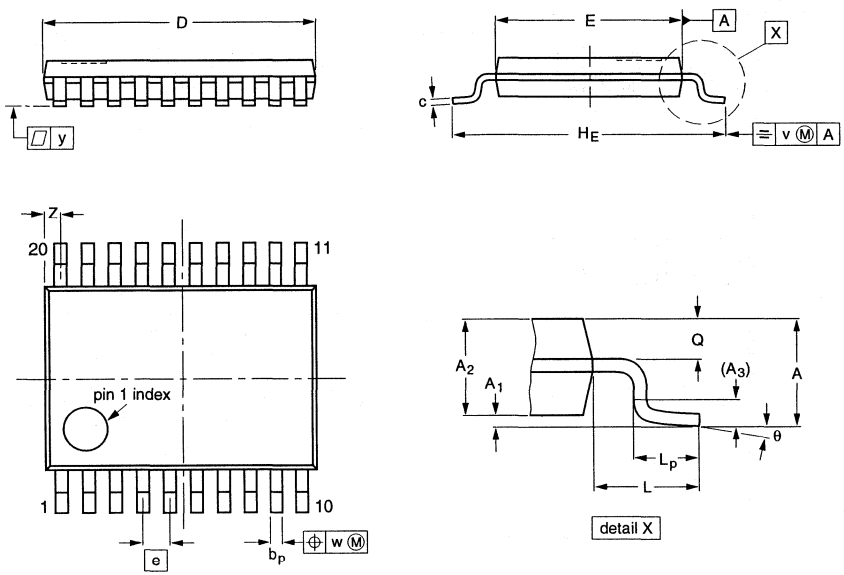
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

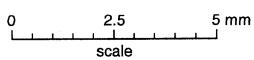
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT403-1		MO-153				~~94-07-12~~ 95-04-04

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**





DIMENSIONS (mm are the original dimensions)

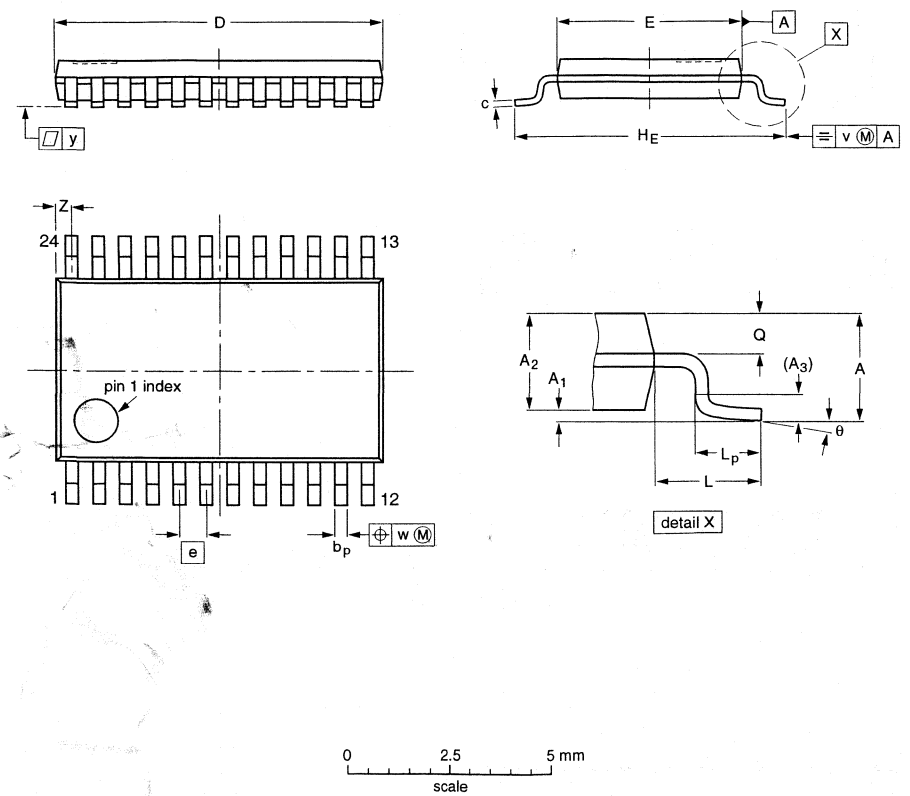
UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT360-1		MO-153AC				~~93-06-16~~ 95-02-04

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm **SOT355-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

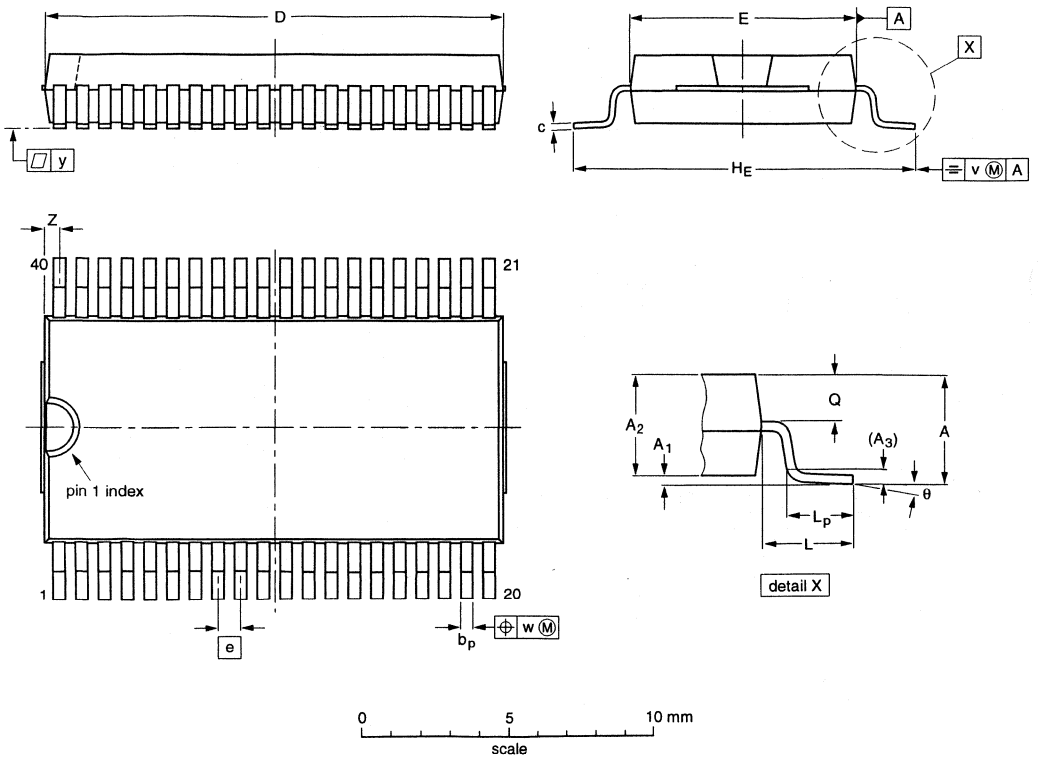
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT355-1		MO-153AD				~~93-06-16~~ 95-02-04

VSO

VSO40: plastic very small outline package; 40 leads SOT158-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

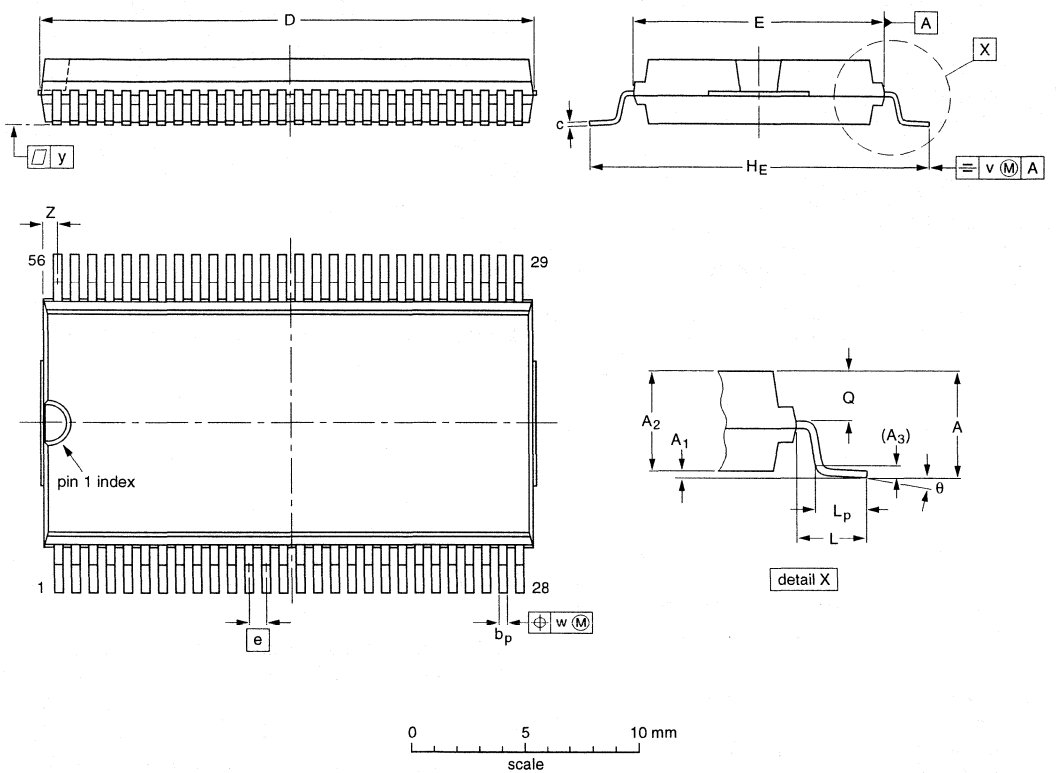
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.70	0.3 0.1	2.45 2.25	0.25	0.42 0.30	0.22 0.14	15.6 15.2	7.6 7.5	0.762	12.3 11.8	2.25	1.7 1.5	1.15 1.05	0.2	0.1	0.1	0.6 0.3	7° 0°
inches	0.11	0.012 0.004	0.096 0.089	0.010	0.017 0.012	0.0087 0.0055	0.61 0.60	0.30 0.29	0.03	0.48 0.46	0.089	0.067 0.059	0.045 0.041	0.008	0.004	0.004	0.024 0.012	

Notes

1. Plastic or metal protrusions of 0.4 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT158-1						~~92-11-17~~ 95-01-24

VSO56: plastic very small outline package; 56 leads **SOT190-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	3.3	0.3 0.1	3.0 2.8	0.25	0.42 0.30	0.22 0.14	21.65 21.35	11.1 11.0	0.75	15.8 15.2	2.25	1.6 1.4	1.45 1.30	0.2	0.1	0.1	0.90 0.55	7° 0°
inches	0.13	0.012 0.004	0.12 0.11	0.01	0.017 0.012	0.0087 0.0055	0.85 0.84	0.44 0.43	0.0295	0.62 0.60	0.089	0.063 0.055	0.057 0.051	0.008	0.004	0.004	0.035 0.022	

Note

1. Plastic or metal protrusions of 0.3 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT190-1						~~96-04-02~~ 97-08-11

INTRODUCTION

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9397 750 0011).

THROUGH-HOLE MOUNTED PACKAGES

Table 1 Types of through-hole mounted packages

TYPE	DESCRIPTION
DIP	plastic dual in-line package
SDIP	plastic shrink dual in-line package
HDIP	plastic heat-dissipating dual in-line package
DBS	plastic dual in-line bent from a single in-line package
SIL	plastic single in-line package

Soldering by dipping or wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

SURFACE MOUNTED PACKAGES

Table 2 Types of surface mounted packages

TYPE	DESCRIPTION
SO	plastic small outline package
SSOP	plastic shrink small outline package
TSSOP	plastic thin shrink small outline package
VSO	plastic very small outline package
QFP	plastic quad flat package
LQFP	plastic low profile quad flat package
SQFP	plastic shrink quad flat package
TQFP	plastic thin quad flat package
PLCC	plastic leaded chip carrier

Reflow soldering

Reflow soldering techniques are suitable for all SMD packages, ease of soldering varies with the type of package as indicated in Table 3.

The choice of heating method may be influenced by larger plastic packages (QFP or PLCC with 44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information on moisture prevention, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Table 3 Suitability of surface mounted packages for various soldering methods: rating from 'a' to 'd': **'a' indicates most suitable** (soldering is not difficult); **'d' indicates least suitable** (soldering is achievable with difficulty).

PACKAGE TYPE	REFLOW METHOD					DOUBLE WAVE METHOD
	INFRARED	HOT BELT	HOT GAS	VAPOUR PHASE	RESISTANCE	
SO	a	a	a	a	d	a
SSOP	a	a	a	c	d	c
TSSOP	b	b	b	c	d	d
VSO	b	b	a	b	a	b
QFP	b	b	a	c	a	c
LQFP	b	b	a	c	d	d
SQFP	b	b	a	c	d	d
TQFP	b	b	a	c	d	d
PLCC	c	b	b	d	d	b

Wave soldering

Wave soldering is **not** recommended for SSOP, TSSOP, QFP, LQFP, SQFP or TQFP packages, this is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- For SSOP, TSSOP and VSO packages, the longitudinal axis of the package footprint must be parallel to the solder flow **and** must incorporate solder thieves at the downstream end.
- For QFP, LQFP and TQFP packages, the footprint must be at an angle of 45° to the board direction **and** must incorporate solder thieves downstream and at the side corners.

Even with these conditions, consider wave soldering only for the following package types:

- SO
- VSO
- PLCC
- SSOP **only with body width 4.4 mm**, e.g. SSOP16 (SOT369-1) or SSOP20 (SOT266-1).
- QFP **except** QFP52 (SOT379-1), QFP100 (SOT317-1, SOT317-2, SOT382-1) and QFP160 (SOT322-1); these are **not** suitable for wave soldering.
- LQFP **except** LQFP32 (SOT401-1), LQFP48 (SOT313-1, SOT313-2), LQFP64 (SOT314-2), LQFP80 (SOT315-1); these are **not** suitable for wave soldering.
- TQFP **except** TQFP64 (SOT357-1), TQFP80 (SOT375-1) and TQFP100 (SOT386-1); these are **not** suitable for wave soldering.

SQFP are **not** suitable for wave soldering.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Data handbook system

DATA HANDBOOK SYSTEM

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SC07	Small-signal Field-effect Transistors
SC13a	PowerMOS Transistors including TOPFETs and IGBTs
SC13b	Small-signal and Medium-power MOS Transistors
SC14	RF Wideband Transistors
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DC05	Wire Wound Components

Magnetic products

MA01	Soft Ferrites
MA03	Piezoelectric Ceramics Specialty Ferrites
MA04	Dry-reed Switches

Passive components

PA01	Electrolytic Capacitors
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PA03	Potentiometers
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